CSD13380F3 12-V N-Channel FemtoFET™ MOSFET

1 Features

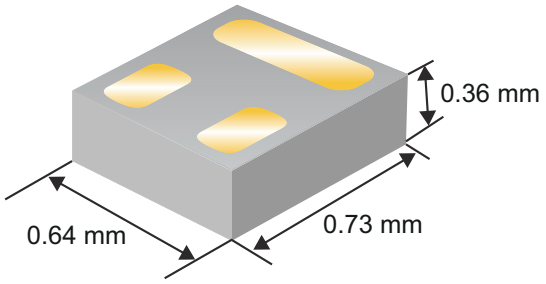
- Low on resistance
- Ultra-low Q_g and Q_{gd}
- High operating drain current
- Ultra-small footprint
  - 0.73 mm × 0.64 mm
- Low profile
  - 0.36-mm max height
- Integrated ESD protection diode
  - Rated > 3-kV HBM
  - Rated > 2-kV CDM
- Lead and halogen free
- RoHS compliant

2 Applications

- Optimized for load switch applications
- Optimized for general purpose switching applications
- Battery applications
- Handheld and mobile applications

3 Description

This 63-mΩ, 12-V N-Channel FemtoFET™ MOSFET is designed and optimized to minimize the footprint in many handheld and mobile applications. This technology is capable of replacing standard small signal MOSFETs while providing a substantial reduction in footprint size.



Typical Part Dimensions

Product Summary

T_A = 25°C		TYPICAL VALUE		UNIT
V_{DS}	Drain-to-Source Voltage	12		V
Q_g	Gate Charge Total (4.5 V)	0.91		nC
Q_{gd}	Gate Charge Gate-to-Drain	0.15		nC
$R_{DS(on)}$	Drain-to-Source On Resistance	V_{GS} = 1.8 V	96	mΩ
		V_{GS} = 2.5 V	73	
		V_{GS} = 4.5 V	63	
$V_{GS(th)}$	Threshold Voltage	0.85		V

Device Information(1)

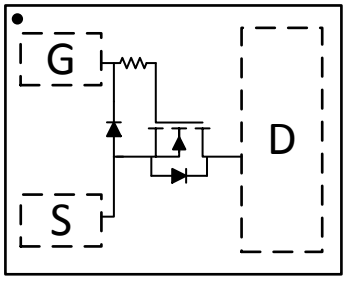
DEVICE	QTY	MEDIA	PACKAGE	SHIP
CSD13380F3	3000	7-Inch Reel	Femto 0.73 mm × 0.64 mm Land Grid Array (LGA)	Tape and Reel
CSD13380F3T	250			

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Absolute Maximum Ratings

T_A = 25°C (unless otherwise stated)		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	12	V
V_{GS}	Gate-to-Source Voltage	8	V
I_D	Continuous Drain Current(1)	3.6	A
	Continuous Drain Current(2)	2.1	
I_{DM}	Pulsed Drain Current(2) (3)	13.5	A
P_D	Power Dissipation(1)	1.4	W
	Power Dissipation(2)	0.5	
$V_{(ESD)}$	Human-Body Model (HBM)	3	kV
	Charged-Device Model (CDM)	2	
T_J, T_{stg}	Operating Junction, Storage Temperature	–55 to 150	°C

(1) Max Cu, typical $R_{\theta JA}$ = 90°C/W on 1-in^2 (6.45-cm^2), 2-oz (0.071-mm) thick Cu pad on a 0.06-in (1.52-mm) thick FR4 PCB.
(2) Min Cu, typical $R_{\theta JA}$ = 255°C/W.
(3) Pulse duration ≤ 100 µs, duty cycle ≤ 1%.



Top View

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (October 2016) to Revision A (February 2022)	Page
• Changed ultra-low profile bullet from 0.35 mm to 0.36 mm in height	1
• Updated ultra-low profile image height from 0.35 mm to 0.36 mm	1
• Changed ultra-low profile image height from 0.35 mm to 0.36 mm	8
• Added FemtoFET Surface Mount Guide note	9

5 Specifications

5.1 Electrical Characteristics

T_A = 25°C (unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0 V, I_{DS} = 250 µA	12			V
I_{DSS}	Drain-to-source leakage current	V_{GS} = 0 V, V_{DS} = 9.6 V			50	nA
I_{GSS}	Gate-to-source leakage current	V_{DS} = 0 V, V_{GS} = 8 V			25	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_{DS} = 250 µA	0.55	0.85	1.30	V
$R_{DS(on)}$	Drain-to-source on resistance	V_{GS} = 1.8 V, I_{DS} = 0.1 A		96	135	mΩ
		V_{GS} = 2.5 V, I_{DS} = 0.4 A		73	92	
		V_{GS} = 4.5 V, I_{DS} = 0.4 A		63	76	
g_{fs}	Transconductance	V_{DS} = 1.2 V, I_{DS} = 0.4 A		4.3		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input capacitance	V_{GS} = 0 V, V_{DS} = 6 V, f = 1 MHz		120	156	pF
C_{oss}	Output capacitance			81	105	pF
C_{rss}	Reverse transfer capacitance			9.6	12.5	pF
R_G	Series gate resistance			16		Ω
Q_g	Gate charge total (4.5 V)	V_{DS} = 6 V, I_{DS} = 0.4 A		0.91	1.2	nC
Q_{gd}	Gate charge gate-to-drain			0.15		nC
Q_{gs}	Gate charge gate-to-source			0.19		nC
$Q_{g(th)}$	Gate charge at V_{th}			0.15		nC
Q_{oss}	Output charge	V_{DS} = 6 V, V_{GS} = 0 V		0.81		nC
$t_{d(on)}$	Turnon delay time	V_{DS} = 6 V, V_{GS} = 4.5 V, I_{DS} = 0.4 A, R_G = 2 Ω		4		ns
t_r	Rise time			4		ns
$t_{d(off)}$	Turnoff delay time			11		ns
t_f	Fall time			3		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	I_{SD} = 0.4 A, V_{GS} = 0 V		0.71	1	V
Q_{rr}	Reverse recovery charge	V_{DS}= 6 V, I_F = 0.4 A, di/dt = 100 A/µs		2.1		nC
t_{rr}	Reverse recovery time			8		ns

5.2 Thermal Information

T_A = 25°C (unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(1)		90		°C/W
	Junction-to-ambient thermal resistance(2)		255		

(1) Device mounted on FR4 material with 1-in^2 (6.45-cm^2), 2-oz (0.071-mm) thick Cu.
(2) Device mounted on FR4 material with minimum Cu mounting area.

5.3 Typical MOSFET Characteristics

T_A = 25°C (unless otherwise stated)

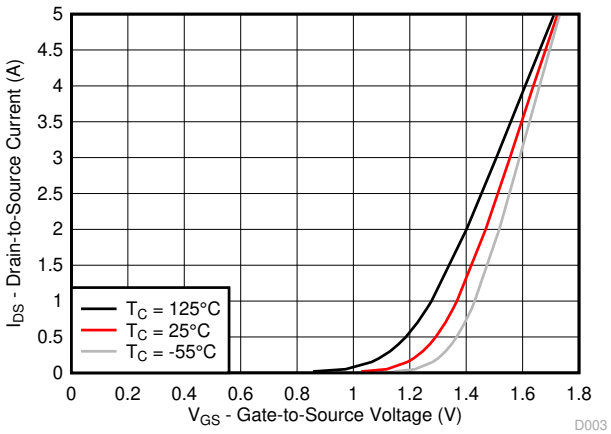


Figure 5-1. Transient Thermal Impedance

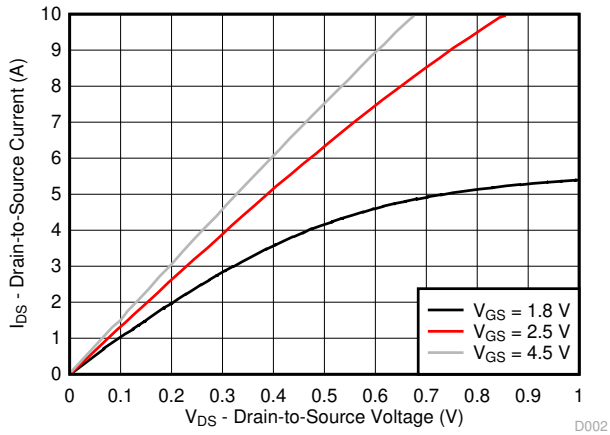
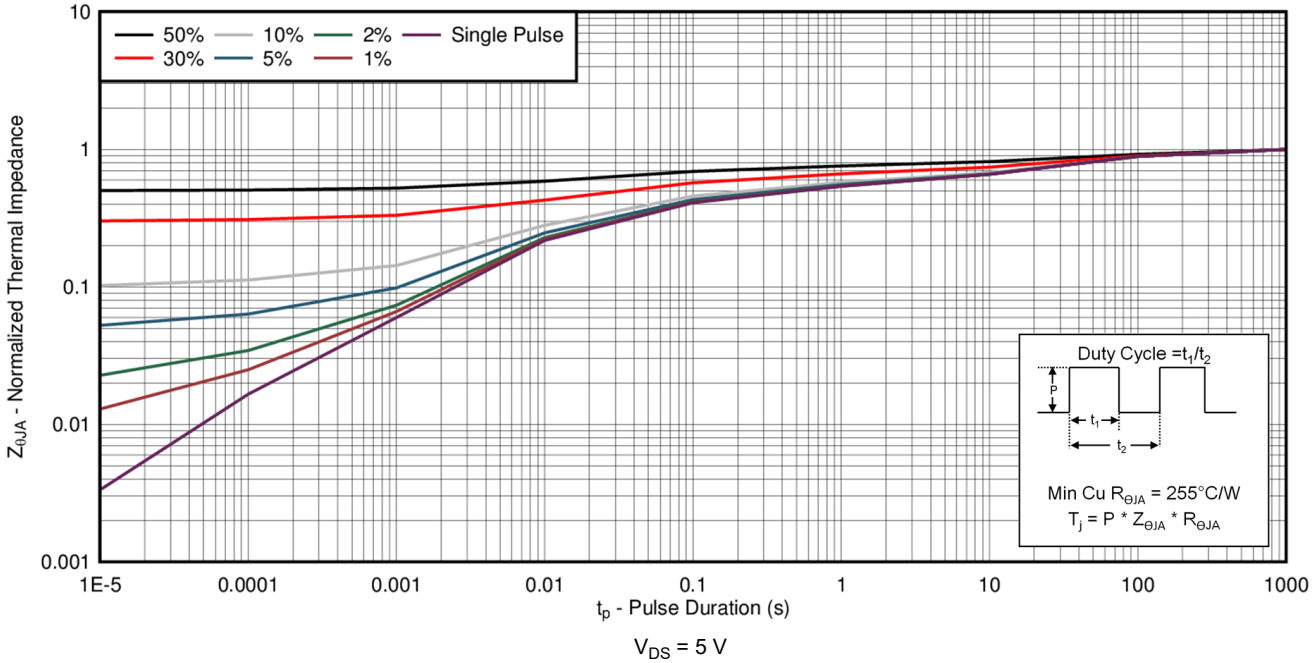
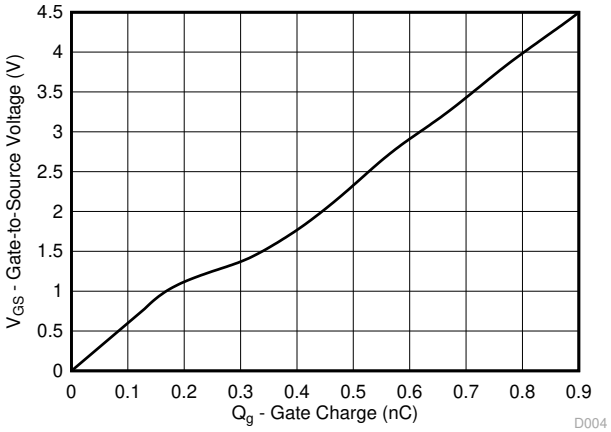


Figure 5-2. Saturation Characteristics



V_{DS} = 5 V

Figure 5-3. Transfer Characteristics



V_{DS} = 6 V I_D = 0.4 A

Figure 5-4. Gate Charge

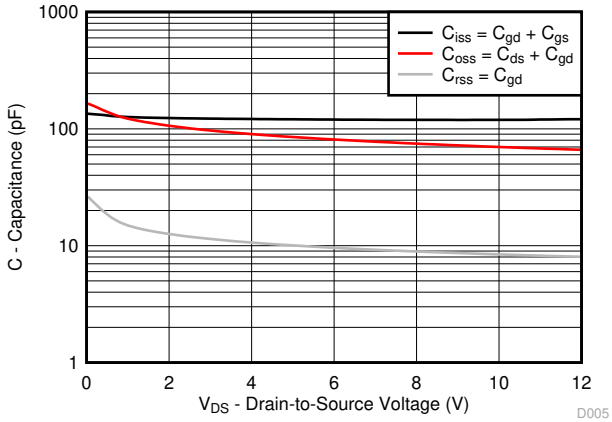
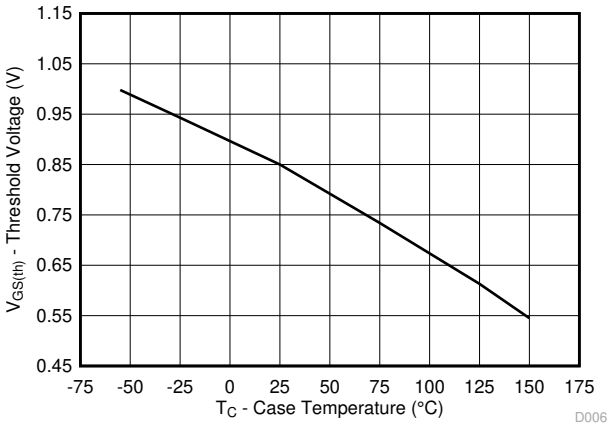


Figure 5-5. Capacitance



I_D = 250 µA

Figure 5-6. Threshold Voltage vs Temperature

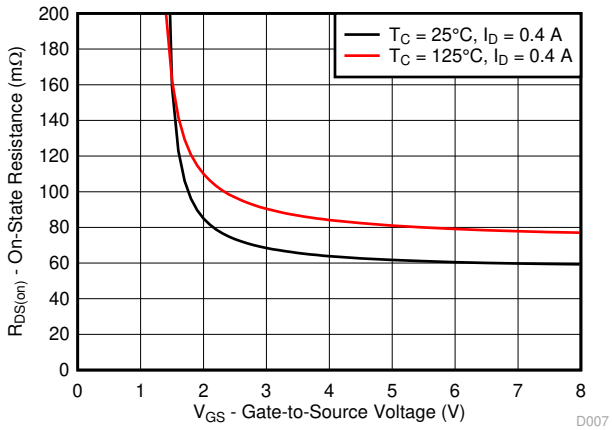
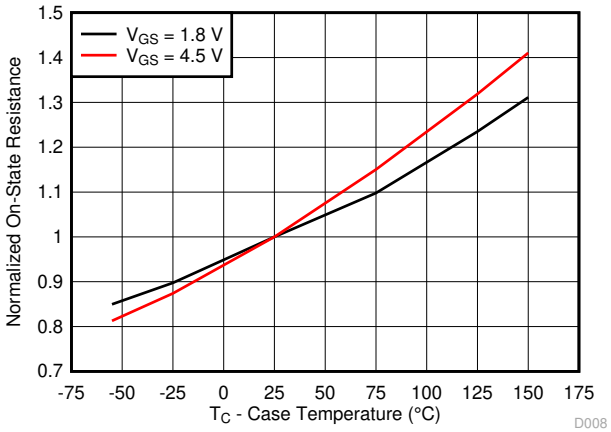


Figure 5-7. On-State Resistance vs Gate-to-Source Voltage



I_D = 0.4A

Figure 5-8. Normalized On-State Resistance vs Temperature

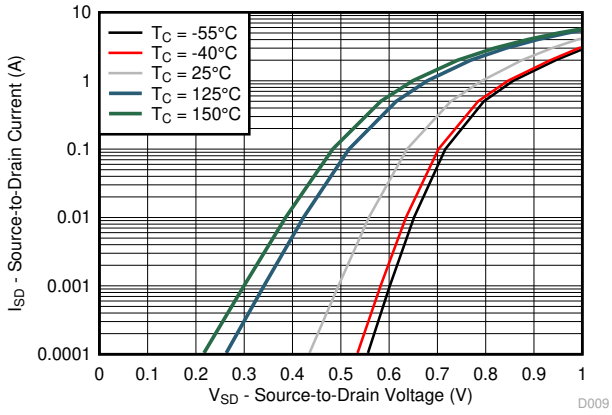
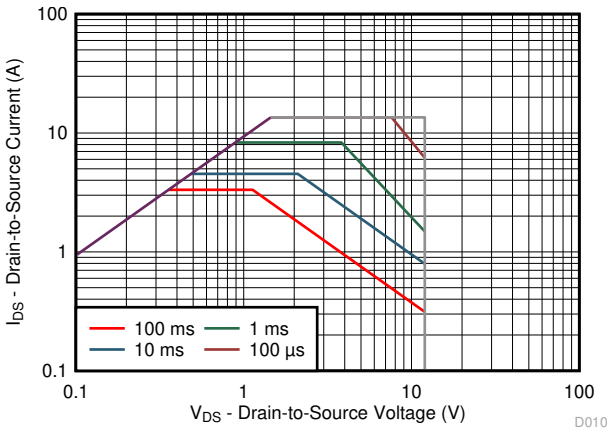


Figure 5-9. Typical Diode Forward Voltage



Single pulse, typical $R_{\theta JA}$ = 255°C/W (min Cu)

Figure 5-10. Maximum Safe Operating Area

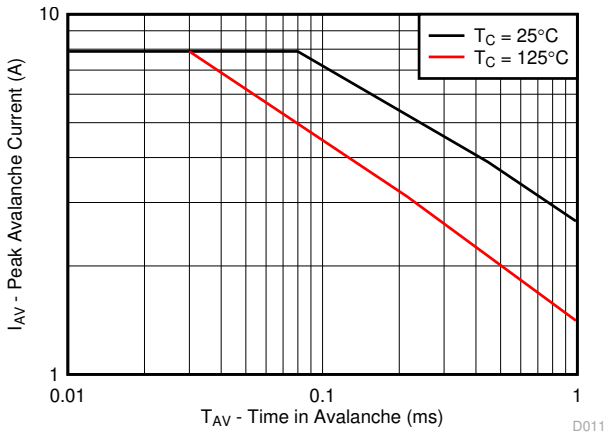
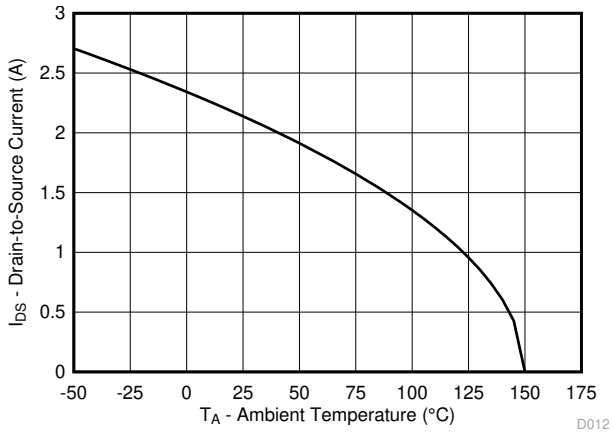


Figure 5-11. Single Pulse Unclamped Inductive Switching



Typical $R_{\theta JA}$ = 255°C/W (min Cu)

Figure 5-12. Maximum Drain Current vs Temperature

6 Device and Documentation Support

6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

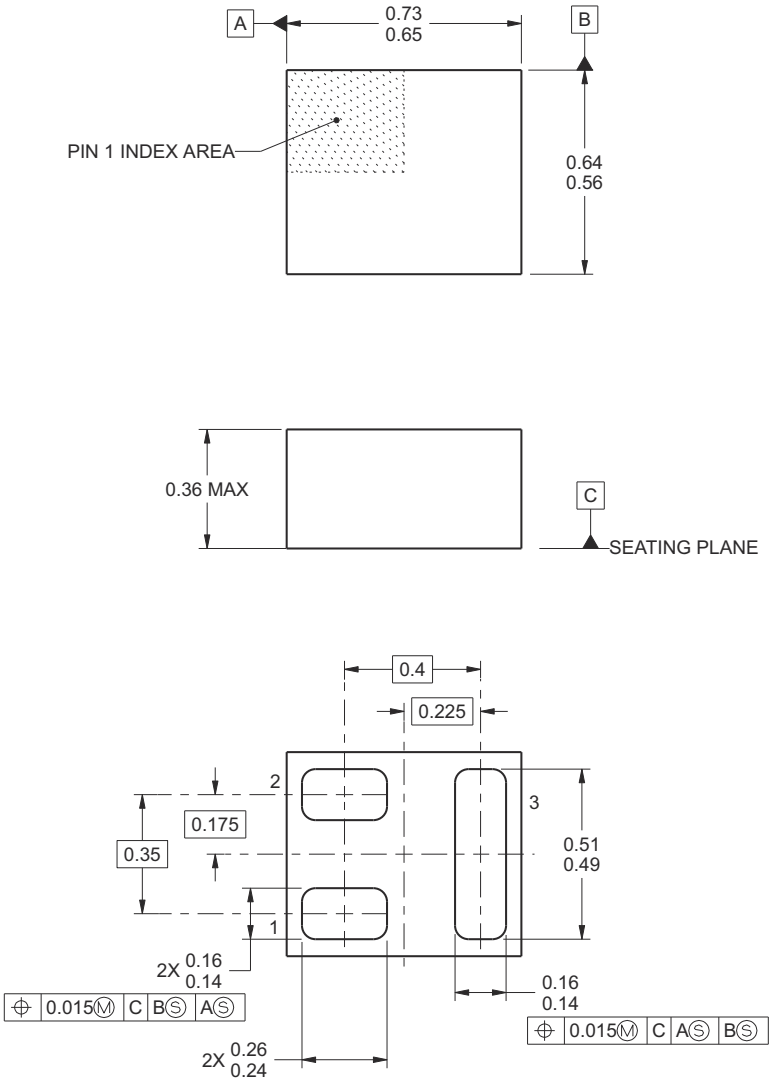
6.2 Trademarks

FemtoFET™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Mechanical Dimensions

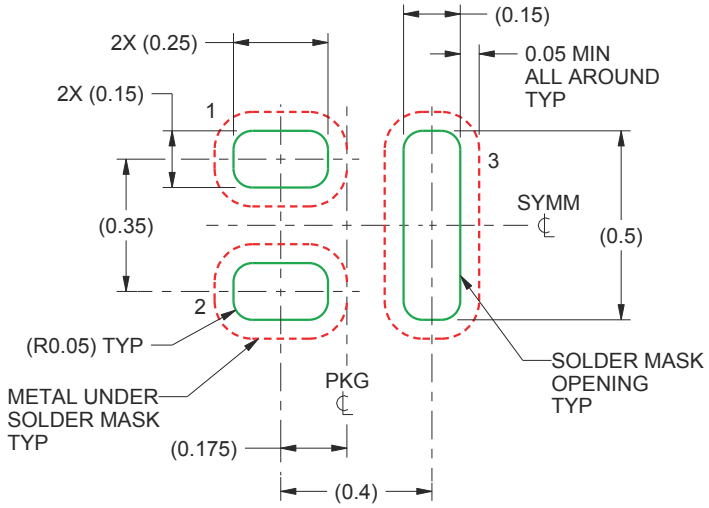


A. All linear dimensions are in millimeters (dimensions and tolerancing per AME T14.5M-1994).
B. This drawing is subject to change without notice.
C. This package is a PB-free solder land design.

Table 7-1. Pin Configuration

POSITION	DESIGNATION
Pin 1	Gate
Pin 2	Source
Pin 3	Drain

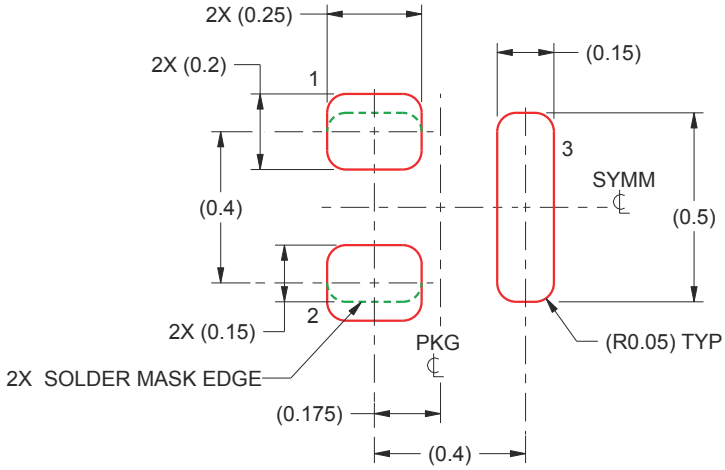
7.2 Recommended Minimum PCB Layout



A. All dimensions are in millimeters.

A. For more information, see *FemtoFET Surface Mount Guide* (SLRA003D).

7.3 Recommended Stencil Pattern



A. All dimensions are in millimeters.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD13380F3	ACTIVE	PICOSTAR	YJM	3	3000	RoHS & Green	NIAU	Level-1-260C-UNLIM	-55 to 150	D	Samples
CSD13380F3T	ACTIVE	PICOSTAR	YJM	3	250	RoHS & Green	NIAU	Level-1-260C-UNLIM	-55 to 150	D	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

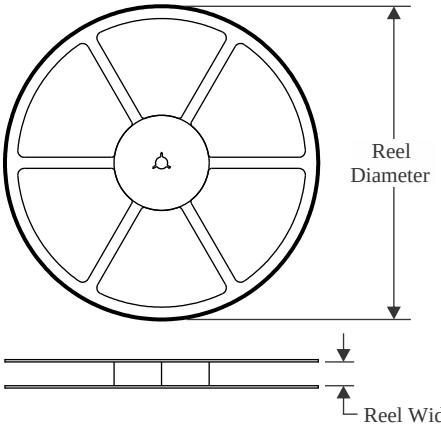
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

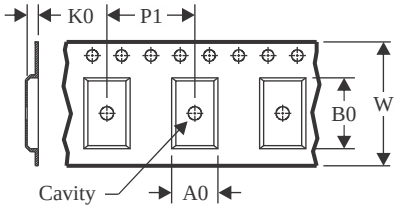
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

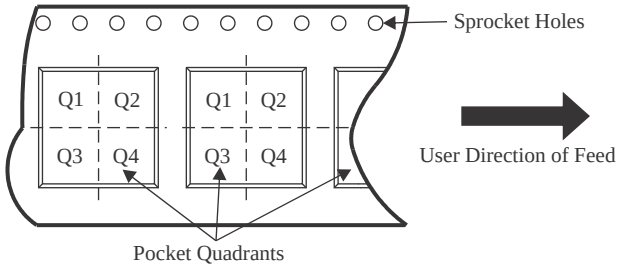


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

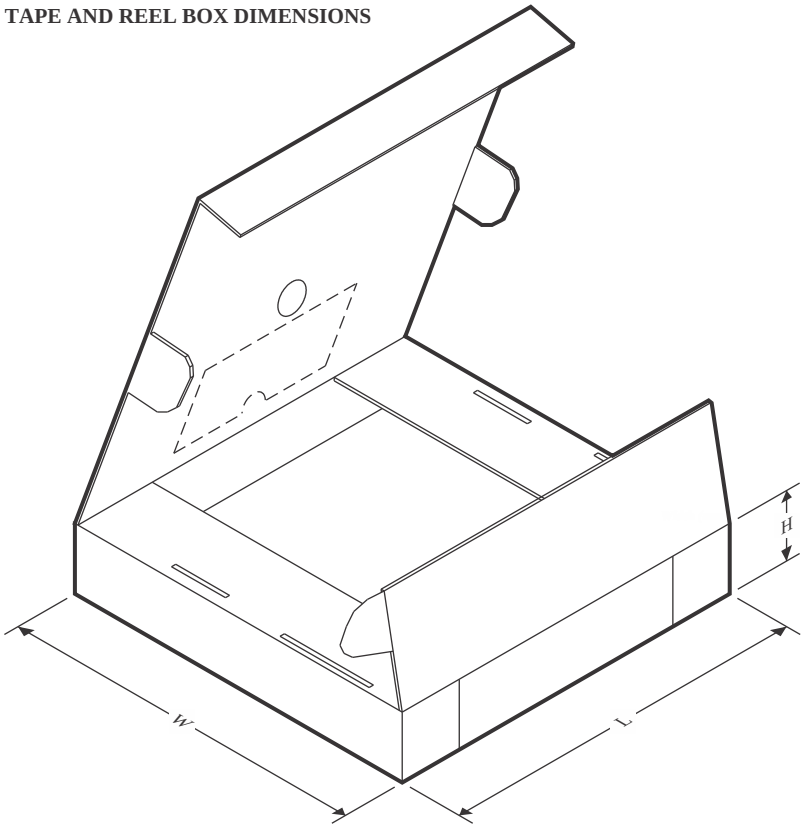
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD13380F3	PICOSTAR	YJM	3	3000	180.0	8.4	1.94	0.79	0.44	4.0	8.0	Q2
CSD13380F3T	PICOSTAR	YJM	3	250	180.0	8.4	1.94	0.79	0.44	4.0	8.0	Q2
CSD13380F3T	PICOSTAR	YJM	3	250	178.0	8.4	0.7	0.79	0.44	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

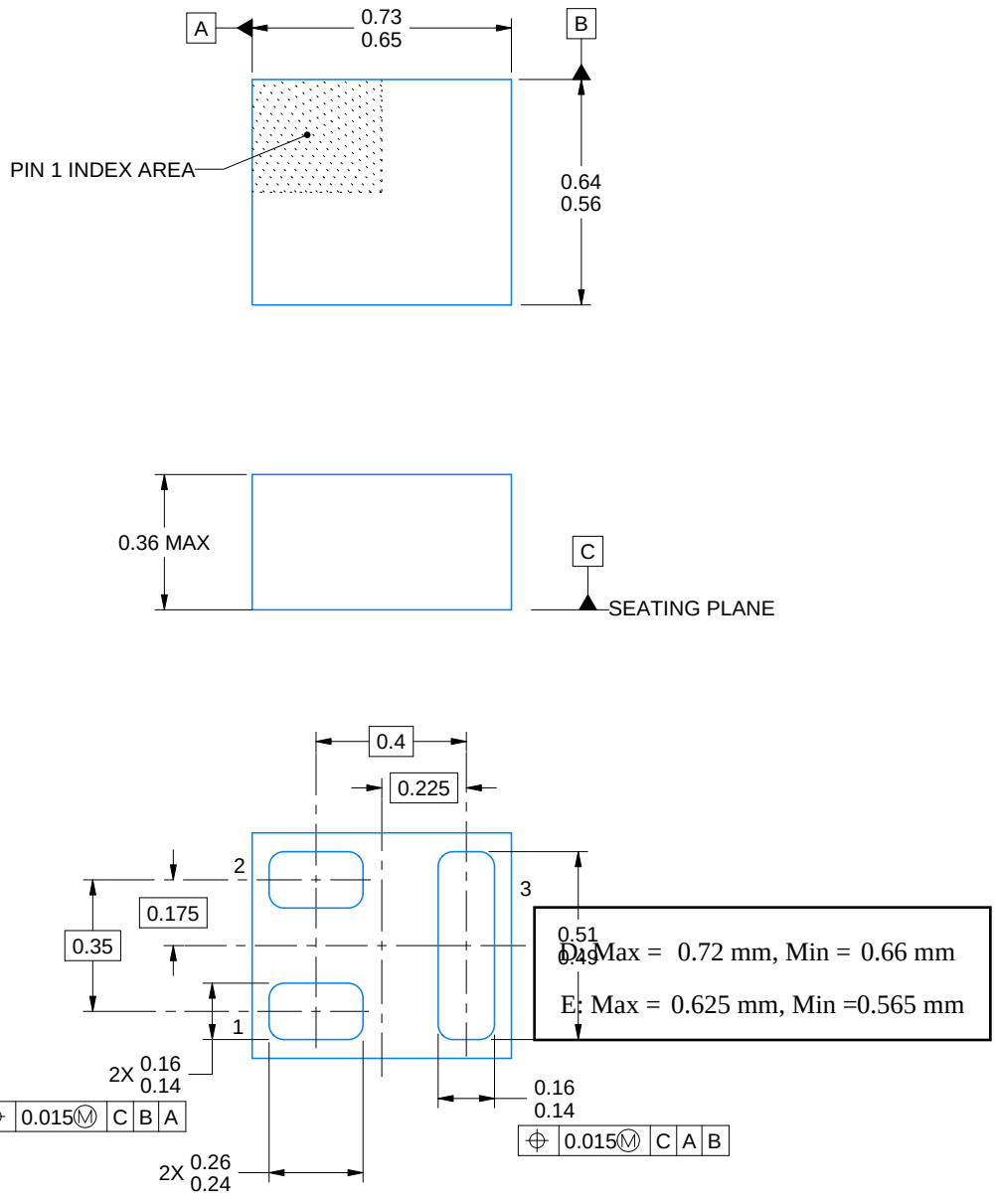
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD13380F3	PICOSTAR	YJM	3	3000	182.0	182.0	20.0
CSD13380F3T	PICOSTAR	YJM	3	250	182.0	182.0	20.0
CSD13380F3T	PICOSTAR	YJM	3	250	220.0	220.0	35.0

PACKAGE OUTLINE

YJM0003A

PicoStar™ - 0.36 mm max height

PicoStar™

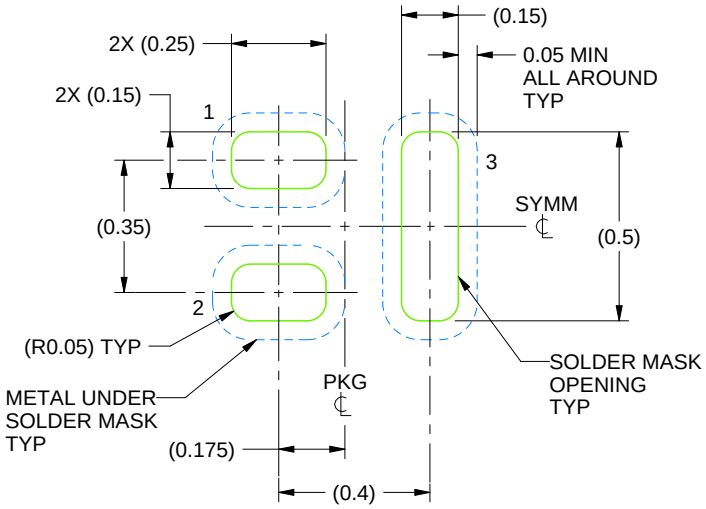


4222304/B 03/2022

PicoStar is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M
2. This drawing is subject to change without notice.
3. This package is a Pb-free bump design. Bump finish may vary. To determine the exact finish, refer to the device datasheet or contact a local TI representative.

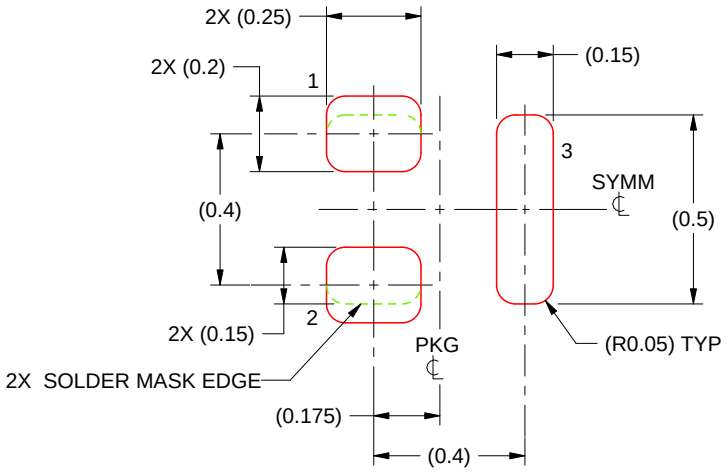


LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:50X

4222304/B 03/2022

NOTES: (continued)

4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:50X

4222304/B 03/2022

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265