TEXAS INSTRUMENTS
LM5009
SNVS402I – FEBRUARY 2006 – REVISED MAY 2021

LM5009 Wide Input, 100-V,150-mA, Step-Down Switching Regulator

1 Features

- Newer product: LM5163 100-V, 0.5-A synchronous buck DC/DC converter
- Integrated N-channel MOSFET
- 150-mA output current capability
- Ultra-fast transient response
- No loop compensation required
- V_{IN} feedforward provides constant operating frequency
- Switching frequency can exceed 600 kHz
- Highly efficient operation
- 2% accurate 2.5-V feedback from –40°C to +125°C
- Internal start-up regulator
- Intelligent current limit protection
- External shutdown control
- Thermal shutdown
- 8-pin VSSOP and thermally enhanced 8-pin WSON packages

2 Applications

- Heat sink eliminator for classic linear regulator applications
- 12-V, 24-V, 36-V, and 48-V rectified AC systems
- Non-isolated AC mains charge-coupled supplies
- LED current source

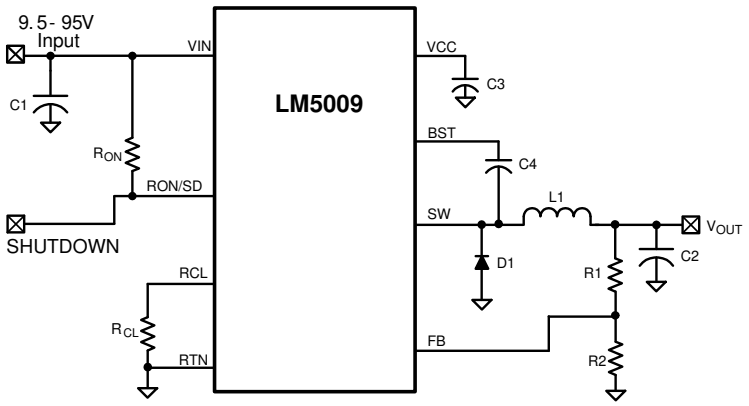
3 Description

The LM5009 step-down switching regulator features all of the functions needed to implement a low-cost and efficient, buck regulator. This device is capable of driving a 150-mA load current from a 9.5-V to 95-V input source. The switching frequency can exceed 600 kHz, depending on the input and output voltages. The output voltage can be set from 2.5 V to 85 V. This high-voltage regulator contains an N-channel buck switch and an internal startup regulator. The device is easy to implement and is provided in 8-pin VSSOP and thermally-enhanced, 8-pin WSON packages. The regulator operation is based on a control scheme using an on-time inversely proportional to VIN. This feature allows the operating frequency to remain relatively constant over load and input voltage variations. The control scheme requires no loop compensation, resulting in an ultrafast transient response. An intelligent current limit is implemented with forced off-time that is inversely proportional to V_{OUT}. This scheme ensures short-circuit protection and provides minimum foldback. Other features include thermal shutdown, V_{CC} undervoltage lockout, gate drive undervoltage lockout, and maximum duty cycle limiter.

The new product LM5163 offers reduced BOM count, reduced solution size, lower operating quiescent current and many other features. Start WEBENCH® design with LM5163.

Device Information

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM5009	VSSOP (8)	3.00 mm × 3.00 mm
	WSON (8)	4.00 mm × 4.00 mm



Typical Application Circuit

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision H (October 2015) to Revision I (May 2021)	Page
• Added information for LM5163 promotion	1
• Updated the numbering format for tables, figures, and cross-references throughout the document.	1
• Changed *Section 2* bullets	1
• Changed *Section 3*, editorial	1

Changes from Revision G (February 2013) to Revision H (October 2015)	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section.	1

Changes from Revision F (February 2013) to Revision G (February 2013)	Page
• Changed layout of National Data Sheet to TI format	16

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5 Pin Configuration and Functions

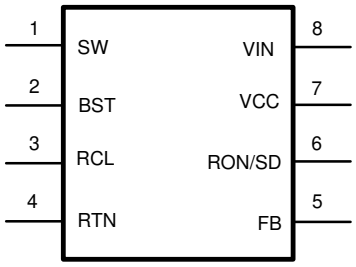


Figure 5-1. DGK, NGU Packages 8-Pin VSSOP, WSON Top View

Table 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
BST	2	I	Boost pin. An external capacitor is required between the BST and SW pins. A 0.022-µF ceramic capacitor is recommended. An internal diode charges the capacitor from V_{CC}.
EP	—	—	Exposed pad (WSON package only). Exposed metal pad on the underside of the device. Connecting this pad to the PC board ground plane is recommended to aid in heat dissipation.
FB	5	I	Feedback input from regulated output. This pin is connected to the inverting input of the internal regulation comparator. The regulation threshold is 2.5 V.
RCL	3	I	Current limit off-time set pin. A resistor between this pin and RTN sets the off-time when current limit is detected. The off-time is preset to 35 µs if FB = 0 V.
RON/SD	6	I	On-time set pin. A resistor between this pin and VIN sets the switch on-time as a function of V_{IN}. The minimum recommended on-time is 250 ns at the maximum input voltage. This pin can be used for remote shutdown.
RTN	4	—	Ground pin. Ground for the entire circuit.
SW	1	O	Switching output. Power switching output. Connect to the inductor, recirculating diode, and bootstrap capacitor.
VCC	7	O	Output from the internal high-voltage startup regulator. Regulated at 7.0 V. If an auxiliary voltage is available to raise the voltage on this pin above the regulation set point (7 V), the internal series pass regulator shuts down, reducing the device power dissipation. Do not exceed 14 V. This voltage provides gate drive power for the internal buck switch. An internal diode is provided between this pin and the BST pin. A local 0.1-µF decoupling capacitor is required.
VIN	8	I	Input voltage. Recommended operating range: 9.5 V to 95 V.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
V_{IN} to RTN	–0.3	100	V
BST to RTN	–0.3	114	V
SW to RTN (steady-state)		–1	V
BST to VCC		100	V
BST to SW		14	V
VCC to RTN		14	V
All other inputs to RTN	–0.3	7	V
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) (3)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
(3) The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{IN}	Line voltage	9.5	95	V
	Operating junction temperature	–40	125	°C

(1) Operating ratings are conditions under which operation of the device is intended to be functional. For specifications and test conditions, see the *Section 6.5*.

6.4 Thermal Information

THERMAL METRIC(1)		LM5009		UNIT
		DGK (VSSOP)	NGU (WSON)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	157.7	42.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	50.2	41.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	77.9	20.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	4.5	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	76.5	20.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	4.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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6.5 Electrical Characteristics

Typical limits are for T_J = 25°C only, and all maximum and minimum limits apply over the junction temperature (T_J) range of –40°C to +125°C. Minimum and maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{IN} = 48 V and R_{ON} = 200 kΩ.(1).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC} SUPPLY						
V_{CC} reg	V_{CC} regulator output		6.6	7	7.4	V
	V_{CC} current limit(2)			9.5		mA
	V_{CC} undervoltage lockout voltage (V_{CC} increasing)			6.3		V
	V_{CC} undervoltage hysteresis			200		mV
	V_{CC} UVLO delay (filter)	100-mV overdrive		10		µs
	I_{IN} operating current	Non-switching, FB = 3 V		485	675	µA
	I_{IN} shutdown current	RON/SD = 0 V		76	150	µA
SWITCH CHARACTERISTICS						
	Buck switch Rds(on)	I_{TEST} = 200 mA(3)		2.0	4.4	Ω
	Gate drive UVLO	V_{BST} − V_{SW} rising	3.4	4.5	5.5	V
	Gate drive UVLO hysteresis			430		mV
CURRENT LIMIT						
	Current limit threshold		0.25	0.31	0.37	A
	Current limit response time	I_{switch} overdrive = 0.1-A time to switch off		400		ns
	OFF time generator (test 1)	FB = 0 V, R_{CL} = 100 kΩ		35		µs
	OFF time generator (test 2)	FB = 2.3 V, R_{CL} = 100 kΩ		2.56		µs
ON TIME GENERATOR						
	T_{ON} - 1	V_{IN} = 10 V, R_{ON} = 200 kΩ	2.15	2.77	3.5	µs
	T_{ON} - 2	V_{IN} = 95 V, R_{ON} = 200 kΩ	200	300	420	ns
	Remote shutdown threshold	Rising	0.4	0.7	1.05	V
	Remote shutdown hysteresis			35		mV
MINIMUM OFF TIME						
	Minimum off timer	FB = 0 V		300		ns
REGULATION AND OV COMPARATORS						
	FB reference threshold	Internal reference, trip point for switch on	2.445	2.5	2.550	V
	FB overvoltage threshold	Trip point for switch off		2.875		V
	FB bias current			1		nA
THERMAL SHUTDOWN						
T_{sd}	Thermal shutdown temperature			165		°C
	Thermal shutdown hysteresis			25		°C

(1) All electrical characteristics having room temperature limits are tested during production with T_A = T_J = 25°C. All hot and cold limits are specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) The V_{CC} output is intended as a self bias for the internal gate drive power and control circuits. Device thermal limitations limit external loading.
(3) For devices procured in the WSON-8 package, the Rds(on) limits are specified by design characterization data only.

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6.6 Typical Characteristics

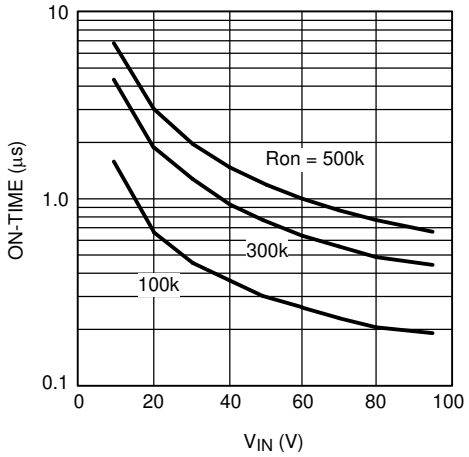


Figure 6-1. On-Time vs V_{IN} and R_{ON}

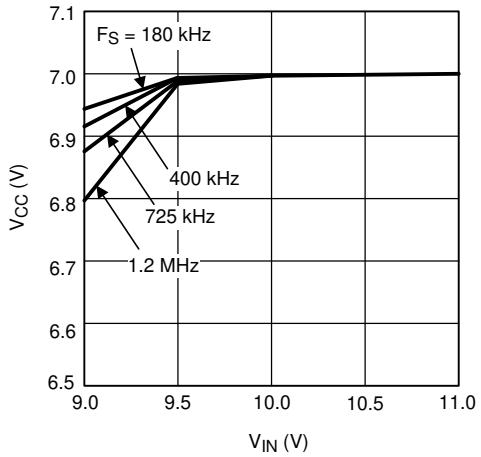


Figure 6-2. V_{CC} vs V_{IN} and F_S

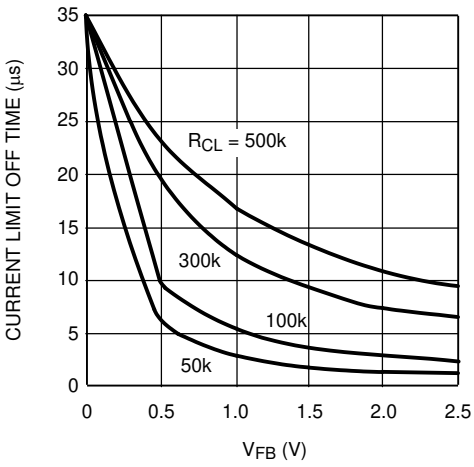


Figure 6-3. Current Limit Off-Time vs V_{FB} and R_{CL}

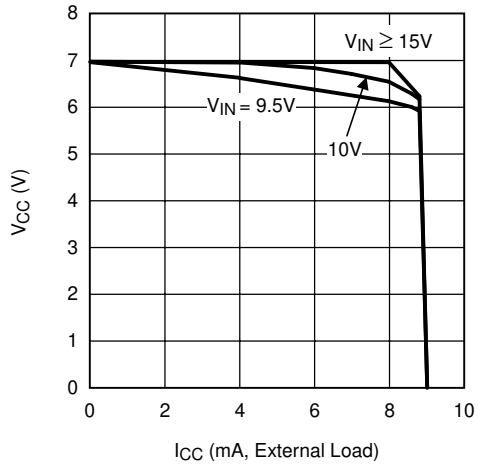


Figure 6-4. V_{CC} vs I_{CC} and V_{IN}

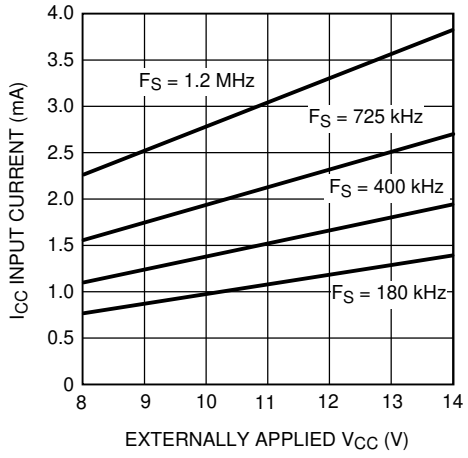


Figure 6-5. I_{CC} Current vs Applied V_{CC} Voltage

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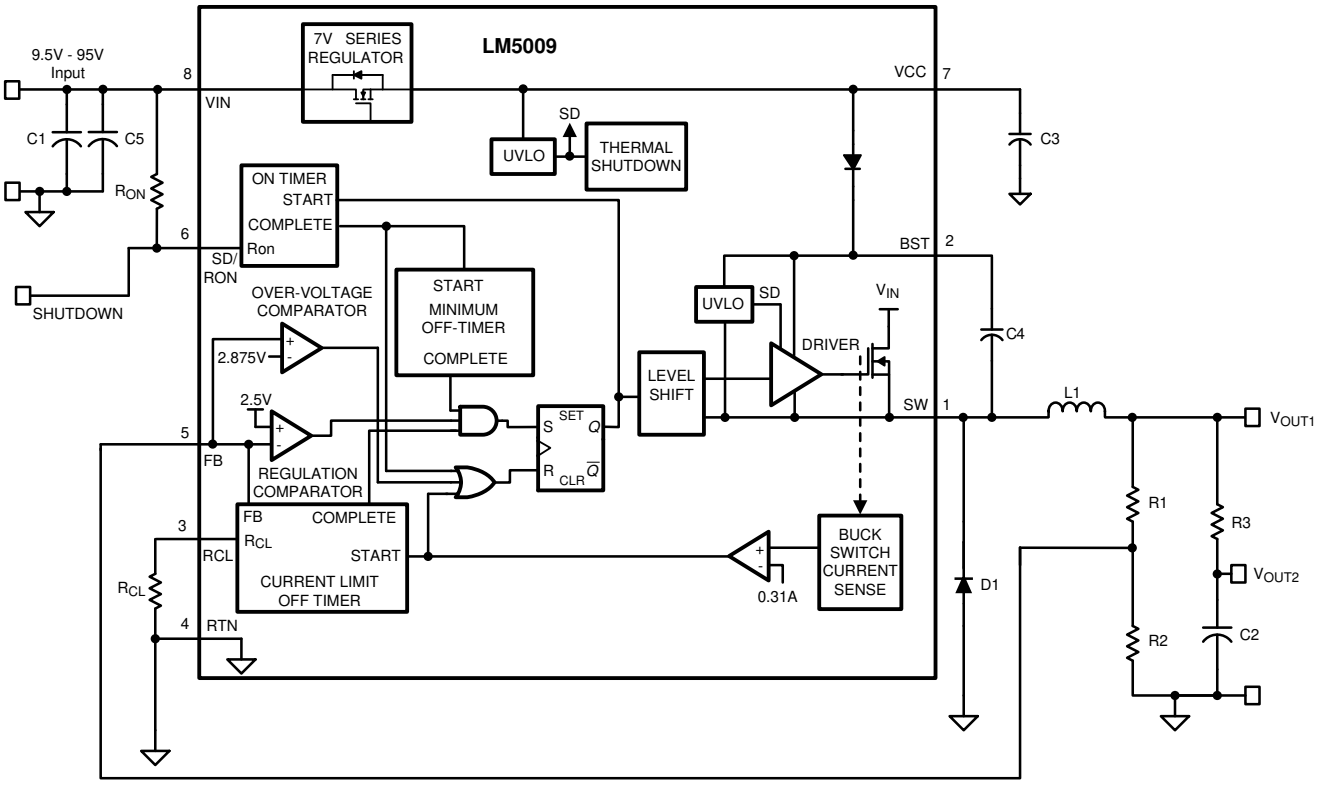
7 Detailed Description

7.1 Overview

The LM5009 step-down switching regulator features all the functions needed to implement a low-cost, efficient, buck bias power converter. This high-voltage regulator contains a 100-V N-channel buck switch, is easy to implement, and is provided in VSSOP-8 and thermally-enhanced, WSON-8 packages. The regulator is based on a control scheme using an on-time inversely proportional to V_{IN}. The control scheme requires no loop compensation. Current limit is implemented with forced off-time that is inversely proportional to V_{OUT}. This scheme ensures short-circuit protection and provides minimum foldback. The functional block diagram of the LM5009 is shown in the *Section 7.2* section.

The LM5009 can be applied in numerous applications to efficiently regulate down higher voltages. This regulator is well-suited for 48-V telecom and 42-V automotive power bus ranges. Additional features include: thermal shutdown, V_{CC} undervoltage lockout, gate drive undervoltage lockout, maximum duty cycle limit timer, and the intelligent current limit off timer.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Control Circuit Overview

The LM5009 is a buck dc-dc regulator that uses a control scheme where the on-time varies inversely with line voltage (V_{IN}). Control is based on a comparator and the on-time one-shot, with the output voltage feedback (FB) compared to an internal reference (2.5 V). If the FB level is below the reference, then the buck switch is turned on for a fixed time determined by the line voltage and a programming resistor (R_{ON}). Following the on period, the switch remains off for at least the minimum off-timer period of 300 ns. If FB is still below the reference at that time, then the switch turns on again for another on-time period. This cycle continues until regulation is achieved, at which time the off-time increases based on the required duty cycle.

The LM5009 operates in discontinuous conduction mode at light load currents, and continuous conduction mode at heavy load current. In discontinuous conduction mode, current through the output inductor starts at zero

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and ramps up to a peak during the on-time, then ramps back to zero before the end of the off-time. The next on-time period starts when the voltage at FB falls below the internal reference—until then, the inductor current remains zero. In this mode the operating frequency is lower than in continuous conduction mode, and varies with load current. Therefore, at light loads the conversion efficiency is maintained because the switching losses reduce with the reduction in load and frequency. The discontinuous operating frequency can be calculated as by Equation 1:

$$F = \frac{V_{OUT}^2 \times L \times 1.28 \times 10^{20}}{R_L \times (R_{ON})^2} \quad (1)$$

where

- R_L = the load resistance

In continuous conduction mode, current flows continuously through the inductor and never ramps down to zero. In this mode, the operating frequency is greater than the discontinuous mode frequency and remains relatively constant with load and line variations. The approximate continuous mode operating frequency can be calculated by Equation 2:

$$F = \frac{V_{OUT}}{1.25 \times 10^{-10} \times R_{ON}} \quad (2)$$

The output voltage (V_{OUT}) is programmed by two external resistors; see the *Section 7.2* section. The regulation point is calculated by Equation 3:

$$V_{OUT} = 2.5 \times (R1 + R2) / R2 \quad (3)$$

This regulator regulates the output voltage based on ripple voltage at the feedback input, requiring a minimum amount of equivalent series resistance (ESR) for the output capacitor C2. A minimum of 25 mV of ripple voltage at the feedback pin (FB) is required for the LM5009. In cases where the capacitor ESR is too small, additional series resistance may be required (see R3 in the *Section 7.2* section).

For applications where lower output voltage ripple is required, the output can be taken directly from a low-ESR output capacitor, as shown in Figure 7-1. However, R3 slightly degrades the load regulation.

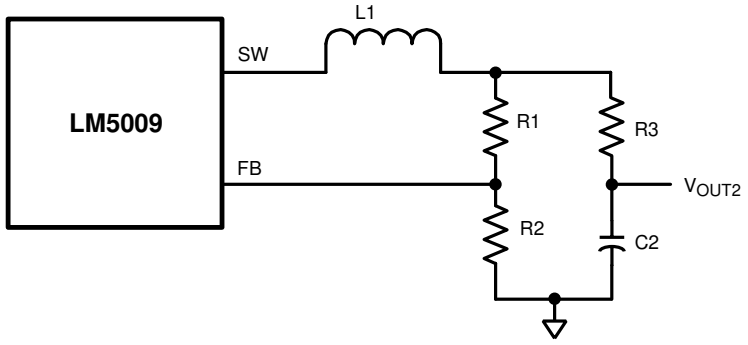


Figure 7-1. Low Ripple Output Configuration

7.3.2 High Voltage Startup Regulator

The LM5009 contains an internal high voltage startup regulator. The input pin (VIN) can be connected directly to line voltages up to 95 V, with transient capability to 100 V. The regulator is internally current limited at 9.5 mA. Upon power-up, the regulator sources current into the external capacitor at VCC (C3). When the voltage on the VCC pin reaches the undervoltage lockout threshold of 6.3 V, the buck switch is enabled.

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In applications involving a high value for V_{IN}, where power dissipation in the V_{CC} regulator is a concern, an auxiliary voltage can be diode connected to the VCC pin. Setting the voltage between 8 V and 14 V shuts off the internal regulator, reducing internal power dissipation, as shown in Figure 7-2. The current required into the VCC pin is illustrated in the *Section 6.6* section.

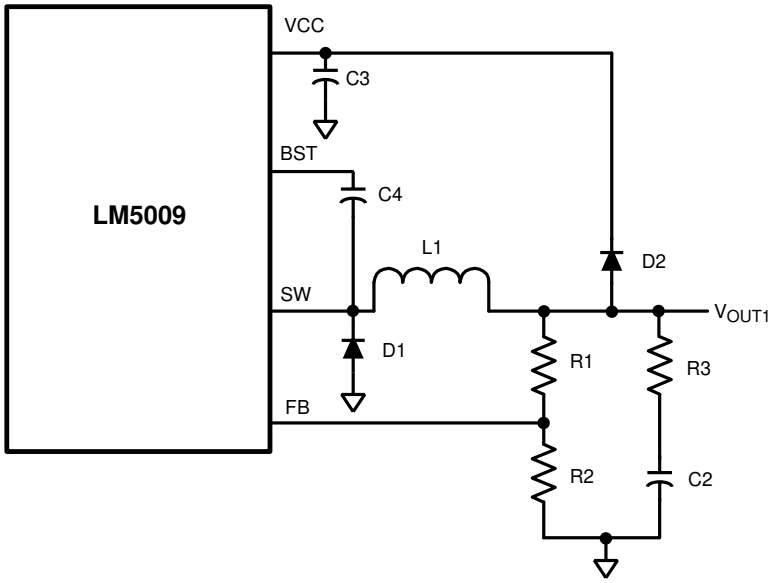


Figure 7-2. Self-Biased Configuration

7.3.3 Regulation Comparator

The feedback voltage at FB is compared to an internal 2.5-V reference. In normal operation (the output voltage is regulated), an on-time period is initiated when the voltage at FB falls below 2.5 V. The buck switch stays on for the programmed on-time, causing the FB voltage to rise above 2.5 V. After the on-time period, the buck switch stays off until the FB voltage again falls below 2.5 V. During start-up, the FB voltage is below 2.5 V at the end of each on-time, resulting in the minimum off-time. Bias current at the FB pin is less than 5 nA over temperature.

7.3.4 Overvoltage Comparator

The feedback voltage at FB is compared to an internal 2.875-V reference. If the voltage at FB rises above 2.875 V, then the on-time pulse is immediately terminated. This condition can occur if the input voltage, or the output load, changes suddenly. The buck switch does not turn on again until the voltage at FB falls below 2.5 V.

7.3.5 On-Time Generator

The on-time for the LM5009 is determined by the R_{ON} resistor, and is inversely proportional to the input voltage (V_{IN}), resulting in a nearly constant frequency because V_{IN} is varied over its range. The on-time equation is shown in Equation 4:

$$T_{ON} = 1.25 \times 10^{-10} \times R_{ON} / V_{IN} \quad (4)$$

Select R_{ON} for a minimum on-time (at maximum V_{IN}) greater than 250 ns, for proper current limit operation. This requirement limits the maximum frequency for each application, depending on V_{IN} and V_{OUT}.

7.3.6 Current Limit

The LM5009 contains an intelligent current limit off timer. If the current in the buck switch exceeds 0.31 A, then the present cycle is immediately terminated and a non-resettable off timer is initiated. The length of off-time is controlled by an external resistor (R_{CL}) and the FB voltage. When FB = 0 V, a maximum off-time is required and the time is preset to 35 µs. This condition occurs when the output is shorted and during the initial part of start-up. This amount of time ensures safe short-circuit operation up to the maximum input voltage of 95 V. In cases of overload where the FB voltage is above 0 V (not a short-circuit) the current limit off-time is less than 35 µs.

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Reducing the off-time during less severe overloads reduces the amount of foldback, recovery time, and start-up time. The off-time is calculated from Equation 5:

$$T_{OFF} = \frac{10^{-5}}{0.285 + \frac{V_{FB}}{(6.35 \times 10^{-6} \times R_{CL})}} \quad (5)$$

The current limit sensing circuit is blanked for the first 50 ns to 70 ns of each on-time so it is not falsely tripped by the current surge that occurs at turn-on. The current surge is required by the recirculating diode (D1) for its turn-off recovery.

7.3.7 N-Channel Buck Switch and Driver

The LM5009 integrates an N-channel buck switch and associated floating high-voltage gate driver. The gate driver circuit works in conjunction with an external bootstrap capacitor and an internal high-voltage diode. A 0.022-µF ceramic capacitor (C4) connected between the BST pin and SW pin provides the voltage to the driver during the on-time.

During each off-time, the SW pin is at approximately –1 V, and the bootstrap capacitor charges from V_{CC} through the internal diode. The minimum off timer ensures a minimum time for each cycle to recharge the bootstrap capacitor.

An external re-circulating diode (D1) carries the inductor current after the internal buck switch turns off. This diode must be of the ultra-fast or Schottky type to minimize turn-on losses and current overshoot.

7.3.8 Thermal Protection

Operate the LM5009 so that the junction temperature does not exceed 125°C during normal operation. An internal thermal shutdown circuit is provided to protect the LM5009 in the event of a higher than normal junction temperature. When activated, typically at 165°C, the controller is forced into a low-power reset state, disabling the buck switch. This feature prevents catastrophic failures from accidental device overheating. When the junction temperature reduces below 140°C (typical hysteresis = 25°C), the buck switch is enabled and normal operation is resumed.

7.4 Device Functional Modes

The LM5009 can be remotely disabled by taking the RON/SD pin to ground, as shown in Figure 7-3. The voltage at the RON/SD pin is between 1.7 V and 5 V, depending on V_{IN} and the value of the R_{ON} resistor.

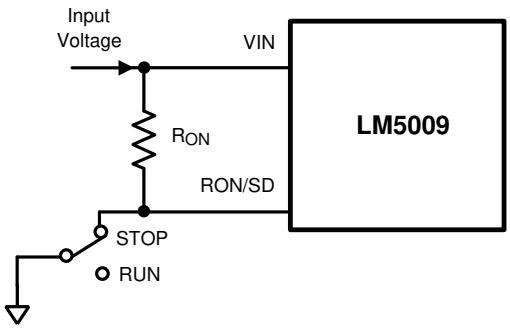


Figure 7-3. Shutdown Implementation

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The LM5009 is a non-synchronous buck regulator designed to operate over a wide input voltage range and output current. Spreadsheet-based quick-start calculation tools and the on-line WEBENCH® software can be used to create a buck design along with the bill of materials, estimated efficiency, and the complete solution cost.

8.2 Typical Application

A typical buck application circuit with the LM5009 is shown in Figure 8-1. The circuit can operate over a wide input voltage range of 9.5 V to 95 V and provides a stable output of 10 V over the load current being varied from 50 mA to 200 mA. The resulting curves are shown in Figure 8-2 through Figure 8-5.

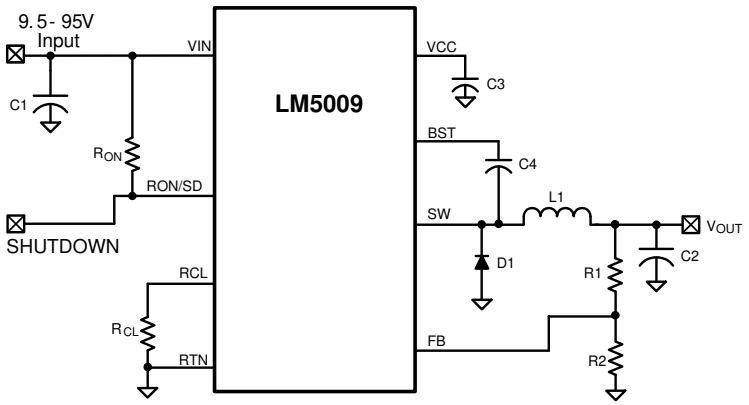


Figure 8-1. Typical Buck Application Circuit

8.2.1 Design Requirements

A typical buck application circuit with the LM5009 can be summarized by the operating conditions listed in Table 8-1.

Table 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	9.5 V to 95 V
Output voltage	10 V
Load current range	50 mA to 200 mA
Nominal switching frequency	330 kHz

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8.2.2 Detailed Design Procedure

8.2.2.1 Output Resistor Divider Selection

R1 and R2: From the *Section 7.2* section, V_{OUT1} can be determined to be equal to V_{FB} × (R1 + R2) / R2, and because V_{FB} = 2.5 V, the ratio of R1 to R2 calculates as 3:1. Standard values of 3.01 kΩ (R1) and 1.00 kΩ (R2) are chosen. Other values can be used as long as the 3:1 ratio is maintained. The selected values, however, provide a small amount of output loading (2.5 mA) in the event that the main load is disconnected and allows the circuit to maintain regulation until the main load is reconnected.

8.2.2.2 Frequency Selection

F_s and R_{ON}: Unless the application requires a specific frequency, the choice of frequency is generally a compromise because the size of L1 and C2, and the switching losses are affected. The maximum-allowed frequency, based on a minimum on-time of 250 ns, is calculated by Equation 6:

$$F_{MAX} = V_{OUT} / (V_{INMAX} \times 250\ ns) \quad (6)$$

For this exercise, F_{MAX} = 444 kHz. From Equation 2, R_{ON} calculates to 180 kΩ. A standard-value, 237-kΩ resistor is used to allow for tolerances in Equation 2, resulting in a nominal frequency of 337 kHz.

8.2.2.3 Inductor Selection

L1: The main parameter affected by the inductor is the output current ripple amplitude. The choice of inductor value therefore depends on both the minimum and maximum load currents, keeping in mind that the maximum ripple current occurs at maximum V_{IN}.

1. **Minimum load current:** To maintain continuous conduction at minimum I_O (100 mA), the ripple amplitude (I_{OR}) must be less than 200 mA peak-to-peak so the lower peak of the waveform does not reach zero. L1 is calculated using Equation 7:

$$L1 = \frac{V_{OUT1} \times (V_{IN} - V_{OUT1})}{I_{OR} \times F_s \times V_{IN}} \quad (7)$$

   At V_{IN} = 90 V, L1 (min) calculates to 132 µH. The next larger standard value (150 µH) is chosen and, with this value, I_{OR} calculates to 176 mA peak-to-peak at V_{IN} = 90 V and 33 mA peak-to-peak at V_{IN} = 12 V.
2. **Maximum load current:** At a load current of 150 mA, the peak of the ripple waveform must not reach the minimum value of the LM5009 current limit threshold (250 mA). Therefore, the ripple amplitude must be less than 200 mA peak-to-peak, which is already satisfied in Equation 7. With L1 = 150 µH, at maximum V_{IN} and I_O, the peak of the ripple is 238 mA. Although L1 must carry this peak current without saturating or exceeding its temperature rating, L1 must also be capable of carrying the maximum value of the LM5009 current limit threshold (370 mA) without saturating because the current limit is reached during startup.

8.2.2.4 VCC and Bootstrap Capacitor

C3: The capacitor on the V_{CC} output provides not only noise filtering and stability, but also prevents false triggering of the V_{CC} UVLO at the buck switch on and off transitions. For this reason, C3 must be no smaller than 0.1 µF.

C4: The recommended value is 0.022 µF for C4 because this value is appropriate in the majority of applications. A high-quality ceramic capacitor, with low ESR is recommended because C4 supplies the surge current to charge the buck switch gate at turn-on. A low ESR also ensures a quick recharge during each off-time. At minimum VIN when the on-time is at maximum, C4 can possibly not fully recharge at start-up during each 300-ns off-time. This failure to recharge results from the circuit being unable to complete the start-up and achieve output regulation. This condition can occur when the frequency is intended to be low (for example, R_{ON} = 500 kΩ). In this case, increase C4 to maintain sufficient voltage across the buck switch driver during each on-time.

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8.2.2.5 Output Capacitor Selection

C2 and R3: When selecting the output filter capacitor C2, the items to consider are ripple voltage resulting from the C2 ESR, ripple voltage resulting from the C2 capacitance, and the nature of the load.

1. **ESR and R3:** A low ESR for C2 is generally desirable to minimize power losses and heating within the capacitor. However, this regulator requires a minimum amount of ripple voltage at the feedback input for proper loop operation. For the LM5009, the minimum ripple required at pin 5 is 25 mV peak-to-peak, requiring a minimum ripple at V_{OUT1} of 100 mV. The minimum ESR required at V_{OUT1} is 3 Ω because the minimum ripple current (at minimum V_{IN}) is 33 mA peak-to-peak. R3 is inserted as illustrated in the *Section 7.2* section because quality capacitors for SMPS applications have considerably less ESR. The value of R3, along with the ESR of C2, must result in at least a 25-mV peak-to-peak ripple at pin 5. Generally, R3 is 0.5 Ω to 5.0 Ω.
2. **Nature of the load:** The load can be connected to V_{OUT1} or V_{OUT2}. V_{OUT1} provides good regulation, but with a ripple voltage that ranges from 100 mV (at V_{IN} = 12 V) to 580 mV (at V_{IN} = 90 V). Alternatively, V_{OUT2} provides low ripple (3 mV to 13 mV) but lower regulation resulting from R3.

   C2 generally must be no smaller than 3.3 µF. Typically, the value of C2 is 10 µF to 20 µF, with the optimum value determined by the load. If the load current is fairly constant, a small value suffices for C2. If the load current includes significant transients, a larger value is necessary. For each application, experimentation is needed to determine the optimum values for R3 and C2.
3. **Ripple reduction:** The ripple amplitude at V_{OUT1} can be reduced by reducing R3 and by adding a capacitor across R1 to transfer the ripple at V_{OUT1} directly to the FB pin without attenuation. The new value of R3 is calculated by Equation 8:

$$R3 = 25\ mV / I_{OR(min)} \quad (8)$$

   where

   - $I_{OR(min)}$ is the minimum ripple current amplitude—33 mAp-p in this example

   The added capacitor value is calculated by Equation 9:

$$C = T_{ON(max)} / (R1 // R2) \quad (9)$$

   where

   - $T_{ON(max)}$ is the maximum on-time (at minimum V_{IN})

   The selected capacitor must be larger than the value calculated in Equation 9.

8.2.2.6 Current Limit Off-Timer Setting

R_{CL}: When a current limit condition is detected, the minimum off-time set by this resistor must be greater than the maximum normal off-time that occurs at maximum V_{IN}. Using Equation 4, the minimum on-time is 0.329 µs, yielding a maximum off-time of 2.63 µs. This value is further increased by 82 ns (to 2.72 µs), resulting from a ±25% tolerance of the on-time. This value is then increased to allow for the response time of the current limit detection loop (400 ns).

The off-time determined by Equation 5 has a ±25% tolerance, as given by Equation 10:

$$t_{OFFCL(MIN)} = (2.72\ \mu s \times 1.25) + 0.4\ \mu s = 3.8\ \mu s \quad (10)$$

Using Equation 5, R_{CL} calculates to 167 kΩ (at V_{FB} = 2.5 V). The closest standard value is 169 kΩ.

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8.2.2.7 Rectifier Diode Selection

D1: The important parameters are reverse recovery time and forward voltage. Reverse recovery time determines how long the reverse current surge lasts each time that the buck switch is turned on. The forward voltage drop is significant in the event that the output is short-circuited because only this diode voltage forces the inductor current to reduce during the forced off-time. For this reason, a higher voltage is better, although higher voltages affect efficiency. A good choice is an ultrafast or Schottky diode with a reverse recovery time of approximately 30 ns and a forward voltage drop of approximately 0.7 V. Other types of diodes can have a lower forward voltage drop, but can also have longer recovery times or greater reverse leakage. The D1 reverse voltage rating must be at least as great as the maximum V_{IN}, and the D1 current rating must be greater than the maximum current limit threshold (370 mA).

8.2.2.8 Input Capacitor Selection

C1: The purpose of this capacitor is to supply most of the switch current during the on-time and to limit the voltage ripple at VIN, on the assumption that the voltage source feeding VIN has an output impedance greater than zero. At maximum load current, when the buck switch turns on, the current into pin 8 suddenly increases to the lower peak of the output current waveform, ramps up to the peak value, and then drops to zero at turn-off. The average input current during this on-time is the load current (150 mA). For a worst-case calculation, C1 must supply this average load current during the maximum on-time. To keep the input voltage ripple to less than 2 V (for this exercise), C1 calculates to Equation 11:

$$C1 = \frac{I \times t_{ON}}{\Delta V} = \frac{0.15A \times 2.47\ \mu s}{2.0V} = 0.185\ \mu F \tag{11}$$

Quality ceramic capacitors in this value have a low ESR that adds only a few millivolts to the ripple. The capacitance is dominant in this case. To allow for the capacitor tolerance, temperature effects, and voltage effects, a 1.0-µF, 100-V, X7R capacitor is used.

C5: This capacitor helps avoid supply voltage transients and ringing resulting from long lead inductance at VIN. A low-ESR, 0.1-µF ceramic chip capacitor is recommended, located close to the LM5009.

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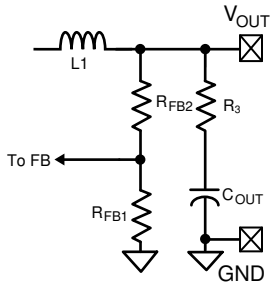
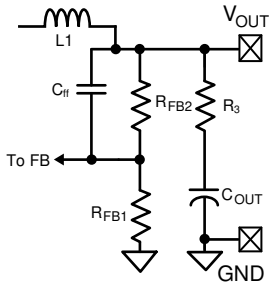
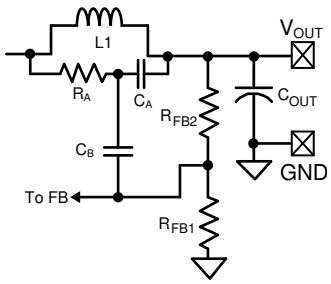
8.2.2.9 Ripple Configuration

The LM5009 uses a constant-on-time (COT) control scheme where the on-time is terminated by a one-shot and the off-time is terminated by the feedback voltage (V_{FB}) falling below the reference voltage. Therefore, for stable operation, the feedback voltage must decrease monotonically in phase with the inductor current during the off-time. Furthermore, this change in feedback voltage (V_{FB}) during off-time must be large enough to dominate any noise present at the feedback node.

Table 8-2 presents three different methods for generating appropriate voltage ripple at the feedback node. Type 1 and type 2 ripple circuits couple the ripple from the output of the converter to the feedback node (FB). The output voltage ripple has two components:

1. Capacitive ripple caused by the inductor current ripple charging or discharging the output capacitor.
2. Resistive ripple caused by the inductor current ripple flowing through the ESR of the output capacitor and R3.

Table 8-2. Ripple Configuration

TYPE 1	TYPE 2	TYPE 3
Lowest cost	Reduced ripple	Minimum ripple
		
$R_3 \geq \frac{25\ mV \times V_O}{V_{REF} \times \Delta I_{L1,min}}$ (12)	$C_{ff} \geq \frac{5}{F_{SW} \times (R_{FB2} \text{ IIR}_{FB1})}$ $R_3 \geq \frac{25\ mV}{\Delta I_{L1,min}}$ (13)	$R_A C_A \geq \frac{(V_{IN,min} - V_O) \times T_{ON(@\ V_{IN,min})}}{25mV}$ (14)

The capacitive ripple is out of phase with the inductor current. As a result, the capacitive ripple does not decrease monotonically during the off-time. The resistive ripple is in phase with the inductor current and decreases monotonically during the off-time. The resistive ripple must exceed the capacitive ripple at output (V_{OUT}) for stable operation. If this condition is not satisfied, then unstable switching behavior is observed in COT converters with multiple on-time bursts in close succession followed by a long off-time.

The type 3 ripple method uses a ripple injection circuit with R_A, C_A, and the switch node (SW) voltage to generate a triangular ramp. This triangular ramp is then ac-coupled into the feedback node (FB) using the capacitor C_B. This circuit is suited for applications where low output voltage ripple is imperative because this circuit does not use the output voltage ripple. See application note *AN-1481 Controlling Output Ripple and Achieving ESR Independence in Constant On-Time (COT) Regulator Designs*, SNVA166 for more details on each ripple generation method.

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8.2.3 Application Curves

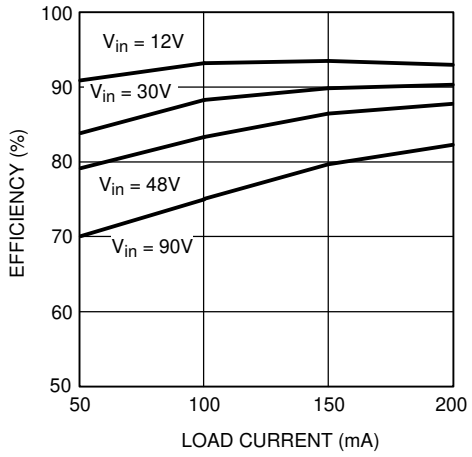


Figure 8-2. Efficiency vs Load Current and V_{IN}

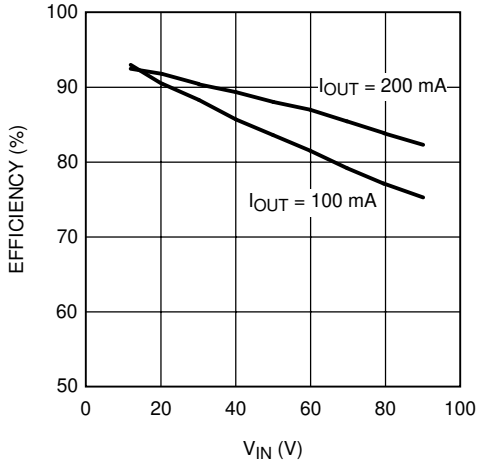


Figure 8-3. Efficiency vs V_{IN} and Load Current

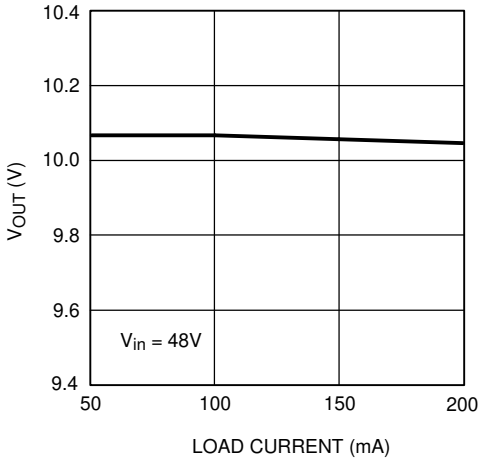


Figure 8-4. V_{OUT} vs Load Current

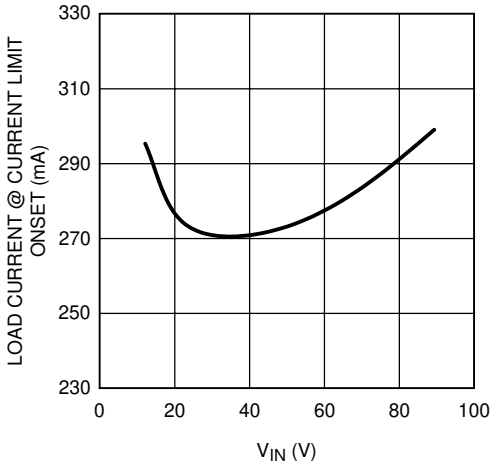


Figure 8-5. Current Limit vs V_{IN}

8.3 Do's and Don'ts

A minimum load current of 1 mA is required to maintain proper operation. If the load current falls below that level, the bootstrap capacitor can discharge during the long off-time and the circuit either shuts down or cycles on and off at a low frequency. If the load current is expected to drop below 1 mA in the application, choose the feedback resistors to be low enough in value to provide the minimum required current at nominal V_{OUT}.

9 Power Supply Recommendations

The LM5009 is designed to operate with an input power supply capable of supplying a voltage range between 9 V and 95 V. The input power supply must be well-regulated and capable of supplying sufficient current to the regulator during peak load operation. Also, like in all applications, the power-supply source impedance must be small compared to the module input impedance to maintain the stability of the converter.

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10 Layout

10.1 Layout Guidelines

The LM5009 regulation and overvoltage comparators are very fast, and as such respond to short-duration noise pulses. Layout considerations are therefore critical for optimum performance. The components at pins 1, 2, 3, 5, and 6 must be as physically close as possible to the device, thereby minimizing noise pickup in the PC tracks. The two major current loops conduct currents that switch very fast and, therefore, those loops must be as small as possible to minimize conducted and radiated electromagnetic interference (EMI). The first loop is formed by C_{IN}, through the VIN to SW pins, L_{IND}, C_{OUT}, and back to C_{IN}. The second current loop is formed by D1, L_{IND}, and C_{OUT}.

If the internal dissipation of the LM5009 produces excessive junction temperatures during normal operation, good use of the PC board ground plane can help considerably to dissipate heat. The exposed pad on the bottom of the WSON-8 package can be soldered to a ground plane on the PC board, and that plane must extend out from beneath the device to help dissipate heat. Additionally, the use of wide PC board traces, where possible, can also help conduct heat away from the device. Judicious positioning of the PC board within the end product, along with the use of any available air flow (forced or natural convection) can help reduce the junction temperatures.

10.2 Layout Example

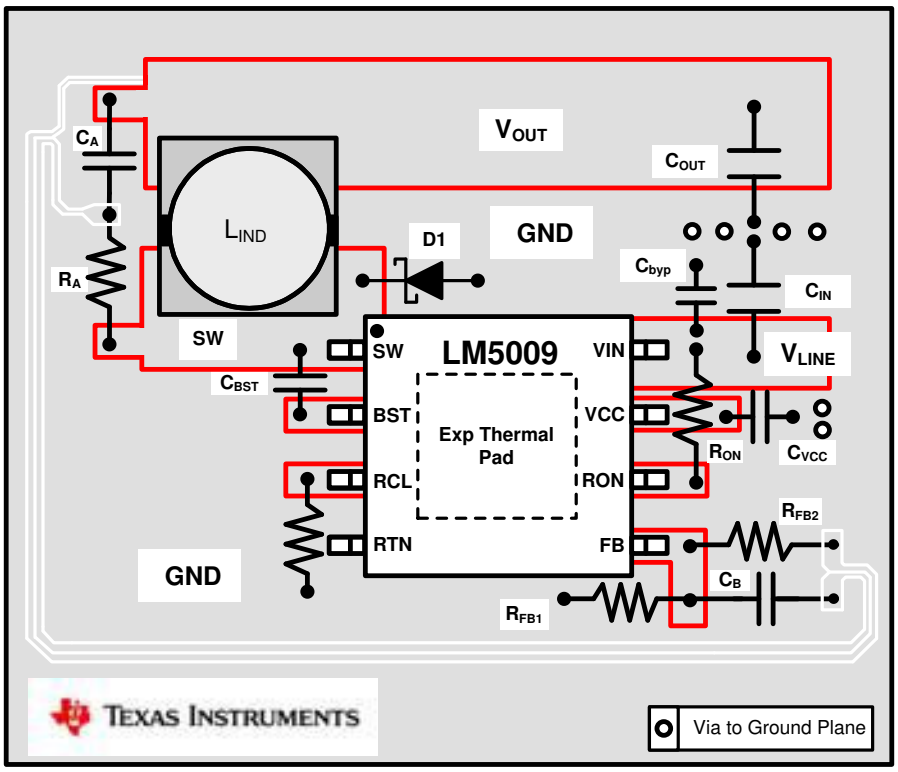


Figure 10-1. LM5009 Buck Layout Example with the WSON Package

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

Application note *AN-1481 Controlling Output Ripple and Achieving ESR Independence in Constant On-Time (COT) Regulator Designs*, SNVA166

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.4 Trademarks

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11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM5009MM	LIFEBUY	VSSOP	DGK	8	1000	Non-RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 125	SLLB	
LM5009MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	SLLB	Samples
LM5009MMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	SLLB	Samples
LM5009SDC/NOPB	ACTIVE	WSON	NGU	8	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	5009SD	Samples
LM5009SDCX/NOPB	ACTIVE	WSON	NGU	8	4500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	5009SD	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

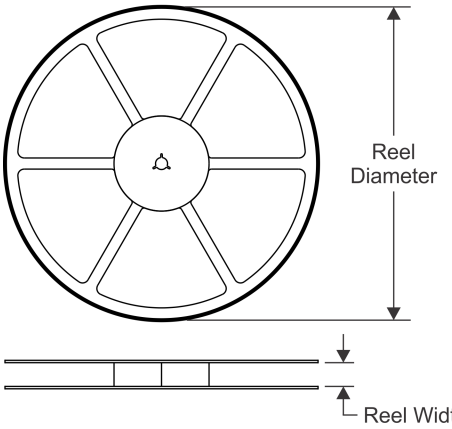
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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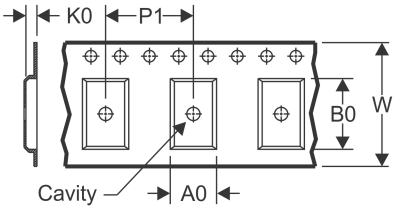
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

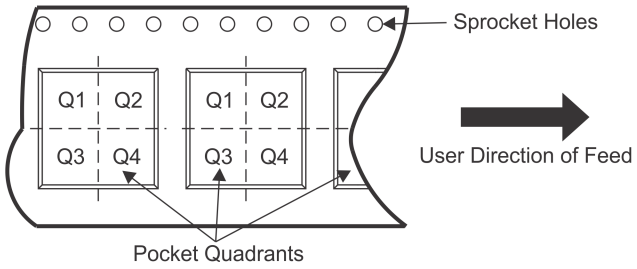


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

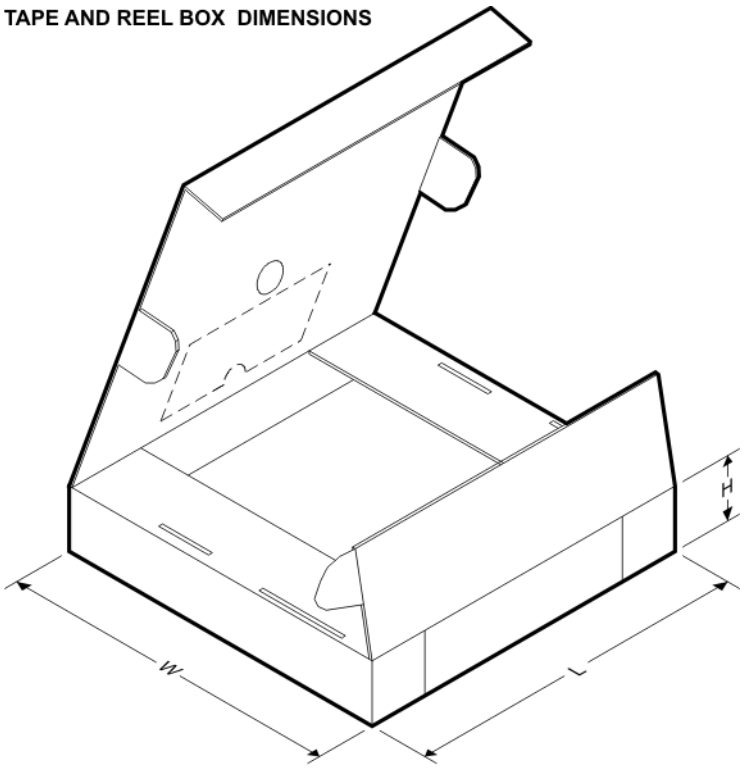
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5009MM	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5009MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5009MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5009SDC/NOPB	WSON	NGU	8	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM5009SDCX/NOPB	WSON	NGU	8	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

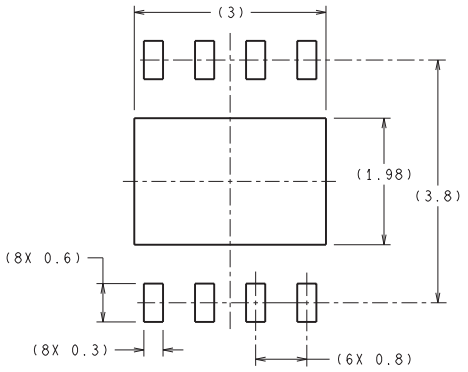
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

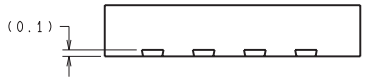
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5009MM	VSSOP	DGK	8	1000	208.0	191.0	35.0
LM5009MM/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LM5009MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LM5009SDC/NOPB	WSON	NGU	8	1000	208.0	191.0	35.0
LM5009SDCX/NOPB	WSON	NGU	8	4500	367.0	367.0	35.0

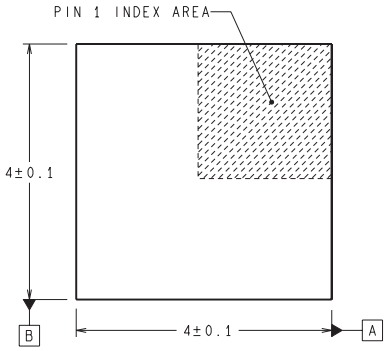
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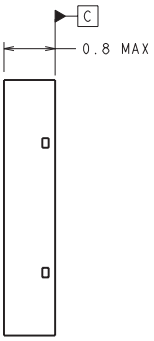


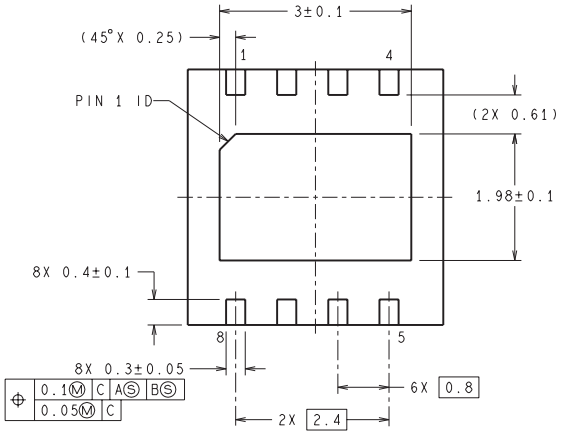
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DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY



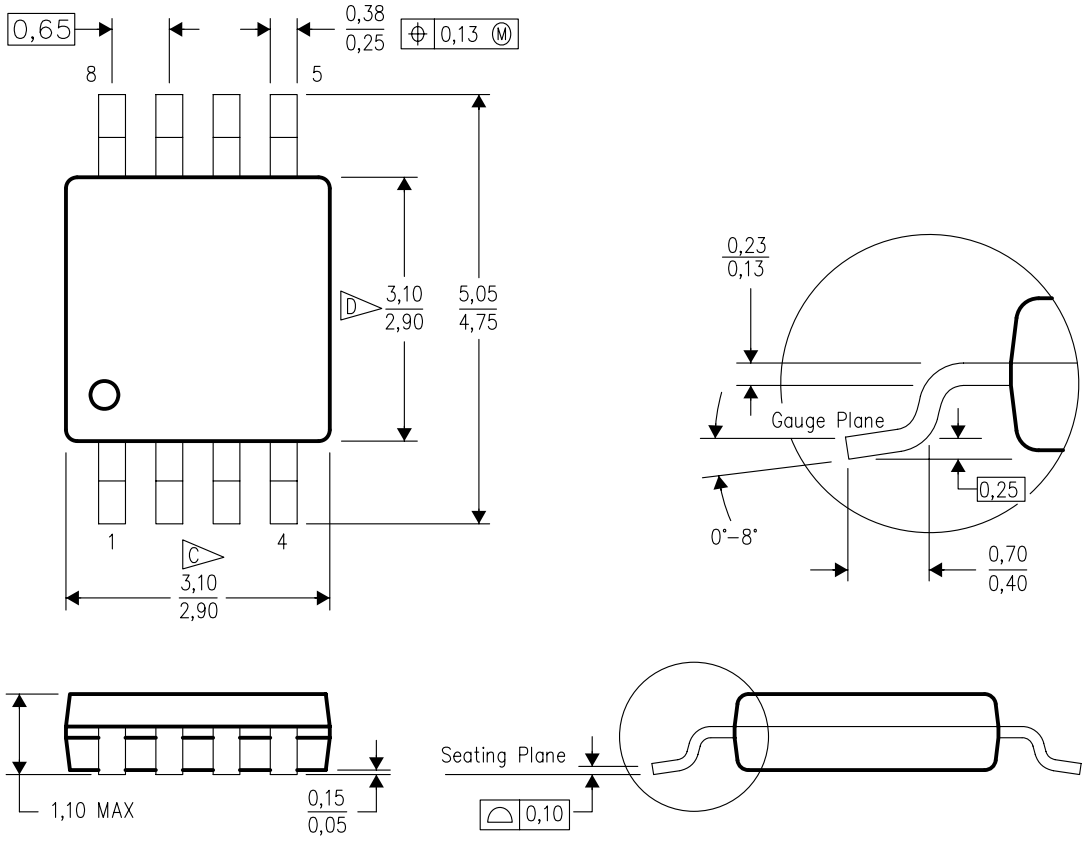






SDC08B (Rev A)

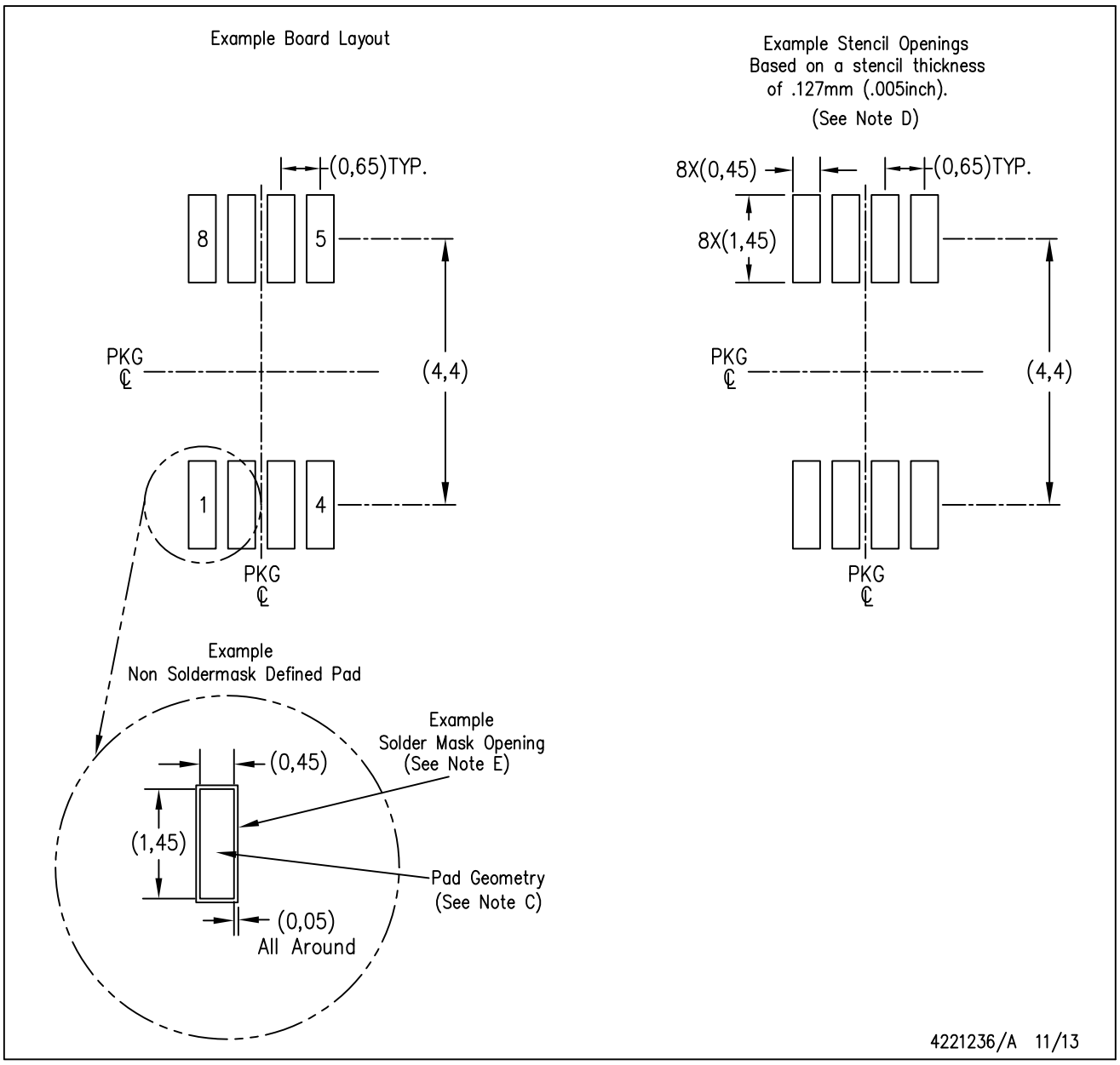
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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