

## LMH6733 Single Supply, 1.0 GHz, Triple Operational Amplifier

Check for Samples: [LMH6733](#)

### FEATURES

- Supply Range 3 to 12V Single Supply
- Supply Range  $\pm 1.5V$  to  $\pm 6V$  Split Supply
- 1.0 GHz  $-3$  dB Small Signal Bandwidth
  - ( $A_V = +1$ ,  $V_S = \pm 5V$ )
- 650 MHz  $-3$  dB Small Signal Bandwidth
  - ( $A_V = +2$ ,  $V_S = 5V$ )
- Low Supply Current (5.5 mA per op Amp,  $V_S = 5V$ )
- 2.1 nV/ $\sqrt{Hz}$  Input Noise Voltage
- 3750 V/ $\mu s$  Slew Rate
- 70 mA Linear Output Current
- CMIR and Output Swing to 1V from Each Supply Rail

### APPLICATIONS

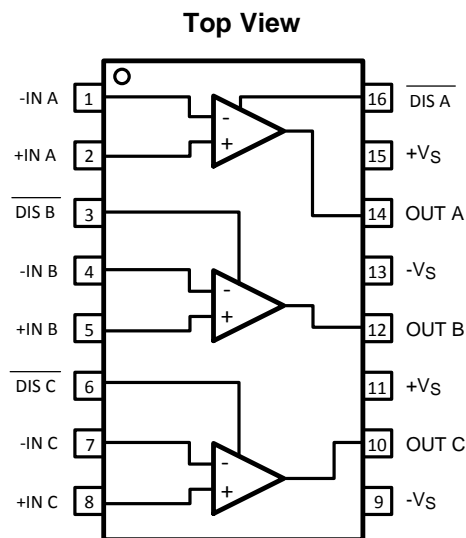
- HDTV Component Video Driver
- High Resolution Projectors
- Flash A/D Driver
- D/A Transimpedance Buffer
- Wide Dynamic Range IF Amp
- Radar/Communication Receivers
- DDS Post-Amps
- Wideband Inverting Summer
- Line Driver

### DESCRIPTION

The LMH6733 is a triple, wideband, operational amplifier designed specifically for use where high speed and low power are required. Input voltage range and output voltage swing are optimized for operation on supplies as low as 3V and up to  $\pm 6V$ . Benefiting from TI's current feedback architecture, the LMH6733 offers a gain range of  $\pm 1$  to  $\pm 10$  while providing stable operation without external compensation, even at unity gain. These amplifiers provide 650 MHz small signal bandwidth at a gain of 2 V/V, a low 2.1 nV/ $\sqrt{Hz}$  input referred noise and only consume 5.5 mA (per amplifier) from a single 5V supply.

The LMH6733 is offered in a 16-Pin SSOP package with flow through pinout for ease of layout and is also pin compatible with the LMH6738. Each amplifier has an individual shutdown pin.

### Connection Diagram



**Figure 1. 16-Pin SSOP Package  
See Package Number DBQ0016A**



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## Absolute Maximum Ratings <sup>(1)(2)</sup>

ESD Tolerance <sup>(3)</sup>	
Human Body Model	2000V
Machine Model	200V
Supply Voltage (V <sup>+</sup> - V <sup>-</sup> )	13.2V
I <sub>OUT</sub>	<sup>(4)</sup>
Common Mode Input Voltage	±V <sub>CC</sub>
Maximum Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Soldering Information	
Infrared or Convection (20 sec.)	235°C
Wave Soldering (10 sec.)	260°C
Storage Temperature Range	-65°C to +150°C

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications, see the Electrical Characteristics tables.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
- (3) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC) Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).
- (4) The maximum output current (I<sub>OUT</sub>) is determined by device power dissipation limitations. See the [Power Dissipation](#) section of the Applications Information for more details.

## Operating Ratings <sup>(1)</sup>

Thermal Resistance			
<b>Package</b>	<b>(θ<sub>JC</sub>)</b>		<b>(θ<sub>JA</sub>)</b>
16-Pin SSOP	36°C/W		120°C/W
Temperature Range <sup>(2)</sup>	-40°C		+85°C
Supply Voltage (V <sup>+</sup> - V <sup>-</sup> )	3V	to	12V

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications, see the Electrical Characteristics tables.
- (2) The maximum power dissipation is a function of T<sub>J(MAX)</sub>, θ<sub>JA</sub>. The maximum allowable power dissipation at any ambient temperature is P<sub>D</sub> = (T<sub>J(MAX)</sub> - T<sub>A</sub>) / θ<sub>JA</sub>. All numbers apply for packages soldered directly onto a PC Board.

## 5V Electrical Characteristics <sup>(1)</sup>

A<sub>V</sub> = +2, V<sub>CC</sub> = 5V, R<sub>L</sub> = 100Ω, R<sub>F</sub> = 340Ω; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>Frequency Domain Performance</b>						
UGBW	-3 dB Bandwidth	Unity Gain, V <sub>OUT</sub> = 200 mV <sub>PP</sub>		870		MHz
SSBW	-3 dB Bandwidth	V <sub>OUT</sub> = 200 mV <sub>PP</sub> , R <sub>L</sub> = 100Ω		650		MHz
SSBW		V <sub>OUT</sub> = 200 mV <sub>PP</sub> , R <sub>L</sub> = 150Ω		685		
LSBW		V <sub>OUT</sub> = 2 V <sub>PP</sub>		480		
0.1 dB BW	0.1 dB Gain Flatness	V <sub>OUT</sub> = 200 mV <sub>PP</sub>		320		MHz

- (1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T<sub>J</sub> = T<sub>A</sub>. No specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T<sub>J</sub> > T<sub>A</sub>.

**5V Electrical Characteristics <sup>(1)</sup> (continued)**
 $A_V = +2$ ,  $V_{CC} = 5V$ ,  $R_L = 100\Omega$ ,  $R_F = 340\Omega$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>Time Domain Response</b>						
TRS	Rise and Fall Time (10% to 90%)	2V Step		0.8		ns
SR	Slew Rate	2V Step		1900		V/ $\mu$ s
$t_s$	Settling Time to 0.1%	2V Step		10		ns
$t_e$	Enable Time	From $\overline{\text{Disable}}$ = Rising Edge		10		ns
$t_d$	Disable Time	From $\overline{\text{Disable}}$ = Falling Edge		15		ns
<b>Distortion</b>						
HD2L	2 <sup>nd</sup> Harmonic Distortion	2 $V_{PP}$ , 10 MHz		-63		dBc
HD3L	3 <sup>rd</sup> Harmonic Distortion	2 $V_{PP}$ , 10 MHz		-73		dBc
<b>Equivalent Input Noise</b>						
$V_N$	Non-Inverting Voltage	>10 MHz		2.1		nV/ $\sqrt{\text{Hz}}$
$I_{CN}$	Inverting Current	>10 MHz		18.6		pA/ $\sqrt{\text{Hz}}$
$N_{CN}$	Non-Inverting Current	>10 MHz		26.9		pA/ $\sqrt{\text{Hz}}$
<b>Video Performance</b>						
DG	Differential Gain	4.43 MHz, $R_L = 150\Omega$		0.03		%
DP	Differential Phase	4.43 MHz, $R_L = 150\Omega$		0.025		deg
<b>Static, DC Performance</b>						
VIO	Input Offset Voltage <sup>(2)</sup>			0.4	2.0 2.5	mV
IBN	Input Bias Current <sup>(2)</sup>	Non-Inverting	2	16.7	28 32	$\mu$ A
IBI	Input Bias Current <sup>(2)</sup>	Inverting		1.0	17 19	$\mu$ A
PSRR	Power Supply Rejection Ratio <sup>(2)</sup>	+PSRR	59 59	61		dB
		-PSRR	58 57	61		
CMRR	Common Mode Rejection Ratio <sup>(2)</sup>		52 51.5	54.5		dB
XTLK	Crosstalk	Input Referred, $f = 10$ MHz, Drive Channels A,C Measure Channel B		-80		dB
$I_{CC}$	Supply Current <sup>(2)</sup>	All Three Amps Enabled, No Load		16.7	18	mA
	Supply Current Disabled $V^+$	$R_L = \infty$		1.54	1.8	mA
	Supply Current Disabled $V^-$	$R_L = \infty$		0.75	1.8	mA
<b>Miscellaneous Performance</b>						
$R_{IN+}$	Non-Inverting Input Resistance			200		k $\Omega$
$C_{IN+}$	Non-Inverting Input Capacitance			1		pF
$R_{IN-}$	Inverting Input Impedance	Output Impedance of Input Buffer.		27		$\Omega$
$R_O$	Output Impedance	DC		0.05		$\Omega$
$V_O$	Output Voltage Range <sup>(2)</sup>	$R_L = 100\Omega$	1.25-3.75 1.3-3.7	1.12-3.88		V
		$R_L = \infty$	1.11-3.89 1.15-3.85	1.03-3.97		
CMIR	Common Mode Input Range <sup>(2)</sup>	CMRR > 40 dB	1.1-3.9 1.2-3.8	1.0-4.0		V
$I_O$	Linear Output Current <sup>(3)</sup> <sup>(2)</sup>	$V_{IN} = 0V$ , $V_{OUT} < \pm 42$ mV	$\pm 50$	$\pm 60$		mA

(2) Parameter 100% production tested at 25° C.

(3) The maximum output current ( $I_{OUT}$ ) is determined by device power dissipation limitations. See the [Power Dissipation](#) section of the Applications Information for more details.

### 5V Electrical Characteristics <sup>(1)</sup> (continued)

$A_V = +2$ ,  $V_{CC} = 5V$ ,  $R_L = 100\Omega$ ,  $R_F = 340\Omega$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$I_{SC}$	Short Circuit Current <sup>(4)</sup>	$V_{IN} = 2V$ Output Shorted to Ground		170		mA
$I_{IH}$	Disable Pin Bias Current High	$\overline{\text{Disable}} \text{ Pin} = V^+$		-72		$\mu A$
$I_{IL}$	Disable Pin Bias Current Low	$\overline{\text{Disable}} \text{ Pin} = 0V$		-360		$\mu A$
$V_{DMAX}$	Voltage for Disable	$\overline{\text{Disable}} \text{ Pin} \leq V_{DMAX}$		3.2		V
$V_{DMIN}$	Voltage for Enable	$\overline{\text{Disable}} \text{ Pin} \geq V_{DMIN}$		3.6		V

(4) Short circuit current should be limited in duration to no more than 10 seconds. See the [Power Dissipation](#) section of the Application Section for more details.

### $\pm 5V$ Electrical Characteristics <sup>(1)</sup>

$A_V = +2$ ,  $V_{CC} = \pm 5V$ ,  $R_L = 100\Omega$ ,  $R_F = 383\Omega$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>Frequency Domain Performance</b>						
UGBW	-3 dB Bandwidth	Unity Gain, $V_{OUT} = 200 \text{ mV}_{PP}$		1000		MHz
SSBW	-3 dB Bandwidth	$V_{OUT} = 200 \text{ mV}_{PP}$ , $R_L = 100\Omega$		830		MHz
SSBW		$V_{OUT} = 200 \text{ mV}_{PP}$ , $R_L = 150\Omega$		950		
LSBW		$V_{OUT} = 2 \text{ V}_{PP}$		600		
0.1 dB BW	0.1 dB Gain Flatness	$V_{OUT} = 200 \text{ mV}_{PP}$		350		MHz
<b>Time Domain Response</b>						
TRS	Rise and Fall Time (10% to 90%)	2V Step		0.7		ns
TRL		5V Step		0.8		
SR	Slew Rate	4V Step		3750		V/ $\mu s$
$t_s$	Settling Time to 0.1%	2V Step		10		ns
$t_e$	Enable Time	From $\overline{\text{Disable}} = \text{Rising Edge}$		10		ns
$t_d$	Disable Time	From $\overline{\text{Disable}} = \text{Falling Edge}$		15		ns
<b>Distortion</b>						
HD2L	2 <sup>nd</sup> Harmonic Distortion	2 $V_{PP}$ , 10 MHz		-72		dBc
HD3L	3 <sup>rd</sup> Harmonic Distortion	2 $V_{PP}$ , 10 MHz		-63		dBc
<b>Equivalent Input Noise</b>						
$V_N$	Non-Inverting Voltage	>10 MHz		2.1		$nV/\sqrt{Hz}$
$I_{CN}$	Inverting Current	>10 MHz		18.6		$pA/\sqrt{Hz}$
$N_{CN}$	Non-Inverting Current	>10 MHz		26.9		$pA/\sqrt{Hz}$
<b>Video Performance</b>						
DG	Differential Gain	4.43 MHz, $R_L = 150\Omega$		0.03		%
DP	Differential Phase	4.43 MHz, $R_L = 150\Omega$		0.03		Deg
<b>Static, DC Performance</b>						
VIO	Input Offset Voltage <sup>(2)</sup>			0.6	2.2 2.5	mV
IBN	Input Bias Current <sup>(2)</sup>	Non-Inverting	-14 -19	3.5	19 24	$\mu A$
IBI	Input Bias Current <sup>(2)</sup>	Inverting		5	23 26	$\mu A$
PSRR	Power Supply Rejection Ratio <sup>(2)</sup>	+PSRR	59	61.5		dB
		-PSRR	58	61		
CMRR	Common Mode Rejection Ratio <sup>(2)</sup>		53 52.5	55		dB

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that  $T_J = T_A$ . No specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where  $T_J > T_A$ .

(2) Parameter 100% production tested at 25° C.

**±5V Electrical Characteristics <sup>(1)</sup> (continued)**
 $A_V = +2$ ,  $V_{CC} = \pm 5V$ ,  $R_L = 100\Omega$ ,  $R_F = 383\Omega$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
XTLK	Crosstalk	Input Referred, $f = 10$ MHz, Drive Channels A,C Measure Channel B		-80		dB
$I_{CC}$	Supply Current <sup>(2)</sup>	All Three Amps Enabled, No Load		19.5	20.8 <b>22.0</b>	mA
	Supply Current Disabled $V^+$	$R_L = \infty$		1.54	1.8	mA
	Supply Current Disabled $V^-$	$R_L = \infty$		0.75	1.8	mA
<b>Miscellaneous Performance</b>						
$R_{IN+}$	Non-Inverting Input Resistance			200		k $\Omega$
$C_{IN+}$	Non-Inverting Input Capacitance			1		pF
$R_{IN-}$	Inverting Input Impedance	Output Impedance of Input Buffer		30		$\Omega$
$R_O$	Output Impedance	DC		0.05		$\Omega$
$V_O$	Output Voltage Range <sup>(2)</sup>	$R_L = 100\Omega$	$\pm 3.55$ <b><math>\pm 3.5</math></b>	$\pm 3.7$		V
		$R_L = \infty$	$\pm 3.85$	$\pm 4.0$		
CMIR	Common Mode Input Range <sup>(2)</sup>	CMRR > 43 dB	$\pm 3.9$ <b><math>\pm 3.8</math></b>	$\pm 4.0$		V
$I_O$	Linear Output Current <sup>(3) (2)</sup>	$V_{IN} = 0V$ , $V_{OUT} < \pm 42$ mV	70	$\pm 80$		mA
$I_{SC}$	Short Circuit Current <sup>(4)</sup>	$V_{IN} = 2V$ Output Shorted to Ground		237		mA
$I_{IH}$	Disable Pin Bias Current High	Disable Pin = $V^+$		-72		$\mu A$
$I_{IL}$	Disable Pin Bias Current Low	Disable Pin = 0V		-360		$\mu A$
$V_{DMAX}$	Voltage for Disable	Disable Pin $\leq V_{DMAX}$		3.2		V
$V_{DMIM}$	Voltage for Enable	Disable Pin $\geq V_{DMIN}$		3.6		V

- (3) The maximum output current ( $I_{OUT}$ ) is determined by device power dissipation limitations. See the [Power Dissipation](#) section of the Applications Information for more details.
- (4) Short circuit current should be limited in duration to no more than 10 seconds. See the [Power Dissipation](#) section of the Application Section for more details.

### Typical Performance Characteristics

$A_V = +2$ ,  $V_{CC} = 5V$ ,  $R_L = 100\Omega$ ,  $R_F = 340\Omega$ ; unless otherwise specified).

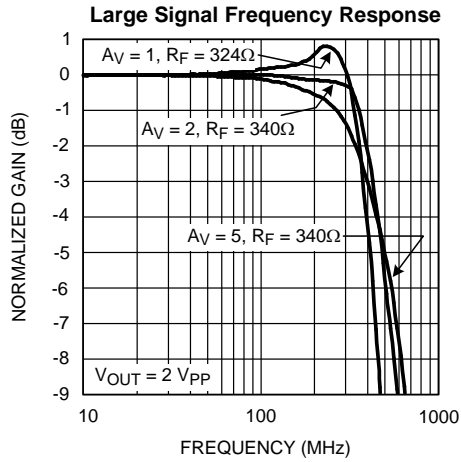


Figure 2.

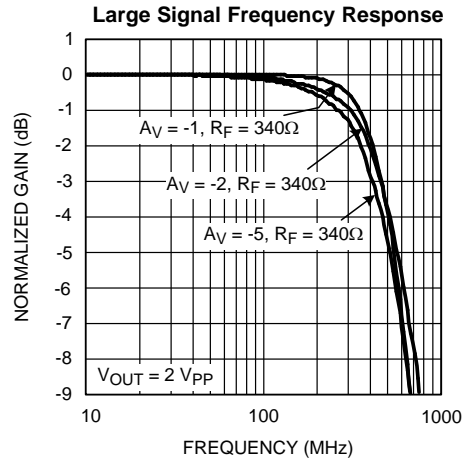


Figure 3.

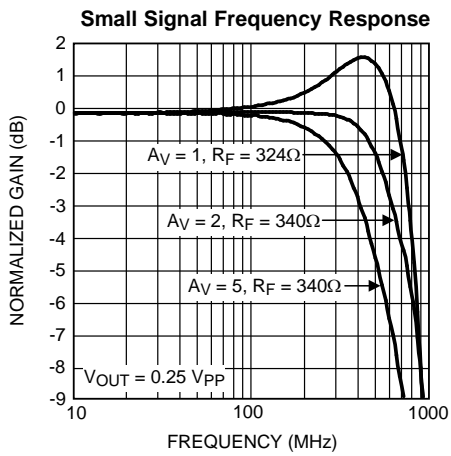


Figure 4.

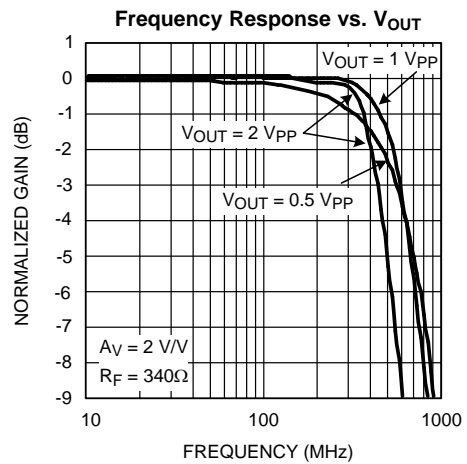


Figure 5.

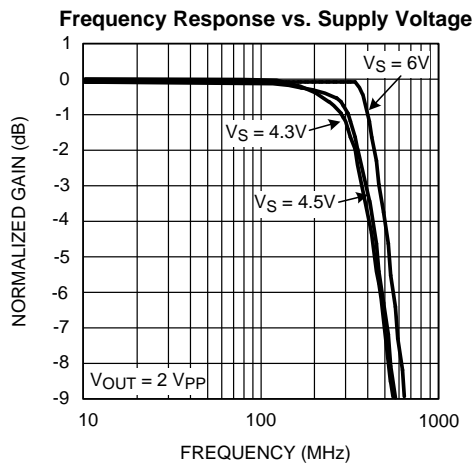


Figure 6.

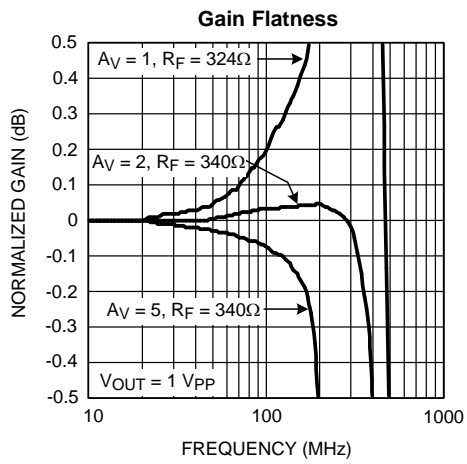


Figure 7.

Typical Performance Characteristics (continued)

$A_V = +2$ ,  $V_{CC} = 5V$ ,  $R_L = 100\Omega$ ,  $R_F = 340\Omega$ ; unless otherwise specified).

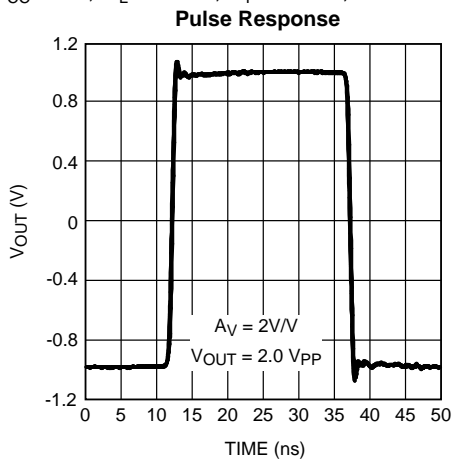


Figure 8.

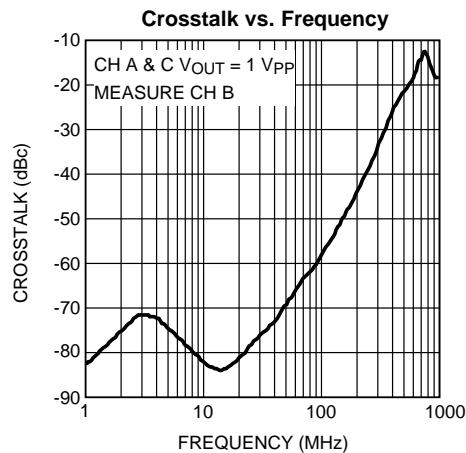


Figure 9.

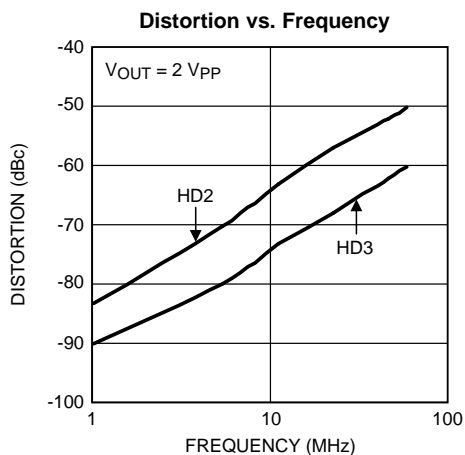


Figure 10.

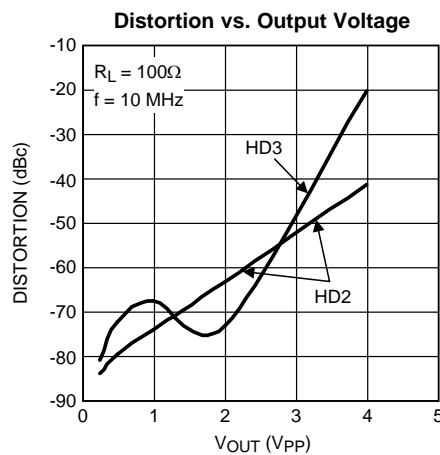


Figure 11.

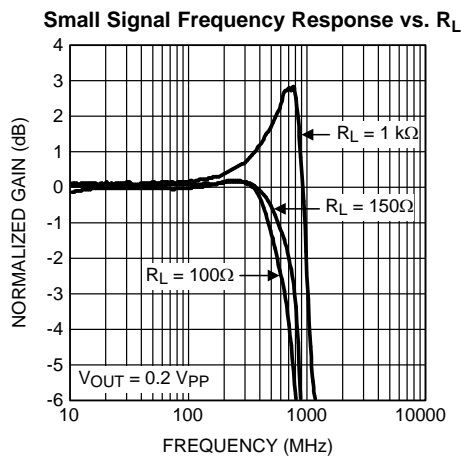


Figure 12.

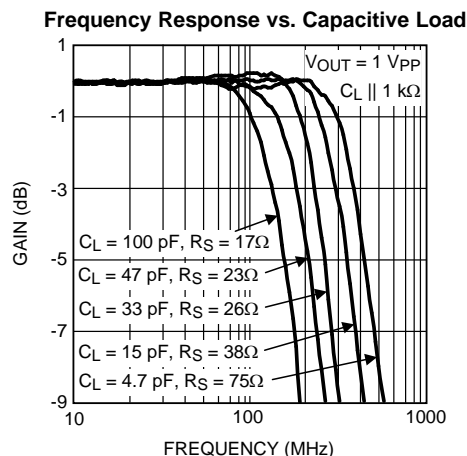


Figure 13.

**Typical Performance Characteristics (continued)**

$A_V = +2$ ,  $V_{CC} = 5V$ ,  $R_L = 100\Omega$ ,  $R_F = 340\Omega$ ; unless otherwise specified).

**Series Output Resistance vs. Capacitive Load**

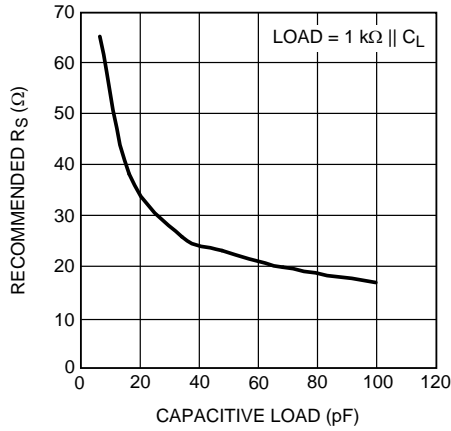


Figure 14.

**PSRR vs. Frequency**

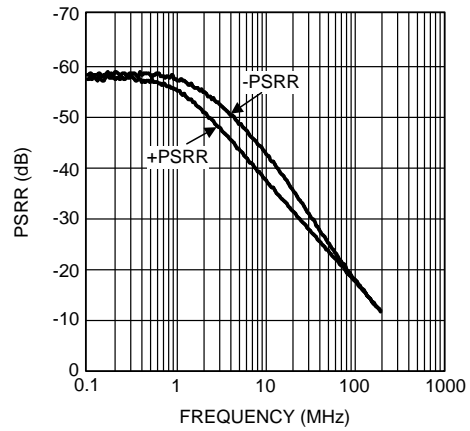


Figure 15.

**CMRR vs. Frequency**

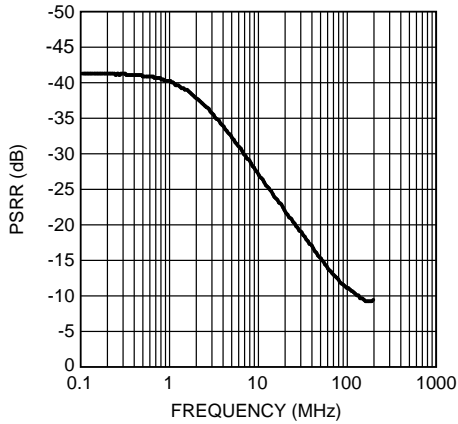


Figure 16.

**Closed Loop Output Impedance |Z|**

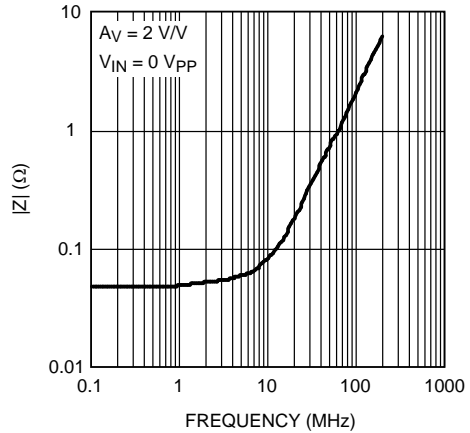


Figure 17.

**Disabled Channel Isolation vs. Frequency**

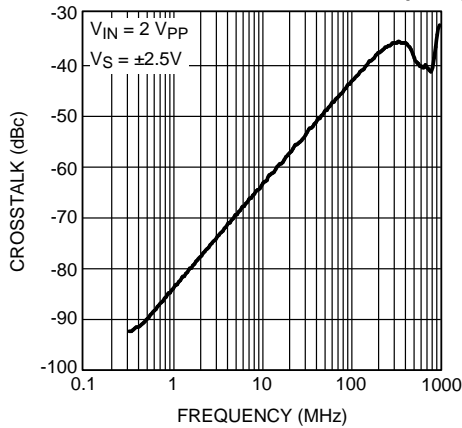


Figure 18.

**Disable Timing**

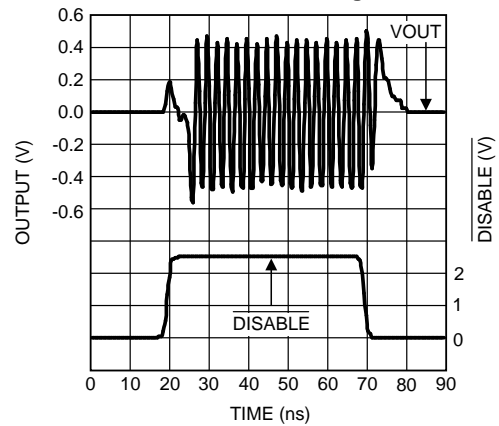


Figure 19.



Typical Performance Characteristics (continued)

$A_V = +2$ ,  $V_{CC} = 5V$ ,  $R_L = 100\Omega$ ,  $R_F = 340\Omega$ ; unless otherwise specified).

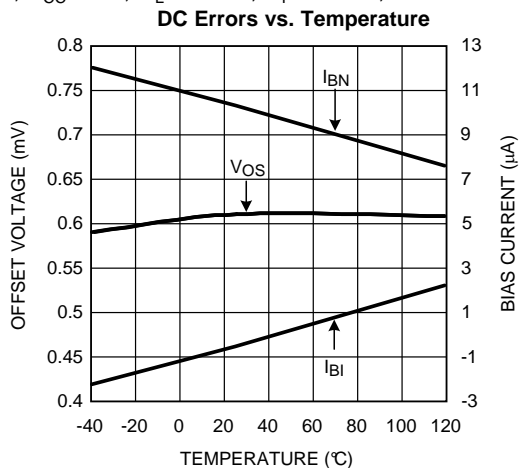


Figure 20.

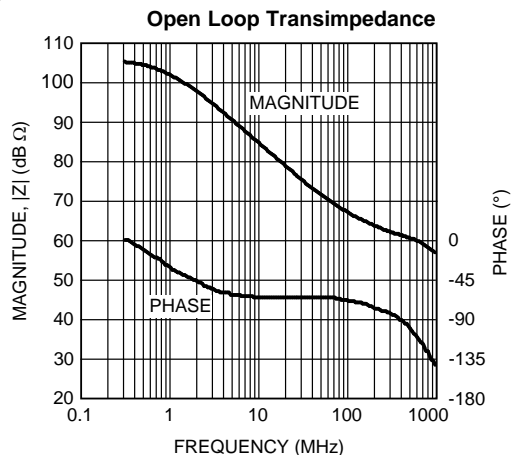


Figure 21.

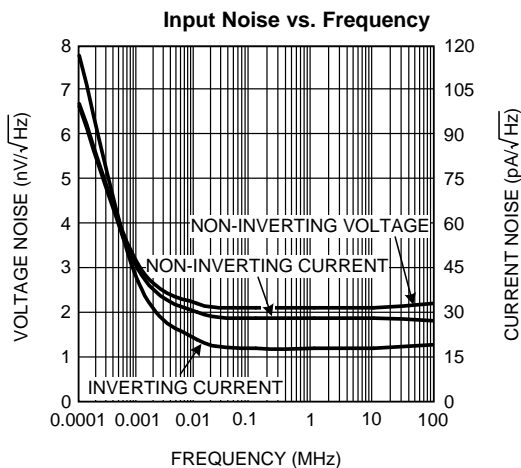


Figure 22.

Typical Performance Characteristics

$A_V = +2$ ,  $V_{CC} = \pm 5V$ ,  $R_L = 100\Omega$ ,  $R_F = 383\Omega$ ; unless otherwise specified).

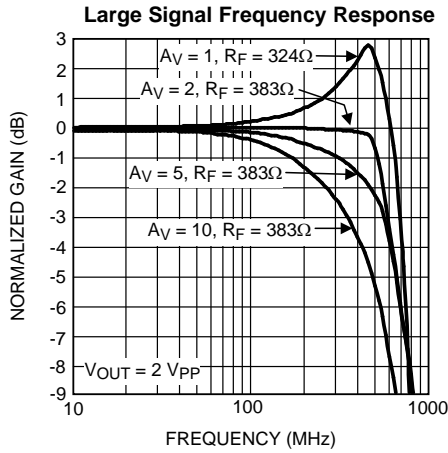


Figure 23.

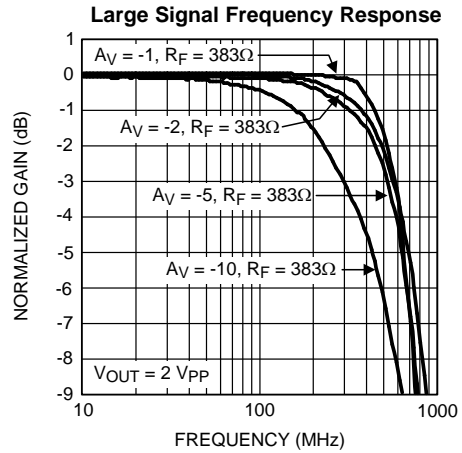


Figure 24.

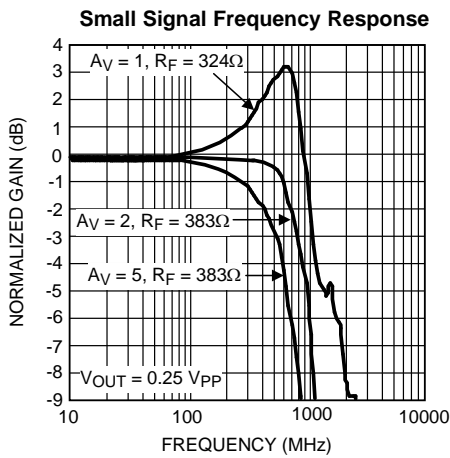


Figure 25.

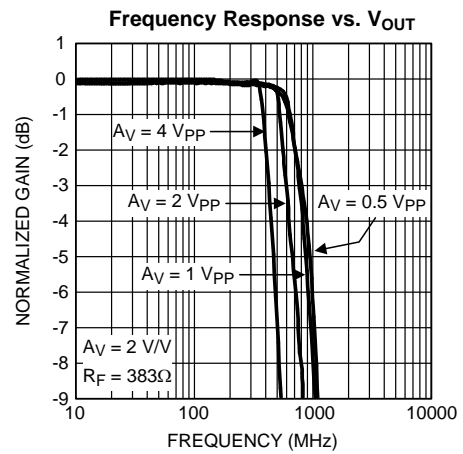


Figure 26.

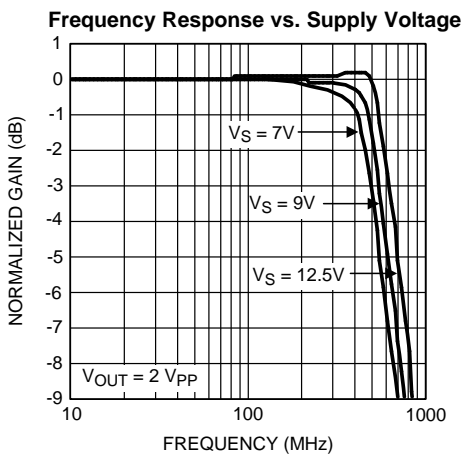


Figure 27.

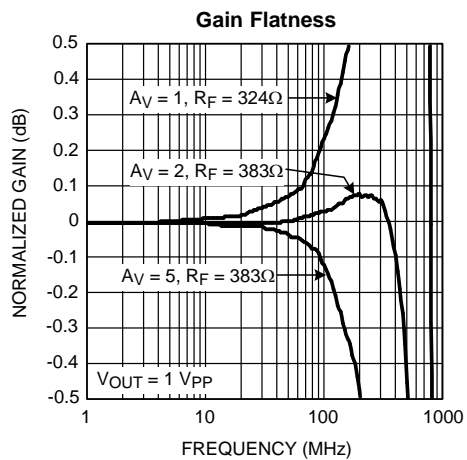


Figure 28.

Typical Performance Characteristics (continued)

$A_V = +2$ ,  $V_{CC} = \pm 5V$ ,  $R_L = 100\Omega$ ,  $R_F = 383\Omega$ ; unless otherwise specified).

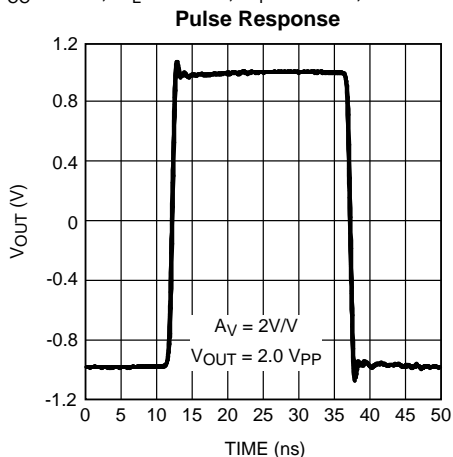


Figure 29.

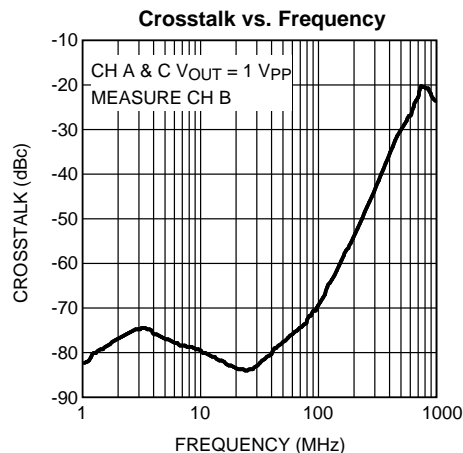


Figure 30.

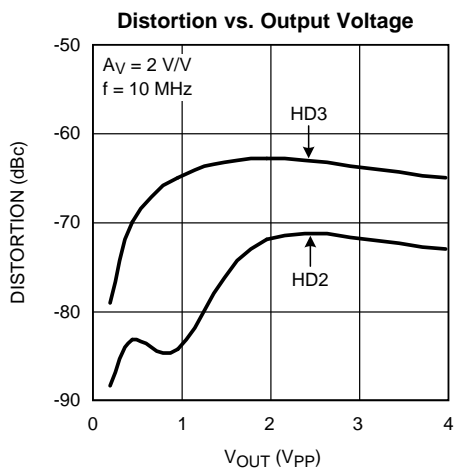


Figure 31.

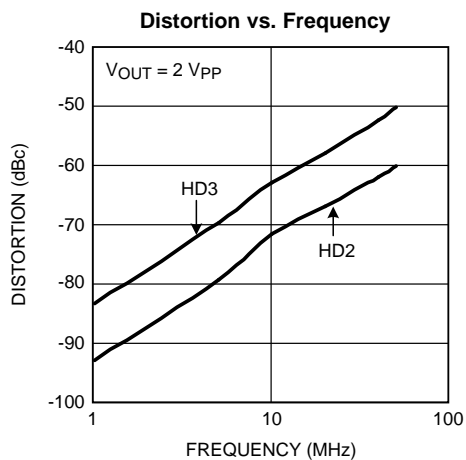


Figure 32.

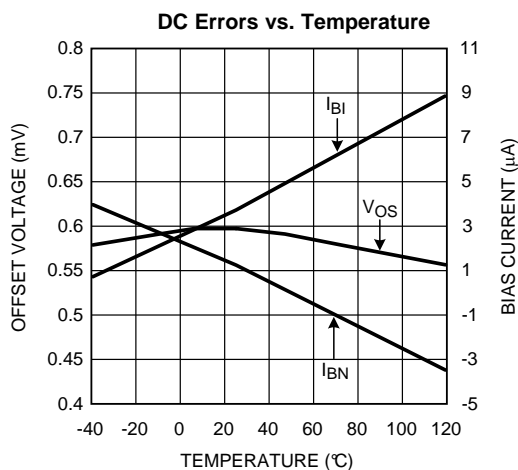
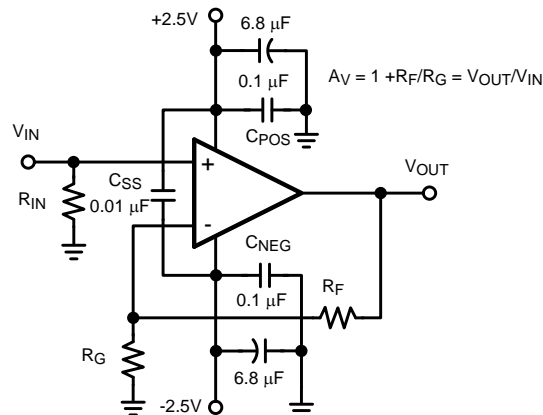
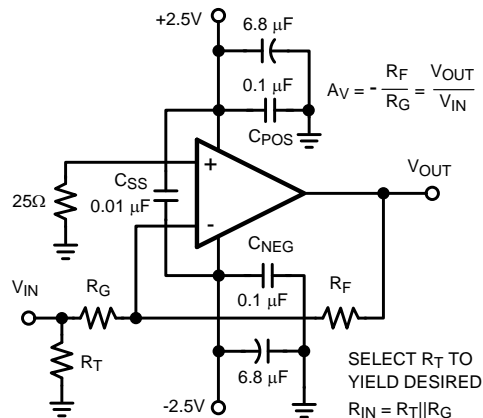


Figure 33.

## APPLICATION INFORMATION



**Figure 34. Recommended Non-Inverting Gain Circuit**



**Figure 35. Recommended Inverting Gain Circuit**

### General Information

The LMH6733 is a high speed current feedback amplifier, optimized for very high speed and low distortion. The LMH6733 has no internal ground reference so single or split supply configurations are both equally useful.

### Feedback Resistor Selection

One of the key benefits of a current feedback operational amplifier is the ability to maintain optimum frequency response independent of gain by using the appropriate values for the feedback resistor ( $R_F$ ). The Electrical Characteristics and Typical Performance plots specify an  $R_F$  of 340Ω, a gain of +2 V/V and ±2.5V power supplies (unless otherwise specified). Generally, lowering  $R_F$  from its recommended value will peak the frequency response and extend the bandwidth while increasing the value of  $R_F$  will cause the frequency response to roll off faster. Reducing the value of  $R_F$  too far below its recommended value will cause overshoot, ringing and, eventually, oscillation.

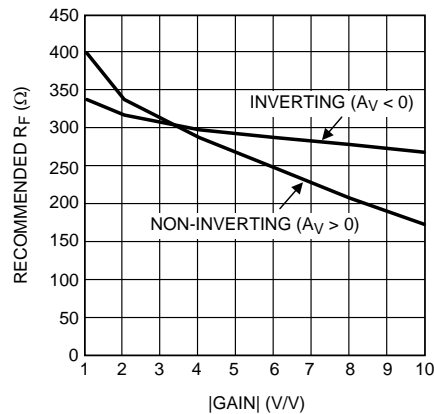


Figure 36. Recommended R<sub>F</sub> vs. Gain

See Figure 36 for selecting a feedback resistor value for gains of  $\pm 1$  to  $\pm 10$ . Since each application is slightly different it is worth some experimentation to find the optimal R<sub>F</sub> for a given circuit. In general a value of R<sub>F</sub> that produces about 0.1 dB of peaking is the best compromise between stability and maximal bandwidth. Note that it is not possible to use a current feedback amplifier with the output shorted directly to the inverting input. The buffer configuration of the LMH6733 requires a 324Ω feedback resistor for stable operation.

The LMH6733 has been optimized for high speed operation. As shown in Figure 36 the suggested value for R<sub>F</sub> decreases for higher gains. Due to the impedance of the input buffer there is a practical limit for how small R<sub>F</sub> can go, based on the lowest practical value of R<sub>G</sub>. This limitation applies to both inverting and non-inverting configurations. For the LMH6733 the input resistance of the inverting input is approximately 30Ω and 20Ω is a practical (but not hard and fast) lower limit for R<sub>G</sub>. The LMH6733 begins to operate in a gain bandwidth limited fashion in the region where R<sub>G</sub> is nearly equal to the input buffer impedance. Note that the amplifier will operate with R<sub>G</sub> values well below 20Ω, however results may be substantially different than predicted from ideal models. In particular the voltage potential between the inverting and non-inverting inputs cannot be expected to remain small.

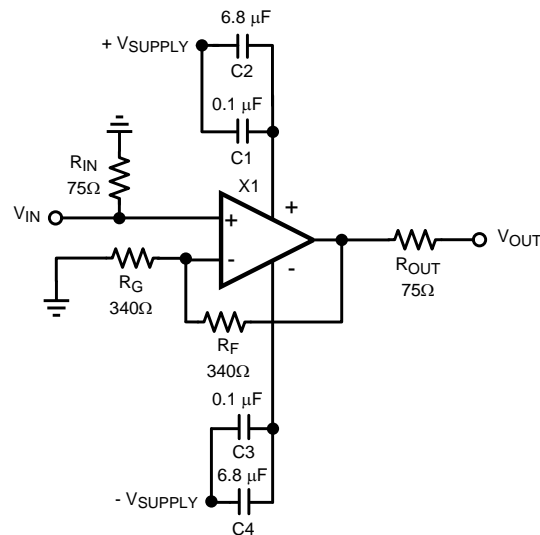
Inverting gain applications that require impedance matched inputs may limit gain flexibility somewhat (especially if maximum bandwidth is required). The impedance seen by the source is R<sub>G</sub> || R<sub>T</sub> (R<sub>T</sub> is optional). The value of R<sub>G</sub> is R<sub>F</sub> / gain. Thus for an inverting gain of  $-5$  V/V and an optimal value for R<sub>F</sub> the input impedance is equal to 55Ω. Using a termination resistor this can be brought down to match a 25Ω source; however, a 150Ω source cannot be matched. To match a 150Ω source would require using a 1050Ω feedback resistor and would result in reduced bandwidth.

For more information see Application Note OA-13 which describes the relationship between R<sub>F</sub> and closed-loop frequency response for current feedback operational amplifiers. The value for the inverting input impedance for the LMH6733 is approximately 30Ω. The LMH6733 is designed for optimum performance at gains of +1 to +10 V/V and  $-1$  to  $-9$  V/V. Higher gain configurations are still useful; however, the bandwidth will fall as gain is increased, much like a typical voltage feedback amplifier.

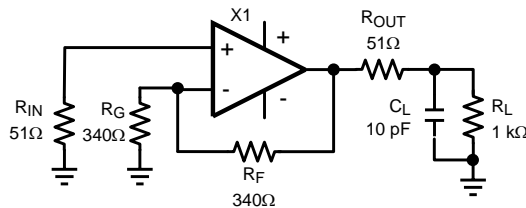
### Active Filter

The choice of reactive components requires much attention when using any current feedback operational amplifier as an active filter. Reducing the feedback impedance, especially at higher frequencies, will almost certainly cause stability problems. Likewise capacitance on the inverting input should be avoided. See Application Notes OA-07 and OA-26 for more information on Active Filter applications for Current Feedback Op Amps.

When using the LMH6733 as a low pass filter the value of R<sub>F</sub> can be substantially reduced from the value recommended in the R<sub>F</sub> vs. Gain charts. The benefit of reducing R<sub>F</sub> is increased gain at higher frequencies, which improves attenuation in the stop band. Stability problems are avoided because in the stop band additional device bandwidth is used to cancel the input signal rather than amplify it. The benefit of this change depends on the particulars of the circuit design. With a high pass filter configuration reducing R<sub>F</sub> will likely result in device instability and is not recommended.



**Figure 37. Typical Video Application**



**Figure 38. Decoupling Capacitive Loads**

## Driving Capacitive Loads

Capacitive output loading applications will benefit from the use of a series output resistor  $R_{OUT}$ . shows the use of a series output resistor,  $R_{OUT}$ , to stabilize the amplifier output under capacitive loading. Capacitive loads of 5 to 120 pF are the most critical, causing ringing, frequency response peaking and possible oscillation. The chart “Frequency Response vs. Capacitive Load” give a recommended value for selecting a series output resistor for mitigating capacitive loads. The values suggested in the charts are selected for .5 dB or less of peaking in the frequency response. This gives a good compromise between settling time and bandwidth. For applications where maximum frequency response is needed and some peaking is tolerable, the value of  $R_{OUT}$  can be reduced slightly from the recommended values.

## CAT5 High Definition Video Transmission

The LMH6733 can be used to send component 1080i High Definition (HD) video over CAT5 twisted-pairs. As shown [Figure 39](#) , the LMH6733 can be utilized to perform all three video transmitter, video receiver, and equalization circuitry. The equalization circuitry enhances the video signal to accomodate for the CAT5 attenuation over various cable lengths. Refer to application note [AN-1822](#) for more details regarding this application.

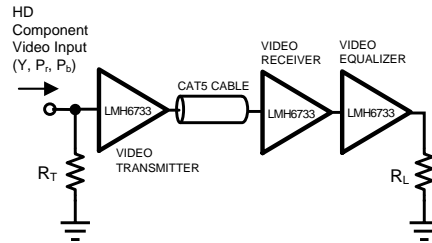


Figure 39. CAT5 High Definition Video Transmission

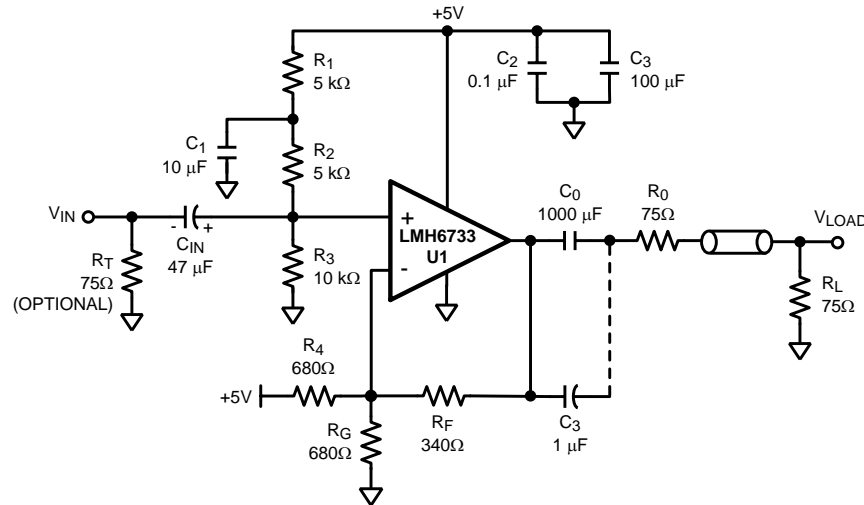


Figure 40. AC Coupled Single Supply Video Amplifier

### AC-Coupled Video

The LMH6733 can be used as an AC-coupled single supply video amplifier for driving 75Ω coax with a gain of 2. The input signal is nominally 0.7V or 1.0V for component Y<sub>P<sub>R</sub>B</sub> and RGB, depending on the presence of a sync. R<sub>1</sub>, R<sub>2</sub>, and R<sub>3</sub> simply set the input to the center of the input linear range while C<sub>IN</sub> AC couples the video onto the op amp's input.

As can be seen in , Figure 40 amplifier U1 is used in a positive gain configuration set for a closed loop gain of 2. The feedback resistor R<sub>F</sub> is 340Ω. The gain resistor is created from the parallel combination of R<sub>G</sub> and R<sub>4</sub>, giving a Thevenin equivalent of 340Ω connected to 2.5V.

The 75Ω back termination resistor R<sub>O</sub> divides the signal such that V<sub>OUT</sub> equals a buffered version of V<sub>IN</sub>. The back termination will eliminate any reflection of the signal that comes from the load. The input termination resistor, R<sub>T</sub>, is optional – it is used only if matching of the incoming line is necessary. In some applications, it is recommended that a small valued ceramic capacitor be used in parallel with C<sub>O</sub> which is itself electrolytic because of its rather large value. The ceramic cap will tend to shunt the inductive behavior of this electrolytic cap, C<sub>O</sub>, at higher frequencies for an improved overall, low-impedance output.

### Inverting Input Parasitic Capacitance

Parasitic capacitance is any capacitance in a circuit that was not intentionally added. It comes about from electrical interaction between conductors. Parasitic capacitance can be reduced but never entirely eliminated. Most parasitic capacitances that cause problems are related to board layout or lack of termination on transmission lines. Please see the section on [Layout Considerations](#) for hints on reducing problems due to parasitic capacitances on board traces. Transmission lines should be terminated in their characteristic impedance at both ends.

High speed amplifiers are sensitive to capacitance between the inverting input and ground or power supplies. This shows up as gain peaking at high frequency. The capacitor raises device gain at high frequencies by making  $R_G$  appear smaller. Capacitive output loading will exaggerate this effect. In general, avoid introducing unnecessary parasitic capacitance at both the inverting input and the output.

One possible remedy for this effect is to slightly increase the value of the feedback (and gain set) resistor. This will tend to offset the high frequency gain peaking while leaving other parameters relatively unchanged. If the device has a capacitive load as well as inverting input capacitance using a series output resistor as described in the section on “[Driving Capacitive Loads](#)” will help.

## Layout Considerations

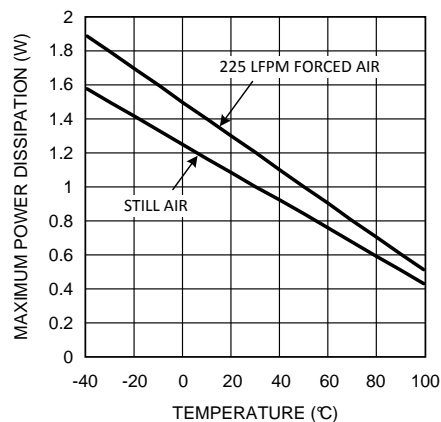
Whenever questions about layout arise, use the evaluation board as a guide. The LMH730275 is the evaluation board supplied with samples of the LMH6733.

To reduce parasitic capacitances ground and power planes should be removed near the input and output pins. Components in the feedback loop should be placed as close to the device as possible. For long signal paths controlled impedance lines should be used, along with impedance matching elements at both ends.

Bypass capacitors should be placed as close to the device as possible. Bypass capacitors from each rail to ground are applied in pairs. The larger electrolytic bypass capacitors can be located farther from the device, the smaller ceramic capacitors should be placed as close to the device as possible. The LMH6733 has multiple power and ground pins for enhanced supply bypassing. Every pin should ideally have a separate bypass capacitor. Sharing bypass capacitors may slightly degrade second order harmonic performance, especially if the supply traces are thin and /or long. In [Figure 34](#) and [Figure 35](#)  $C_{SS}$  is optional, but is recommended for best second harmonic distortion. Another option to using  $C_{SS}$  is to use pairs of .01  $\mu\text{F}$  and .1  $\mu\text{F}$  ceramic capacitors for each supply bypass.

## Video Performance

The LMH6733 has been designed to provide excellent performance with production quality video signals in a wide variety of formats such as HDTV and High Resolution VGA. NTSC and PAL performance is nearly flawless. Best performance will be obtained with back terminated loads. The back termination reduces reflections from the transmission line and effectively masks transmission line and other parasitic capacitances from the amplifier output stage. [Figure 37](#) shows a typical configuration for driving a 75 $\Omega$  cable. The amplifier is configured for a gain of two to make up for the 6 dB of loss in  $R_{OUT}$ .



**Figure 41. Maximum Power Dissipation**



## Power Dissipation

The LMH6733 is optimized for maximum speed and performance in the small form factor of the standard SSOP-16 package. To achieve its high level of performance, the LMH6733 consumes an appreciable amount of quiescent current which cannot be neglected when considering the total package power dissipation limit. The quiescent current contributes to about 40° C rise in junction temperature when no additional heat sink is used ( $V_S = \pm 5V$ , all 3 channels on). Therefore, it is easy to see that proper precautions need to be taken in order to make sure the junction temperature's absolute maximum rating of 150°C is not violated.

To ensure maximum output drive and highest performance, thermal shutdown is not provided. Therefore, it is of utmost importance to make sure that the  $T_{JMAX}$  is never exceeded due to the overall power dissipation (all 3 channels).

With the LMH6733 used in a back-terminated 75Ω RGB analog video system (with 2  $V_{PP}$  output voltage), the total power dissipation is around 305 mW of which 220 mW is due to the quiescent device dissipation (output black level at 0V). With no additional heat sink used, that puts the junction temperature to about 120° C when operated at 85°C ambient.

To reduce the junction temperature many options are available. Forced air cooling is the easiest option. An external add-on heat-sink can be added to the SSOP-16 package, or alternatively, additional board metal (copper) area can be utilized as heat-sink.

An effective way to reduce the junction temperature for the SSOP-16 package (and other plastic packages) is to use the copper board area to conduct heat. With no enhancement the major heat flow path in this package is from the die through the metal lead frame (inside the package) and onto the surrounding copper through the interconnecting leads. Since high frequency performance requires limited metal near the device pins the best way to use board copper to remove heat is through the bottom of the package. A gap filler with high thermal conductivity can be used to conduct heat from the bottom of the package to copper on the circuit board. Vias to a ground or power plane on the back side of the circuit board will provide additional heat dissipation. A combination of front side copper and vias to the back side can be combined as well.

Follow these steps to determine the maximum power dissipation for the LMH6733:

1. Calculate the quiescent (no-load) power:

$$P_{AMP} = I_{CC} \times (V_S)$$

where

- $V_S = V^+ - V^-$  (1)

2. Calculate the RMS power dissipated in the output stage:

$$P_D (rms) = rms ((V_S - V_{OUT}) \times I_{OUT})$$

where

- $V_{OUT}$  and  $I_{OUT}$  are the voltage and the current across the external load
- $V_S$  is the total supply voltage (2)

3. Calculate the total RMS power:

$$P_T = P_{AMP} + P_D \quad (3)$$

The maximum power that the LMH6733, package can dissipate at a given temperature can be derived with the following equation (See [Figure 41](#)):

$$P_{MAX} = (150^\circ C/W - T_{AMB}) / \theta_{JA}$$

where

- $T_{AMB}$  = ambient temperature (°C)
- $\theta_{JA}$  = thermal resistance, from junction to ambient, for a given package (°C/W)
- For the SSOP package  $\theta_{JA}$  is 120°C/W (4)

## ESD Protection

The LMH6733 is protected against electrostatic discharge (ESD) on all pins. The LMH6733 will survive 2000V Human Body Model and 200V Machine Model events.

Under closed loop operation the ESD diodes have no affect on circuit performance. There are occasions, however, when the ESD diodes will be evident. If the LMH6733 is driven by a large signal while the device is powered down the ESD diodes will conduct.

The current that flows through the ESD diodes will either exit the chip through the supply pins or will flow through the device, hence it is possible to power up a chip with a large signal applied to the input pins. Shorting the power pins to each other will prevent the chip from being powered up through the input.

## Evaluation Boards

Texas Instruments provides the following evaluation boards as a guide for high frequency layout and as an aid in device testing and characterization. Many of the datasheet plots were measured with these boards.



Device	Package	Evaluation Board Part Number
LMH6733MQ	SSOP	LMH730275

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**REVISION HISTORY**

<b>Changes from Revision C (April 2013) to Revision D</b>	<b>Page</b>
<hr/> <ul style="list-style-type: none"><li>• Changed layout of National Data Sheet to TI format .....</li></ul>	<hr/> <b>18</b>

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMH6733MQ/NOPB	ACTIVE	SSOP	DBQ	16	95	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LH67 33MQ	
LMH6733MQX/NOPB	ACTIVE	SSOP	DBQ	16	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LH67 33MQ	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH6733MQX/NOPB	SSOP	DBQ	16	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH6733MQX/NOPB	SSOP	DBQ	16	2500	356.0	356.0	35.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
LMH6733MQ/NOPB	DBQ	SSOP	16	95	495	8	4064	3.05





# PACKAGE OUTLINE

## DBQ0016A

### SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



#### NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MO-137, variation AB.

# EXAMPLE BOARD LAYOUT

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

4214846/A 03/2014

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.127 MM] THICK STENCIL  
SCALE:8X

4214846/A 03/2014

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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