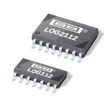


LOG112
LOG2112

SBOS246D – JUNE 2002 – REVISED APRIL 2005

Precision
LOGARITHMIC AND LOG RATIO AMPLIFIERS

FEATURES

- EASY-TO-USE COMPLETE FUNCTION
- OUTPUT SCALING AMPLIFIER
- ON-CHIP 2.5V VOLTAGE REFERENCE
- HIGH ACCURACY: 0.2% FSO Over 5 Decades
- WIDE INPUT DYNAMIC RANGE: 7.5 Decades, 100pA to 3.5mA
- LOW QUIESCENT CURRENT: 1.75mA
- WIDE SUPPLY RANGE: ±4.5V to ±18V
- PACKAGES: SO-14 (narrow) and SO-16

APPLICATIONS

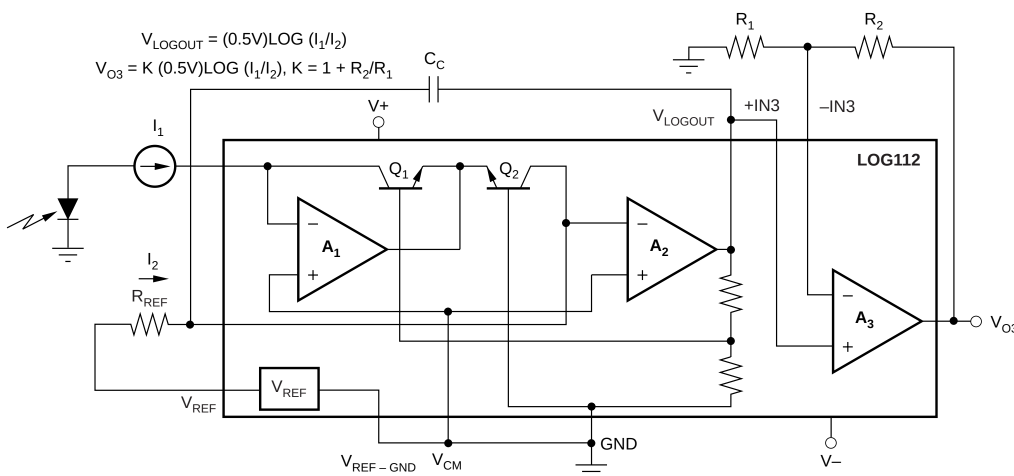
- LOG, LOG RATIO: Communication, Analytical, Medical, Industrial, Test, General Instrumentation
- PHOTODIODE SIGNAL COMPRESSION AMP
- ANALOG SIGNAL COMPRESSION IN FRONT OF ANALOG-TO-DIGITAL (A/D) CONVERTER
- ABSORBANCE MEASUREMENT
- OPTICAL DENSITY MEASUREMENT

DESCRIPTION

The LOG112 and LOG2112 are versatile integrated circuits that compute the logarithm or log ratio of an input current relative to a reference current. V_{LOGOUT} of the LOG112 and LOG2112 are trimmed to 0.5V per decade of input current, ensuring high precision over a wide dynamic range of input signals.

The LOG112 and LOG2112 features a 2.5V voltage reference that may be used to generate a precision current reference using an external resistor.

Low DC offset voltage and temperature drift allow accurate measurement of low-level signals over the specified temperature range of –5°C to +75°C.



NOTE: Internal resistors are used to compensate gain change over temperature.
The V_{CM} pin is internally connected to GND in the LOG2112.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage, V+ to V–	±18V
Inputs	±18V
Input Current	±10mA
Output Short-Circuit Current[2]	Continuous
Operating Temperature	–40°C to +85°C
Storage Temperature	–55°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

NOTES: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. (2) One output per package.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

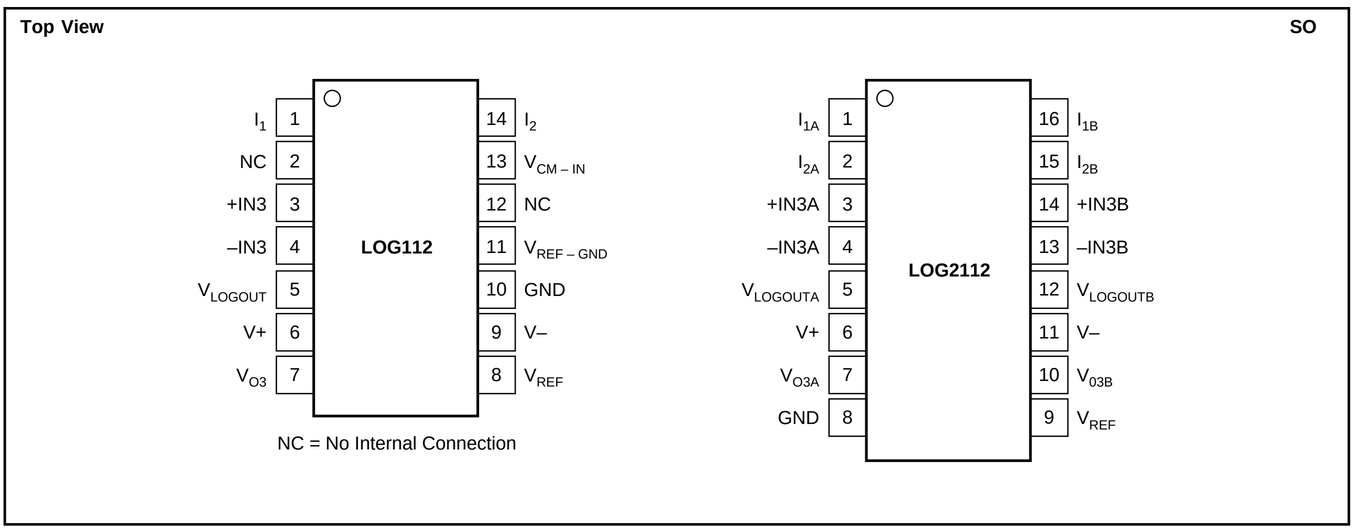
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION[1]

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING
LOG112	SO-14	D	LOG112A
LOG2112	SO-16	DW	LOG2112A

NOTES: (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

PIN CONFIGURATION



ELECTRICAL CHARACTERISTICS

Boldface limits apply over the specified temperature range, T_A = –5°C to +75°C.

At T_A = +25°C, V_S = ±5V, and R_{OUT} = 10kΩ, unless otherwise noted.

PARAMETER	CONDITION	LOG112, LOG2112 MIN	TYP	MAX	UNITS
CORE LOG FUNCTION					
V_{IN}/V_{OUT} Equation		V_{LOGOUT} = (0.5V)LOG (I_1/I_2)			V
LOG CONFORMITY ERROR(1)					
Initial	1nA to 100µA (5 decades)		0.01	0.2	%
	100pA to 3.5mA (7.5 decades)		0.13		%
over Temperature	**1nA to 100µA (5 decades)**		0.0001		**%/°C**
	100pA to 3.5mA (7.5 decades)		0.005		**%/°C**
GAIN(2)					
Initial Value	1nA to 100µA		0.5		V/decade
Gain Error	1nA to 100µA		0.10	±1	%
vs Temperature	**T_{MIN} to T_{MAX}**		**0.003**	**0.01**	**%/°C**
INPUT, A_{1A} and A_{1B}, A_{2A}, A_{2B}					
Offset Voltage			±0.3	±1.5	mV
vs Temperature	**T_{MIN} to T_{MAX}**		**±2**		**µV/°C**
vs Power Supply (PSRR)	V_S = ±4.5V to ±18V		5	20	µV/V
Input Bias Current			±5		pA
vs Temperature	**T_{MIN} to T_{MAX}**		**Doubles Every 10°C**		
Voltage Noise	f = 10Hz to 10kHz		3		µVrms
	f = 1kHz		30		nV/√Hz
Current Noise	f = 1kHz		4		fA/√Hz
Common-Mode Voltage Range (Positive)		(V+) – 2	(V+) – 1.5		V
(Negative)		(V–) + 2	(V–) + 1.2		V
Common-Mode Rejection Ratio (CMRR)			10		µV/V
OUTPUT, ($V_{LOG\ OUT}$) A_{2A}, A_{2B}					
Output Offset, V_{OSO}, Initial			±3	±15	mV
vs Temperature	**T_{MIN} to T_{MAX}**		**±10**		**µV/°C**
Full-Scale Output (FSO)	V_S = ±5V	(V–) + 1.2		(V+) – 1.5	V
Short-Circuit Current			±18		mA
TOTAL ERROR(3)(4)	I_1 or I_2 remains fixed while other varies.				
Initial	Min to Max				
	I_1 or I_2 = 5mA (V_S ≥ ±6V)			±150	mV
	I_1 or I_2 = 3.5mA			±75	mV
	I_1 or I_2 = 1mA			±20	mV
	I_1 or I_2 = 100µA			±20	mV
	I_1 or I_2 = 10µA			±20	mV
	I_1 or I_2 = 1µA			±20	mV
	I_1 or I_2 = 100nA			±20	mV
	I_1 or I_2 = 10nA			±20	mV
	I_1 or I_2 = 1nA			±20	mV
	I_1 or I_2 = 350pA			±20	mV
	I_1 or I_2 = 100pA			±20	mV
vs Temperature	**I_1 or I_2 = 3.5mA**		**±1.2**		**mV/°C**
	I_1 or I_2 = 1mA		**±0.4**		**mV/°C**
	I_1 or I_2 = 100µA		**±0.1**		**mV/°C**
	I_1 or I_2 = 10µA		**±0.05**		**mV/°C**
	I_1 or I_2 = 1µA		**±0.05**		**mV/°C**
	I_1 or I_2 = 100nA		**±0.09**		**mV/°C**
	I_1 or I_2 = 10nA		**±0.2**		**mV/°C**
	I_1 or I_2 = 1nA		**±0.3**		**mV/°C**
	I_1 or I_2 = 350pA		**±0.1**		**mV/°C**
	I_1 or I_2 = 100pA		**±0.3**		**mV/°C**
vs Supply	I_1 or I_2 = 3.5mA		±3.0		mV/V
	I_1 or I_2 = 1mA		±0.1		mV/V
	I_1 or I_2 = 100µA		±0.1		mV/V
	I_1 or I_2 = 10µA		±0.1		mV/V
	I_1 or I_2 = 1µA		±0.1		mV/V
	I_1 or I_2 = 100nA		±0.1		mV/V
	I_1 or I_2 = 10nA		±0.1		mV/V
	I_1 or I_2 = 1nA		±0.25		mV/V
	I_1 or I_2 = 350pA		±0.1		mV/V
	I_1 or I_2 = 100pA		±0.1		mV/V

NOTES: (1) Log Conformity Error is the peak deviation from the best-fit-straight line of V_O versus LOG (I_1/I_2) curve expressed as a percent of peak-to-peak full-scale output. K, scale factor, equals 0.5V output per decade of input current. (2) Scale factor of core log function is trimmed to 0.5V output per decade change of input current. (3) Worst-case Total Error for any ratio of I_1/I_2, as the largest of the two errors, when I_1 and I_2 are considered separately. (4) Total Error includes offset voltage, bias current, gain, and log conformity. (5) Bandwidth (3dB) and transient response are a function of both the compensation capacitor and the level of input current.

ELECTRICAL CHARACTERISTICS (Cont.)

Boldface limits apply over the specified temperature range, **T_A = –5°C to +75°C.**

At T_A = +25°C, V_S = ±5V, and R_L = 10kΩ, unless otherwise noted.

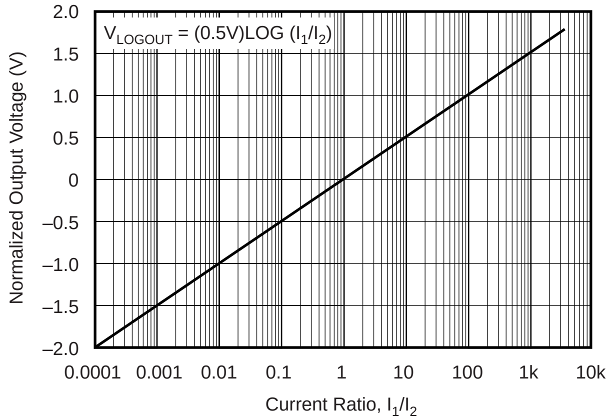
PARAMETER	CONDITION	LOG112, LOG2112 MIN	TYP	MAX	UNITS
FREQUENCY RESPONSE, CORE LOG[5]					
BW, 3dB					
I_2 = 10nA	C_C = 4500pF		0.1		kH
I_2 = 1µA	C_C = 150pF		38		kH
I_2 = 10µA	C_C = 150pF		40		kH
I_2 = 1mA	C_C = 50pF		45		kHz
Step Response					
Increasing					
I_1 = 10nA to 100nA	C_C = 120pF, I_2 = 31.6nA		1.1		ms
I_1 = 1µA to 100µA	C_C = 375pF, I_2 = 10µA		1.6		µs
I_1 = 1µA to 1mA	C_C = 950pF, I_2 = 31.6µA		1.5		µs
Decreasing					
I_1 = 100nA to 10nA	C_C = 120pF, I_2 = 31.6nA		2.1		ms
I_1 = 100µA to 1µA	C_C = 375pF, I_2 = 10µA		31.2		µs
I_1 = 1mA to 1µA	C_C = 950pF, I_2 = 31.6µA		39		µs
Increasing					
I_2 = 10nA to 100nA	C_C = 125pF, I_1 = 31.6nA		2.6		ms
I_2 = 1µA to 100µA	C_C = 750pF, I_1 = 10µA		113		µs
I_2 = 1µA to 1mA	C_C = 10.5nF, I_1 = 31.6µA		1.2		ms
Decreasing					
I_2 = 100nA to 10nA	C_C = 125pF, I_1 = 31.6nA		630		µs
I_2 = 100µA to 1µA	C_C = 750pF, I_1 = 10µA		6.6		µs
I_2 = 1mA to 1µA	C_C = 10.5nF, I_1 = 31.6µA		13.3		µs
OP AMP, A3					
Input Offset Voltage			+250	±1000	µV
vs Temperature	**T_{MIN} to T_{MAX}**		**±2**		**µV/°C**
vs Supply	V_S = ±4.5V to ±18V		5	50	µV/V
Input Bias Current			–10		nA
Input Offset Current			±0.5		nA
Input Voltage Range		(V–)		(V+) – 1.5	V
Input Noise, f = 0.1Hz to 10Hz			1		$µV_{PP}$
f = 1kHz			28		nV/√Hz
Open-Loop Voltage Gain			88		dB
Gain-Bandwidth Product			1.4		MHz
Slew Rate			0.5		V/µs
Settling Time, 0.01%	G = –1, 3V Step, C_L = 100pF		16		µs
Rated Output		(V–) + 1.5		(V+) – 0.9	V
Short-Circuit Current			±4		mA
VOLTAGE REFERENCE					
Bandgap Voltage			2.5		V
Error, Initial			±0.05	±0.5	%
vs Temperature	T_{MIN} to T_{MAX}		±25		ppm/°C
vs Supply	V_S = ±4.5V to ±18V		±10		ppm/V
vs Load	I_{LOAD} = 10mA		±600		ppm/mA
Short-Circuit Current			16		mA
POWER SUPPLY					
Operating Range	V_S	±4.5		±18	V
Quiescent Current	I_O = 0				
LOG112			±1.25	±1.75	mA
LOG2112			±2.5	±3.5	mA
TEMPERATURE RANGE					
Specified Range, T_{MIN} to T_{MAX}		–5		75	°C
Operating Range		–40		85	°C
Storage Range		–55		125	°C
Thermal Resistance, θ_{JA} SO-14			110		°C/W
SO-16			80		°C/W

NOTES: (1) Log Conformity Error is the peak deviation from the best-fit-straight line of V_O vs LOG(I_1/I_2) curve expressed as a percent of peak-to-peak full-scale output. K, scale factor, equals 0.5V output per decade of input current. (2) Scale factor of core log function is trimmed to 0.5V output per decade change of input current. (3) Worst-case Total Error for any ratio of I_1/I_2, as the largest of the two errors, when I_1 and I_2 are considered separately. (4) Total Error includes offset voltage, bias current, gain, and log conformity. (5) Bandwidth (3dB) and transient response are a function of both the compensation capacitor and the level of input current.

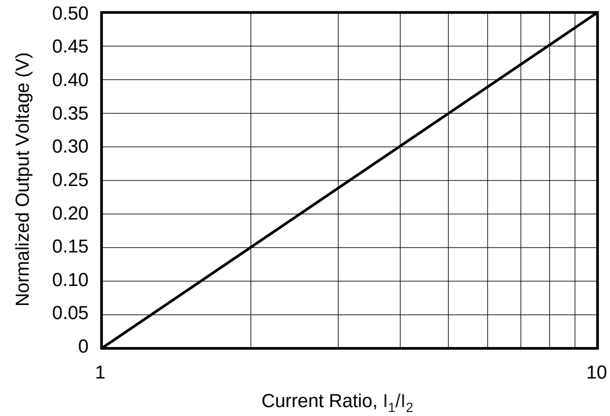
TYPICAL CHARACTERISTICS

At $T_A = +25°C$, $V_S = \pm5V$, and $R_L = 10k\Omega$, unless otherwise noted.

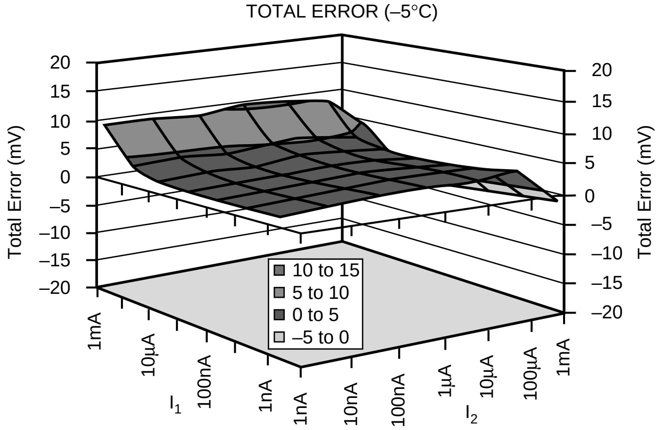
NORMALIZED TRANSFER FUNCTION



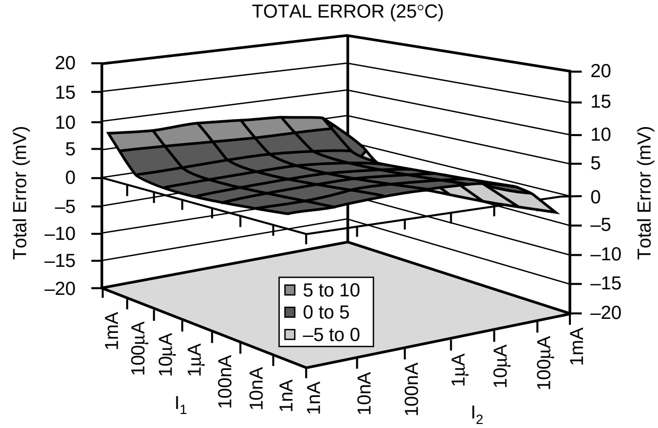
ONE CYCLE OF NORMALIZED TRANSFER FUNCTION



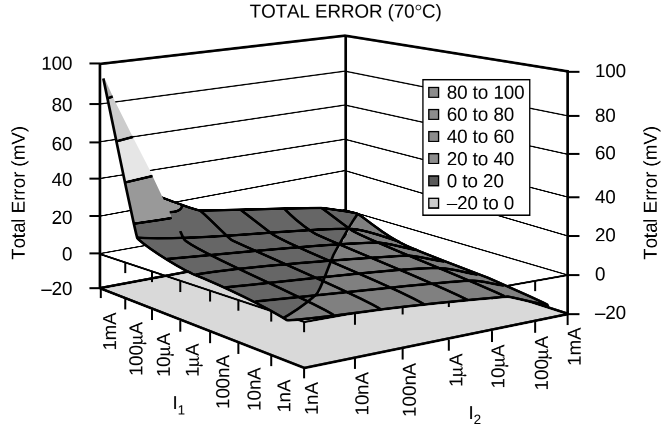
TOTAL ERROR (–5°C)



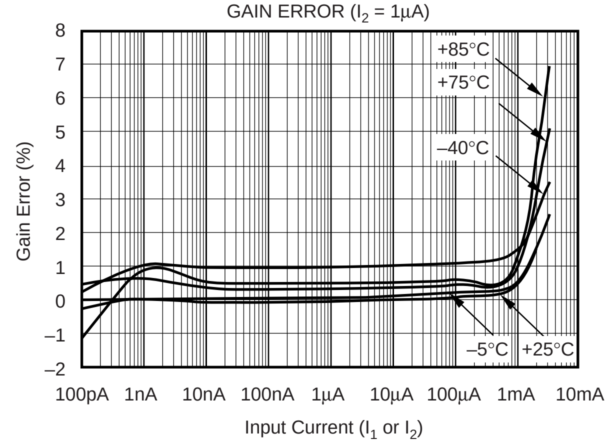
TOTAL ERROR (25°C)



TOTAL ERROR (70°C)

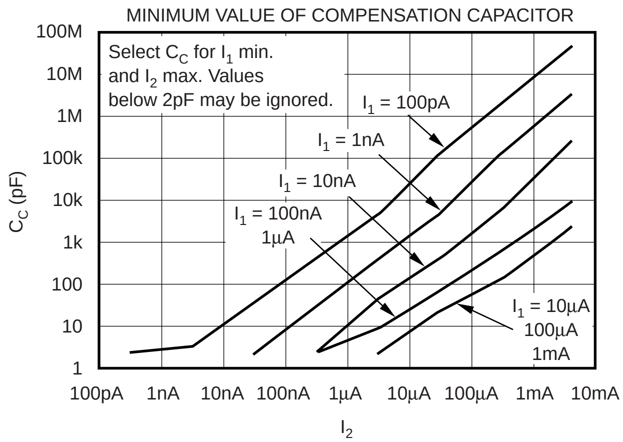


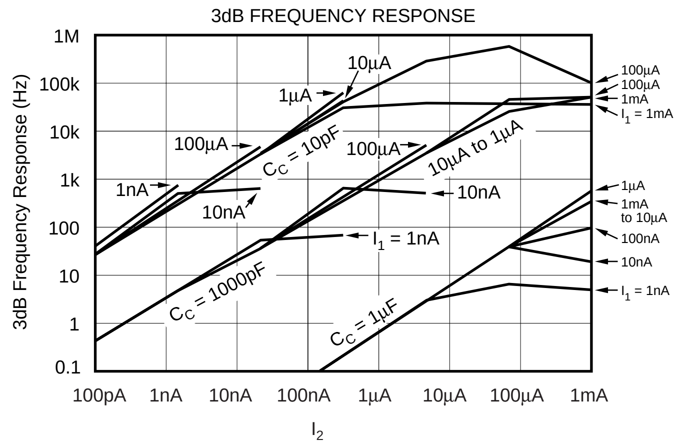
GAIN ERROR ($I_2 = 1\mu A$)

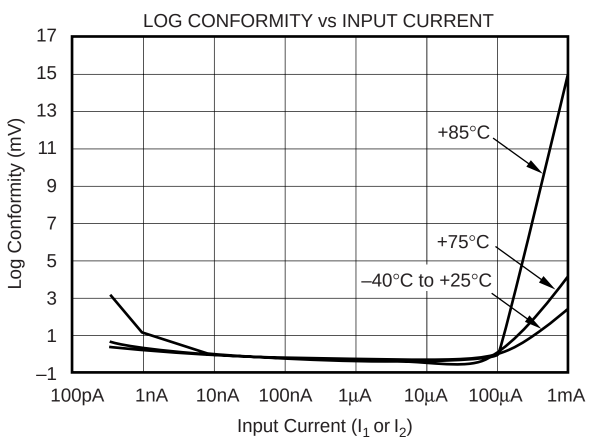


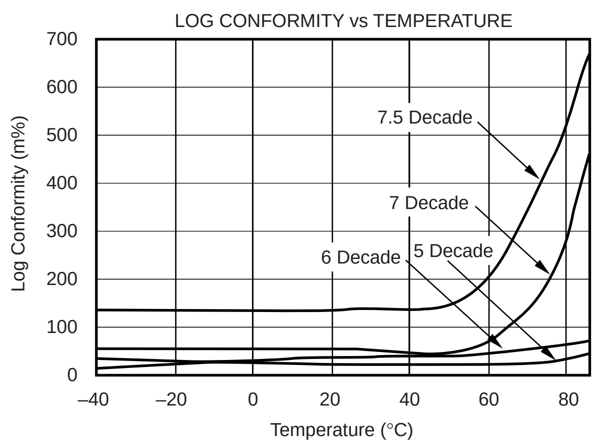
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V_S = ±5V, and R_L = 10kΩ, unless otherwise noted.









APPLICATION INFORMATION

The LOG112 is a true logarithmic amplifier that uses the base-emitter voltage relationship of bipolar transistors to compute the logarithm, or logarithmic ratio of a current ratio.

Figure 1 and Figure 2 show the basic connections required for operation of the LOG112 and LOG2112. In order to reduce the influence of lead inductance of power-supply lines, it is recommended that each supply be bypassed with a 10µF tantalum capacitor in parallel with a 1000pF ceramic capacitor, as shown in Figure 1 and Figure 2. Connecting the capacitors as close to the LOG112 and LOG2112 as possible will contribute to noise reduction as well.

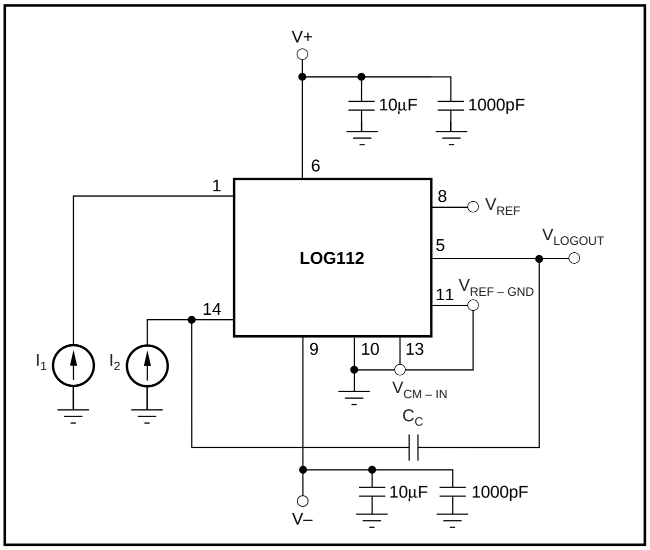


FIGURE 1. Basic Connections of the LOG112.

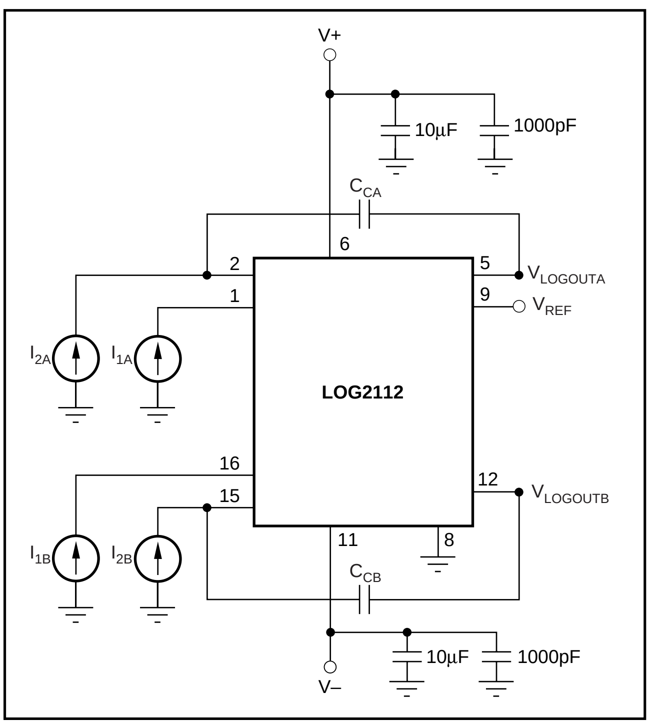


FIGURE 2. Basic Connections of the LOG2112.

INPUT CURRENT RANGE

To maintain specified accuracy, the input current range of the LOG112 and LOG2112 should be limited from 100pA to 3.5mA. Input currents outside of this range may compromise the LOG112 performance. Input currents larger than 3.5mA result in increased nonlinearity. An absolute maximum input current rating of 10mA is included to prevent excessive power dissipation that may damage the input transistor.

On ±5V supplies, the total input current ($I_1 + I_2$) is limited to 4.5mA. Due to compliance issues internal to the LOG112 and LOG2112, to accommodate larger total input currents, supplies should be increased.

SETTING THE REFERENCE CURRENT

When the LOG112 and LOG2112 are used to compute logarithms, either I_1 or I_2 can be held constant to become the reference current to which the other is compared.

V_{LOGOUT} is expressed as:

$$V_{LOGOUT} = (0.5V)LOG\ (I_1/I_{REF}) \tag{1}$$

I_{REF} can be derived from an external current source (such as that shown in Figure 3), or it may be derived from a voltage source with one or more resistors. When a single resistor is used, the value may be large depending on I_{REF}. If I_{REF} is 10nA and +2.5V is used:

$$R_{REF} = 2.5V/10nA = 250M\Omega \tag{2}$$

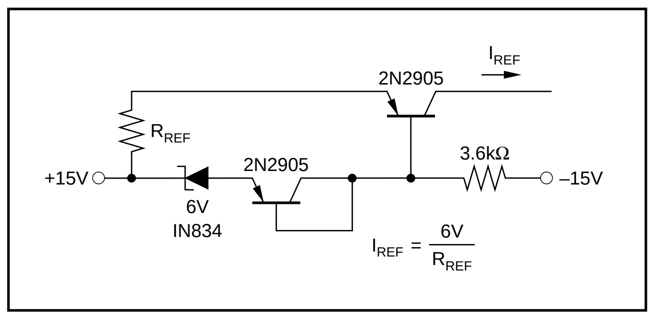


FIGURE 3. Temperature Compensated Current Source.

A voltage divider may be used to reduce the value of the resistor, as shown in Figure 4. When using this method, one must consider the possible errors caused by the amplifier's input offset voltage. The input offset voltage of amplifier A_1 has a maximum value of 1.5mV, making V_{REF} a suggested value of 100mV.

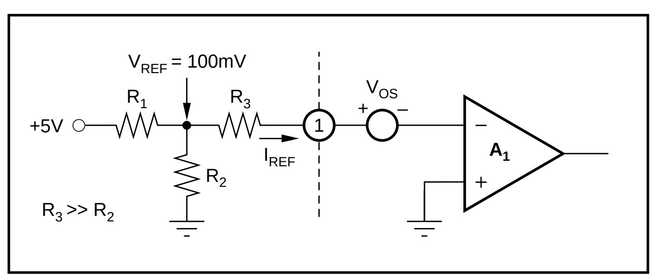


FIGURE 4. T Network for Reference Current.

Figure 5 shows a low-level current source using a series resistor. The low offset op amp reduces the effect of the LOG112 and LOG2112's input offset voltage.

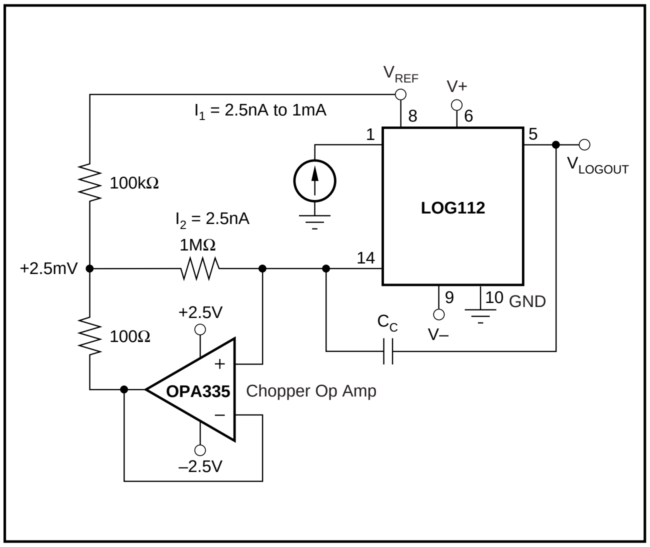


FIGURE 5. Current Source with Offset Compensation.

FREQUENCY RESPONSE

The frequency response curves seen in the Typical Characteristic curves are shown for constant DC I_1 and I_2 with a small-signal AC current on one input.

The 3dB frequency response of the LOG112 and LOG2112 are a function of the magnitude of the input current levels and of the value of the frequency compensation capacitor. See Typical Characteristic curve, *3dB Frequency Response* for details.

The transient response of the LOG112 and LOG2112 are different for increasing and decreasing signals. This is due to the fact that a log amp is a nonlinear gain element and has different gains at different levels of input signals. Smaller input currents require greater gain to maintain full dynamic range, and will slow the frequency response of the LOG112 and LOG2112.

FREQUENCY COMPENSATION

Frequency compensation for the LOG112 is obtained by connecting a capacitor between pins 5 and 14. Frequency compensation for the LOG2112 is obtained by connecting a capacitor between pins 2 and 5, or 15 and 12. The size of the capacitor is a function of the input currents, as shown in the Typical Characteristic curves (*Minimum Value of Compensation Capacitor*). For any given application, the smallest value of the capacitor which may be used is determined by the maximum value of I_2 and the minimum value of I_1. Larger values of C_C make the LOG112 and LOG2112 more stable, but reduce the frequency response.

In an application, highest overall bandwidth can be achieved by detecting the signal level at V_{OUT}, then switching in appropriate values of compensation capacitors.

NEGATIVE INPUT CURRENTS

The LOG112 and LOG2112 function only with positive input currents (conventional current flows into input current pins). In situations where negative input currents are needed, the circuits in Figures 6, 7, and 8 may be used.

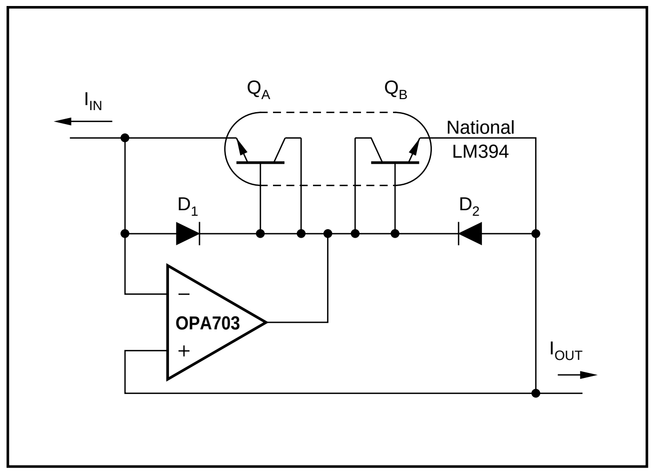


FIGURE 6. Current Inverter/Current Source.

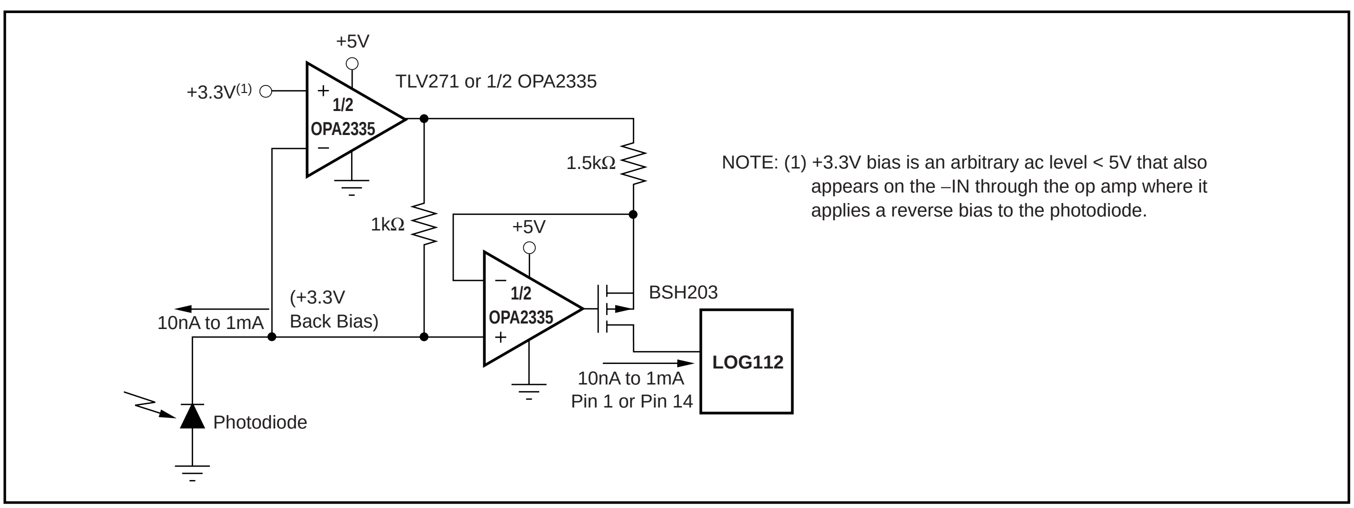


FIGURE 7. Precision Current Inverter/Current Source.

VOLTAGE INPUTS

The LOG112 and LOG2112 give the best performances with current inputs. Voltage inputs may be handled directly with series resistors, but the dynamic input range is limited to approximately three decades of input voltage by voltage noise and offsets. The transfer function of Equation 13 applies to this configuration.

ACHIEVING HIGHER ACCURACY WITH HIGHER INPUT CURRENTS

As input current to the LOG112 increases, output accuracy degrades. For a 4.5mA input current on ±5V supplies and a 10mA input current on ±12V supplies, total output error can be between 15% and 25%. Applying a common-mode voltage to V_{CM} of at least +1V and up to 2.5V, brings the log transistors out of saturation and reduces output error to approximately 10%. To avoid forward biasing a photodiode, return the cathode to the V_{CM} pin, as shown in Figure 9. To reverse bias the photodiode, apply a more positive voltage to the cathode than the anode.

APPLICATION CIRCUITS

LOG RATIO

One of the more common uses of log ratio amplifiers is to measure absorbance. See Figure 10 for a typical application.

Absorbance of the sample is $A = \log\lambda_1{}' / \lambda_1$ (3)

If D_1 and D_2 are matched $A \propto (0.5V) \log I_1/I_2$ (4)

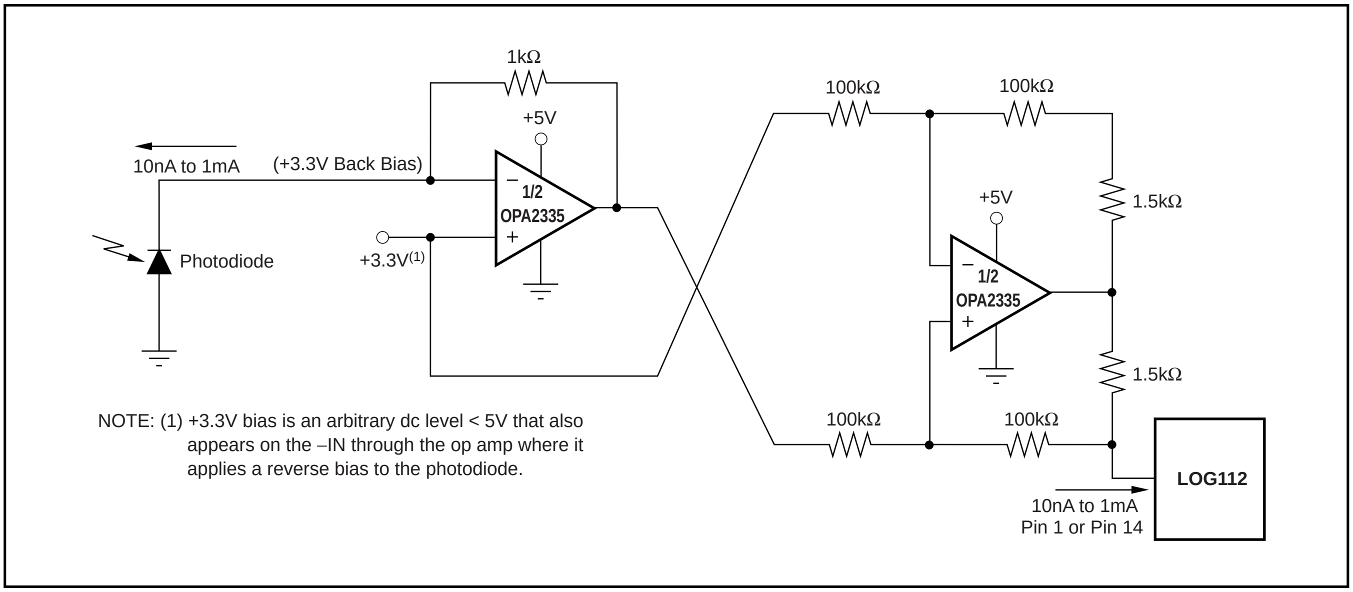


FIGURE 8. Precision Current Inverter/Current Source.

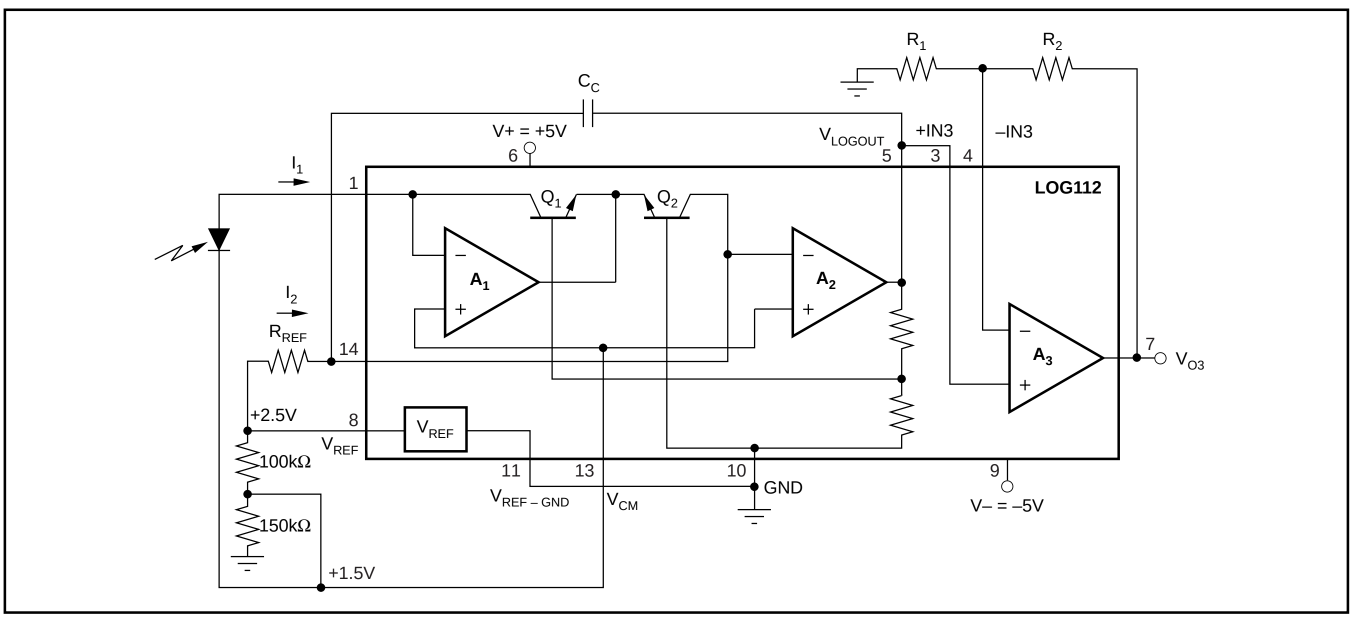


FIGURE 9. Extending Input Current Level and Improving Accuracy by Applying a Common-Mode Voltage.

DATA COMPRESSION

In many applications, the compressive effects of the logarithmic transfer function are useful. For example, a LOG112 preceding a 12-bit A/D converter can produce the dynamic range equivalent to a 20-bit converter.

OPERATION ON SINGLE SUPPLY

Many applications do not have the dual supplies required to operate the LOG112 and LOG2112. Figure 11 shows the LOG112 and LOG2112 configured for operation with a single +5V supply.

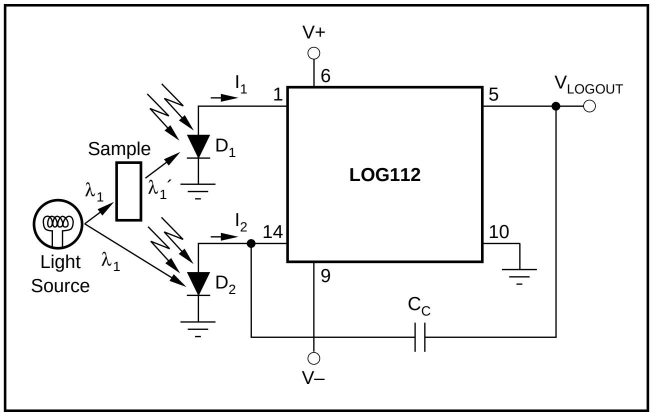


FIGURE 10. Absorbance Measurement.

MEASURING AVALANCHE PHOTODIODE CURRENT

The wide dynamic range of the LOG112 and LOG2112 is useful for measuring avalanche photodiode current (APD), as shown in Figure 12.

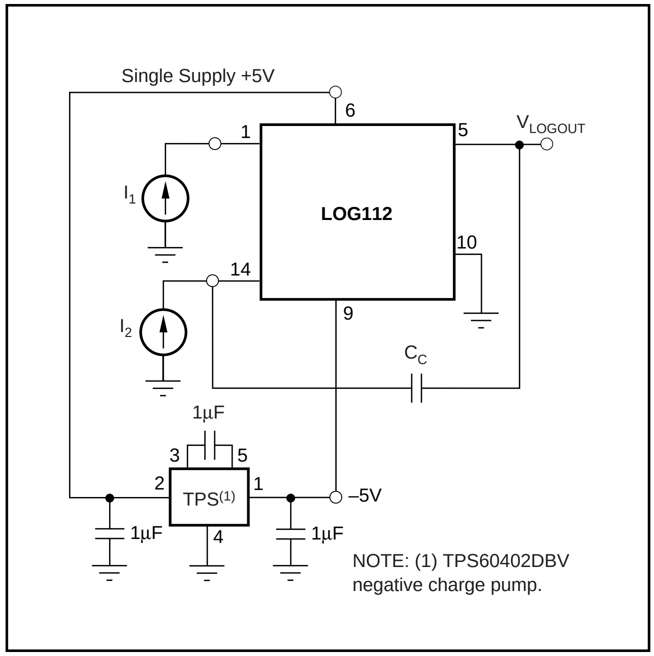


FIGURE 11. Single +5V Power-Supply Operation.

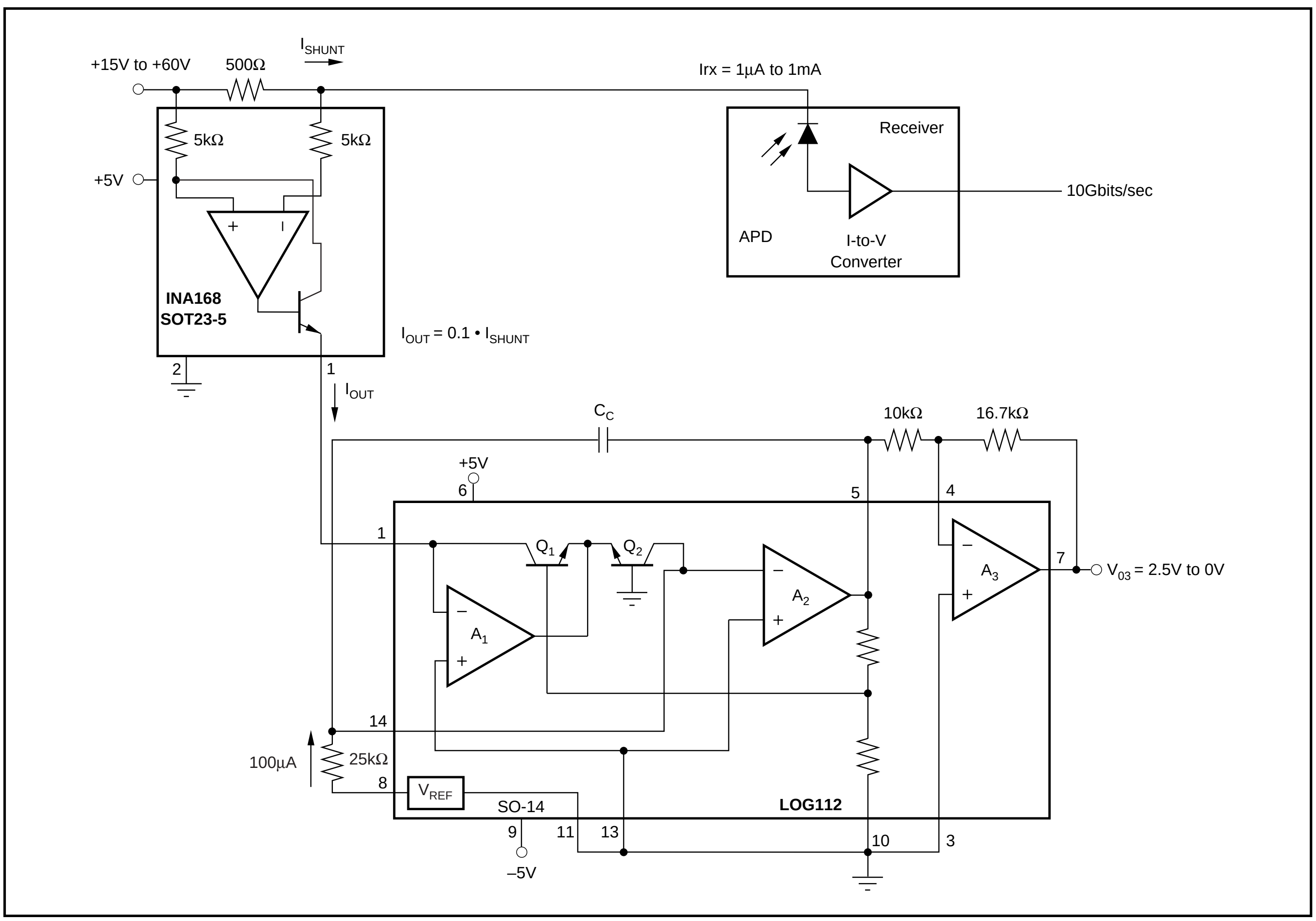


FIGURE 12. High-Side Shunt for APD Measures 3 Decades of APD Current.

INSIDE THE LOG112

Using the base-emitter voltage relationship of matched bipolar transistors, the LOG112 establishes a logarithmic function of input current ratios. Beginning with the base-emitter voltage defined as:

$$V_{BE} = V_T \ln \frac{I_C}{I_S} \quad \text{where}: V_T = \frac{kT}{q} \tag{1}$$

k = Boltzmann's constant = $1.381 \cdot 10^{-23}$

T = Absolute temperature in degrees Kelvin

q = Electron charge = $1.602 \cdot 10^{-19}$ Coulombs

I_C = Collector current

I_S = Reverse saturation current

From the circuit in Figure 12:

$$V_L = V_{BE_1} - V_{BE_2} \tag{2}$$

Substituting (1) into (2) yields:

$$V_L = V_{T_1} \ln \frac{I_1}{I_{S_1}} - V_{T_2} \ln \frac{I_2}{I_{S_2}} \tag{3}$$

If the transistors are matched and isothermal and $V_{TI} = V_{T2}$, then (3) becomes:

$$V_L = V_{T_1}\left[\ln \frac{I_1}{I_S} - \ln \frac{I_2}{I_S}\right] \tag{4}$$

$$V_L = V_T \ln \frac{I_1}{I_2} \text{ and since} \tag{5}$$

$$\ln x = 2.3 \log_{10} x \tag{6}$$

$$V_L = n\, V_T \log \frac{I_1}{I_2} \tag{7}$$

where n = 2.3 (8)

also

$$V_{OUT} = V_L \frac{R_1 + R_2}{R_1} \tag{9}$$

$$V_{OUT} = \frac{R_1 + R_2}{R_1} n\, V_T \log \frac{I_1}{I_2} \tag{10}$$

or

$$V_{OUT} = (0.5V)\text{LOG}\left(\frac{I_1}{I_2}\right) \tag{11}$$

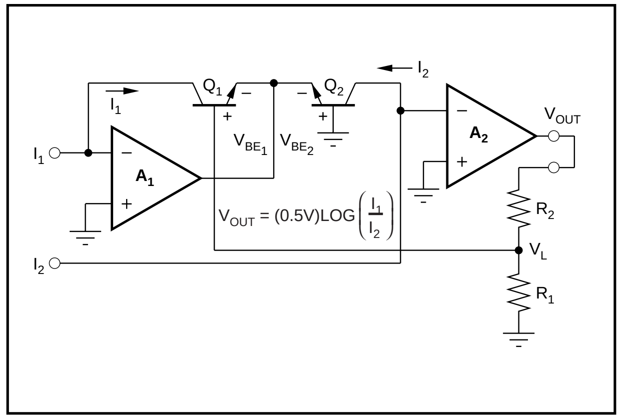


FIGURE 13. Simplified Model of a Log Amplifier.

NOTE: R_1 is a metal resistor used to compensate for gain over temperature.

DEFINITION OF TERMS

TRANSFER FUNCTION

The ideal transfer function is:

$$V_{LOGOUT} = (0.5V)\text{LOG}\ (I_1/I_2)$$

Figure 14 shows the graphical representation of the transfer over valid operating range for the LOG112 and LOG2112.

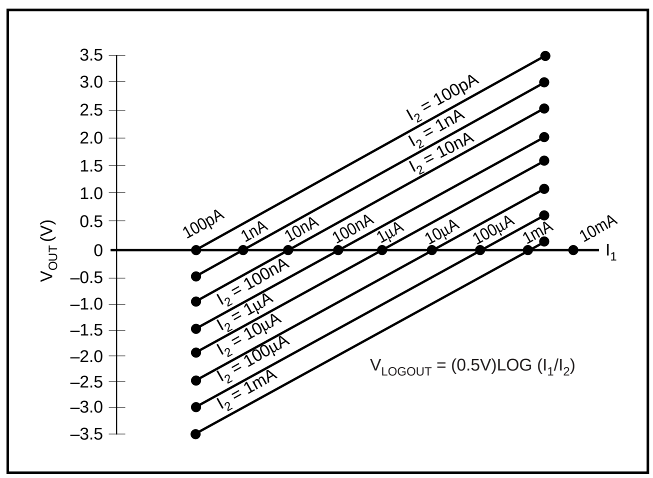


FIGURE 14. Transfer Function with Varying I_2 and I_1.

ACCURACY

Accuracy considerations for a log ratio amplifier are somewhat more complicated than for other amplifiers. This is because the transfer function is nonlinear and has two inputs, each of which can vary over a wide dynamic range. The accuracy for any combination of inputs is determined from the total error specification.

TOTAL ERROR

The total error is the deviation (expressed in mV) of the actual output from the ideal output of $V_{LOGOUT} = (0.5V)\text{LOG}\ (I_1/I_2)$. Thus,

$$V_{LOGOUT(ACTUAL)} = V_{LOGOUT(IDEAL)} \pm \text{Total Error} \tag{6}$$

It represents the sum of all the individual components of error normally associated with the log amp when operated in the current input mode. The worst-case error for any given ratio of I_1/I_2 is the largest of the two errors when I_1 and I_2 are considered separately. Temperature can affect total error.

ERRORS RTO AND RTI

As with any transfer function, errors generated by the function may be Referred-to-Output (RTO) or Referred-to-Input (RTI). In this respect, log amps have a unique property: given some error voltage at the log amp's output, that error corresponds to a constant percent of the input regardless of the actual input level.

LOG CONFORMITY

For the LOG112 and LOG2112, log conformity is calculated the same as linearity and is plotted I_1/I_2 on a semi-log scale. In many applications, log conformity is the most important specification. This is true because bias current errors are negligible (5pA compared to input currents of 100pA and above) and the scale factor and offset errors may be trimmed to zero or removed by system calibration. This leaves log conformity as the major source of error.

Log conformity is defined as the peak deviation from the best fit straight line of the V_{LOGOUT} versus log (I_1/I_2) curve. This is expressed as a percent of ideal full-scale output. Thus, the nonlinearity error expressed in volts over m decades is:

$$V_{LOGOUT\ (NONLIN)} = 0.5\text{V/dec} \bullet 2\text{NmV} \quad (7)$$

where N is the log conformity error, in percent.

INDIVIDUAL ERROR COMPONENTS

The ideal transfer function with current input is:

$$V_{LOGOUT} = (0.5\text{V})\text{LOG}\left(\frac{I_1}{I_2}\right) \quad (8)$$

The actual transfer function with the major components of error is:

$$V_{LOGOUT} = (0.5\text{V})(1 \pm \Delta K)\log\left(\frac{I_1 - I_{B1}}{I_2 - I_{B2}}\right) \pm \text{Nm} \pm V_{OSO} \quad (9)$$

The individual component of error is:

ΔK = gain error (0.10%, typ), as specified in the specification table.

I_{B1} = bias current of A_1 (5pA, typ)
I_{B2} = bias current of A_2 (5pA, typ)

N = log conformity error (0.01%, 0.13%, typ)

0.01% for m = 5, 0.13% for m = 7.5

V_{OSO} = output offset voltage (3mV, typ)

m = number of decades over which N is specified

For example, what is the error when:

$$I_1 = 1\mu\text{A and } I_2 = 100\text{nA} \quad (10)$$

$$(11)$$

$$V_{LOGOUT} = (0.5 \pm 0.001)\log\left(\frac{10^{-6} - 5 \bullet 10^{-12}}{10^{-7} - 5 \bullet 10^{-12}}\right) \pm (2)(0.0001)5 \pm 3.0\text{mV}$$
$$= 0.505\text{V}$$

Since the ideal output is 0.5V, the error as a percent of the reading is:

$$\%\ \text{error} = \frac{0.505\text{V}}{0.5} \bullet 100\% = 1.01\% \quad (12)$$

For the case of voltage inputs, the actual transfer function is:

$$(13)$$

$$V_{LOGOUT} = (0.5\text{V})(1 \pm \Delta K)\log\left(\frac{\frac{V_1}{R_1} - I_{B_1} \pm \frac{E_{OS_1}}{R_1}}{\frac{V_2}{R_2} - I_{B_2} \pm \frac{E_{OS_2}}{R_2}}\right) \pm \text{Nm} \pm V_{OSO}$$

Where $\frac{E_{OS1}}{R_1}$ and $\frac{E_{OS2}}{R_2}$ (offset error) are considered to be zero for large values of resistance from external input current sources.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LOG112AID	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	LOG112A	Samples
LOG112AIDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	LOG112A	Samples
LOG2112AIDW	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	LOG2112A	Samples
LOG2112AIDWR	ACTIVE	SOIC	DW	16	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	LOG2112A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

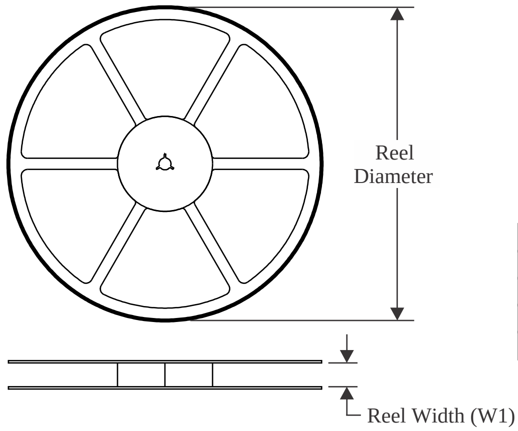
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

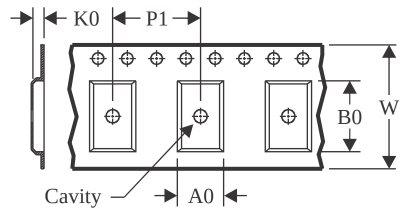
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

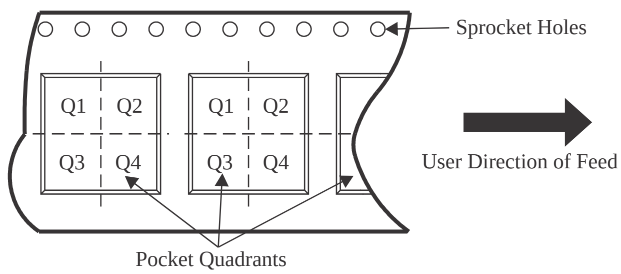


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

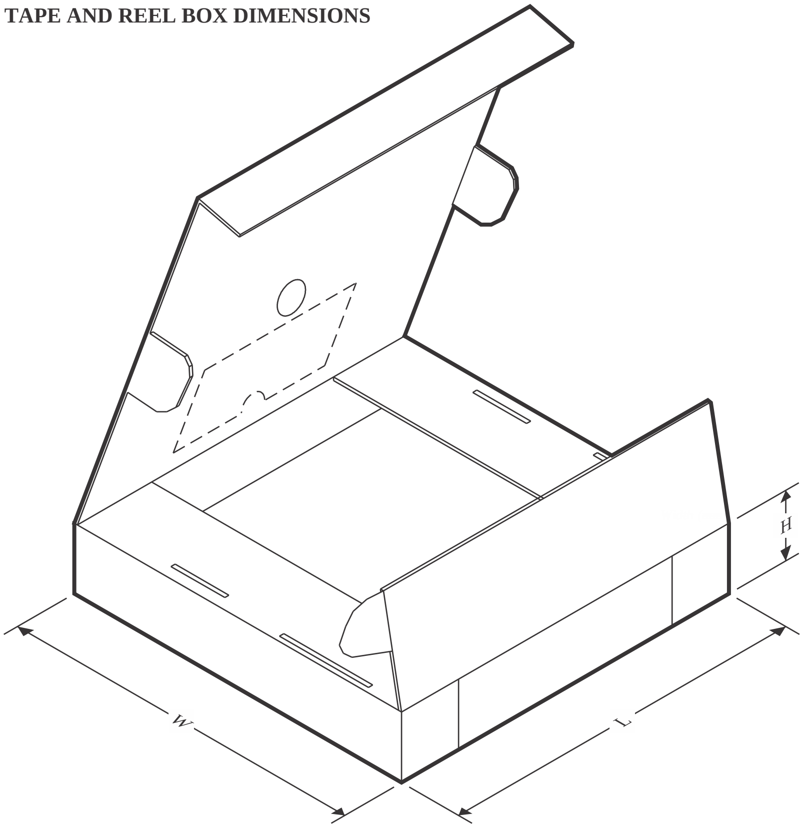
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LOG112AIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LOG2112AIDWR	SOIC	DW	16	1000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

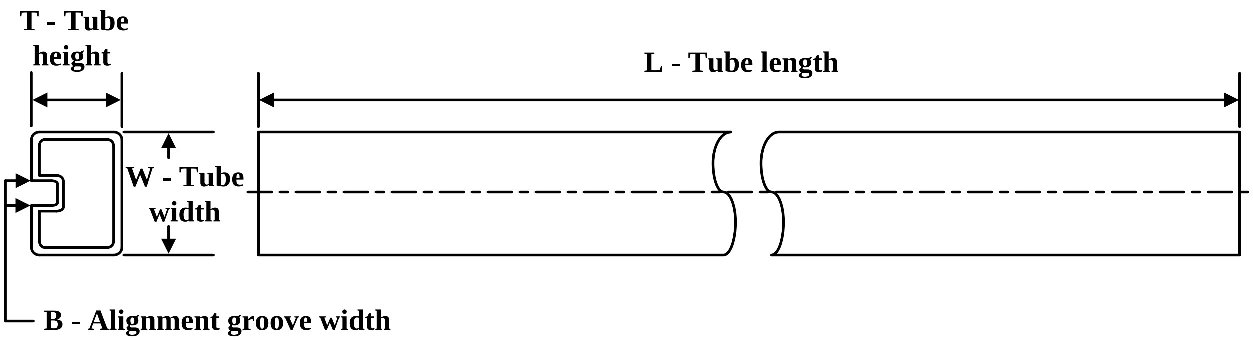
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LOG112AIDR	SOIC	D	14	2500	356.0	356.0	35.0
LOG2112AIDWR	SOIC	DW	16	1000	356.0	356.0	35.0

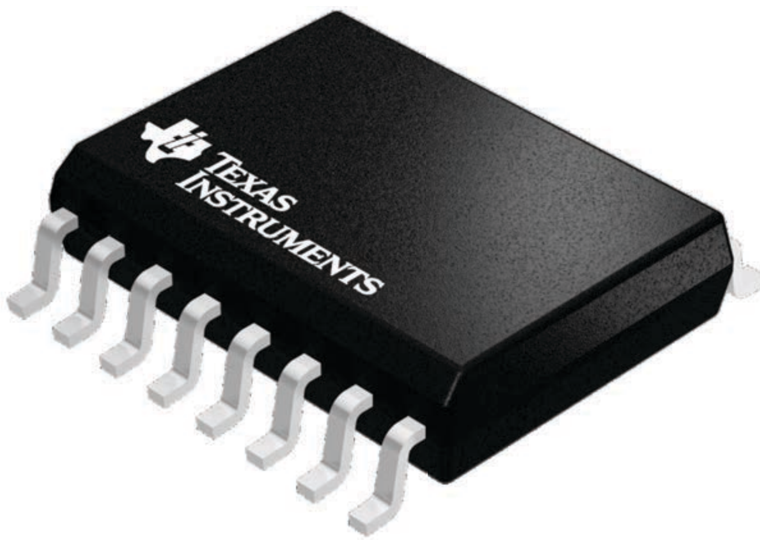
TUBE



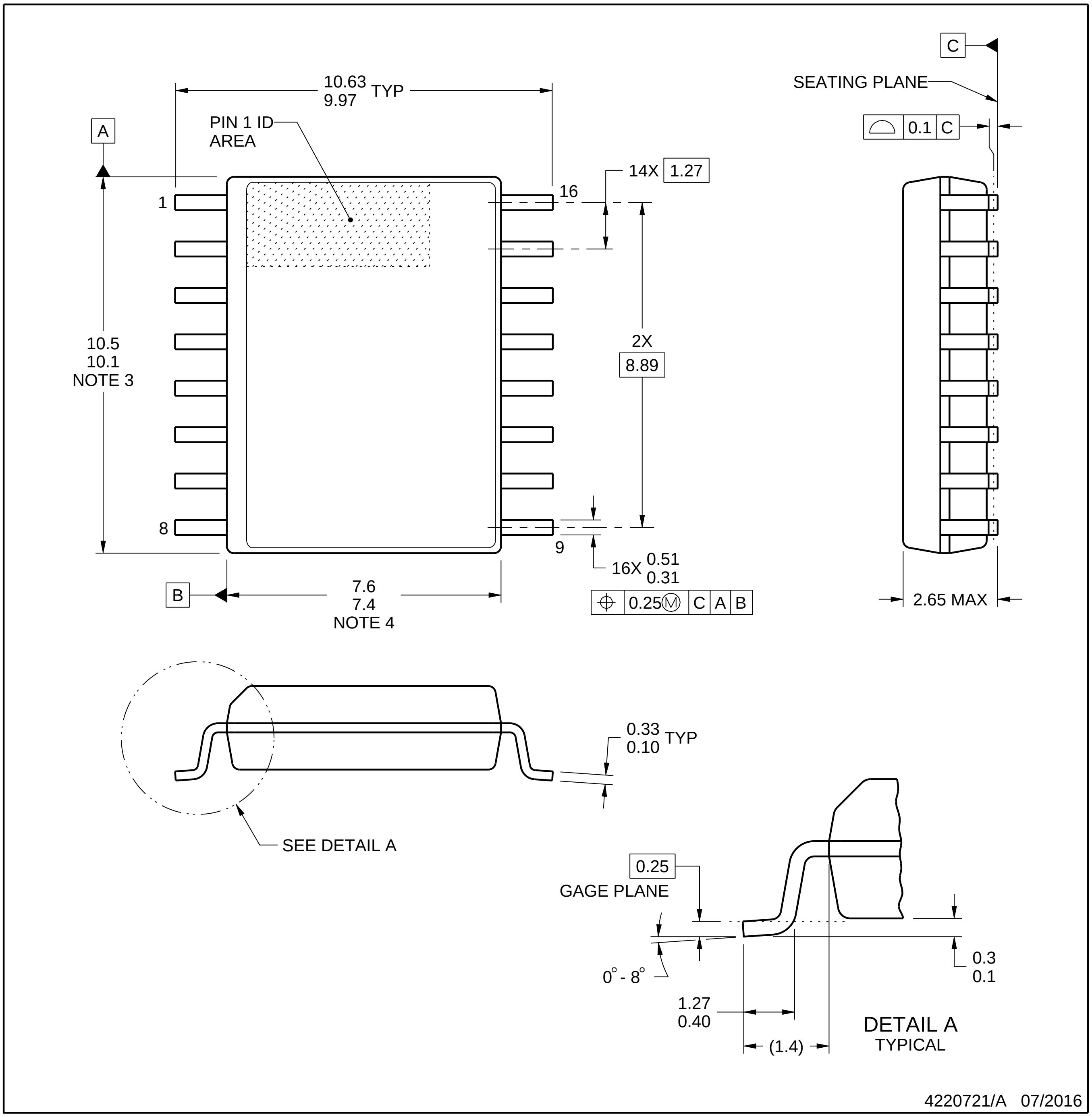
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LOG112AID	D	SOIC	14	50	506.6	8	3940	4.32
LOG2112AIDW	DW	SOIC	16	40	507	12.83	5080	6.6

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



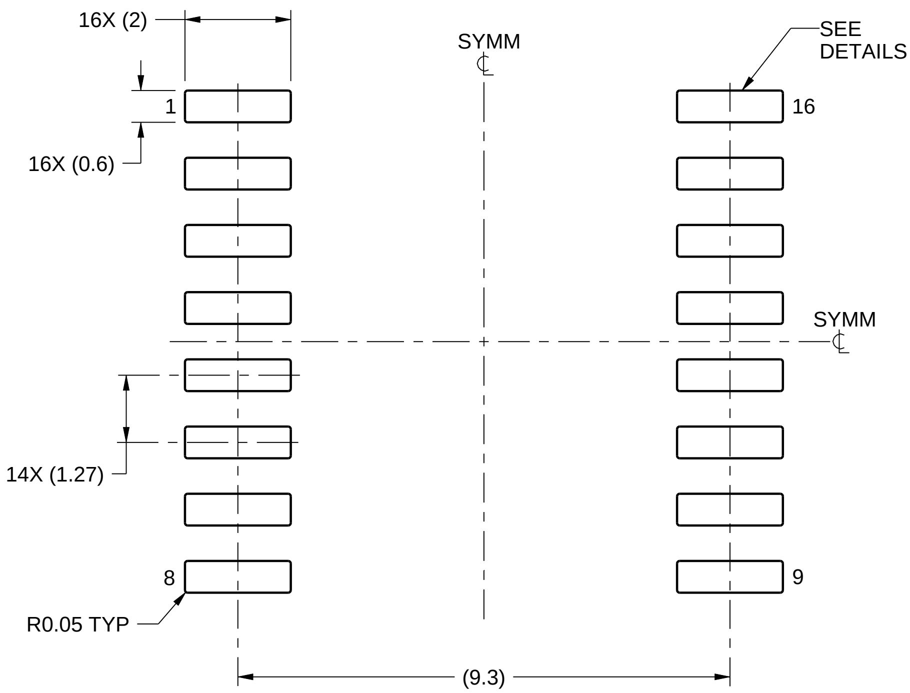
4224780/A



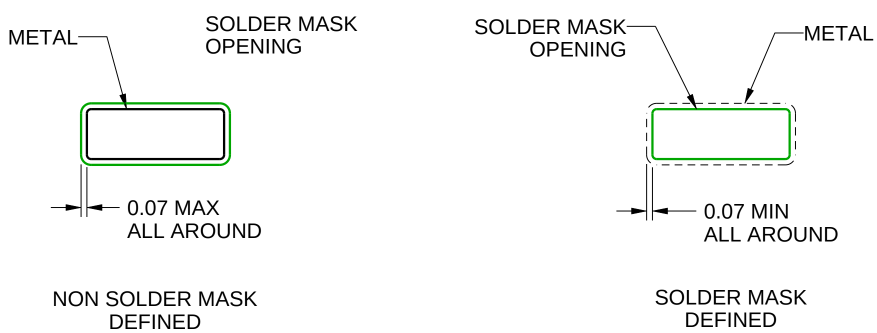
4220721/A 07/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:7X

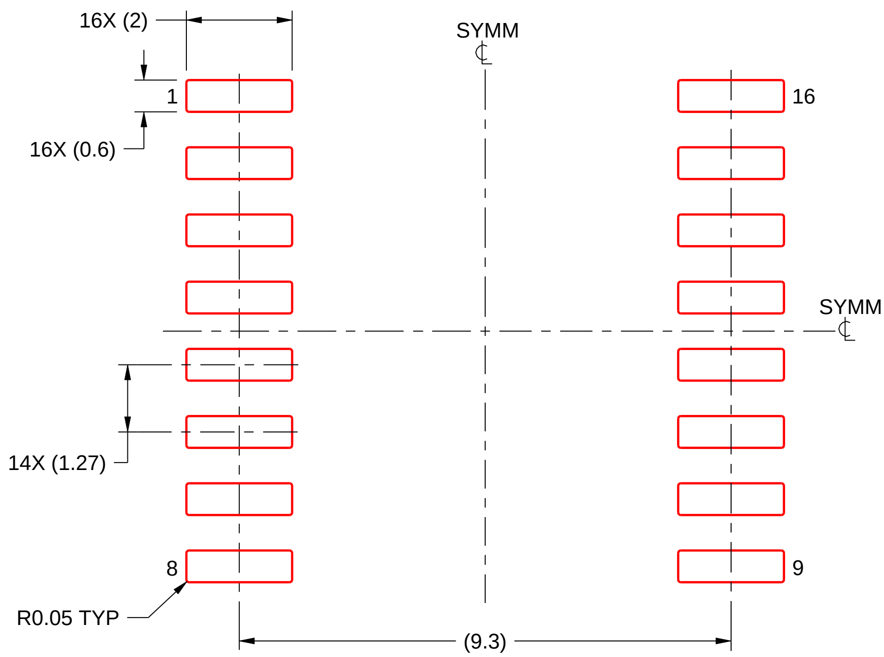


SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



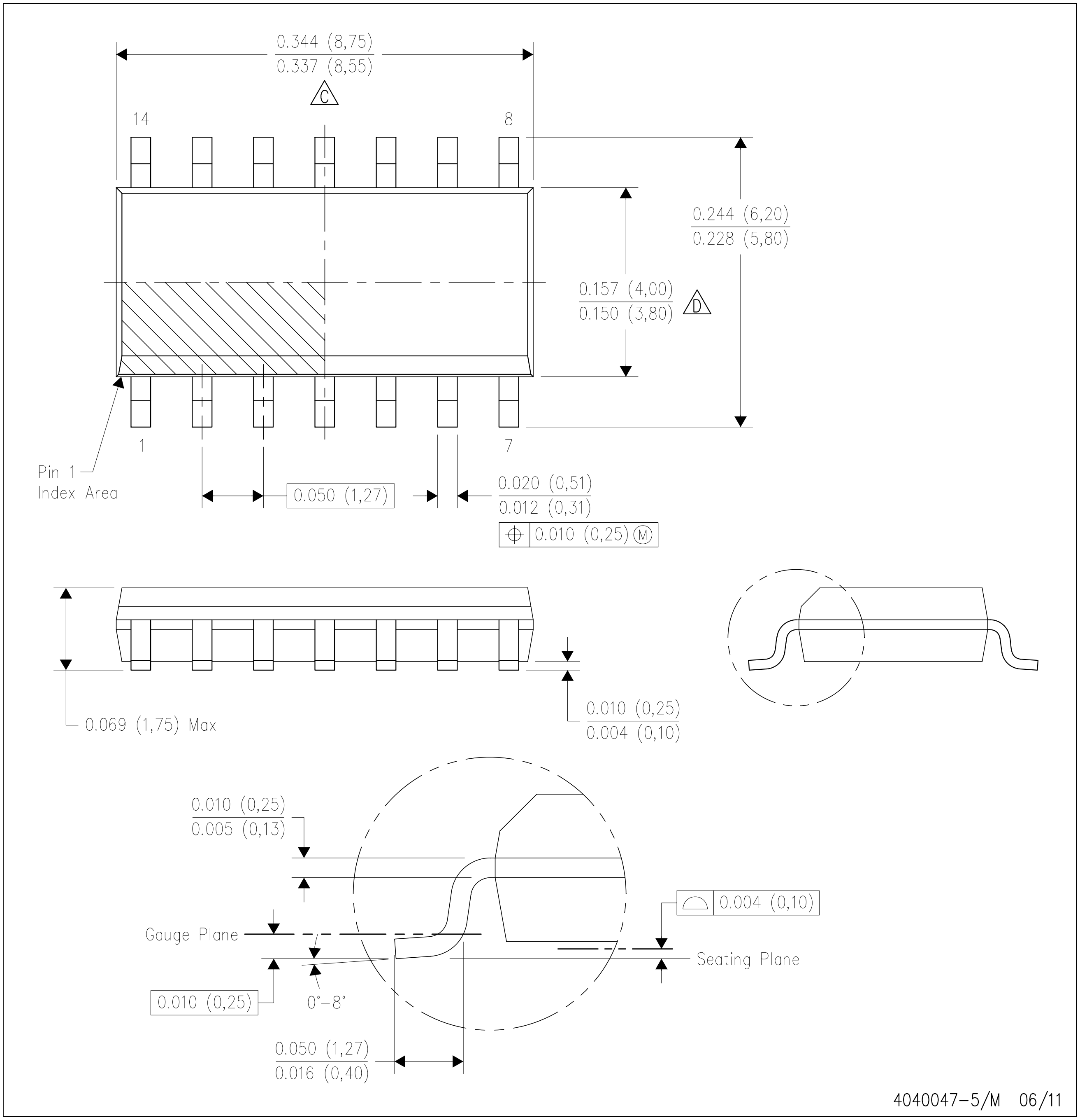
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

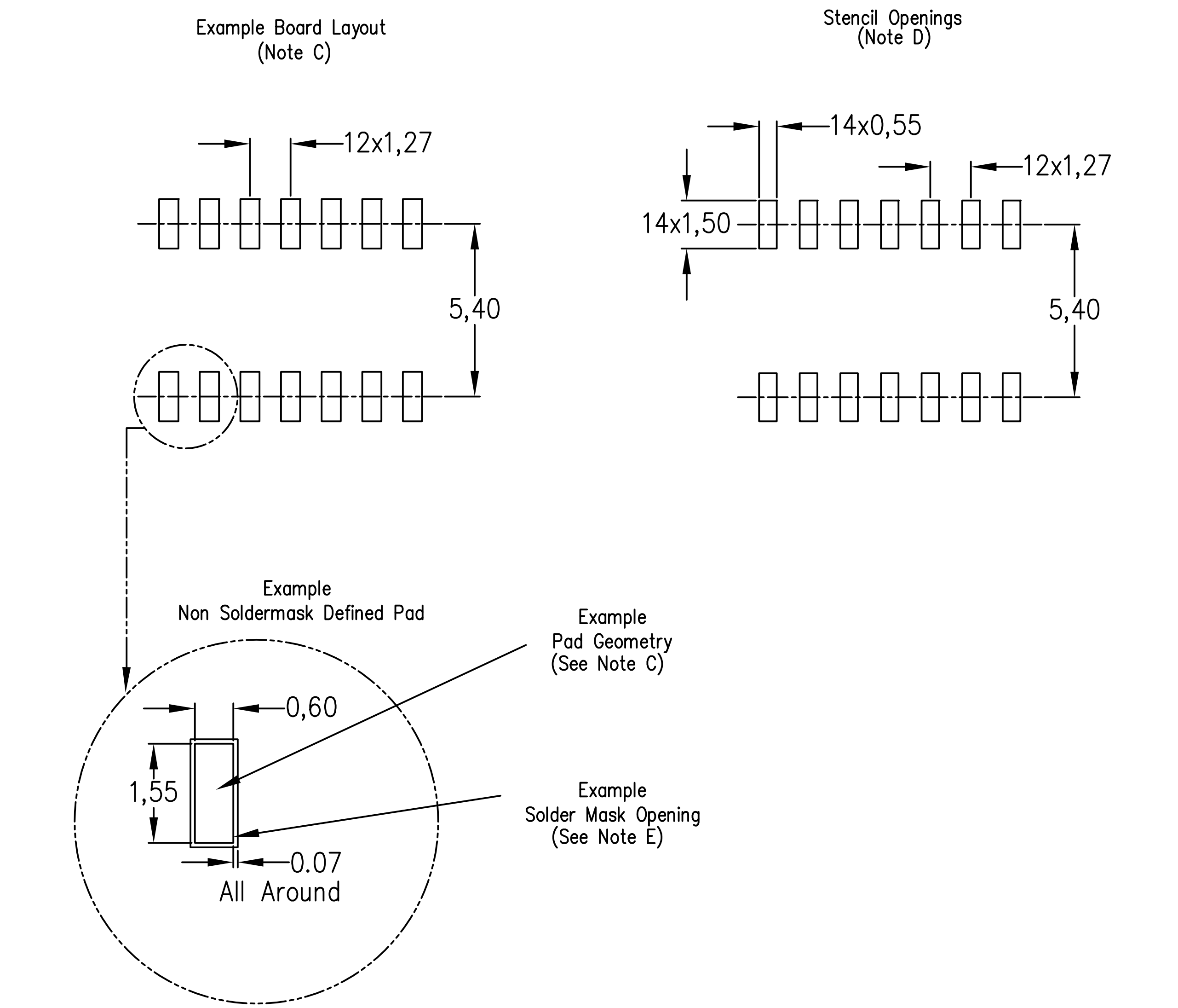
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14) PLASTIC SMALL OUTLINE



4211283-3/E 08/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265