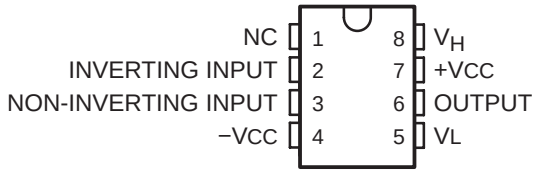
features

- High Linearity Near Limiting
- Fast Recovery from Overdrive: 2.4 ns
- IiMiting Voltage Accuracy: ±15 mV
- −3dB Bandwidth (G = +1): 450 MHz
- Slew Rate: 1000 V/μs
- ±5-V and 5-V Supply Operation
- Unity Gain Version of the OPA689

applications

- Fast Limiting ADC Input Buffers
- CCD Pixel Clock Stripping
- Video Sync Stripping
- HF Mixers
- IF Limiting Amplifiers
- AM Signal Generation
- Non−Linear Analog Signal Processing
- High Speed Comparators

JD PACKAGE
(TOP VIEW)



NC - No internal connection

description

The OPA688 is a wideband, unity gain stable voltage-feedback op amp that offers bipolar output voltage limiting. Two buffered limiting voltages take control of the output when it attempts to drive beyond these limits. This new output limiting architecture holds the limiter offset error to ±15 mV. The op amp operates linearly to within 30 mV of the output limit voltages.

The combination of narrow nonlinear range and low limiting offset allows the limiting voltages to be set within 100 mV of the desired linear output range. A fast 2.4-ns recovery from limiting ensures that overdrive signals will be transparent to the signal channel. Implementing the limiting function at the output, as opposed to the input, gives the specified limiting accuracy for any gain, and allows the OPA688 to be used in all standard op amp applications.

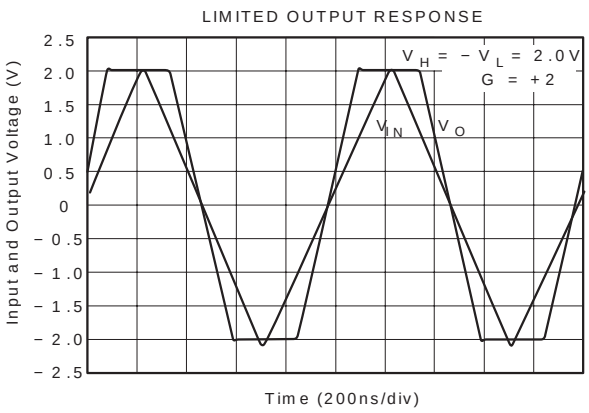
Non-linear analog signal processing will benefit from the OPA688s sharp transition from linear operation to output limiting. The quick recovery time supports high-speed applications.

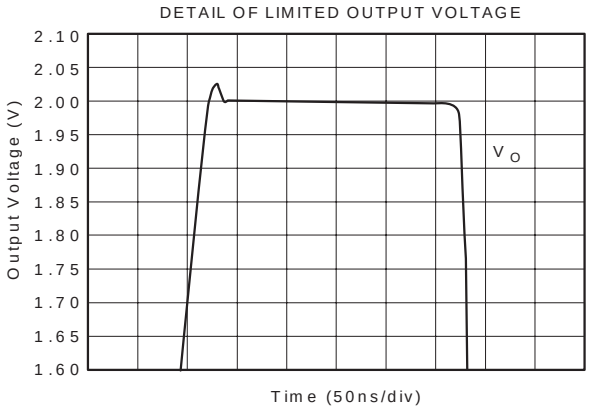
The OPA688M is available in an industry standard pinout CDIP-8 package. For higher gain, or transimpedance applications requiring output limiting with fast recovery, consider the OPA689M.

ORDERING INFORMATION†

T_A	PACKAGE		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−55°C to 125°C	CDIP - JD	Tube	OPA688MJD	OPA688MJD

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.





absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Power supply . . . . . ±6.5 V
Common-mode input voltage, V_{ID} . . . . . $\pm V_{CC}$
Differential input voltage, V_{ID} . . . . . $\pm V_{CC}$
Limiter voltage range . . . . . $\pm(V_S - 0.7\ V)$
Operating free-air temperature range, T_A . . . . . −55°C to 125°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 300°C
Junction temperature, T_J . . . . . 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Operating voltage	Split-Rail Operation		±5	±6	V
	Single-Supply Operation		5	12	
Operating free-air temperature		−55		125	°C

electrical characteristics, V_{CC} = ±5 V, V_{ICM} = 0 V, R_L = 500 Ω, limiter pins open (unless otherwise noted) (see Note 1)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
AC Performance (see Figure 1)						
Small signal bandwidth	V_O < 0.2 Vp-p, G = +1, R_F = 25 Ω			450		MHz
	V_O < 0.2 Vp-p, G = +2			215		
	V_O < 0.2 Vp-p, G = −1			215		
Gain-bandwidth product (G ≥ 5)	V_O < 0.2 Vp-p			250		MHz
Bandwidth for 0.1 dB gain flatness	V_O = 0.2 V			30		MHz
Gain peaking	G = +1, V_O < 0.2 Vp-p, R_F = 25 Ω			11		dB
Large signal bandwidth	V_O = 4 Vp-p, V_H = −V_L = 2.5 V			145		MHz
Slew rate	4 V step, V_H = −V_L = 2.5 V			1000		V/µs
Rise and fall time	0.2 V step			1.9		ns
Settling time to 0.05%	2 V step			8		ns
Spurious free dynamic range	V_O = 2 Vp-p, f = 5 MHz			66		dB
Differential gain	R_L = 500 Ω, NTSC, PAL			0.02		%
Differential phase	R_L = 500 Ω, NTSC, PAL			0.01		°
Input noise, voltage noise density	f ≥ 1 MHz			6.3		nV/√Hz
Input noise, current noise density	f ≥ 1 MHz			2		pA/√Hz
DC Performance						
Open-loop voltage gain (A_{VOL})	V_O = ±0.5 V	T_A = 25°C	46	52		dB
		T_A = Full range	43			
Input offset voltage (V_{IO})		T_A = 25°C		±2	±8	mV
		T_A = Full range			±11	
Input bias current (I_{IB}) (See Note 2)		T_A = 25°C		±6	±12	µA
		T_A = Full range			±20	
Input offset current (I_{IO})		T_A = 25°C		±0.3	±2	µA
		T_A = Full range			±4	
Input						
Common-mode rejection ratio (CMRR)	V_{ICM} = ±0.5 V, Input referred	T_A = 25°C	50	57		dB
		T_A = Full range	47			
Common-mode input voltage range (V_{ICR}) (See Note 3)		T_A = 25°C	±3.2	±3.3		V
		T_A = Full range	±3.1			
Input impedance, differential mode				0.4 1		MΩ pF
Input impedance, common mode				1 1		MΩ pF

electrical characteristics, V_{CC} = ±5 V, V_{ICM} = 0 V, R_L = 500 Ω, limiter pins open (unless otherwise noted) (see Note 1) (continued)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Output						
Output voltage range (V_{OH}, V_{OL})	V_H = 4.3 V, V_L = −4.3 V, $R_L \geq$ 500 Ω	T_A = 25°C	±3.9	±4.1		V
		T_A = Full range	±3.7			
Current output, sourcing (I_{OH})	V_H = 4.3 V, V_L = −4.3 V, R_L = 20 Ω	T_A = 25°C	90	105		mA
		T_A = Full range	80			
Current output, sinking (I_{OL})	V_H = 4.3 V, V_L = −4.3 V, R_L = 20 Ω	T_A = 25°C	−70	−85		mA
		T_A = Full range	−60			
Closed-loop output impedance	G = +1, R_F = 25 Ω, f < 100 kHz			0.2		Ω
Power Supply						
Operating voltage (V_{CC})				±5	±6	V
Quiescent current (I_{CC})		T_A = 25°C	14	15.8	17	mA
		T_A = Full range	11		20	
Power supply rejection ratio (PSRR)	Input referred, V_S = ±4.5 V to ±5.5 V	T_A = 25°C	58	70		dB
		T_A = Full range	55			dB
Output Voltage Limiters (pins 5 and 8)						
Default output limited voltage	Limiter pins open	T_A = 25°C	±3	±3.3		V
		T_A = Full range	±2.8			
Limiter output offset voltage	(V_O − V_H) or (V_O − V_L)	T_A = Full range		±15	±50	mV
Limiter input bias current magnitude (See Note 4)	V_O = 0 V	T_A = 25°C	35	54	65	µA
		T_A = Full range	31		70	
Limiter input impedance				2 1		MΩ pF
Limiter feedthrough (See Note 5)	f = 5 MHz			−60		dB
Maximum limiter voltage					±4.3	V
Minimum limiter voltage separation			400			mV
Op amp bias current shift (See Note 2)				3		µA
Limiter small signal bandwidth	V_I = ±2 V, V_O < 0.02 Vp-p			450		MHz
Limter slew rate (See Note 6)				100		V/µs
Limiter step response, overshoot	V_I = ±2 V			250		mV
Limiter step response, recovery time	V_I = ±2 V			2.4		ns
Linearity guardband (See Note 7)	V_O = 2 Vp-p, f = 5 MHz			30		mV

NOTES:
1. All typical limits are at T_A = 25°C unless otherwise specified.
2. Current is considered positive out of node.
3. CMIR tested as < 3dB degradation from minimum CMRR at specified limits.
4. I_{VH} (V_H bias current) is positive, and I_{VL} (V_L bias current) is negative, under these conditions. See Note 3, Figure 30 and Figure 37.
5. Limiter feedthrough is the ratio of the output magnitude to the sinewave added to V_H (or V_L) when V_{IN} = 0.
6. V_H slew rate conditions are: V_{IN} = +2 V, G = +2, V_L = −2 V, V_H = step between 2 V and 0 V. V_L slew rate conditions are similar.
7. Linearity Guardband is defined for an output sinusoid (f = 5 MHz, V_O = 0 V_{DC} ±1 V_{P-P}) centered between the limiter levels (V_H and V_L). It is the difference between the limiter level and the peak output voltage where SFDR decreases by 3dB (see Figure 38).

electrical characteristics, V_{CC} = 5 V, V_{ICM} = 2.5 V, R_L = 500 Ω, limiter pins open (unless otherwise noted) (see Note 1)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
AC Performance (see Figure 2)						
Small signal bandwidth	V_O < 0.2 Vp-p, G = +1, R_F = 25 Ω			375		MHz
	V_O < 0.2 Vp-p, G = +2			200		
	V_O < 0.2 Vp-p, G = −1			190		
Gain bandwidth product (G ≥ +5)	V_O < 0.2 Vp-p			230		MHz
Gain peaking	V_O < 0.2 Vp-p, G = +1, R_F = 25 Ω			10		dB
Bandwidth for 0.1 dB gain flatness	V_O < 0.2 Vp-p			30		MHz
Large signal bandwidth	V_O < 2 Vp-p			200		MHz
Slew rate	2 V step			820		V/µs
Rise and fall time	0.2 V step			2.3		ns
Settling time to 0.05%	1 V step			12		ns
Spurious free dynamic range	V_O = 2 Vp-p, f = 5 MHz			64		dB
Input noise, voltage noise density	f > 1 MHz			6.3		nV/√Hz
Input noise, current noise density	f > 1 MHz			2		pA/√Hz
DC Performance						
Open-loop voltage gain (AVOL)	V_O = ±0.4 V	T_A = 25°C	46	52		dB
		T_A = Full range	43			
Input offset voltage (V_{IO})		T_A = 25°C		±2	±8	mV
		T_A = Full range			±11	
Input bias current (I_{IB})		T_A = 25°C		±6	±12	µA
		T_A = Full range			±20	
Input offset current (I_{IO})		T_A = 25°C		±0.3	±2	µA
		T_A = Full range			±4	
Input						
Common-mode rejection ratio (CMRR)	V_{ICM} = ±0.5 V, Input referred	T_A = 25°C	48	55		dB
		T_A = Full range	45			
Common-mode input voltage range (V_{ICR}) (See Note 3)		T_A = 25°C	V_{ICM} ±0.7 V	V_{ICM} ±0.8 V		V
		T_A = Full range	V_{ICM} ±0.6 V			
Input impedance, differential mode				0.4 1		MΩ pF
Input impedance, common mode				1 1		MΩ pF
Output						
Output voltage range (V_{OH}, V_{OL})	V_H = V_{ICM} + 1.8 V, V_L = V_{ICM} − 1.8 V, R_L ≥ 500 Ω	T_A = 25°C	V_{ICM}± 1.4 V	V_{ICM}± 1.6 V		V
		T_A = Full range	V_{ICM}± 1.3 V			
Current output, sourcing (I_{OH})	V_{CC} = ±2.5 V, R_L = 20 Ω	T_A = 25°C	60	70		mA
		T_A = Full range	50			
Current output, sinking (I_{OL})	V_{CC} = ±2.5 V, R_L = 20 Ω	T_A = 25°C	−50	−60		mA
		T_A = Full range	−40			
Closed-loop output impedance	G = +1, R_F = 25 Ω, f < 100 kHz			0.2		Ω

electrical characteristics, V_{CC} = 5 V, V_{ICM} = 2.5 V, R_L = 500 Ω, limiter pins open (unless otherwise noted) (see Note 1) (continued)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Power Supply						
Operating voltage (V_{CC})				5	12	V
Quiescent current (I_{CC})		T_A = 25°C	11	13	15	mA
		T_A = Full range	9		16.5	
Power supply rejection ratio (PSRR)	Input referred, V_{CC} = ±2 V to ±3 V	T_A = Full range	55	70		dB
Output Voltage Limiters (pins 5 and 8)						
Default output limited voltage	Limiter pins open	T_A = 25°C	V_{ICM} ±0.6 V	V_{ICM} ±0.9 V		V
		T_A = Full range	V_{ICM} ±0.4 V			V
Limiter output offset voltage	(V_O − V_H) or (V_O − V_L)	T_A = Full range		±15	±50	mV
Limiter input bias current magnitude (See Note 4)	V_O = 2.5 V	T_A = 25°C	0	35	65	µA
		T_A = Full range	0		85	
Limiter input bias current drift				30		nA/°C
Limiter input impedance				2 1		MΩ pF
Limiter feedthrough (See Note 5)	f = 5 MHz			−60		dB
Maximum limiter voltage					V_{ICM} ± 1.8	V
Minimum limiter voltage separation			400			mV
Output bias current shift (See Note 2)				5		µA
Limiter small signal bandwidth	V_I = V_{ICM} ± 1.2 V, V_O < 0.02 Vp-p			300		MHz
Limiter slew rate (See Note 6)				20		V/µs
Limiter step response, overshoot	V_I = V_{ICM} ± 1.2 V			55		mV
Limiter step response, recovery time	V_I = V_{ICM} ± 1.2 V			15		ns
Linearity guardband (See Note 7)	V_O = 2 Vp-p, f = 5 MHz		30			mV

NOTES:
1. All typical limits are at T_A = 25°C unless otherwise specified.
2. Current is considered positive out of node.
3. CMIR tested as < 3dB degradation from minimum CMRR at specified limits.
4. I_{VH} (V_H bias current) is positive, and I_{VL} (V_L bias current) is negative, under these conditions. See Note 3, Figure 31 and Figure 37.
5. Limiter feedthrough is the ratio of the output magnitude to the sinewave added to V_H (or V_L) when V_{IN} = 0.
6. V_H slew rate conditions are: V_{IN} = V_{ICM} + 0.4 V, G = +2, V_L = V_{ICM} − 1.2 V, V_H = stepped between V_{ICM} + 1.2 V and V_{ICM}. V_L slew rate conditions are similar.
7. Linearity Guardband is defined for an output sinusoid (f = 5 MHz, V_O = 0 V_{DC} ±1 V_{P-P}) centered between the limiter levels (V_H and V_L). It is the difference between the limiter level and the peak output voltage where SFDR decreases by 3dB (see Figure 38).

TYPICAL CHARACTERISTICS

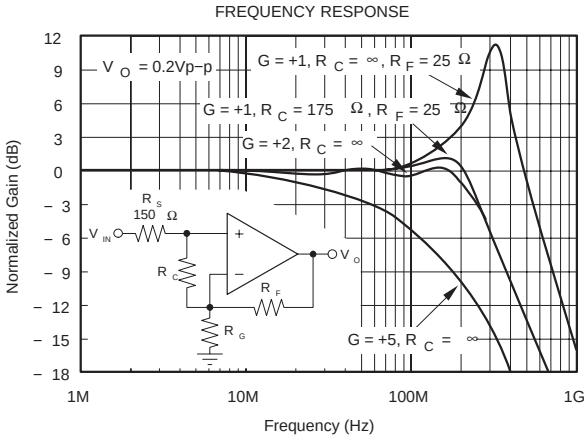


Figure 1

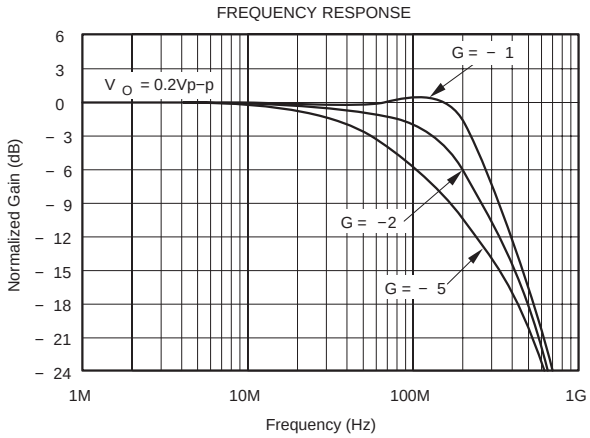


Figure 2

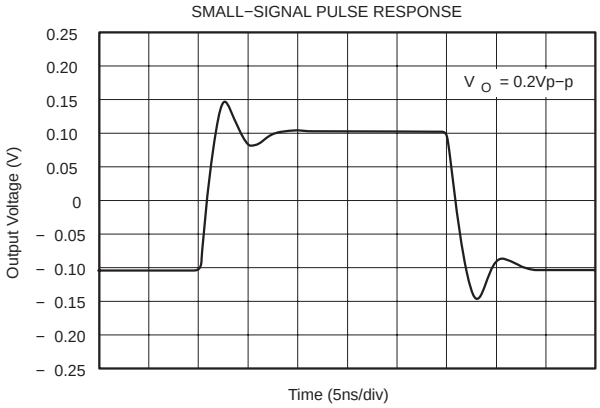


Figure 3

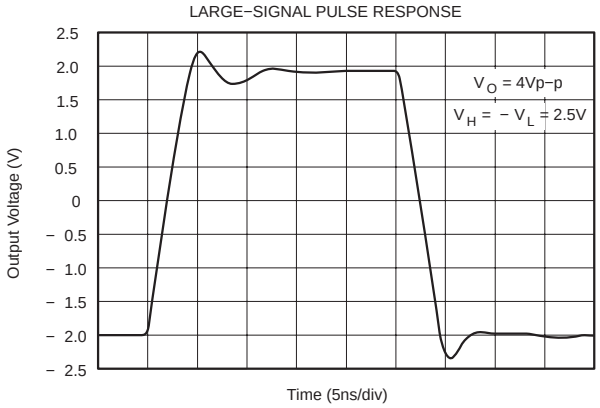


Figure 4

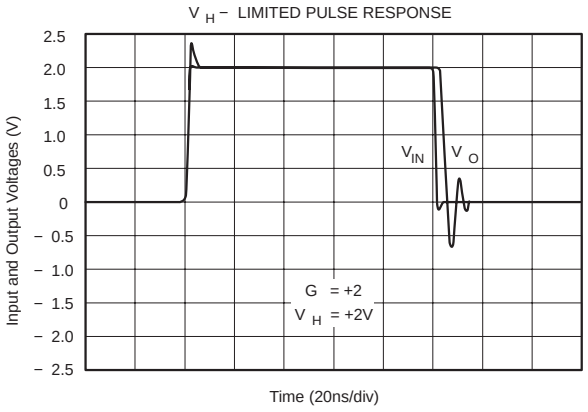


Figure 5

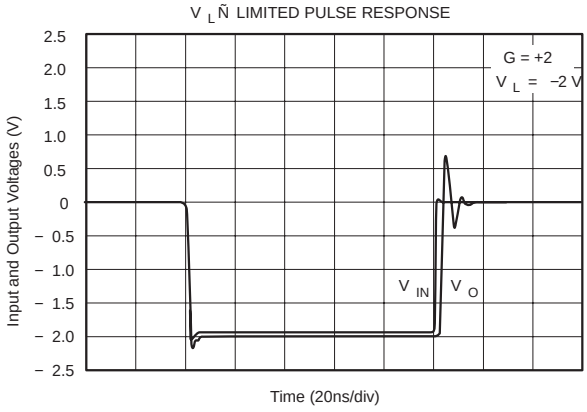


Figure 6

TYPICAL CHARACTERISTICS

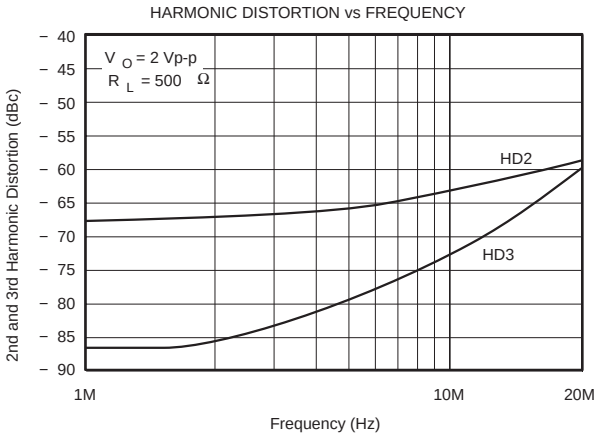


Figure 7

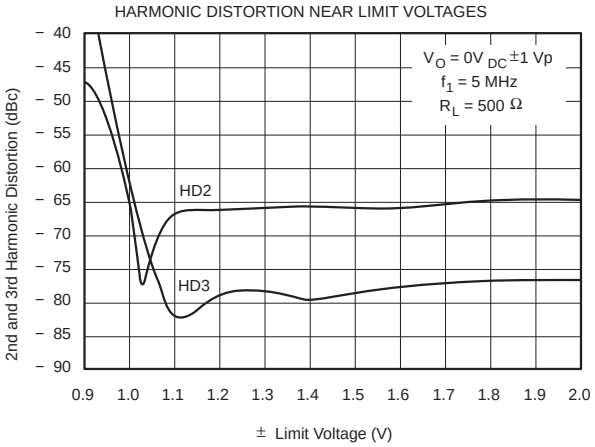


Figure 8

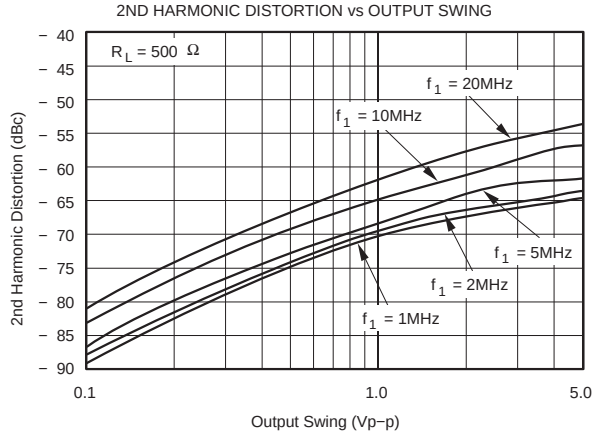


Figure 9

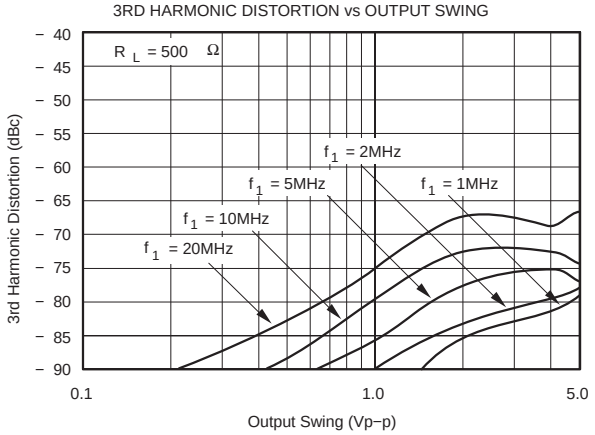


Figure 10

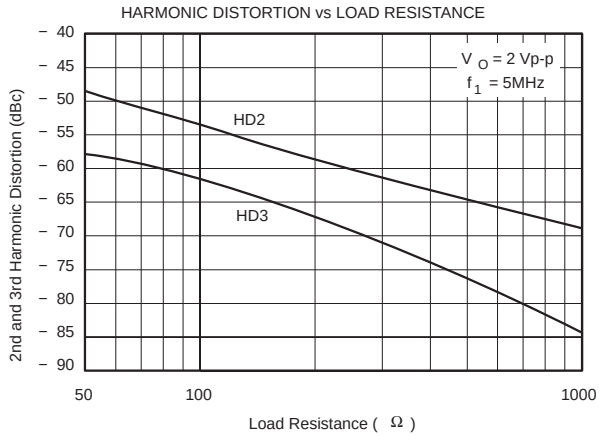


Figure 11

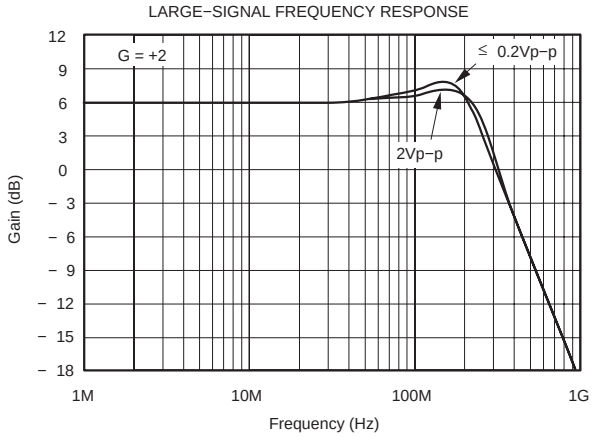


Figure 12

TYPICAL CHARACTERISTICS

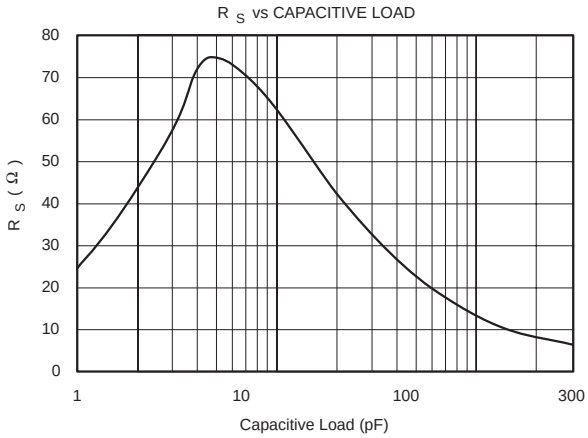


Figure 13

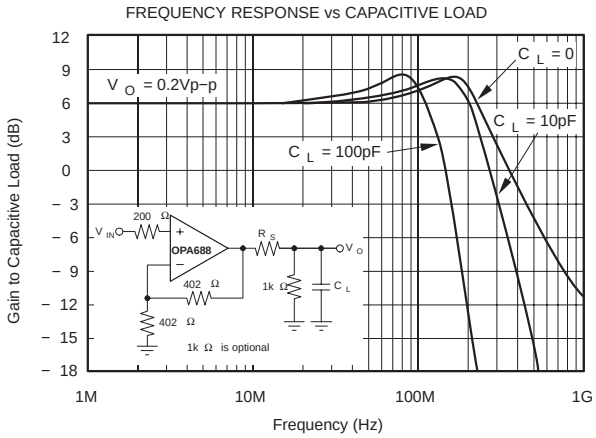


Figure 14

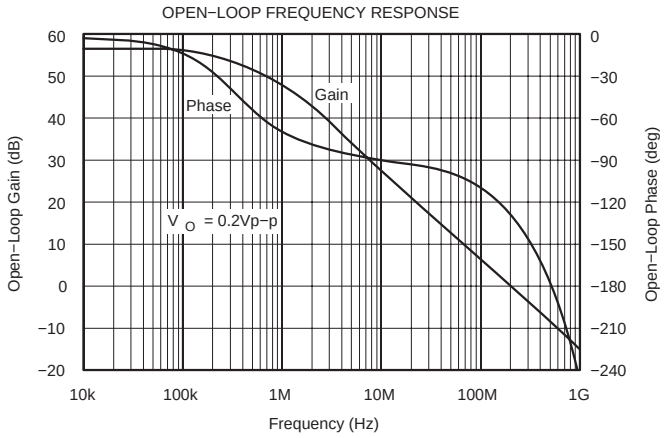


Figure 15

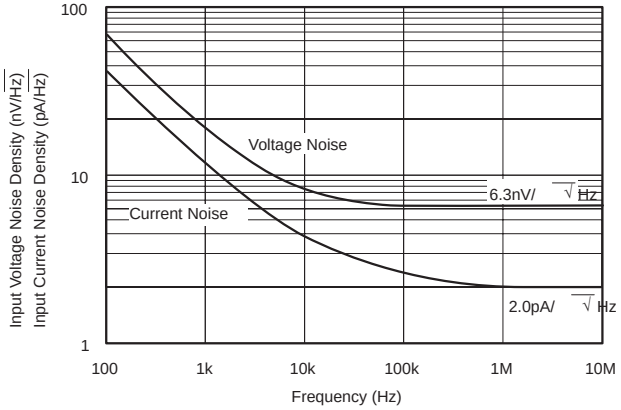


Figure 16

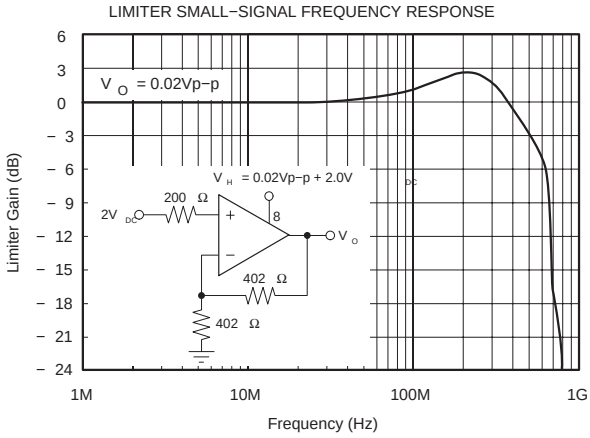


Figure 17

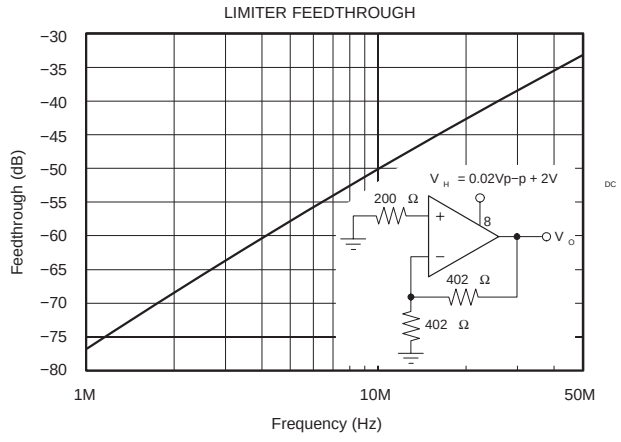


Figure 18

TYPICAL CHARACTERISTICS

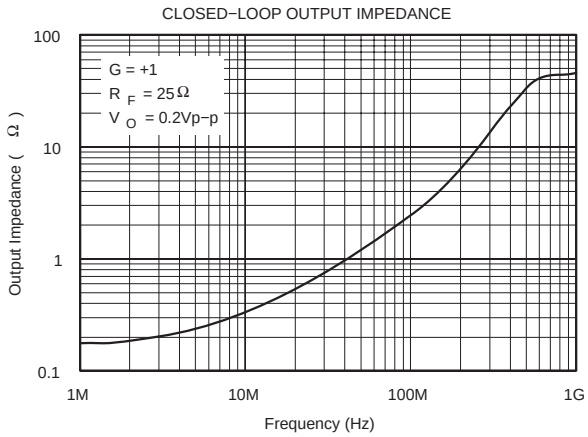


Figure 19

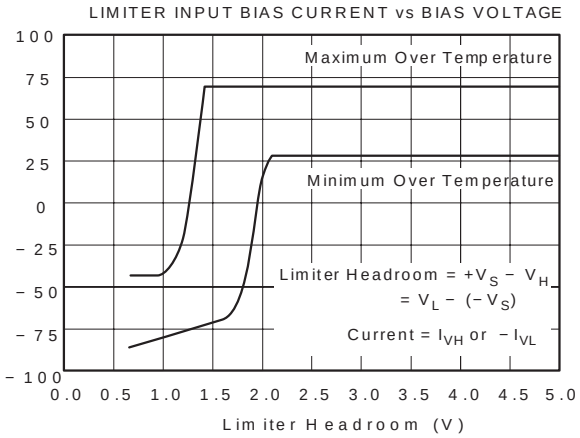


Figure 20

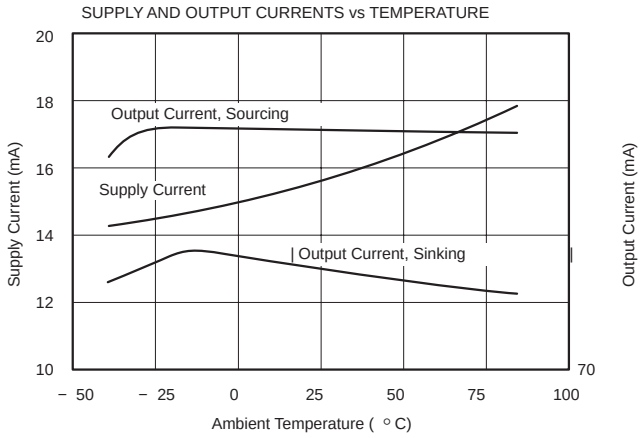


Figure 21

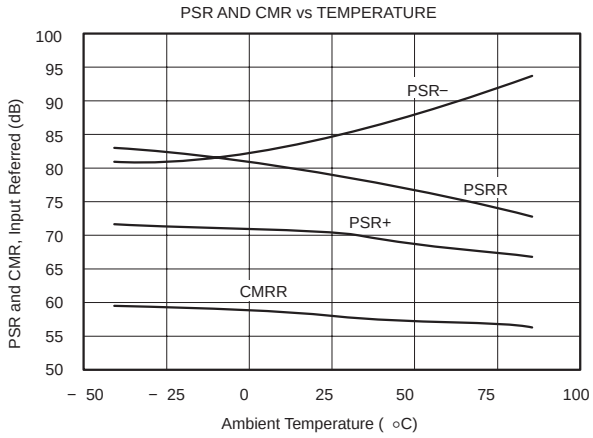


Figure 22

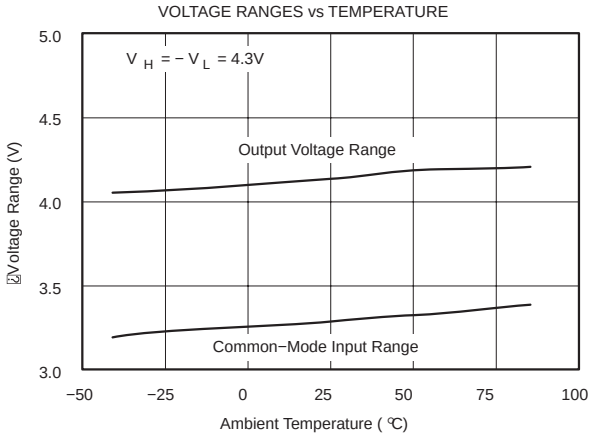


Figure 23

TYPICAL CHARACTERISTICS

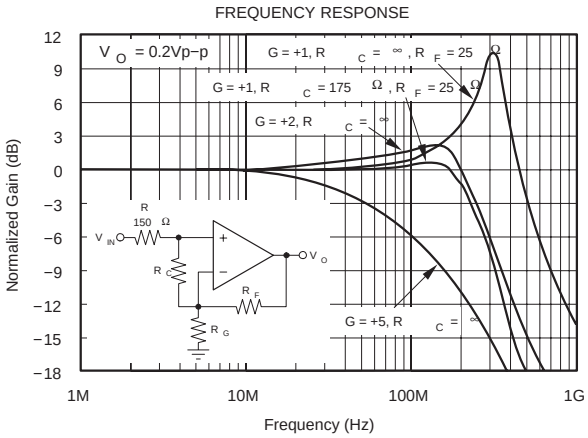


Figure 24

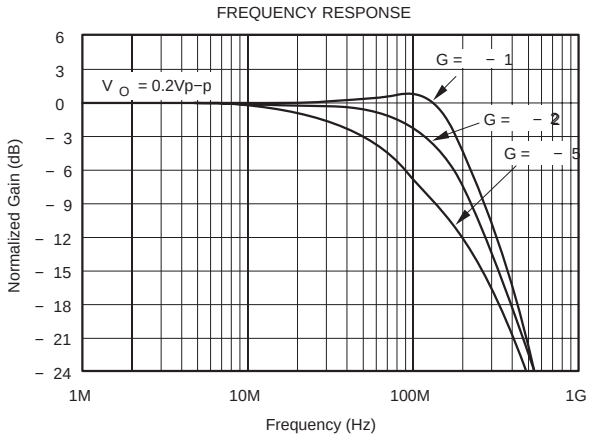


Figure 25

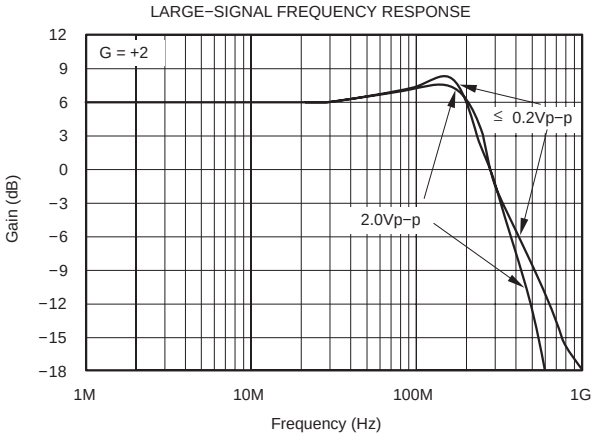


Figure 26

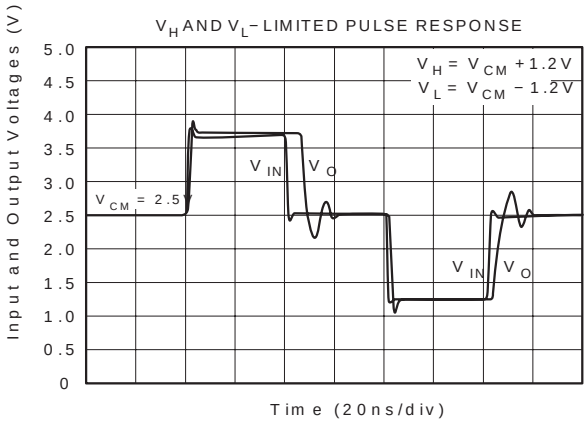


Figure 27

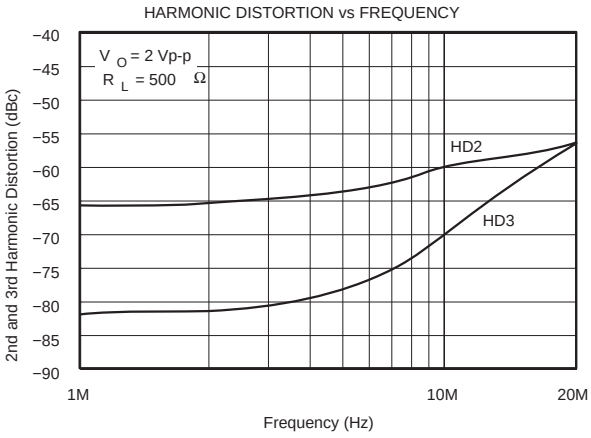


Figure 28

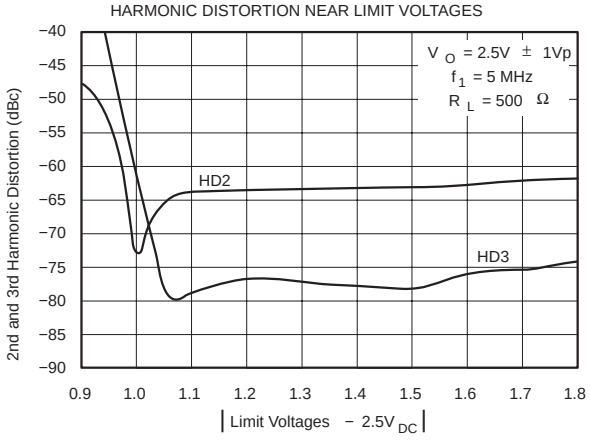


Figure 29

APPLICATION INFORMATION

dual-supply, non-inverting amplifier

Figure 30 shows a non-inverting gain amplifier for dual-supply operation. This circuit was used for AC characterization of the OPA688, with a 50-Ω source, which it matches, and a 500-Ω load. The power-supply bypass capacitors are shown explicitly in Figures 30 and 31, but will be assumed in the other figures. The limiter voltages (V_H and V_L) and their bias currents (I_{VH} and I_{VL}) have the polarities shown.

single-supply, non-inverting amplifier

Figure 31 shows an AC-coupled, non-inverting gain amplifier for single +5V supply operation. This circuit was used for AC characterization of the OPA688, with a 50W source, which it matches, and a 500-Ω load. The power-supply bypass capacitors are shown explicitly in Figures 30 and 31, but will be assumed in the other figures. The limiter voltages (V_H and V_L) and their bias currents (I_{VH} and I_{VL}) have the polarities shown. Notice that the single-supply circuit can use three resistors to set V_H and V_L, where the dual-supply circuit usually uses four to reference the limit voltages to ground.

limited output, ADC input driver

Figure 32 shows a simple ADC (Analog-to-Digital Converter) driver that operates on a single supply, and gives excellent distortion performance. The limit voltages track the input range of the converter, completely protecting against input overdrive.

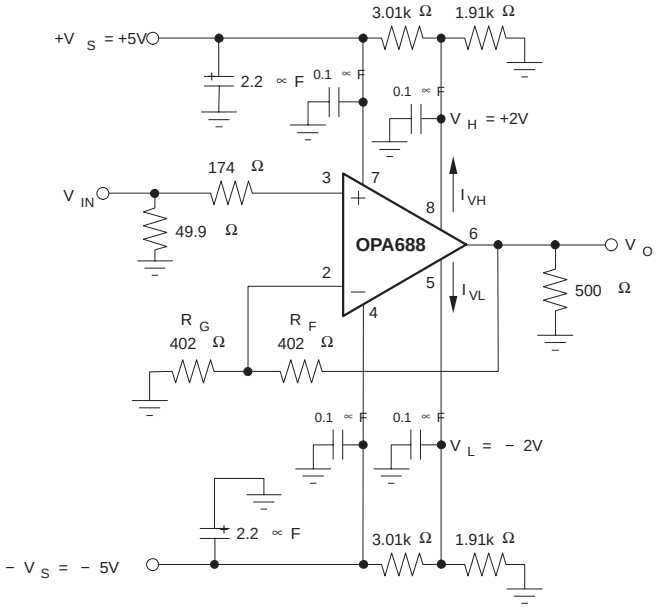


Figure 30. DC-Coupled, Dual Supply Amplifier

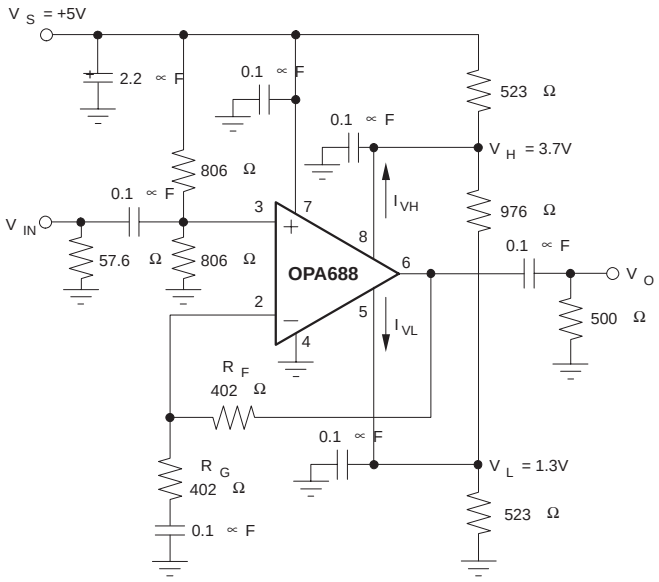


Figure 31. AC-Coupled, Single Supply Amplifier

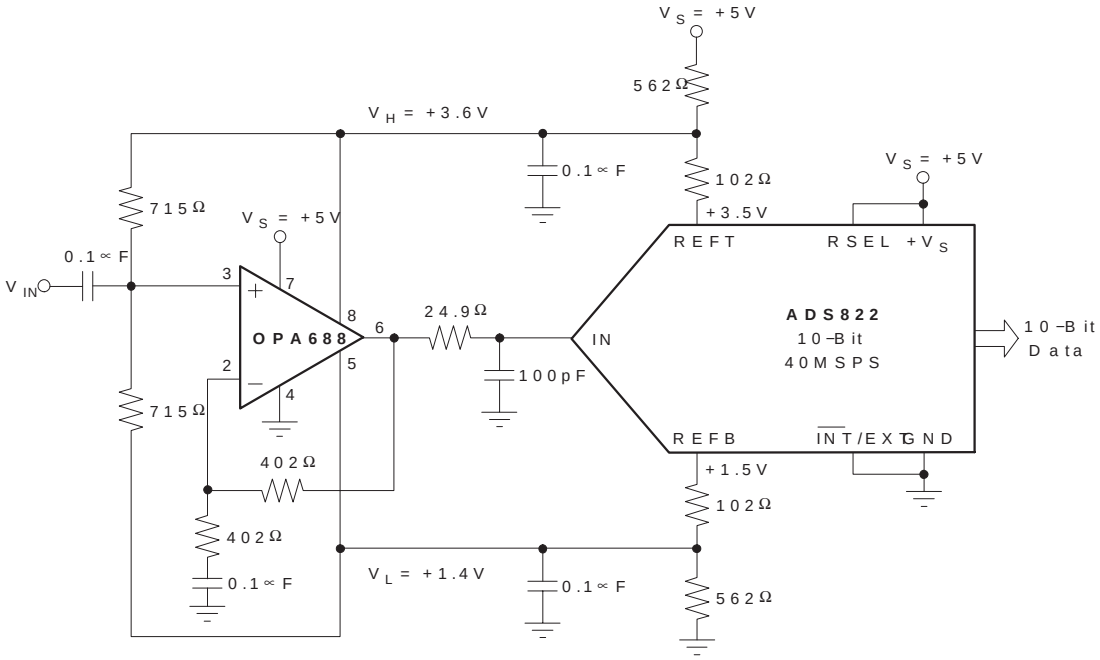


Figure 32. Single Supply, Limiting ADC Input Driver

precision half wave rectifier

Figure 33 shows a half wave rectifier with outstanding precision and speed. V_H (pin 8) will default to a voltage between 3.1 and 3.8 V if left open, while the negative limit is set to ground.

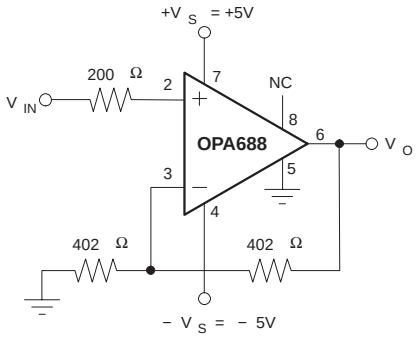


Figure 33. Precision Half Wave Rectifier

very high speed Schmitt trigger

Figure 34 shows a very high-speed Schmitt trigger. The output levels are precisely defined, and the switching time is exceptional. The output voltage swings between ±2V.

unity-gain buffer

Figure 35 shows a unity-gain voltage buffer using the OPA688. The feedback resistor (R_F) isolates the output from any board inductance between pins 2 and 6. We recommend that

$R_F \times$ 24.9W for unity-gain buffer applications. R_C is an optional compensation resistor that reduces the peaking typically seen at G = +1. Choosing $R_C = R_S + R_F$ gives a unity gain buffer with approximately the G = +2 frequency response.

DC restorer

Figure 36 shows a DC restorer using the OPA688 and OPA660. The OPA660's OTA amplifier is used as a Current Conveyor (CCII) in this circuit, with a current gain of 1.0.

When V_O tries to go below ground, CCII charges C_1 through D_1, which restores the output back to ground. D_1 adds a propagation delay to the restoration process, which then has an exponential decay with time constant R_1C_1/G (G = +2 = the OPA688 gain). When the signal is above ground, it decays to ground with a time constant of R_2C_1. The OPA688 output recovers very quickly from overdrive.

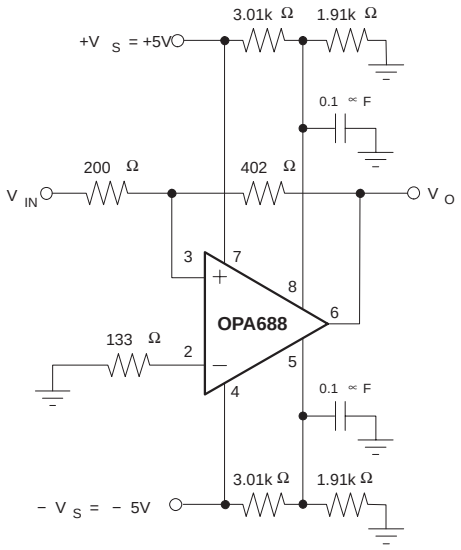


Figure 34. Very High Speed Schmitt Trigger

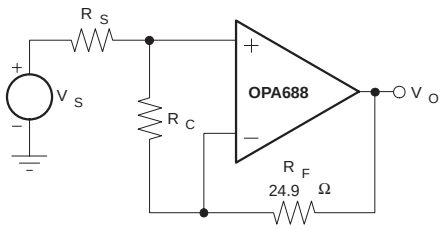


Figure 35. Unity-Gain Buffer

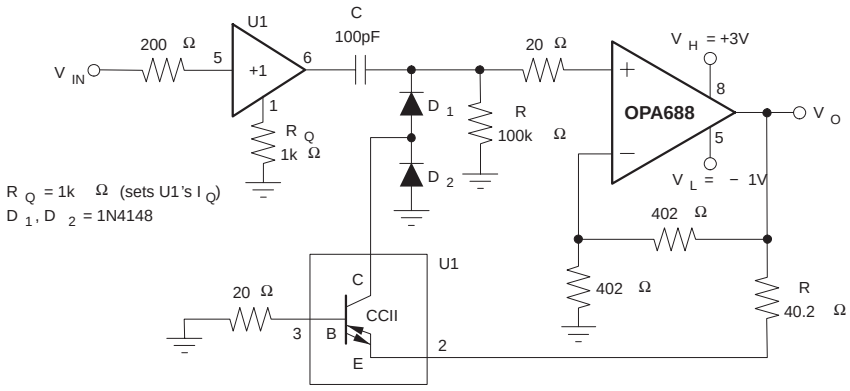


Figure 36. DC Restorer

design-in tools

applications support

The Texas Instrments web site (http://www.ti.com) has the latest data sheets and other design aids.

theory of operation

The OPA688 is a voltage-feedback op amp that is unity-gain stable. The output voltage is limited to a range set by the voltage on the limiter pins (5 and 8). When the input tries to overdrive the output, the limiters take control of the output buffer. This avoids saturating any part of the signal path, giving quick overdrive recovery and excellent limiter accuracy at any signal gain.

The limiters have a very sharp transition from the linear region of operation to output limiting. This allows the limiter voltages to be set very near (< 100mV) the desired signal range. The distortion performance is also very good near the limiter voltages.

circuit layout

Achieving optimum performance with the high-frequency OPA688 requires careful attention to layout design and component selection. Recommended PCB layout techniques and component selection criteria are:

a) **Minimize parasitic capacitance to any AC ground** for all of the signal I/O pins. Open a window in the ground and power planes around the signal I/O pins, and leave the ground and power planes unbroken elsewhere.

b) **Provide a high quality power supply.** Use linear regulators, ground plane and power planes to provide power. Place high-frequency 0.1 μF decoupling capacitors < 0.2” away from each power-supply pin. Use wide, short traces to connect to these capacitors to the ground and power planes. Also use larger (2.2 μF to 6.8 μF) high-frequency decoupling capacitors to bypass lower frequencies. They may be somewhat further from the device, and be shared among several adjacent devices.

c) **Place external components close** to the OPA688. This minimizes inductance, ground loops, transmission line effects and propagation delay problems. Be extra careful with the feedback (R_F), input and output resistors.

d) **Use high-frequency components** to minimize parasitic elements. Resistors should be a very low reactance type. Surface-mount resistors work best and allow a tighter layout. Metal film or carbon composition axially-leaded resistors can also provide good performance when their leads are as short as possible. Never use wirewound resistors for high-frequency applications. Remember that most potentiometers have large parasitic capacitances and inductances.

Multilayer ceramic chip capacitors work best and take up little space. Monolithic ceramic capacitors also work very well. Use RF type capacitors with low ESR and ESL. The large power pin bypass capacitors (2.2 μF to 6.8 μF) should be tantalum for better high-frequency and pulse performance.

e) **Choose low resistor values** to minimize the time constant set by the resistor and its parasitic parallel capacitance. Good metal film or surface mount resistors have approximately 0.2 pF parasitic parallel capacitance. For resistors > 1.5 kΩ, this adds a pole and/or zero below 500 MHz.

Make sure that the output loading is not too heavy. The recommended 402-Ω feedback resistor is a good starting point in your design.

f) **Use short direct traces to other wideband devices** on the board. Short traces act as a lumped capacitive load. Wide traces (50 to 100 mils) should be used. Estimate the total capacitive load at the output, and use the series isolation resistor recommended in the typical performance curve ”R_S vs Capacitive Load”. Parasitic loads < 2 pF may not need the isolation resistor.

g) **When long traces are necessary,** use transmission line design techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50-Ω transmission line is not required on board—a higher characteristic impedance will help reduce output loading. Use a matching series resistor at the output of the op amp to drive a transmission line, and a matched load resistor at the other end to make the line appear as a resistor. If the 6 dB of attenuation that the matched load produces is not acceptable, and the line is not too long, use the series resistor at the source only. This will isolate the source from the reactive load presented by the line, but the frequency response will be degraded.

Multiple destination devices are best handled as separate transmission lines, each with its own series source and shunt load terminations. Any parasitic impedances acting on the terminating resistors will alter the transmission line match, and can cause unwanted signal reflections and reactive loading.

h) **Do not use sockets** for high-speed parts like the OPA688. The additional lead length and pin-to-pin capacitance introduced by the socket creates an extremely troublesome parasitic network. Best results are obtained by soldering the part onto the board.

power supplies

The OPA688 is nominally specified for operation using either ±5-V supplies or a single +5-V supply. The maximum specified total supply voltage of 12 V allows reasonable tolerances on the supplies. Higher supply voltages can break down internal junctions, possibly leading to catastrophic failure. Single-supply operation is possible as long as common mode voltage constraints are observed. The common mode input and output voltage specifications can be interpreted as a required headroom to the supply voltage. Observing this input and output headroom requirement will allow design of non-standard or single-supply operation circuits. Figure 31 shows one approach to single-supply operation.

ESD protection

ESD damage has been known to damage MOSFET devices, but any semiconductor device is vulnerable to ESD damage. This is particularly true for very high-speed, fine geometry processes.

ESD damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers, this may cause a noticeable degradation of offset voltage and drift. Therefore, ESD handling precautions are required when handling the OPA688.

output limiters

The output voltage is linearly dependent on the input(s) when it is between the limiter voltages V_H (pin 8) and V_L (pin 5). When the output tries to exceed V_H or V_L, the corresponding limiter buffer takes control of the output voltage and holds it at V_H or V_L.

Because the limiters act on the output, their accuracy does not change with gain. The transition from the linear region of operation to output limiting is very sharp—the desired output signal can safely come to within 30 mV of V_H or V_L with no onset of non-linearity.

The limiter voltages can be set to within 0.7 V of the supplies ($V_L \geq -V_S + 0.7$ V, $V_H \leq +V_S - 0.7$ V). They must also be at least 400 mV apart ($V_H - V_L \geq 0.4$V).

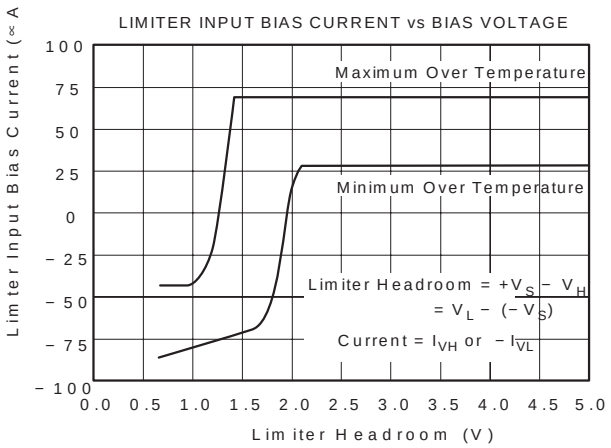


Figure 37. Limiter Bias Current vs Bias Voltage

When pins 5 and 8 are left open, V_H and V_L go to the Default Voltage Limit; the minimum values are in the Specifications. Looking at Figure 37 for the zero bias current case will show the expected range of (V_S _ default limit voltages) = headroom.

When the limiter voltages are more than 2.1V from the supplies ($V_L > -V_S + 2.1$ V or $V_H < +V_S - 2.1$ V), you can use simple resistor dividers to set V_H and V_L (see Figure 30). Make sure you include the Limiter Input Bias Currents (Figure 37) in the calculations (i.e., $I_{VL} \geq -50$ µA out of pin 5, and $I_{VH} \leq +50$ µA out of pin 8). For good limiter voltage accuracy, run at least 1-mA quiescent bias current through these resistors.

When the limiter voltages need to be within 2.1V of the supplies ($V_L \leq -V_S + 2.1$ V or $V_H \geq +V_S - 2.1$ V), consider using low impedance buffers to set V_H and V_L to minimize errors due to bias current uncertainty. This will typically be the case for single supply operation (V_S = +5V). Figure 31 runs 2.5 mA through the resistive divider that sets V_H and V_L. This keeps errors due to I_{VH} and I_{VL} < ±1% of the target limit voltages.

The limiters' DC accuracy depends on attention to detail. The two dominant error sources can be improved as follows:

- Power supplies, when used to drive resistive dividers that set V_H and V_L, can contribute large errors (e.g., ±5%). Using a more accurate source, and bypassing pins 5 and 8 with good capacitors, will improve limiter PSRR.
- The resistor tolerances in the resistive divider can also dominate. Use 1% resistors.

Other error sources also contribute, but should have little impact on the limiters' DC accuracy:

- Reduce offsets caused by the Limiter Input Bias Currents. Select the resistors in the resistive divider(s) as described above.
- Consider the signal path DC errors as contributing to uncertainty in the useable output swing.
- The Limiter Offset Voltage only slightly degrades limiter accuracy.

Figure 38 shows how the limiters affect distortion performance. Virtually no degradation in linearity is observed for output voltage swinging right up to the limiter voltages.

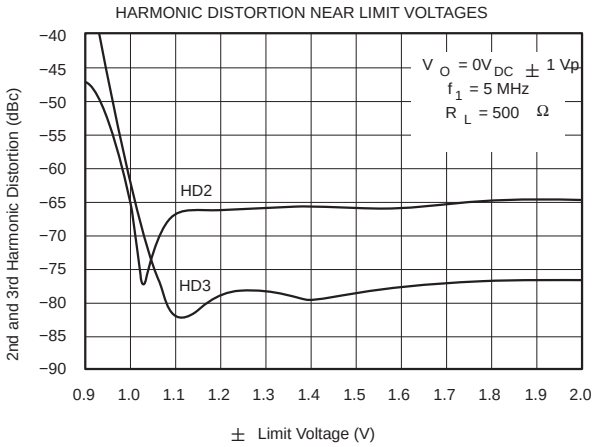
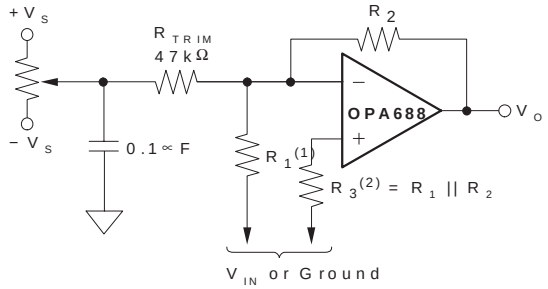


Figure 38. Harmonic Distortion Near Limit Voltages

offset voltage adjustment

The circuit in Figure 39 allows offset adjustment without degrading offset drift with temperature. Use this circuit with caution since power supply noise can inadvertently couple into the op amp.



NOTES: (1) Set $R_1 << R_{TRIM}$. (2) R_3 is optional and minimizes out ut offset due to in ut bias currents.

Figure 39. Offset Voltage Trim

Remember that additional offset errors can be created by the amplifier's input bias currents. Whenever possible, match the impedance seen by both DC input bias currents using R_3. This minimizes the output offset voltage caused by the input bias currents.

output drive

The OPA688 has been optimized to drive 500-Ω loads, such as ADCs. It still performs very well driving 100-Ω loads; the specifications are shown for the 500-Ω load. This makes the OPA688 an ideal choice for a wide range of high-frequency applications.

Many high-speed applications, such as driving ADCs, require op amps with low output impedance. As shown in the typical performance curve "Output Impedance vs Frequency", the OPA688 maintains very low closed-loop output impedance over frequency. Closed-loop output impedance increases with frequency, since loop gain decreases with frequency.

thermal considerations

The OPA688 will not require heat-sinking under most operating conditions. Maximum desired junction temperature will set a maximum allowed internal power dissipation as described below. In no case should the maximum junction temperature be allowed to exceed 150°C.

The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}) and the additional power dissipated in the output stage (P_{DL}) while delivering load power. P_{DQ} is simply the specified no-load supply current times the total supply voltage across the part. P_{DL} depends on the required output signals and loads. For a grounded resistive load, and equal bipolar supplies, it is at a maximum when the output is at 1/2 either supply voltage. In this condition, $P_{DL} = V_S^2/(4R_L)$ where R_L includes the feedback network loading. Note that it is the power in the output stage, and not in the load, that comprises P_{DL}.

The operating junction temperature is: $T_J = T_A + P_D \Theta_{JA}$, where T_A is the ambient temperature.

For example, the maximum T_J for a OPA688M with G = +2, R_{FB} = 402 Ω, R_L = 100 Ω, and $\pm V_S$ = ±5 V at the maximum T_A = + 85°C is calculated as:

$$P_{DQ} = (10\ V \times 20\ mA) = 200\ mW$$

$$P_{DL} = \frac{(5\ V)^2}{4 \times (100\ \Omega \parallel 804\ \Omega)} = 70\ mW$$

$$P_D = 200\ mW + 70\ mW = 270\ mW$$

$$T_J = 85°C + 270\ mW \times (119°C/W) = 117°C$$

capacitive loads

Capacitive loads, such as the input to ADCs, will decrease the amplifier's phase margin, which may cause high-frequency peaking or oscillations. Capacitive loads × 2 pF should be isolated by connecting a small resistor in series with the output as shown in Figure 40. Increasing the gain from +2 will improve the capacitive drive capabilities due to increased phase margin.

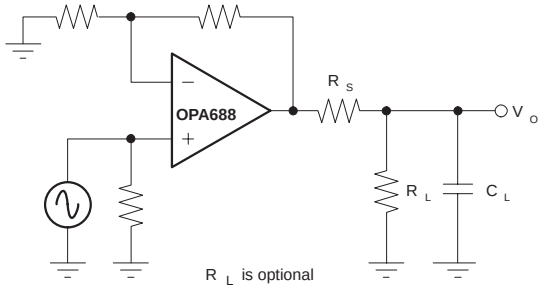


Figure 40. Driving Capacitive Loads

In general, capacitive loads should be minimized for optimum high-frequency performance. The capacitance of coax cable (29 pF/foot for RG-58) will not load the amplifier when the coaxial cable, or transmission line, is terminated in its characteristic impedance.

frequency response compensation

The OPA688 is internally compensated to be unity-gain stable, and has a nominal phase margin of 60° at a gain of +2. Phase margin and peaking improve at higher gains. Recall that an inverting gain of −1 is equivalent to a gain of +2 for bandwidth purposes (i.e., noise gain = 2).

Standard external compensation techniques work with this device. For example, in the inverting configuration, the bandwidth may be limited without modifying the inverting gain by placing a series RC network to ground on the inverting node. This has the effect of increasing the noise gain at high frequencies, which limits the bandwidth.

To maintain a wide bandwidth at high gains, cascade several op amps, or use the high gain optimized OPA689.

In applications where a large feedback resistor is required, such as photodiode transimpedance amplifier, the parasitic capacitance from the inverting input to ground causes peaking or oscillations. To compensate for this effect, connect a small capacitor in parallel with the feedback resistor. The bandwidth will be limited by the pole that the feedback resistor and this capacitor create. In other high gain applications, use a three resistor ”Tee” network to reduce the RC time constants set by the parasitic capacitances. Be careful to not increase the noise generated by this feedback network too much.

pulse settling time

The OPA688 is capable of an extremely fast settling time in response to a pulse input. Frequency response flatness and phase linearity are needed to obtain the best settling times. For capacitive loads, such as an ADC, use the recommended R_S in the typical performance curve ”R_S vs Capacitive Load”. Extremely fine-scale settling (0.01%) requires close attention to ground return current in the supply decoupling capacitors.

The pulse settling characteristics when recovering from overdrive are very good.

distortion

The OPA688’s distortion performance is specified for a 500-Ω load, such as an ADC. Driving loads with smaller resistance will increase the distortion as illustrated in Figure 41. Remember to include the feedback network in the load resistance calculations.

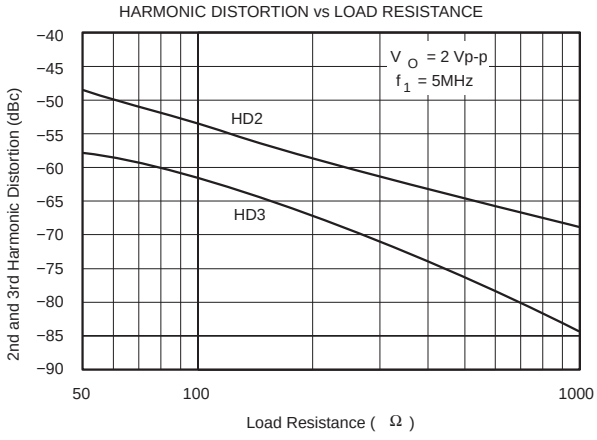


Figure 41. 5 MHz Harmonic Distortion vs Load Resistance

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA688MJD	NRND	CDIP SB	JD	8	45	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	OPA688MJD	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

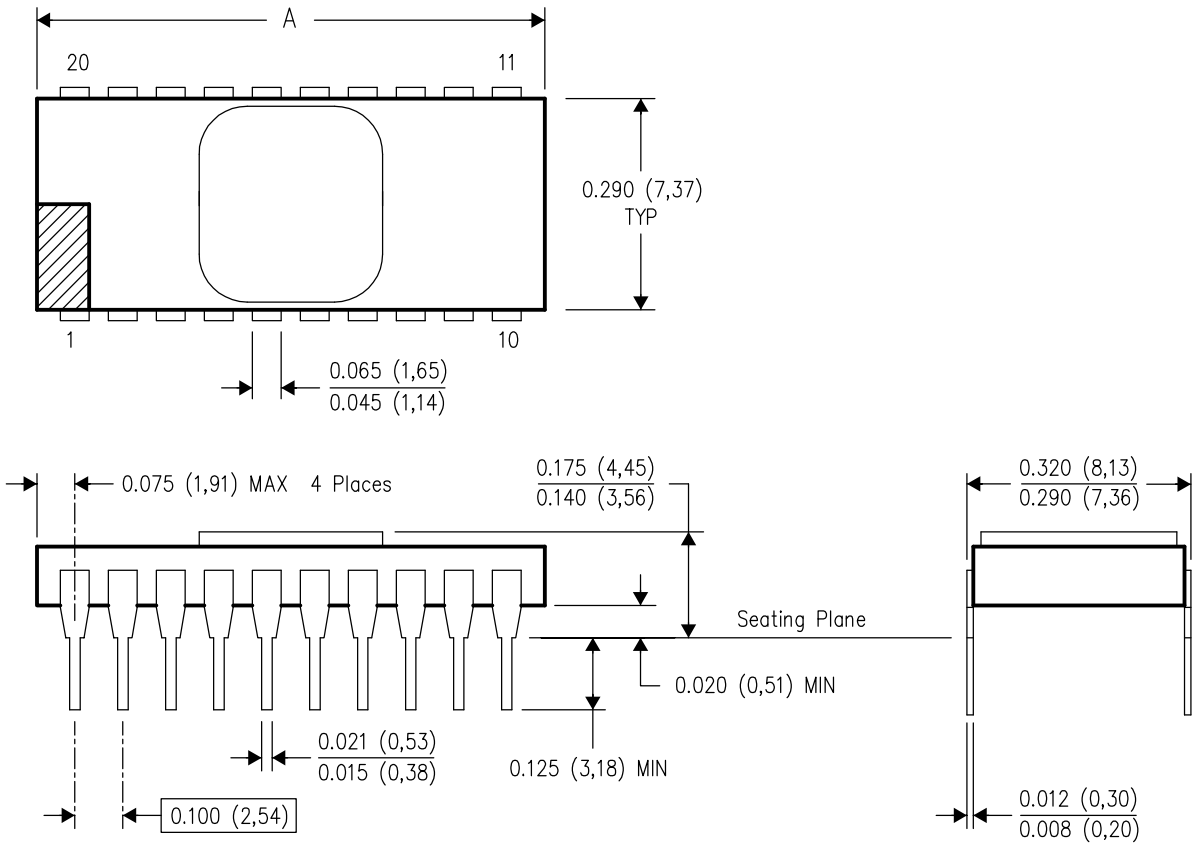
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

JD (R–CDIP–T**) CERAMIC SIDE–BRAZE DUAL–IN–LINE PACKAGE

20 PINS SHOWN



DIM \ PINS **	8	14	16	18	20	24
A MAX	0.405 (10,29)	0.757 (19,23)	0.810 (20,57)	0.910 (23,11)	1.010 (25,65)	1.100 (27,94)

4040086–2/F 07/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within MIL STD 1835 CDIP2 – T8, T14, T16, T18, T20 and T24 respectively.

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