SNx5173 Quadruple Differential Line Receivers

1 Features

- Meet or exceed the requirements of TIA/EIA-422-B, TIA/EIA-423-B, and TIA/EIA-485-A and ITU recommendations V.10, V.11, X.26, and X.27
- Designed for multipoint bus transmission on long bus lines in noisy environments
- 3-State outputs
- Common-mode input voltage range of –12 V to 12 V
- Input sensitivity: ±200 mV
- Input hysteresis: 50 mV typical
- High Input Impedance : 12 kΩ minimum
- Operate from single 5-V supply
- Low power requirements
- Pin-to-pin replacement for AM26LS32

2 Applications

- Motor drives
- Factory automation and control

3 Description

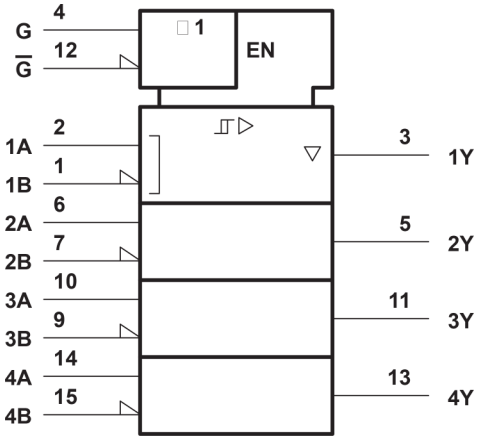
The SN55173 and SN75173 are monolithic quadruple differential line receivers with 3-state outputs. They are designed to meet the requirements of TIA/EIA-422-B, TIA/EIA-423-B, TIA/EIA-485-A, and several ITU recommendations. The standards are for balanced multipoint bus transmission at rates up to 10 megabits per second. The four receivers share two OR enable inputs, one active when high, the other active when low. These devices feature high input impedance, input hysteresis for increased noise immunity, and input sensitivity of ± 200 mV over a common-mode input voltage range of – 12 V to 12 V. Fail-safe design specifies that if the inputs are open circuited, the outputs are always high. The SN65173 and SN75173 are designed for optimum performance when used with the SN75172 or SN75174 quad differential line drivers.

The SN55173 is characterized over the full military temperature range of – 55°C to 125°C. The SN75173 is characterized for operation from 0°C to 70°C.

Package Information

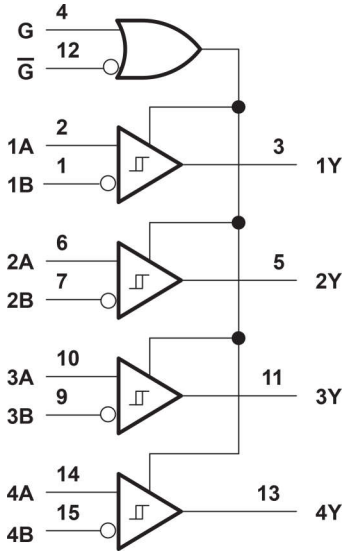
PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
SN55173	J (CDIP, 16)	6.92 mm × 19.56 mm
	FK (LCCC, 20)(3)	8.89 mm × 8.89 mm
SN75173	D (SOIC, 16)	9.9 mm × 6 mm
	N (PDIP, 16)	19.3 × 9.4 mm
	NS (SO, 16)	10.2 × 7.8 mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) Not recommended for new designs.



A. This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the D, J, and N packages.
B. Pin numbers shown are for the D, J, and N packages.

Logic Symbol



Logic Diagram (Positive Logic)

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Pin Configuration and Functions

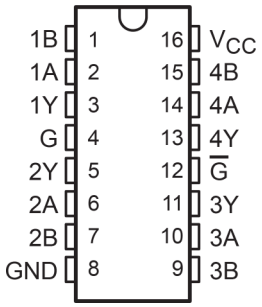
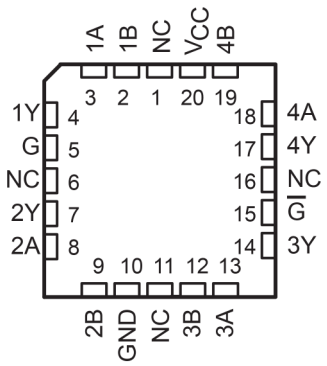


Figure 4-1. SN55173: J Package
SN75173: D, N or NS Package
(Top View)

Table 4-1. Pin Functions

PIN		TYPE#none#	DESCRIPTION
NAME	NO.		
1B	1	I	Channel 1 Differential Receiver Inverting Input
1A	2	I	Channel 1 Differential Receiver Non-Inverting Input
1Y	3	O	Channel 1 Single Ended Output
G	4	I	Active High Enable
2Y	5	O	Channel 2 Single Ended Output
2A	6	I	Channel 2 Differential Receiver Non-Inverting Input
2B	7	I	Channel 2 Differential Receiver Inverting Input
GND	8	GND	Device GND
3B	9	I	Channel 3 Differential Receiver Inverting Input
3A	10	I	Channel 3 Differential Receiver Non-Inverting Input
3Y	11	O	Channel 3 Single Ended Output
$\overline{G}$	12	I	Active Low Enable
4Y	13	O	Channel 4 Single Ended Output
4A	14	I	Channel 4 Differential Receiver Non-Inverting Input
4B	15	I	Channel 4 Differential Receiver Inverting Input
V_{CC}	16	PWR	Device V_{CC} (4.75 V to 5.25 V)

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NC – No internal connection

Figure 4-2. SN55173: FK Package (Top View)

A. The SN55173 FK package is not recommended for new designs.

Table 4-2. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
NC	1, 6, 11, 16	--	No Connect
1B	2	I	Differential Receiver Inverting Input
1A	3	I	Differential Receiver Non-Inverting Input
1Y	4	O	Single Ended Output
G	5	I	Active High Enable
2Y	7	O	Single Ended Output
2A	8	I	Differential Receiver Non-Inverting Input
2B	9	I	Differential Receiver Inverting Input
GND	10	GND	Device GND
3B	12	I	Differential Receiver Inverting Input
3A	13	I	Differential Receiver Non-Inverting Input
3Y	14	O	Single Ended Output
$\overline{G}$	15	I	Active Low Enable
4Y	17	O	Single Ended Output
4A	18	I	Differential Receiver Non-Inverting Input
4B	19	I	Receiver Inverting Input
V_{CC}	20	PWR	Device VCC

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC} (2)	Supply voltage				V
V_I	Input voltage (A or B inputs)			± 25	V
V_{ID} (3)	Differential input voltage			± 25	V
$V_{I(EN)}$	Enable input voltage				V
I_{OL}	Low-level output current			50	mA
	Continuous total dissipation		See Dissipation Rating Table		
	Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds:	D or N package		260	°C
	Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds:	J package		300	°C
T_{stg}	Storage temperature range		65	150	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential input voltage, are with respect to network ground terminal.
(3) Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.

5.2 Dissipation Rating Table

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
FK	1375 mW	11 mW/°C	880 mW	275 mW
J	1375 mW	11 mW/°C	880 mW	275 mW

5.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	SN55173	4.5	5	5.5	V
	SN75173	4.75	5	5.25	V
Common-mode input voltage, V_{IC}				± 12	V
Differential input voltage, V_{ID}				± 12	V
High-level enable-input voltage, V_{IH}		2			V
Low-level enable-input voltage, V_{IL}				0.8	V
High-level output current, I_{OH}				– 400	µA
Low-level output current, I_{OL}				16	mA
Operating free-air temperature, T_A	SN55173	– 55		125	°C
	SN75173	0		70	

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5.4 Thermal Information

THERMAL METRIC[1]		D (SOIC)	N (PDIP)	NS (SOP)	J (CDIP)	UNIT
		16-PINS				
$R_{\theta JA}$	Junction-to-ambient thermal resistance	84.6	60.6	88.5	65.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	43.5	48.1	46.2	54.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.2	40.6	50.7	42.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.4	27.5	13.5	22.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	42.8	40.3	50.3	41.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

5.5 Electrical Characteristics

over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature

PARAMETER		TEST CONDITIONS			MIN	TYP[1]	MAX	UNIT
VIT+	Positive-going input threshold voltage	V_O = 2.7 V,	I_O = – 0.4 mA				0.2	V
VIT–	Negative-going input threshold voltage	V_O = 0.5 V,	I_O = 16 mA			– 0.2[2]		V
Vhys	Hysteresis (V_{IT+} – $V_{IT–}$)	See Figure 5-1				50		mV
VIK	Enable-input clamp voltage	I_I = – 18 mA					– 1.5	V
VOH	High-level output voltage	V_{ID} = 200 mV,	I_{OH} = – 400 µA	SN55173	2.5			V
				SN75173	2.7			V
VOL	Low-level output voltage	V_{ID} = – 200 mV,	See Figure 6-1	I_{OL} = 8 mA			0.45	V
				I_{OL} = 16 mA			0.5	
IOZ	High-impedance-state output current	V_O = 0.4 V to 2.4 V					± 20	µA
I_I	Line input current	Other input at 0 V,	See Note 3	V_I = 12 V			1	mA
				V_I = – 7 V			– 0.8	
IIH	High-level enable-input current	V_{IH} = 2.7 V					20	µA
IIL	Low-level enable-input current	V_{IL} = 0.4 V					– 100	µA
r_i	Input resistance					12		kΩ
IOS	Short-circuit output current					– 15	– 85	mA
ICC	Supply current	Outputs disabled					70	mA

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.
(2) The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for threshold voltage levels only.
(3) Refer to TIA/EIA-422-B and TIA/EIA-423-B for exact conditions.

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5.6 Switching Characteristics

V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = – 1.5 V to 1.5 V, C_L = 15 pF, See Figure 6-1		20	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output			22	35	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF, See Figure 6-2		17	22	ns
t_{PZL}	Output enable time to low level	C_L = 15 pF, See Figure 6-3		20	25	ns
t_{PHZ}	Output disable time from high level	C_L = 5 pF, See Figure 6-2		21	30	ns
t_{PLZ}	Output disable time from low level	C_L = 5 pF, See Figure 6-3		30	40	ns

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5.7 Typical Characteristics

Operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied.

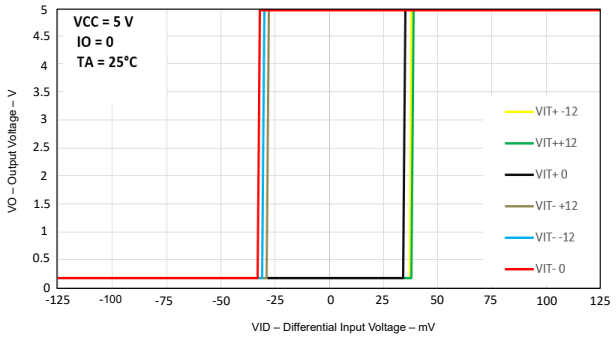


Figure 5-1. Output Voltage vs Differential Input Voltage

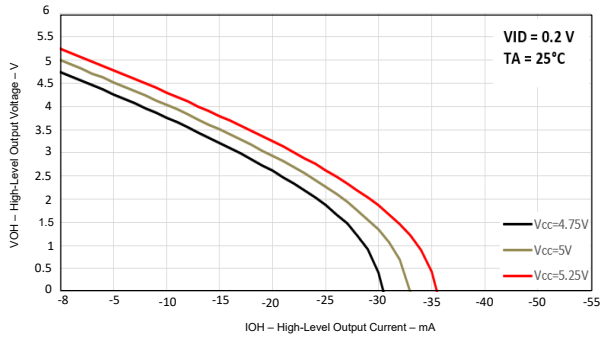


Figure 5-2. High-level Output Voltage vs High-level Output Current

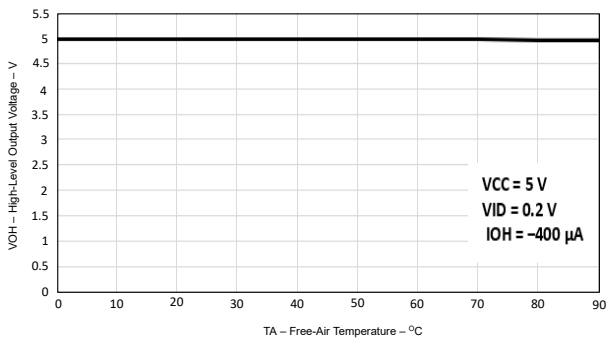


Figure 5-3. High-level Output Voltage vs Free-air Temperature 5

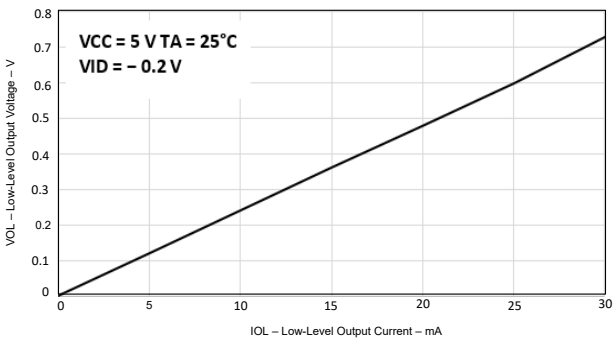


Figure 5-4. Low-level Output Voltage vs Low-level Output Current

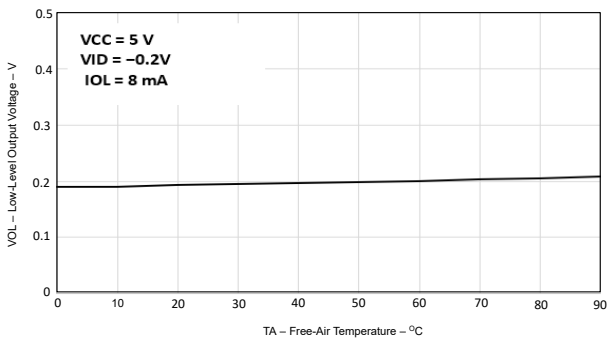


Figure 5-5. Low-level Output Voltage vs Free-air Temperature

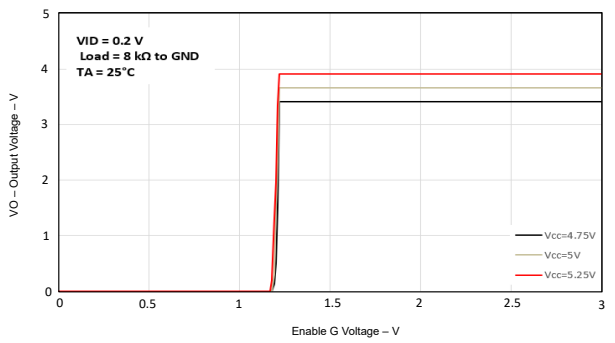


Figure 5-6. Output Voltage vs Enable G Voltage

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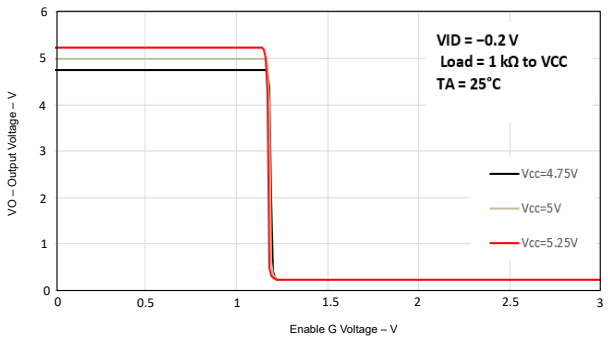


Figure 5-7. Output Voltage vs Enable G Voltage

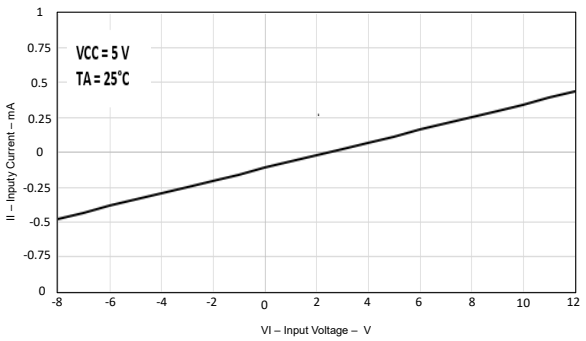
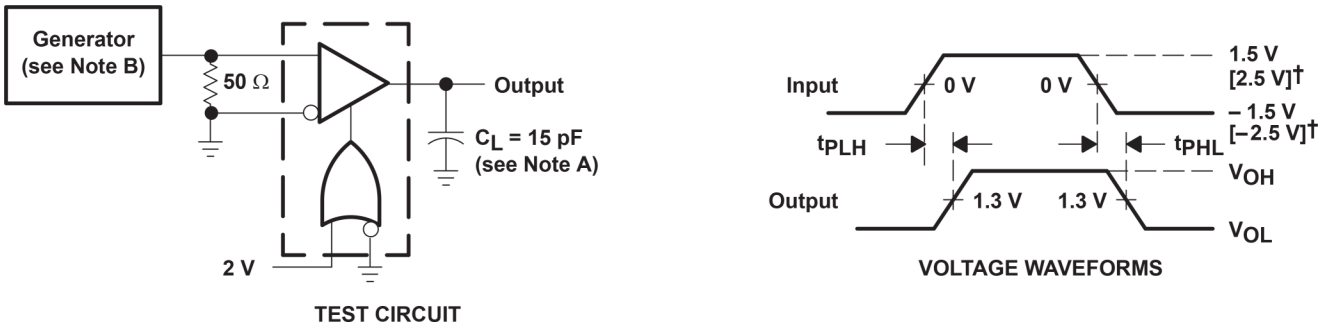


Figure 5-8. Input Current vs Input Voltage

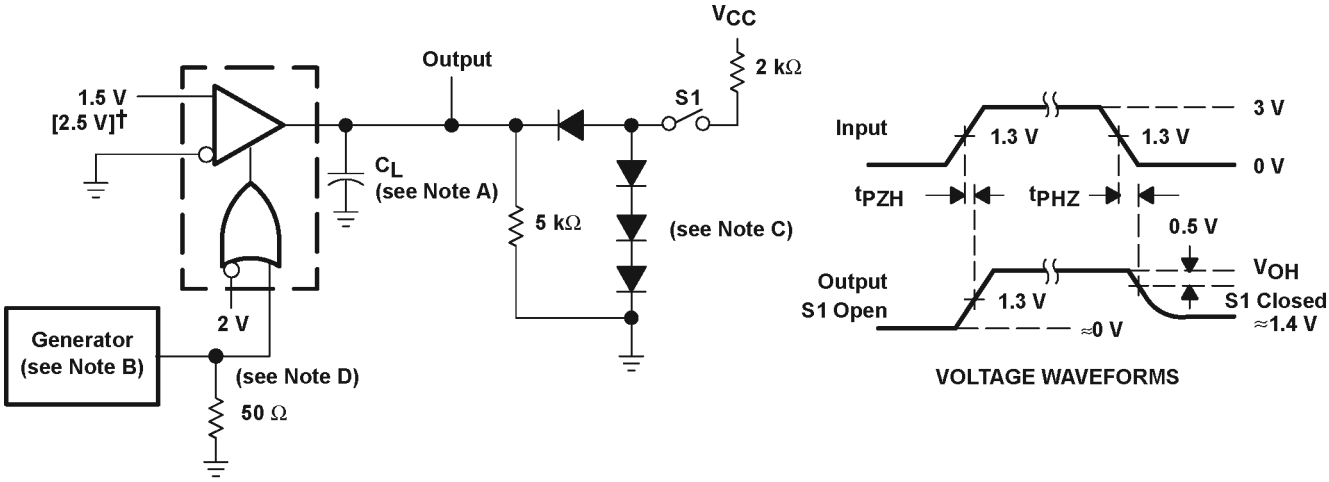
6 Parameter Measurement Information



TEST CIRCUIT VOLTAGE WAVEFORMS

A. † Voltage for the SN55173 only.
B. C_L includes probe and jig capacitance.
C. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r \le 6$ ns, $t_f \le 6$ ns, Z_O = 50 Ω.

Figure 6-1. t_{PLH}, T_{PHL} Test Circuit and Voltage Waveforms

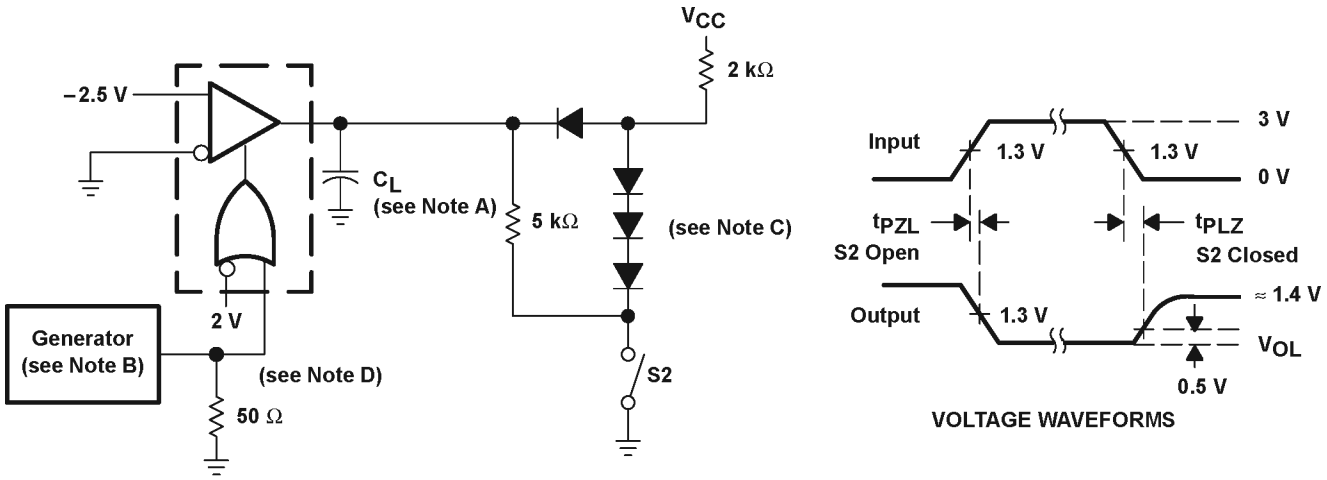


TEST CIRCUIT VOLTAGE WAVEFORMS

A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r \le 6$ ns, $t_f \le 6$ ns, Z_O = 50 Ω.
C. All diodes are 1N916, or equivalent.
D. To test the active-low enable $\overline{G}$, ground G and apply an inverted input waveform to G.

Figure 6-2. t_{PHZ}, T_{PZH} Test Circuit and Voltage Waveforms

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A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r \le 6$ ns, $t_f \le 6$ ns, Z_O = 50 Ω.

C. All diodes are 1N916, or equivalent.

D. To test the active-low enable G, ground G and apply an inverted input waveform to G.

Figure 6-3. t_{PZL}, T_{PLZ} Test Circuit and Voltage Waveforms

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7 Detailed Description

7.1 Device Functional Modes

Table 7-1. Function Table (Each Receiver)

DIFFERENTIAL A–B	ENABLES(1)		OUTPUT Y
	G	$\overline{G}$	
$V_{ID} \geq 0.2$ V	H	X	H
	X	L	H
–0.2 V < V_{ID} < 0.2 V	H	XL	?
	X		?
$V_{ID} \leq$ –0.2 V	H	X	L
	X	L	L
X	L	H	Z
Open circuit	X	L	H
	H	X	H

(1) H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off)

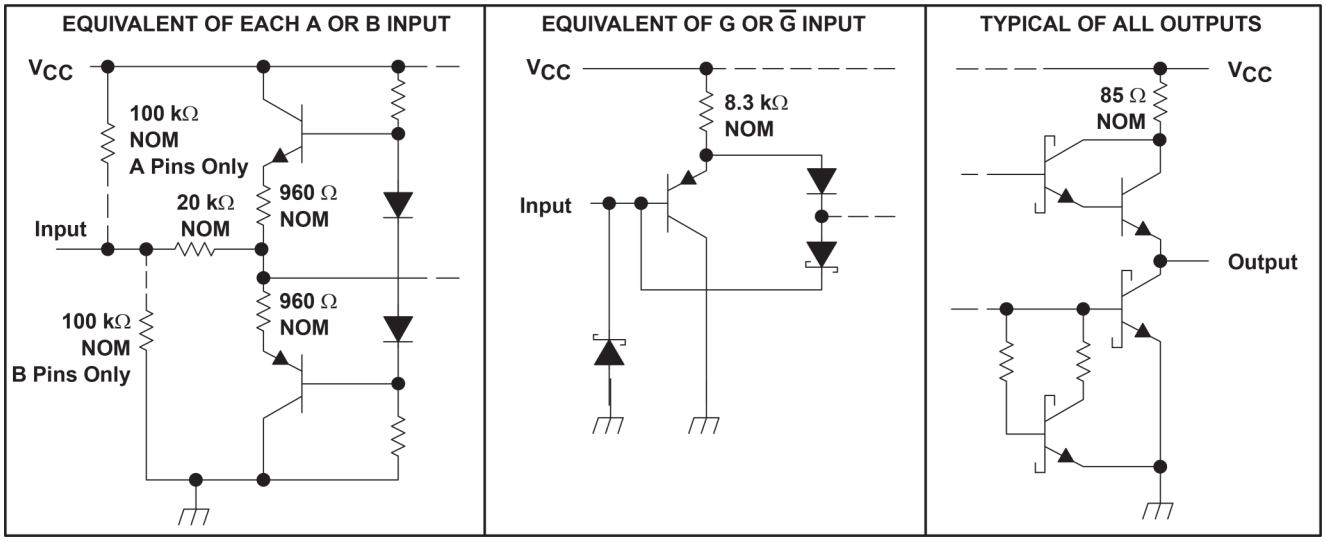


Figure 7-1. Schematics of Inputs and Outputs

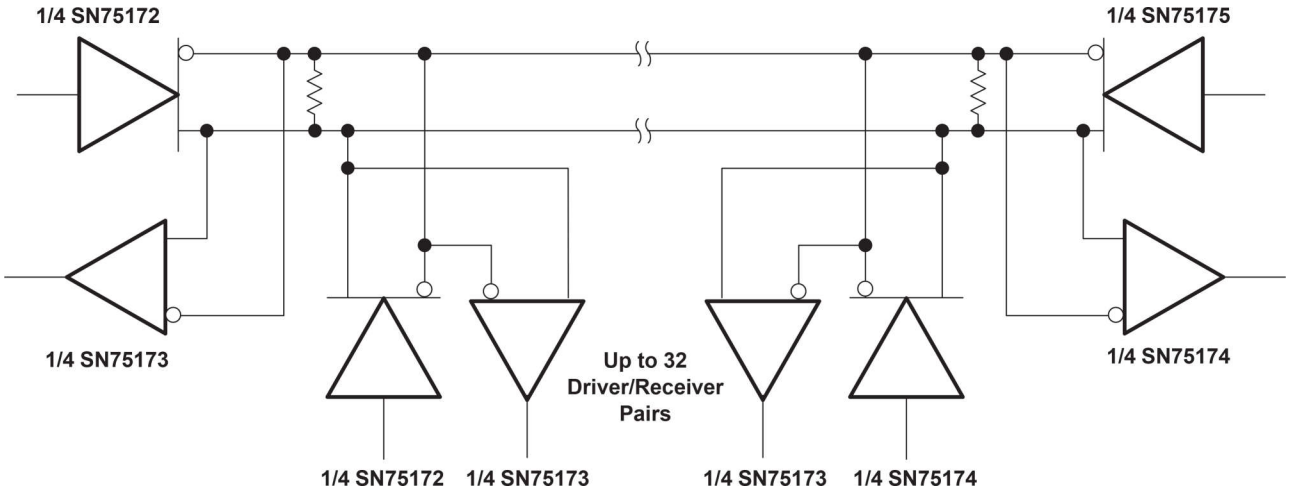
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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information



A. The line should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

Figure 8-1. Typical Application Circuit

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (April 2000) to Revision F (October 2023)	Page
• Changed the numbering format for tables, figures, and cross-references throughout the document	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN55173J	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN55173J	Samples
SN75173D	LIFEBUY	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75173	
SN75173DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75173	Samples
SN75173N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN75173N	Samples
SNJ55173J	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ55173J	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN55173, SN75173 :

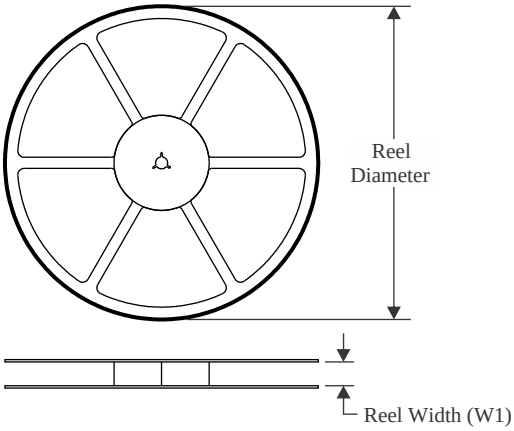
- Catalog : SN75173
- Military : SN55173

NOTE: Qualified Version Definitions:

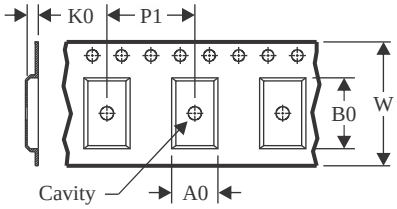
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

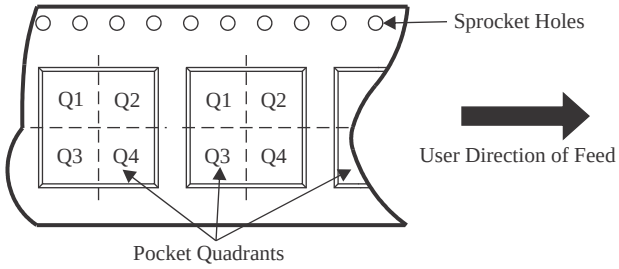


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

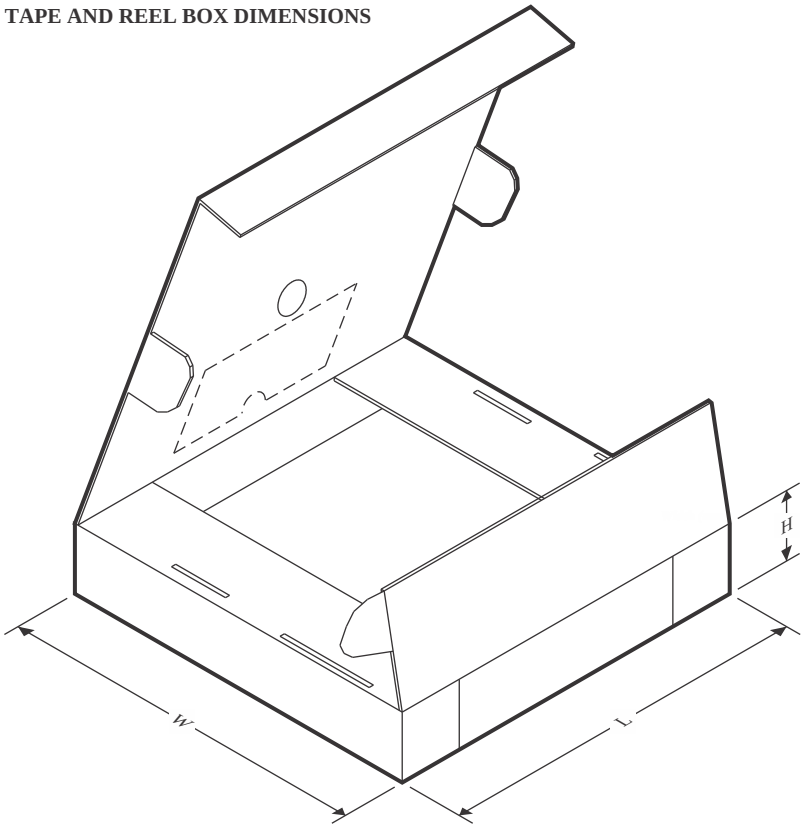
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75173DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

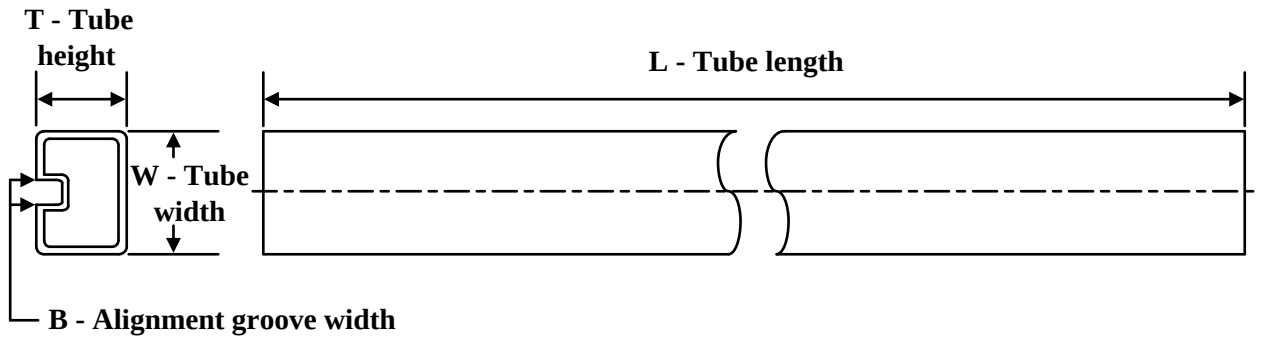
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75173DR	SOIC	D	16	2500	353.0	353.0	32.0

TUBE



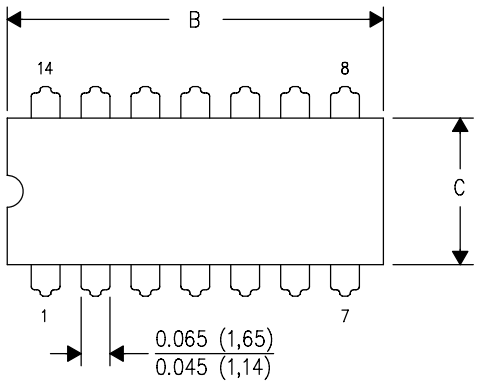
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN75173D	D	SOIC	16	40	507	8	3940	4.32
SN75173N	N	PDIP	16	25	506	13.97	11230	4.32

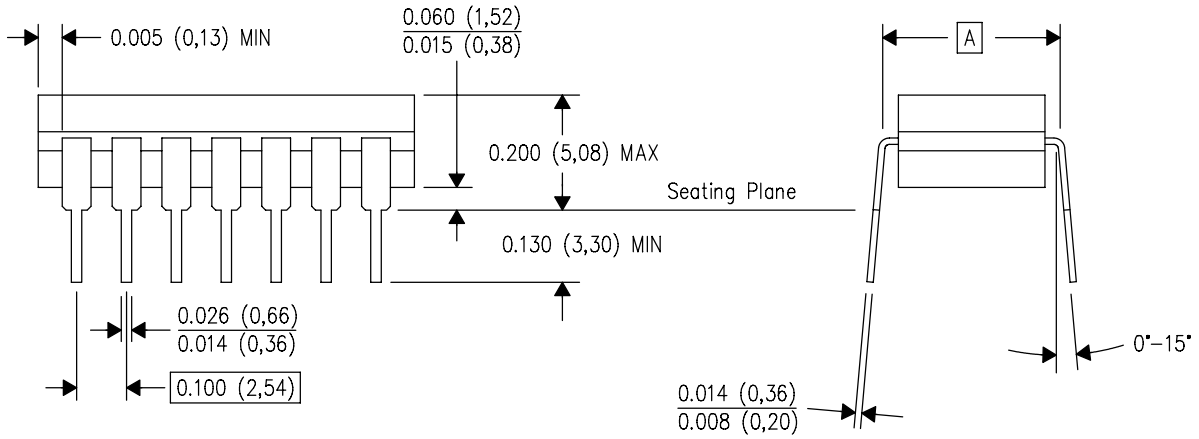
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



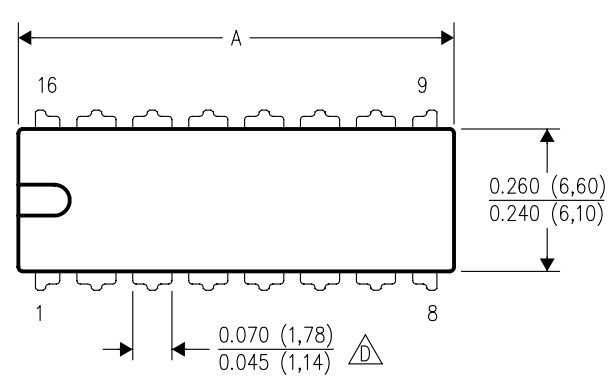
4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

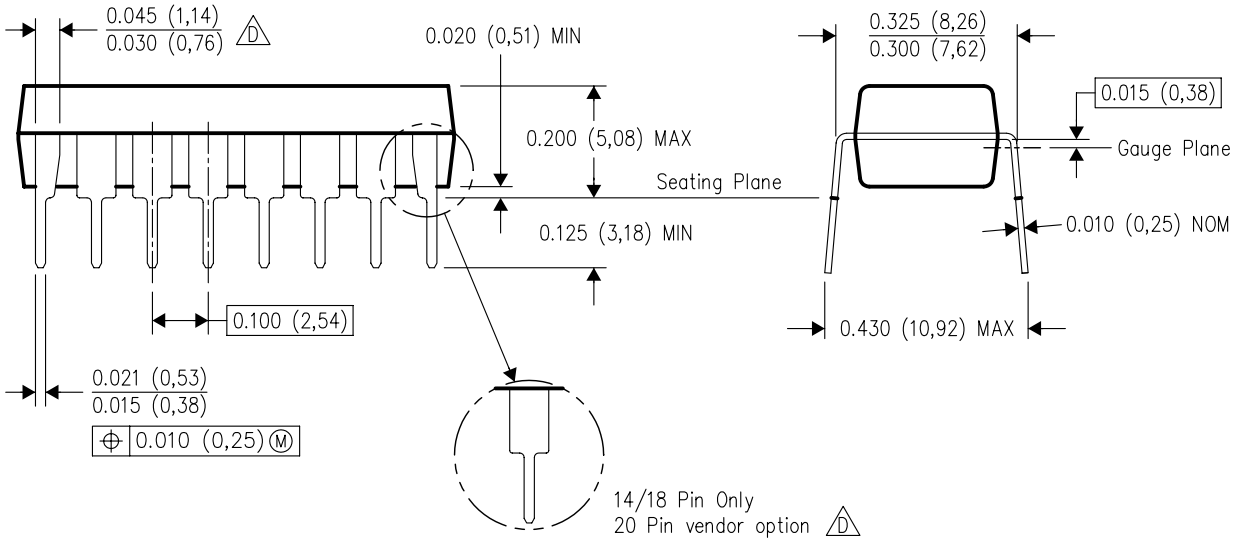
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



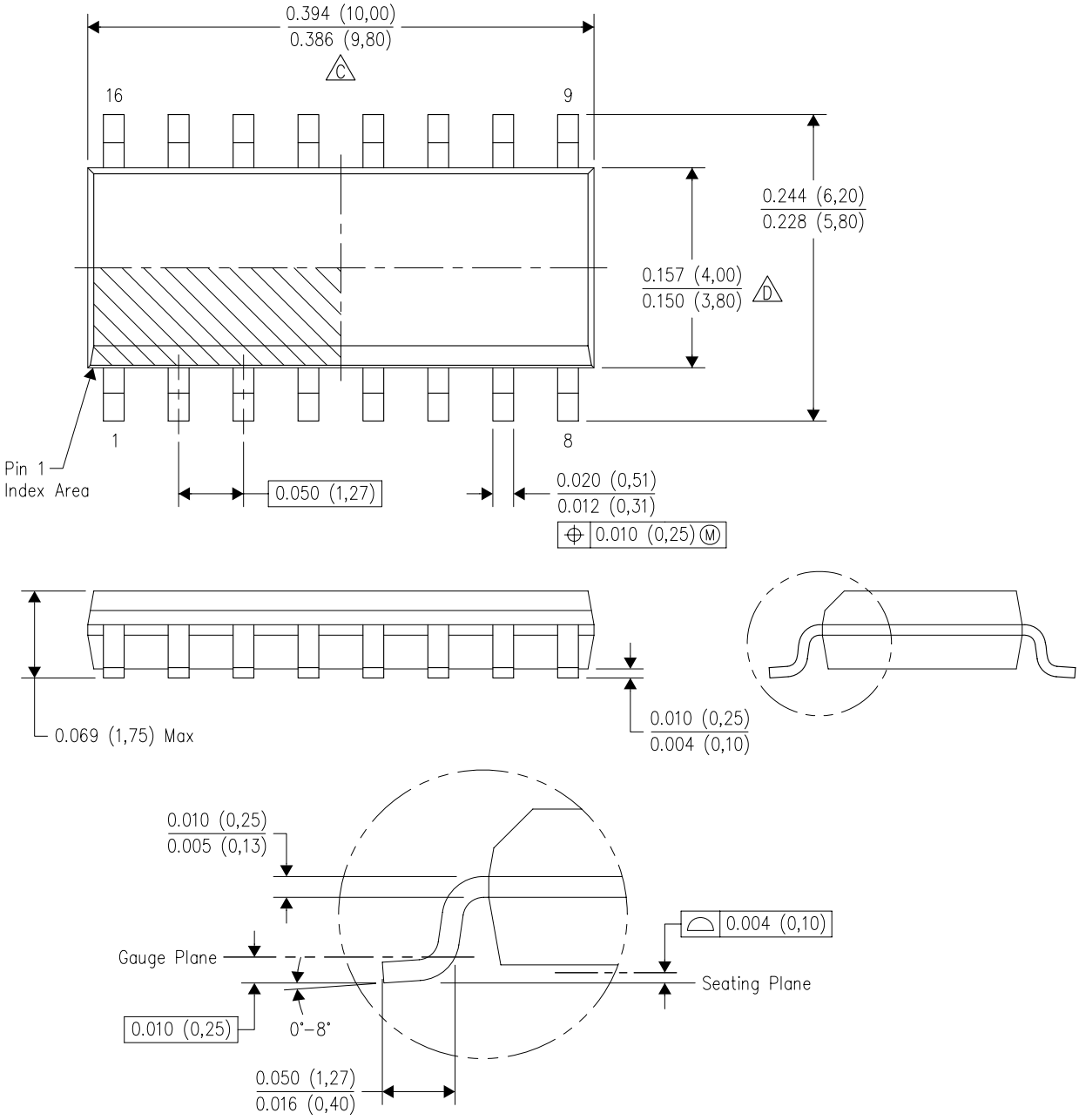
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

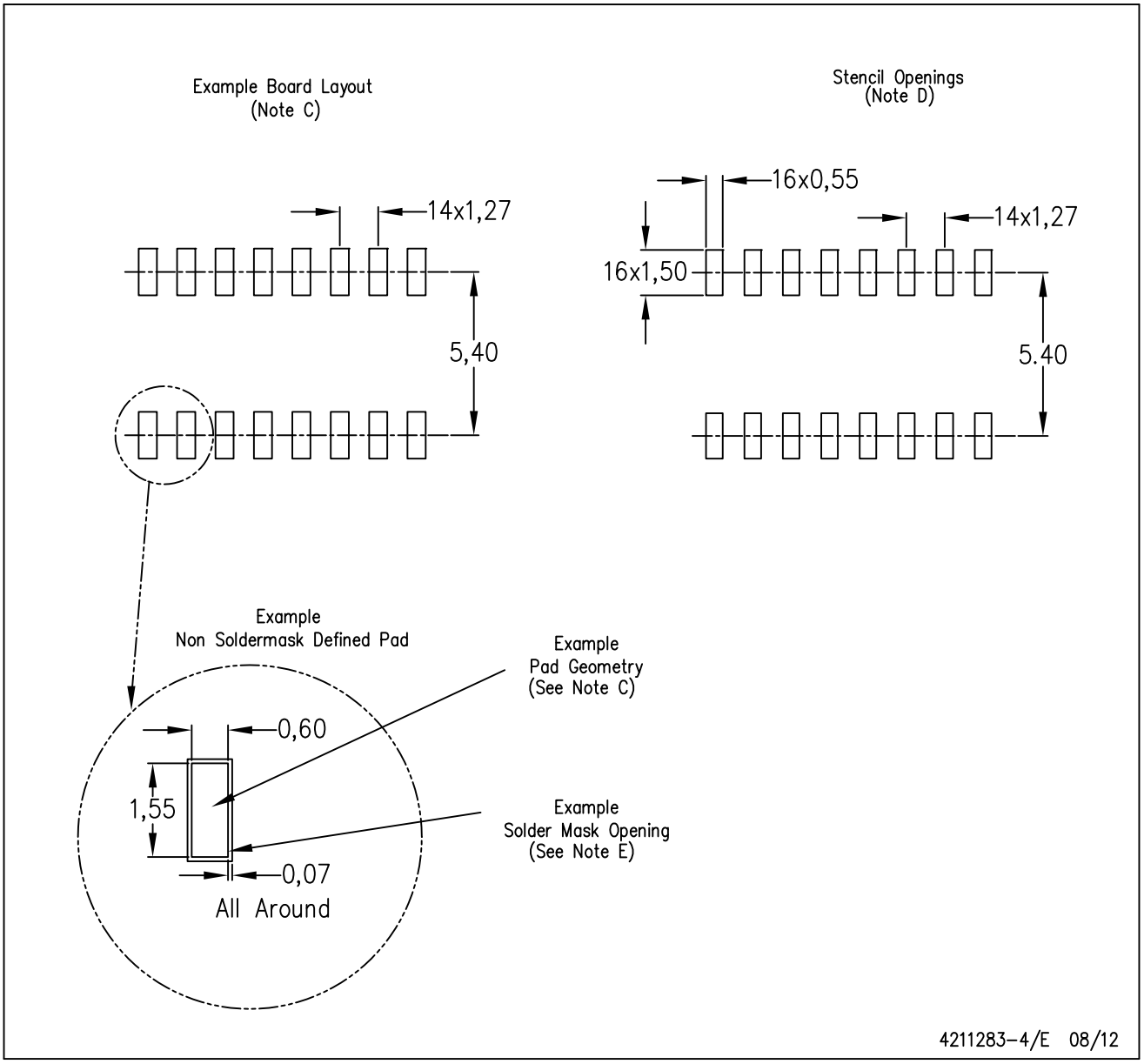
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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