SN65LVPE512 Dual-Channel USB 3.0 Redriver, Equalizer

1 Features

- Single Lane USB 3.0 Equalizer, Redriver
- Selectable Equalization, De-Emphasis and Output Swing Control
- Integrated Termination
- Hot-Plug Capable
- Low Active Power (U0 state)
  - 315 mW (Typical), V_{CC} = 3.3 V
- USB 3.0 Low Power Support
  - 7 mW (Typical) When No Connection Detected
  - 70 mW (Typical) When Link in U2, U3 Mode
- Excellent Jitter and Loss Compensation Capability:
  - > 40 Inches of Total 4-Mil Stripline on FR4
- Small Foot Print: 3 mm × 3 mm and 4 mm × 4 mm 24-pin QFN Packages
- High Protection Against ESD Transient
  - HBM: 5,000 V
  - CDM: 1,500 V
  - MM: 200 V

2 Applications

- Notebooks
- Desktops
- Docking Stations
- Active Cables
- Backplane
- Active Cables

3 Description

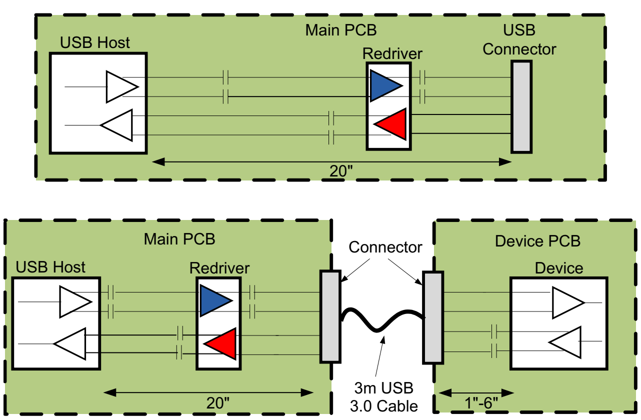
The SN65LVPE512 device is a dual-channel, single-lane USB 3.0 redriver and signal conditioner supporting data rates of 5 Gbps. The device complies with USB 3.0 spec revision 1.0, supporting electrical idle condition and low frequency periodic signals (LFPS) for USB 3.0 power management modes.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN65LVPE512	VQFN (24)	4.00 mm × 4.00 mm
	WQFN (24)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application



Data Flow Block Diagram

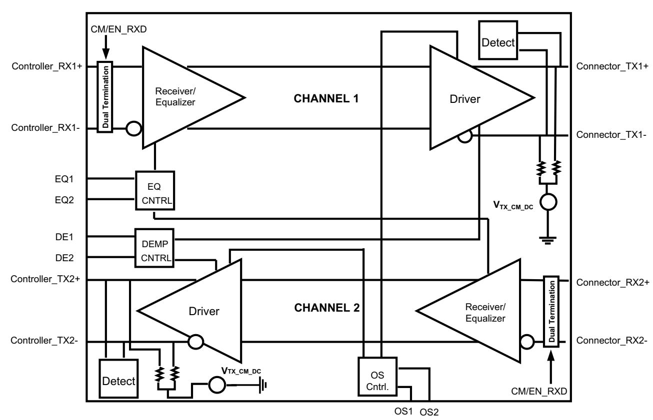


Table of Contents

4 Revision History

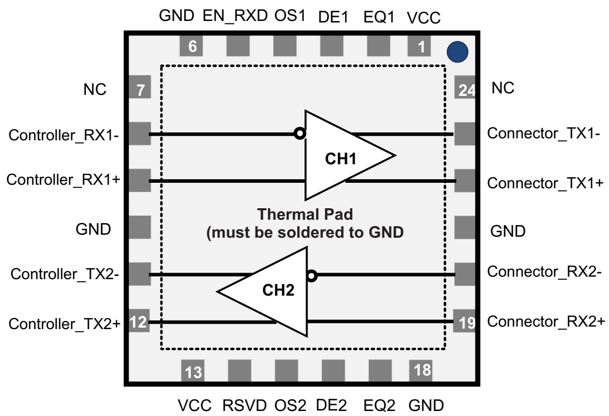
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (January 2013) to Revision B	**Page**
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section.	1

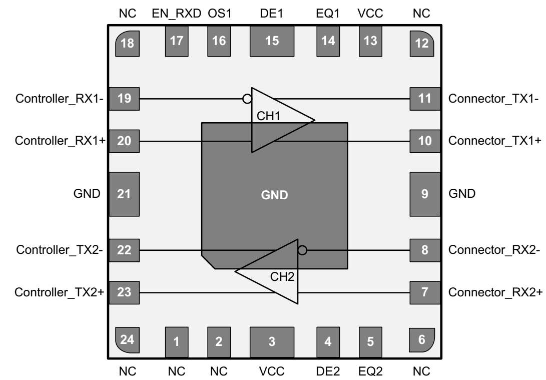
Changes from Original (December 2013) to Revision A	**Page**
• Changed the device status From: Product Preview To: Production	1

5 Pin Configuration and Functions

RGE Package
24-Pin VQFN
Top View



RMQ Package
24-Pin WQFN
Top View



Pin Functions

PIN			I/O TYPE	DESCRIPTION
NAME	VQFN	WQFN		
HIGH SPEED DIFFERENTIAL I/O PINS				
Controller_RX1–	8	19	I, CML	Non-inverting and inverting CML differential input for CH1 and CH2. These pins are tied to an internal voltage bias by dual termination resistor circuit. Pins labeled *Controller* must connect to the USB 3.0 host or device controller. Pins labeled *Connector* must connect to the USB 3.0 connector.
Controller_RX1+	9	20	I, CML	
Connector_RX2–	20	8	I, CML	
Connector_RX2+	19	7	I, CML	
Connector_TX1–	23	11	O, CML	Non-inverting and inverting CML differential output for CH1 and CH2. These pins are tied to an internal voltage bias by termination resistors. Pins labeled *Controller* must connect to the USB 3.0 host or device controller. Pins labeled *Connector* must connect to the USB 3.0 connector.
Connector_TX1+	22	10	O, CML	
Controller_TX2–	11	22	O, CML	
Controller_TX2+	12	23	O, CML	
DEVICE CONTROL PIN				
EN_RXD	5	17	I, LVCMOS	Sets device operation modes per Table 4. Internally pulled to V_{CC}.
RSVD	14	—	I, LVCMOS	RSVD. Can be left as No-Connect.
NC	7, 24	1, 2, 6, 12, 18, 24	No-Connect	Pads are not internally connected.
EQ CONTROL PINS(1)				
DE1, DE2	3, 16	15, 4	I, LVCMOS	Selects de-emphasis settings for CH1 and CH2 per Table 4. Internally tied to $V_{CC}/2$
EQ1, EQ2	2, 17	14, 5	I, LVCMOS	Selects equalization settings for CH1 and CH2 per Table 4. Internally tied to $V_{CC}/2$
OS1, OS2	4, 15	16, NC (2)	I, LVCMOS	Selects output amplitude for CH1 and CH2 per Table 4. Internally tied to $V_{CC}/2$
POWER PINS				
VCC	1,13	3	Power	Positive supply; must be 3.3 V ±10%
GND	6, 10, 18, 21, Thermal Pad	9, Thermal Pad	Power	Supply Ground

(1) Internally biased to $V_{CC}/2$ with > 200-kΩ pullup or pulldown. When pins are left as NC board leakage at this pin pad must be < 1 µA otherwise drive to $V_{CC}/2$ to assert mid-level state
(2) The RMQ has OS2 internally No-Connect, to select the 1042 mVpp level on TX2.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage(2)	V_{CC}	–0.5	4	V
Voltage	Differential I/O	–0.5	4	V
	Control I/O	–0.5	VCC + 0.5	V
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to network ground terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±5000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	
		Machine model(3)	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
(3) Tested in accordance with JEDEC Standard 22, Test Method A115-A

6.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3	3.3	3.6	V
$C_{COUPLING}$	AC-coupling capacitor		75		200	nF
	Operating free-air temperature		–40		85	°C
DEVICE PARAMETERS						
I_{CC}	Supply current	EN_RXD, RSVD, EQ cntrl = NC, K28.5 pattern at 5 Gbps, VID = 1000mVp-p		100	120	mA
$ICC_{Rx.Detect}$		In Rx.Detect mode		2	5	
ICC_{sleep}		EN_RXD = GND		0.01	0.1	
ICC_{U2-U3}		Link in USB low power state		21		
	Maximum data rate				5	Gbps
t_{ENB}	Device enable time	Sleep mode exit time EN_RXD L → H With Rx termination present			100	µs
t_{DIS}	Device disable time	Sleep mode entry time EN_RXD H → L			2	µs
$T_{RX.DETECT}$	Rx.Detect start event	Power-up time			100	µs
CONTROL LOGIC						
V_{IH}	High level input voltage		2.8		V_{CC}	V
V_{IL}	Low level input voltage		–0.3		0.5	V
V_{HYS}	Input hysteresis			150		mV
I_{IH}	High level input current	OSx, EQx, DEx = V_{CC}			30	µA
		EN_RXD = V_{CC}			1	
		RSVD = V_{CC}			30	
I_{IL}	Low level input current	OSx, EQx, DEx = GND	–30			µA
		EN_RXD = GND	–30			
		RSVD = GND	–1			

6.4 Thermal Information

THERMAL METRIC(1)		SN65LVPE512		UNIT
		RGE (VQFN)	RMQ (WQFN)	
		24 PINS	24 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	47.5	41.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.6	37	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	24.6	11.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	6.4	6.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.4	0.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	24.6	11.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Device power dissipation	RSVD, EN_RXD, EQ cntrl pins = NC, K28.5 pattern at 5 Gbps, V_{ID} = 1000 mV_{p-p}		330	450(1)	mW
P_{Slp}	Device power dissipation in sleep mode	EN_RXD = GND		0.03	0.4	mW
RECEIVER AC/DC						
Vin_{diff_p-p}	RX1, RX2 input voltage swing	AC-coupled differential RX peak to peak signal	100		1200	mVpp
VCM_RX	RX1, RX2 common-mode voltage			3.3		V
Vin_{COM_P}	RX1, RX2 AC peak common-mode voltage	Measured at Rx pins with termination enabled			150	mVP
Z_{CM_RX}	DC common-mode impedance		18	26	30	Ω
Z_{diff_RX}	DC differential input impedance		72	80	120	Ω
$Z_{RX\_High\_IMP+}$	DC Input high impedance	Device in sleep mode Rx termination not powered measured with respect to GND over 500 mV maximum	50	85		kΩ
$V_{RX-LFPS-DETpp}$	Low frequency periodic signaling (LFPS) detect threshold	Measured at receiver pin, below minimum output is squelched, above max input signal is passed to output	100		300	mVpp
$RL_{RX-DIFF}$	Differential return loss	50 MHz – 1.25 GHz	10	11		dB
		1.25 GH – 2.5 GHz	6	7		
RL_{RX-CM}	Common-mode return loss	50 MHz – 2.5 GHz	11	13		dB
TRANSMITTER AC/DC						
$V_{TXDIFF\_TB\_P-P}$	Differential peak-to-peak output voltage (VID = 800, 1200 mVpp, 5 Gbps)	R_L = 100 Ω ±1%, DEx, OSx = NC, **Transition Bit**	900	1241	1500	mV
		R_L = 100 Ω ±1%, DEx = NC, OSx = GND **Transition Bit**		1105		
		R_L = 100 Ω ±1%, DEx = NC, OSx = VCC **Transition Bit**		1324		
$V_{TXDIFF\_NTB\_P-P}$		R_L = 100 Ω ±1%, DEx=NC, OSx = 0,1,NC **Non-Transition Bit**		1241		mV
		R_L = 100 Ω ±1%, DEx=0 OSx = 0,1,NC **Non-Transition Bit**		866		
		R_L = 100 Ω ±1%, DEx=1 OSx = 0,1,NC **Non-Transition Bit**		691		
DE	De-emphasis level OS1,2 = NC (for OS1, 2 = 1 and 0 see Table 4)	DE1/DE2 = NC		0		dB
		DE1/DE2 = 0		–3		
		DE1/DE2 = 1		–5		
T_{DE}	De-emphasis width			0.85		UI
Z_{diff_TX}	DC differential impedance		72	90	120	Ω
Z_{CM_TX}	DC common-mode impedance	Measured w.r.t to AC ground over 0 mV to 500 mV	18	23	30	Ω
RL_{diff_TX}	Differential return loss	f = 50 MHz – 1.25 GHz	9	10		dB
		f = 1.25 GHz – 2.5 GHz	6	7		
RL_{CM_TX}	Common-mode return loss	f = 50 MHz – 2.5 GHz	11	12		dB

(1) The maximum rating is simulated under 3.6-V VCC.

Electrical Characteristics (continued)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{TX_SC}	TX short circuit current	TX± shorted to GND			60	mA
$V_{TX\_CM\_DC}$	Transmitter DC common-mode voltage	OSx = NC	2	2.6	3	V
$V_{TX\_CM\_AC\_Active}$	TX AC common-mode voltage active			30	100	mVpp
$VT_{X\_idle\_diff-AC-pp}$	Electrical idle differential peak to peak output voltage	HPF to remove DC	0		10	mVpp
$V_{TX\_CM\_DeltaU1-U0}$	Absolute delta of DC CM voltage during active and idle states			35	200	mV
$V_{TX\_idle\_diff-DC}$	DC Electrical idle differential output voltage	Voltage must be lowpass filtered to remove any AC component	0		10	mV
V_{detect}	Voltage change to allow receiver detect	Positive voltage to sense receiver termination			600	mV
C_{TX}	Tx input capacitance to GND	At 2.5 GHz		1.25		pF

6.6 Timing Requirements

			MIN	NOM	MAX	UNIT
t_R, t_F	Output rise and fall time	20% to 80% of differential voltage measured 1 inch from the output pin	30	65		ps
t_{RF_MM}	Output rise and fall time mismatch	20% to 80% of differential voltage measured 1 inch from the output pin		1.5	20	ps
T_{diff_LH}, T_{diff_HL}	Differential propagation delay	De-Emphasis = –3.5 dB (CH 0 and CH 1). Propagation delay between 50% level at input and output		305	370	ps
$t_{idleEntry}$, $t_{idleExit}$	Idle entry and exit times	See Figure 2		4	6	ns

6.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

			MIN	TYP	MAX	UNIT
T_{TX-EYE} (1) (2)	Total jitter (Tj) at point A	Device setting: OS1 = L, DE1 = –6 dB, EQ1 = 7 dB		0.23	0.5	UI(3)pp
DJ_{TX} (2)	Deterministic jitter (Dj)			0.14	0.3	
RJ_{TX} (2) (4)	Random jitter (Rj)			0.08	0.2	
T_{TX-EYE} (1) (2)	Total jitter (Tj) at point B	Device setting: OS2 = H, DE2 = –6 dB, EQ2 = 7 dB		0.15	0.5	UI(3)Pp
DJ_{TX} (2)	Deterministic jitter (Dj)			0.07	0.3	
RJ_{TX} (2) (4)	Random jitter (Rj)			0.08	0.2	

(1) Includes RJ at 10^{-12} BER
(2) Determininstic jitter measured with K28.5 pattern, Random jitter measured with K28.5 pattern at the ends of reference channel, VID = 1000 mVpp, 5 Gbps, –3.5-dB DE from source
(3) UI = 200 ps
(4) Rj calculated as 14.069 times the RMS random jitter for 10^{-12} BER

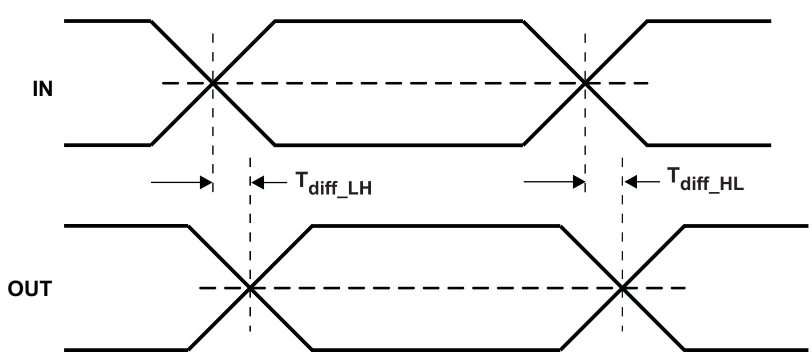


Figure 1. Propagation Delay

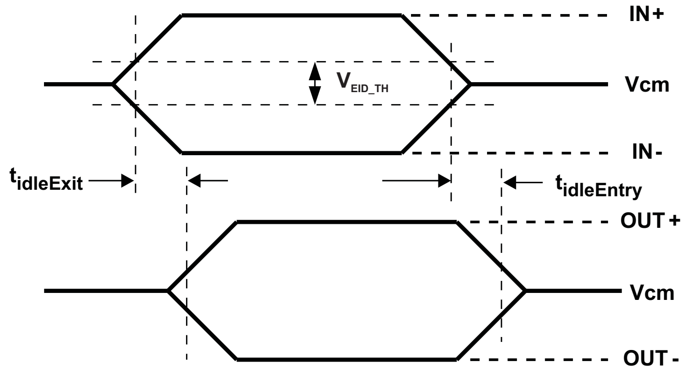


Figure 2. Electrical Idle Mode Exit and Entry Delay

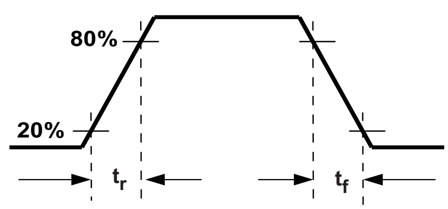


Figure 3. Output Rise and Fall Times

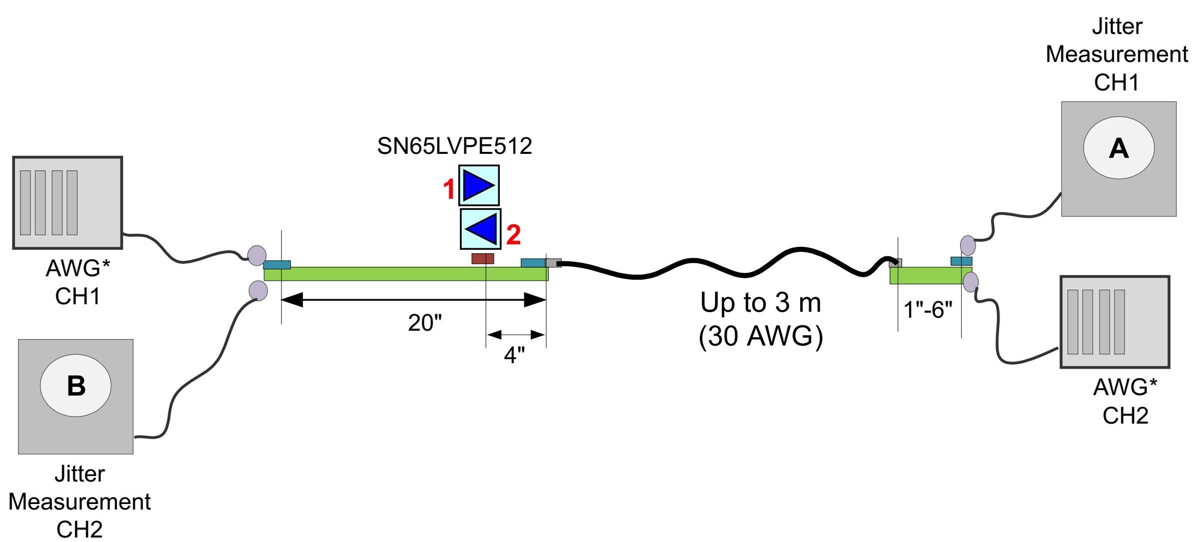


Figure 4. Jitter Measurement Setup

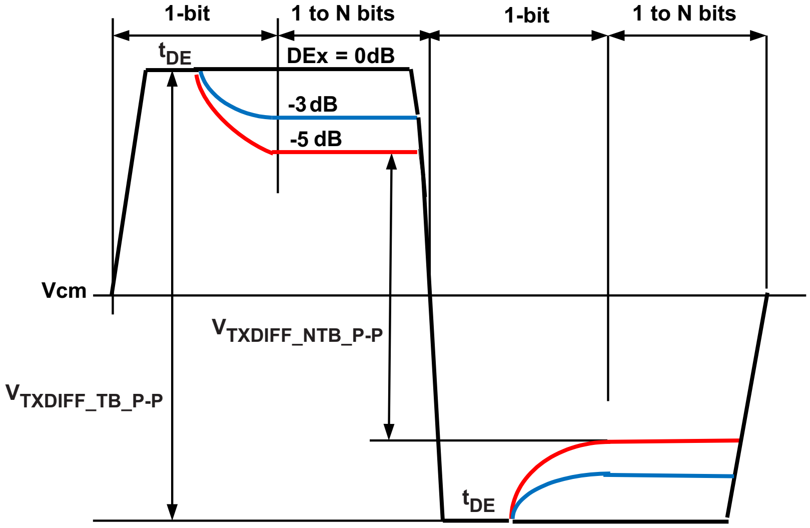


Figure 5. Output De-Emphasis Levels OSx = NC

6.8 Typical Characteristics

Table 1. Case I Fixed Output and Variable Input Trace

GRAPH TITLE	FIGURE NUMBER
DE = 0 dB, EQ = 0 dB, Input = 4 inches, Output = 4 inches + 3-m Cable	Figure 6
DE = 0 dB, EQ = 0 dB, Input = 8 inches, Output = 4 inches + 3-m Cable	Figure 7
DE = 0 dB, EQ = 0 dB, Input = 12 inches, Output = 4 inches + 3-m Cable	Figure 9
DE = 0 dB, EQ = 0 dB, Input = 16 inches, Output = 4 inches + 3-m Cable	Figure 9
DE = 0 dB, EQ = 0 dB, Input = 20 inches, Output = 4 inches + 3-m Cable	Figure 10
DE = 0 dB, EQ = 7 dB, Input = 24 inches, Output = 4 inches + 3-m Cable	Figure 11
DE = 0 dB, EQ = 7 dB, Input = 32 inches, Output = 4 inches + 3-m Cable	Figure 12
DE = 0 dB, EQ = 7 dB, Input = 36 inches, Output = 4 inches + 3-m Cable	Figure 13
DE = 0 dB, EQ = 15 dB, Input = 36 inches, Output = 4 inches + 3-m Cable	Figure 14
DE = 0 dB, EQ = 15 dB, Input = 48 inches, Output = 4 inches + 3-m Cable	Figure 15

Table 2. Case II Fixed Input and Variable Output Trace+ 3m Cable

GRAPH TITLE	FIGURE NUMBER
DE = 0 dB, EQ = 7 dB, Input = 12 inches, Output = 4 inches + 3-m Cable	Figure 16
DE = 0 dB, EQ = 7 dB, Input = 12 inches, Output = 8 inches + 3-m Cable	Figure 17
DE = 0 dB, EQ = 7 dB, Input = 12 inches, Output = 12 inches + 3-m Cable	Figure 18
DE = 0 dB, EQ = 7 dB, Input = 12 inches, Output = 16 inches + 3-m Cable	Figure 19
DE = 0 dB, EQ = 7 dB, Input = 12 inches, Output = 20 inches + 3-m Cable	Figure 20

Table 3. Case III Fixed Input and Variable Output Trace (No Cable)

GRAPH TITLE	FIGURE NUMBER
DE = 0 dB, EQ = 7 dB, Input = 12 Inches, Output = 8 Inches	Figure 21
DE = 0 dB, EQ = 7 dB, Input = 12 Inches, Output = 32 Inches	Figure 22
DE = 0 dB, EQ = 7 dB, Input = 12 Inches, Output = 36 Inches	Figure 23
DE = –3 dB, EQ = 7 dB, Input = 12 Inches, Output = 36 Inches	Figure 24
DE = –5 dB, EQ = 7 dB, Input = 12 Inches, Output = 40 Inches	Figure 25
DE = –5 dB, EQ = 7 dB, Input = 12 Inches, Output = 44 Inches	Figure 26

6.8.1 Case I Fixed Output and Variable Input Trace

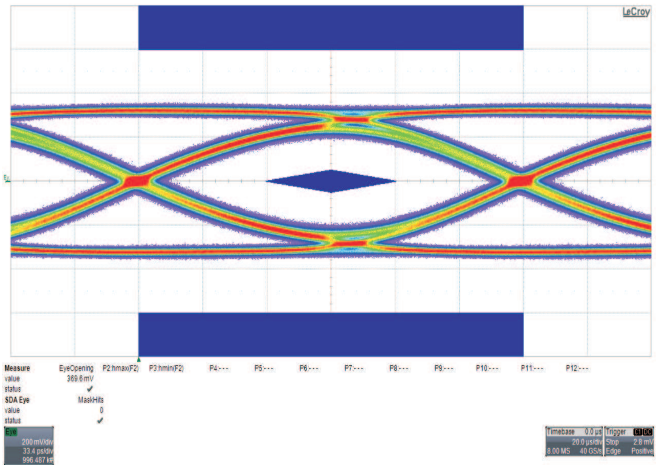


Figure 6. DE = 0 dB, EQ = 0 dB, Input = 4 inches, Output = 4 inches + 3-m Cable

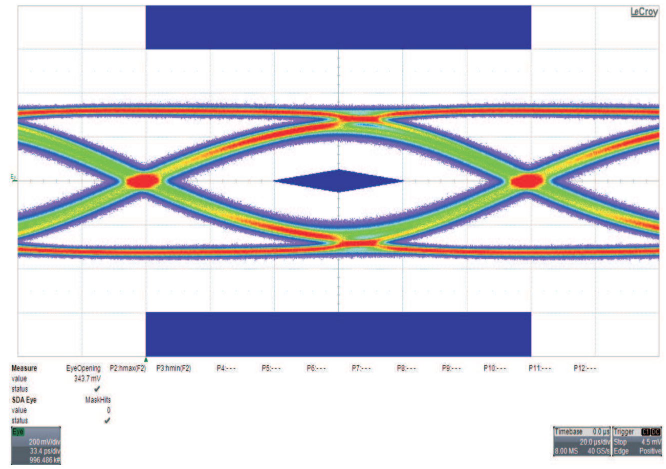


Figure 7. DE = 0 dB, EQ = 0 dB, Input = 8 inches, Output = 4 inches + 3-m Cable

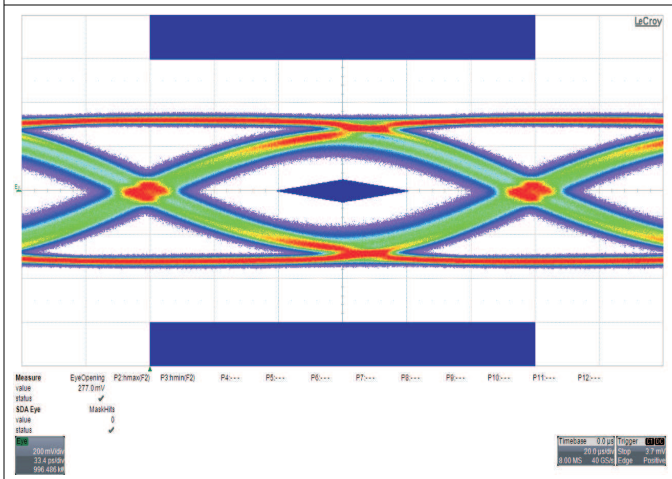


Figure 8. DE = 0 dB, EQ = 0 dB, Input = 12 inches, Output = 4 inches + 3-m Cable

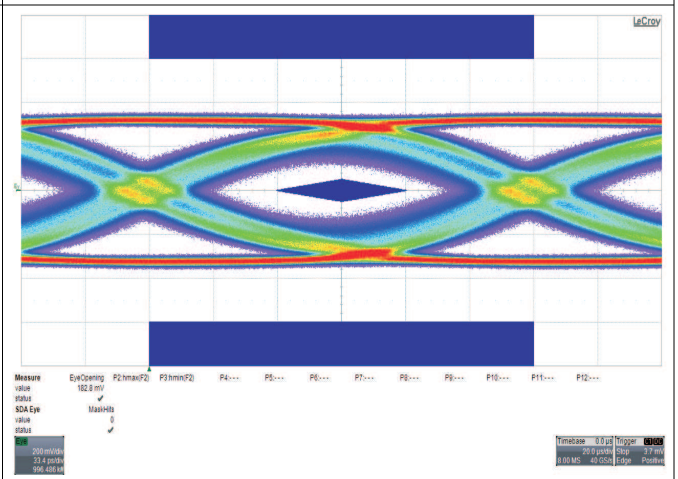


Figure 9. DE = 0 dB, EQ = 0 dB, Input = 16 inches, Output = 4 inches + 3-m Cable

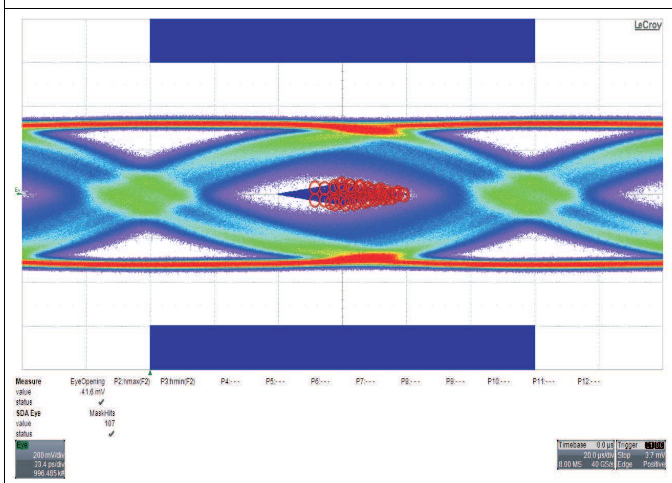


Figure 10. DE = 0 dB, EQ = 0 dB, Input = 20 inches, Output = 4 inches + 3-m Cable

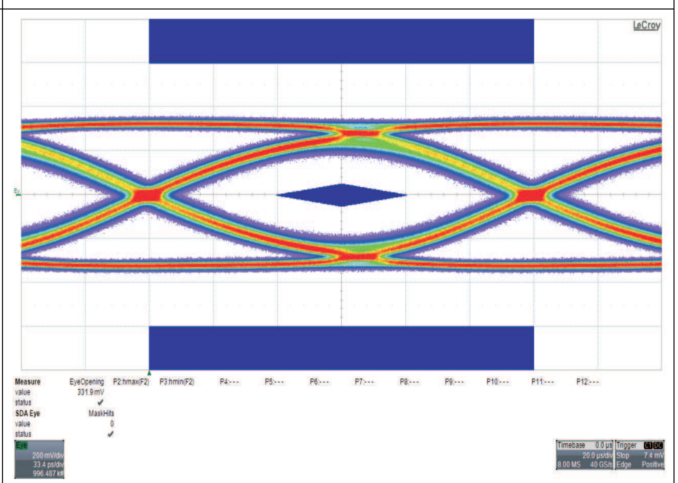


Figure 11. DE = 0 dB, EQ = 7 dB, Input = 24 inches, Output = 4 inches + 3-m Cable

Case I Fixed Output and Variable Input Trace (continued)

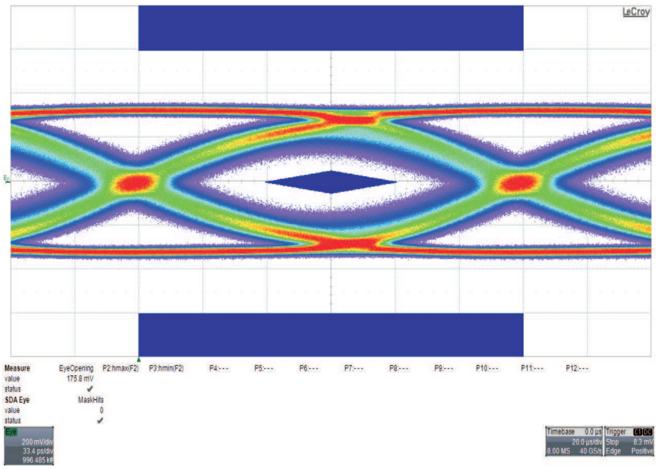


Figure 12. DE = 0 dB, EQ = 7 dB, Input = 32 inches, Output = 4 inches + 3-m Cable

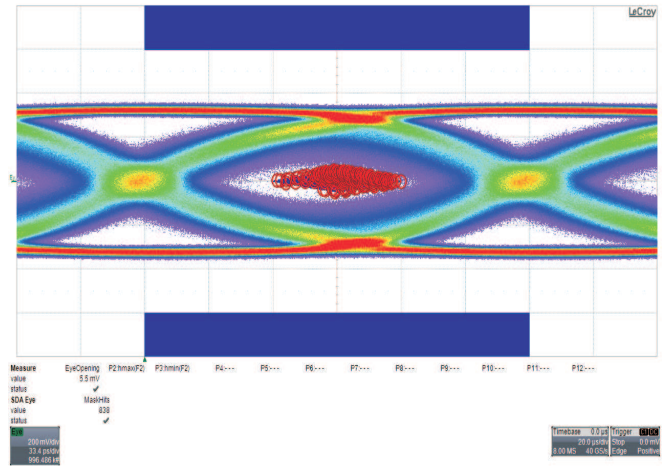


Figure 13. DE = 0 dB, EQ = 7 dB, Input = 36 inches, Output = 4 inches + 3-m Cable

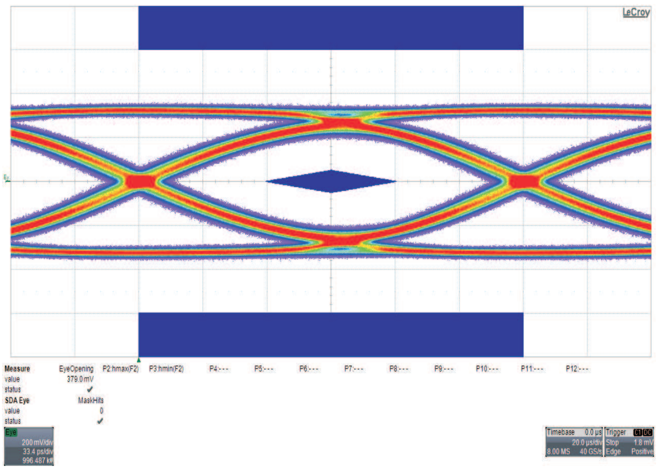


Figure 14. DE = 0 dB, EQ = 15 dB, Input = 36 inches, Output = 4 inches + 3-m Cable

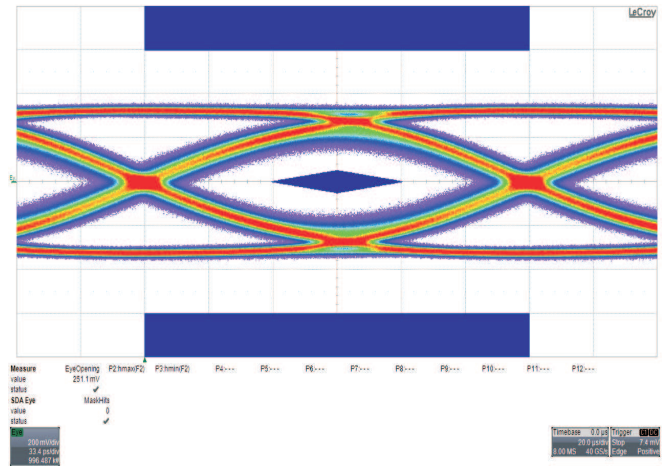


Figure 15. DE = 0 dB, EQ = 15 dB, Input = 48 inches, Output = 4 inches + 3-m Cable

6.8.2 Case II Fixed Input and Variable Output Trace+ 3-m Cable

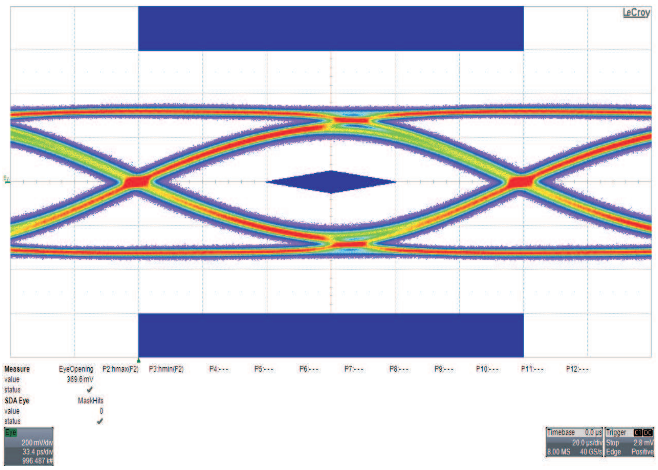


Figure 16. DE = 0 dB, EQ = 7 dB, Input = 12 inches, Output = 4 inches + 3-m Cable

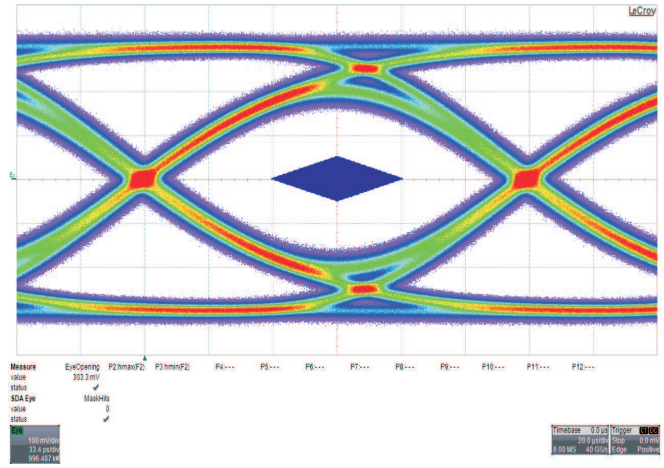


Figure 17. DE = 0 dB, EQ = 7 dB, Input = 12 inches, Output = 8 inches + 3-m Cable

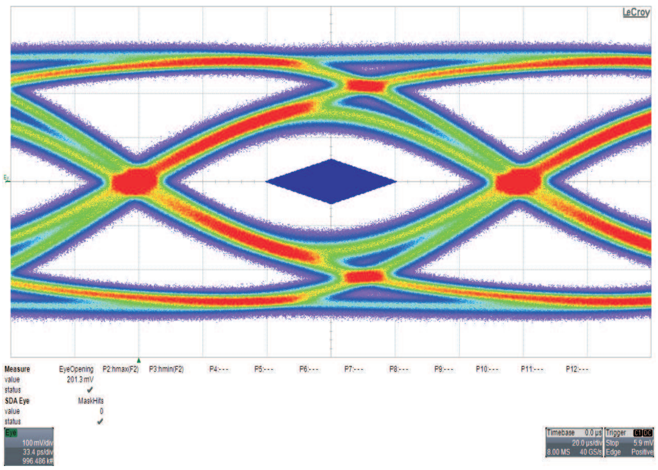


Figure 18. DE = 0 dB, EQ = 7 dB, Input = 12 inches, Output = 12 inches + 3-m Cable

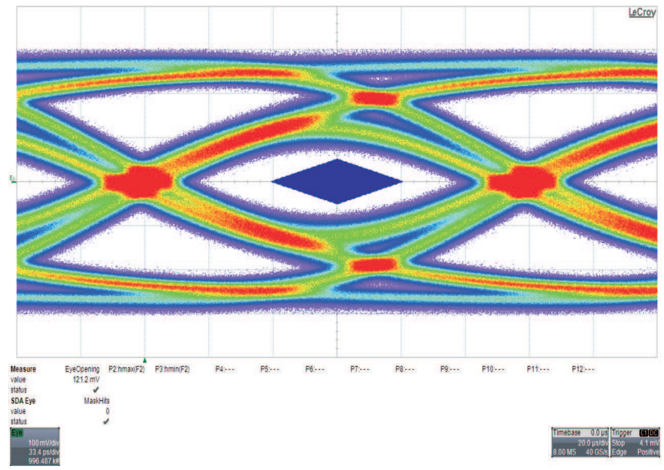


Figure 19. DE = 0 dB, EQ = 7 dB, Input = 12 inches, Output = 16 inches + 3-m Cable

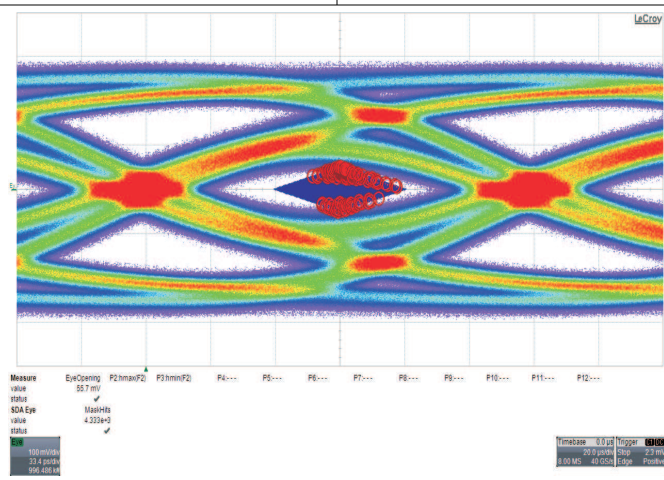


Figure 20. DE = 0 dB, EQ = 7 dB, Input = 12 inches, Output = 20 inches + 3-m Cable

6.8.3 Case III Fixed Input and Variable Output Trace (No Cable)

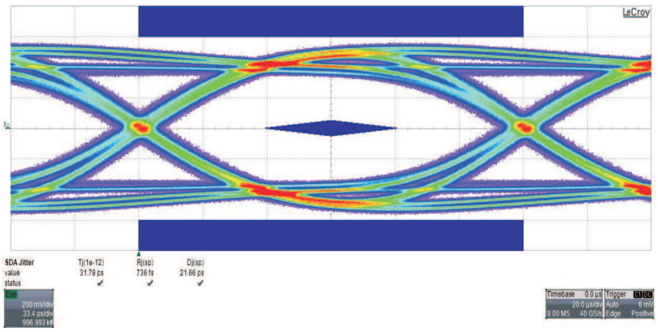


Figure 21. DE = 0 dB, EQ = 7 dB, Input = 12 Inches, Output = 8 Inches

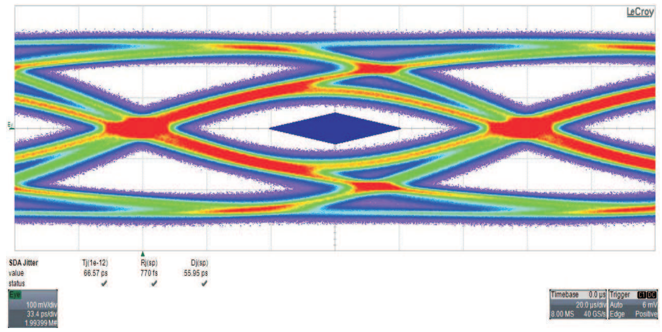


Figure 22. DE = 0 dB, EQ = 7 dB, Input = 12 Inches, Output = 32 Inches

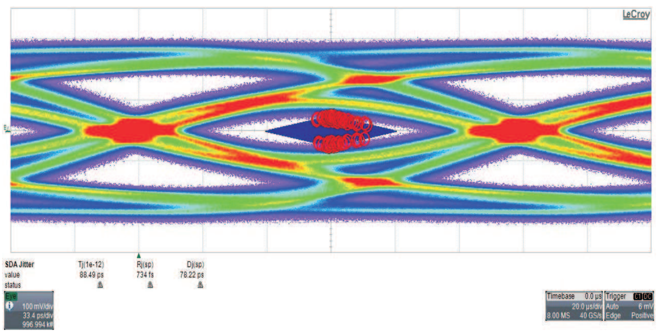


Figure 23. DE = 0 dB, EQ = 7 dB, Input = 12 Inches, Output = 36 Inches

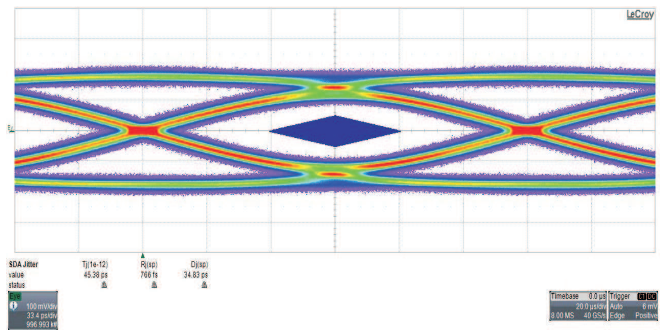


Figure 24. DE = –3 dB, EQ = 7 dB, Input = 12 Inches, Output = 36 Inches

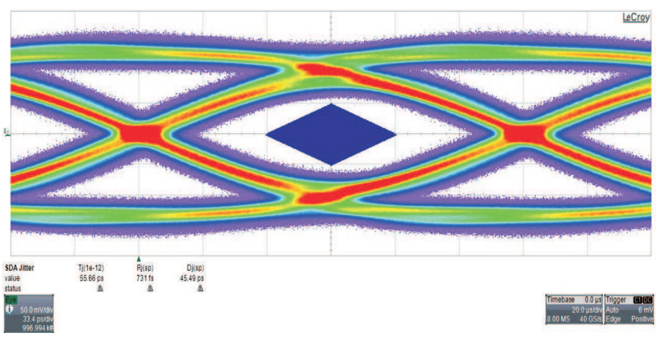


Figure 25. DE = –5 dB, EQ = 7 dB, Input = 12 Inches, Output = 40 Inches

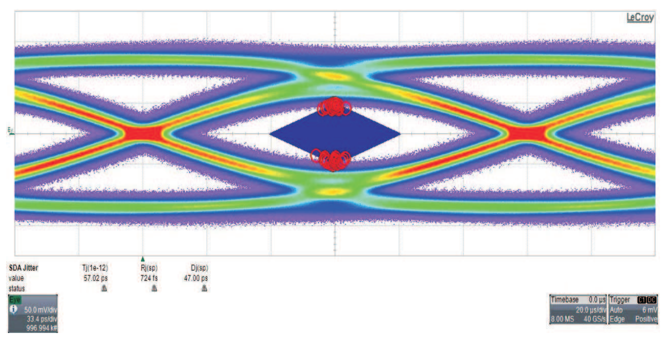


Figure 26. DE = –5 dB, EQ = 7 dB, Input = 12 Inches, Output = 44 Inches

7 Parameter Measurement Information

7.1 Typical Eye Diagram and Performance Curves

Measurement equipment details:

- Generator (source) LeCroy PERT3,
- Signal: 5 Gbps, 1000 mVp-p, 3.5-dB De-Emphasis
- TJ and DJ measurements based on CP0 (USB 3 compliance pattern) which is D0.0 or logical idle with SKP sequences removed
- RJ measurements based on CP1 or D10.2 symbol containing alternating 0s and 1s at Nyquist frequency
- Oscilloscope (Sink) LeCroy 25-GHz Real Time Oscilloscope
- LeCroy QualiPHY software used to measure jitter and collect compliance eye diagrams

Device Operating Conditions: VCC = 3.3 V, Temp = 25°C, EQx, DEx, OSx set to their default value when not mentioned

7.2 Plot 1 Fixed Output Trace +3-m USB 3 Cable With Variable Input Trace

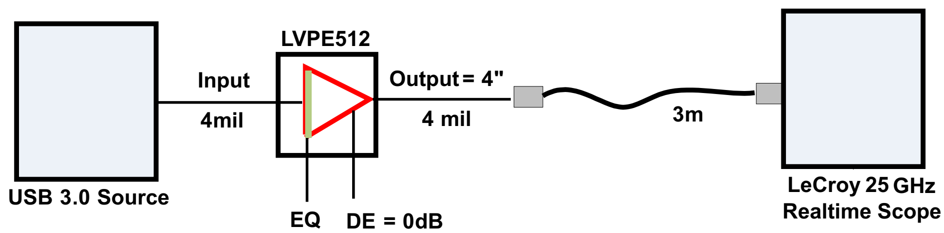


Figure 27. Parameter Measurement Set-Up

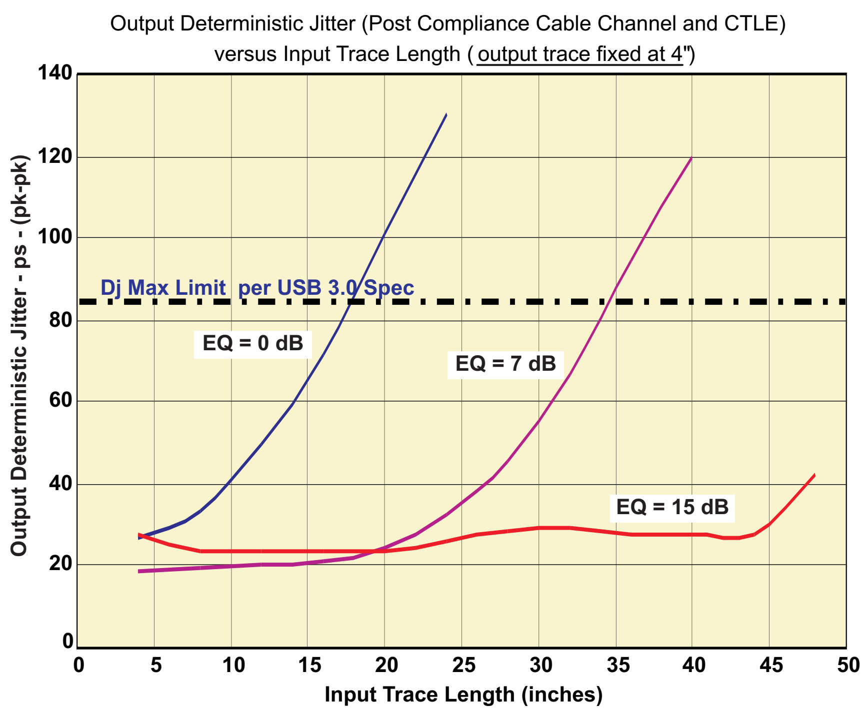


Figure 28. Output DJ vs Input Trace Length With Different EQ Settings

7.3 Plot 2 Fixed Input Trace With Variable Output Trace and +3-m USB 3.0 Cable

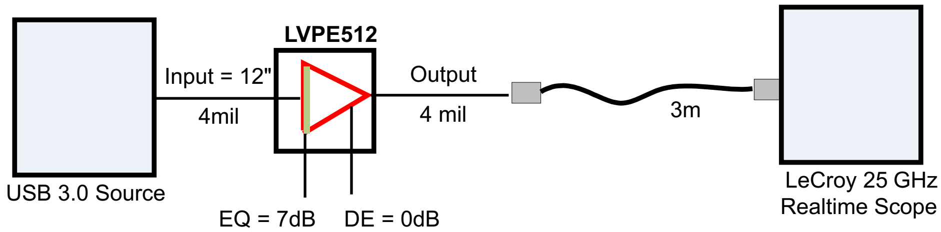


Figure 29. Parameter Measurement Set-Up

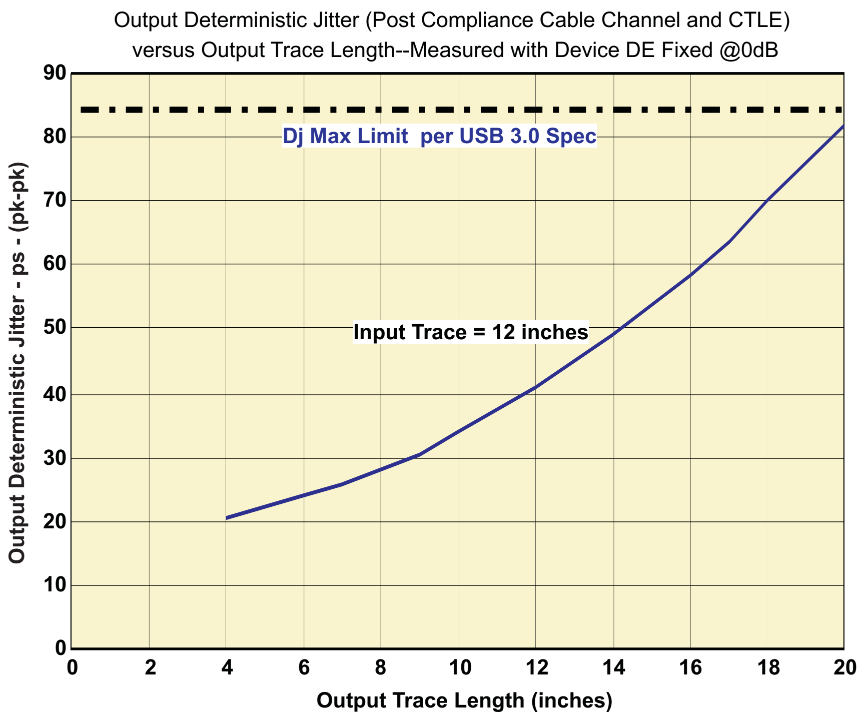


Figure 30. Output DJ

7.4 Plot 3 Fixed Input Trace With Variable Output Trace and (No Cable)

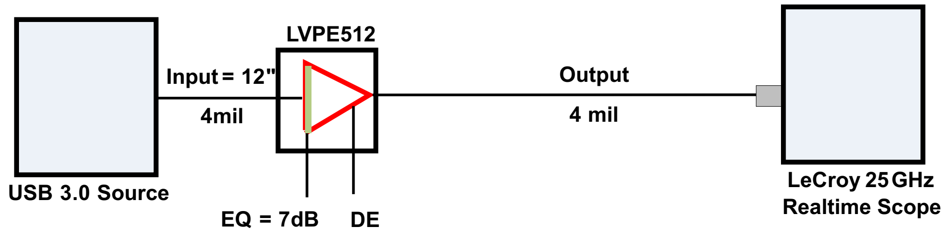


Figure 31. Parameter Measurement Set-Up

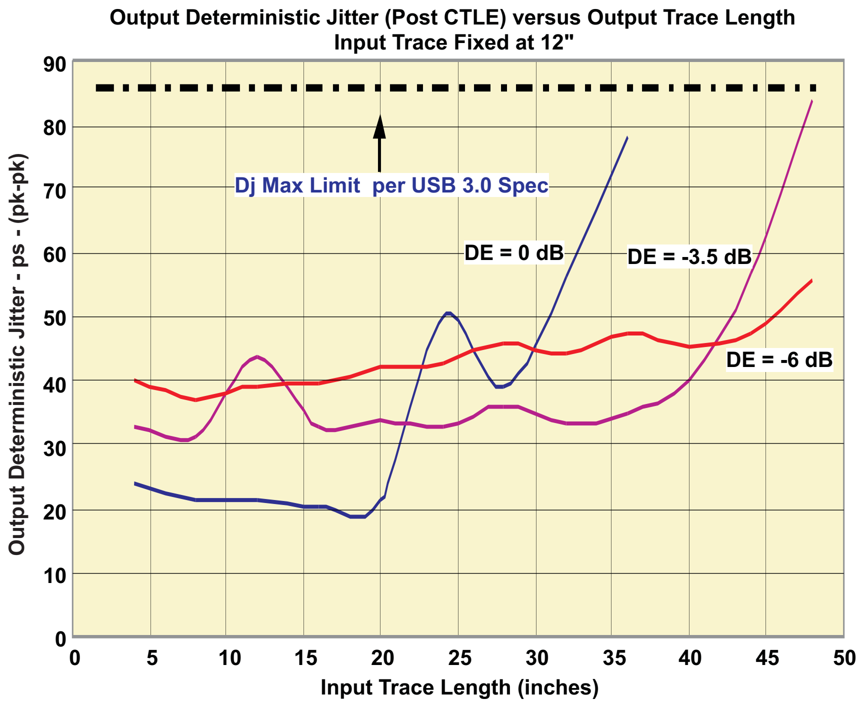


Figure 32. Output DJ vs Input Trace Length With Different EQ Settings

8 Detailed Description

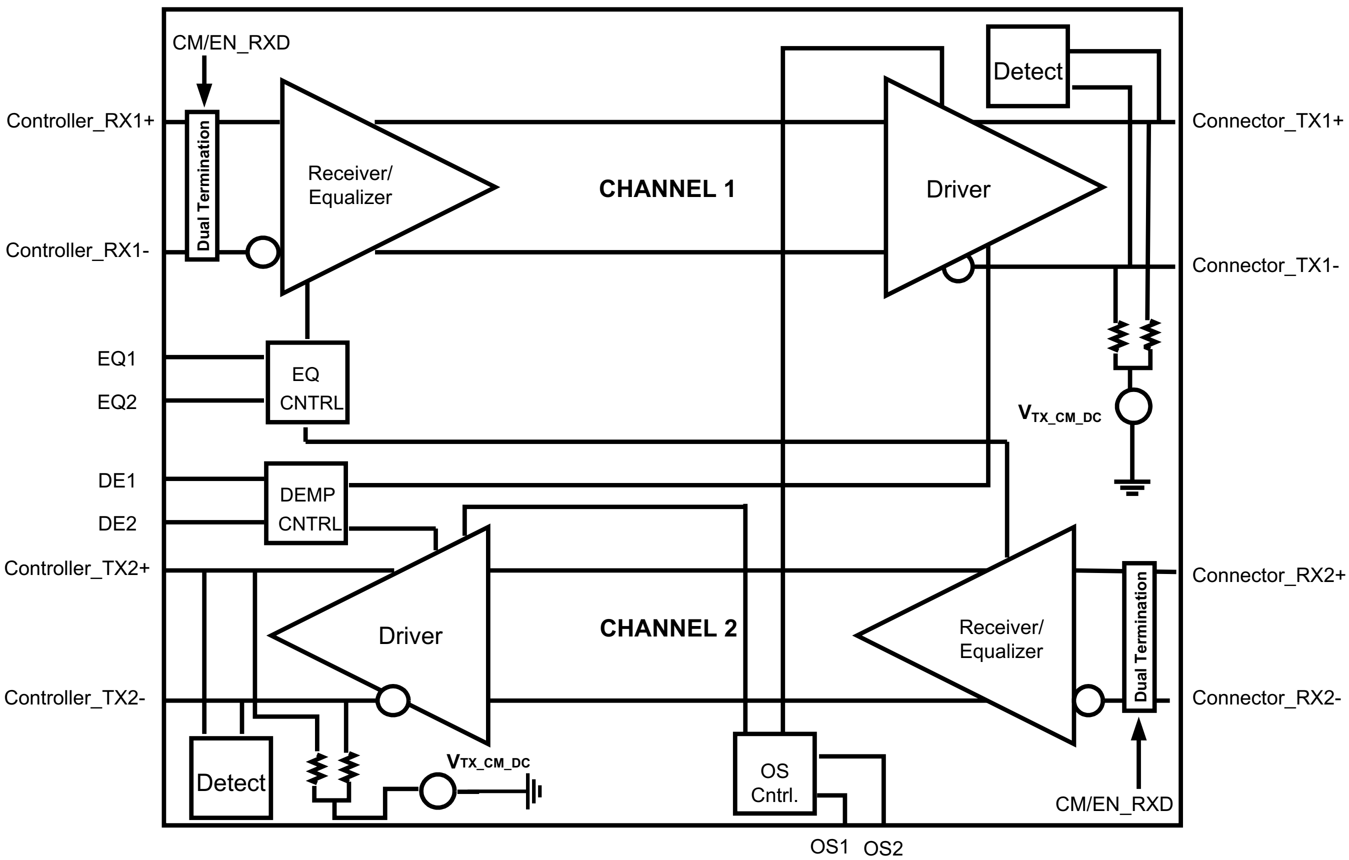
8.1 Overview

When 5-Gbps SuperSpeed USB signals travel across a PCB or cable, signal integrity degrades due to loss and inter-symbol interference. The SN65LVPE512 recovers incoming data by applying equalization that compensates for channel loss, and drives out signals with a high differential voltage. This extends the possible channel length, and enables systems to pass USB 3.0 compliance.

The SN65LVPE512 is located at the Host side, after power up, the SN65LVPE512 periodically performs receiver detection on the TX pair. If it detects a SuperSpeed USB receiver, the RX termination is enabled, and the SN65LVPE512 is ready to re-drive.

The receiver equalizer has three gain settings that are controlled by terminal EQ: 0 dB, 7 dB, and 15 dB. The equalization must be set based on amount of insertion loss in the channel before the SN65LVPE512. Likewise, the output driver supports configuration of De-Emphasis and Output Swing (terminals DE and OS).

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Controller- and Connector-Side Pins

The SN65LVPE512 features a link state machine that makes the device transparent on the USB 3.0 bus while minimizing power. The state machine relies on the system host or device controller to be connected to the pins named *Controller*. The pins labeled connector must be connected to the USB 3.0 receptacle or captive cable. Multiple SN65LVPE512 devices may be used in series.

Feature Description (continued)

8.3.2 Programmable EQ, De-Emphasis and Amplitude Swing

The SN65LVPE512 is designed to minimize signal degradation effects such as crosstalk and inter-symbol interference (ISI) that limits the interconnect distance between two devices. The input stage of each channel offers selectable equalization settings that can be programmed to match loss in the channel. The differential outputs provide selectable de-emphasis to compensate for the anticipated distortion USB 3.0 signal experiences. Level of de-emphasis depends on the length of interconnect and its characteristics. The SN65LVPE512 provides a unique way to tailor output de-emphasis on a per channel basis with use of DE and OS pins. All Rx and Tx equalization settings supported by the device are programmed by six 3-state pins as shown in Table 4.

8.3.3 Receiver Detection

8.3.3.1 At Power Up or Reset

After power-up or anytime EN_RXD is toggled, RX.Detect cycle is performed by first setting Rx termination for each channel to Hi-Z, device then starts sensing for receiver termination that may be attached at the other end of each TX.

If receiver is detected on both channel

- The TX and RX terminations are switched to Z_{DIFF_TX}, Z_{DIFF_RX} respectively.

If no receiver is detected on one or both channels

- The transmitter is pulled to Hi-Z
- The channel is put in low power mode
- Device attempts to detect Rx termination in 12-ms (typical) intervals until termination is found or device is put in sleep mode

8.3.3.2 During U2, U3 Link State

Rx detection is also performed periodically when link is in U2/U3 states. However in these states during Rx detection, input termination is not automatically disabled before performing Rx.Detect. If termination is found device goes back to its low power state if termination is not found then device disables its input termination and then jumps to power up the RX.Detect state.

8.3.4 Electrical Idle Support

Electrical idle support is needed for low frequency periodic signaling (LFPS) used in USB 3.0 side band communication. A link is in an electrical idle state when the TX± voltage is held at a steady constant value like the common-mode voltage. 'LVPE512 detects an electrical idle state when RX± voltage at the device pin falls below VRX_LFPS_DIFFp-p minimum. After detection of an idle state in a given channel the device asserts electrical idle state in its corresponding TX. When RX± voltage exceeds VRX_LFPS_DIFFp-p max normal operation is restored and output start passing input signal. Electrical idle exit and entry time is specified at < 6 ns.

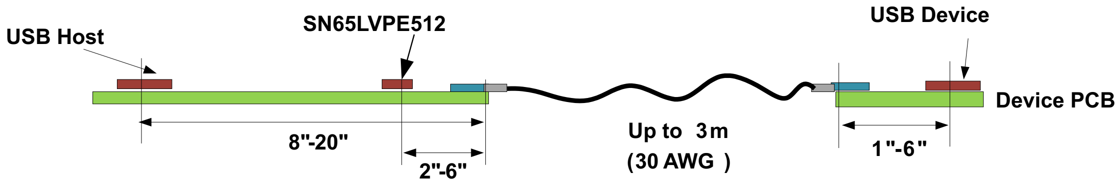
Feature Description (continued)

8.3.5 Signal Control Pin Setting

Table 4. Signal Control Pin Setting

OUTPUT SWING AND EQ CONTROL (at 2.5 GHz)			
OSx(1)	**TRANSISTION BIT AMPLITUDE (TYP mVpp)**	**EQx(1)**	**EQUALIZATION (dB)**
NC (default)	1241	NC (default)	0
0	1105	0	7
1	1324	1	15
OUTPUT DE CONTROL (at 2.5 GHz)			
DEx(1)	**OSx(1) = NC**	**OSx(1) = 0**	**OSx(1) = 1**
NC (default)	0 dB	0 dB	0 dB
0	–3 dB	–2 dB	–4 dB
1	–5 dB	–4 dB	–5.6 dB
CONTROL PINS SETTINGS			
EN_RXD	**DEVICE FUNCTION**		
1 (default)	Normal Operation		
0	Sleep Mode		

(1) Where x = Channel 1 or Channel 2



NOTE: For more detailed placement example of redriver, see *Parameter Measurement Information*.

Figure 33. Redriver Placement Example

8.4 Device Functional Modes

8.4.1 Low Power Modes

Device supports three low power modes as described:

- **Sleep Mode**
  Initiated anytime EN_RXD undergoes a high to low transition and stays low or when device powers up with EN_RXD set low. In sleep mode both input and output terminations are held at HiZ and device ceases operation to conserve power. Sleep mode maximum power consumption is 1 mW, entry time is 2 µs, device exits sleep mode to Rx.Detect mode after EN_RXD is driven to V_{CC}, exit time is 100 µs maximum.
- **RX Detect Mode -- When no remote device is connected**
  Anytime 'LVPE512 detects a break in link (that is, when upstream device is disconnected) or after power up fails to find a remote device, 'LVPE512 goes to Rx Detect mode and conserves power by shutting down majority of its internal circuitry. In this mode, input termination for both channels are driven to Hi-Z. In Rx Detect mode device power is < 10 mW (typical) or less than 5% of its normal operating power. This feature is very useful in saving system power in mobile applications like notebook PC where battery life is critical.

  Anytime an upstream device gets reconnected the redriver automatically senses the connection and goes to normal operating mode. This operation requires no setting to the device.
- **U2/U3 Mode**
  With the help of internal timers the device tracks when link enters USB 3.0 low power modes U2 and U3; in these modes link is in electrical idle state. 'LVPE512 selectively turns off internal circuitry to save on power. Typical power saving is about 75% lower than normal operating mode. The device automatically reverts to active mode when signal activity (LFPS) is detected.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

One example of the SN65LVPE512 used in a Host application on transmit and receive channels is shown in *Typical Application*. The redriver is needed on the PCB path to pass transmitter compliance due to loss between the Host and connector. The redriver uses its equalization to recover the insertion loss and re-drive the signal with boosted swing down the remaining channel, through the USB 3.0 cable, and into the device PCB. Additionally on the receiver path, the SN65LVPE512 compensated for the Host to pass receiver jitter tolerance. The redriver recovers the loss from the Device PCB, connector, and USB 3.0 cable and re-drives the signal going into the Host receiver. The equalization, output swing, and de-emphasis settings are dependent upon the type of USB 3.0 signal path and end application.

9.2 Typical Application

The SN65LVPE512 is placed in the Host side and connected to a USB3 Type-A connector. The EQ and DE terminals must be pulled up, pulled down, or left floating depending on the amount of equalization or de-emphasis that is desired. The OS terminal must be pulled down or left floating depending on the required output swing. This device has terminals to be exclusively connected to the Host and to the Device accordingly.

In this Host side, even though the RX and TX pairs must be AC-coupled because this is an embedded implementation) and Figure 35 only show the AC-coupling caps on the TX pair only to follow the convention.

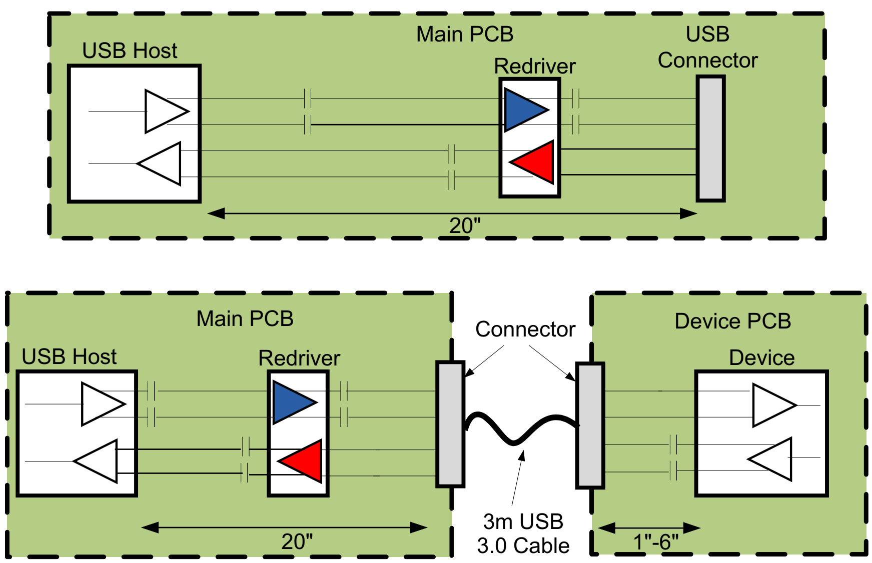


Figure 34. Typical Application Diagram

Typical Application (continued)

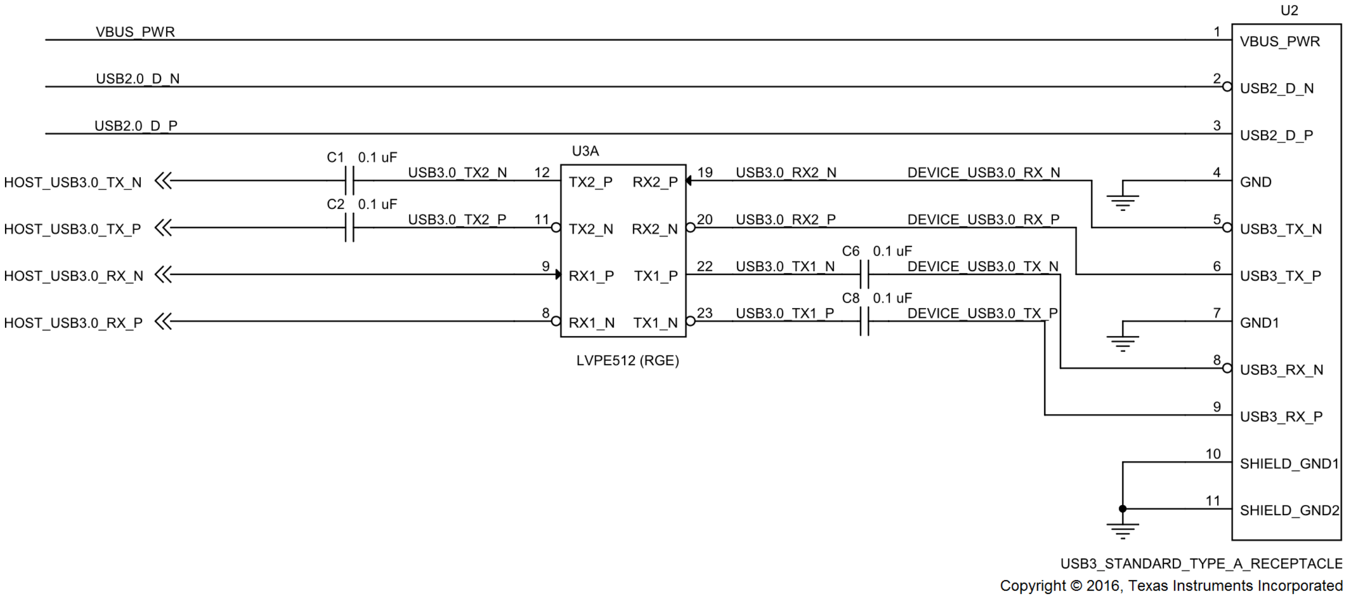


Figure 35. Typical Application With Embedded Host and USB3.0 Device Connector

9.2.1 Design Requirements

Table 5 lists the parameters for this example.

Table 5. Design Parameters

PARAMETER	EXAMPLE VALUE
Input voltage range	100 mV to 1200 mV
Output voltage range	1050 mV to 1200 mV
Equalization	0, 7, 15 dB (2.5 Gbps)
De-Emphasis	0, –3, –5 dB (OS Floating)
VCC	3.3-V nominal supply

9.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Equalization (EQ) setting
- De-Emphasis (DE) setting
- Output Swing Amplitude (OS) setting

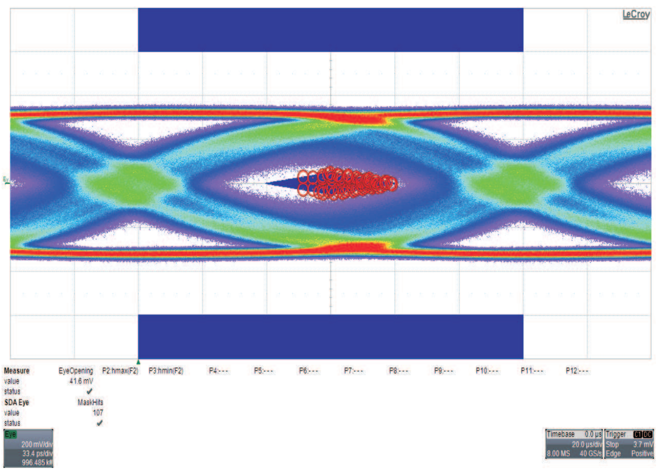
The equalization must be set based on the insertion loss in the pre-channel (channel before the SN65LVPE512 device). The input voltage to the device is able to have a large range because of the receiver sensitivity and the available EQ settings. The EQ terminal can be pulled high through a resistor to VCC, low through a resistor to ground, or left floating.

The De-emphasis setting must be set based on the length and characteristics of the post channel (channel after the SN65LVPE512 device). Output de-emphasis can be tailored using the DE terminal. This terminal must be pulled high through a resistor to VCC, low through a resistor to ground, or left floating.

The output swing setting can also be configured based on the amplitude needed to pass the compliance test. This setting is also based on the length of interconnect or cable the SN65LVPE512 is driving. This terminal must be pulled low through a resistor to ground or left floating.

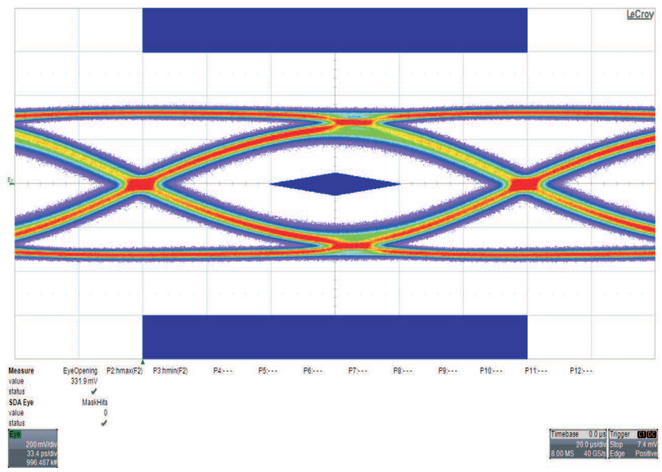
9.2.3 Application Curves

The following plots show the input and output of this typical implementation based on an embedded redriver with a USB 3.0 Type A connector and a Std. USB3.0 3-m long cable.



DE = 0 dB EQ = 0 dB Pre-channel = 20”
Post-channel = 4” + 3m cable

Figure 36. Eye-Mask Measured at the Device End With No Equalization



DE = 0 dB EQ = 0 dB Pre-channel = 20”
Post-channel = 4” + 3m cable

Figure 37. Eye-Mask Measured at the Device End With 7-dB Equalization

10 Power Supply Recommendations

The SN65LVPE512 is designed to operate from a single 3.3-V supply.

11 Layout

11.1 Layout Guidelines

- The 100-nF capacitors on the TXP and SSTXN nets must be placed close to the USB connector (Type A, Type B, and so forth).
- The ESD and EMI protection devices (if used) must also be placed as close as possible to the USB connector.
- Place voltage regulators as far away as possible from the differential pairs.
- In general, the large bulk capacitors associated with each power rail must be placed as close as possible to the voltage regulators.
- TI recommends that small decoupling capacitors for the 1.8-V power rail be placed close to the TUSB551 as shown below.
- The SuperSpeed differential pair traces for RXP/N and TXP/N must be designed with a characteristic impedance of 90 Ω ±10%. The PCB stack-up and materials determine the width and spacing needed for a characteristic impedance of 90 Ω.
- The SuperSpeed differential pair traces must be routed parallel to each other as much as possible. TI recommends the traces be symmetrical.
- In order to minimize crosstalk, TI recommends keeping high-speed signals away from each other. Each pair must be separated by at least 5 times the signal trace width. Separating with ground also helps minimize crosstalk.
- Route all differential pairs on the same layer adjacent to a solid ground plane.
- Do not route differential pairs over any plane split.
- Adding test points causes impedance discontinuity and therefore negatively impacts signal performance. If test points are used, they must be placed in series and symmetrically. They must not be placed in a manner

Layout Guidelines (continued)

that causes stub on the differential pair.

- Avoid 90 degree turns in traces. The use of bends in differential traces must be kept to a minimum. When bends are used, the number of left and right bends must be as equal as possible and the angle of the bend must be ≥ 135 degrees. This minimizes any length mismatch caused by the bends and therefore minimize the impact bends have on EMI.
- Match the etch lengths of the differential pair traces. There must be less than 5-mils difference between a SS differential pair signal and its complement. The USB 2.0 differential pairs must not exceed 50-mils relative trace length difference.
- The etch lengths of the differential pair groups do not need to match (that is, the length of the RXP/N pair to that of the TXP/N pair), but all trace lengths must be minimized.
- Minimize the use of vias in the differential pair paths as much as possible. If this is not practical, make sure that the same via type and placement are used for both signals in a pair. Any vias used must be placed as close as possible to the TUSB551 device.
- To ease routing, the polarity of the SS differential pairs can be swapped. This means that TXP can be routed to TXN or RXN can be routed to RXP.
- Do not place power fuses across the differential pair traces.

11.2 Layout Example

SN65LVPE512 USB3.0 signals routing with embedded Host and Std. Type A connector

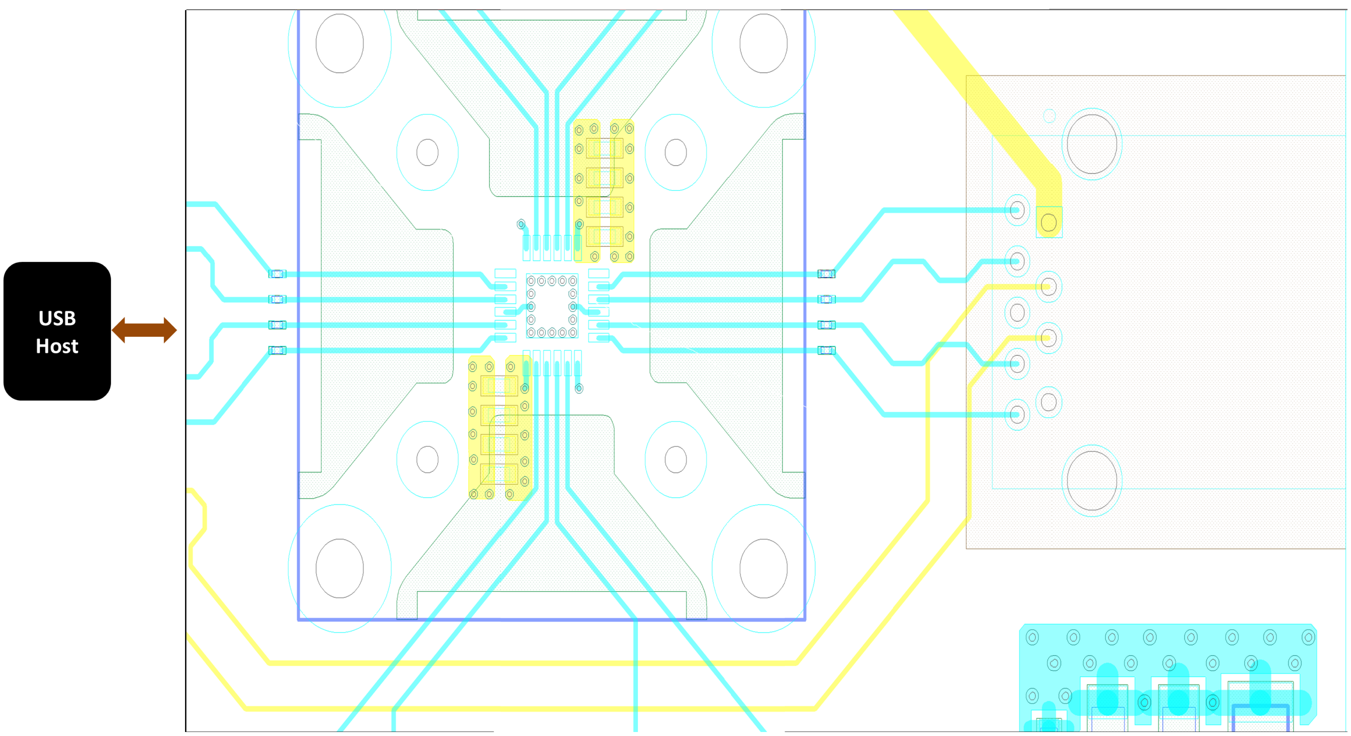


Figure 38. SN65LVPE512 USB3.0 Signals Routing With Embedded Host and Std. Type A Connector

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65LVPE512RGER	NRND	VQFN	RGE	24	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVPE 512	
SN65LVPE512RMQR	NRND	WQFN	RMQ	24	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SN512	

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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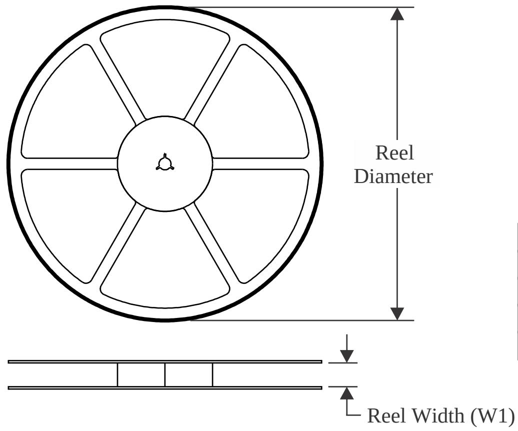
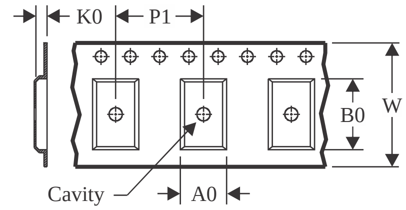
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

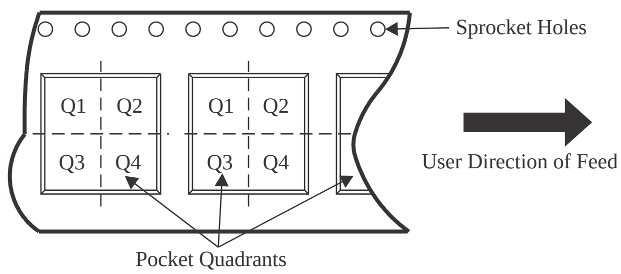


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

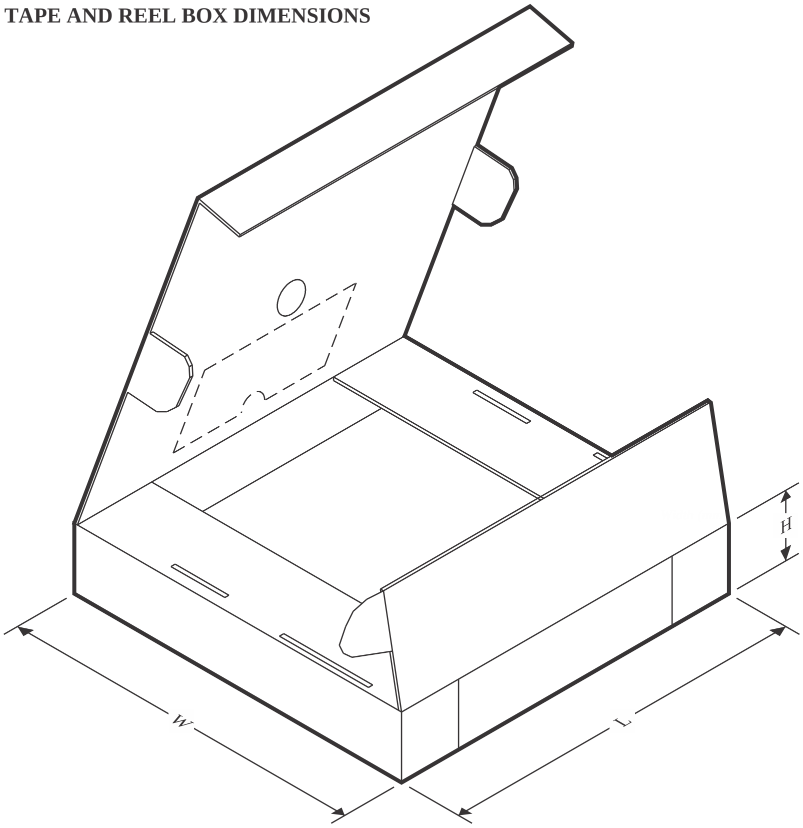
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

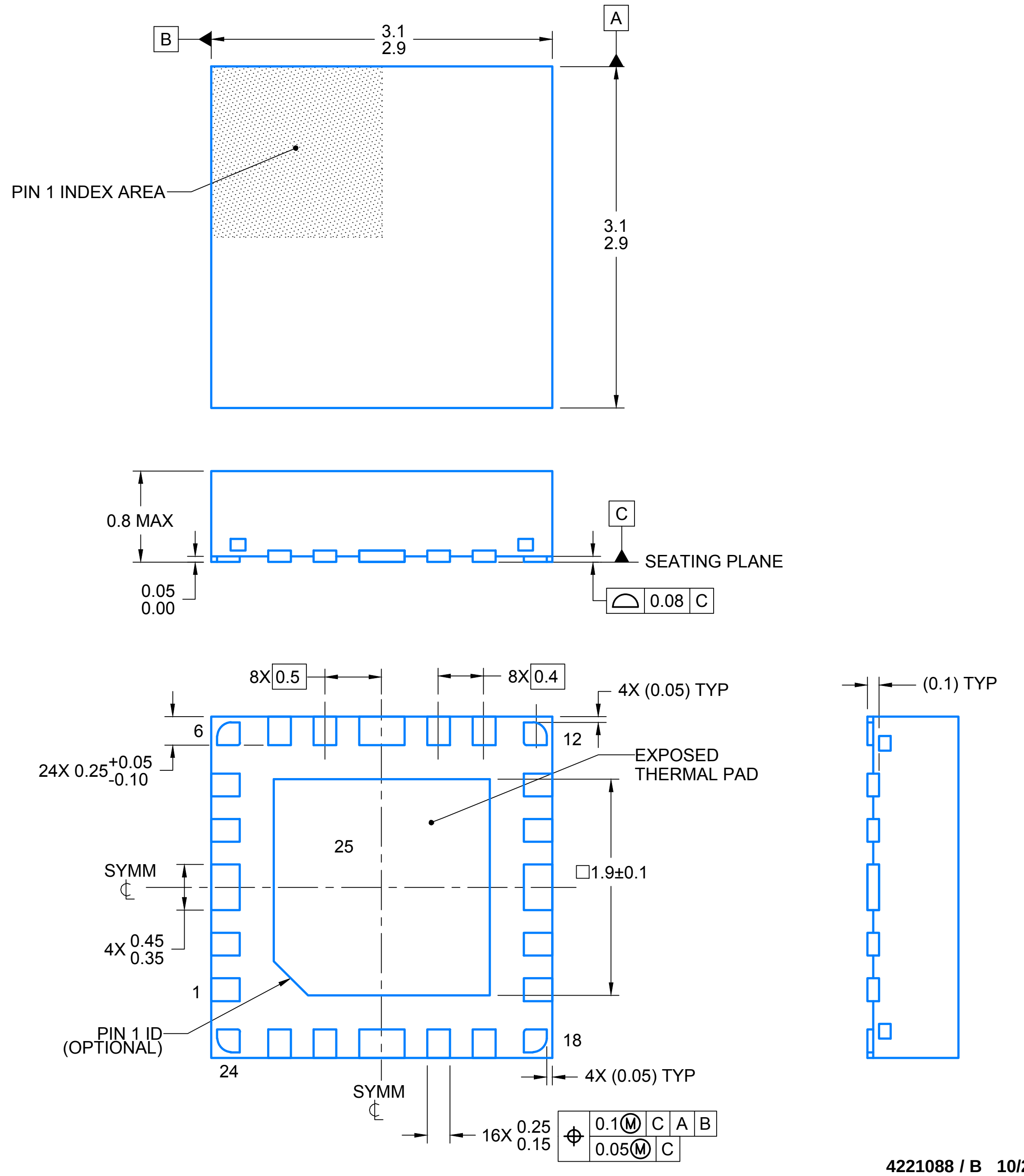
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVPE512RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
SN65LVPE512RMQR	WQFN	RMQ	24	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LVPE512RGER	VQFN	RGE	24	3000	356.0	356.0	35.0
SN65LVPE512RMQR	WQFN	RMQ	24	3000	367.0	367.0	35.0



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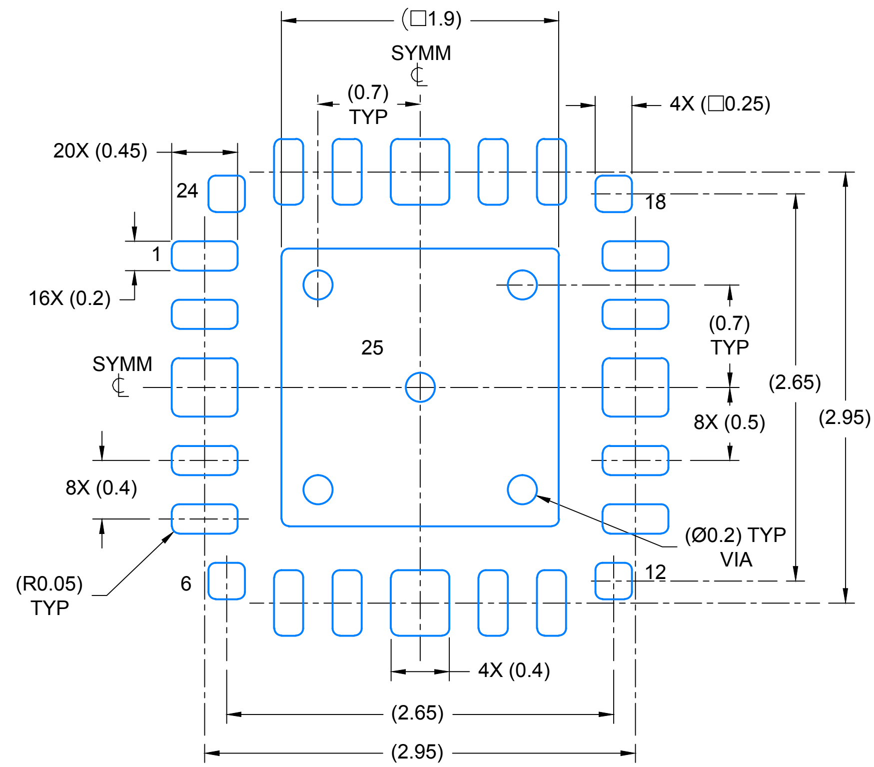
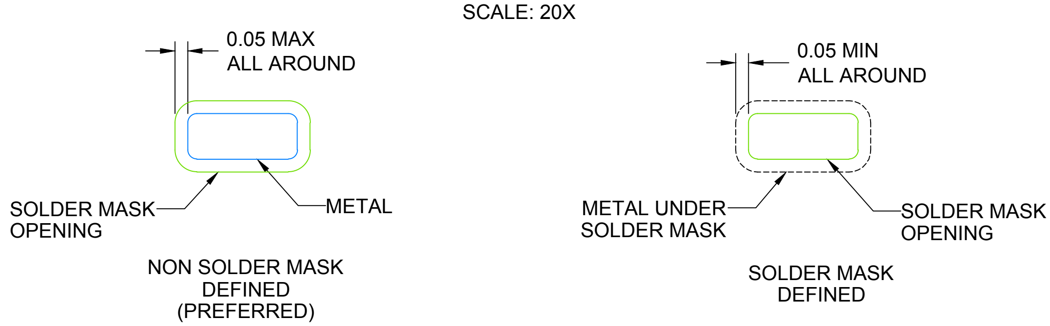
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE: 20X



SOLDER MASK DETAILS

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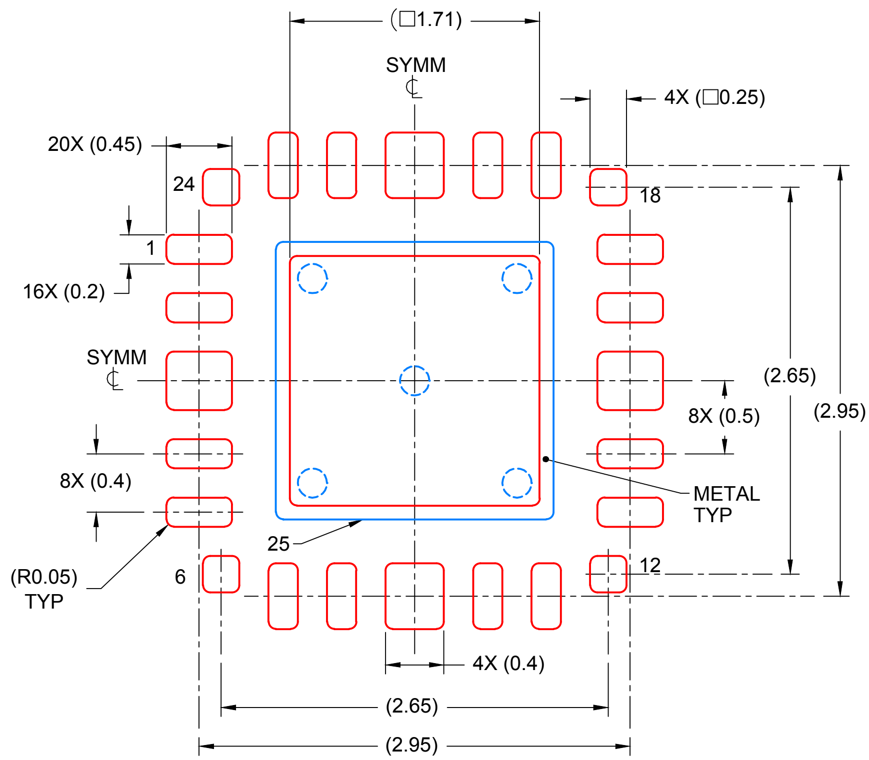
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



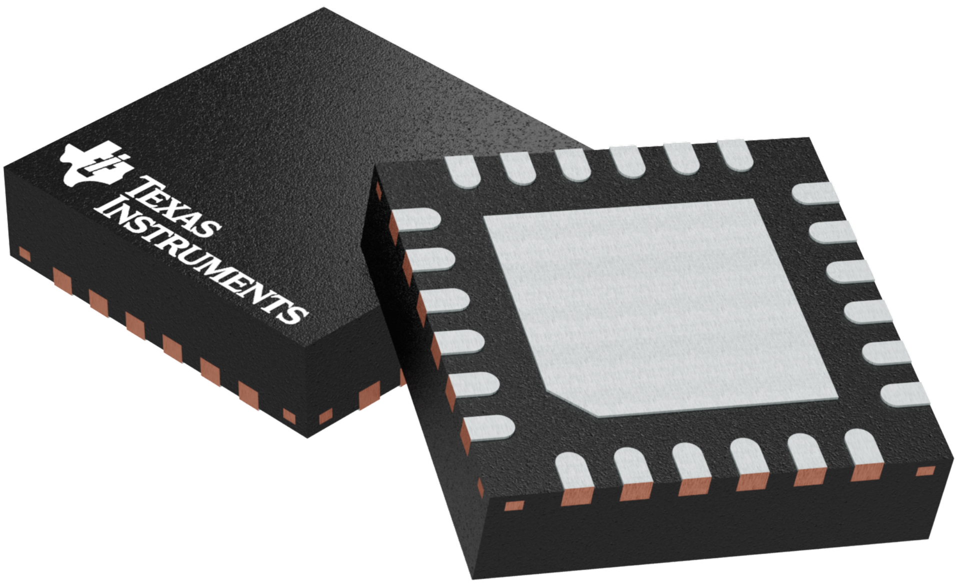
SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD
81% PRINTED COVERAGE BY AREA
SCALE: 20X

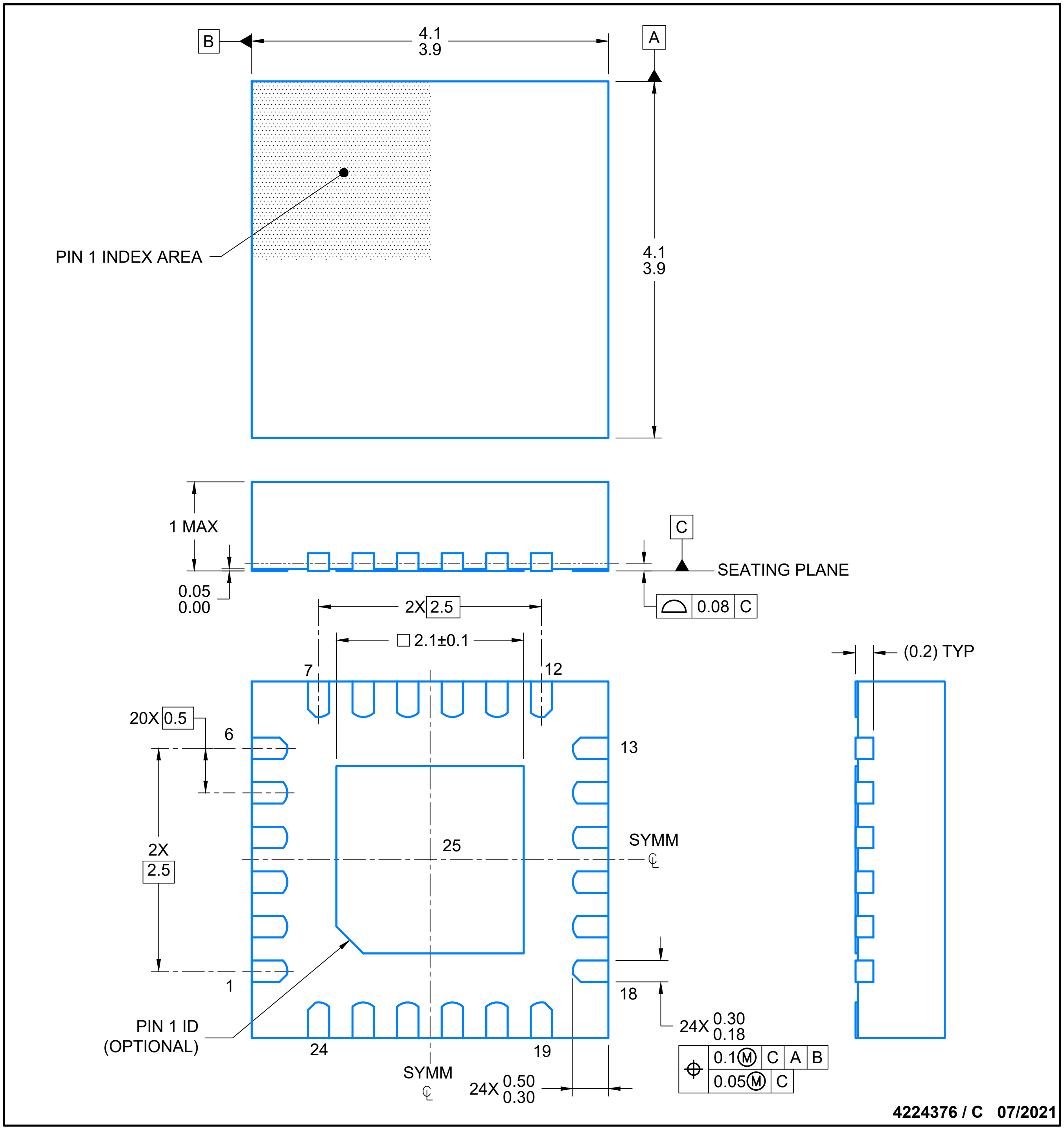
4221088 / B 10/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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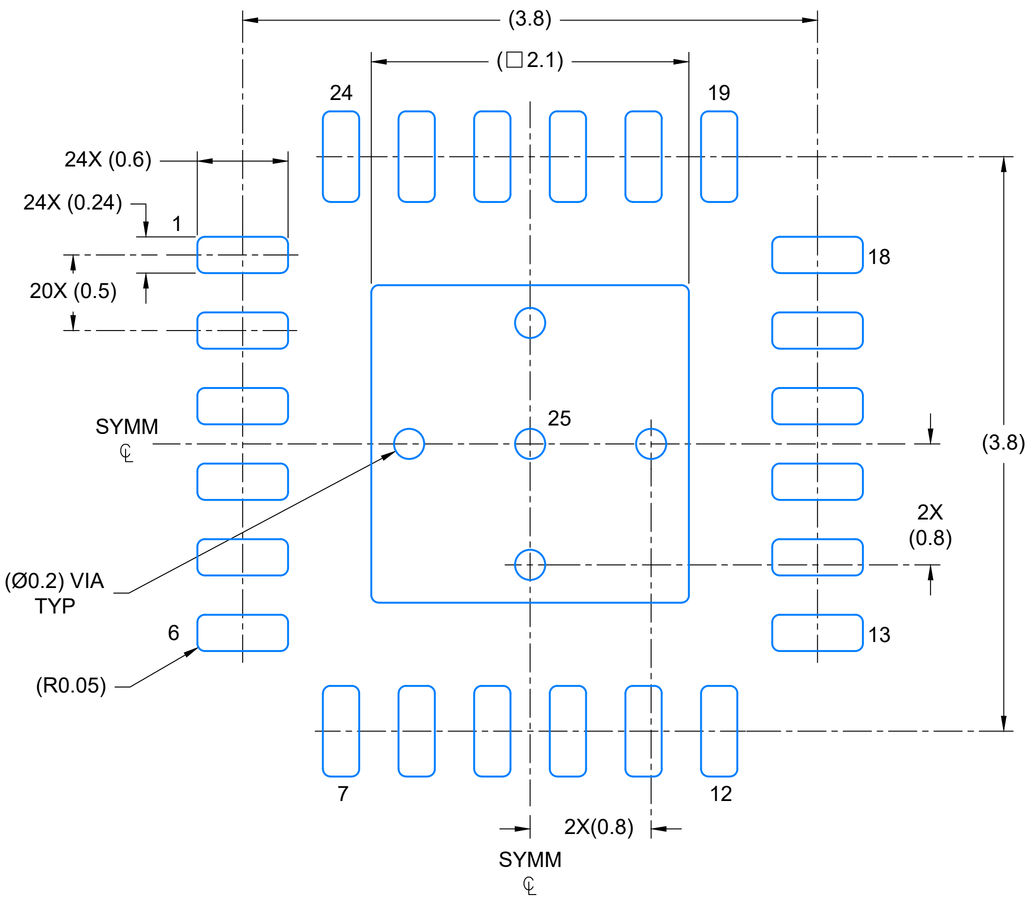
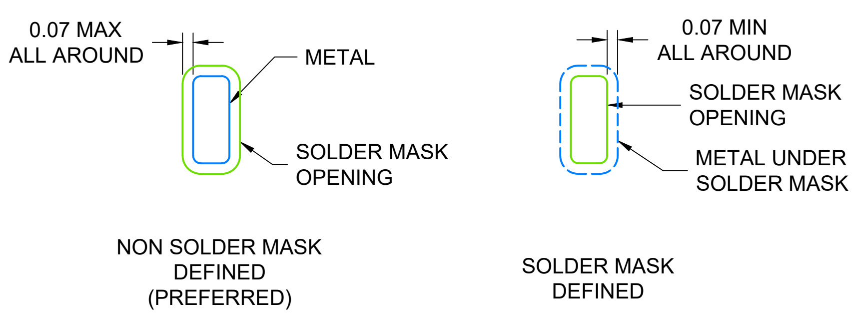
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE: 20X



SOLDER MASK DETAILS

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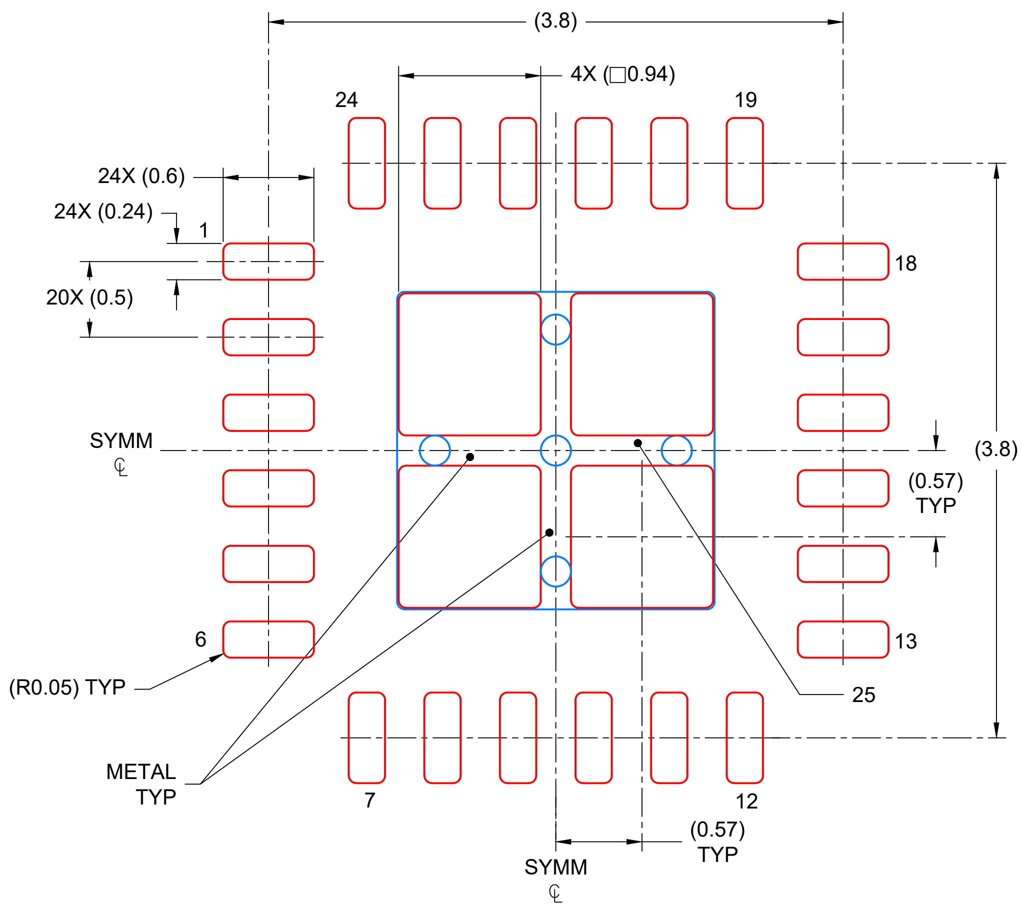
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
80% PRINTED COVERAGE BY AREA
SCALE: 20X

4224376 / C 06/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

IMPORTANT NOTICE AND DISCLAIMER