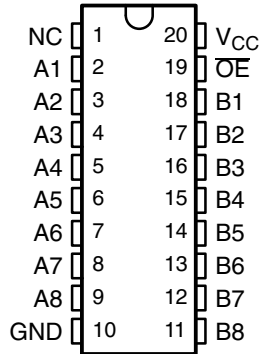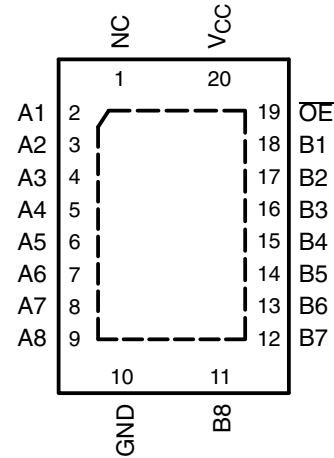- **Standard '245-Type Pinout**
- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Input Levels**

DB, DBQ, DGV, DW, OR PW PACKAGE
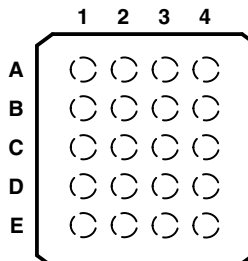**(TOP VIEW)**

NC	1	20	V_{CC}
A1	2	19	$\overline{OE}$
A2	3	18	B1
A3	4	17	B2
A4	5	16	B3
A5	6	15	B4
A6	7	14	B5
A7	8	13	B6
A8	9	12	B7
GND	10	11	B8

NC – No internal connection

RGY PACKAGE
(TOP VIEW)

	NC	V_{CC}	
	1	20	
A1	2	19	$\overline{OE}$
A2	3	18	B1
A3	4	17	B2
A4	5	16	B3
A5	6	15	B4
A6	7	14	B5
A7	8	13	B6
A8	9	12	B7
	10	11	
	GND	B8	

NC – No internal connection

GQN OR ZQN PACKAGE
(TOP VIEW)

	1	2	3	4
A	○	○	○	○
B	○	○	○	○
C	○	○	○	○
D	○	○	○	○
E	○	○	○	○

terminal assignments

	1	2	3	4
A	A1	NC	V_{CC}	$\overline{OE}$
B	A3	B2	A2	B1
C	A5	A4	B4	B3
D	A7	B6	A6	B5
E	GND	A8	B8	B7

NC – No internal connection

description/ordering information

The SN74CBT3245A provides eight bits of high-speed TTL-compatible bus switching. The SOIC, SSOP, TSSOP, and TVSOP packages provide a standard '245 device pinout. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device is organized as one 8-bit switch. When the output-enable ($\overline{OE}$) input is low, the switch is on, and port A is connected to port B. When $\overline{OE}$ is high, the switch is open, and the high-impedance state exists between the two ports.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TEXAS INSTRUMENTS

description/ordering information (continued)

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN – RGY	Tape and reel	SN74CBT3245ARGYR	CU245A
	SOIC – DW	Tube	SN74CBT3245ADW	CBT3245A
		Tape and reel	SN74CBT3245ADWR	
	SSOP – DB	Tape and reel	SN74CBT3245ADBR	CU245A
	SSOP (QSOP) – DBQ	Tape and reel	SN74CBT3245ADBQR	CBT3245A
	TSSOP – PW	Tube	SN74CBT3245APW	CU245A
		Tape and reel	SN74CBT3245APWR	
	TVSOP – DGV	Tape and reel	SN74CBT3245ADGVR	CU245A
	VFBGA – GQN	Tape and reel	SN74CBT3245AGQNR	CU245A
	VFBGA – ZQN (Pb-free)		SN74CBT3245AZQNR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUT $\overline{OE}$	FUNCTION
L	A port = B port
H	Disconnect

logic diagram (positive logic)
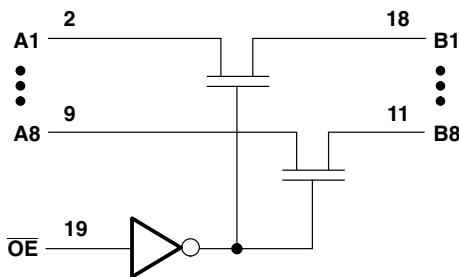
Pin numbers shown are for the DB, DBQ, DGV, DW, PW, and RGY packages.

TEXAS INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC} .... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) .... –0.5 V to 7 V
Continuous channel current .... 128 mA
Input clamp current, I_{IK} ($V_{I/O} < 0$) .... –50 mA
Package thermal impedance, θ_{JA} (see Note 2): DB package .... 70°C/W
              (see Note 2): DBQ package .... 68°C/W
              (see Note 2): DGV package .... 92°C/W
              (see Note 2): DW package .... 58°C/W
              (see Note 2): GQN/ZQN package .... 78°C/W
              (see Note 2): PW package .... 83°C/W
              (see Note 3): RGY package .... 37°C/W
Storage temperature range, T_{stg} .... –65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
    2. The package thermal impedance is calculated in accordance with JESD 51-7.
    3. The package thermal impedance is calculated in accordance with JESD 51-5.

recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level control input voltage	2		V
V_{IL}	Low-level control input voltage		0.8	V
T_A	Operating free-air temperature	–40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP[‡]	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA				–1.2	V
I_I		V_{CC} = 5.5 V,	V_I = 5.5 V or GND				±5	µA
I_{CC}		V_{CC} = 5.5 V,	I_O = 0,	V_I = V_{CC} or GND			50	µA
ΔI_{CC}[§]	Control inputs	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			3.5	mA
C_i	Control inputs	V_I = 3 V or 0				4		pF
$C_{io(OFF)}$		V_O = 3 V or 0,	$\overline{OE}$ = V_{CC}			4		pF
r_{on}[¶]		V_{CC} = 4.5 V	V_I = 0	I_I = 64 mA		5	7	Ω
				I_I = 30 mA		5	7	
			V_I = 2.4 V,	I_I = 15 mA		10	15	

[‡] All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.
[§] This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.
[¶] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

| PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4 V		V_{CC} = 5 V $\pm$ 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}†	A or B	B or A		0.35		0.25	ns
t_{en}	$\overline{OE}$	A or B		6.4	1.9	5.9	ns
t_{dis}	$\overline{OE}$	A or B		5.7	2.1	6	ns

† The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
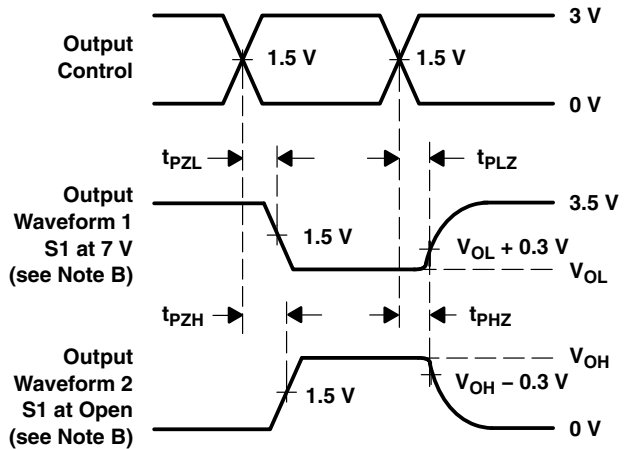
PARAMETER MEASUREMENT INFORMATION
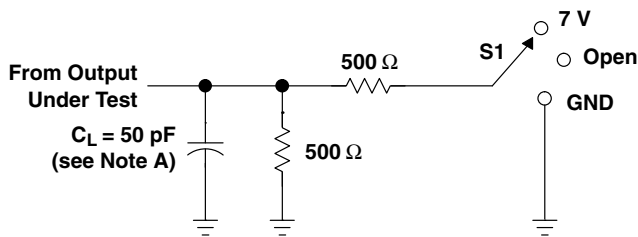
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

LOAD CIRCUIT
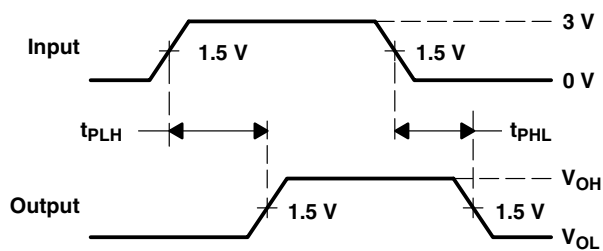
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR $\leq$ 10 MHz, Z_O = 50 Ω, $t_r \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

TEXAS
INSTRUMENTS
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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74CBT3245ADBQR	NRND	SSOP	DBQ	20	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CBT3245A	
SN74CBT3245ADBR	NRND	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CU245A	
SN74CBT3245ADGVR	OBSOLETE	TVSOP	DGV	20		TBD	Call TI	Call TI	-40 to 85	CU245A	
SN74CBT3245ADW	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	-40 to 85	CBT3245A	
SN74CBT3245ADWR	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	-40 to 85	CBT3245A	
SN74CBT3245APW	OBSOLETE	TSSOP	PW	20		TBD	Call TI	Call TI	-40 to 85	CU245A	
SN74CBT3245APWR	OBSOLETE	TSSOP	PW	20		TBD	Call TI	Call TI	-40 to 85	CU245A	
SN74CBT3245ARGYR	OBSOLETE	VQFN	RGY	20		TBD	Call TI	Call TI	-40 to 85	CU245A	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CBT3245ADBQR	SSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74CBT3245ADBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74CBT3245ADGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74CBT3245ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74CBT3245APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74CBT3245ARGYR	VQFN	RGY	20	3000	330.0	12.4	3.8	4.8	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CBT3245ADBQR	SSOP	DBQ	20	2500	356.0	356.0	35.0
SN74CBT3245ADBR	SSOP	DB	20	2000	356.0	356.0	35.0
SN74CBT3245ADGVR	TVSOP	DGV	20	2000	367.0	367.0	35.0
SN74CBT3245ADWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74CBT3245APWR	TSSOP	PW	20	2000	356.0	356.0	35.0
SN74CBT3245ARGYR	VQFN	RGY	20	3000	367.0	367.0	35.0

TUBE

T - Tube height

L - Tube length

W - Tube width

B - Alignment groove width

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74CBT3245ADW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74CBT3245ADWG4	DW	SOIC	20	25	507	12.83	5080	6.6
SN74CBT3245APW	PW	TSSOP	20	70	530	10.2	3600	3.5
SN74CBT3245APWE4	PW	TSSOP	20	70	530	10.2	3600	3.5

DBQ (R−PDSO−G20)   PLASTIC SMALL−OUTLINE PACKAGE

0.344 (8,75)
0.337 (8,55)

20   11

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80)

1   10

0.012 (0,30)
0.008 (0,20)

Pin 1
Index Area

0.025 (0,635)

⌖ 0.005 (0,13) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)   0°−8°

0.035 (0,89)
0.016 (0,40)

4073301−3/H   10/2008
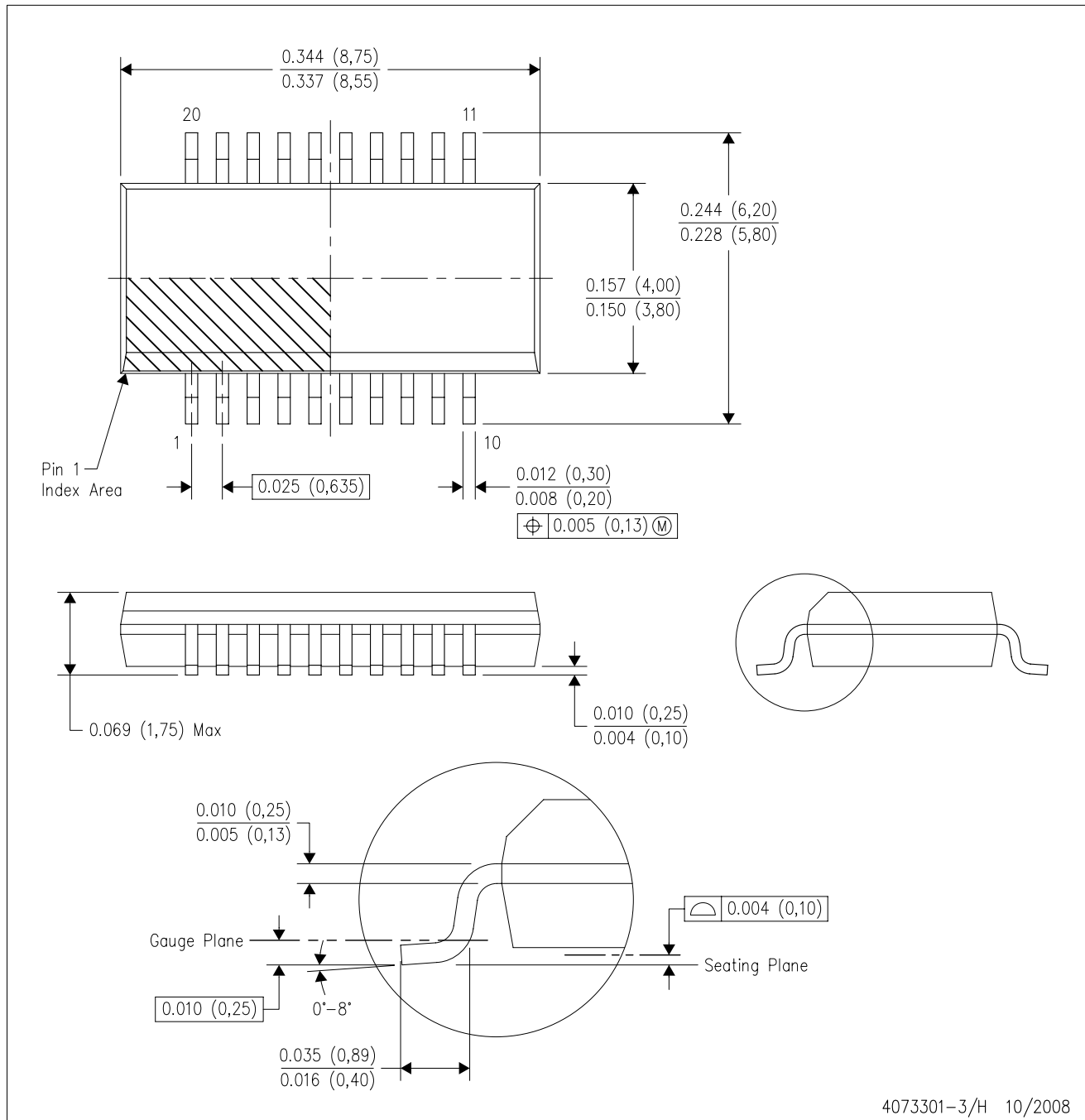
NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
        D. Falls within JEDEC MO−137 variation AD.

TEXAS INSTRUMENTS
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8.2 TYP
7.4

A

PIN 1 INDEX AREA

1

20

18X 0.65

7.5
6.9
NOTE 3

2X
5.85

10

11

B

20X 0.38
0.22

⊕ 0.1 Ⓜ C A B

5.6 5.0
NOTE 4

C

⌒ 0.1 C

SEATING PLANE

SEE DETAIL A

(0.15) TYP

GAGE PLANE

0.25

0° -8°

0.95
0.55

2 MAX

0.05 MIN

DETAIL A
TYPICAL

4214851/B   08/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

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20X (1.85)

1

20X (0.45)

SYMM

(R0.05) TYP

20

18X (0.65)

SYMM

10

11

(7)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK
OPENING

METAL

EXPOSED METAL

0.07 MAX
ALL AROUND

NON-SOLDER MASK
DEFINED
(PREFERRED)

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

0.07 MIN
ALL AROUND

SOLDER MASK
DEFINED

SOLDER MASK DETAILS
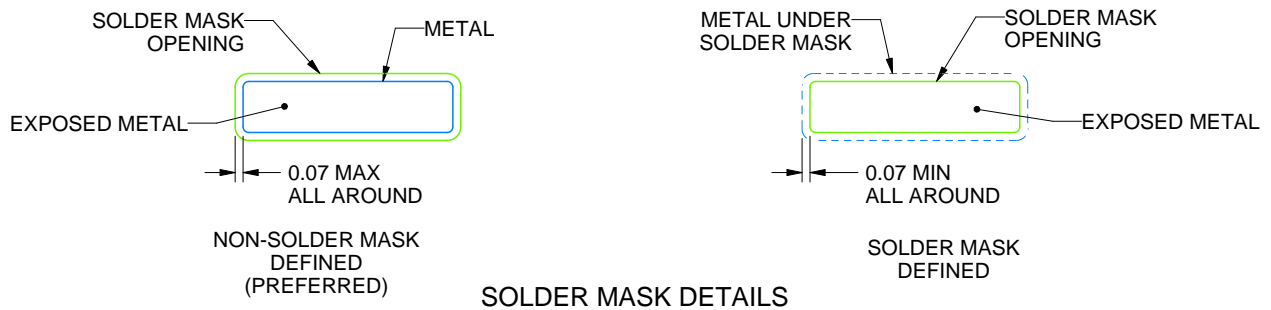
4214851/B   08/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

DB0020A

20X (1.85)

SYMM
℄

1

20X (0.45)

(R0.05) TYP

20

18X (0.65)

SYMM
℄

10

11

(7)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B   08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

10.63 / 9.97 TYP

A

PIN 1 ID AREA

1

20

18X 1.27

13.0 / 12.6 NOTE 3

10

11

2X 11.43

20X 0.51 / 0.31

⊕ 0.25 Ⓜ C A B

B

7.6 / 7.4 NOTE 4

C

SEATING PLANE

⌐ 0.1 C

2.65 MAX

SEE DETAIL A

0.33 / 0.10 TYP

0.25 GAGE PLANE

0° - 8°

1.27 / 0.40

0.3 / 0.1

DETAIL A
TYPICAL

4220724/A   05/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

20X (2)

SYMM

1

20

20X (0.6)

18X (1.27)

SYMM

(R0.05)
TYP

10

11

(9.3)

LAND PATTERN EXAMPLE
SCALE:6X

SOLDER MASK
OPENING

METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

0.07 MAX
ALL AROUND

0.07 MIN
ALL AROUND

NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220724/A   05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

20X (2)

1

20X (0.6)

18X (1.27)

SYMM

20

SYMM

10

11

(9.3)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A   05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

A

6.6
6.2 TYP

PIN 1 INDEX AREA

18X 0.65

1

20

6.6
6.4
NOTE 3

2X

5.85

10

11

B

4.5
4.3
NOTE 4

20X 0.30
0.19

⌖ 0.1 Ⓜ C A B

C

SEATING
PLANE

⌄ 0.1 C

1.2 MAX

SEE DETAIL A

(0.15) TYP

0.25

GAGE PLANE

0.15
0.05

0° -8°

0.75
0.50

DETAIL A
TYPICAL

4220206/A   02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

20X (1.5)

SYMM

1

20X (0.45)

(R0.05) TYP

20

18X (0.65)

SYMM

10

11

(5.8)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK
OPENING

METAL

EXPOSED METAL

0.05 MAX
ALL AROUND

NON-SOLDER MASK
DEFINED
(PREFERRED)

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

0.05 MIN
ALL AROUND

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220206/A   02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

20X (1.5)

SYMM

(R0.05) TYP

1

20X (0.45)

20

18X (0.65)

SYMM

10

11

(5.8)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A   02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

MPDS006C – FEBRUARY 1996 – REVISED AUGUST 2000

DGV (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN

DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

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NOTES: A. All linear dimensions are in millimeters.
      B. This drawing is subject to change without notice.
      C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
      D. Falls within JEDEC: 24/48 Pins – MO-153
                        14/16/20/56 Pins – MO-194

TEXAS INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

RGY 20

VQFN - 1 mm max height

3.5 x 4.5, 0.5 mm pitch

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.
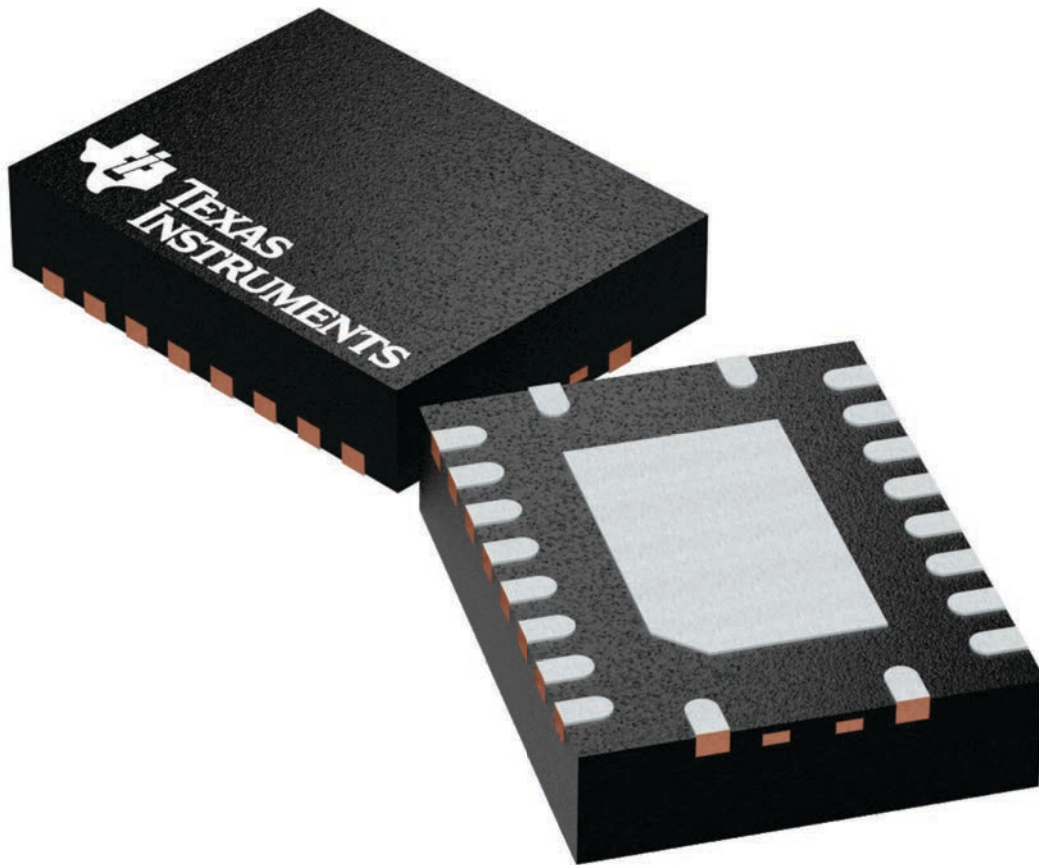
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