SN74LVC1G14 Single Schmitt-Trigger Inverter

1 Features

- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)
- Available in the Texas Instruments NanoFree™ Package
- Supports 5-V V_{CC} Operation
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 4.6 ns at 3.3 V
- Low Power Consumption, 10-µA Max I_{CC}
- ±24-mA Output Drive at 3.3 V
- I_{off} Supports Partial-Power-Down Mode Operation

2 Applications

- AV Receiver
- Audio Dock: Portable
- Blu-ray Player and Home Theater
- Embedded PC
- MP3 Player/Recorder (Portable Audio)
- Personal Digital Assistant (PDA)
- Power: Telecom/Server AC/DC Supply: Single Controller: Analog and Digital
- Solid State Drive (SSD): Client and Enterprise
- TV: LCD/Digital and High-Definition (HDTV)
- Tablet: Enterprise
- Video Analytics: Server
- Wireless Headset, Keyboard, and Mouse

3 Description

This single Schmitt-trigger inverter is designed for 1.65-V to 5.5-V V_{CC} operation.

The SN74LVC1G14 device contains one inverter and performs the Boolean function $Y = \overline{A}$. The device functions as an independent inverter with Schmitt-trigger inputs, so the device has different input threshold levels for positive-going (V_{T+}) and negative-going (V_{T-}) signals to provide hysteresis (ΔV_T) which makes the device tolerant to slow or noisy input signals.

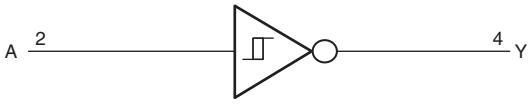
NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs when the device is powered down. This inhibits current backflow into the device which prevents damage to the device.

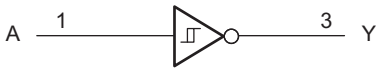
Device Information

ORDER NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LVC1G14DBV	SOT-23 (5)	2.90 mm × 1.60 mm
SN74LVC1G14DCK	SC70 (5)	2.00 mm × 1.25 mm
SN74LVC1G14DRL	SOT-5X3 (5)	1.60 mm × 1.20 mm
SN74LVC1G14DRY	SON (6)	1.45 mm × 1.00 mm
SN74LVC1G14DSF	SON (6)	1.00 mm × 1.00 mm
SN74LVC1G14YZP	DSBGA (5)	1.39 mm × 0.89 mm
SN74LVC1G14YZV	DSBGA (4)	0.89 mm × 0.89 mm
SN74LVC1G14DPW	X2SON (5)	0.80 mm x 0.80 mm

Logic Diagram (Positive Logic)
(DBV, DCK, DRL, DRY, DPW, and YZP Package)



Logic Diagram (Positive Logic)
(YZV Package)



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 Features ... 1
2 Applications ... 1
3 Description ... 1
4 Revision History ... 2
5 Pin Configuration and Functions ... 3
6 Specifications ... 4
6.1 Absolute Maximum Ratings ... 4
6.2 ESD Ratings ... 4
6.3 Recommended Operating Conditions ... 5
6.4 Thermal Information ... 5
6.5 Electrical Characteristics ... 6
6.6 Switching Characteristics: –40°C to 85°C ... 7
6.7 Switching Characteristics: –40°C to 125°C ... 7
6.8 Operating Characteristics ... 7
6.9 Typical Characteristics ... 7
7 Parameter Measurement Information ... 8
8 Detailed Description ... 9
8.1 Overview ... 9
8.2 Functional Block Diagrams ... 9
8.3 Feature Description ... 9
8.4 Device Functional Modes ... 10
9 Application and Implementation ... 11
9.1 Application Information ... 11
9.2 Typical Application ... 11
10 Power Supply Recommendations ... 12
11 Layout ... 12
11.1 Layout Guidelines ... 12
11.2 Layout Example ... 13
12 Device and Documentation Support ... 14
12.1 Documentation Support ... 14
12.2 Receiving Notification of Documentation Updates 14
12.3 Community Resources ... 14
12.4 Trademarks ... 14
12.5 Electrostatic Discharge Caution ... 14
12.6 Glossary ... 14
13 Mechanical, Packaging, and Orderable Information ... 14

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision X (August 2017) to Revision Y — **Page**

- Changed New package pinout added to Pin Functions table. Multiple Pin Functions tables condensed to one. ... 4
- Changed T_j and T_{stg} lines switched for consistency with other devices. ... 4
- Added differentiated ROC temperatures for DPW, YZP and YZV packages ... 5
- Changed format of Switching Characteristics tables to include columns for different C_L conditions ... 7
- Added temperature range to Conditions statement for Switching Characteristics tables ... 7
- Replaced PMI section with updated load circuit and relevant waveform figures. Collapsed parameter measurement values into one table. ... 8

Changes from Revision W (March 2014) to Revision X — **Page**

- Added *Thermal Information* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, and *Layout* section ... 1
- Added DSF, YZP, YZV, and DPW packages to *Device Information* table ... 1
- Changed *Terminal Configuration and Functions* to *Pin Configuration and Functions* ... 3
- Moved Storage temperature, T_{stg} to *Absolute Maximum Ratings* table. ... 4
- Changed *Handling Ratings* table to *ESD Ratings* ... 4
- Changed values in the Thermal Information table to align with JEDEC standards. ... 5
- Added typical application. ... 11
- Added *Documentation Support*, *Receiving Notification of Documentation Updates*, and *Community Resources* ... 14

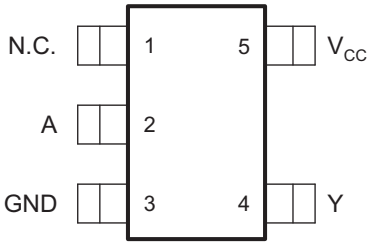
Changes from Revision V (Novmber 2012) to Revision W — **Page**

- Added DPW Package ... 1
- Added *Applications* ... 1
- Moved T_{stg} to *Handling Ratings* table ... 4

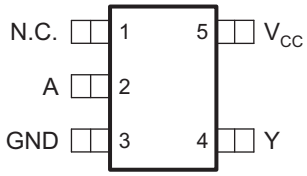
Copyright © 1999–2018, Texas Instruments Incorporated

5 Pin Configuration and Functions

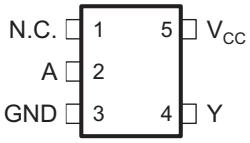
DBV Package
5-Pin SOT-23
Top View



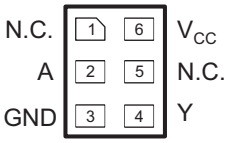
DCK Package
5-Pin SC70
Top View



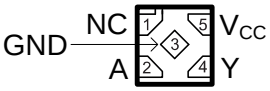
DRL Package
5-Pin SOT-5X3
Top View



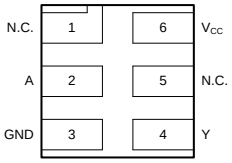
DRY Package
6-Pin SON
Top View



DPW Package
5-Pin X2SON
Top View



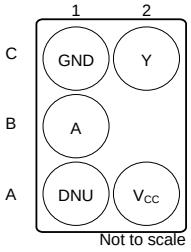
DSF Package
6-Pin SON
Top View



See mechanical drawings for dimensions.

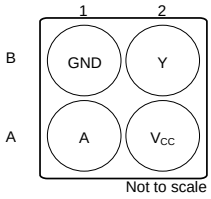
N.C. – No internal connection

YZP Package
5-Pin DSBGA
Bottom View



DNU – Do not use

YZV Package
4-Pin DSBGA
Bottom View



Pin Functions

PIN					I/O	DESCRIPTION
NAME	DBV, DCK, DRL, DPW	DRY, DSF	YZP	YZV		
A	2	2	B1	A1	I	Signal Input
GND	3	3	C1	B1	—	Ground
N.C.	1	1, 5	—	—	—	No internal connection (1)
DNU	—	—	A1	—	—	Do not use (2)
V_{CC}	5	6	A2	A2	—	Positive Supply
Y	4	4	C2	B2	O	Signal Output

(1) Pins labeled N.C. can be connected to any signal or voltage source, including ground. They should always be soldered to the board.
(2) Pins labeled DNU should not be connected to any signal or voltage source, including ground. They should always be soldered to the board.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	6.5	V
V_I	Input voltage (2)		–0.5	6.5	V
V_O	Voltage range applied to any output in the high-impedance or power-off state (2)		–0.5	6.5	V
V_O	Voltage range applied to any output in the high or low state (2) (3)		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CC} or GND			±100	mA
T_j	Maximum junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of V_{CC} is provided in the recommended operating conditions table.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	1000	
		Machine Model (A115-A)	200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Copyright © 1999–2018, Texas Instruments Incorporated

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage	Operating	1.65	5.5	V
		Data retention only	1.5		
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 1.65 V		–4	mA
		V_{CC} = 2.3 V		–8	
		V_{CC} = 3 V		–16	
				–24	
		V_{CC} = 4.5 V		–32	
I_{OL}	Low-level output current	V_{CC} = 1.65 V		4	mA
		V_{CC} = 2.3 V		8	
		V_{CC} = 3 V		16	
				24	
		V_{CC} = 4.5 V		32	
T_A	Operating free-air temperature	YZP, YZV, and DPW packages	–40	85	°C
		All other packages	–40	125	

(1) All unused inputs of the device must be held at V_{CC} or GND to assure proper device operation. See *Implications of Slow or Floating CMOS Inputs*.

6.4 Thermal Information

THERMAL METRIC(1)		SN74LVC1G14							UNIT
		DBV (SOT-23)	DCK (SC70)	DRL (SOT-5X3)	DRY (SON)	DPW (X2SON)	YZV (DSBGA)	YZP (DSBGA)	
		5 PINS	5 PINS	5 PINS	5 PINS	5 PINS	4 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	247.2	276.1	296.2	369.6	522.9	168.2	146.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	154.5	178.9	137.3	257.6	250.5	2.1	1.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	86.8	70.9	145.3	230.8	384.0	55.9	39.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	58.0	47.0	14.7	77.2	46.5	1.1	0.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	86.4	69.3	145.9	231.0	382.8	56.3	39.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	174.1	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

Copyright © 1999–2018, Texas Instruments Incorporated

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	–40°C to 85°C			–40°C to 125°C[1]			UNIT
			MIN	TYP[2]	MAX	MIN	TYP	MAX	
V_{T+} Positive-going input threshold voltage		1.65 V	0.79		1.16	.79		1.16	V
		2.3 V	1.11		1.56	1.11		1.56	
		3 V	1.5		1.87	1.5		1.87	
		4.5 V	2.16		2.74	2.16		2.74	
		5.5 V	2.61		3.33	2.61		3.33	
$V_{T–}$ Negative-going input threshold voltage	DBV, DCK, DRL, DRY, DSF, YZV and YZP packages	1.65 V	0.39		0.62	.39		.64	V
		2.3 V	0.58		0.87	.58		.89	
		3 V	0.84		1.14	.84		1.16	
		4.5 V	1.41		1.79	1.41		1.79	
		5.5 V	1.87		2.29	1.87		2.29	
$V_{T–}$ Negative-going input threshold voltage	DPW package	1.65 V	0.44		0.67				V
		2.3 V	0.63		0.92				
		3 V	0.89		1.19				
		4.5 V	1.46		1.84				
		5.5 V	1.92		2.34				
ΔV_T Hysteresis ($V_{T+} – V_{T–}$)		1.65 V	0.37		0.62	0.37		0.62	V
		2.3 V	0.48		0.77	0.48		0.77	
		3 V	0.56		0.87	0.56		0.87	
		4.5 V	0.71		1.04	0.71		1.04	
		5.5 V	0.71		1.11	0.71		1.11	
V_{OH}	I_{OL} = –100 µA	1.65 V to 4.5 V	V_{CC} – 0.1			V_{CC} – 0.1			V
	I_{OL} = –4 mA	1.65 V	1.2			1.2			
	I_{OL} = –8 mA	2.3 V	1.9			1.9			
	I_{OL} = –16 mA	3 V	2.4			2.4			
	I_{OL} = –24 mA		2.3			2.3			
	I_{OL} = –32 mA	4.5 V	3.8			3.8			
V_{OL}	I_{OL} = 100 µA	1.65 V to 4.5 V			0.1			0.1	V
	I_{OL} = 4 mA	1.65 V			0.45			0.45	
	I_{OL} = 8 mA	2.3 V			0.3			0.3	
	I_{OL} = 16 mA	3 V			0.4			0.4	
	I_{OL} = 24 mA				0.55			0.55	
	I_{OL} = 32 mA	4.5 V			0.55			0.7	
I_I A input	V_I = 5.5 V or GND	0 to 5.5 V			±5			±5	µA
I_{off}	V_I or V_O = 5.5 V	0			±10			±10	µA
I_{CC}	V_I = 5.5 V or GND, I_O = 0	1.65 V to 5.5 V			10			10	µA
ΔI_{CC}	One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	3 V to 5.5 V			500			500	µA
C_i	V_I = V_{CC} or GND	3.3 V		4.5			4.5		pF

(1) These specifications do not apply to DPW, YZV and YZP packages. DPW, YZV and YZP have a recommended operating free-air temperature range of –40°C to 85°C.
(2) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

Copyright © 1999–2018, Texas Instruments Incorporated

6.6 Switching Characteristics: –40°C to 85°C

over recommended operating free-air temperature range, (–40°C to 85°C unless otherwise noted) (see)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	C_L = 15 pF		C_L = 30 pF or 50 pF		UNIT
				MIN	MAX	MIN	MAX	
t_{pd}	A	Y	1.8 V ± 0.15 V	2.8	9.9	3.8	11	ns
			2.5 V ± 0.2 V	1.6	5.5	2	6.5	
			3.3 V ± 0.3 V	1.5	4.6	1.8	5.5	
			5 V ± 0.5 V	0.9	4.4	1.2	5	

6.7 Switching Characteristics: –40°C to 125°C

over operating free-air temperature range, (–40°C to 125°C unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	C_L = 30 pF or 50 pF		UNIT
				MIN	MAX	
t_{pd}	A	Y	1.8 V ± 0.15 V	3.8	13	ns
			2.5 V ± 0.2 V	2	8	
			3.3 V ± 0.3 V	1.8	6.5	
			5 V ± 0.5 V	1.2	6	

6.8 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	f = 10 MHz	1.8 V	20	pF
			2.5 V	21	
			3.3 V	22	
			5 V	25	

6.9 Typical Characteristics

T_A = 25°C

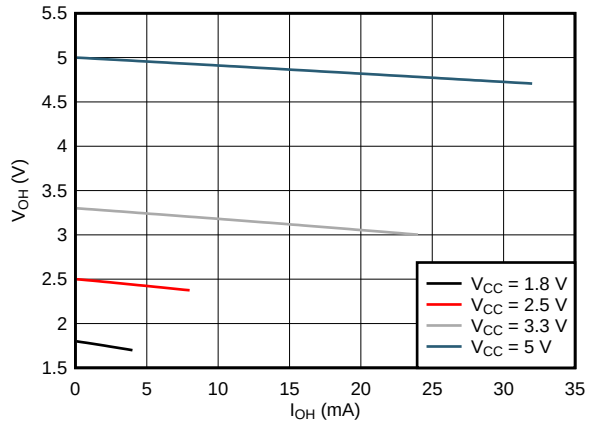


Figure 1. Typical V_{OH} vs I_{OH} - 25°C

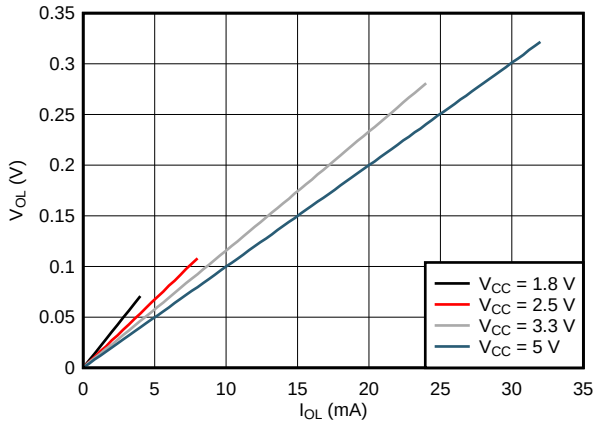
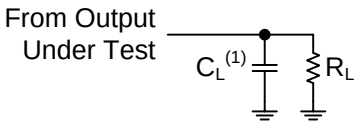


Figure 2. Typical V_{OL} vs I_{OL} - 25°C

Copyright © 1999–2018, Texas Instruments Incorporated

7 Parameter Measurement Information

- Input pulse is supplied by generator having the following characteristics: PRR ≤ 10MHz. Z_O = 50Ω.
- The outputs are measured one at a time, with one transition per measurement.

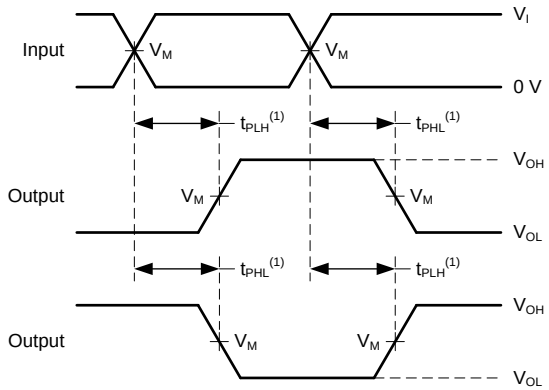


(1) C_L includes probe and jig capacitance.

Figure 3. Load Circuit

Table 1. Parameter Measurement Conditions

V_{cc}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_D
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{cc}	≤ 2 ns	$V_{cc}/2$	2 × V_{cc}	15 pF	1 MΩ	0.15 V
					30 pF	1 kΩ	
2.5 V ± 0.2 V	V_{cc}	≤ 2 ns	$V_{cc}/2$	2 × V_{cc}	15 pF	1 MΩ	0.15 V
					30 pF	500 Ω	
3.3 V ± 0.3 V	3 V	≤ 2.5 ns	1.5 V	6 V	15 pF	1 MΩ	0.3 V
					50 pF	500 Ω	
5 V ± 0.5 V	V_{cc}	≤ 2.5 ns	$V_{cc}/2$	2 × V_{cc}	15 pF	1 MΩ	0.3 V
					50 pF	500 Ω	



(1) The maximum value of t_{pd} is the worst case of t_{PLH} or t_{PHL}

Figure 4. Voltage Waveforms, Propagation Delay Times, Inverting and Non-Inverting Outputs

Copyright © 1999–2018, Texas Instruments Incorporated

8 Detailed Description

8.1 Overview

The SN74LVC1G14 single Schmitt-trigger inverter is designed for 1.65 V to 5.5 V operation and performs the Boolean function Y = $\overline{A}$. This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs when the device is powered down. This inhibits current backflow into the device which prevents damage to the device.

8.2 Functional Block Diagrams

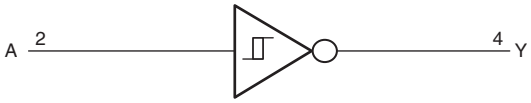


Figure 5. Logic Diagram (Positive Logic)
(DBV, DCK, DRL, DRY, DPW, and YZP Package)

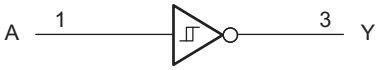


Figure 6. Logic Diagram (Positive Logic)
(YZV Package)

8.3 Feature Description

8.3.1 Balanced High-Drive CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The high drive capability of this device creates fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the power output of the device to be limited to avoid thermal runaway and damage due to over-current. The electrical and thermal limits defined the in the *Absolute Maximum Ratings*

Absolute Maximum Ratings] must be followed at all times.

8.3.2 CMOS Schmitt-Trigger Inputs

Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using ohm's law (R = V ÷ I).

The Schmitt-trigger input architecture provides hysteresis as define in the *Electrical Characteristics*, which makes this device extremely tolerant to slow or noisy inputs. While the inputs can be driven much slower than standard CMOS inputs, it is still recommended to properly terminate unused inputs. Driving the inputs slowly will also increase dynamic current consumption of the device.

Copyright © 1999–2018, Texas Instruments Incorporated

Feature Description (continued)

8.3.3 Clamp Diodes

The inputs and outputs to this device have negative clamping diodes.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input negative-voltage and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

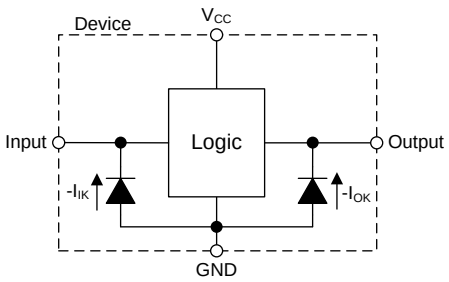


Figure 7. Electrical Placement of Clamping Diodes for Each Input and Output

8.3.4 Partial Power Down (I_{off})

The inputs and outputs for this device enter a high impedance state when the supply voltage is 0 V. The maximum leakage into or out of any input or output pin on the device is specified by I_{off} in the *Electrical Characteristics*.

8.3.5 Over-Voltage Tolerant Inputs

Input signals to this device can be driven above the supply voltage so long as they remain below the maximum input voltage value specified in the *Absolute Maximum Ratings*.

8.4 Device Functional Modes

Table 2 lists the functional modes of the SN74LVC1G14 device.

Table 2. Function Table

INPUT A	OUTPUT Y
H	L
L	H

Copyright © 1999–2018, Texas Instruments Incorporated

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

Mechanical input elements, such as push buttons or rotary knobs, offer simple ways to interact with electronic systems. Typically, these elements have recoil or bouncing, where the mechanical element makes and breaks contact multiple times during human interaction. This bouncing can cause one or more repeated signals to be passed, triggering multiple actions when only a single input was intended. One potential solution to mitigating these multiple inputs is by utilizing a Schmitt-trigger to create a debounce circuit. Figure 8 shows an example of this solution.

9.2 Typical Application

The input due to the push button switches multiple times, causing the output of a non Schmitt-trigger device to trigger multiple times, while the Schmitt-trigger input device with RC delay limits the output pulse to a single pulse desired by the user. The separated positive and negative input voltage threshold values, see Figure 9, prevent multiple triggers from occurring.

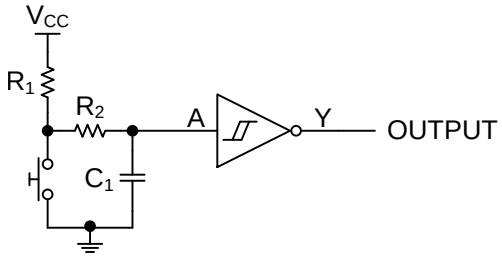


Figure 8. Push Button Debounce Circuit Schematic

9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive also creates fast edges into light loads so routing and load conditions should be considered to prevent ringing.

9.2.2 Detailed Design Procedure

1. Recommended Input Conditions:
   - For specified high and low levels, see (V_{T+} and V_{T-}) in the *Recommended Operating Conditions* table.
   - Inputs are overvoltage tolerant allowing them to go as high as (V_I max) in the *Recommended Operating Conditions* table at any valid V_{CC}.
2. Recommended Output Conditions:
   - Load currents should not exceed (I_O max) per output and should not exceed (Continuous current through V_{CC} or GND) total current for the part. These limits are located in the *Absolute Maximum Ratings* table.

Copyright © 1999–2018, Texas Instruments Incorporated

Typical Application (continued)

9.2.3 Application Curve

Figure 9 is created from the values given in the *Electrical Characteristics*. Linear interpolation shows the values between each given point.

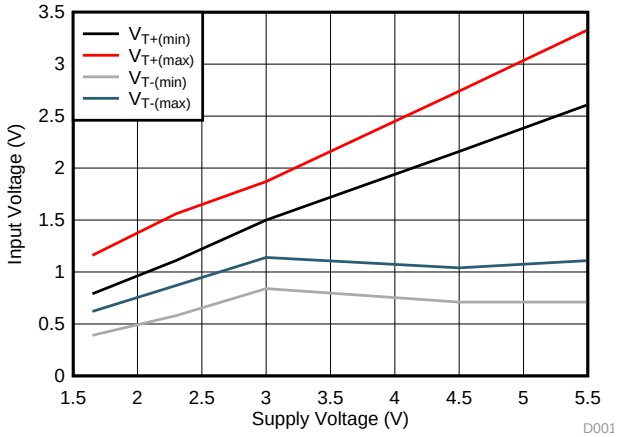


Figure 9. Interpolated Threshold Voltages vs. V_{CC}

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions* table.

The V_{CC} pin must have a good bypass capacitor to prevent power disturbance. A 0.1-µF capacitor is recommended, and it is ok to parallel multiple bypass caps to reject different frequencies of noise. 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor must be installed as close to the power pin as possible for best results.

11 Layout

11.1 Layout Guidelines

Even low data rate digital signals can contain high-frequency signal components due to fast edge rates. When a printed-circuit board (PCB) trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self–inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

An example layout is given in Figure 10 for the DPW (X2SON-5) package. This example layout includes a 0402 (metric) capacitor and uses the measurements found in the example board layout appended to this end of this datasheet. A via of diameter 0.1 mm (3.973 mil) is placed directly in the center of the device. This via can be used to trace out the center pin connection through another board layer, or it can be left out of the layout

Copyright © 1999–2018, Texas Instruments Incorporated

11.2 Layout Example

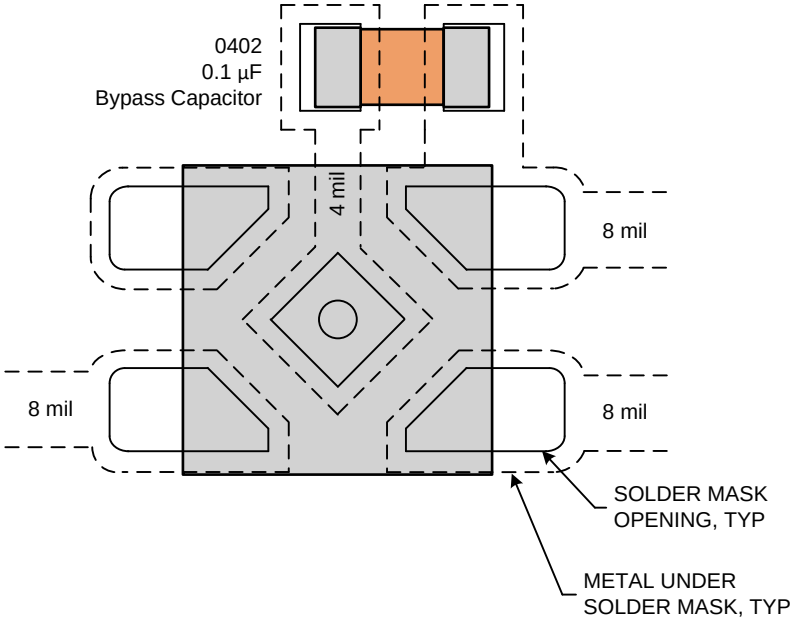


Figure 10. Example Layout With DPW (X2SON-5) Package

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

Implications of Slow or Floating CMOS Inputs

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

NanoFree, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Copyright © 1999–2018, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVC1G14DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(C145, C14F, C14J, C14K, C14R) (C14H, C14S)	Samples
SN74LVC1G14DBVRE4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C14F	Samples
SN74LVC1G14DBVRG4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C14F	Samples
SN74LVC1G14DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(C145, C14F, C14J, C14K, C14R) (C14H, C14S)	Samples
SN74LVC1G14DBVTE4	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C14F	Samples
SN74LVC1G14DBVTG4	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C14F	Samples
SN74LVC1G14DCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(CF5, CFF, CFJ, CFK, CFR, CFT) (CFH, CFS)	Samples
SN74LVC1G14DCKRE4	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CF5 CFS	Samples
SN74LVC1G14DCKT	ACTIVE	SC70	DCK	5	250	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(CF5, CFF, CFJ, CFK, CFR, CFT) (CFH, CFS)	Samples
SN74LVC1G14DCKTE4	ACTIVE	SC70	DCK	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CF5 CFS	Samples
SN74LVC1G14DCKTG4	ACTIVE	SC70	DCK	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CF5 CFS	Samples
SN74LVC1G14DPWR	ACTIVE	X2SON	DPW	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	9H	Samples
SN74LVC1G14DRLR	ACTIVE	SOT-5X3	DRL	5	4000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(CF7, CFR)	Samples
SN74LVC1G14DRLRG4	ACTIVE	SOT-5X3	DRL	5	4000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(CF7, CFR)	Samples
SN74LVC1G14DRYR	ACTIVE	SON	DRY	6	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CF	Samples
SN74LVC1G14DSFR	ACTIVE	SON	DSF	6	5000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CF	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVC1G14YZPR	ACTIVE	DSBGA	YZP	5	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(CF7, CFN)	Samples
SN74LVC1G14YZVR	ACTIVE	DSBGA	YZV	4	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	CF (7, N)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LVC1G14 :

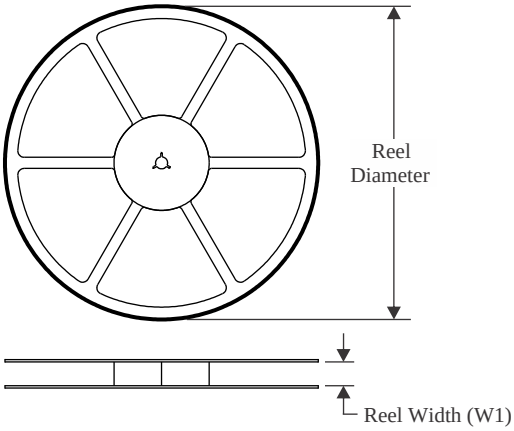
- Automotive : SN74LVC1G14-Q1
- Enhanced Product : SN74LVC1G14-EP

NOTE: Qualified Version Definitions:

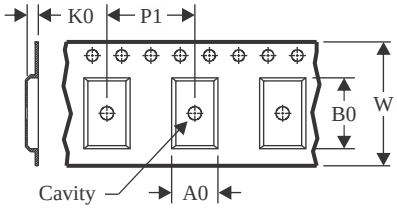
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

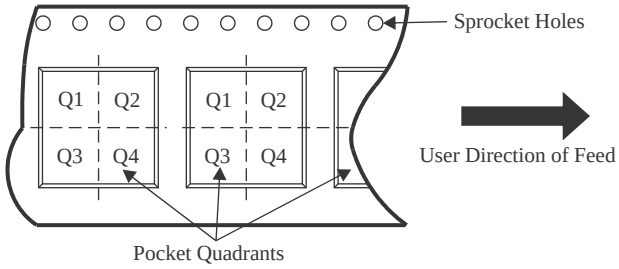


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

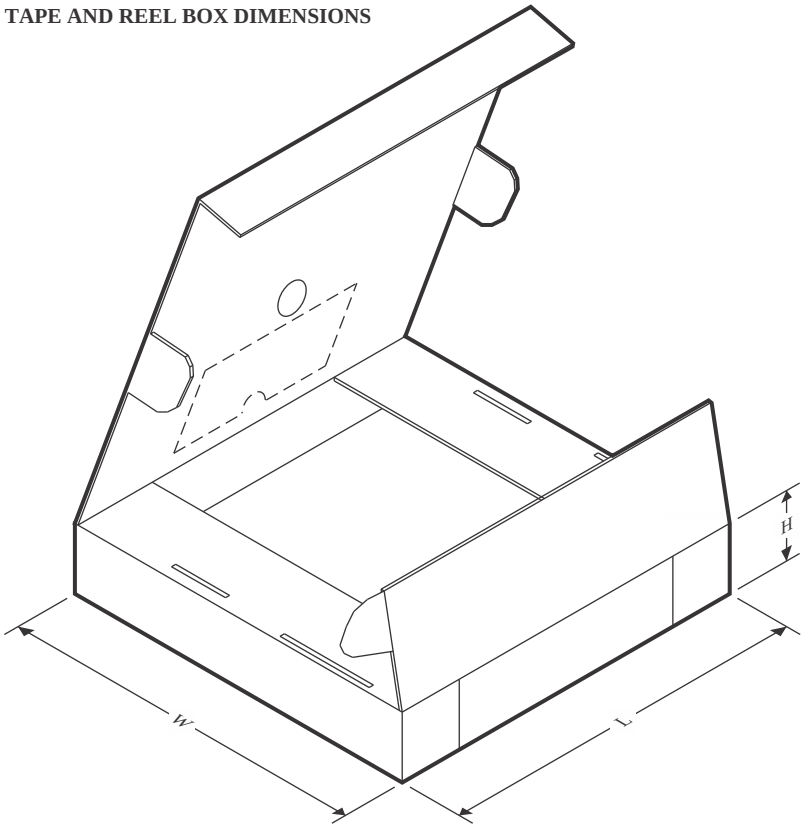
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G14DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1G14DBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G14DBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
SN74LVC1G14DBVTG4	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G14DCKR	SC70	DCK	5	3000	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3
SN74LVC1G14DCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G14DCKT	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1G14DCKTG4	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1G14DPWR	X2SON	DPW	5	3000	178.0	8.4	0.91	0.91	0.5	2.0	8.0	Q3
SN74LVC1G14DRLR	SOT-5X3	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
SN74LVC1G14DRYR	SON	DRY	6	5000	180.0	9.5	1.2	1.65	0.7	4.0	8.0	Q1
SN74LVC1G14DSFR	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
SN74LVC1G14YZPR	DSBGA	YZP	5	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1
SN74LVC1G14YZVR	DSBGA	YZV	4	3000	178.0	9.2	1.0	1.0	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G14DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
SN74LVC1G14DBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74LVC1G14DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74LVC1G14DBVTG4	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74LVC1G14DCKR	SC70	DCK	5	3000	210.0	185.0	35.0
SN74LVC1G14DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G14DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G14DCKTG4	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G14DPWR	X2SON	DPW	5	3000	205.0	200.0	33.0
SN74LVC1G14DRLR	SOT-5X3	DRL	5	4000	202.0	201.0	28.0
SN74LVC1G14DRYR	SON	DRY	6	5000	189.0	185.0	36.0
SN74LVC1G14DSFR	SON	DSF	6	5000	184.0	184.0	19.0
SN74LVC1G14YZPR	DSBGA	YZP	5	3000	220.0	220.0	35.0
SN74LVC1G14YZVR	DSBGA	YZV	4	3000	220.0	220.0	35.0

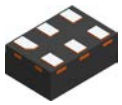
DRY 6 USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

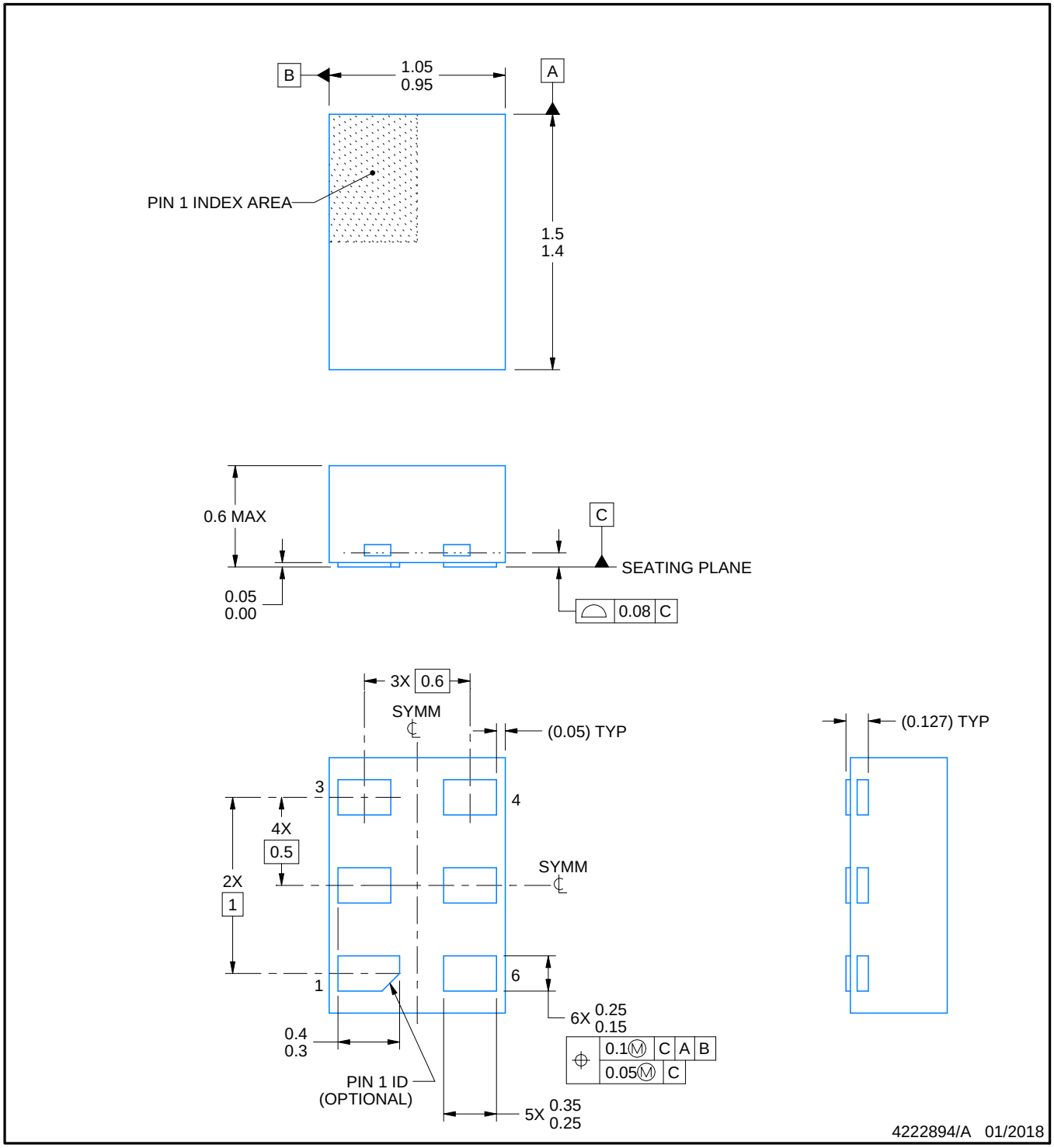
DRY0006A



PACKAGE OUTLINE

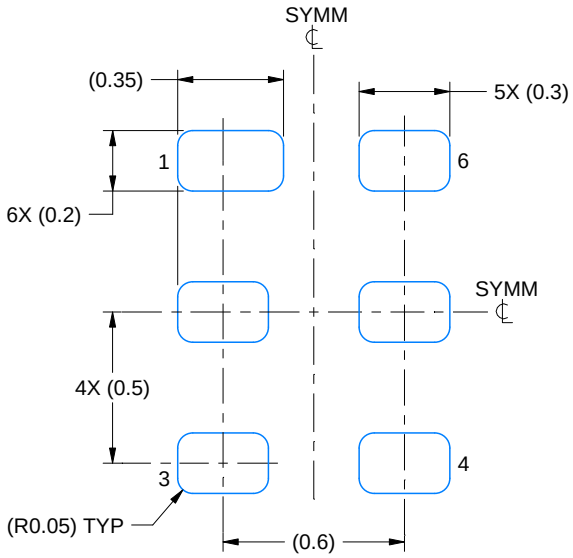
USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

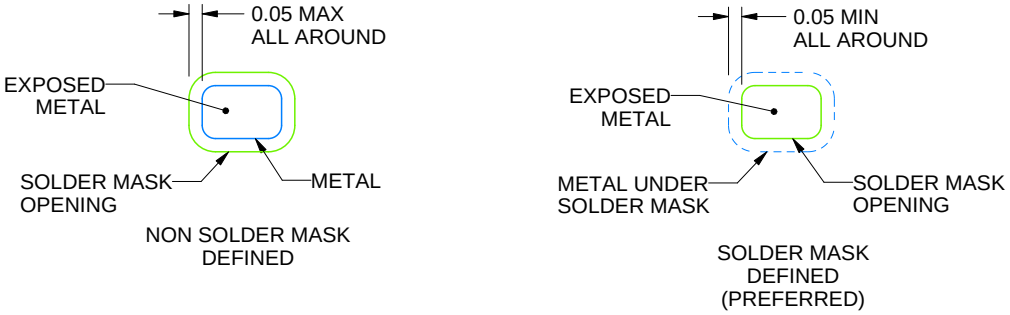


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4222894/A 01/2018

NOTES: (continued)

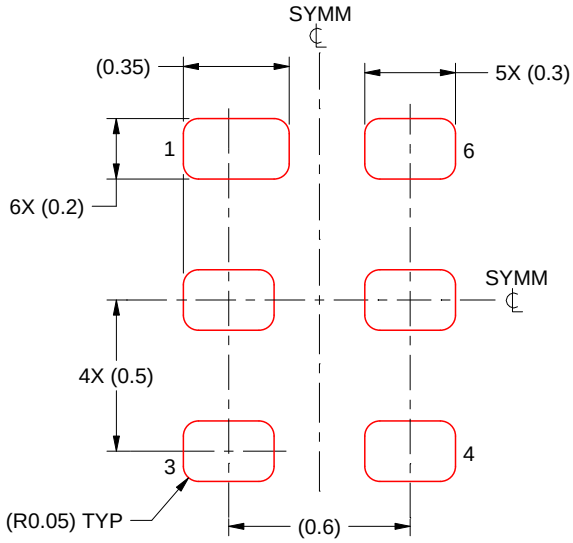
3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222894/A 01/2018

NOTES: (continued)

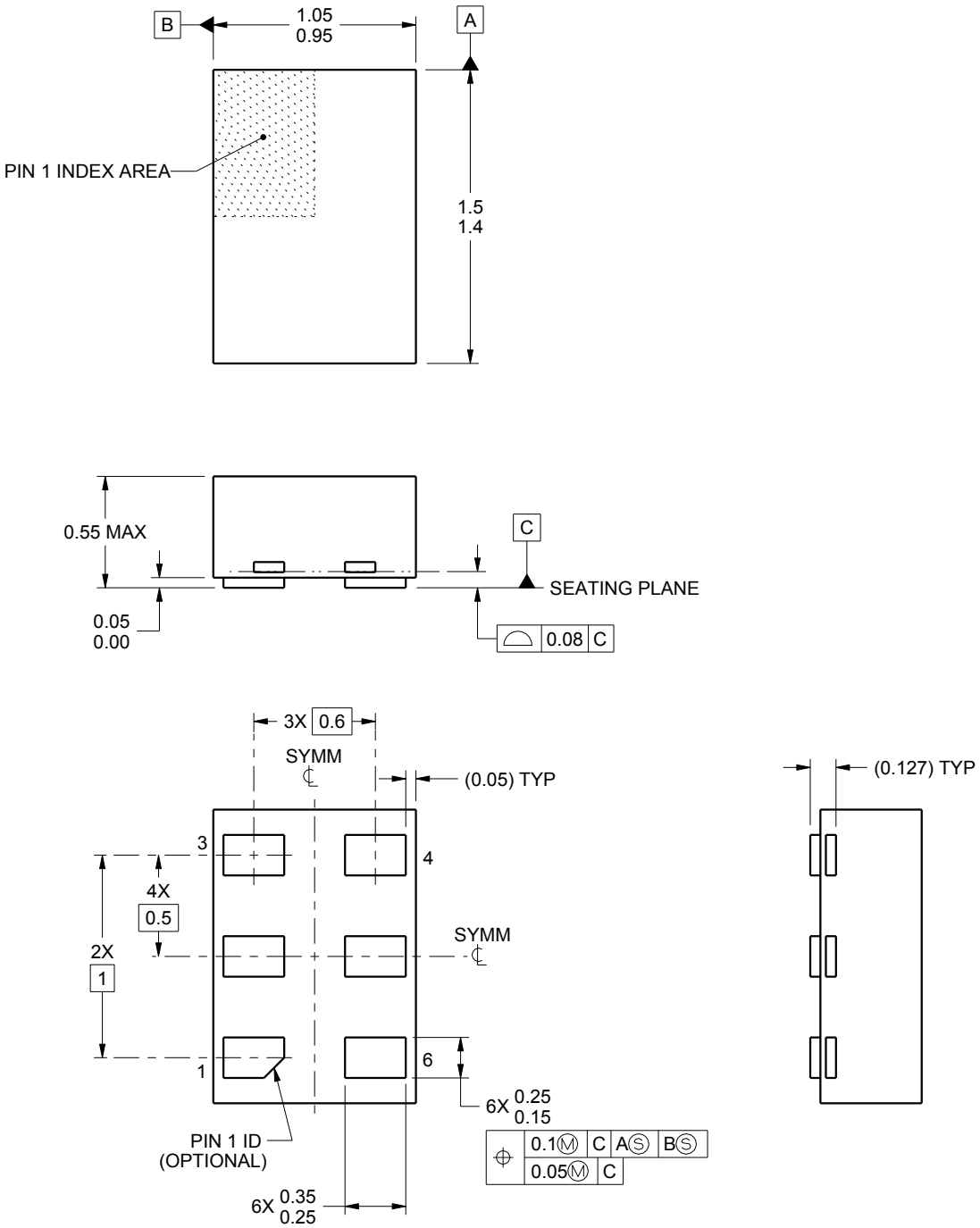
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DRY0006B

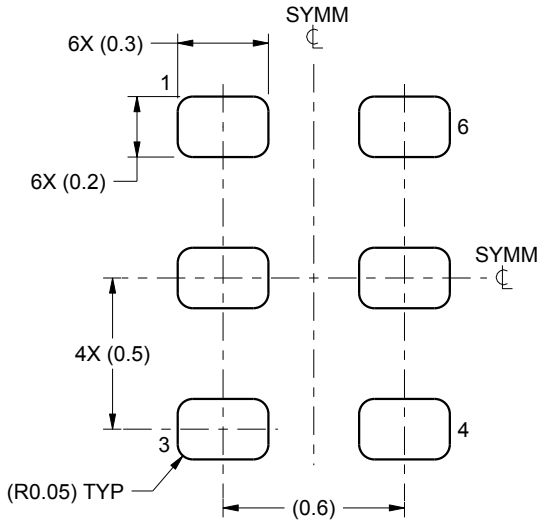
USON - 0.55 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

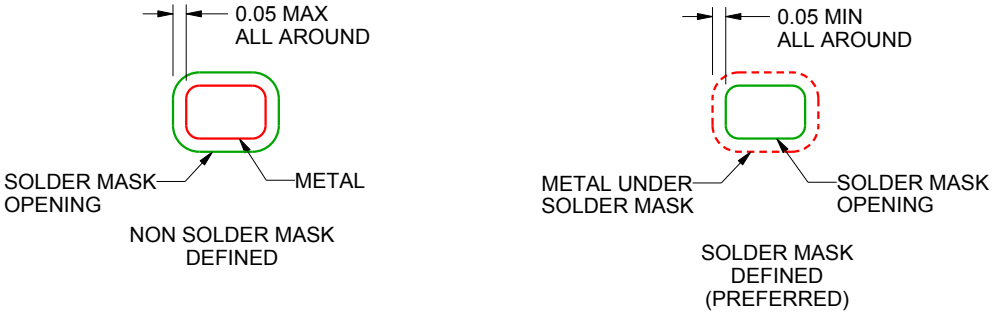


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
SCALE:40X



SOLDER MASK DETAILS

4222207/B 02/2016

NOTES: (continued)

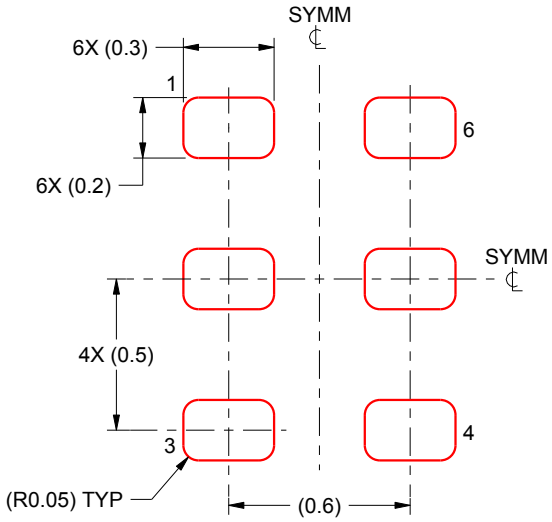
3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DRY0006B

USON - 0.55 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222207/B 02/2016

NOTES: (continued)

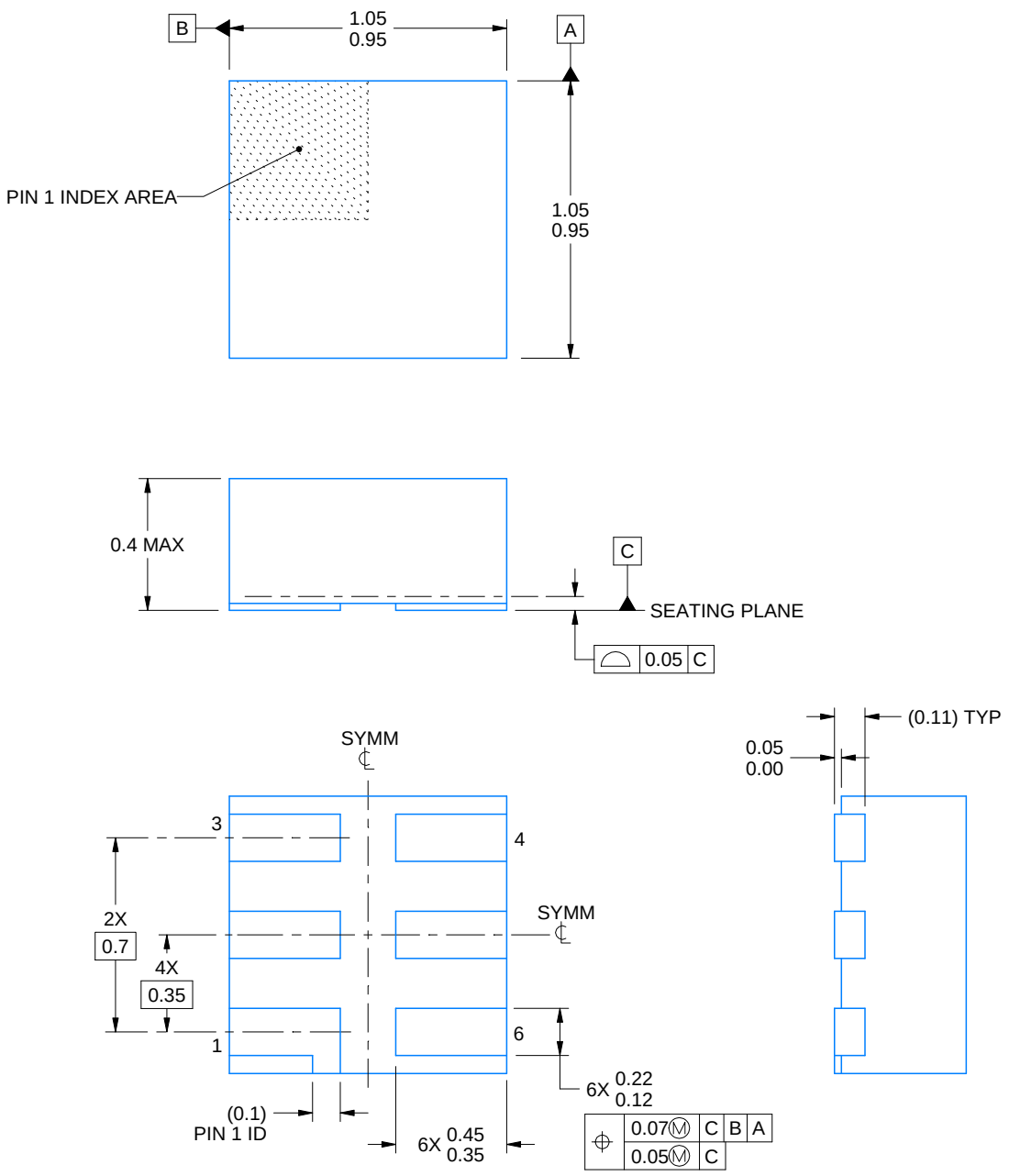
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DSF0006A

X2SON - 0.4 mm max height

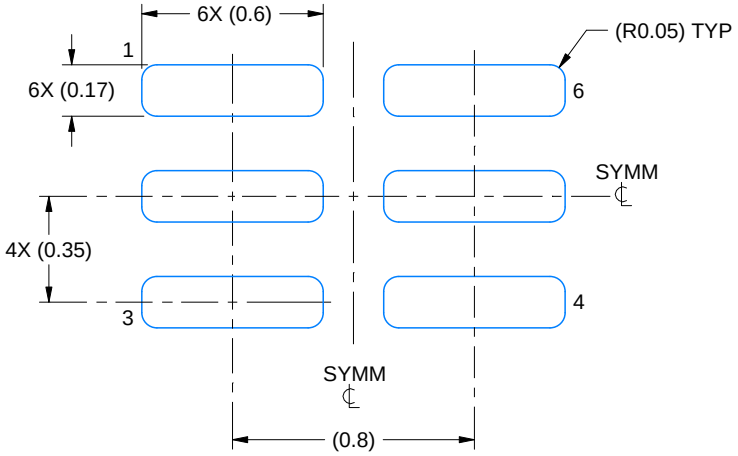
PLASTIC SMALL OUTLINE - NO LEAD



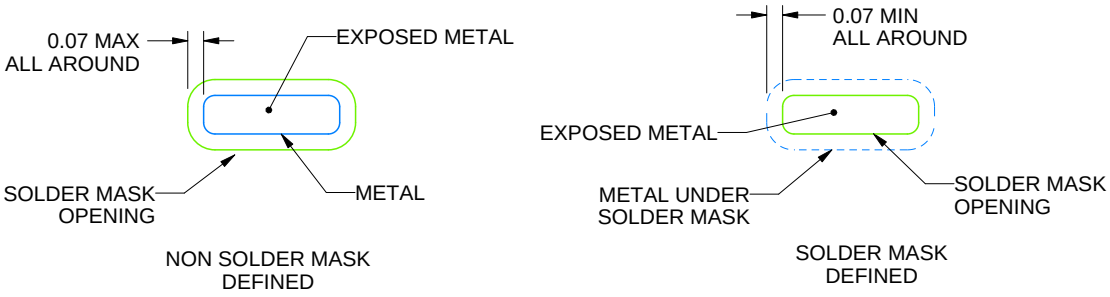
4220597/B 06/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-287, variation X2AAF.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4220597/B 06/2022

NOTES: (continued)

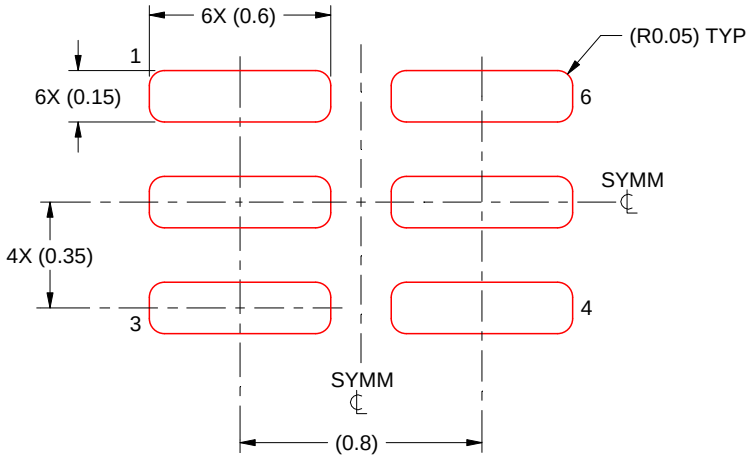
4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DSF0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.09 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:40X

4220597/B 06/2022

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

GENERIC PACKAGE VIEW

DPW 5 X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

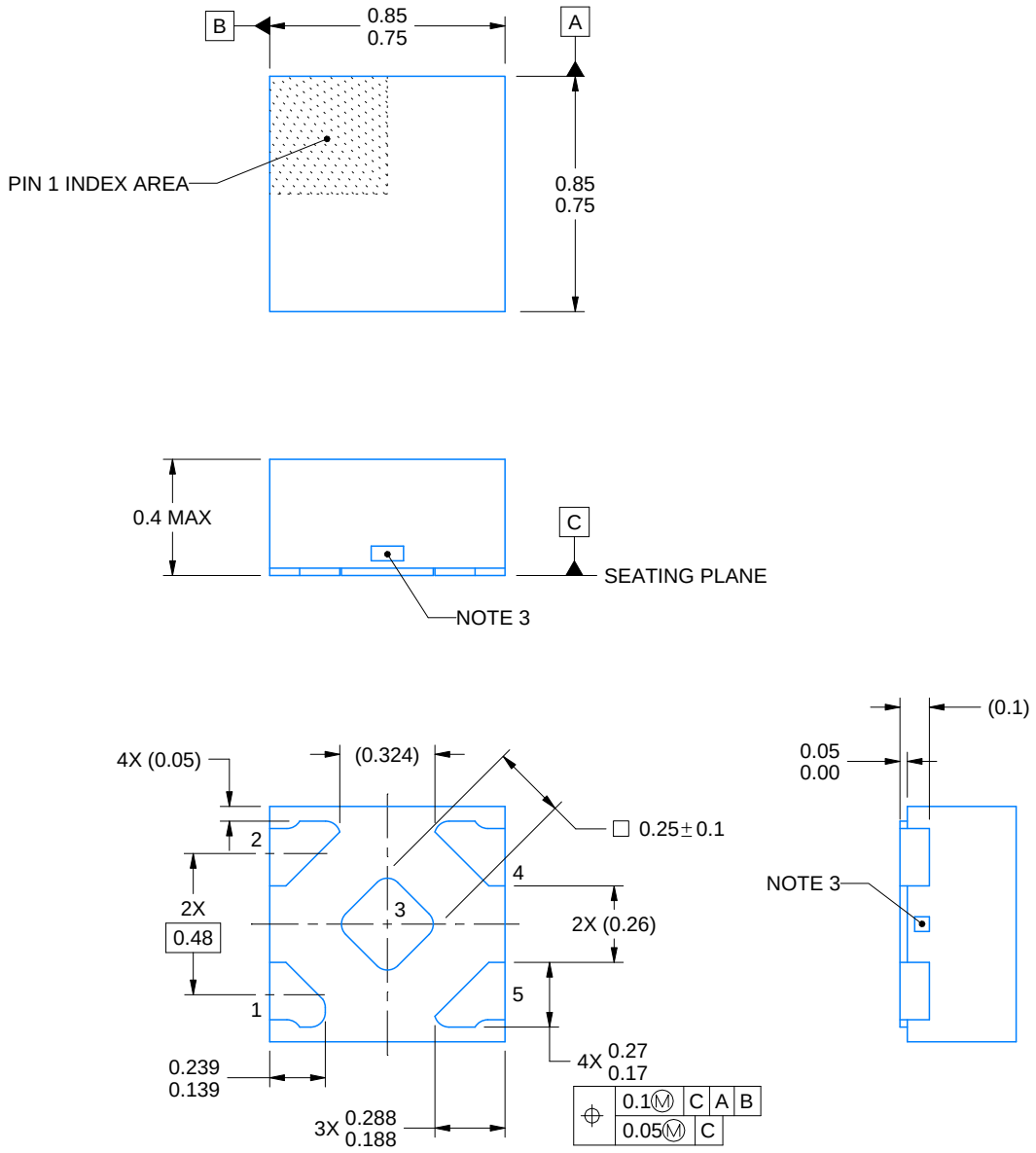
4211218-3/D

PACKAGE OUTLINE

DPW0005A

X2SON - 0.4 mm max height

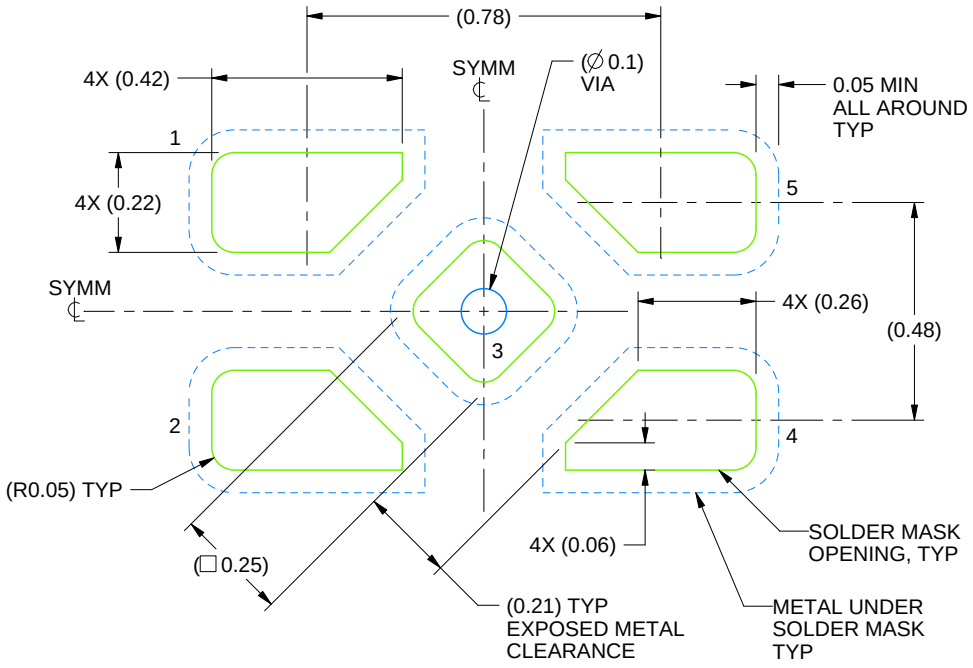
PLASTIC SMALL OUTLINE - NO LEAD



4223102/D 03/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The size and shape of this feature may vary.



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:60X

4223102/D 03/2022

NOTES: (continued)

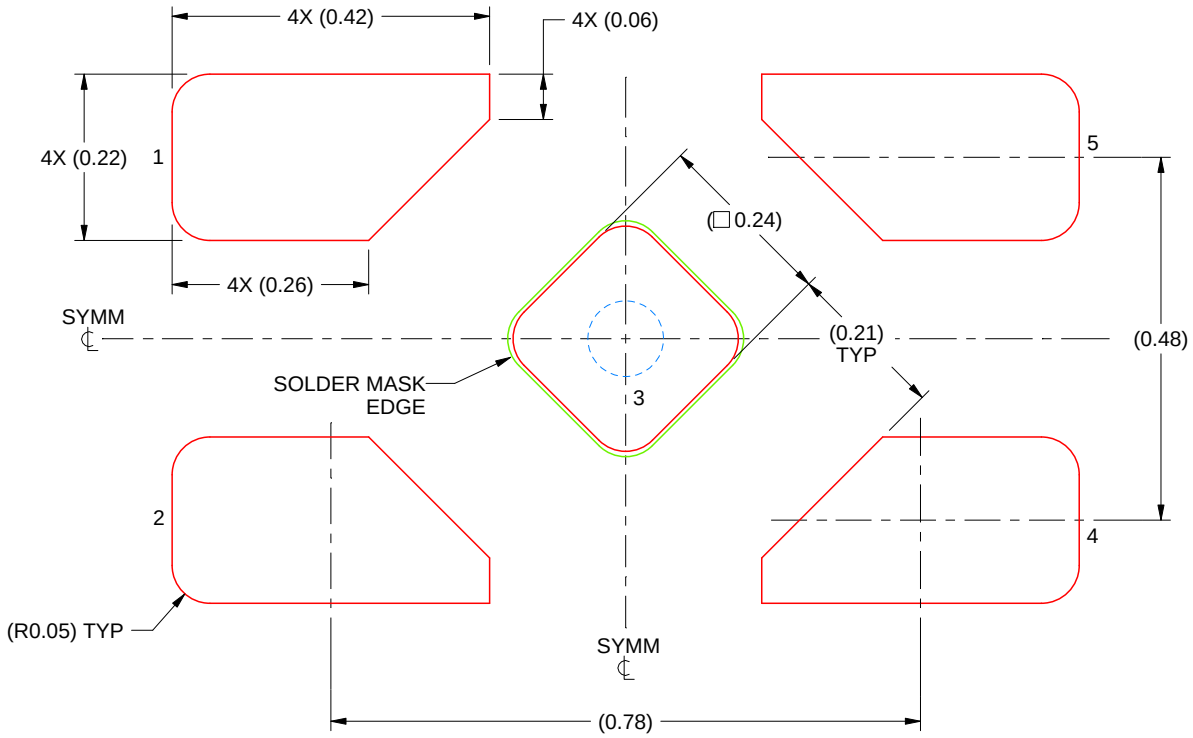
4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DPW0005A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 3
92% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:100X

4223102/D 03/2022

NOTES: (continued)

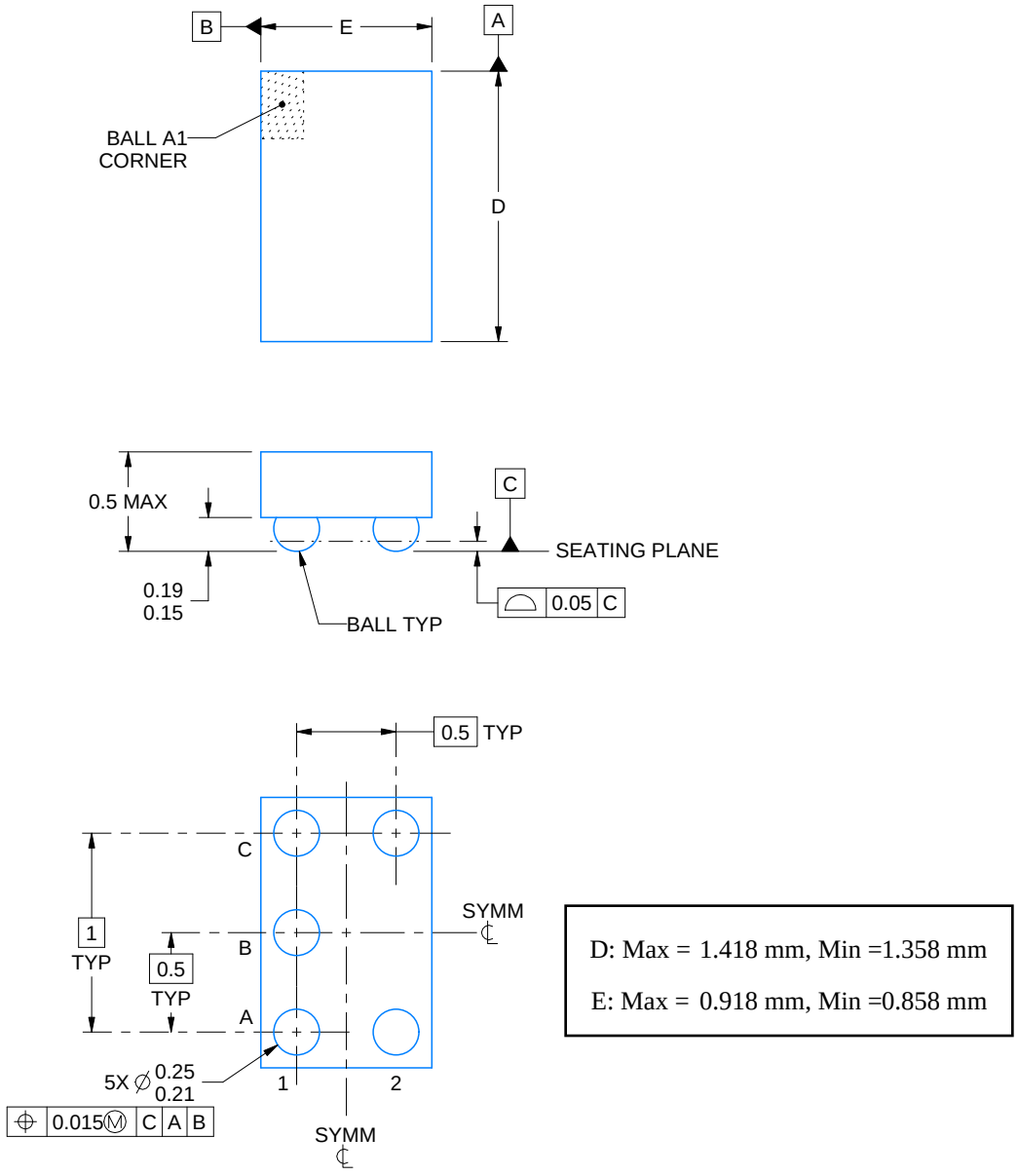
5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

YZP0005

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



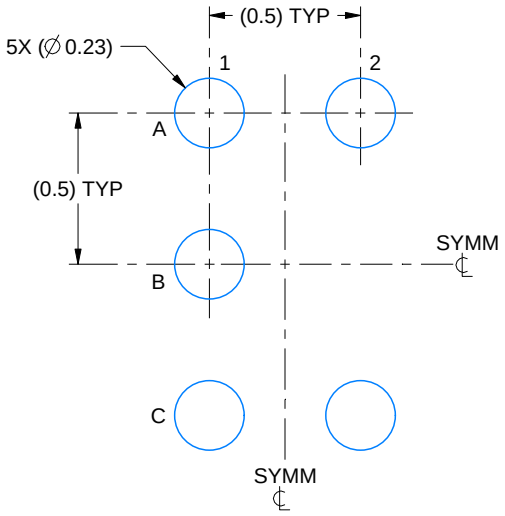
D: Max = 1.418 mm, Min =1.358 mm

E: Max = 0.918 mm, Min =0.858 mm

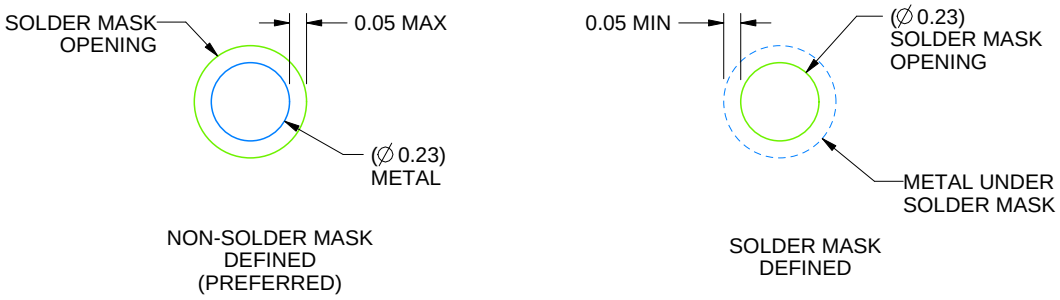
4219492/A 05/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:40X

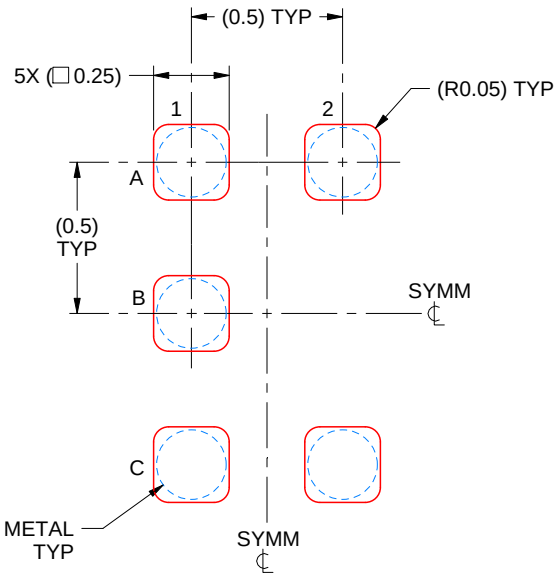


SOLDER MASK DETAILS
NOT TO SCALE

4219492/A 05/2017

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



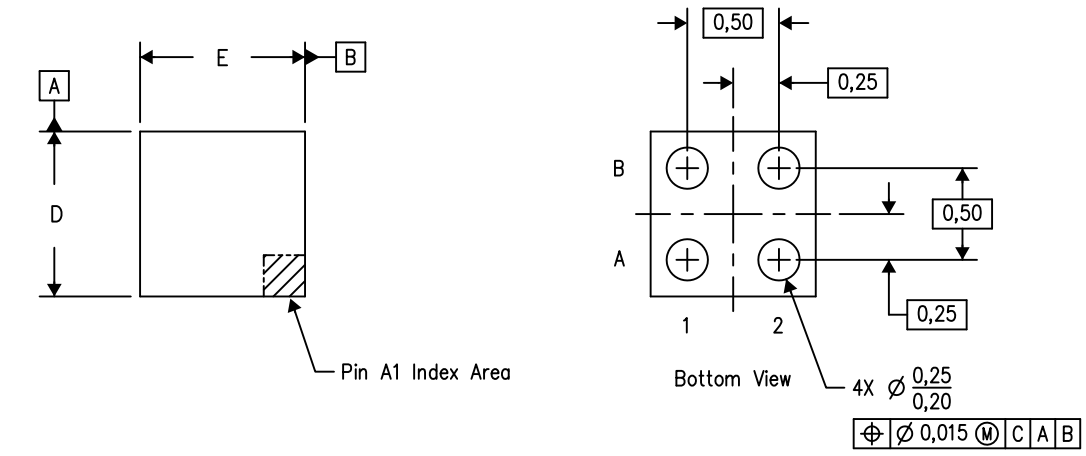
SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

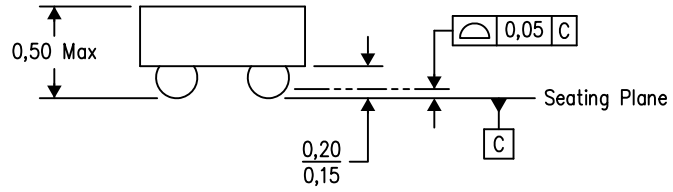
4219492/A 05/2017

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

YZV (S–XBGA–N4) DIE–SIZE BALL GRID ARRAY





D: Max = 0.918 mm, Min =0.858 mm

E: Max = 0.918 mm, Min =0.858 mm

4206083/C 07/13

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

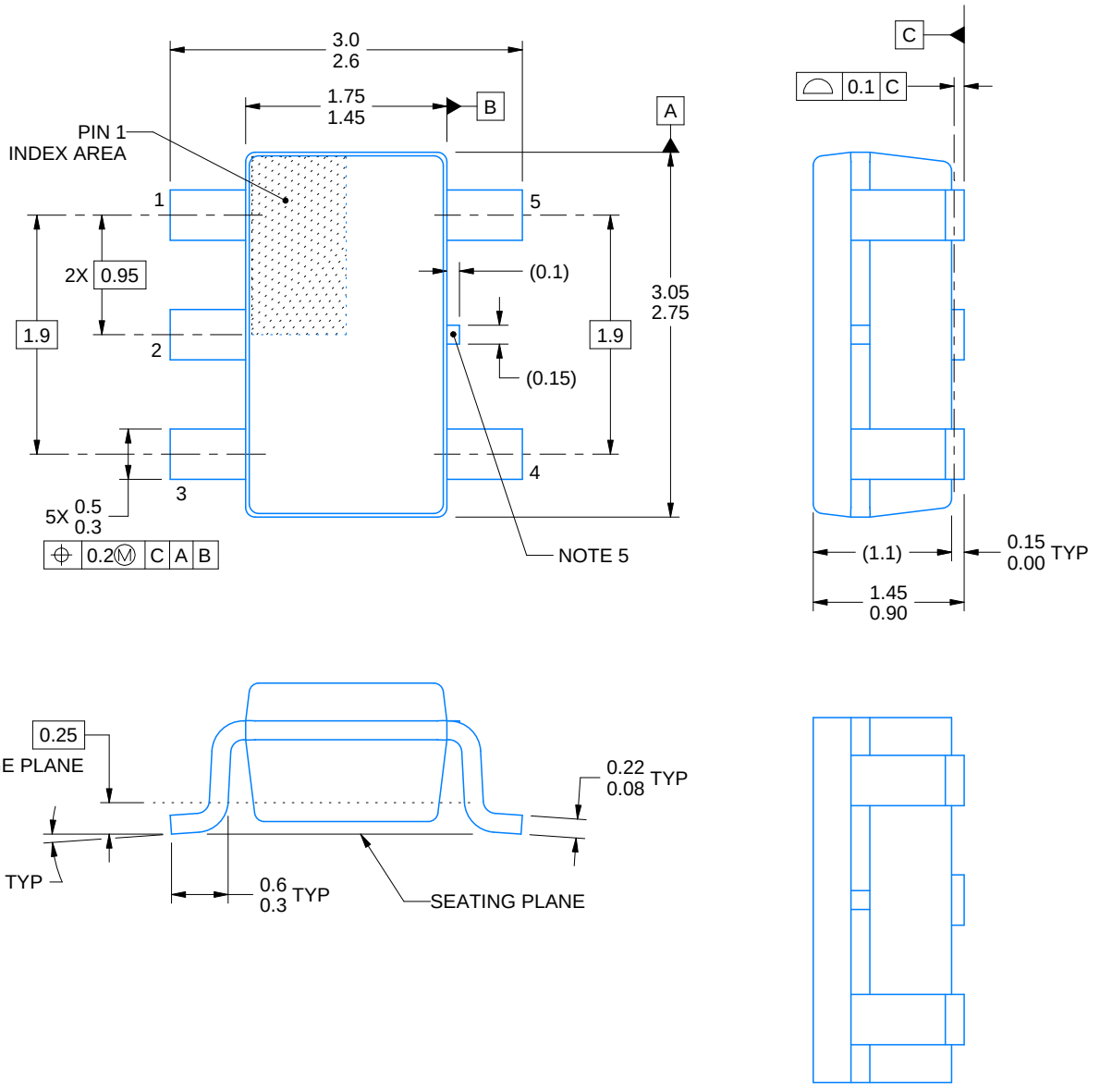
NanoFree is a trademark of Texas Instruments.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

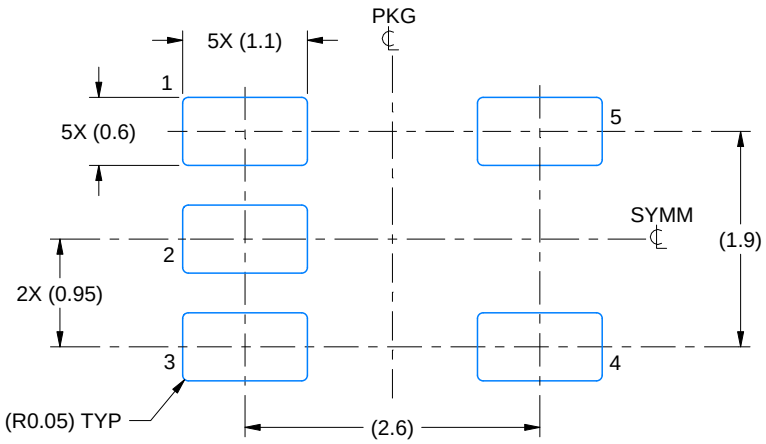


ALTERNATIVE PACKAGE SINGULATION VIEW

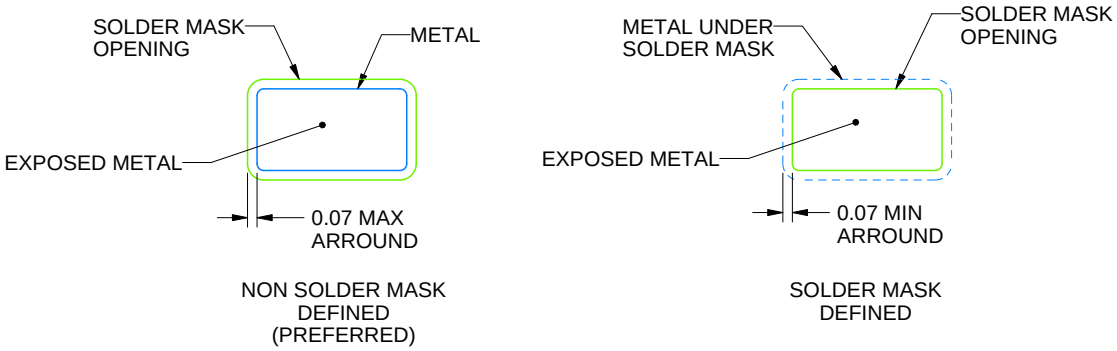
4214839/J 02/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

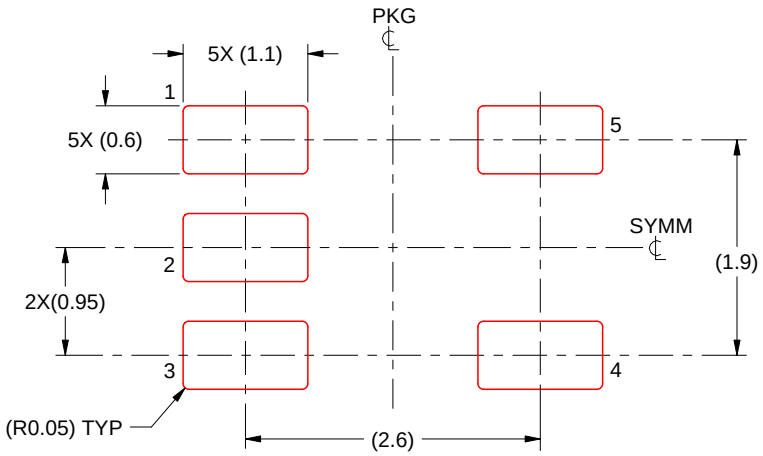


SOLDER MASK DETAILS

4214839/J 02/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/J 02/2024

NOTES: (continued)

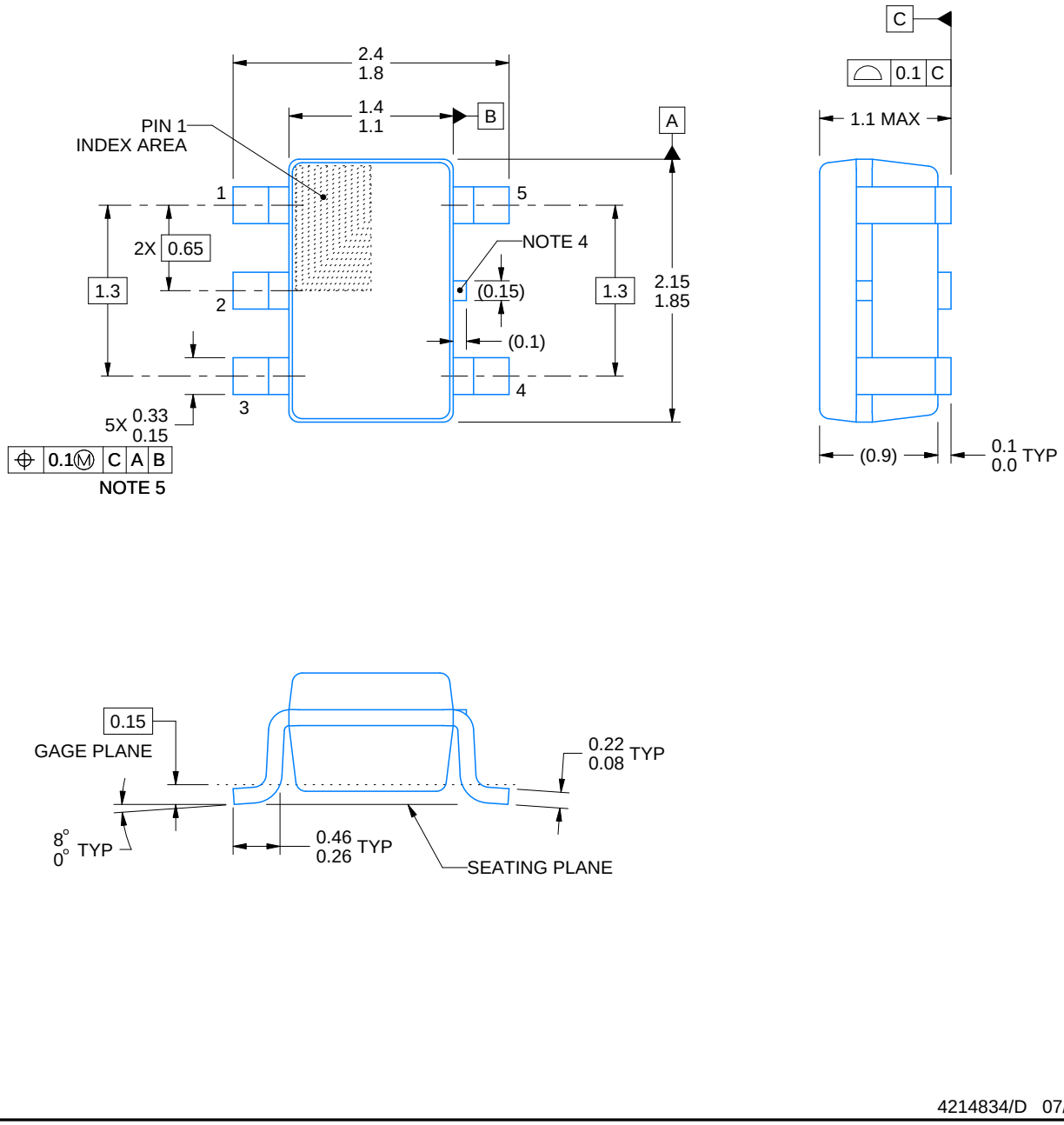
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

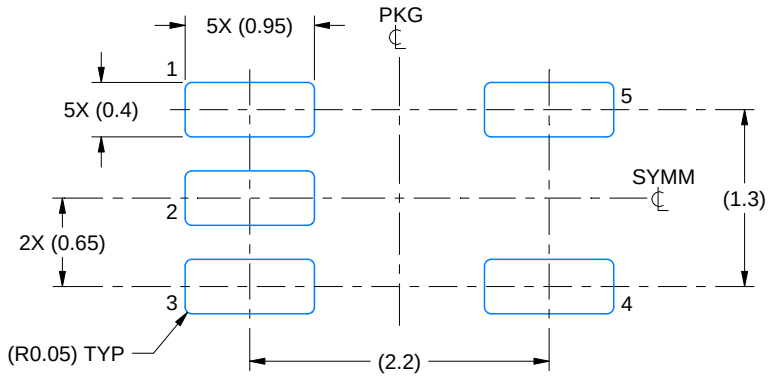
SMALL OUTLINE TRANSISTOR



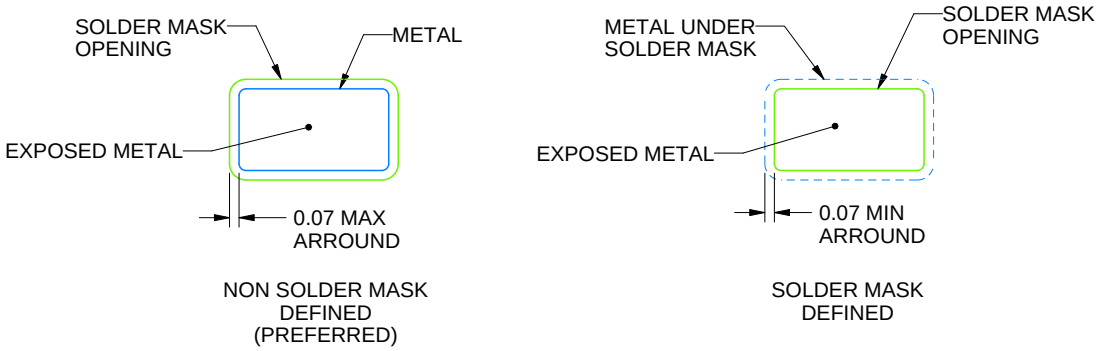
4214834/D 07/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

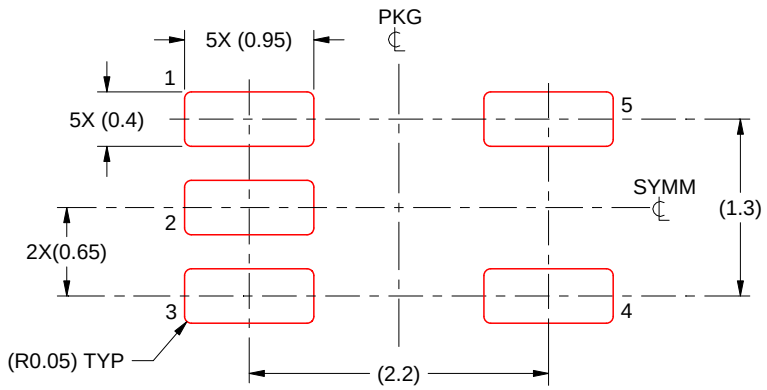


SOLDER MASK DETAILS

4214834/D 07/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/D 07/2023

NOTES: (continued)

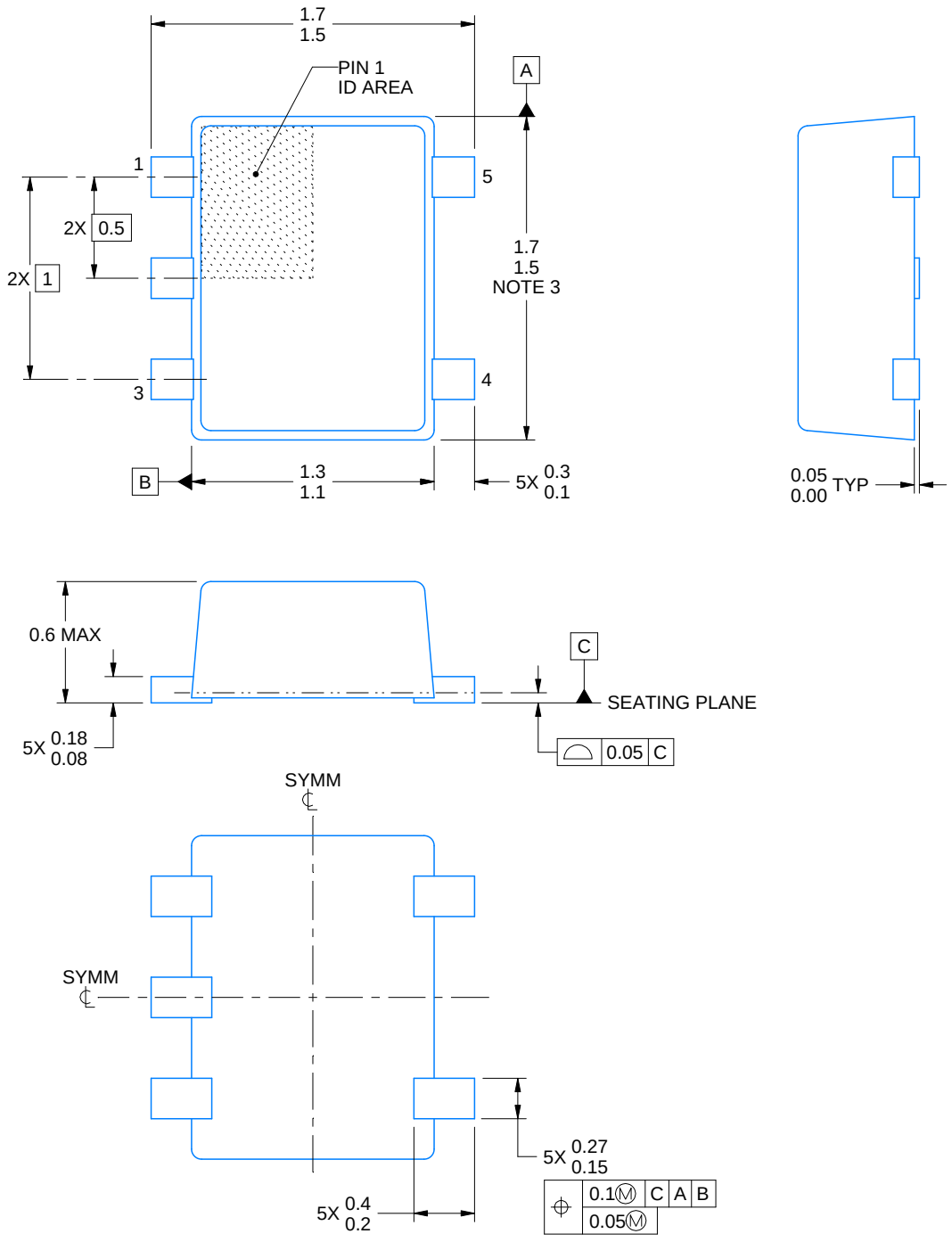
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DRL0005A

SOT - 0.6 mm max height

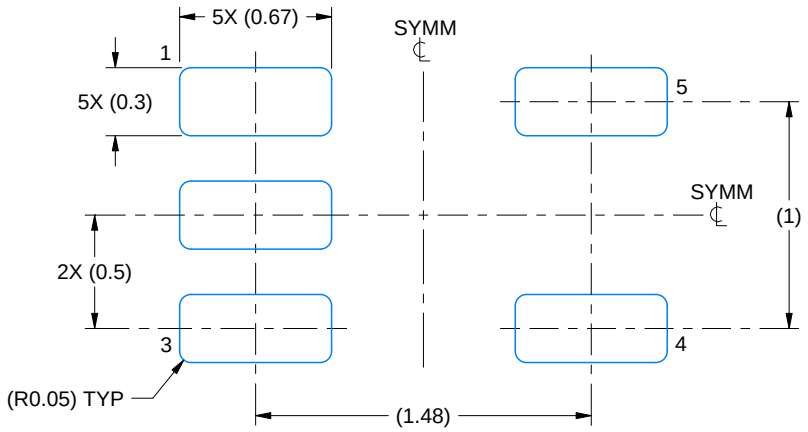
PLASTIC SMALL OUTLINE



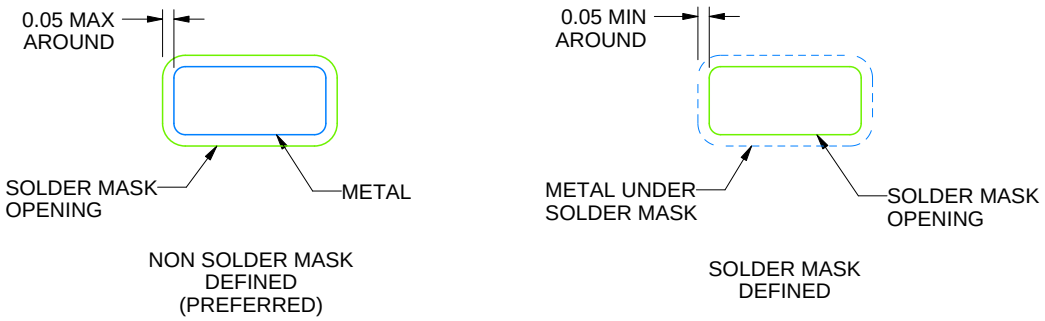
4220753/B 12/2020

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD-1



LAND PATTERN EXAMPLE
SCALE:30X

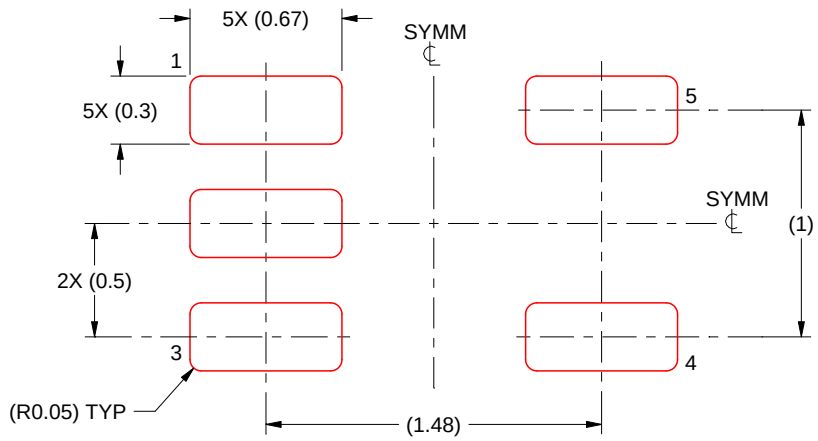


SOLDERMASK DETAILS

4220753/B 12/2020

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4220753/B 12/2020

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated