THS413x High-Speed, Low-Noise, Fully-Differential I/O Amplifiers

1 Features

- High performance
  - Bandwidth: 170 MHz (V_{CC} = ±15 V, G = 1 V/V)
  - Slew rate: 51 V/µs
  - Gain bandwidth product: 215 MHz
  - Distortion: –102 dBc THD at 2 V_{PP}, 250 kHz
- Voltage noise
  - 1/f voltage noise corner: 350 Hz
  - 1.25 nV/√Hz input-referred noise
- Single supply operating range: 5 V to 30 V
- Quiescent current (shutdown): 860 µA (THS4130)
- Temperature range: –40°C to +85°C
- Packages: PowerPAD™ HVSSOP-8, SOIC-8, VSSOP-8

2 Applications

- Single-ended to differential conversion
- Differential ADC driver
- Differential antialiasing
- Differential transmitter and receiver
- Output level shifter
- Medical ultrasound

3 Description

The THS4130 and THS4131 devices (THS413x) are a family of fully differential input/output amplifiers fabricated using Texas Instruments state-of-the-art, high-voltage, complementary, bipolar process.

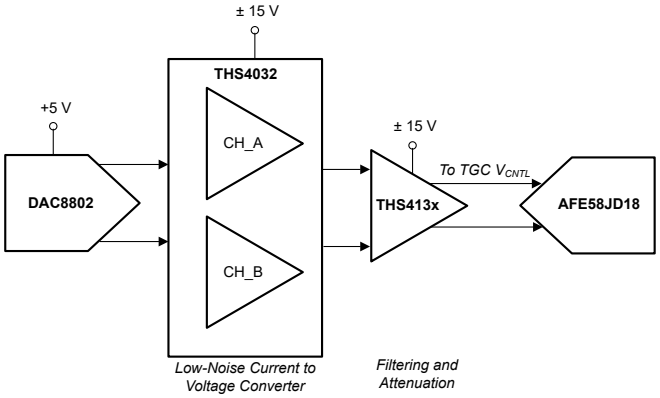
The THS413x use a true, fully differential signal path from input to output, and provide a high supply capability of up to ±15 V. This design leads to an excellent common-mode noise rejection performance (95 dB at 800 kHz) and total harmonic distortion (−102 dBc at 2 V_{PP}, 250 kHz). The wide supply range allows high-voltage differential signal chains to benefit from the improved headroom and dynamic range without adding separate amplifiers for each polarity of the differential signal.

The THS413x are characterized for operation over the wide temperature range of –40°C to +85°C.

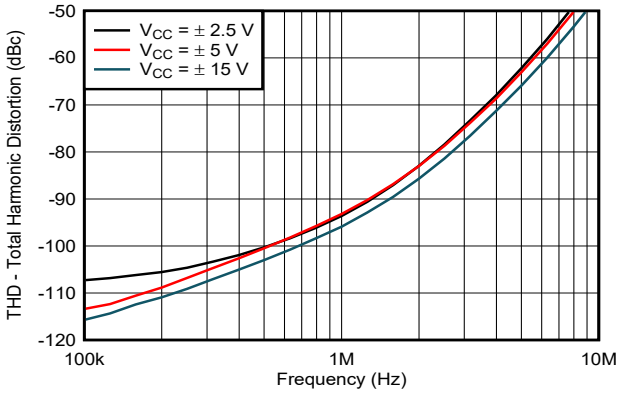
Device Information

PART NUMBER(1)	POWER DOWN PIN	PACKAGE(2)
THS4130	Yes	D, (SOIC, 8), DGK (VSSOP, 8), DGN (HVSSOP, 8)
THS4131	No	

(1) See the *Device Comparison Table*.
(2) For all available packages, see the orderable addendum at the end of the data sheet.



Time Gain Control DAC Reference for Ultrasound



V_{OUT} = 2 V_{PP}

Total Harmonic Distortion vs Frequency

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision K (August 2022) to Revision L (August 2023) **Page**

- Changed MSOP and MSOP-PowerPad to VSSOP and HVSSOP in Thermal Information table....4
- Changed thermal specifications for DGN package in *Thermal Information* table....4
- Changed the Electrical Characteristics section to combine both Electrical Characteristics tables into one table with improved small-signal bandwidth, slew rate, settling time, total harmonic distortion (THD), spurious-free dynamic range (SFDR), voltage noise, offset voltage drift, output swing, and quiescent current parameters for the DGN package....5
- Changed input current noise typical from 1.3 pA/√Hz to 1.7 pA/√Hz for DGN package....5
- Changed common-mode input offset voltage maximum from 3.5 mV to 5.5 mV for DGN package....5
- Changed maximum input bias current from 6 µA to 15.4 µA for DGN package....5
- Changed single input resistance parameter into seperate common-mode and differential input resistance parameters for DGN package....5
- Changed *Typical Characteristics: THS413xD, THS413xDGK* title to *Typical Characteristics* and deleted obsolete *Typical Characteristics: THS413xDGN* section; all plots now in one section....7

Changes from Revision J (March 2022) to Revision K (August 2022) **Page**

- Updated thermal specifications for DGK package in *Thermal Information* table....4
- Changed title of *Electrical Characteristics: THS413xD* to *Electrical Characteristics: THS413xD, THS413xDGK*....5
- Changed title of *Typical Characteristics: THS413xD* to *Typical Characteristics: THS413xD, THS413xDGK*....7

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5 Device Comparison Table

T_A	D (SOIC, 8)	DGK (VSSOP, 8)	DGN (HVSSOP, 8)
0°C to +70°C	THS4130CD	THS4130CDGK	THS4130CDGN
	THS4131CD	THS4131CDGK	THS4131CDGN
–40°C to +85°C	THS4130ID	THS4130IDGK	THS4130IDGN
	THS4131ID	THS4131IDGK	THS4131IDGN

6 Pin Configuration and Functions

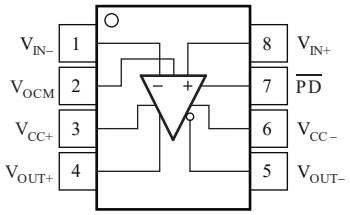

Figure 6-1. D Package, 8-Pin SOIC, DGK Package, 8-pin VSSOP, DGN Package, 8-Pin HVSSOP THS4130 (Top View)

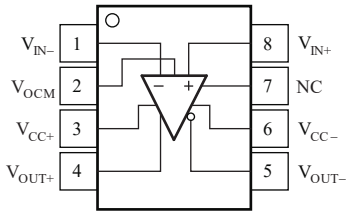

Figure 6-2. D Package, 8-Pin SOIC, DGK Package, 8-pin VSSOP, DGN Package, 8-Pin HVSSOP THS4131 (Top View)

Table 6-1. Pin Functions

PIN			TYPE(1)	DESCRIPTION
NAME	NO.			
	THS4130	THS4131		
NC	—	7	—	No connect
$\overline{PD}$	7	—	I	Active low power-down pin
V_{CC+}	3	3	I/O	Positive supply voltage pin
$V_{CC–}$	6	6	I/O	Negative supply voltage pin
$V_{IN–}$	1	1	I	Negative input pin
V_{OCM}	2	2	I	Common mode input pin
V_{OUT+}	4	4	O	Positive output pin
$V_{OUT–}$	5	5	O	Negative output pin
V_{IN+}	8	8	I	Positive input pin
Thermal Pad	Thermal Pad	Thermal Pad	—	Thermal pad. DGN (HVSSOP) package only. For the best thermal performance, connect the thermal pad to a large copper plane. This pad is electrically isolated from the die so the pad can be connected to any pin on the package.

(1) I = input, O = output.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_I	Input voltage		$-V_{CC}$	$+V_{CC}$	V
V_{CC-} to V_{CC+}	Supply voltage			33	V
	Supply turn on and turn off dV/dT(2)			1.7	V/µs
I_O	Output current(3)			150	mA
V_{ID}	Differential input voltage		−1.5	1.5	V
I_{IN}	Continuous input current			10	mA
T_J	Junction temperature			150	°C
	Junction temperature, continuous operation, long-term reliability(4)			125	°C
T_A	Ambient temperature	C-suffix	0	70	°C
		I-suffix	–40	85	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If briefly operating outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Stay below this specification to make sure that the edge-triggered ESD absorption devices across the supply pins remain off.
(3) Some of the THS413x packages incorporate a thermal pad on the underside of the chip. This thermal pad acts as a heat sink and must be connected to a thermally dissipative plane for proper power dissipation. Failure to do so can result in exceeding the maximum junction temperature which can permanently damage the device. See TI technical briefs SLMA002 and SLMA004 for more information about using the PowerPAD integrated circuit package.
(4) The maximum junction temperature for continuous operation is limited by package constraints. Operation greater than this temperature can result in reduced reliability, reduced lifetime of the device, or both.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	Dual supply	±2.5		±15	V
		Single supply	5		30	
T_A	Operating free-air temperature	C-suffix device	0		70	°C
		I-suffix device	–40		85	

7.4 Thermal Information

THERMAL METRIC(1)		THS413x			UNIT
		D (SOIC)	DGK (VSSOP)	DGN (HVSSOP)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	126.3	147.3	57.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	67.3	37.9	76.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	69.8	83.2	30.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	19.5	0.9	4.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	69.0	81.6	29.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	14.3	°C/W

(1) For information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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7.5 Electrical Characteristics

at V_{CC} = ±5 V, gain = 1 V/V, R_F = 390 Ω, R_L = 800 Ω, and T_A = +25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DYNAMIC PERFORMANCE							
SSBW	Small-signal bandwidth (–3 dB)	V_I = 63 mV_{PP}, gain = 1, R_F = 390 Ω, single-ended input, differential output	V_{CC} = 5 V		165		MHz
			V_{CC} = ±5 V		166		
			V_{CC} = ±15 V		170		
		V_I = 63 mV_{PP}, gain = 2, R_F = 750 Ω, single-ended input, differential output	V_{CC} = 5 V		97		
			V_{CC} = ±5 V		98		
			V_{CC} = ±15 V		100		
SR	Slew rate(2)				67		V/µs
t_s	Settling time	To 0.1%	Step voltage = 2 V, gain = 1		39		ns
		To 0.01%	Step voltage = 2 V, gain = 1		61		
DISTORTION PERFORMANCE							
THD	Total harmonic distortion	V_{CC} = 5 V, V_O = 2 V_{PP}, differential input/output	f = 250 kHz		–101		dBc
			f = 1 MHz		–87		
		V_{CC} = ±5 V, V_O = 2 V_{PP}, differential input/output	f = 250 kHz		–100		
			f = 1 MHz		–87		
		V_{CC} = ±15 V, V_O = 2 V_{PP}, differential input/output	f = 250 kHz		–102		
			f = 1 MHz		–88		
		V_{CC} = ±5 V, V_O = 4 V_{PP}, differential input/output	f = 250 kHz		–94		
			f = 1 MHz		–79		
		V_{CC} = ±15 V, V_O = 4 V_{PP}, differential input/output	f = 250 kHz		–95		
			f = 1 MHz		–80		
SFDR	Spurious-free dynamic range	V_O= 2 V_{PP}, f = 250 kHz, differential input/output	V_{CC} = ±2.5		103		dBc
			V_{CC} = ±5		106		
			V_{CC} = ±15		108		
		V_O = 4 V_{PP}, f = 250 kHz, differential input/output	V_{CC} = ±5		98		
			V_{CC} = ±15		100		
IMD3	Third intermodulation distortion	$V_{I(PP)}$ = 4 V, F_1 = 3 MHz, F_2 = 3.5 MHz			–53		dBc
OIP3	Third-order intercept	$V_{I(PP)}$ = 4 V, F_1 = 3 MHz, F_2 = 3.5 MHz			41.5		dB
NOISE PERFORMANCE							
V_n	Input voltage noise	f = 10 kHz			1.25		nV/√Hz
I_n	Input current noise	f = 10 kHz			1.7		pA/√Hz
DC PERFORMANCE							
A_{OL}	Open-loop gain	T_A = 25°C		71	78		dB
		T_A = full range		69			
V_{OS}	Input offset voltage	T_A = 25°C			±0.2	2	mV
		T_A = full range(1)				3	
	Common-mode input offset voltage	Referred to V_{OCM}			0.2	5.5	mV
	Input offset voltage drift	T_A = full range(1)			2		µV/°C
I_{IB}	Input bias current	T_A = full range(1)			5	15.4	µA
I_{OS}	Input offset current	T_A = full range(1)			100	500	nA
	Input offset current drift				1		nA/°C
INPUT CHARACTERISTICS							

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7.5 Electrical Characteristics (continued)

at V_{CC} = ±5 V, gain = 1 V/V, R_F = 390 Ω, R_L = 800 Ω, and T_A = +25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
CMRR	Common-mode rejection ratio	T_A = full range(1)		80	95		dB
V_{ICM}	Common-mode input voltage			–3.77 to 4.3	–4 to 4.5		V
R_{I_CM}	Common-mode input resistance	Measured into each input pin			215		MΩ
R_{I_DIFF}	Differential input resistance	Measured into each input pin			10		kΩ
C_{I_CM}	Common-mode input capacitance	Measured into each input pin, closed loop			1.4		pF
C_{I_DIFF}	Differential input capacitance	Measured into each input pin, closed loop			2.5		
OUTPUT CHARACTERISTICS							
R_O	Output resistance	Open loop			41		Ω
	Output voltage swing	V_{CC} = 5 V, R_L = 1 kΩ	T_A = 25°C	1.2 to 3.8	0.9 to 4.1		V
			T_A = full range(1)	1.3 to 3.7	±4		
		V_{CC} = ±5 V, R_L = 1 kΩ	T_A = 25°C	±3.7			
			T_A = full range(1)	±3.6			
		V_{CC} = ±15 V, R_L = 1 kΩ	T_A = 25°C	±11.5	±12.4		
			T_A = full range(1)	±11.2			
I_O	Output current	V_{CC} = 5 V, R_L = 7 Ω	T_A = 25°C	25	45		mA
			T_A = full range	20			
		V_{CC} = ±5 V, R_L = 7 Ω	T_A = 25°C	30	55		
			T_A = full range(1)	28			
		V_{CC} = ±15 V, R_L = 7 Ω	T_A = 25°C	65	85		
			T_A = full range(1)	60			
POWER SUPPLY							
I_{CC}	Quiescent current	V_{CC} = ±5 V	T_A = 25°C		10.4	15	mA
			T_A = full range(1)			16	
		V_{CC} = ±15 V	T_A = 25°C		13		
$I_{CC(SD)}$	Quiescent current (shutdown) (THS4130 only)	$\overline{PD}$ = –5 V	T_A = 25°C		0.86	1.4	mA
			T_A = full range(1)			1.5	
PSRR	Power-supply rejection ratio (dc)		T_A = +25°C	73	98		dB
			T_A = full range(1)	70			

(1) The full range temperature is 0°C to +70°C for the C-suffix device, and –40°C to +85°C for the I-suffix device.
(2) Slew rate is measured from an output level range of 25% to 75%.

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7.6 Typical Characteristics

at T_A = 25°C, V_{CC} = ±5 V, R_F = 390 Ω, gain = +1 V/V, differential input, differential output, and R_L = 800 Ω (unless otherwise noted)

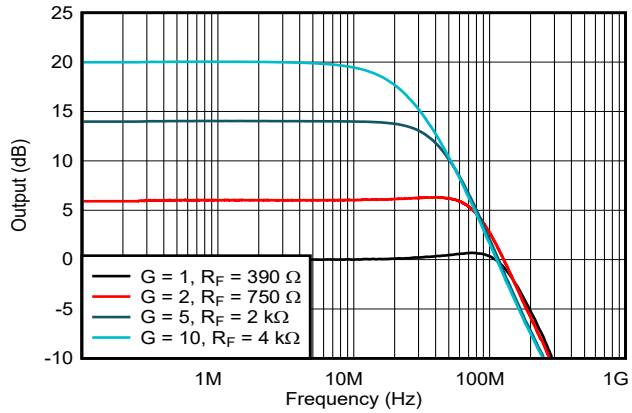


Figure 7-1. Small-Signal Frequency Response

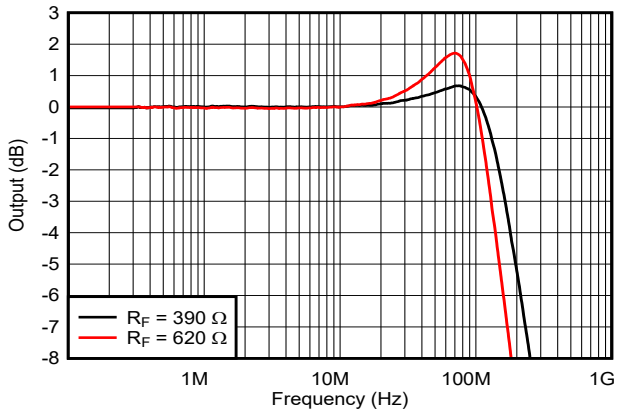


Figure 7-2. Small-Signal Frequency Response

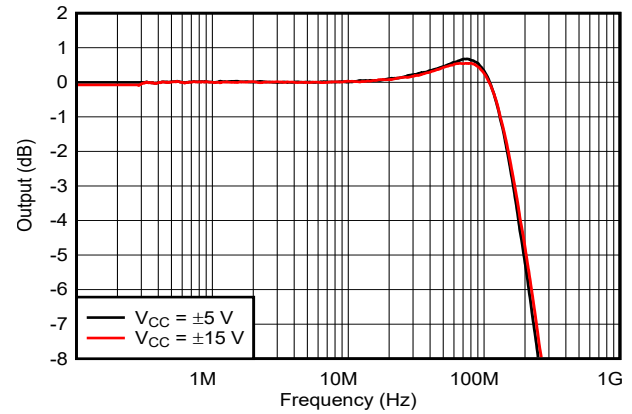


Figure 7-3. Small-Signal Frequency Response

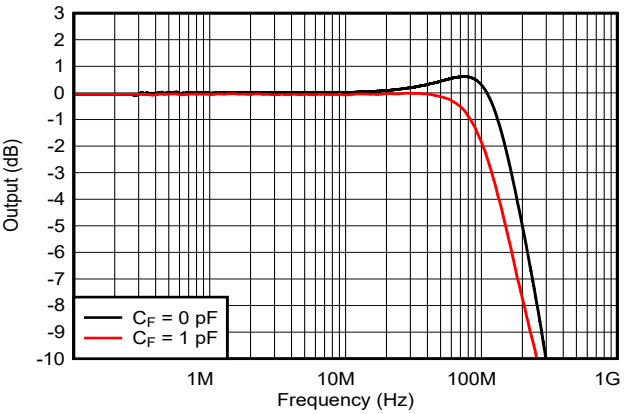


Figure 7-4. Small-Signal Frequency Response

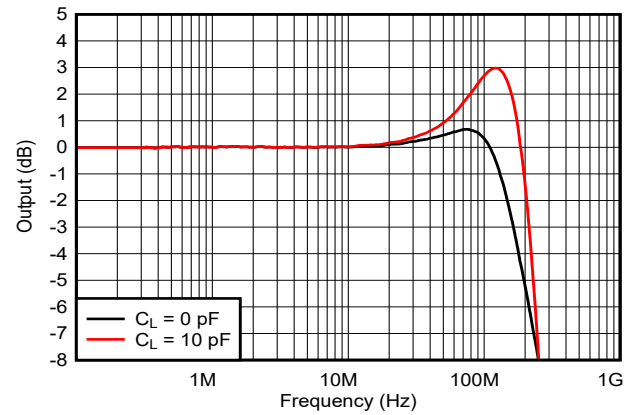


Figure 7-5. Small-Signal Frequency Response

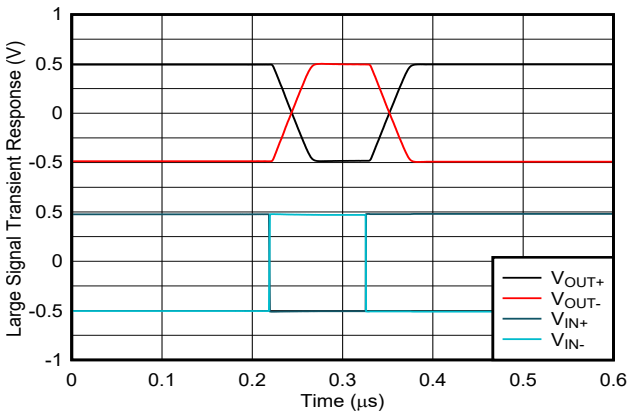
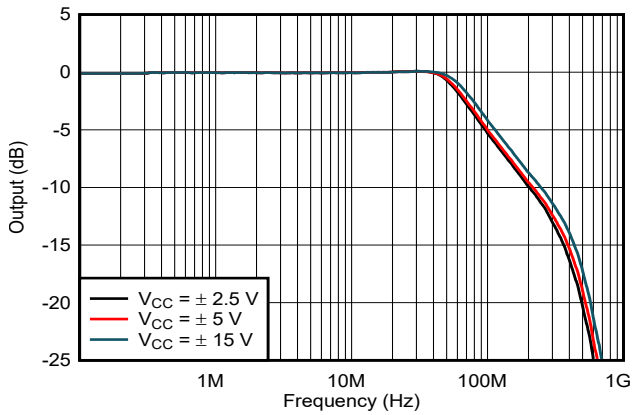


Figure 7-6. Large-Signal Transient Response (Differential In/ Single Out)

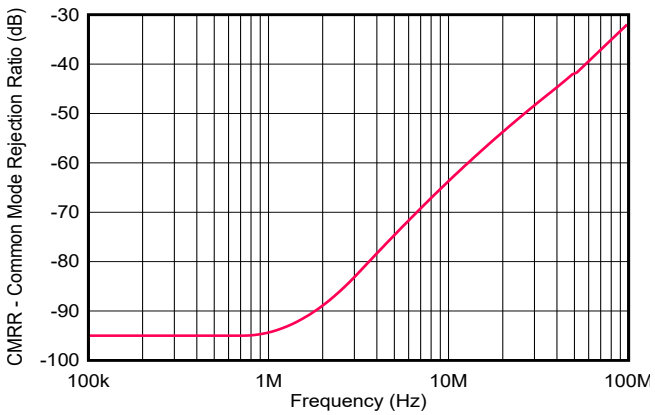
7.6 Typical Characteristics (continued)

at T_A = 25°C, V_{CC} = ±5 V, R_F = 390 Ω, gain = +1 V/V, differential input, differential output, and R_L = 800 Ω (unless otherwise noted)



V_I = 0.2 V_{RMS}

Figure 7-7. Large-Signal Frequency Response



R_F = 1 kΩ

Figure 7-8. Common-Mode Rejection Ratio vs Frequency

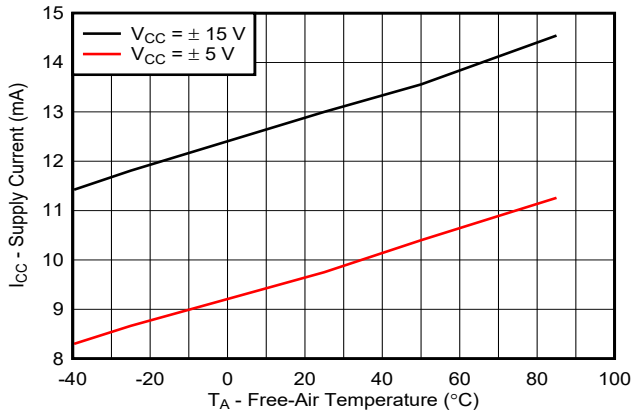


Figure 7-9. Supply Current vs Free-Air Temperature

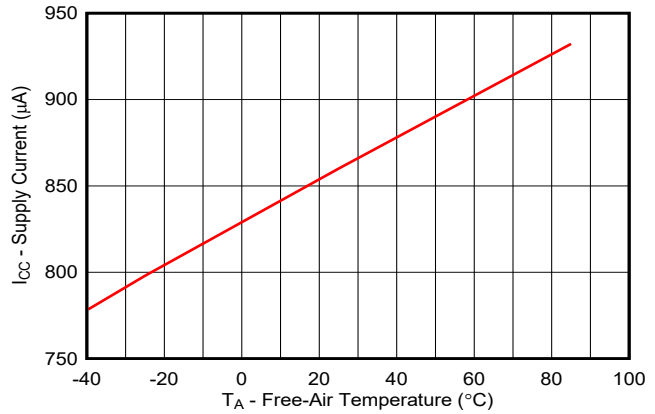


Figure 7-10. Supply Current vs Free-Air Temperature (Shutdown State)

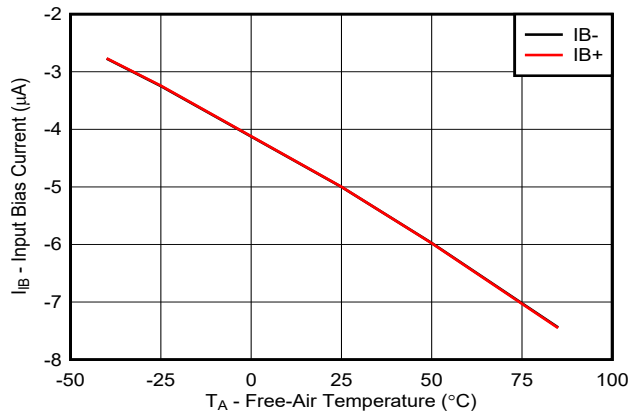
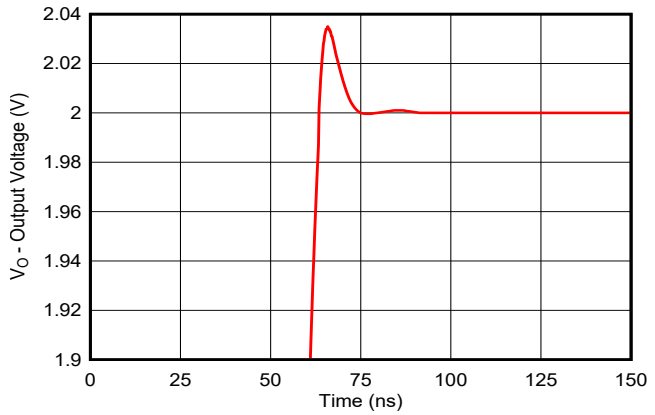


Figure 7-11. Input Bias Current vs Free-Air Temperature



R_F = 510 Ω, C_F= 1 pF, V_{CC}= 5 V, V_O = 4 V_{PP}

Figure 7-12. Settling Time

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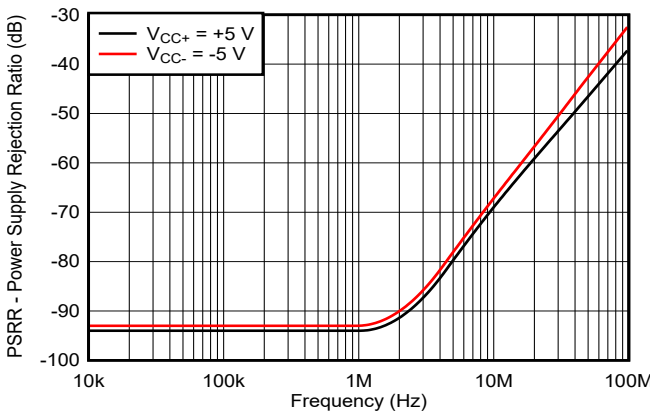
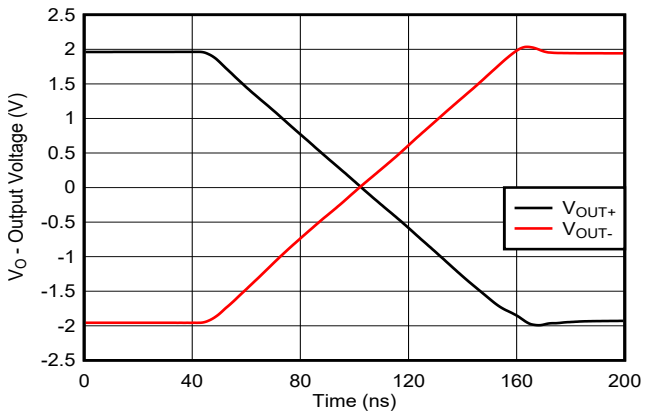
7.6 Typical Characteristics (continued)

at T_A = 25°C, V_{CC} = ±5 V, R_F = 390 Ω, gain = +1 V/V, differential input, differential output, and R_L = 800 Ω (unless otherwise noted)



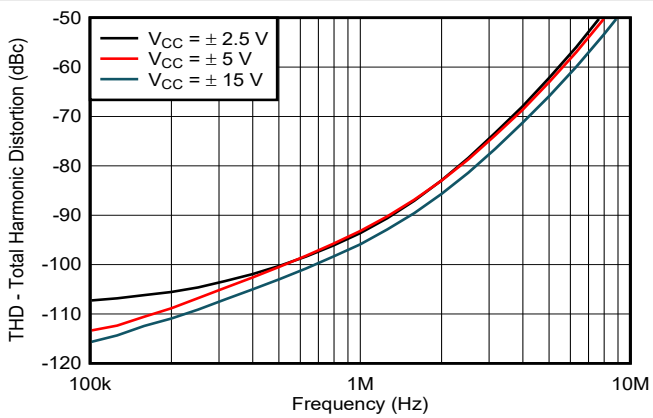
R_F = 330 Ω, R_L = 400 Ω

Figure 7-13. Power-Supply Rejection Ratio vs Frequency (Differential Out)



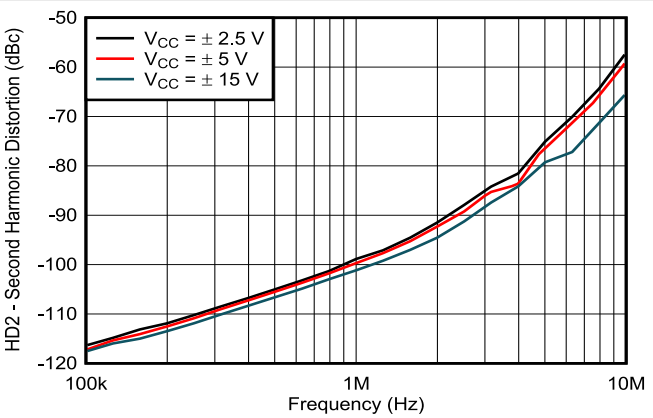
V_{I_Peak} = 2 V, C_L = 10 pF, V_{CC} = ±15 V

Figure 7-14. Large-Signal Transient Response



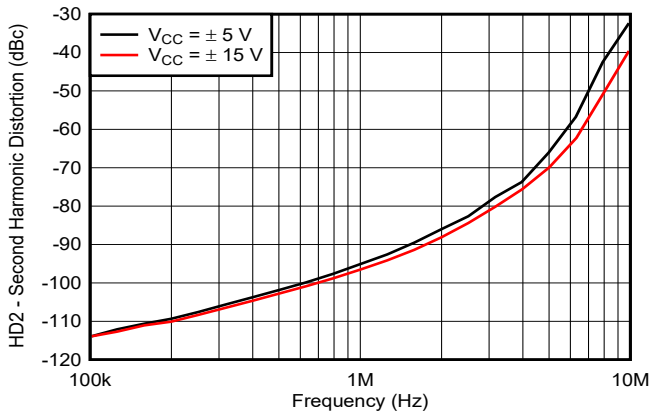
V_{OUT} = 2 V_{PP}

Figure 7-15. Total Harmonic Distortion vs Frequency



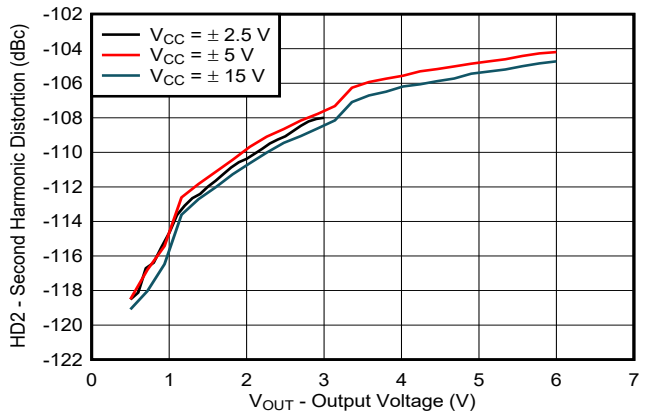
V_{OUT} = 2 V_{PP}, single-ended input, differential output

Figure 7-16. Second-Harmonic Distortion vs Frequency



V_{OUT} = 4 V_{PP}, single-ended input, differential output

Figure 7-17. Second-Harmonic Distortion vs Frequency

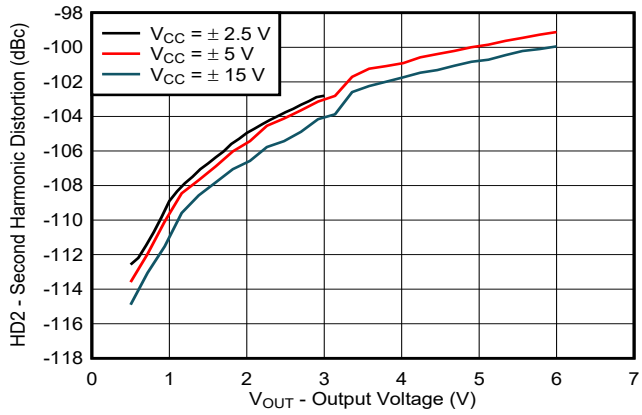


f = 250 kHz, single-ended input, differential output

Figure 7-18. Second-Harmonic Distortion vs Output Voltage

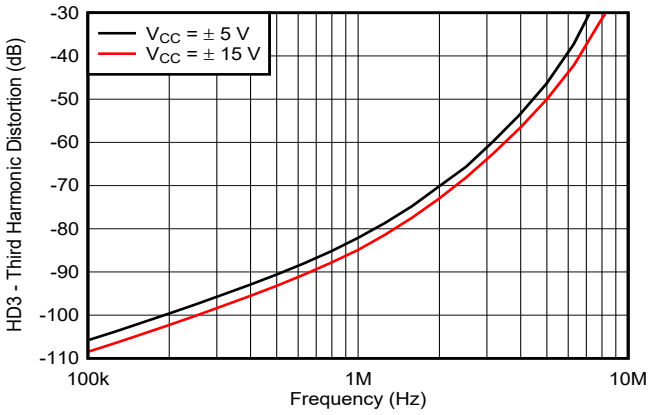
7.6 Typical Characteristics (continued)

at T_A = 25°C, V_{CC} = ±5 V, R_F = 390 Ω, gain = +1 V/V, differential input, differential output, and R_L = 800 Ω (unless otherwise noted)



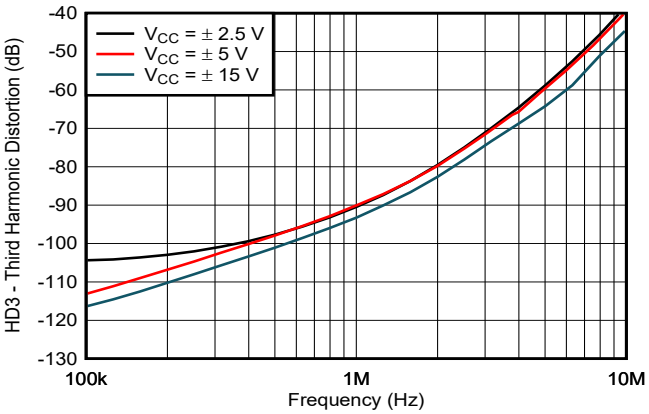
f = 500 kHz, single-ended input, differential output

Figure 7-19. Second-Harmonic Distortion vs Output Voltage



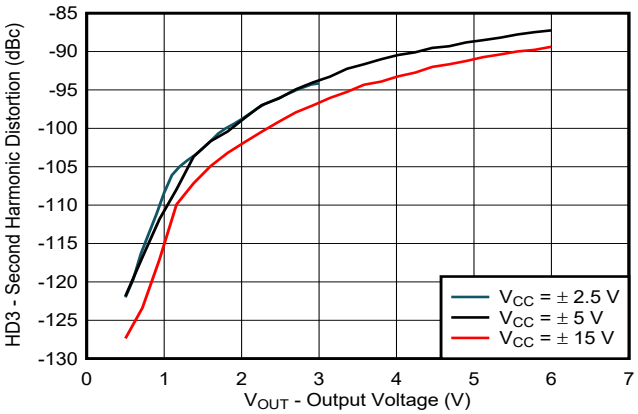
V_{OUT} = 4 V_{PP}, single-ended input, differential output

Figure 7-20. Third-Harmonic Distortion vs Frequency



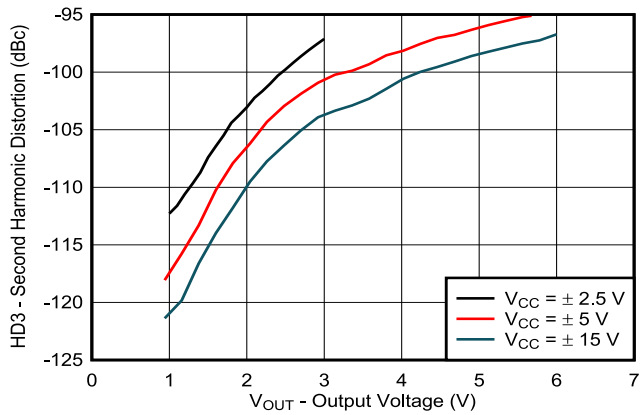
V_{OUT} = 2 V_{PP}, single-ended input, differential output

Figure 7-21. Third-Harmonic Distortion vs Frequency



f = 500 kHz, single-ended input, differential output

Figure 7-22. Third-Harmonic Distortion vs Output Voltage



f = 250 kHz, single-ended input, differential output

Figure 7-23. Third-Harmonic Distortion vs Output Voltage

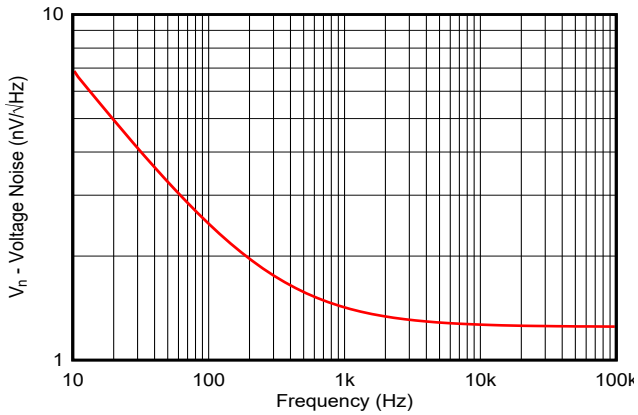


Figure 7-24. Voltage Noise vs Frequency

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7.6 Typical Characteristics (continued)

at T_A = 25°C, V_{CC} = ±5 V, R_F = 390 Ω, gain = +1 V/V, differential input, differential output, and R_L = 800 Ω (unless otherwise noted)

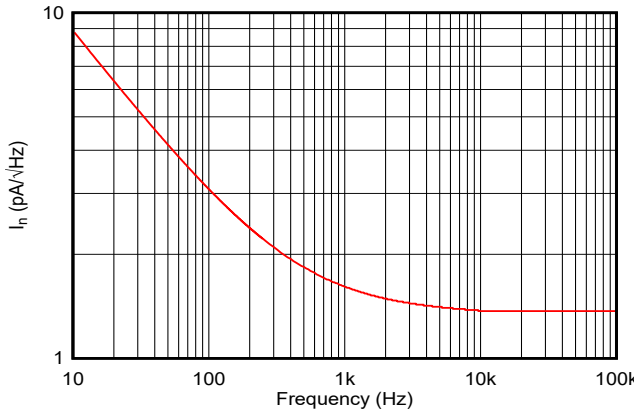
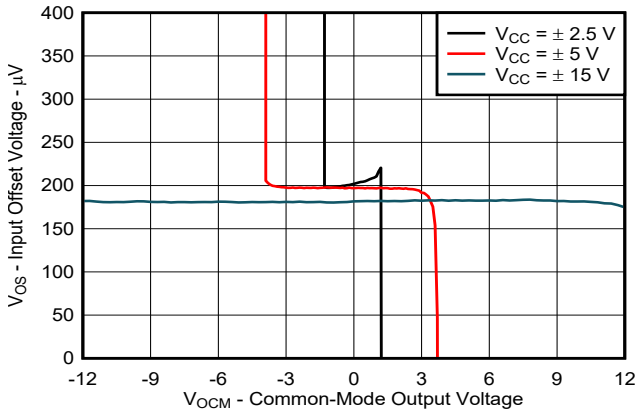
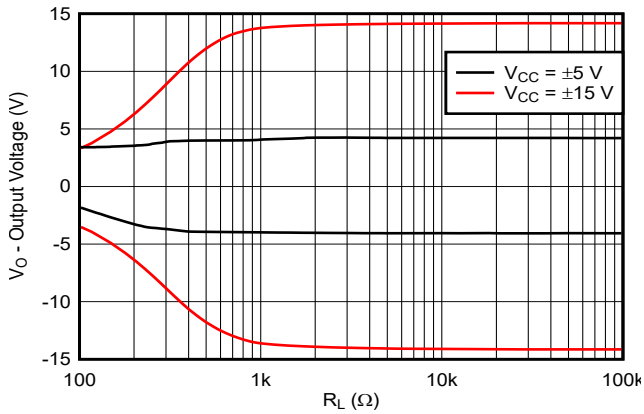


Figure 7-25. Current Noise vs Frequency



R_F = 1 kΩ

Figure 7-26. Input Offset Voltage vs Common-Mode Output Voltage



R_F = 1 kΩ, G = 2 V/V

Figure 7-27. Output Voltage vs Differential Load Resistance

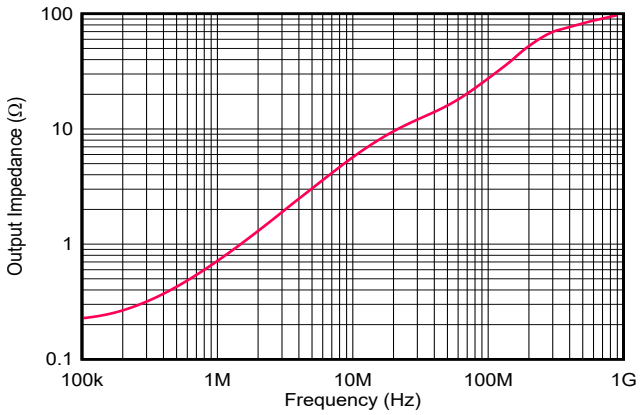


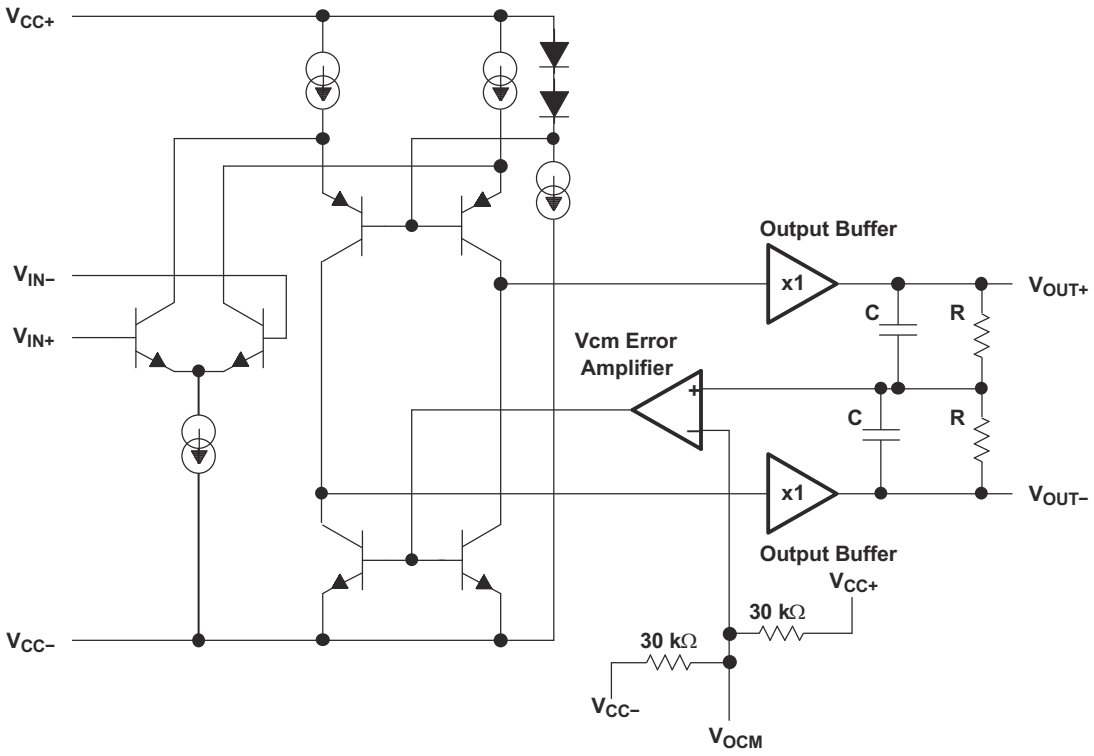
Figure 7-28. Output Impedance vs Frequency

8 Detailed Description

8.1 Overview

The THS413x devices are fully differential amplifiers (FDAs). Differential signal processing offers a number of performance advantages in high-speed analog signal processing systems, including immunity to external common-mode noise, suppression of even-order nonlinearities, and increased dynamic range. FDAs not only serve as the primary means of providing gain to a differential signal chain, but also provide a monolithic solution for converting single-ended signals into differential signals allowing for easy, high-performance processing. For more information on the basic theory of operation for FDAs, see the *Fully Differential Amplifiers* application note.

8.2 Functional Block Diagram



8.3 Feature Description

Figure 8-1 and Figure 8-2 depict the differences between the operation of the THS413x in two different modes. FDAs can work with either differential or single-ended inputs.

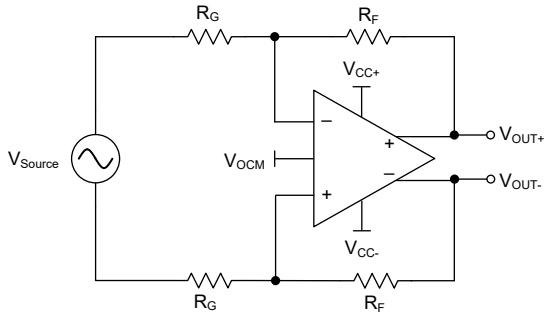


Figure 8-1. Amplifying Differential Input Signals

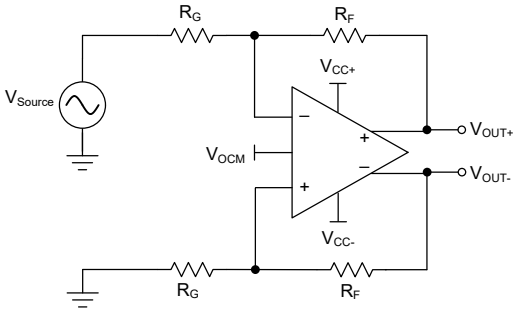


Figure 8-2. Amplifying Single-ended Input Signals

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8.4 Device Functional Modes

8.4.1 Power-Down Mode

Power-down mode is used when power saving is required. The THS4130 power-down ($\overline{PD}$) pin is an active low input. If left unconnected, an internal 250-kΩ resistor to V_{CC+} keeps the device turned on. The threshold voltage for the power-down function is approximately 1.4 V greater than $V_{CC–}$. Therefore, if the $\overline{PD}$ pin is 1.4 V greater than $V_{CC–}$, then the device is active. If the $\overline{PD}$ pin is less than 1.4 V greater than $V_{CC–}$, then the device is off. Pull the pin to $V_{CC–}$ to turn the device off. Figure 8-3 shows the simplified version of the power-down circuit. While in power-down mode, the amplifier goes into a high-impedance state. The amplifier output impedance is typically greater than 1 MΩ in power-down mode.

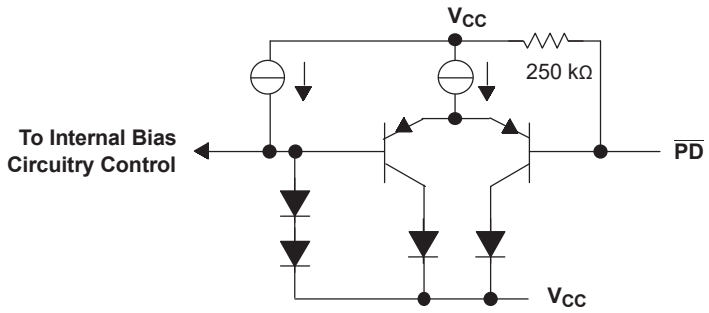
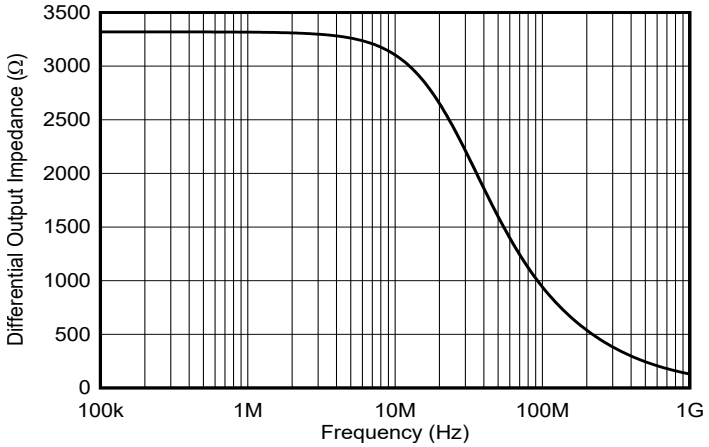


Figure 8-3. Simplified Power-Down Circuit

Similar to an op amp in an inverting configuration, the output impedance of an FDA is determined by the feedback network configuration. In addition, the THS4130 has an internal 10-kΩ resistor at each output that is tied to the V_{CM} error amplifier (see Section 8.2). The differential output impedance is equal to [(2 × R_F + 2 × R_G) || 20 kΩ]. Figure 8-4 shows the closed=loop output impedance of the THS4130 when in power-down.



V_{CC} = ±5 V, gain = 1 V/V, R_F = 1 kΩ, $\overline{PD}$ = $V_{CC–}$

Figure 8-4. Output Impedance (in Power-Down) vs Frequency

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9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Output Common-Mode Voltage

The output common-mode voltage pin sets the dc output voltage of the THS413x. A voltage applied to the VOCM pin from a low-impedance source can be used to directly set the output common-mode voltage. If left floating, then the VOCM pin defaults to the mid-rail voltage, defined as:

$$\frac{(V_{CC+}) + (V_{CC-})}{2} \tag{1}$$

To minimize common-mode noise, connect a 0.1-µF bypass capacitor to the VOCM pin. Output common-mode voltage causes additional current to flow in the feedback resistor network. This current is supplied by the output stage of the amplifier; therefore, additional power dissipation is created. For commonly-used feedback resistance values, this current is easily supplied by the amplifier. The additional internal power dissipation created by this current can be significant in some applications and can dictate the use of the HVSSOP package to effectively control self-heating.

9.1.1.1 Resistor Matching

Resistor matching is important in FDAs to maintain good output balance. An ideal differential output signal implies the two outputs of the FDA should be exactly equal in amplitude and shifted 180° in phase. Any imbalance in amplitude or phase between the two output signals results in an undesirable common-mode signal at the output. The output balance error is a measure of how well the outputs are balanced and is defined as the ratio of the output common-mode voltage to the output differential signal.

$$Output\ Balance\ Error = \frac{\left(\frac{V_{OUT+} - V_{OUT-}}{2}\right)}{V_{OUT+} - V_{OUT-}} \tag{2}$$

At low frequencies, resistor mismatch is the primary contributor to output balance errors. Additionally CMRR, PSRR, and HD2 performance diminish if resistor mismatch occurs. Therefore, to optimize performance, use 1% tolerance resistors or better. Table 9-1 provides the recommended resistor values to use for a particular gain.

Table 9-1. Recommended Resistor Values

GAIN (V/V)	R_G (Ω)	R_F (Ω)
1	390	390
2	374	750
5	402	2010
10	402	4020

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9.1.2 Driving a Capacitive Load

Driving capacitive loads with high-performance amplifiers is not a problem as long as certain precautions are taken. The THS413x have been internally compensated to maximize bandwidth and slew rate performance. When the amplifier is compensated in this manner, capacitive loading directly on the output decreases the device phase margin leading to high-frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, place a resistor in series with the output of the amplifier, as shown in Figure 9-1. A minimum value of 20 Ω works well for most applications. For example, in 50-Ω transmission systems, setting the series resistor value to 50 Ω both isolates any capacitance loading and provides the proper line impedance matching at the source end.

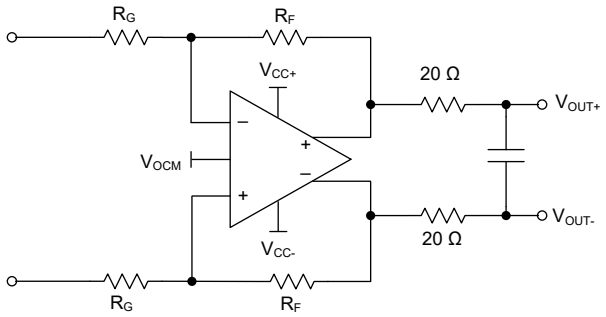

Figure 9-1. Driving a Capacitive Load

9.1.3 Data Converters

Driving data converters are one of the most popular applications for fully-differential amplifiers. Figure 9-2 shows a typical configuration of an FDA attached to a differential analog-to-digital converter (ADC).

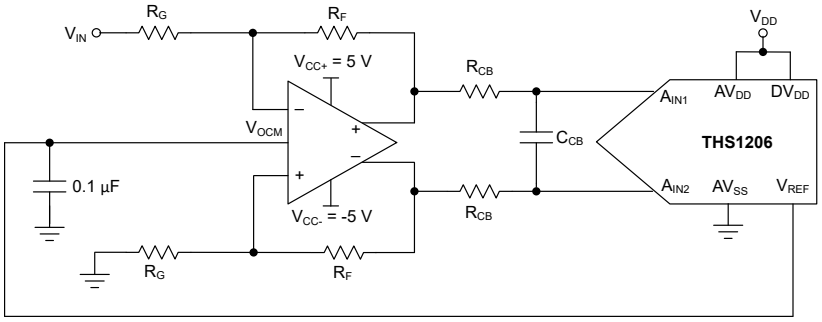

Figure 9-2. Fully-Differential Amplifier Attached to a Differential ADC

FDAs can operate with a single supply. V_{OCM} defaults to the mid-rail voltage, $V_{CC}/2$. The differential output can be fed into a data converter. This method eliminates the use of a transformer in the circuit. If the ADC has a reference voltage output (V_{ref}), then connect V_{ref} directly to the V_{OCM} of the amplifier using a bypass capacitor to reduce broadband common-mode noise.

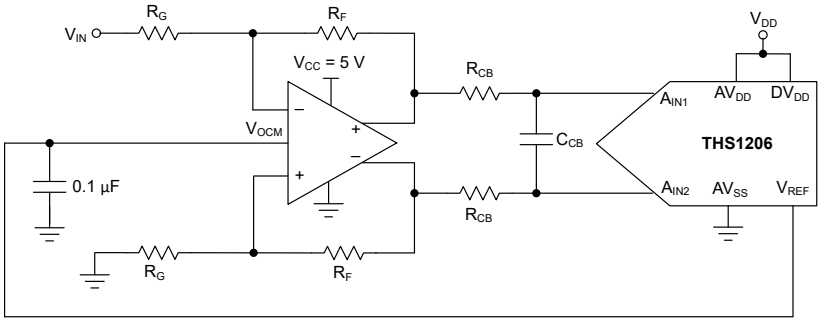

Figure 9-3. Fully-Differential Amplifier Using a Single Supply

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9.1.4 Single-Supply Applications

For proper operation, the input common-mode voltage to the input terminal of the amplifier must not exceed the common-mode input voltage range. However, some single-supply applications can require the input voltage to exceed the common-mode input voltage range. In such cases, to bring the common-mode input voltage within the specifications of the amplifier, the circuit configuration of Figure 9-4 is suggested.

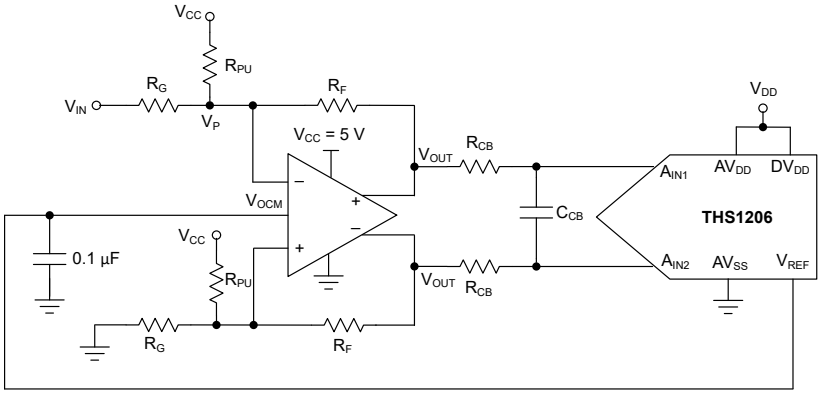

Figure 9-4. Circuit With Improved Common-Mode Input Voltage

Equation 3 is used to calculate R_{PU}:

$$R_{PU} = \frac{V_P - V_{CC}}{(V_{IN} - V_P)\frac{1}{R_G} + \left(V_{OUT} - V_P\right)\frac{1}{R_F}} \quad (3)$$

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9.2 Typical Application

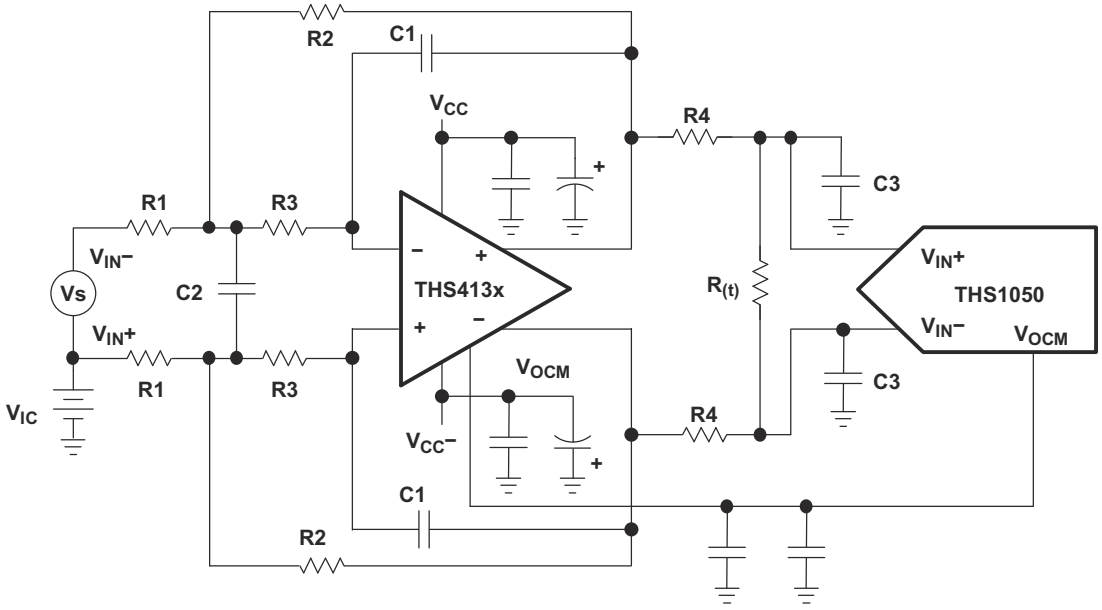

Figure 9-5. Antialias Filtering

For signal conditioning in ADC applications, make sure to limit the input frequency to the ADC. Low-pass filters can prevent the aliasing of the high-frequency noise with the frequency of operation. This design example shows a method by which the noise can be filtered in the THS413x. Figure 9-5 shows the design example for the THS413x in active low-pass filter topology driving an ADC.

9.2.1 Design Requirements

Table 9-2 shows example design parameters and values for the typical application design example in Figure 9-5.

Table 9-2. Design Parameters

DESIGN PARAMETERS	VALUE
Supply voltage	±2.5 V to ±15 V
Amplifier topology	Voltage feedback
Output control	DC-coupled with output common-mode control capability
Filter requirement	500-kHz, multiple-feedback low-pass filter

9.2.2 Detailed Design Procedure

Figure 9-5 shows a multiple-feedback (MFB) low-pass filter. The transfer function for this filter circuit is:

$$H_d(f) = \left[\frac{K}{-\left[\frac{f}{FSF \times fc}\right]^2 + \frac{1}{Q}\frac{jf}{FSF \times fc} + 1}\right] \times \left[\frac{\frac{Rt}{2R4 + Rt}}{1 + \frac{j2\pi fR4RtC3}{2R4 + Rt}}\right]$$

$$where\ K = \frac{R2}{R1}, FSF \times fc = \frac{1}{2\pi\sqrt{2 \times R2R3C1C2}}, and\ Q = \frac{\sqrt{2 \times R2R3C1C2}}{R3C1 + R2C1 + KR3C1} \quad (4)$$

K sets the pass-band gain, fc is the cutoff frequency for the filter, FSF is a frequency scaling factor, and Q is the quality factor.

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$$FSF = \sqrt{Re^2 + |Im|^2}\ and\ Q = \frac{\sqrt{Re^2 + |Im|^2}}{2Re} \quad (5)$$

where Re is the real part and Im is the imaginary part of the complex pole pair. Setting R2 = R, R3 = mR, C1 = C, and C2 = nC results in:

$$FSF \times fc = \frac{1}{2\pi Rc\sqrt{2 \times mn}}\ and\ Q = \frac{\sqrt{2 \times mn}}{1 + m(1 + K)} \quad (6)$$

Start by determining the ratios, m and n, required for the gain and Q of the filter type being designed, then select C and calculate R for the desired fc.

9.2.3 Application Curve

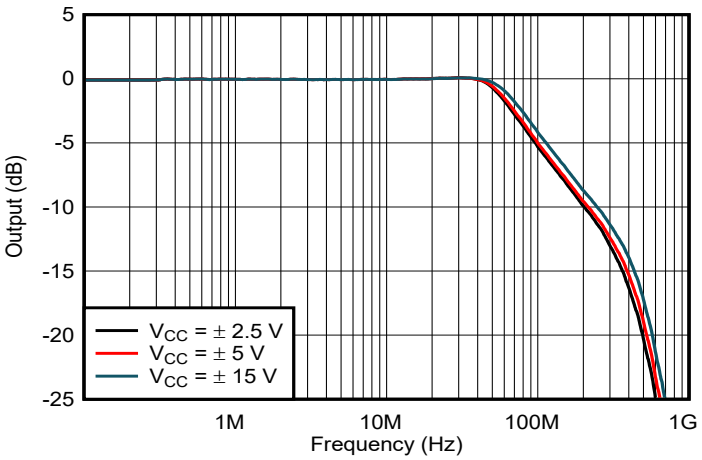

Figure 9-6. Large-Signal Frequency Response

9.3 Power Supply Recommendations

The THS413x devices are designed to operate on power supplies ranging from ±2.5 V to ±15 V (single-ended supplies of 5 V to 30 V). Use a power-supply accuracy of 5% or better. When operated on a board with high-speed digital signals, make sure to provide isolation between digital signal noise and the analog input pins. The THS413x are connected to power supplies through pin 3 (V_{CC+}) and pin 6 (V_{CC-}). Decouple each supply pin to GND as close to the device as possible with a low-inductance, surface-mount ceramic capacitor of approximately 10 nF. When vias are used to connect the bypass capacitors to a ground plane, configure the vias for minimal parasitic inductance. One method of reducing via inductance is to use multiple vias. For broadband systems, two capacitors per supply pin are advised.

To avoid undesirable signal transients, do not power on the THS413x with large inputs signals present. Careful planning of system power on sequencing is especially important to avoid damage to ADC inputs when an ADC is used in the application.

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9.4 Layout

9.4.1 Layout Guidelines

To achieve the levels of high-frequency performance of the THS413x devices, follow proper printed-circuit board (PCB) high-frequency design techniques. Following is a general set of guidelines. In addition, a THS413x evaluation board is available to use as a guide for layout or for evaluating device performance.

- Ground planes—Use a ground plane on the board to provide all components with a low inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize the stray capacitance.
- Proper power-supply decoupling—use a 6.8-µF tantalum capacitor in parallel with a 0.1-µF ceramic capacitor on each supply pin. Sharing the tantalum among several amplifiers is possible depending on the application; however, always use a 0.1-µF ceramic capacitor on the supply pin of every amplifier. In addition, place the 0.1-µF capacitor as close as possible to the supply pin. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. Strive for distances of less than 0.1 inches between the device power pin and the ceramic capacitors.
- Short trace runs or compact part placements—to optimize high-frequency performance, minimize stray series inductance. The best method is to make the circuit layout as compact as possible, thereby minimizing the length of all trace runs. Pay particular attention to the inputs of the amplifier; keep the length as short as possible. This short length helps minimize stray capacitance at the input of the amplifier.

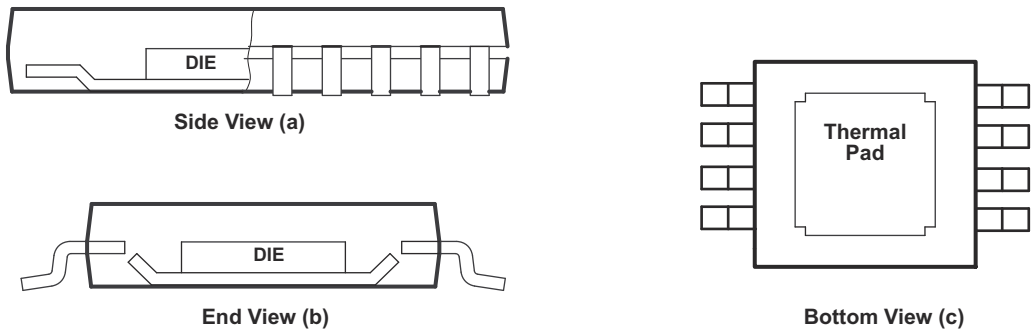
9.4.1.1 PowerPAD™ Integrated Circuit Package Design Considerations

The THS413x is available in a thermally-enhanced DGN package, which is a member of the PowerPAD™ integrated circuit package family. This package is constructed using a downset leadframe upon which the die is mounted (see Figure 9-7 **a** and Figure 9-7 **b**). This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package (see Figure 9-7 **c**). Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad can also be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat dissipating device.

The PowerPAD package represents a breakthrough in combining the small area and ease of assembly of the surface mount with the previously awkward mechanical methods of using a heat sink.

More complete details of the PowerPAD installation process and thermal management techniques can be found in *PowerPAD Thermally-Enhanced Package* application report. This document can be found on the TI website at www.ti.com by searching for the keyword PowerPAD. The document can also be ordered through your local TI sales office; refer to SLMA002 when ordering.



Note: The thermal pad (PowerPAD) is electrically isolated from all other pins and can be connected to any potential from V_{CC-} to V_{CC+}. Typically, the thermal pad is connected to the ground plane because this plane tends to physically be the largest and is able to dissipate the most amount of heat.

Figure 9-7. Views of Thermally-Enhanced DGN Package

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9.4.2 Layout Example

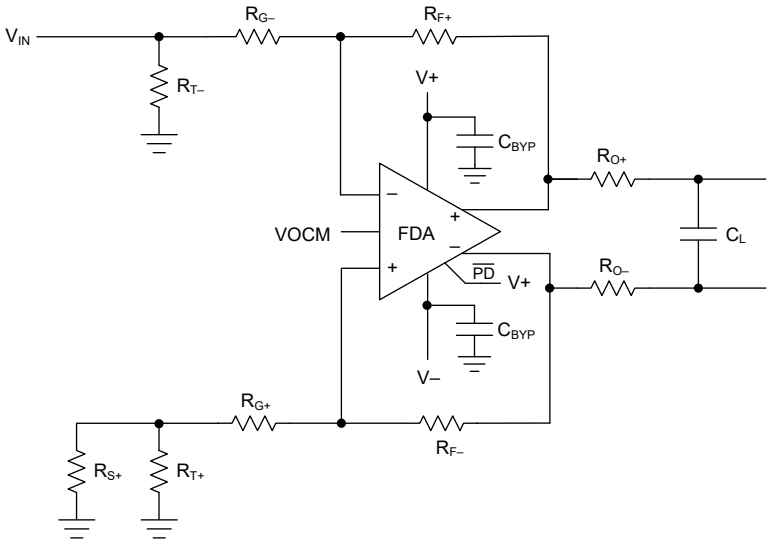

Figure 9-8. Representative Schematic for Layout

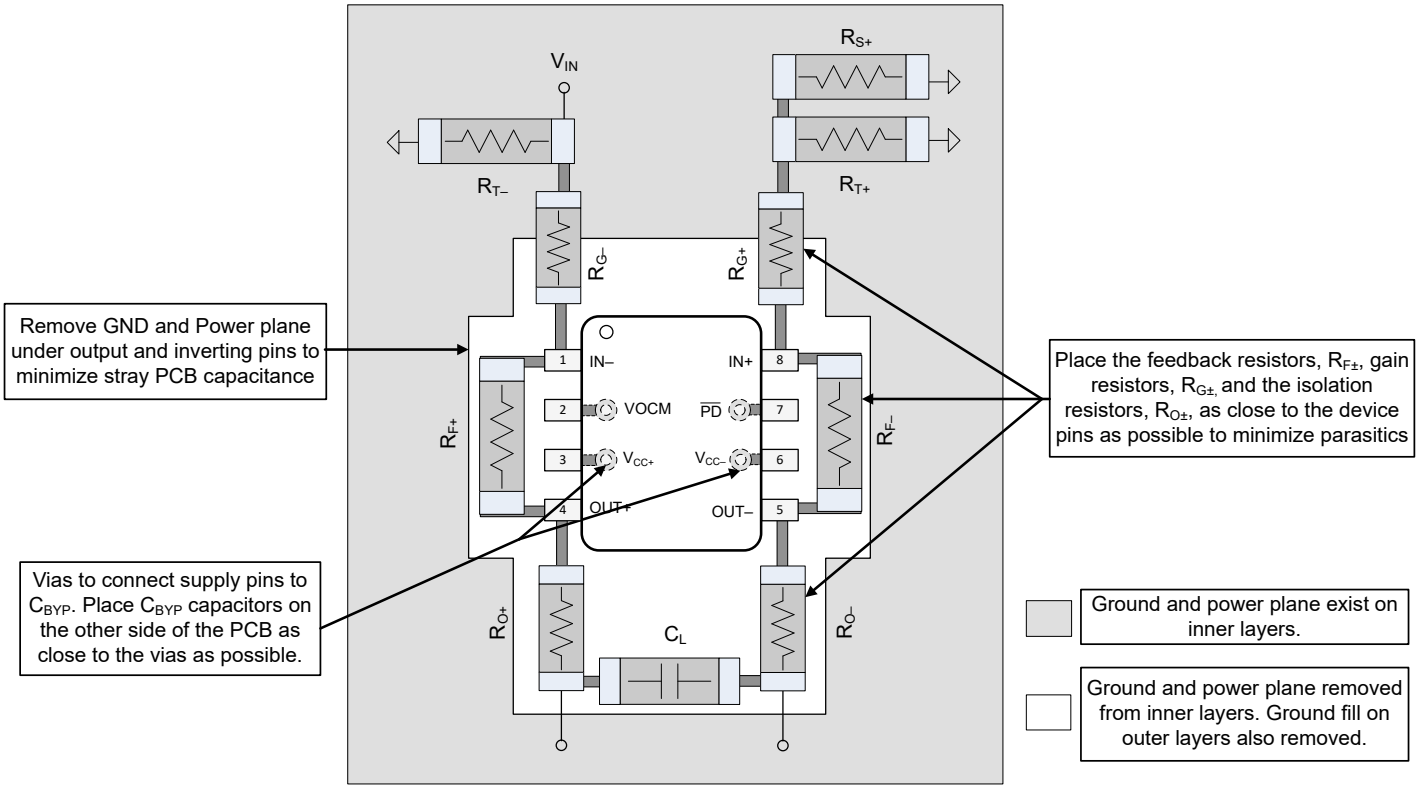

Figure 9-9. Layout Recommendations

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10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Design Guide for 2.3 nV/√Hz, Differential, Time Gain Control (TGC) DAC Reference Design for Ultrasound* design guide
- Texas Instruments, *EVM User's Guide for High-Speed Fully-Differential Amplifier* user's guide
- Texas Instruments, *Fully Differential Amplifiers* application note
- Texas Instruments, *Maximizing Signal Chain Distortion Performance Using High Speed Amplifiers* application note
- Texas Instruments, *PowerPAD Thermally-Enhanced Package* application report
- Texas Instruments, *PowerPAD™ Made Easy* application report
- Texas Instruments, *TI Precision Labs - Fully Differential Amplifiers* video series

10.2 Receiving Notification of Documentation Updates

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PowerPAD™ and TI E2E™ are trademarks of Texas Instruments.
All trademarks are the property of their respective owners.

10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THS4130CD	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	4130C	
THS4130CDG4	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	4130C	
THS4130CDGNR	LIFEBUY	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	AOB	
THS4130CDGNRG4	LIFEBUY	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	AOB	
THS4130IDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ASO	Samples
THS4130IDGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	(4130, AOC)	Samples
THS4130IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4130I	Samples
THS4131CD	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	4131C	
THS4131CDG4	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	4131C	
THS4131CDGNR	LIFEBUY	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	AOD	
THS4131CDR	LIFEBUY	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	4131C	
THS4131ID	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4131I	
THS4131IDG4	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4131I	
THS4131IDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ASP	Samples
THS4131IDGN	LIFEBUY	HVSSOP	DGN	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AOE	
THS4131IDGNG4	LIFEBUY	HVSSOP	DGN	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AOE	
THS4131IDGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	(4131, AOE)	Samples
THS4131IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4131I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

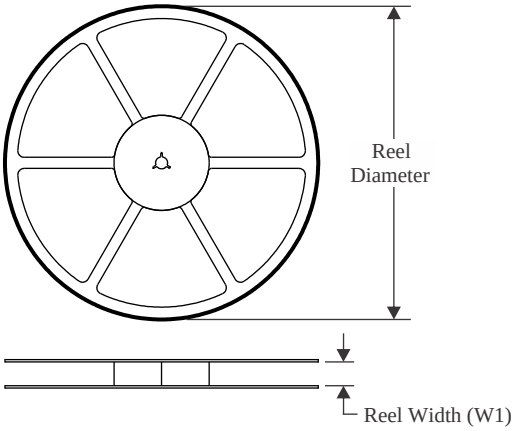
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

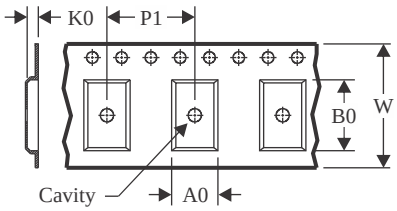
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

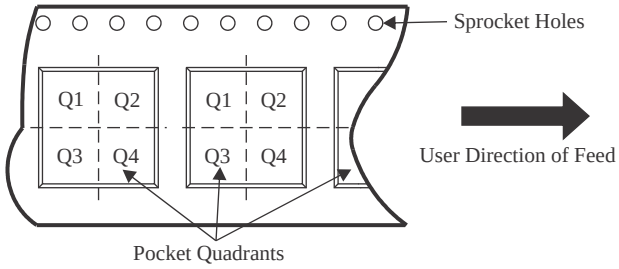


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

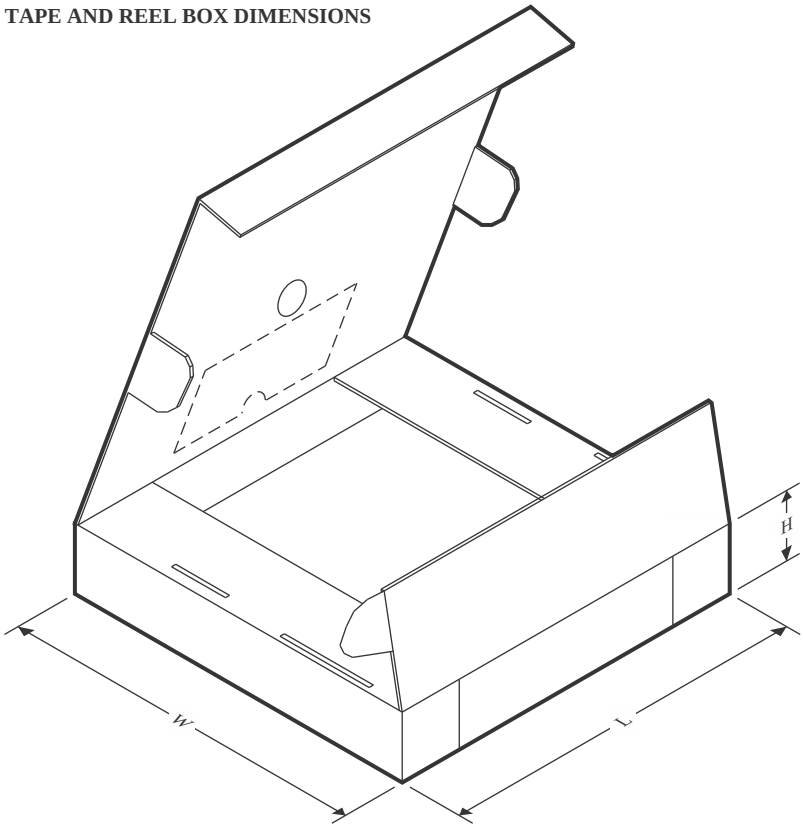
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS4130CDGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4130IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4130IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4130IDGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4130IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
THS4131CDGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4131CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
THS4131IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4131IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4131IDGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4131IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

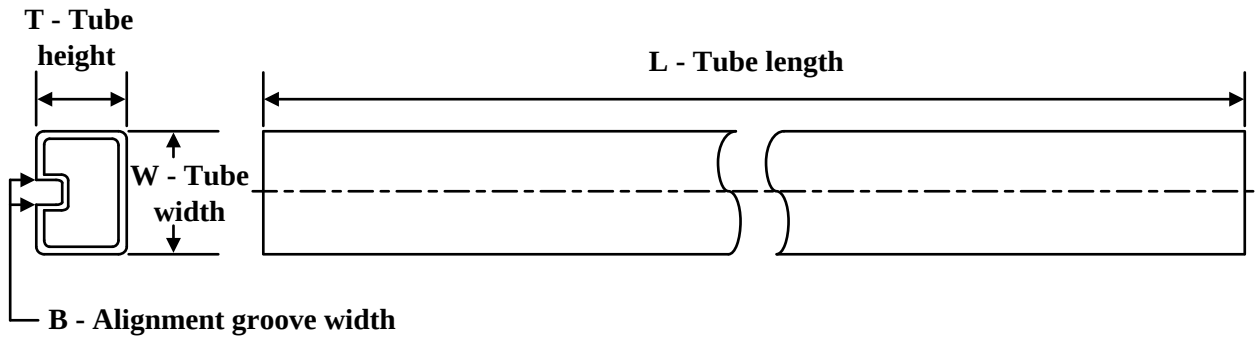
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS4130CDGNR	HVSSOP	DGN	8	2500	358.0	335.0	35.0
THS4130IDGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
THS4130IDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
THS4130IDGNR	HVSSOP	DGN	8	2500	358.0	335.0	35.0
THS4130IDR	SOIC	D	8	2500	350.0	350.0	43.0
THS4131CDGNR	HVSSOP	DGN	8	2500	358.0	335.0	35.0
THS4131CDR	SOIC	D	8	2500	350.0	350.0	43.0
THS4131IDGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
THS4131IDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
THS4131IDGNR	HVSSOP	DGN	8	2500	358.0	335.0	35.0
THS4131IDR	SOIC	D	8	2500	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
THS4130CD	D	SOIC	8	75	505.46	6.76	3810	4
THS4130CDG4	D	SOIC	8	75	505.46	6.76	3810	4
THS4131CD	D	SOIC	8	75	505.46	6.76	3810	4
THS4131CDG4	D	SOIC	8	75	505.46	6.76	3810	4
THS4131ID	D	SOIC	8	75	505.46	6.76	3810	4
THS4131IDG4	D	SOIC	8	75	505.46	6.76	3810	4

GENERIC PACKAGE VIEW

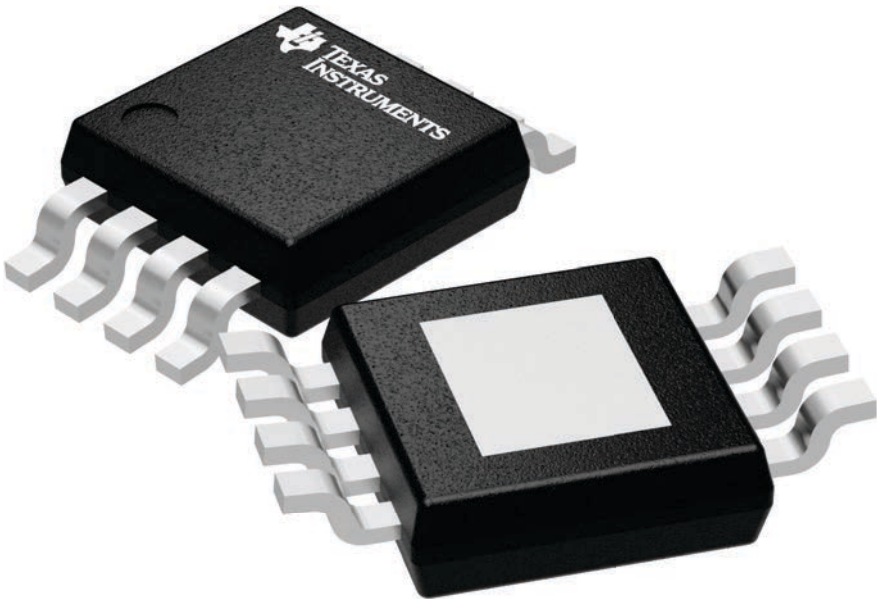
DGN 8

PowerPAD VSSOP - 1.1 mm max height

3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

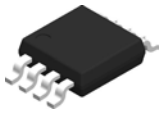
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225482/A

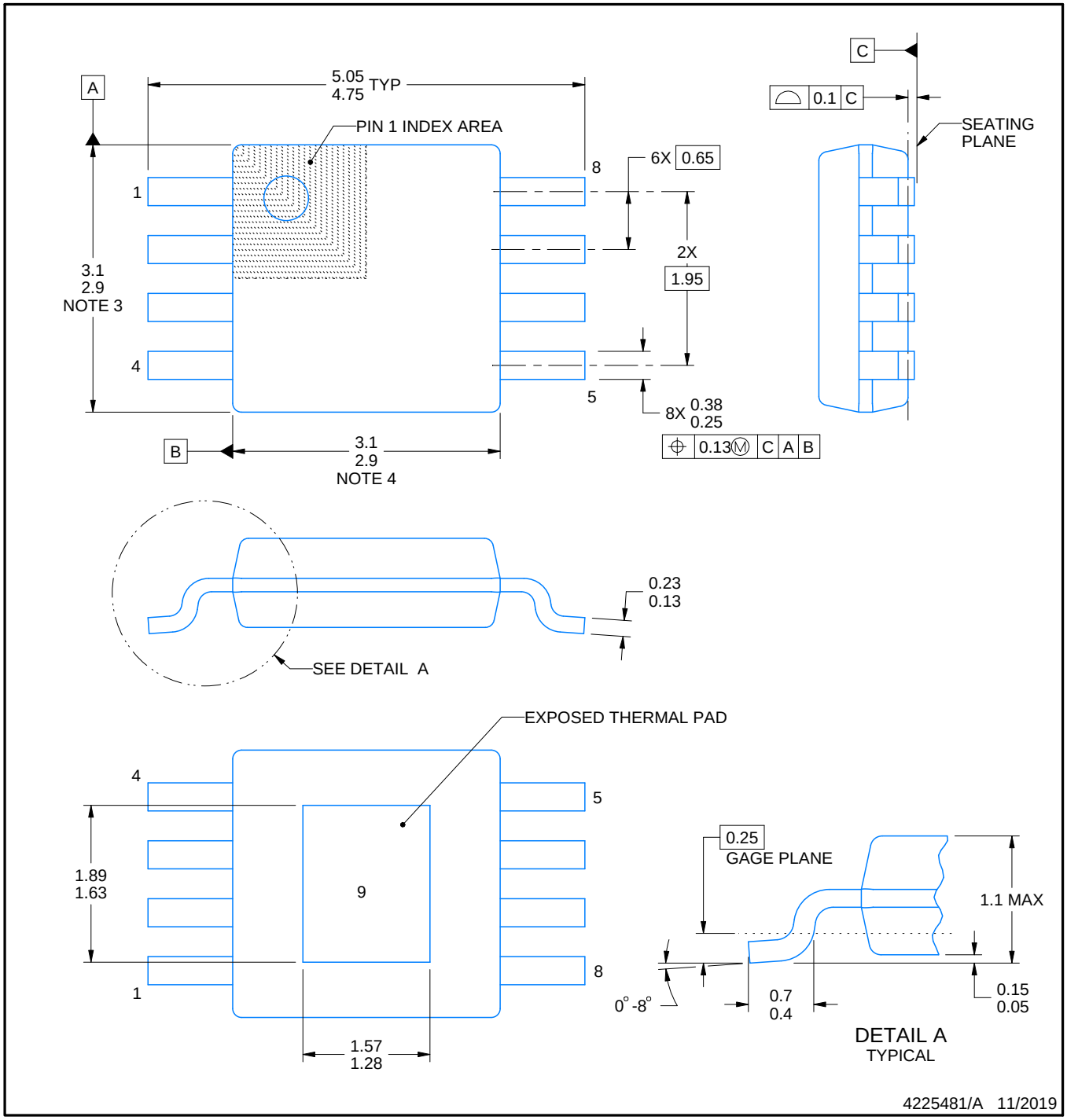
PACKAGE OUTLINE

DGN0008D



PowerPAD™ VSSOP - 1.1 mm max height

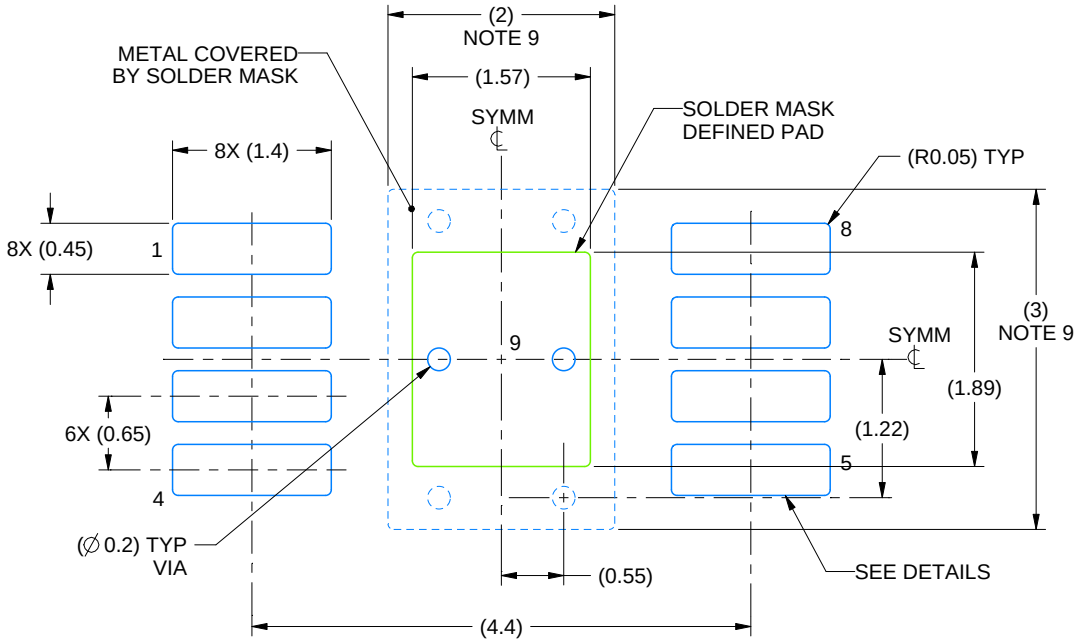
SMALL OUTLINE PACKAGE



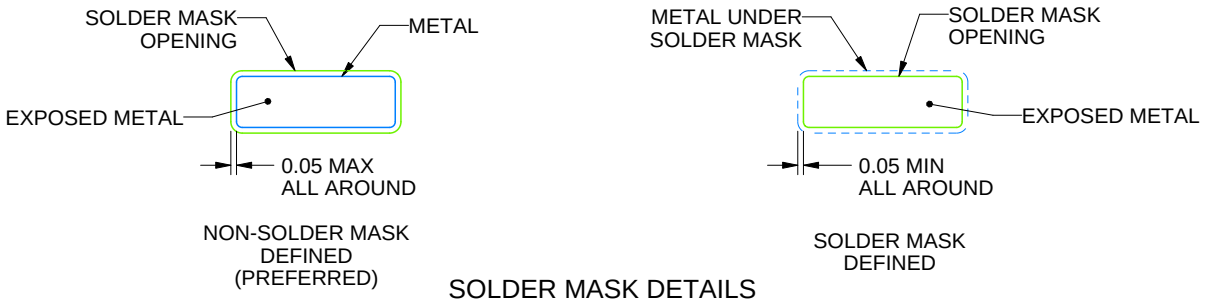
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

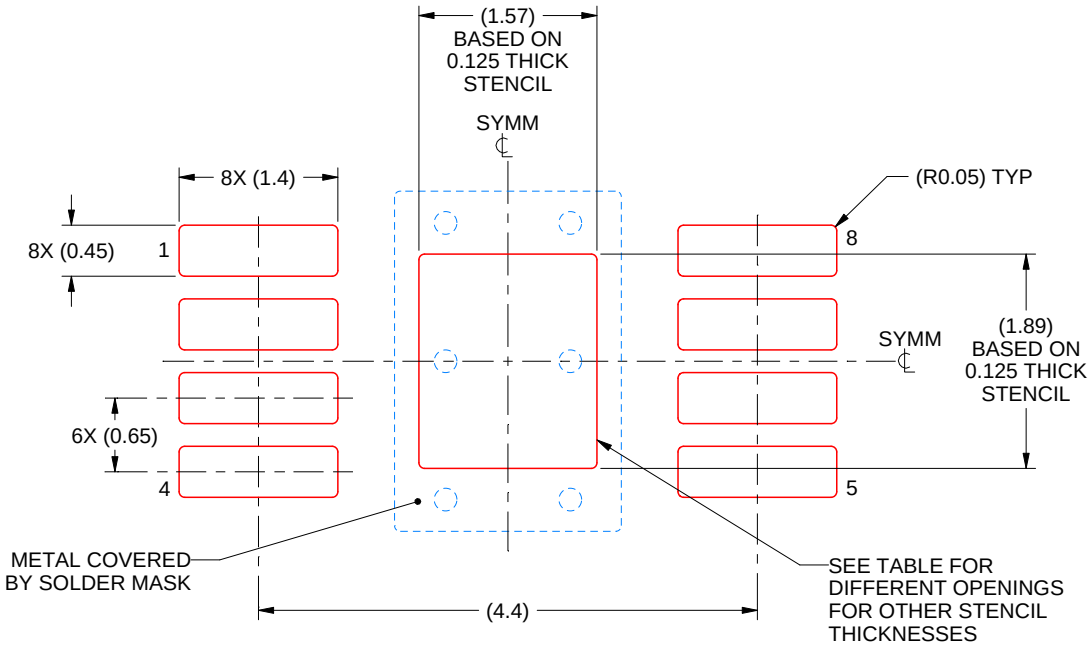


SOLDER MASK DETAILS

4225481/A 11/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

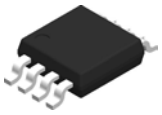
4225481/A 11/2019

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

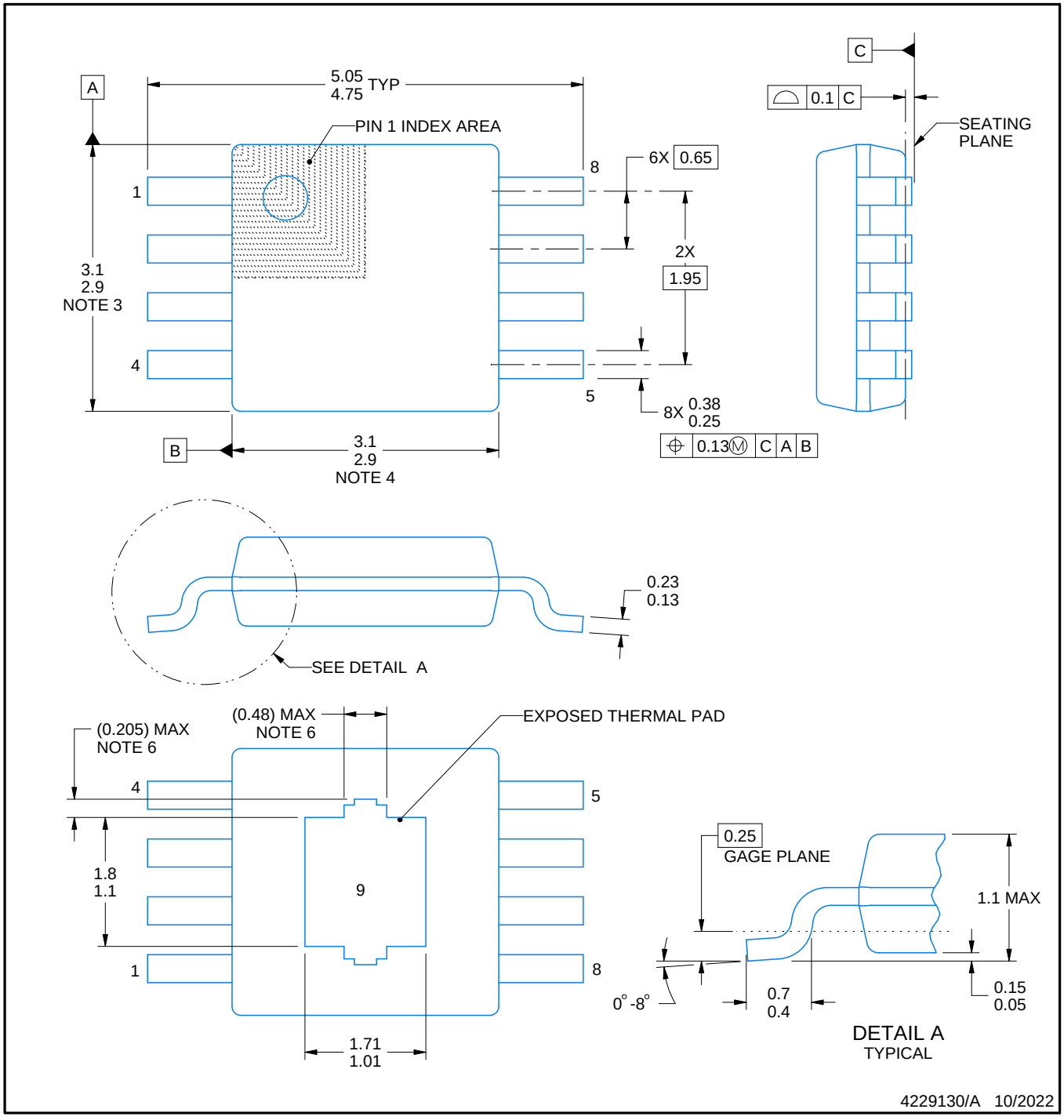
PACKAGE OUTLINE

DGN0008H



PowerPAD™ VSSOP - 1.1 mm max height

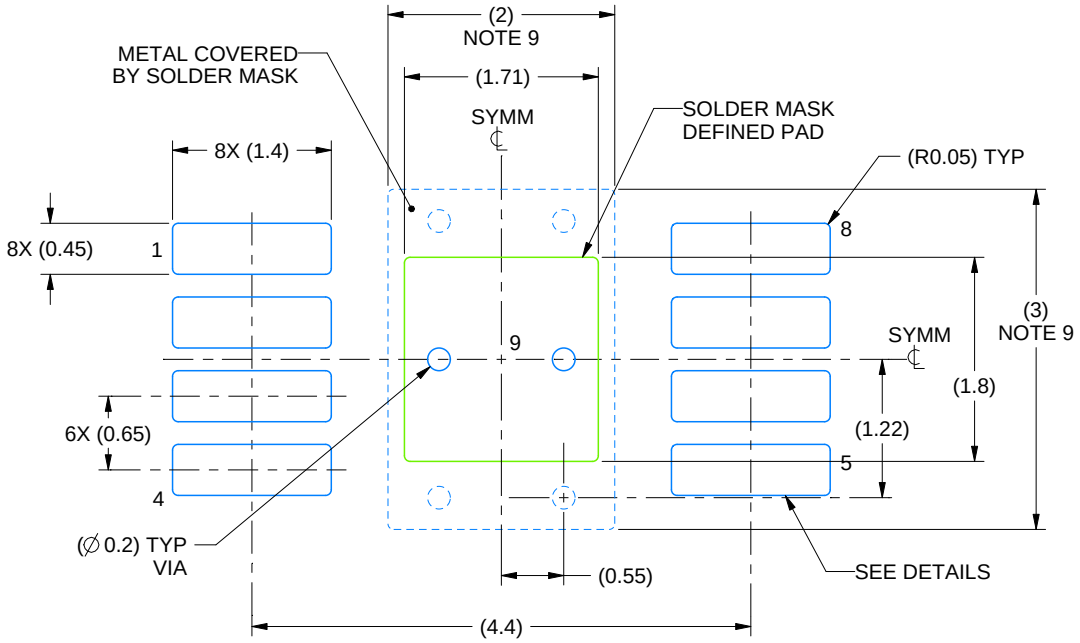
SMALL OUTLINE PACKAGE



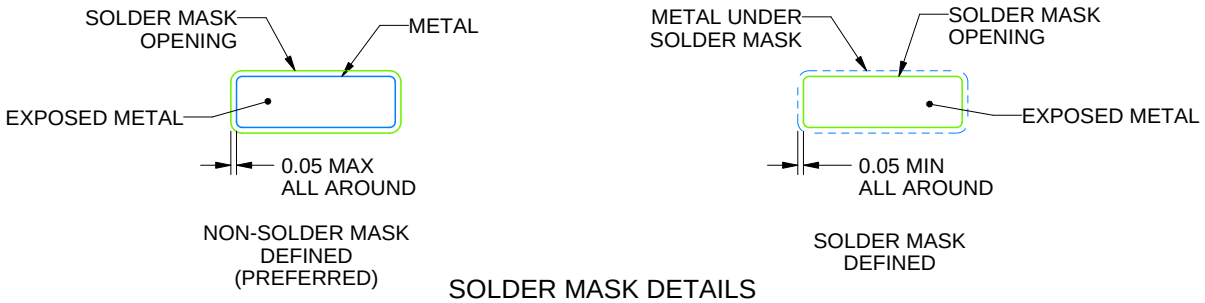
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.
6. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

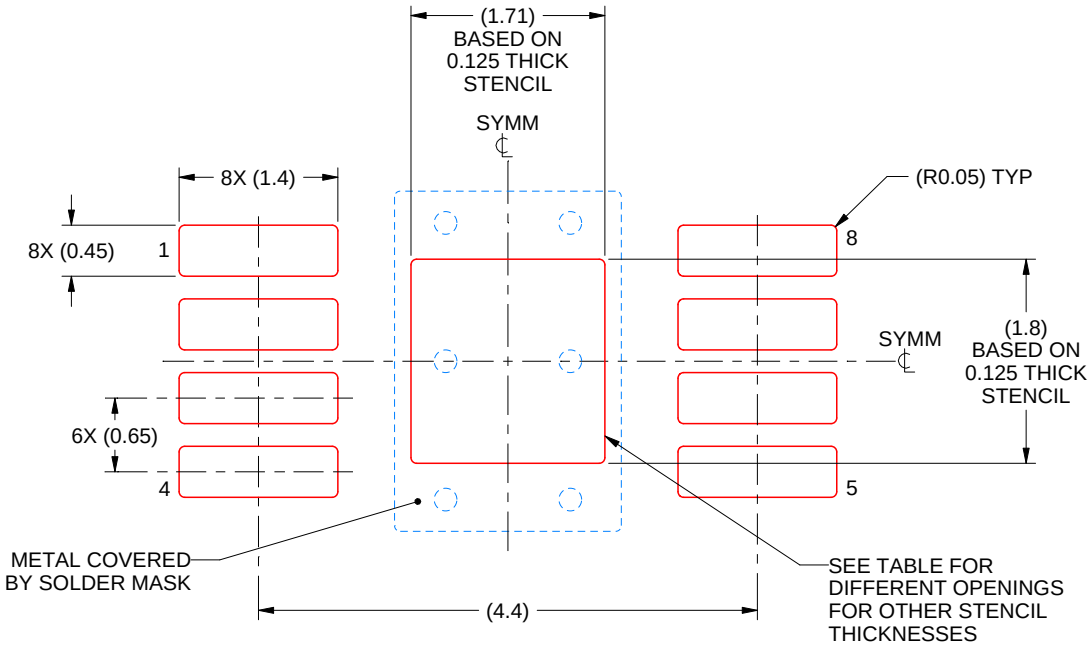


SOLDER MASK DETAILS

4229130/A 10/2022

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
9. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.



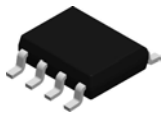
SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.91 X 2.01
0.125	1.71 X 1.80 (SHOWN)
0.15	1.56 X 1.64
0.175	1.45 X 1.52

4229130/A 10/2022

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

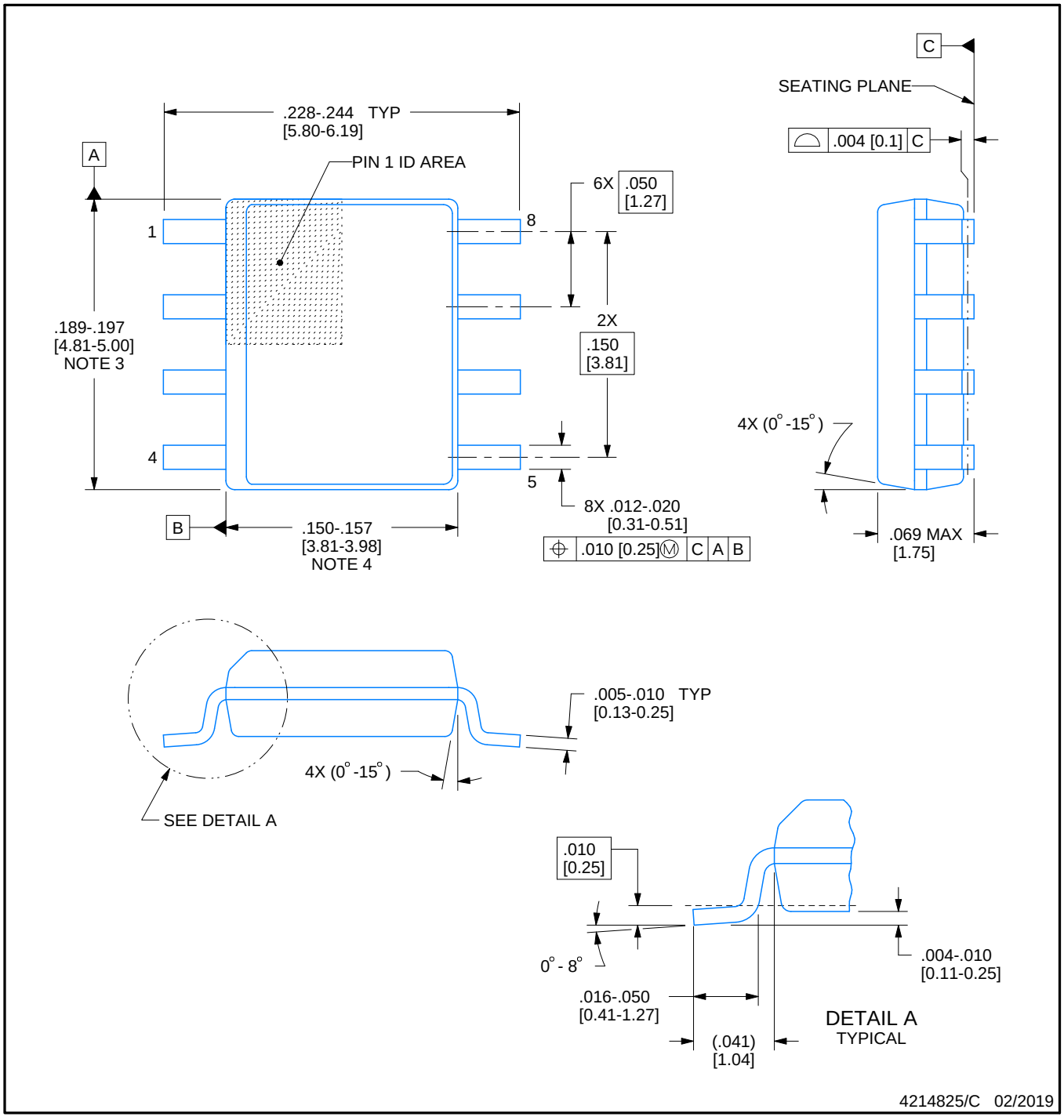


PACKAGE OUTLINE

D0008A

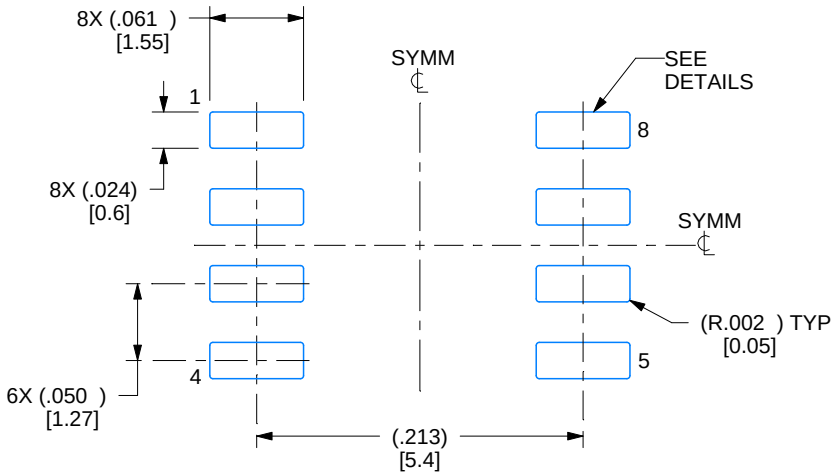
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

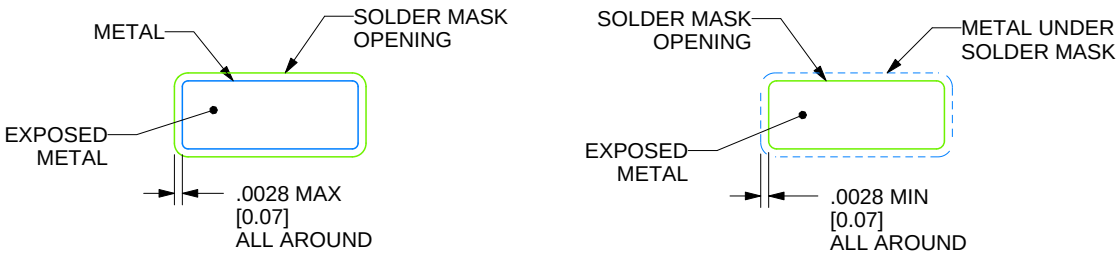


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

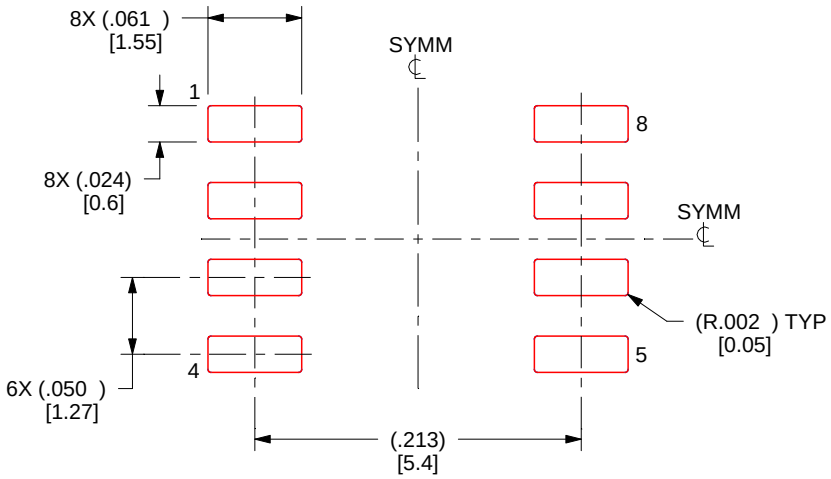
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



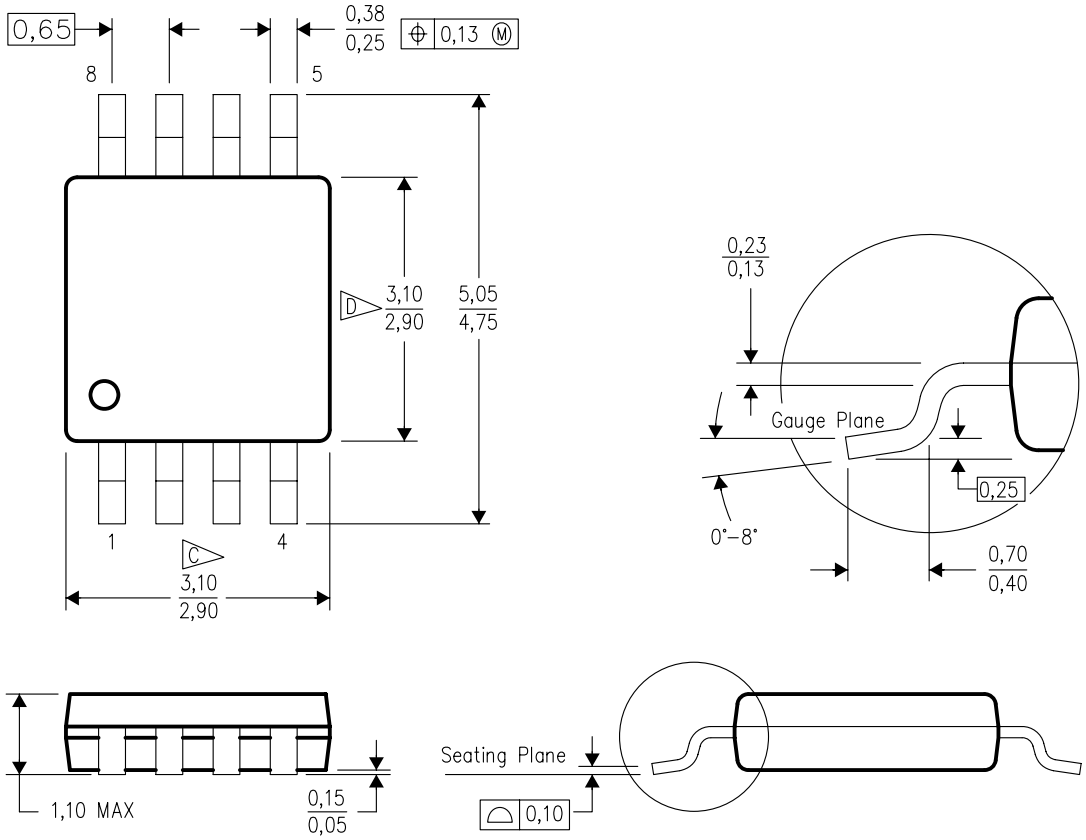
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

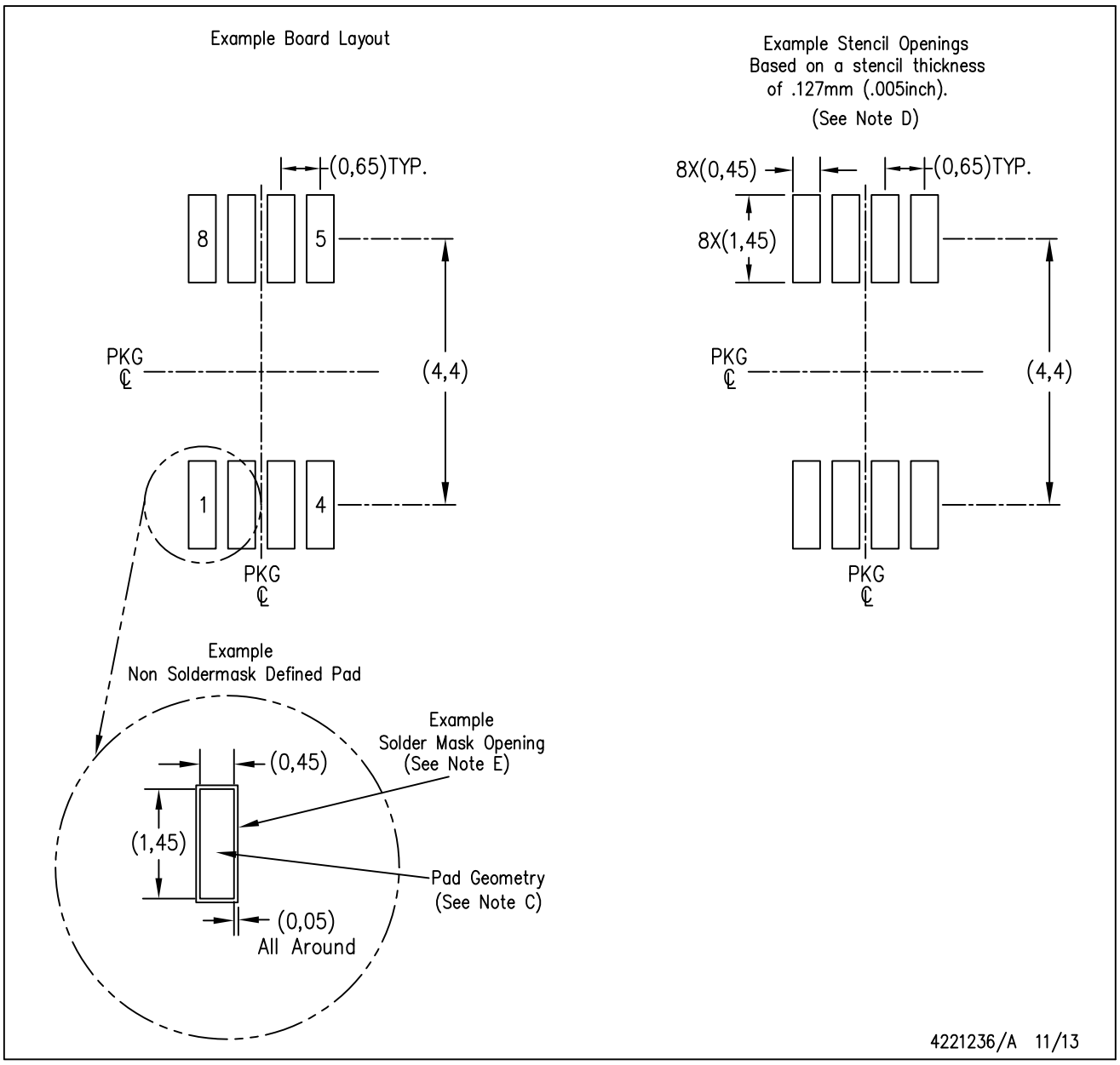
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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