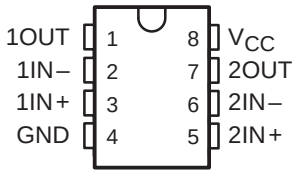
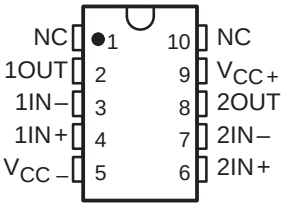
- **Very Low Power Consumption**
- **Power Dissipation With ±2-V Supplies 170 μW Typ**
- **Low Input Bias and Offset Currents**
- **Output Short-Circuit Protection**
- **Low Input Offset Voltage**
- **Internal Frequency Compensation**
- **Latch-Up-Free Operation**
- **Popular Dual Operational Amplifier Pinout**

TL022M . . . JG PACKAGE
TL022C . . . D OR P PACKAGE
(TOP VIEW)



TL022M . . . U PACKAGE
(TOP VIEW)

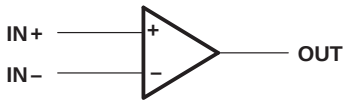


TL022M IS NOT RECOMMENDED FOR NEW DESIGNS

description

The TL022 is a dual low-power operational amplifier designed to replace higher power devices in many applications without sacrificing system performance. High input impedance, low supply currents, and low equivalent input noise voltage over a wide range of operating supply voltages result in an extremely versatile operational amplifier for use in a variety of analog applications including battery-operated circuits. Internal frequency compensation, absence of latch-up, high slew rate, and output short-circuit protection assure ease of use.

symbol (each amplifier)



The TL022C is characterized for operation from 0°C to 70°C. The TL022M is characterized for operation over the full military temperature range of –55°C to 125°C.

AVAILABLE OPTIONS

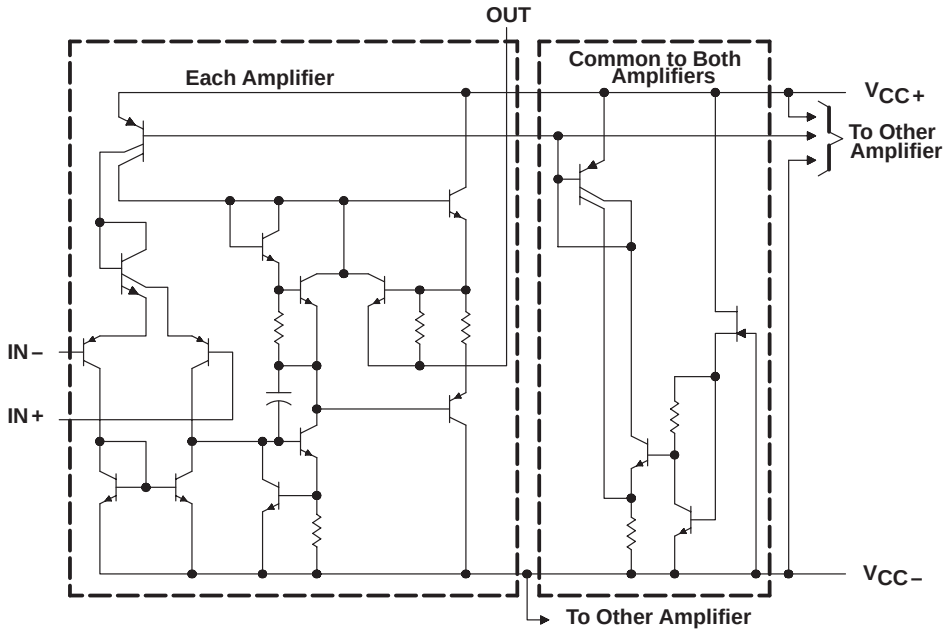
T_A	V_{IO}max AT 25°C	PACKAGE			
		SMALL OUTLINE (D)	CERAMIC DIP (JG)	PLASTIC DIP (P)	CERAMIC FLAT PACK (U)
0°C to 70°C	5 mV	TL022CD	—	TL022CP	—
–55°C to 125°C	5 mV	—	TL022MJG	—	TL022MU

The D package is available taped and reeled. Add the suffix R to the device type (i.e. TL022CDR).

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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schematic



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		TL022C	TL022M	UNIT
Supply voltage, V_{CC+} (see Note 1)		18	22	V
Supply voltage, V_{CC-} (see Note 1)		–18	–22	V
Differential input voltage (see Note 2)		±30	±30	V
Input voltage (any input, see Notes 1 and 3)		±15	±15	V
Duration of output short circuit (see Note 4)		unlimited	unlimited	
Continuous total dissipation		See Dissipation Rating Table		
Operating free-air temperature range		0 to 70	–55 to 125	°C
Storage temperature range		–65 to 150	–65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	JG or U package		300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or P package	260		°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at IN+ with respect to IN–.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output may be shorted to ground or either power supply. For the TL022M only, the unlimited duration of the short circuit applies at (or below) 125°C case temperature or 75°C free-air temperature.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	680 mW	5.8 mW/°C	33°C	464 mW	—
JG	680 mW	8.4 mW/°C	69°C	672 mW	210 mW
P	680 mW	8.0 mW/°C	65°C	640 mW	—
U	675 mW	5.4 mW/°C	25°C	432 mW	135 mW

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{CC+}	5	15	V
Supply voltage, V_{CC-}	−5	−15	V

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TL022C			TL022M			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, R_S = 50 Ω	25°C		1	5		1	5	mV
			Full range			7.5			6	
I_{IO}	Input offset current	V_O = 0	25°C		15	80		5	40	nA
			Full range			200			100	
I_{IB}	Input bias current	V_O = 0	25°C		100	250		50	100	nA
			Full range			400			250	
V_{ICR}	Common-mode input voltage range		25°C	±12	±13		±12	±13		V
			Full range	±12			±12			
$V_{O(PP)}$	Maximum peak-to-peak output voltage swing	R_L = 10 kΩ	25°C	20	26		20	26		V
		R_L ≥ 10 kΩ	Full range	20			20			
A_{VD}	Large-signal differehtial voltage amplification	R_L ≥ 10 kΩ, V_O = ±10 V	25°C	60	80		72	86		dB
			Full range	60			66			
B_1	Unity-gain bandwidth		25°C		0.5			0.5		MHz
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	60	72		60	72		dB
			Full range	60			60			
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	V_{CC} = ± 9 V to ±15 V, R_S = 50 Ω	25°C		30	200		30	150	μV/V
			Full range			200			150	
V_n	Equivalent input noise voltage	A_{VD} = 20 dB, B = 1 Hz, f = 1 kHz	25°C		50			50		nV/Hz
I_{OS}	Short-circuit output current		25°C		±6			±6		mA
I_{CC}	Supply current (both amplifiers)	V_O = 0, No load	25°C		130	250		130	250	μA
			Full range			250			250	
P_D	Total dissipation (both amplifiers)	V_O = 0, No load	25°C		3.9	7.5		3.9	6	mW
			Full range			7.5			6	

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range for TL022C is 0°C to 70°C and for TL022M is −55°C to 125°C.

operating characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Rise time	V_I = 20 mV, R_L = 10 kΩ, C_L = 100 pF, See Figure 1		0.3		μs
	Overshoot factor			5%		
SR	Slew rate at unity gain	V_I = 10 V, R_L = 10 kΩ, C_L = 100 pF, See Figure 1		0.5		V/μs

PARAMETER MEASUREMENT INFORMATION

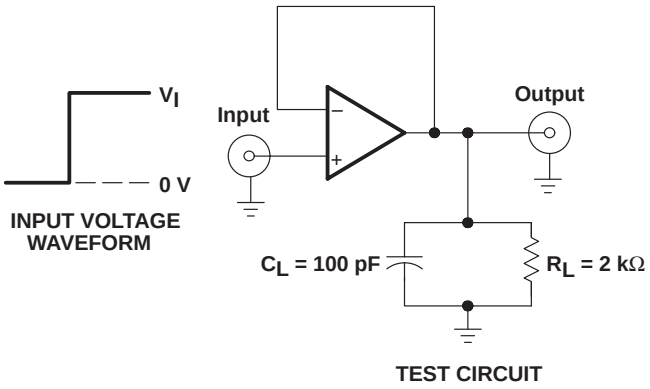


Figure 1. Rise Time, Overshoot Factor, and Slew Rate

TYPICAL CHARACTERISTICS

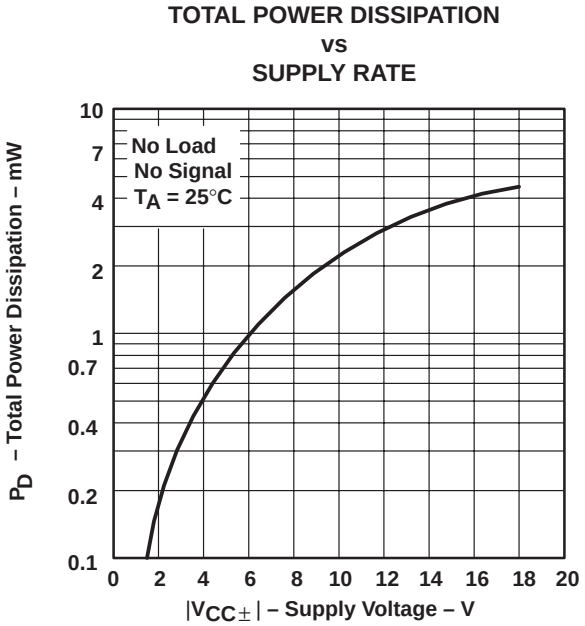


Figure 2

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL022CD	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL022C	
TL022CDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL022C	Samples
TL022CDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL022C	Samples
TL022CDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL022C	Samples
TL022CDRG4	ACTIVE	SOIC	D	8	2500	TBD	Call TI	Call TI	0 to 70		Samples
TL022CDRG4	ACTIVE	SOIC	D	8	2500	TBD	Call TI	Call TI	0 to 70		Samples
TL022CDRG4	ACTIVE	SOIC	D	8	2500	TBD	Call TI	Call TI	0 to 70		Samples
TL022CP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL022CP	Samples
TL022CP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL022CP	Samples
TL022CP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL022CP	Samples
TL022CPSR	LIFEBUY	SO	PS	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T022	
TL022CPSR	LIFEBUY	SO	PS	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T022	
TL022CPSR	LIFEBUY	SO	PS	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T022	
TL022CPSRG4	LIFEBUY	SO	PS	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T022	
TL022CPSRG4	LIFEBUY	SO	PS	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T022	
TL022CPSRG4	LIFEBUY	SO	PS	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T022	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

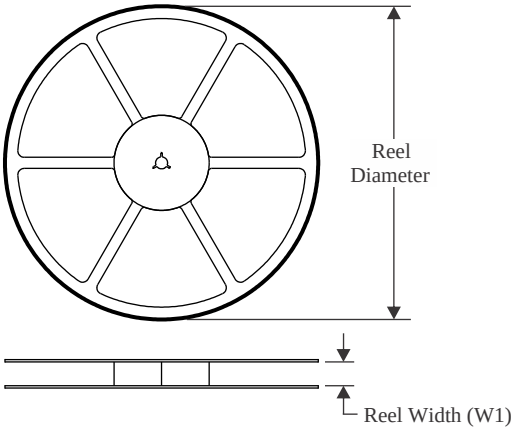
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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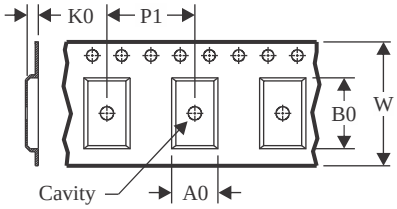
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

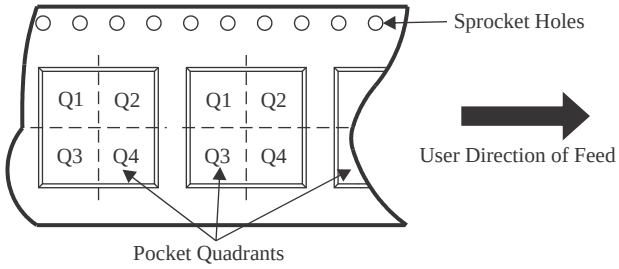


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

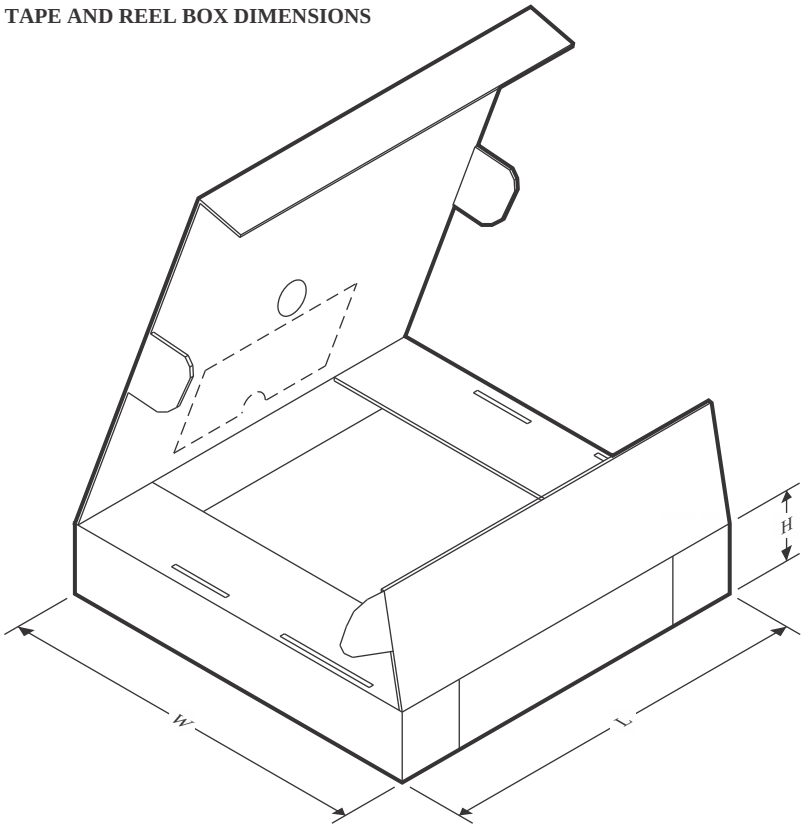
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL022CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL022CPSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1

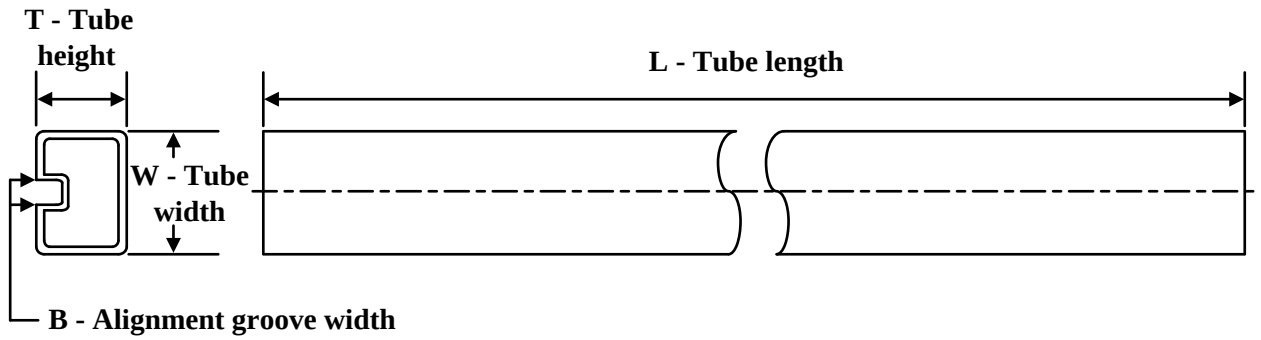
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

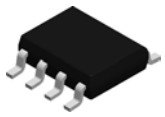
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL022CDR	SOIC	D	8	2500	340.5	338.1	20.6
TL022CPSR	SO	PS	8	2000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TL022CD	D	SOIC	8	75	507	8	3940	4.32
TL022CP	P	PDIP	8	50	506	13.97	11230	4.32

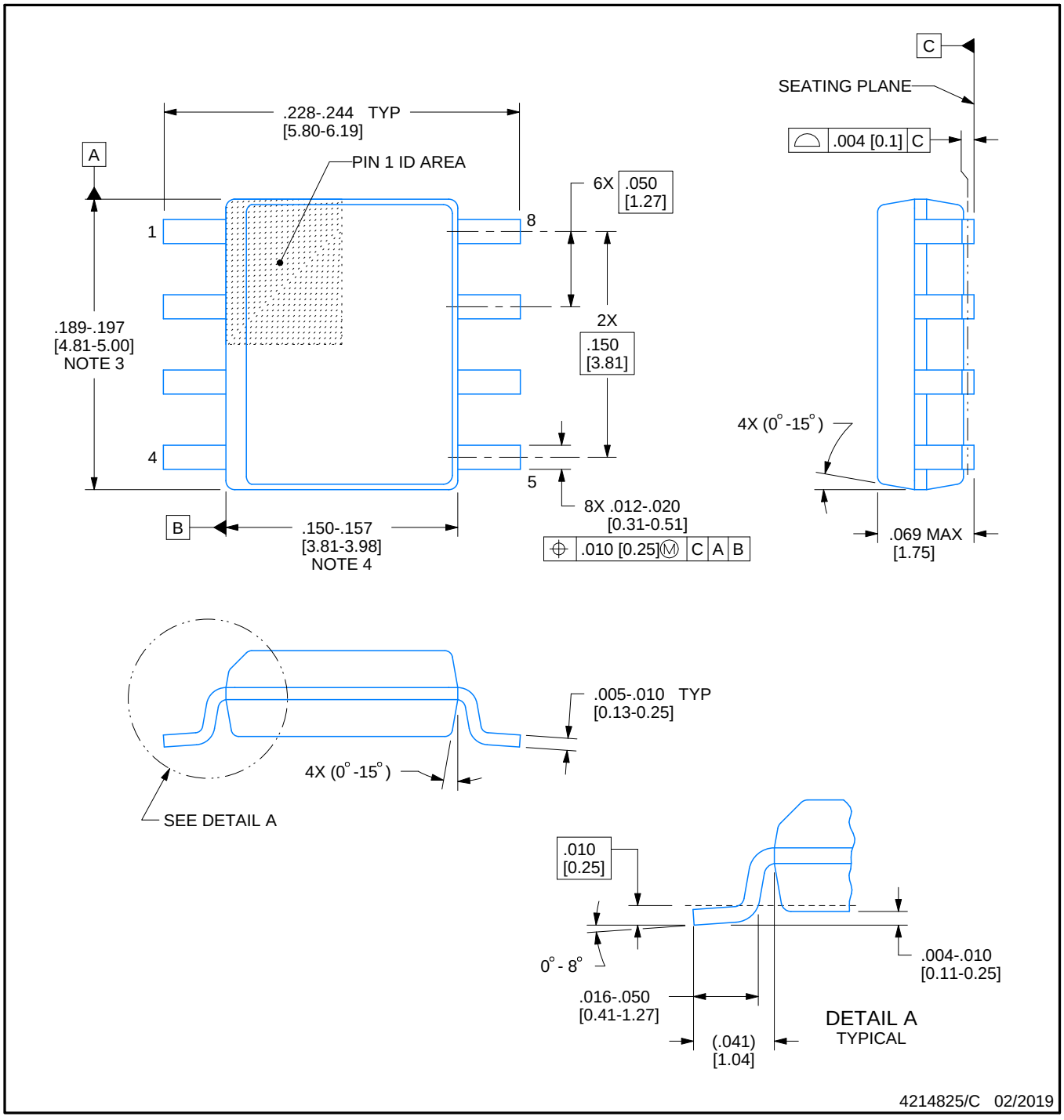


PACKAGE OUTLINE

D0008A

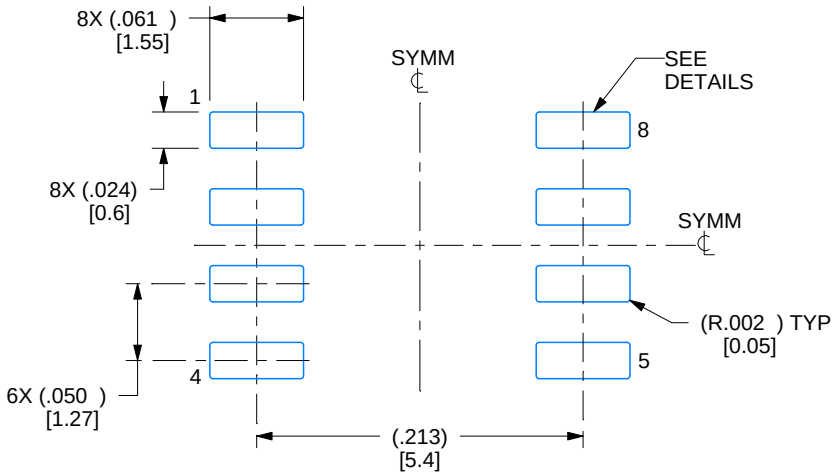
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

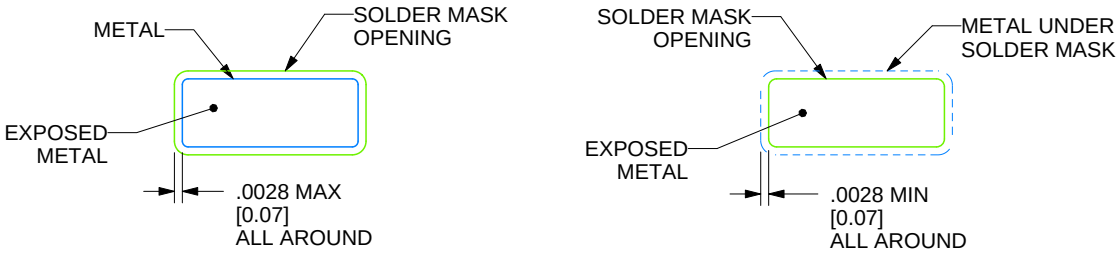


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

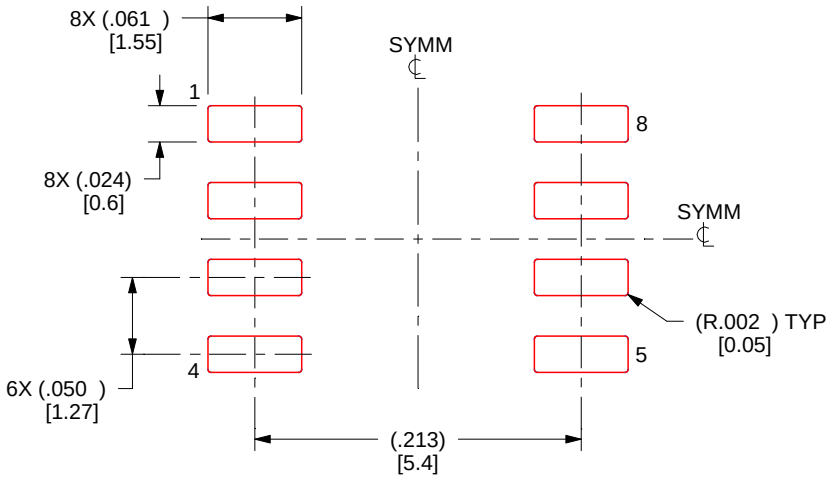
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

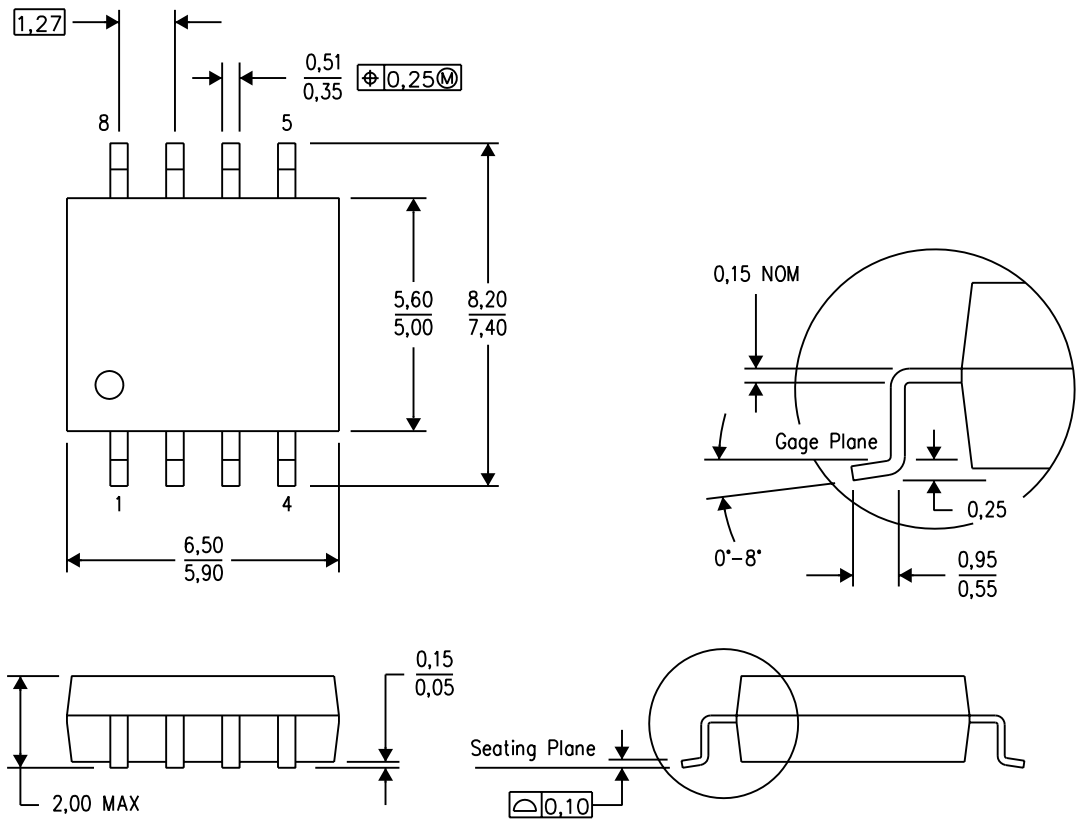
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

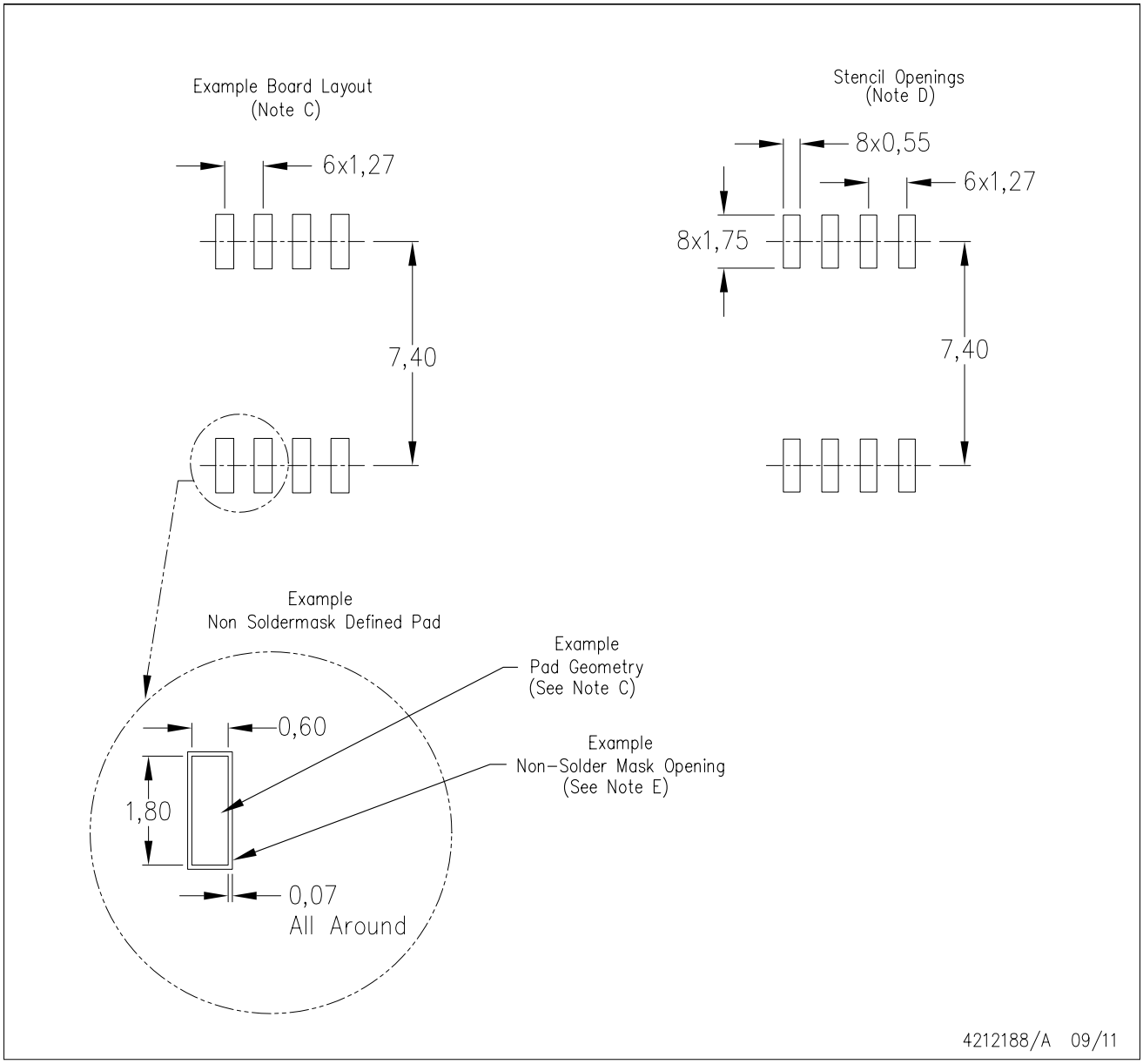
PS (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



4040063/C 03/03

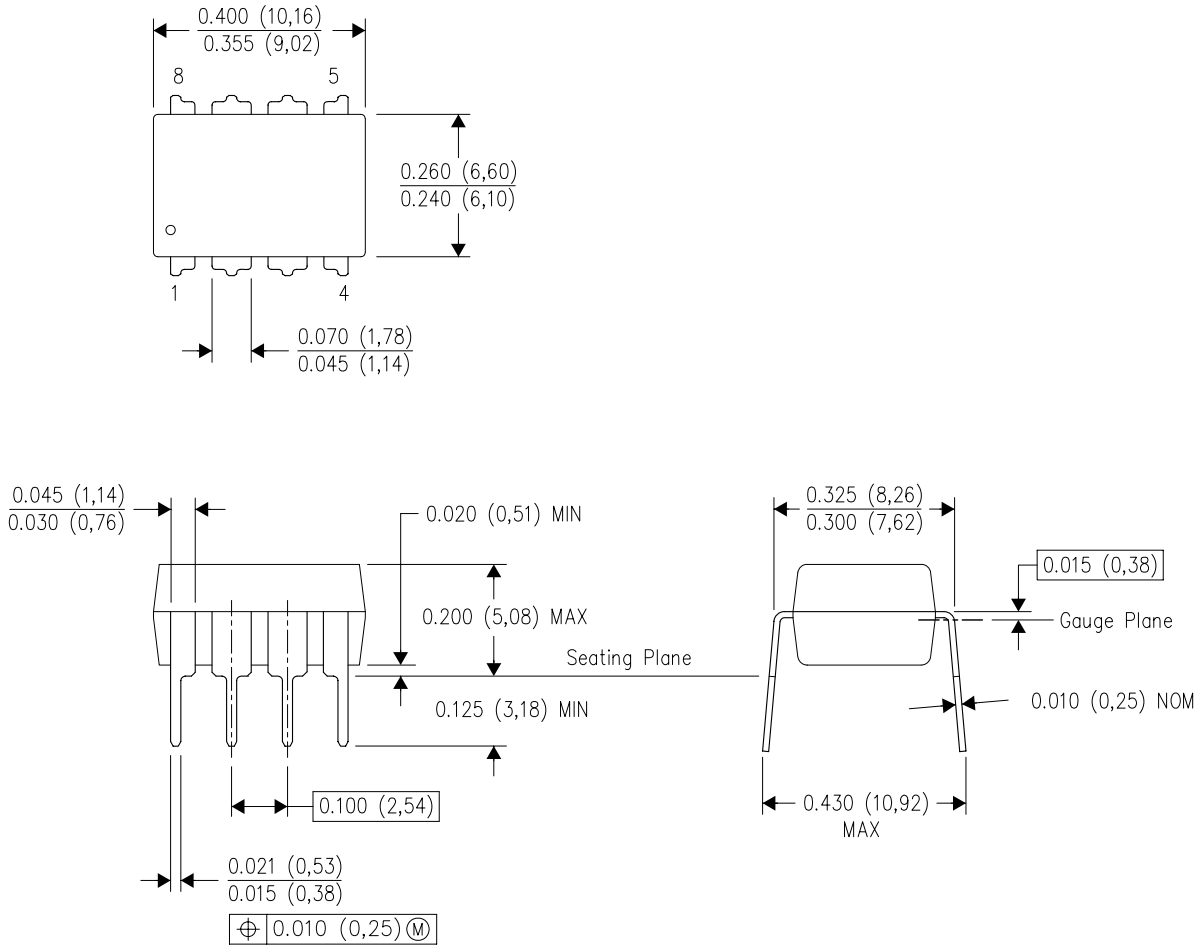
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PS (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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