# TLVx376 Low Offset and Drift, Low-Noise, Precision Operational Amplifiers for Cost-Sensitive Systems

## 1 Features

- Low Noise: 8 nV/√Hz at 1 kHz
- 0.1-Hz to 10-Hz Noise: 1.6 $\mu V_{PP}$
- Quiescent Current: 815 μA (typical)
- Low Offset Voltage (typical):
  - Single and Dual Versions: 40 μV
  - Quad Version: 50 μV
- Gain Bandwidth Product: 5.5 MHz
- Rail-to-Rail Input and Output
- Single-Supply Operation
- Supply Voltage: 2.2 V to 5.5 V
- Industry-Standard Packages:
  - SOT-23, SOIC, VSSOP, TSSOP

## 2 Applications

- Solar Inverters
- Medical Instrumentation
- ADC Buffers
- Handheld Test Equipment
- Active Filtering
- Sensor Conditioning

## 3 Description

The TLVx376 family represents a new generation of low-noise operational amplifiers with e-trim™, offering both excellent dc precision and ac performance. Rail-to-rail input and output, low offset (125 μV, maximum), low noise (8 nV/√Hz), a quiescent current of 1.2 mA (maximum), and a 5.5-MHz bandwidth with a fast slew rate of 2 V/μs make this family of devices very attractive for a variety of precision and portable applications. In addition, these devices have a reasonably wide supply range with excellent PSRR, making the family ideal for applications that run directly from batteries without regulation.

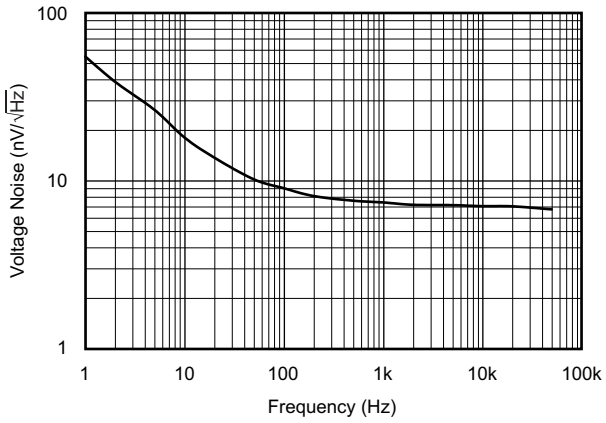
The TLV376 (single version) is available in SOT-23-5 and SOIC-8 packages. The TLV2376 (dual) is offered in VSSOP-8 and SOIC-8 packages. The TLV4376 (quad) is offered in a TSSOP-14 package. All versions are specified for operation from –40°C to +125°C.

**Device Information**(1)

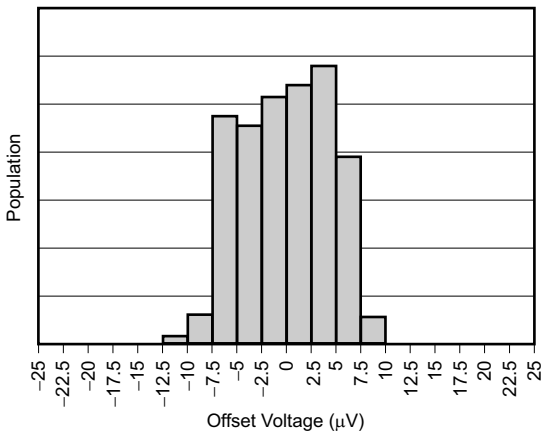
| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| TLV376 | SOIC (8) | 4.90 mm × 3.91 mm |
| | SOT-23 (5) | 2.90 mm × 1.60 mm |
| TLV2376 | SOIC (8) | 4.90 mm × 3.91 mm |
| | VSSOP (8) | 3.00 mm × 3.00 mm |
| TLV4376 | PW (14) | 5.00 mm × 4.40 mm |

(1) For all available packages, see the package option addendum at the end of the data sheet.

**INPUT VOLTAGE NOISE SPECTRAL DENSITY**




**OFFSET VOLTAGE PRODUCTION DISTRIBUTION**




An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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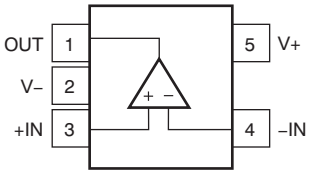
## 4 Revision History

| DATE | REVISION | NOTES |
|---|---|---|
| October 2016 | * | Initial release. |

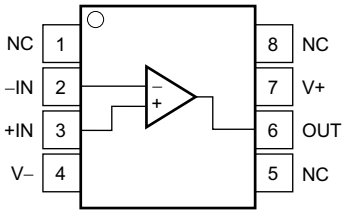

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# 5 Pin Configuration and Functions

**TLV376: DBV Package**
**5-Pin SOT23**
**Top View**



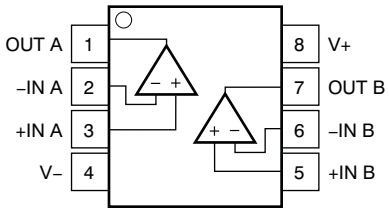

**TLV376: D Package**
**8-Pin SOIC**
**Top View**




**Pin Functions: TLV376**

| PIN | | | I/O | DESCRIPTION |
|---|---|---|---|---|
| NAME | DBV | D | | |
| –IN | 4 | 2 | I | Negative input signal |
| +IN | 3 | 3 | I | Positive input signal |
| NC | — | 1, 5, 8 | — | No connection |
| OUT | 1 | 6 | O | Output signal |
| V– | 2 | 4 | — | Negative supply voltage |
| V+ | 5 | 7 | — | Positive supply voltage |

**TLV2376: D and DGK Packages**
**8-Pin SOIC and 8-Pin VSSOP**
**Top View**

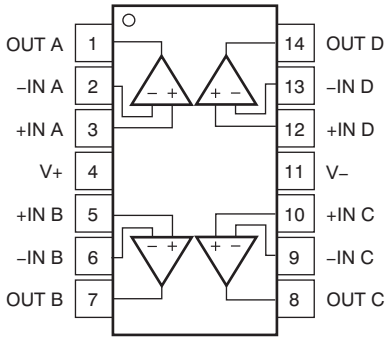



**Pin Functions: TLV2376**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | D, DGK | | |
| –IN A | 2 | I | Inverting input, channel A |
| –IN B | 6 | I | Inverting input, channel B |
| +IN A | 3 | I | Noninverting input, channel A |
| +IN B | 5 | I | Noninverting input, channel B |
| OUT A | 1 | O | Output, channel A |
| OUT B | 7 | O | Output, channel B |
| V– | 4 | — | Negative supply voltage |
| V+ | 8 | — | Positive supply voltage |

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**TLV4376: PW Package**
**14-Pin TSSOP**
**Top View**




## Pin Functions: TLV4376

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | PW | | |
| –IN A | 2 | O | Inverting input, channel A |
| –IN B | 6 | O | Inverting input, channel B |
| –IN C | 9 | O | Inverting input, channel C |
| –IN D | 13 | O | Inverting input, channel D |
| +IN A | 3 | I | Noninverting input, channel A |
| +IN B | 5 | I | Noninverting input, channel B |
| +IN C | 10 | I | Noninverting input, channel C |
| +IN D | 12 | I | Noninverting input, channel D |
| OUT A | 1 | O | Output, channel A |
| OUT B | 7 | O | Output, channel B |
| OUT C | 8 | O | Output, channel C |
| OUT D | 14 | O | Output, channel D |
| V– | 11 | — | Negative supply voltage |
| V+ | 4 | — | Positive supply voltage |


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# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Voltage | Supply, $V_S$ = (V+) – (V–) | | 7 | V |
| | Signal input pin(2) | (V–) – 0.5 | (V+) + 0.5 | V |
| Current | Signal input pin(2) | –10 | 10 | mA |
| | Output short-circuit(3) | Continuous | | |
| Temperature | Specified, $T_A$ | –40 | 125 | °C |
| | Junction, $T_J$ | | 150 | |
| | Storage, $T_{stg}$ | –65 | 150 | |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input pins are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails must be current limited to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±4000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101(2) | ±1000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Supply voltage, $V_S$ = (V+) – (V–) | Single supply | 2.2 | | 5.5 | V |
| | Dual supply | ±1.1 | | ±2.75 | |
| $T_A$ Specified temperature range | | –40 | | 125 | °C |

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## 6.4 Thermal Information: TLV376

| THERMAL METRIC(1) | | TLV376 | | UNIT |
|---|---|---|---|---|
| | | D (SOIC) | DBV (SOT-23) | |
| | | 8 PINS | 5 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 100.1 | 273.8 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 42.4 | 126.8 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 41.0 | 85.9 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 4.8 | 10.9 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 40.3 | 84.9 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | n/a | n/a | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 6.5 Thermal Information: TLV2376

| THERMAL METRIC(1) | | TLV2376 | | UNIT |
|---|---|---|---|---|
| | | D (SOIC) | DGK (VSSOP) | |
| | | 8 PINS | 8 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 111.1 | 171.2 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 54.7 | 63.9 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 51.7 | 92.8 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 10.5 | 9.2 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 51.2 | 91.2 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | n/a | n/a | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 6.6 Thermal Information: TLV4376

| THERMAL METRIC(1) | | TLV4376 | UNIT |
|---|---|---|---|
| | | PW (TSSOP) | |
| | | 14 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 107.8 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 29.6 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 52.6 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 1.5 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 51.6 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | n/a | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.


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## 6.7 Electrical Characteristics

at $T_A$ = 25°C, $R_L$ = 10 kΩ connected to $V_S$ / 2, $V_{CM}$ = $V_S$ / 2, and $V_{OUT}$ = $V_S$ / 2 (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **OFFSET VOLTAGE** | | | | | | |
| $V_{OS}$ | Input offset voltage | TLV376, TLV2376 | | 40 | 100 | µV |
| | | TLV4376 | | 50 | 125 | |
| $dV_{OS}/dT$ | Offset voltage vs temperature | $T_A$ = –40°C to +125°C | | 1.0 | | µV/°C |
| PSRR | Power-supply rejection ratio | $V_S$ = 2.2 V to 5.5 V, $V_{CM}$ < (V+) – 1.3 V | 84 | 110 | | dB |
| | Channel separation, dc | TLV2376, TLV4376 | | 0.5 | | mV/V |
| **INPUT BIAS CURRENT** | | | | | | |
| $I_B$ | Input bias current | | | 0.3 | | pA |
| | | $T_A$ = –40°C to +125°C | | See *Typical Characteristics* | | |
| $I_{OS}$ | Input offset current | | | 0.2 | | pA |
| **NOISE** | | | | | | |
| | Input voltage noise | f = 0.1 Hz to 10 Hz | | 2.2 | | $\mu V_{PP}$ |
| $e_n$ | Input voltage noise density | f = 1 kHz | | 8.0 | | $nV/\sqrt{Hz}$ |
| $i_n$ | Input current noise | f = 1 kHz | | 2 | | $fA/\sqrt{Hz}$ |
| **INPUT VOLTAGE RANGE** | | | | | | |
| $V_{CM}$ | Common-mode voltage range | | (V–) – 0.1 | | (V+) + 0.1 | V |
| CMRR | Common-mode rejection ratio | (V–) < $V_{CM}$ < (V+) – 1.3 V | 72 | 88 | | dB |
| **INPUT CAPACITANCE** | | | | | | |
| | Differential | | | 6.5 | | pF |
| | Common-mode | | | 13 | | pF |
| **OPEN-LOOP GAIN** | | | | | | |
| $A_{OL}$ | Open-loop voltage gain | 100 mV < $V_O$ < (V+) – 100 mV, $R_L$ = 2 kΩ | 100 | 126 | | dB |
| **FREQUENCY RESPONSE ($C_L$ = 100 pF, $V_S$ = 5.5 V)** | | | | | | |
| GBW | Gain-bandwidth product | | | 5.5 | | MHz |
| SR | Slew rate | G = 1 | | 2 | | V/µs |
| $t_S$ | Settling time | To 0.1%, 2-V step , G = 1 | | 1.6 | | µs |
| | | To 0.01%, 2-V step , G = 1 | | 2 | | |
| | Overload recovery time | $V_{IN}$ × gain > $V_S$ | | 0.33 | | µs |
| THD+N | Total harmonic distortion + noise | $V_O$ = 1 $V_{RMS}$, G = 1, f = 1 kHz, $R_L$ = 10 kΩ | | 0.0005% | | |
| **OUTPUT** | | | | | | |
| | Voltage output swing from rail | $R_L$ = 10 kΩ | | 10 | 20 | mV |
| $I_{SC}$ | Short-circuit current | Sourcing | | 30 | | mA |
| | | Sinking | | –50 | | |
| $C_{LOAD}$ | Capacitive load drive | | | See *Typical Characteristics* | | |
| $R_O$ | Open-loop output impedance | | | 150 | | Ω |
| **POWER SUPPLY** | | | | | | |
| $V_S$ | Specified voltage range | | 2.2 | | 5.5 | V |
| | Operating voltage range | | | 2 to 5.5 | | V |
| $I_Q$ | Quiescent current per amplifier | $I_O$ = 0 mA, $V_S$ = 5.5 V, $V_{CM}$ < (V+) – 1.3 V | | 815 | 1200 | µA |
| **TEMPERATURE** | | | | | | |
| | Specified range | | –40 | | 125 | °C |

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## 6.8 Typical Characteristics

at $T_A$ = 25°C, $V_S$ = 5 V, $R_L$ = 10 kΩ connected to $V_S$ / 2, $V_{CM}$ = $V_S$ / 2, and $V_{OUT}$ = $V_S$ / 2 (unless otherwise noted)

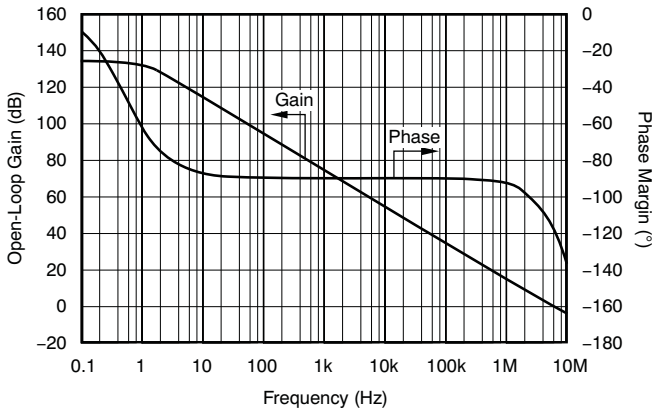



**Figure 1. Open-Loop Gain and Phase vs Frequency**

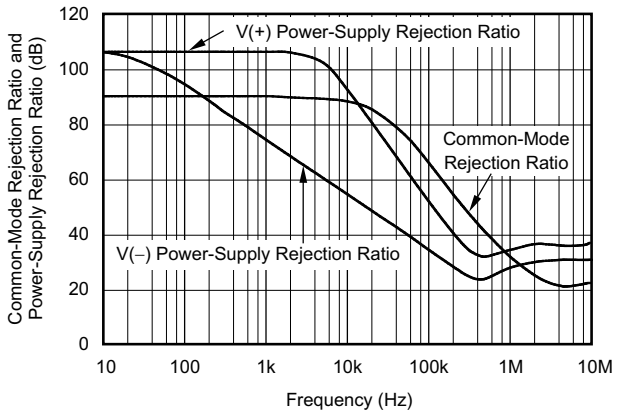



**Figure 2. Power-Supply and Common-Mode Rejection Ratio vs Frequency**

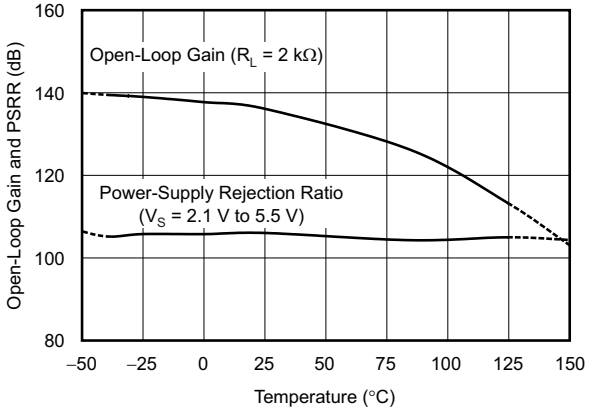



**Figure 3. Open-Loop Gain and Power-Supply Rejection Ratio vs Temperature**

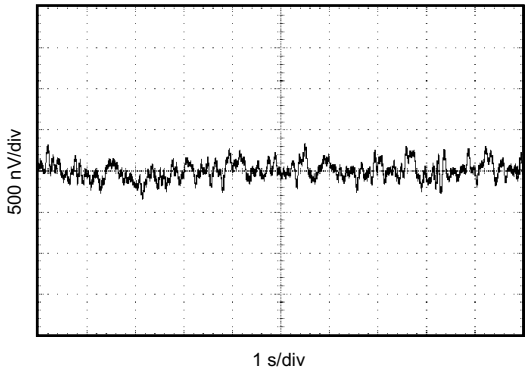



**Figure 4. 0.1-Hz to 10-Hz Input Voltage Noise**

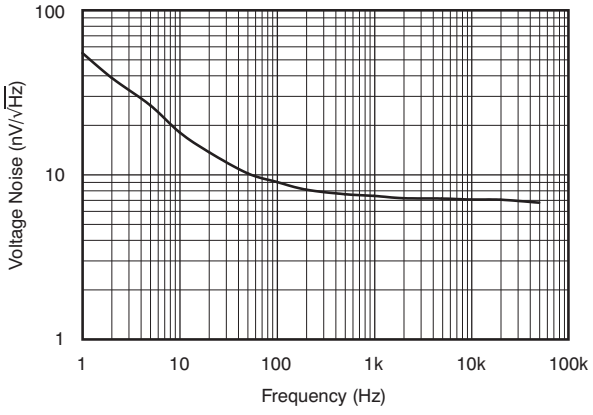



**Figure 5. Input Voltage Noise Spectral Density**

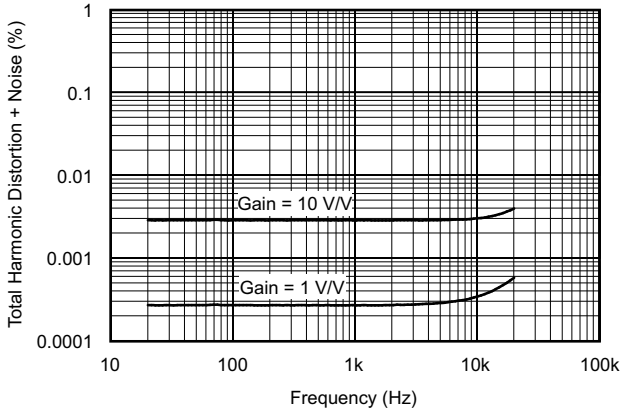



**Figure 6. Total Harmonic Distortion + Noise vs Frequency**


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## Typical Characteristics (continued)

at $T_A$ = 25°C, $V_S$ = 5 V, $R_L$ = 10 kΩ connected to $V_S$ / 2, $V_{CM}$ = $V_S$ / 2, and $V_{OUT}$ = $V_S$ / 2 (unless otherwise noted)

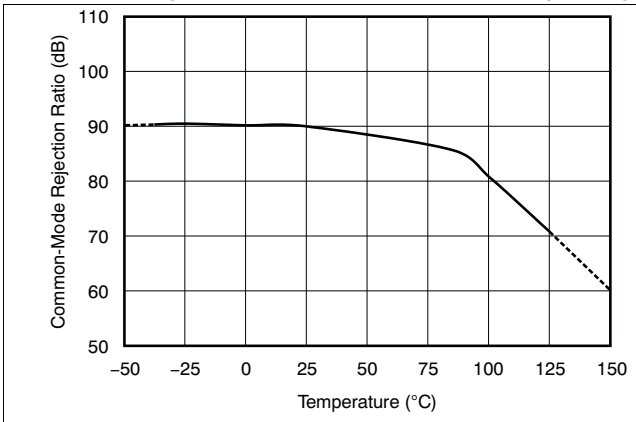



**Figure 7. Common-Mode Rejection Ratio vs Temperature**

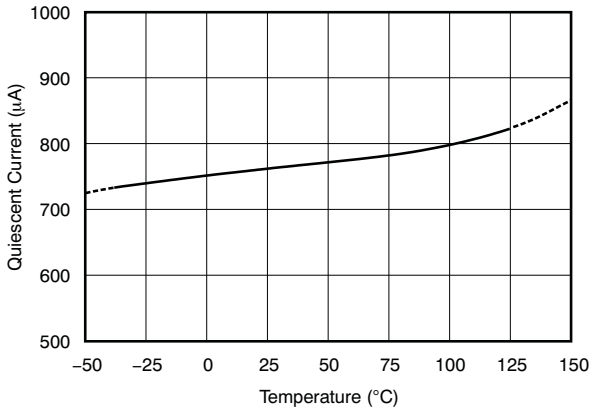



**Figure 8. Quiescent Current vs Temperature**

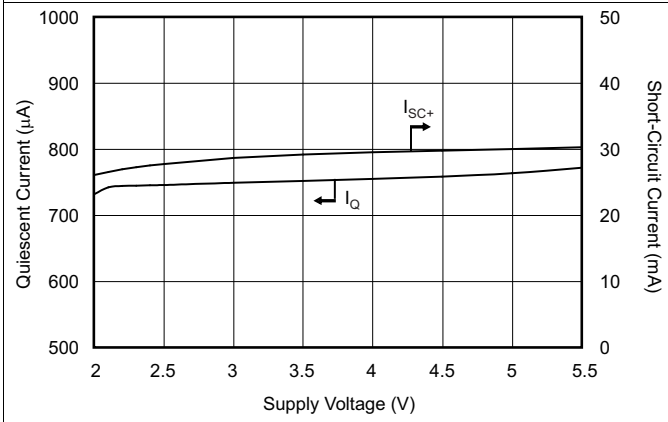



**Figure 9. Quiescent and Short-Circuit Current vs Supply Voltage**

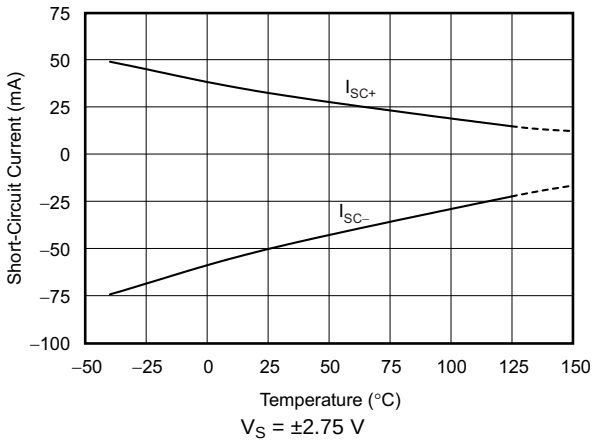



**Figure 10. Short-Circuit Current vs Temperature**

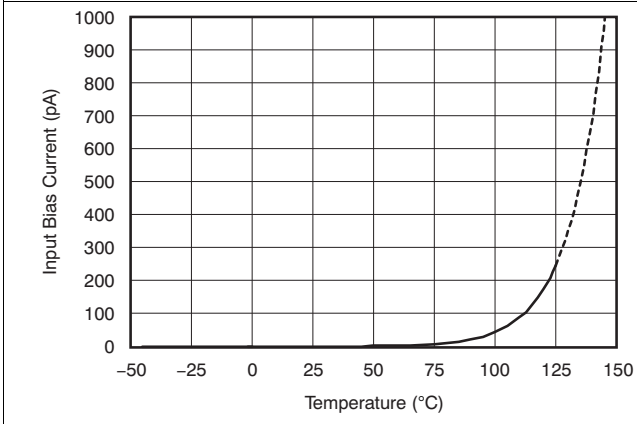



**Figure 11. Input Bias Current vs Temperature**

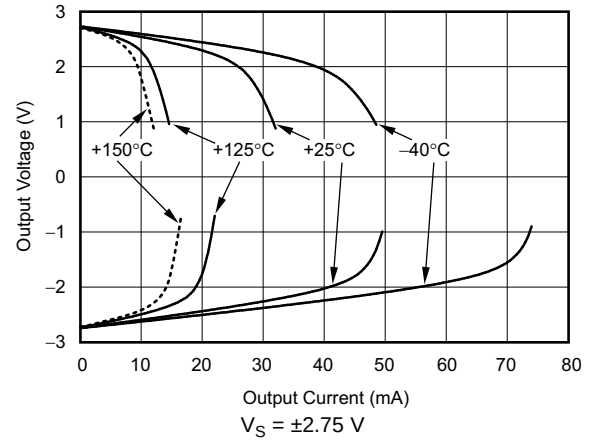



**Figure 12. Output Voltage vs Output Current**

## Typical Characteristics (continued)

at $T_A$ = 25°C, $V_S$ = 5 V, $R_L$ = 10 kΩ connected to $V_S$ / 2, $V_{CM}$ = $V_S$ / 2, and $V_{OUT}$ = $V_S$ / 2 (unless otherwise noted)

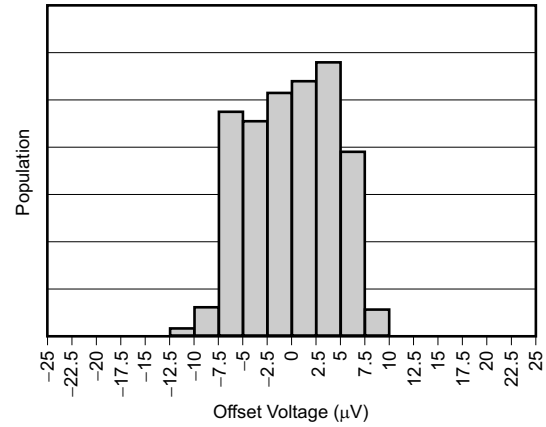



**Figure 13. Offset Voltage Production Distribution Histogram**

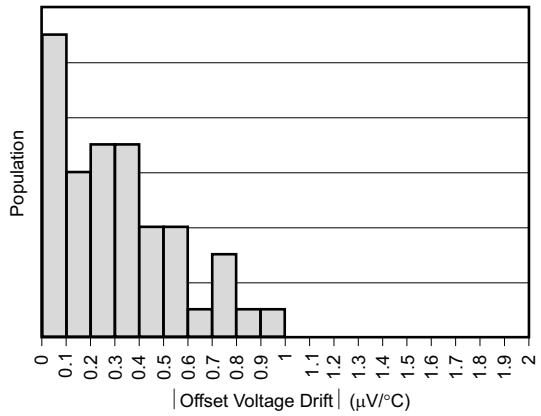



**Figure 14. Offset Voltage Drift Production Distribution Histogram (–40°C to 125°C)**

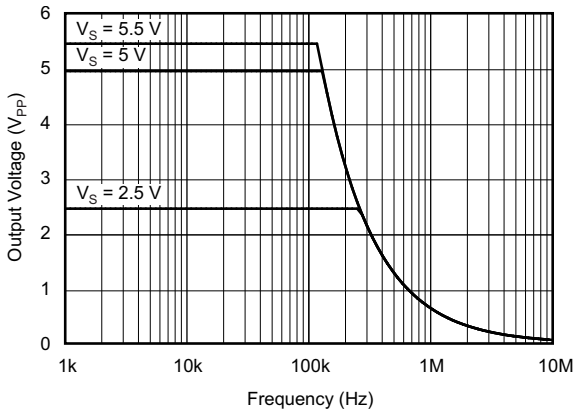



**Figure 15. Maximum Output Voltage vs Frequency**

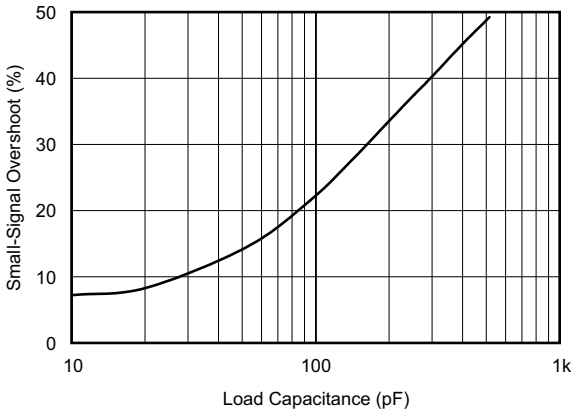
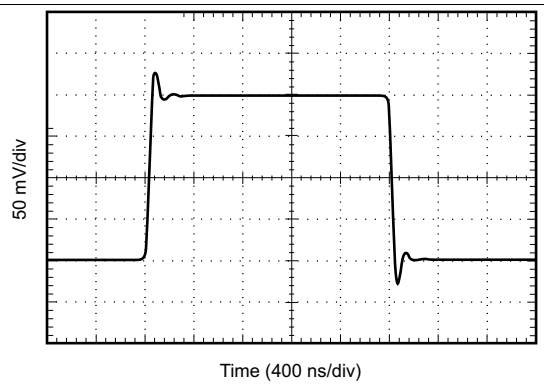
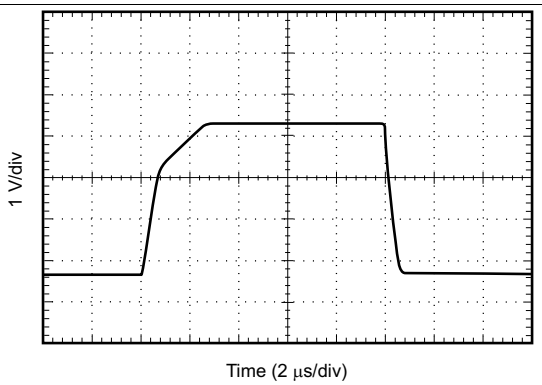



**Figure 16. Small-Signal Overshoot vs Load Capacitance**




G = +1 V/V, $R_L$ = 10 kΩ, $C_L$ = 50 pF

**Figure 17. Small-Signal Pulse Response**




G = +1 V/V, $R_L$ = 2 kΩ, $C_L$ = 50 pF

**Figure 18. Large-Signal Pulse Response**


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## Typical Characteristics (continued)

at $T_A$ = 25°C, $V_S$ = 5 V, $R_L$ = 10 kΩ connected to $V_S$ / 2, $V_{CM}$ = $V_S$ / 2, and $V_{OUT}$ = $V_S$ / 2 (unless otherwise noted)

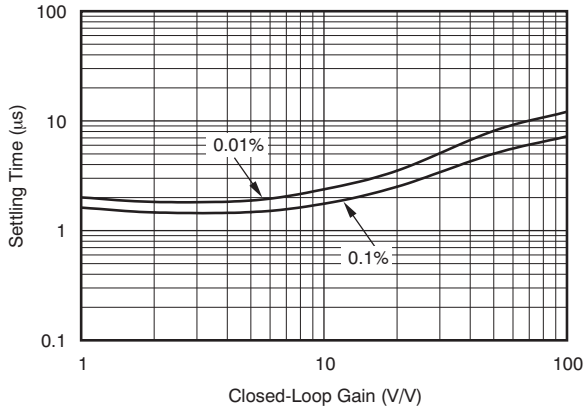



**Figure 19. Settling Time vs Closed-Loop Gain**

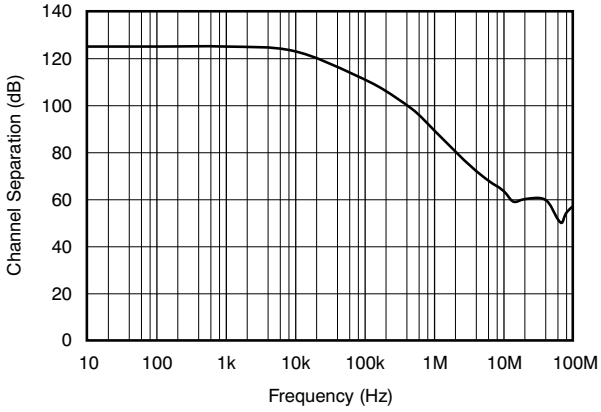



**Figure 20. Channel Separation vs Frequency**

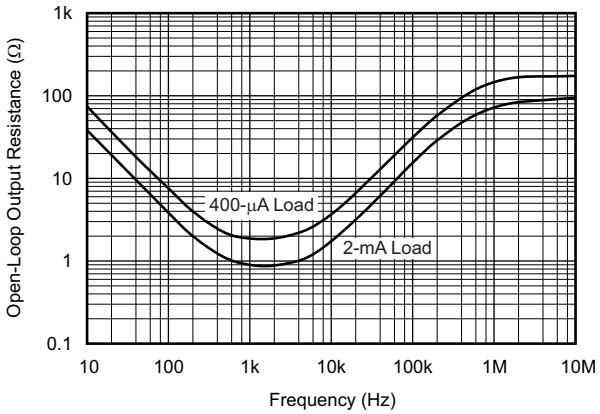


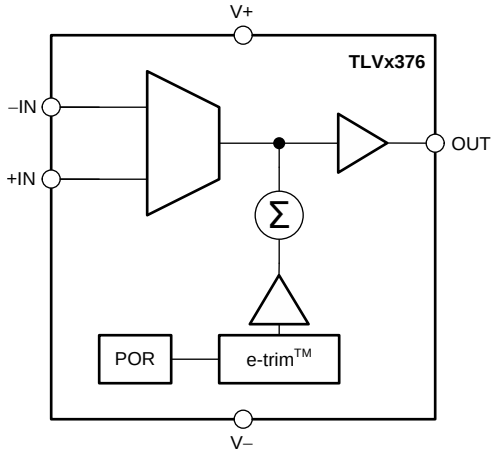

**Figure 21. Open-Loop Output Resistance vs Frequency**

# 7 Detailed Description

## 7.1 Overview

The TLVx376 family belongs to a new generation of low-noise operational amplifiers with e-trim™, giving customers outstanding dc precision and ac performance. Low noise, rail-to-rail input and output, and low offset, drawing a low quiescent current, make these devices ideal for a variety of precision and portable applications. In addition, this family of devices have a wide supply range with excellent PSRR, making the TLVx376 a suitable option for applications that are battery-powered without regulation.

## 7.2 Functional Block Diagram




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## 7.3 Feature Description

The TLVx376 family of precision amplifiers offers excellent dc performance as well as excellent ac performance. Operating from a single power supply, the TLVx376 is capable of driving large capacitive loads, has a wide input common-mode voltage range, and is well-suited to drive the inputs of successive-approximation register (SAR) analog-to-digital converters (ADCs) as well as 24-bit and higher resolution converters. All devices feature internal ESD protection. The TLVx376 family is offered in a variety of industry-standard packages for applications that require space savings.

### 7.3.1 Operating Voltage

The TLVx376 family of amplifiers operate over a power-supply range of 2.2 V to 5.5 V (±1.1 V to ±2.75 V). Many of the specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics* section.

### 7.3.2 Capacitive Load and Stability

The TLVx376 series of amplifiers can be used in applications where driving a capacitive load is required. As with all op amps, there can be specific instances where the TLVx376 can become unstable, leading to oscillation. The particular op amp circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether an amplifier is stable in operation or not. An op amp in the unity-gain (+1 V/V) buffer configuration and driving a capacitive load exhibits a greater tendency to be unstable than an amplifier operated at a higher noise gain. The capacitive load, in conjunction with the op amp output resistance, creates a pole within the feedback loop that degrades the phase margin. The phase margin reduces when the capacitive loading increases.

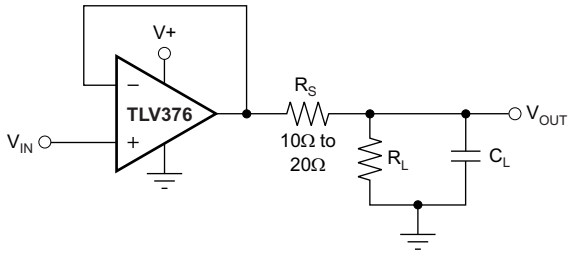

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## Feature Description (continued)

### 7.3.3 Input Offset Voltage and Input Offset Voltage Drift

The TLVx376 family of operational amplifiers is manufactured using TI's e-trim™ technology. Each amplifier is trimmed in production, thereby minimizing errors associated with input offset voltage and input offset voltage drift. The e-trim™ technology is a TI proprietary method of trimming internal device parameters during either wafer probing or final testing.

The TLVx376 in a unity-gain configuration can directly drive up to 250 pF of pure capacitive load. Increasing the gain enhances the ability of the amplifier to drive greater capacitive loads; see Figure 16. In unity-gain configurations, capacitive load drive can be improved by inserting a small (10 Ω to 20 Ω) resistor, $R_S$, in series with the output, as shown in Figure 22. This resistor significantly reduces ringing and maintains dc performance for purely capacitive loads. However, if there is a resistive load in parallel with the capacitive load, a voltage divider is created, introducing a gain error at the output and slightly reducing the output swing. The error introduced is proportional to the ratio $R_S$ / $R_L$, and is generally negligible at low output current levels.




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**Figure 22. Improving Capacitive Load Drive**

### 7.3.4 Common-Mode Voltage Range

The input common-mode voltage range of the TLVx376 series extends 100 mV beyond the supply rails. The offset voltage of the amplifier is very low, from approximately (V–) to (V+) – 1 V, as shown in Figure 23. The offset voltage increases when common-mode voltage exceeds (V+) –1 V. Common-mode rejection is specified from (V–) to (V+) – 1.3 V.

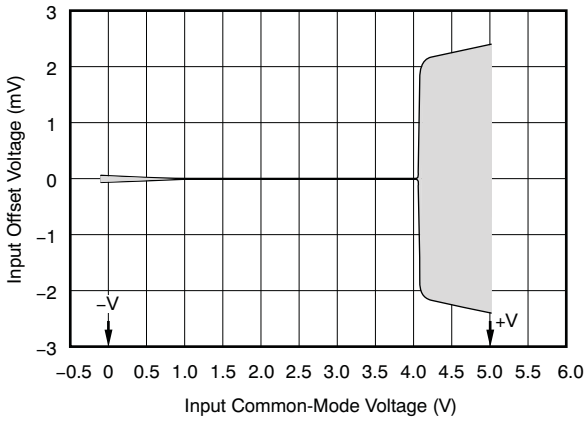



**Figure 23. Offset and Common-Mode Voltage**

## Feature Description (continued)

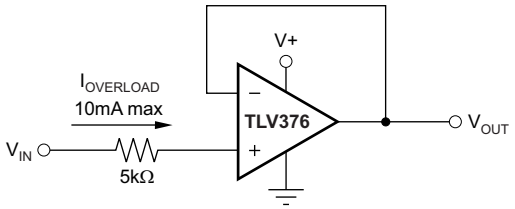
Parameters that can vary across the common-mode voltage range are listed in Table 1.

**Table 1. Parameters With Variation Across the Common-Mode Voltage Range**

| PARAMETER | | (V–) - 0.1 V < $V_{CM}$ < (V+) – 1.3 V | (V+) – 1.3 V < $V_{CM}$ < (V+) + 0.1 V | UNIT |
|---|---|---|---|---|
| | | TYP | TYP | |
| **OFFSET VOLTAGE** | | | | |
| $V_{OS}$ | Input offset voltage | 40 | 2500 | µV |
| $dV_{OS}/dT$ | Offset voltage vs temperature | 1 | 25 | µV/°C |
| **OPEN LOOP GAIN** | | | | |
| $A_{OL}$ | Open-loop voltage gain | 126 | 96 | dB |
| **INPUT VOLTAGE RANGE** | | | | |
| CMRR | Common-mode rejection ratio | 88 | 43 | dB |
| **FREQUENCY RESPONSE** | | | | |
| GBW | Gain-bandwidth product | 5.5 | 5.5 | MHz |
| PM | Phase margin | 72 | 72 | Degrees |
| SR | Slew rate, G = 1 | 2 | 1.1 | V/µs |
| **NOISE** | | | | |
| $e_n$ | Input voltage noise density, f = 1 kHz | 8 | 135 | nV/√Hz |
| $i_n$ | Input current noise, f = 1 kHz | 2 | 47 | fA/√Hz |

### 7.3.5 Input and ESD Protection

The TLVx376 family incorporates internal electrostatic discharge (ESD) protection circuits on all pins. In the case of input and output pins, this protection primarily consists of current-steering diodes connected between the input and power-supply pins. These ESD protection diodes also provide in-circuit, input overdrive protection, as long as the current is limited to 10 mA as stated in the *Absolute Maximum Ratings* table. Figure 24 shows how a series input resistor can be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input. In noise-sensitive applications, the value of this resistor must be as low as possible.




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**Figure 24. Input Current Protection**

## 7.4 Device Functional Modes

The TLVx376 family has a single functional mode and is operational when the power-supply voltage is greater than 2.2 V (±1.1 V). The maximum power-supply voltage for the TLVx376 family is 5.5 V (±2.75 V).


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# 8 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

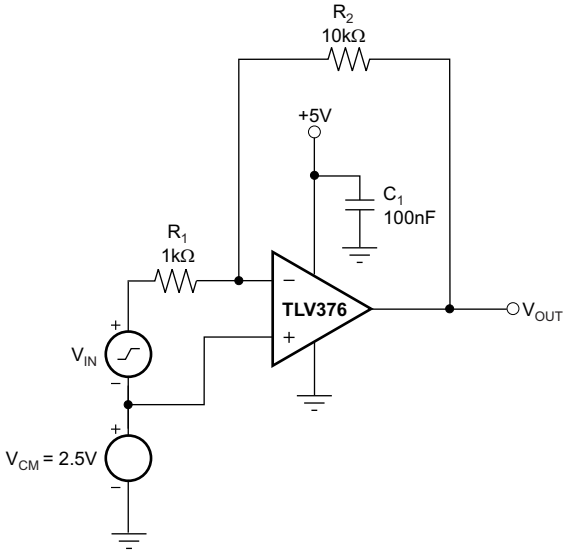
The TLV376 family of operational amplifiers is built using e-trim™, a proprietary technique in which offset voltage is adjusted during the final steps of manufacturing. This technique compensates for performance shifts that can occur during the molding process. Through e-trim™, the TLV376 family delivers excellent offset voltage (40 μV, typical). Additionally, the amplifier boasts a fast slew rate, low drift, low noise, and excellent PSRR and $A_{OL}$. These 5.5-MHz CMOS op amps only consume 815-μA (typical) quiescent current.

### 8.1.1 Operating Characteristics

The TLVx376 family of amplifiers has parameters that are fully specified from 2.2 V to 5.5 V (±1.1 V to ±2.75 V). Many of the specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics* section.

### 8.1.2 Basic Amplifier Configurations

The TLVx376 family is unity-gain stable. The TLVx376 does not exhibit output phase inversion when the input is overdriven. A typical single-supply connection is shown in Figure 25. The TLV376 is configured as a basic inverting amplifier with a gain of –10 V/V. This single-supply connection has an output centered on the common-mode voltage, $V_{CM}$. For the circuit shown, this voltage is 2.5 V, but can be any value within the common-mode input voltage range.



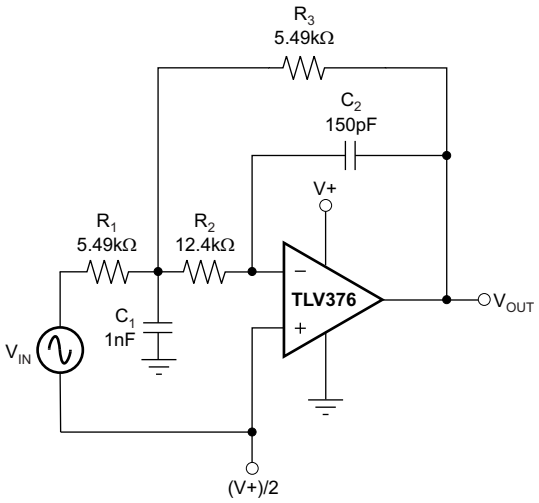

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**Figure 25. Basic Single-Supply Connection**

## Application Information (continued)

### 8.1.3 Active Filtering

The TLVx376 family is well-suited for filter applications requiring a wide-bandwidth, fast slew rate, low-noise, single-supply operational amplifier. Figure 26 shows a 50-kHz, 2nd-order, low-pass filter. The components have been selected to provide a maximally-flat Butterworth response. Beyond the cutoff frequency, roll-off is –40 dB per decade. The Butterworth response is ideal for applications requiring predictable gain characteristics (such as the antialiasing filter used ahead of an ADC).

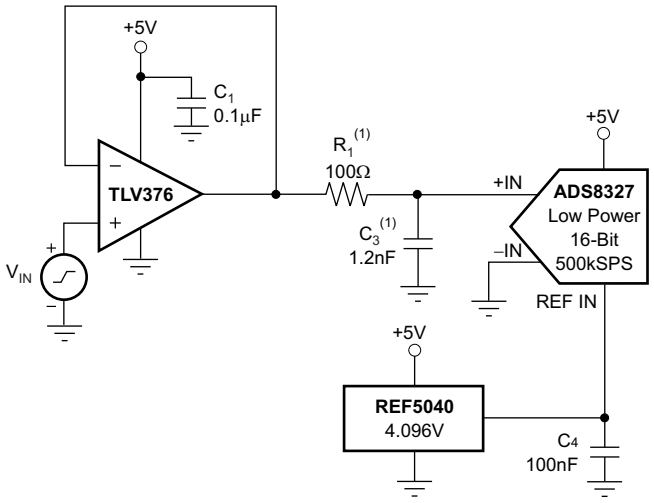



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**Figure 26. Second-Order, Butterworth, 50-kHz, Low-Pass Filter**

### 8.1.4 Driving an Analog-to-Digital Converter

The low-noise and wide-gain bandwidth of the TLVx376 family make these devices ideal for driving ADCs. Figure 27 shows the TLV376 driving an ADS8327, a 16-bit, 250-kSPS converter. The amplifier is connected as a unity-gain, noninverting buffer.




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NOTE: Suggested value; may require adjustment based on specific application.

**Figure 27. Driving an ADS8327**


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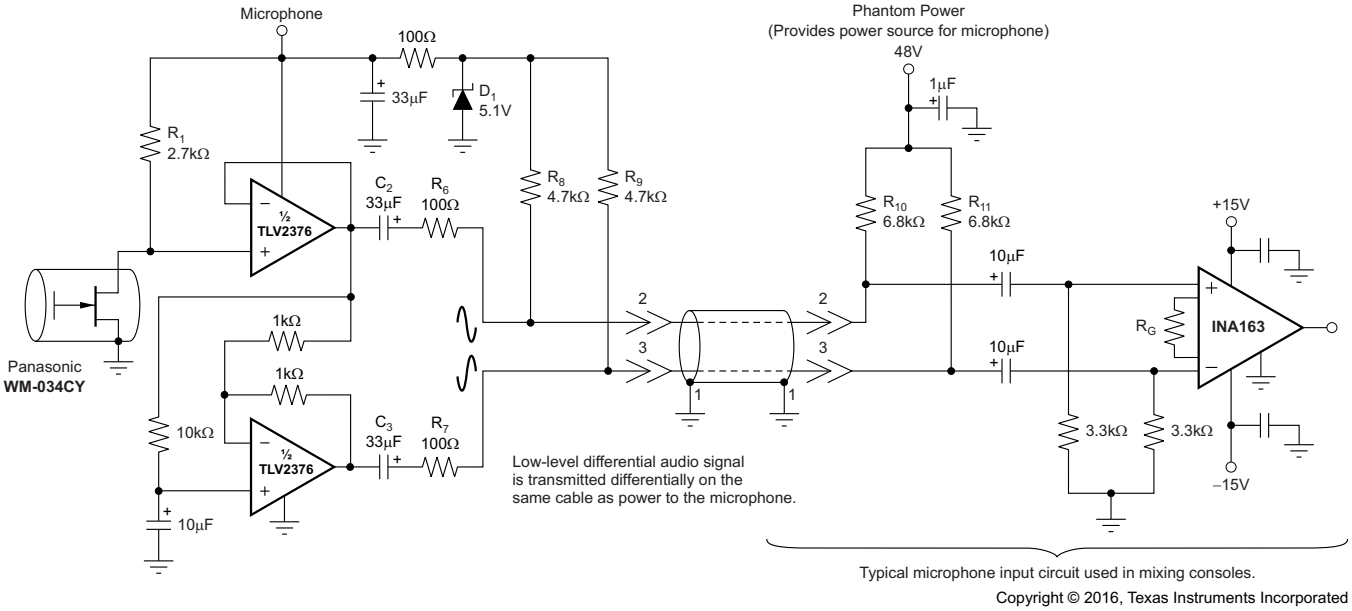
## Application Information (continued)

### 8.1.5 Phantom-Powered Microphone

The circuit shown in Figure 28 depicts how a remote microphone amplifier can be powered by a phantom source on the output side of the signal cable. The cable serves double duty, carrying both the differential output signal from and dc power to the microphone amplifier stage.

A TLV2376 serves as a single-ended input to a differential output amplifier with a 6-dB gain. Common-mode bias for the two op amps is provided by the dc voltage developed across the electret microphone element. A 48-V phantom supply is reduced to 5.1 V by the series 6.8-kΩ resistors on the output side of the cable, and the 4.7 kΩ and zener diode on the input side of the cable. AC coupling blocks the different dc voltage levels from each other on each end of the cable.

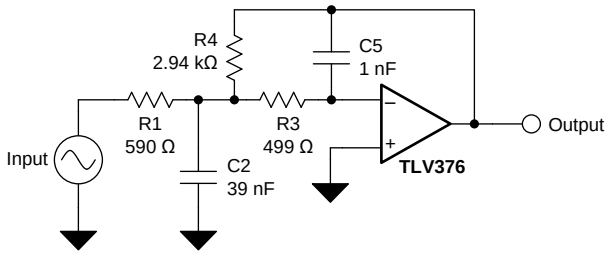
An INA163 instrumentation amplifier provides differential inputs and receives the balanced audio signals from the cable. The INA163 gain can be set from 0 dB to 80 dB by selecting the $R_G$ value. The INA163 circuit is typical of the input circuitry used in mixing consoles.




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**Figure 28. Phantom-Powered Electret Microphone**

## 8.2 Typical Application




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**Figure 29. Second-Order, Low-Pass Filter**

### 8.2.1 Design Requirements

Low-pass filters are commonly employed in signal-processing applications to reduce noise and prevent aliasing. The TLV376 is ideally suited to construct high-speed, high-precision active filters. Figure 29 shows a second-order, low-pass filter commonly encountered in signal-processing applications.

Use the following parameters for this design example:

- Gain = 5 V/V (inverting gain)
- Low-pass cutoff frequency = 25 kHz
- Second-order Chebyshev filter response with 3-dB gain peaking in the passband

### 8.2.2 Detailed Design Procedure

The infinite-gain multiple-feedback circuit for a low-pass network function is shown in the *Application Curve* section. Use Equation 1 to calculate the voltage transfer function.

$$\frac{\text{Output}}{\text{Input}}(s) = \frac{-1/R_1R_3C_2C_5}{s^2 + (s/C_2)(1/R_1 + 1/R_3 + 1/R_4) + 1/R_3R_4C_2C_5} \quad (1)$$

This circuit in Figure 29 produces a signal inversion. For this circuit, the gain at dc and the low-pass cutoff frequency are calculated by Equation 2:

$$\text{Gain} = \frac{R_4}{R_1}$$

$$f_C = \frac{1}{2\pi}\sqrt{(1/R_3R_4C_2C_5)} \quad (2)$$

Software tools are readily available to simplify filter design. The WEBENCH® filter designer is a simple, powerful, and easy-to-use active filter design program. The WEBENCH® filter designer allows optimized filter designs to be created by using a selection of TI operational amplifiers and passive components from TI's vendor partners.

Available as a web-based tool from the WEBENCH® design center, the WEBENCH® filter designer allows complete multistage active filter solutions to be designed, optimized, and simulated within minutes.


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## Typical Application (continued)

### 8.2.3 Application Curve

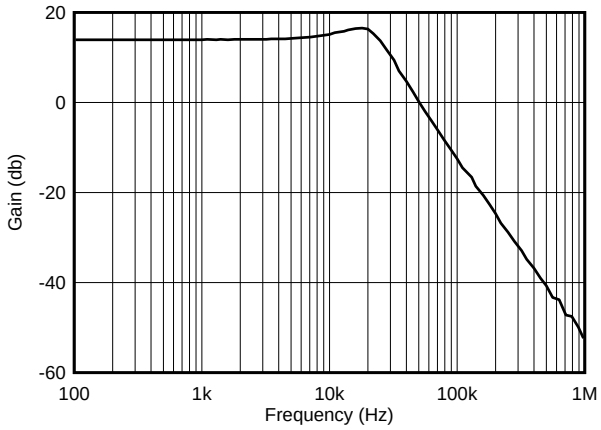



**Figure 30. Measured Frequency Response of the Second-Order, Low-Pass Filter**

# 9 Power Supply Recommendations

The TLVx376 family of devices are specified for operation from 2.2 V to 5.5 V (±1.1 V to ±2.75 V); many specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics* section.

# 10 Layout

## 10.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and the op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-equivalent series resistance (ESR), 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current. For more detailed information, see the *Circuit Board Layout Techniques* application report.
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As illustrated in Figure 32, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.

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## Layout Guidelines (continued)

- Any precision integrated circuit can experience performance shifts resulting from moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

## 10.2 Layout Example

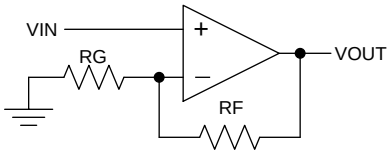



**Figure 31. Schematic Representation of Figure 32**

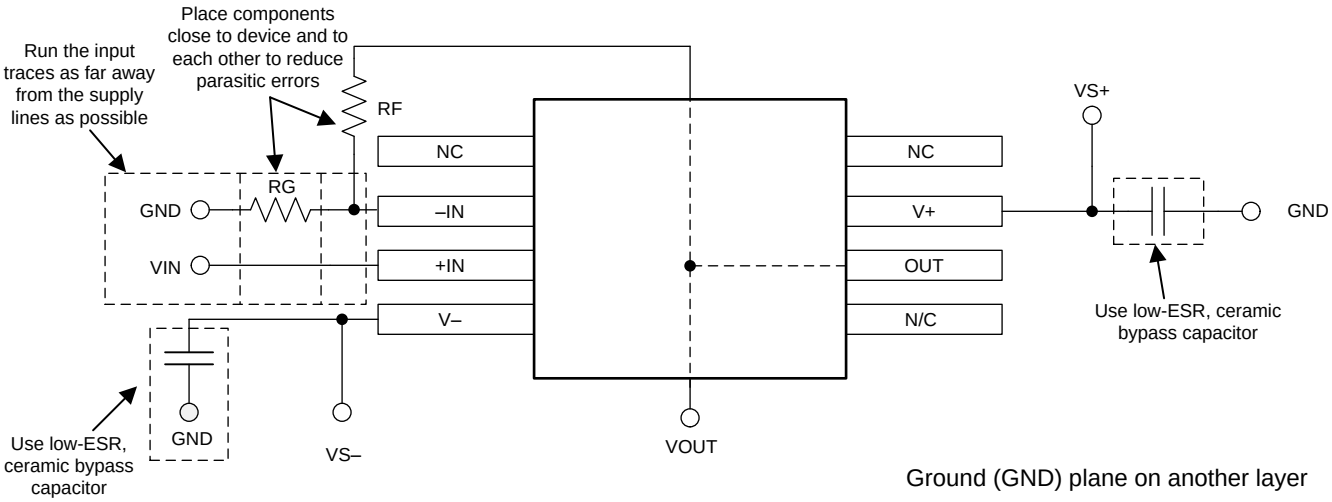



**Figure 32. Layout Example**


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# 11 Device and Documentation Support

## 11.1 Device Support

### 11.1.1 Development Support

#### *11.1.1.1 TINA-TI™ (Free Software Download)*

TINA-TI™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI™ is a free, fully-functional version of the TINA-TI™ software, preloaded with a library of macromodels in addition to a range of both passive and active models. TINA-TI™ provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI™ offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

**NOTE**

These files require that either the TINA software (from DesignSoft™) or TINA-TI™ software be installed. Download the free TINA-TI™ software from the TINA-TI™ folder.

#### *11.1.1.2 TI Precision Designs*

TI Precision Designs are analog solutions created by TI's precision analog applications experts and offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits. TI Precision Designs are available online at www.ti.com/ww/en/analog/precision-designs/.

#### *11.1.1.3 WEBENCH® Filter Designer*

WEBENCH® Filter Designer is a simple, powerful, and easy-to-use active filter design program. The WEBENCH® Filter Designer lets you create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners.

Available as a web-based tool from the WEBENCH® Design Center, WEBENCH® Filter Designer allows you to design, optimize, and simulate complete multistage active filter solutions within minutes.

## 11.2 Documentation Support

### 11.2.1 Related Documentation

For related documentation see the following:

- *Circuit Board Layout Techniques* Application Report (SLOA089)
- *Operational amplifier gain stability, Part 3: AC gain-error analysis* Application Report (SLYT383)
- *Operational amplifier gain stability, Part 2: DC gain-error analysis* Application Report (SLYT374)
- *Using infinite-gain, MFB filter topology in fully differential active filters* Application Report (SLYT343)
- *Op Amp Performance Analysis* Application Report (SBOA054)
- *Single-Supply Operation of Operational Amplifiers* Application Report (SBOA059)
- *Tuning in Amplifiers* Application Report (SBOA067)
- *Shelf-Life Evaluation of Lead-Free Component Finishes* Application Report (SZZA046)
- *ADS832x Low Power, 16-Bit, 500-kHz, Single/Dual Unipolar Input, Analog-to-Digital Converters With Serial Interface* (SLAS415)
- *REF50xx Low-Noise, Very Low Drift, Precision Voltage Reference* (SBOS410)
- *INA163 Low-Noise, Low-Distortion Instrumentation Amplifier* (SBOS177)
- *ADS7822 12-Bit, 200kHz, microPower Sampling Analog-to-Digital Converter* (SBAS062)

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## 11.3 Related Links

Table 2 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 2. Related Links**

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---|---|---|---|---|---|
| TLV376 | Click here | Click here | Click here | Click here | Click here |
| TLV2376 | Click here | Click here | Click here | Click here | Click here |
| TLV4376 | Click here | Click here | Click here | Click here | Click here |

## 11.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on Alert me to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 11.5 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 11.6 Trademarks

e-trim, TINA-TI, E2E are trademarks of Texas Instruments.
DesignSoft is a trademark of DesignSoft, Inc.
All other trademarks are the property of their respective owners.

## 11.7 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 11.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.


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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TLV2376IDGKR | ACTIVE | VSSOP | DGK | 8 | 2500 | RoHS & Green | NIPDAU \| SN \| NIPDAUAG | Level-2-260C-1 YEAR | -40 to 125 | 13F6 | Samples |
| TLV2376IDGKT | ACTIVE | VSSOP | DGK | 8 | 250 | RoHS & Green | NIPDAU \| SN \| NIPDAUAG | Level-2-260C-1 YEAR | -40 to 125 | 13F6 | Samples |
| TLV2376IDR | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | TLV 2376 | Samples |
| TLV376IDBVR | ACTIVE | SOT-23 | DBV | 5 | 3000 | RoHS & Green | NIPDAU \| SN | Level-2-260C-1 YEAR | -40 to 125 | 12J | Samples |
| TLV376IDBVT | ACTIVE | SOT-23 | DBV | 5 | 250 | RoHS & Green | NIPDAU \| SN | Level-2-260C-1 YEAR | -40 to 125 | 12J | Samples |
| TLV376IDR | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | TLV 15M | Samples |
| TLV4376IPWR | ACTIVE | TSSOP | PW | 14 | 2000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | TLV4376 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

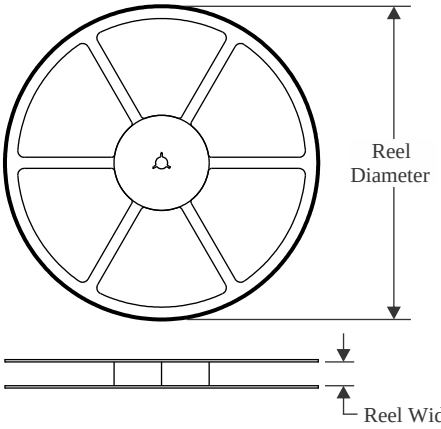
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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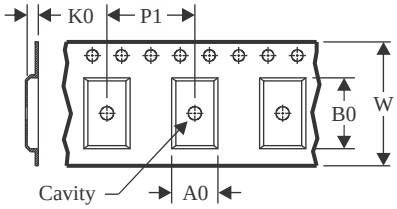
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## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

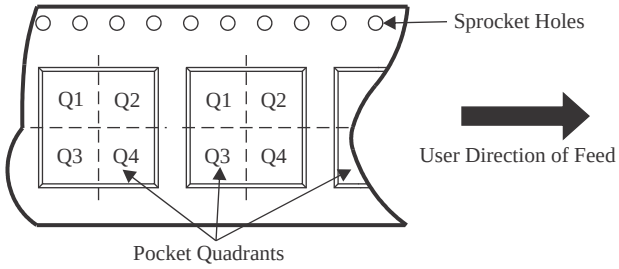



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

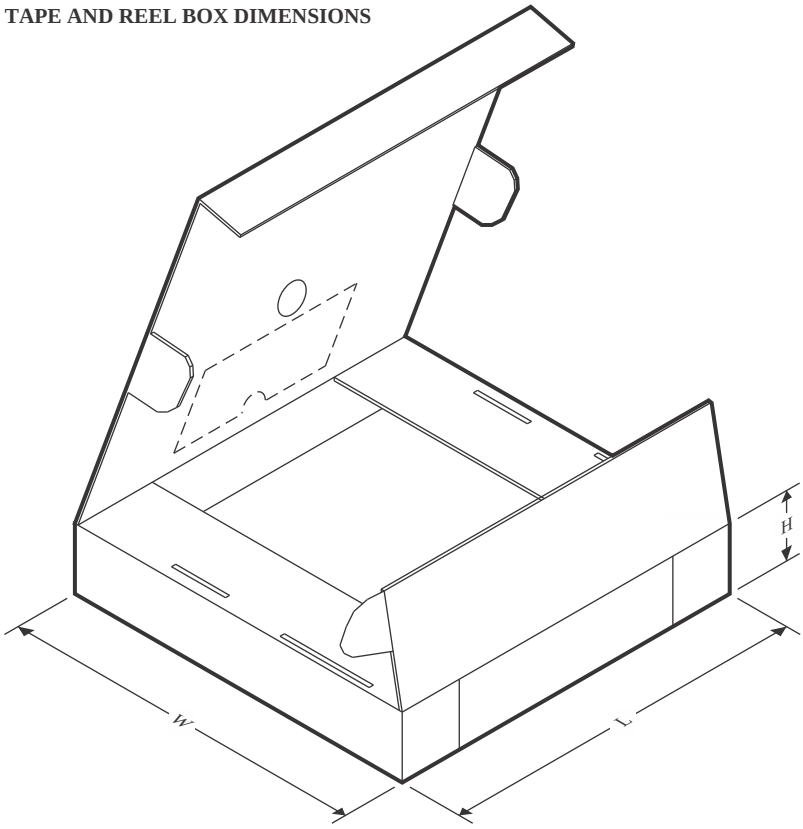
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TLV2376IDGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TLV2376IDGKT | VSSOP | DGK | 8 | 250 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TLV2376IDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLV376IDBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TLV376IDBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 8.4 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TLV376IDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLV4376IPWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

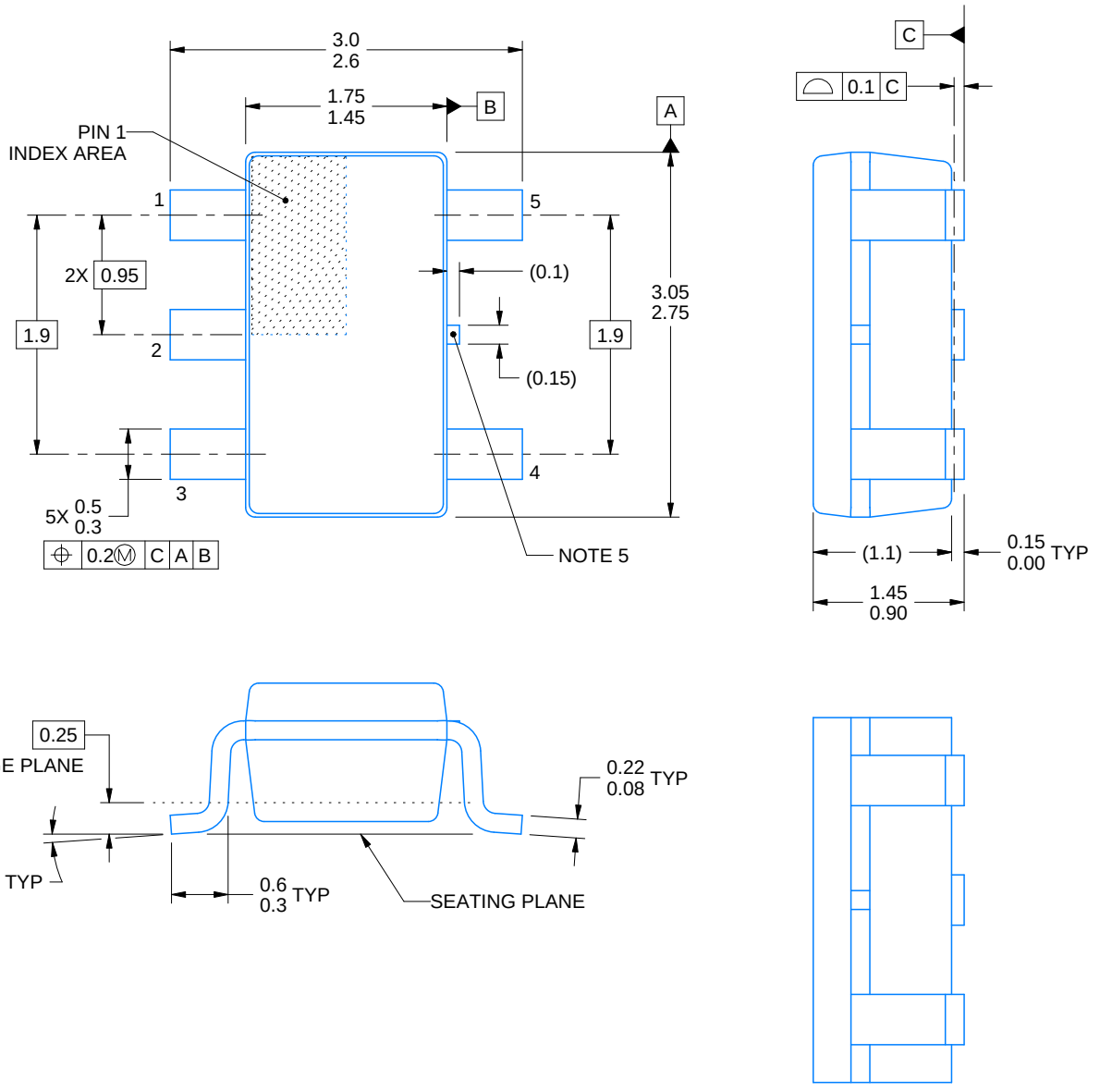
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TLV2376IDGKR | VSSOP | DGK | 8 | 2500 | 356.0 | 356.0 | 35.0 |
| TLV2376IDGKT | VSSOP | DGK | 8 | 250 | 356.0 | 356.0 | 35.0 |
| TLV2376IDR | SOIC | D | 8 | 2500 | 356.0 | 356.0 | 35.0 |
| TLV376IDBVR | SOT-23 | DBV | 5 | 3000 | 223.0 | 270.0 | 35.0 |
| TLV376IDBVT | SOT-23 | DBV | 5 | 250 | 223.0 | 270.0 | 35.0 |
| TLV376IDR | SOIC | D | 8 | 2500 | 356.0 | 356.0 | 35.0 |
| TLV4376IPWR | TSSOP | PW | 14 | 2000 | 356.0 | 356.0 | 35.0 |

# PACKAGE OUTLINE

## DBV0005A

## SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

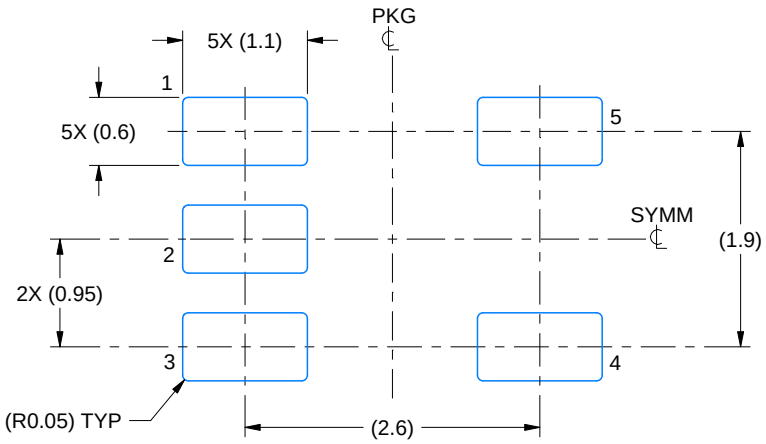



ALTERNATIVE PACKAGE SINGULATION VIEW

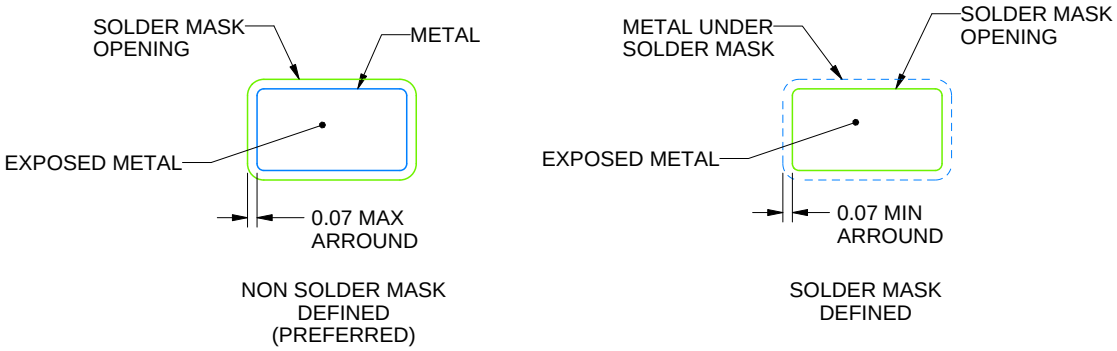
4214839/J 02/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

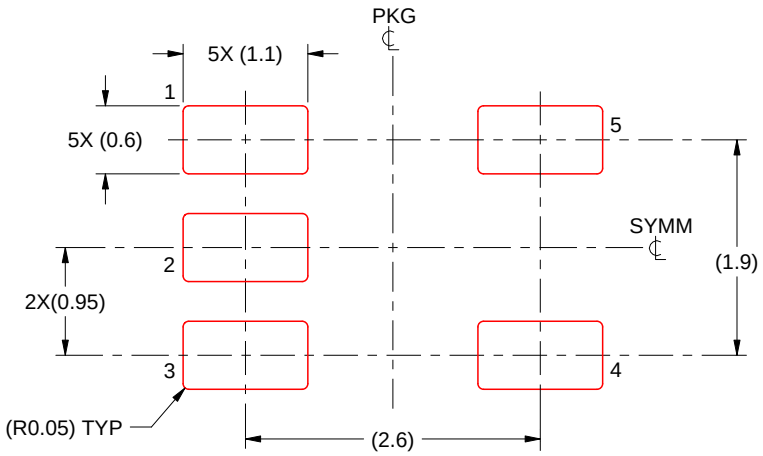



SOLDER MASK DETAILS

4214839/J 02/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



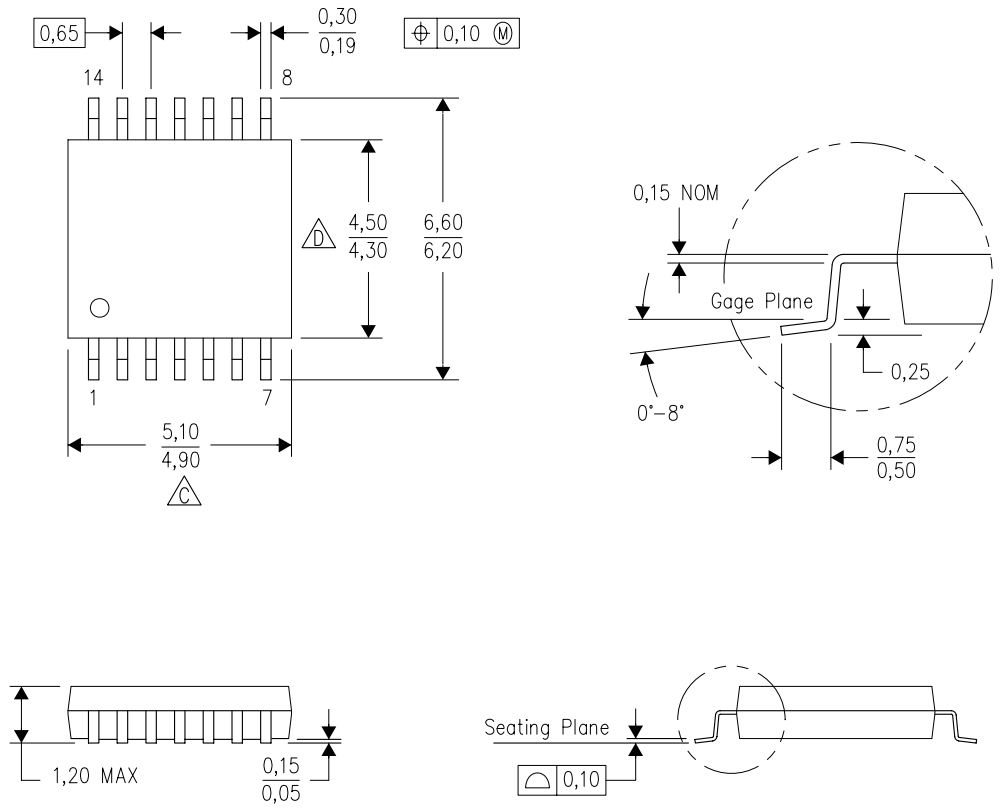

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/J 02/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

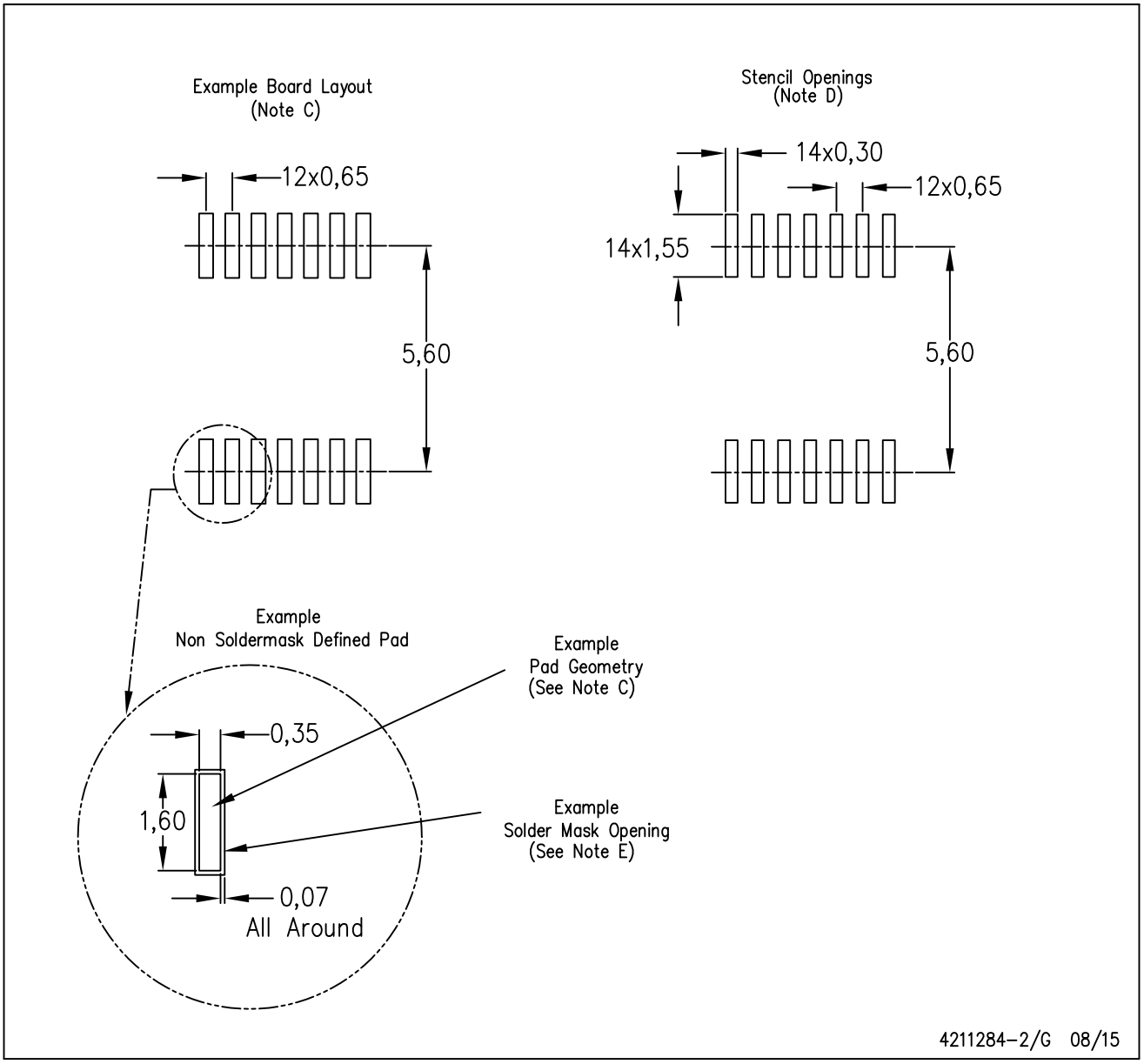
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



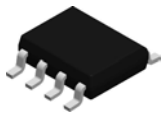

4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

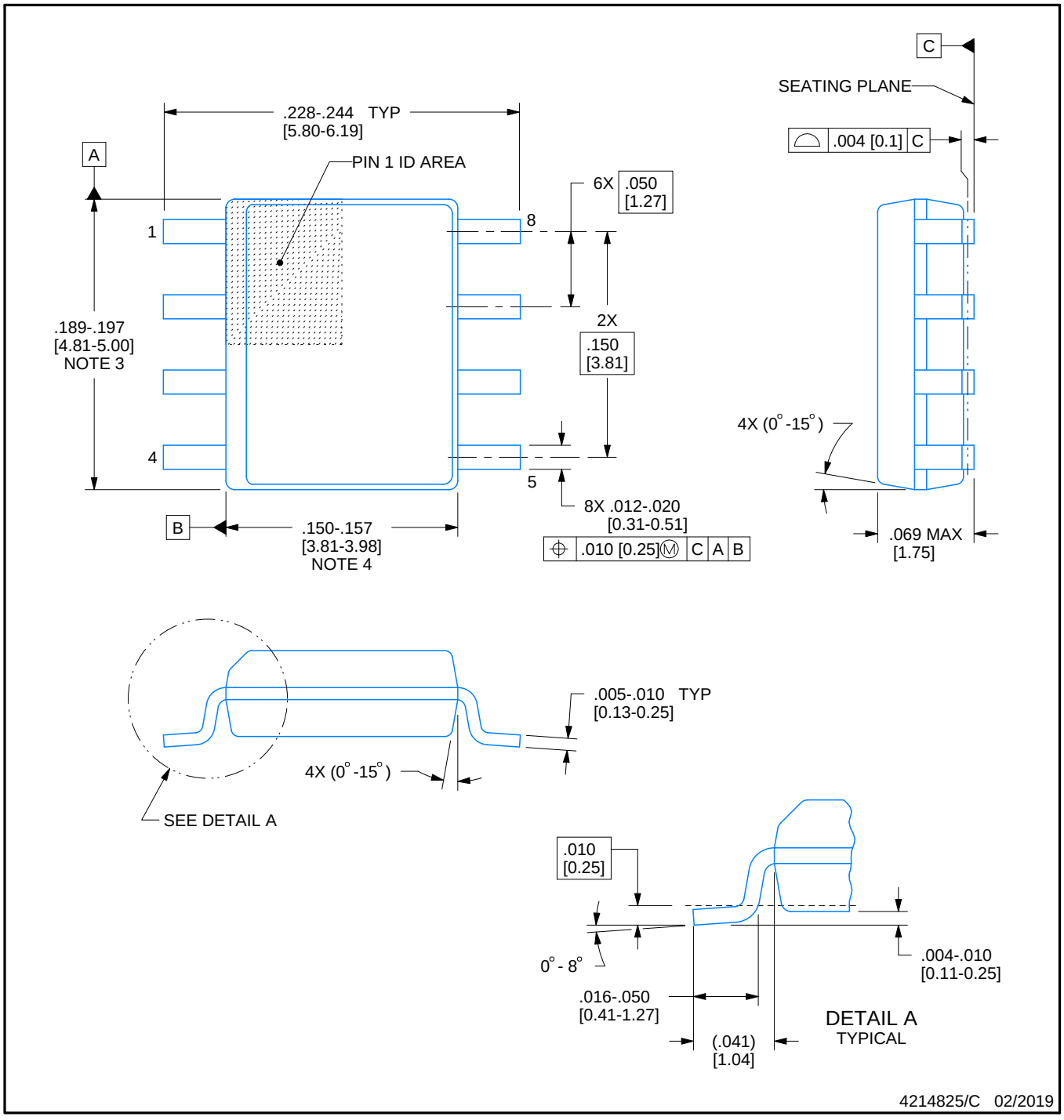


# PACKAGE OUTLINE

## D0008A

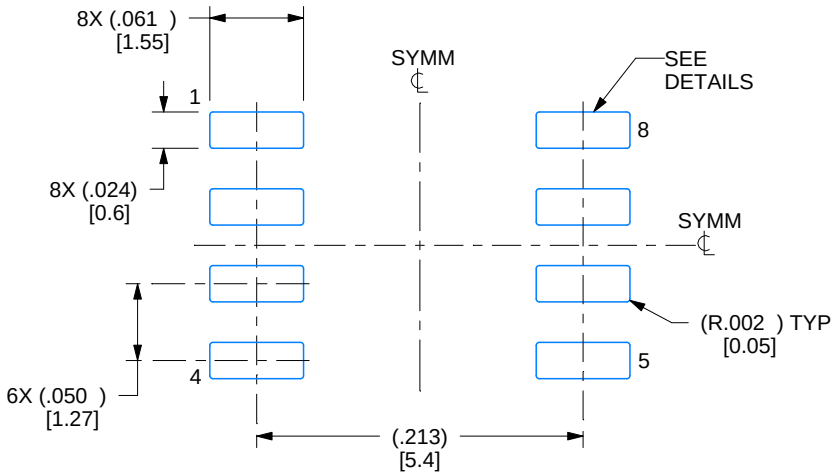
## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

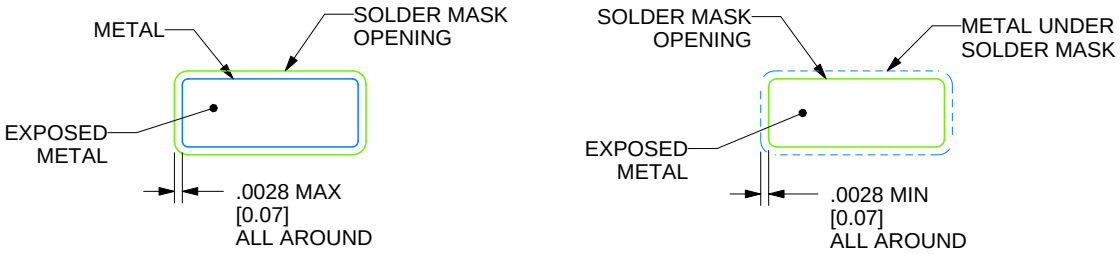



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X




SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

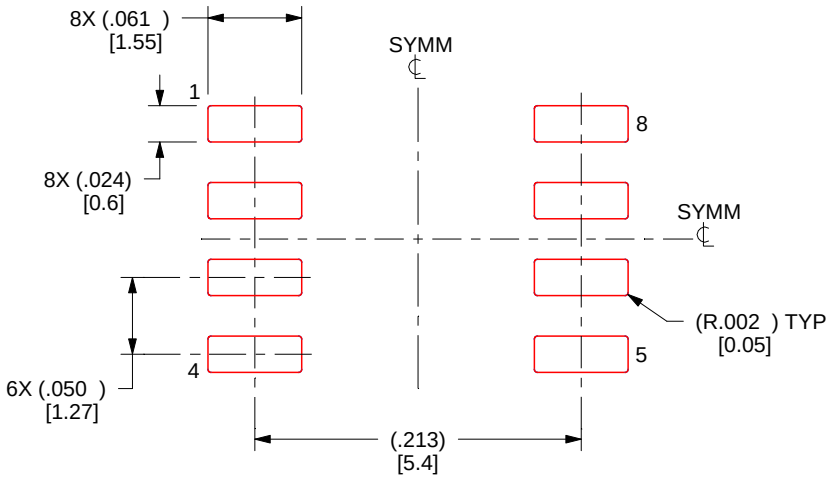
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## D0008A

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



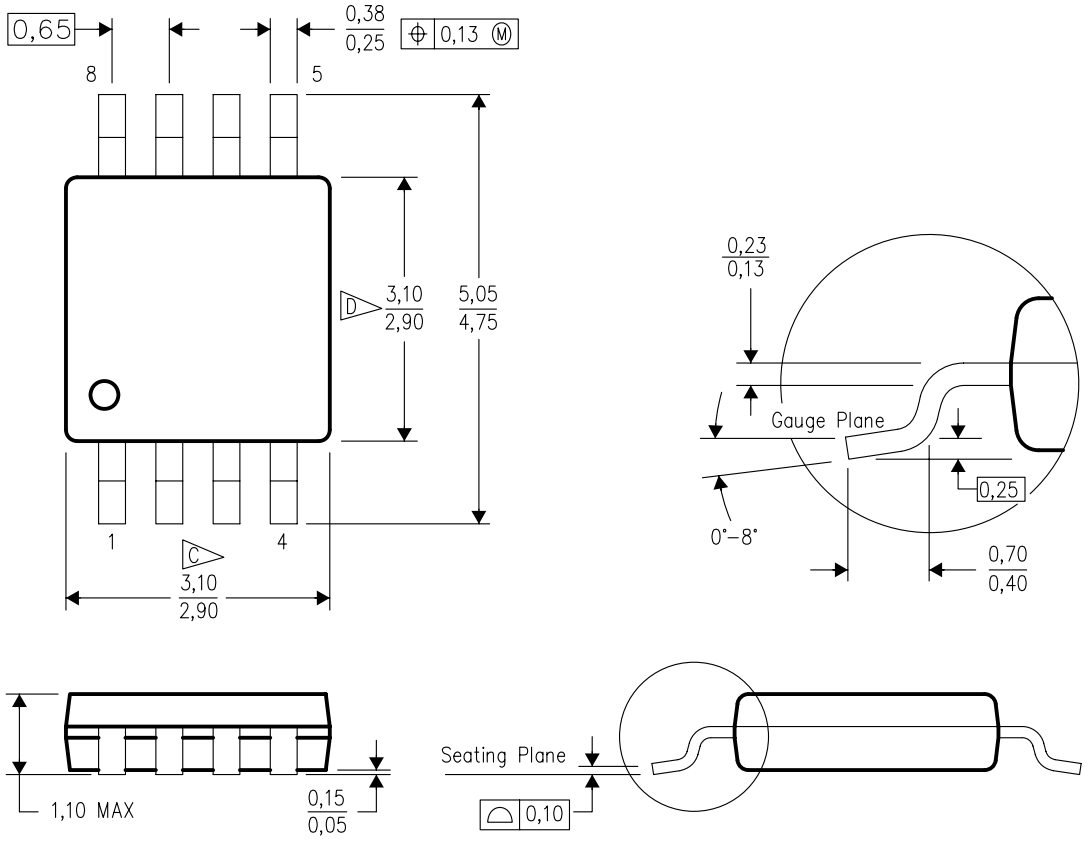

SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

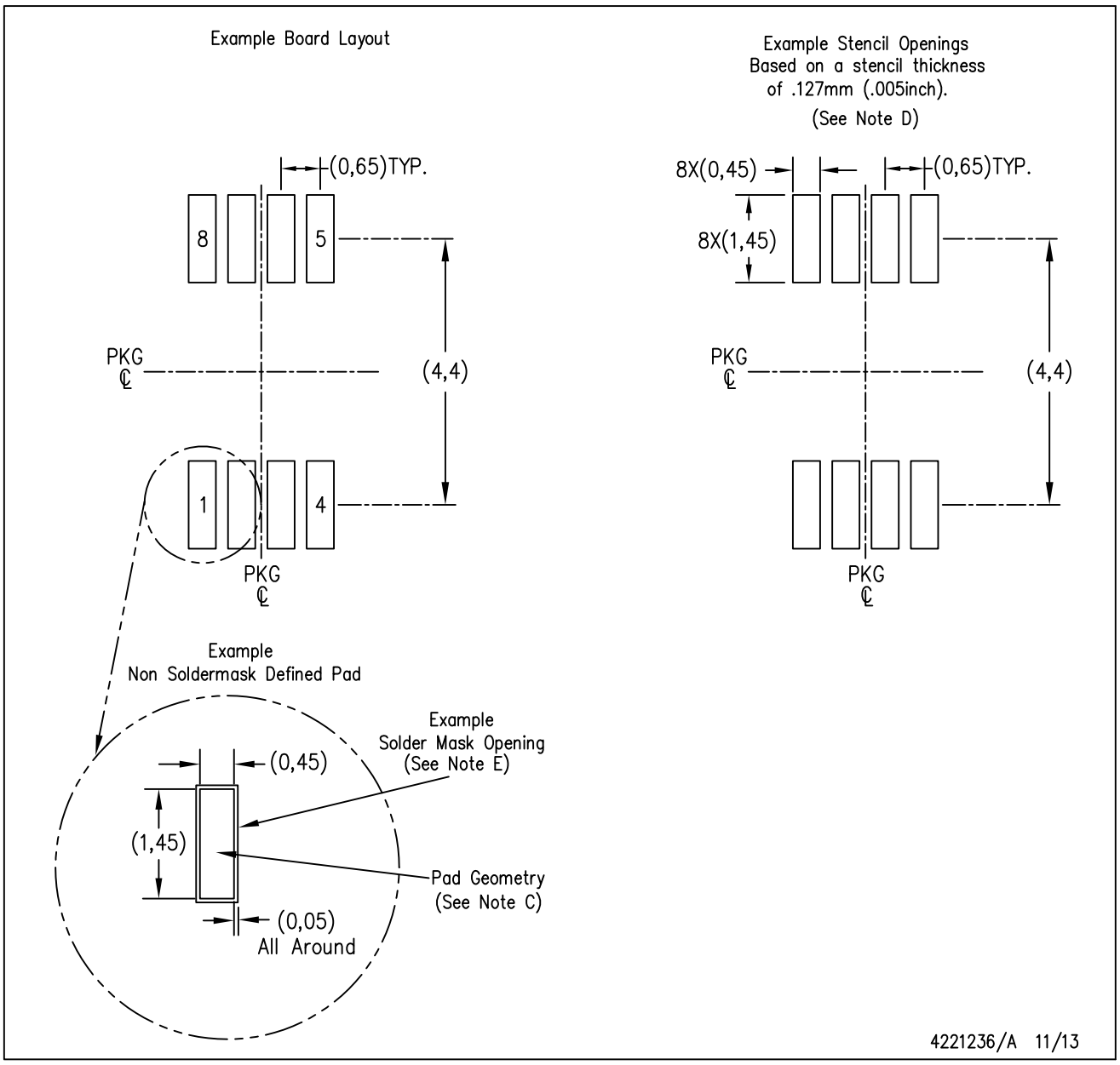
## DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE




4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

# DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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