TLV702 300-mA, Low-I_Q, Low-Dropout Regulator

1 Features

- Very Low Dropout:
  - 37 mV at I_{OUT} = 50 mA, V_{OUT} = 2.8 V
  - 75 mV at I_{OUT} = 100 mA, V_{OUT} = 2.8 V
  - 220mV at I_{OUT} = 300 mA, V_{OUT} = 2.8 V
- 2% Accuracy
- Low I_Q: 35 µA
- Fixed-Output Voltage Combinations Possible from 1.2 V to 4.8 V
- High PSRR: 68 dB at 1 kHz
- Stable With Effective Capacitance of 0.1 µF(1)
- Thermal Shutdown and Overcurrent Protection
- Packages: 5-Pin SOT-23 and 1.5-mm × 1.5-mm, 6-Pin WSON

(1) See the *Input and Output Capacitor Requirements* in *Application Information*.

2 Applications

- Wireless Handsets
- Smart Phones
- ZigBee® Networks
- *Bluetooth*® Devices
- Li-Ion Battery-Operated Handheld Products
- WLAN and Other PC Add-on Cards

3 Description

The TLV702 series of low-dropout (LDO) linear regulators are low quiescent current devices with excellent line and load transient performance. These LDOs are designed for power-sensitive applications. A precision bandgap and error amplifier provides overall 2% accuracy. Low output noise, very high power-supply rejection ratio (PSRR), and low-dropout voltage make this series of devices ideal for a wide selection of battery-operated handheld equipment. All device versions have thermal shutdown and current limit for safety.

Furthermore, these devices are stable with an effective output capacitance of only 0.1 µF. This feature enables the use of cost-effective capacitors that have higher bias voltages and temperature derating. The devices regulate to specified accuracy with no output load.

The TLV702P series also provides an active pulldown circuit to quickly discharge the outputs.

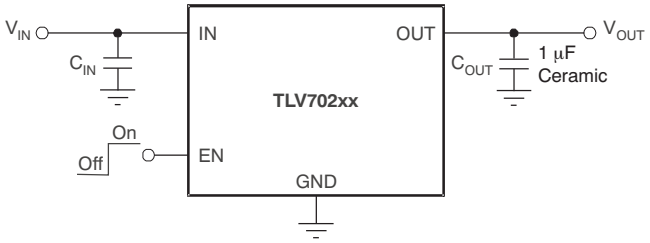
The TLV702 series of LDO linear regulators are available in SOT23-5 and 1.5-mm × 1.5-mm WSON-6 packages.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLV702	SOT-23 (5)	2.90 mm × 1.60 mm
	WSON (6)	1.50 mm × 1.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Circuit



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (March 2015) to Revision D — **Page**

- Changed OUT pin number from 5 to 3 in WSON column of Pin Functions table ... 3
- Added footnote to maximum EN voltage specification ... 4
- Added parameter names to *Recommended Operating Conditions* table ... 4

Changes from Revision B (February 2011) to Revision C — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Changed Pin Configuration and Functions section; updated table format ... 3
- Deleted *Ordering Information* table ... 3
- Changed "free-air temperature" to "junction temperature" in *Absolute Maximum Ratings* condition statement ... 4
- Changed *Thermal Information* table; updated thermal resistance values for all packages ... 4
- Deleted *Dissipation Ratings* table ... 4
- Changed V_{DO} dropout voltage test conditions; deleted I_{OUT} = 50 mA and I_{OUT} = 100 mA with V_{OUT} = 2.8 V test parameters ... 5
- Deleted *EVM Dissipation Ratings* table ... 16

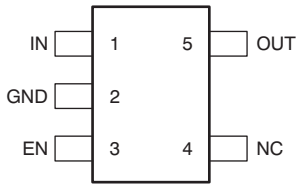
Changes from Revision A (October 2010) to Revision B — **Page**

- Added SON-6 (DSE) package and related references to data sheet ... 1

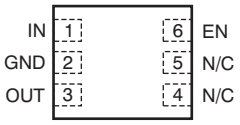
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5 Pin Configuration and Functions

DBV Package
5-Pin SOT-23
Top View



DSE Package
6-Pin WSON
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	SOT-23	WSON		
IN	1	1	I	Input pin. A small, 1-μF ceramic capacitor is recommended from this pin to ground to assure stability and good transient performance. See *Input and Output Capacitor Requirements* in *Application Information* for more details.
GND	2	2	—	Ground pin
EN	3	6	I	Enable pin. Driving EN over 0.9 V turns on the regulator. Driving EN below 0.4 V puts the regulator into shutdown mode and reduces operating current to 1 μA, nominal. For TLV702P, output voltage is discharged through an internal 120-Ω resistor when device is shut down.
NC	4	4, 5	—	No connection. This pin can be tied to ground to improve thermal dissipation.
OUT	5	3	O	Regulated output voltage pin. A small, 1-μF ceramic capacitor is needed from this pin to ground to assure stability. See *Input and Output Capacitor Requirements* in *Application Information* for more details.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage(2)	IN	–0.3	6	V
	EN	–0.3	6(3)	
	OUT	–0.3	6	
Current (source)	OUT	Internally limited		
Output short-circuit duration		Indefinite		
Total continuous power dissipation		See *Thermal Information*		
Temperature	Operating virtual junction, T_J	–55	150	°C
	Storage, T_{stg}	–55	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.
(2) All voltages are with respect to network ground terminal.
(3) The absolute maximum rating is V_{IN} + 0.3 V or 6.0 V, whichever is smaller.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted).

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	2		5.5	V
V_{OUT}	Output voltage	1.2		4.8	V
I_{OUT}	Output current	0		300	mA

6.4 Thermal Information

THERMAL METRIC(1)		TLV702		UNIT
		DBV (SOT-23)	DSE (WSON)	
		5 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	249.2	321.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	136.4	207.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	85.9	281.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	19.5	42.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	85.3	284.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	142.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 Electrical Characteristics

At V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2 V (whichever is greater); I_{OUT} = 10 mA, V_{EN} = 0.9 V, C_{OUT} = 1 µF, and T_J = –40°C to +125°C, unless otherwise noted. Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range		2		5.5	V
V_{OUT}	DC output accuracy	–40°C ≤ T_J ≤ 125°C	–2%	0.5%	2%	
$\Delta V_{OUT(\Delta VIN)}$	Line regulation	$V_{OUT(nom)}$ + 0.5 V ≤ V_{IN} ≤ 5.5 V, I_{OUT} = 10 mA		1	5	mV
$\Delta V_{OUT(\Delta IOUT)}$	Load regulation	0 mA ≤ I_{OUT} ≤ 300 mA		1	15	mV
V_{DO}	Dropout voltage(1)	V_{IN} = 0.98 × $V_{OUT(nom)}$, I_{OUT} = 300 mA		260	375	mV
I_{CL}	Output current limit	V_{OUT} = 0.9 × $V_{OUT(nom)}$	320	500	860	mA
I_{GND}	Ground pin current	I_{OUT} = 0 mA		35	55	µA
		I_{OUT} = 300 mA, V_{IN} = V_{OUT} + 0.5 V		370		µA
I_{SHDN}	Ground pin current (shutdown)	V_{EN} ≤ 0.4 V, V_{IN} = 2 V		400		nA
		V_{EN} ≤ 0.4 V, 2 V ≤ V_{IN} ≤ 4.5 V, T_J = –40°C to +85°C		1	2	µA
PSRR	Power-supply rejection ratio	V_{IN} = 2.3 V, V_{OUT} = 1.8 V, I_{OUT} = 10 mA, f = 1 kHz		68		dB
V_n	Output noise voltage	BW = 100 Hz to 100 kHz, V_{IN} = 2.3 V, V_{OUT} = 1.8 V, I_{OUT} = 10 mA		48		μV_{RMS}
t_{STR}	Start-up time(2)	C_{OUT} = 1 µF, I_{OUT} = 300 mA		100		µs
$V_{EN(high)}$	Enable pin high (enabled)		0.9		V_{IN}	V
$V_{EN(low)}$	Enable pin low (disabled)		0		0.4	V
I_{EN}	Enable pin current	V_{IN} = V_{EN} = 5.5 V		0.04		µA
UVLO	Undervoltage lockout	V_{IN} rising		1.9		V
$R_{DISCHARGE}$	Active pulldown resistance (TLV702P only)	V_{EN} = 0 V		120		Ω
T_{sd}	Thermal shutdown temperature	Shutdown, temperature increasing		165		°C
		Reset, temperature decreasing		145		°C
T_J	Operating junction temperature		–40		125	°C

(1) V_{DO} is measured for devices with $V_{OUT(nom)}$ ≥ 2.35 V.
(2) Start-up time = time from EN assertion to 0.98 × $V_{OUT(nom)}$.

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6.6 Typical Characteristics

Over operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2 V, whichever is greater; I_{OUT} = 10 mA, V_{EN} = V_{IN}, C_{OUT} = 1 µF, unless otherwise noted. Typical values are at T_J = 25°C.

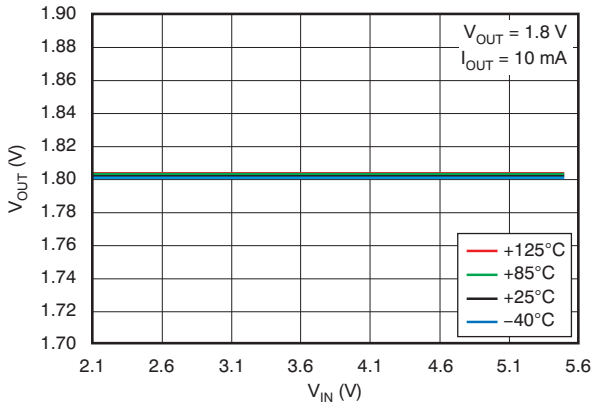


Figure 1. Line Regulation

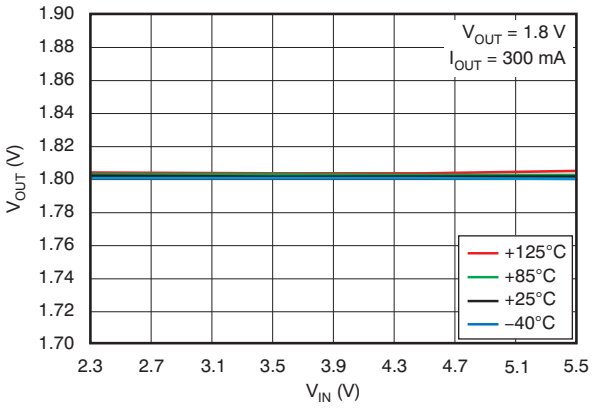


Figure 2. Line Regulation

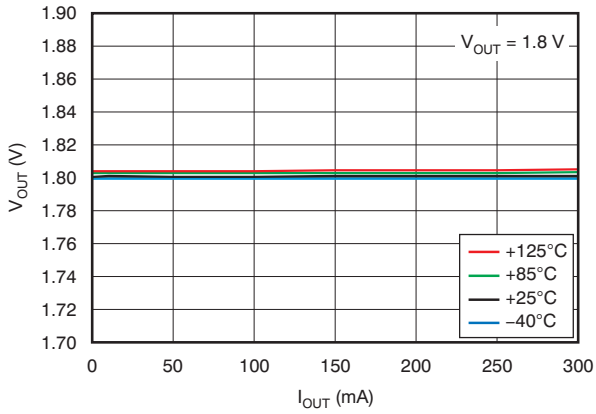


Figure 3. Load Regulation

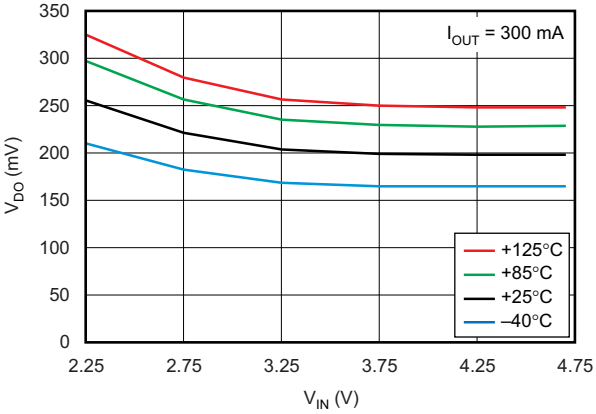


Figure 4. Dropout Voltage vs Input Voltage

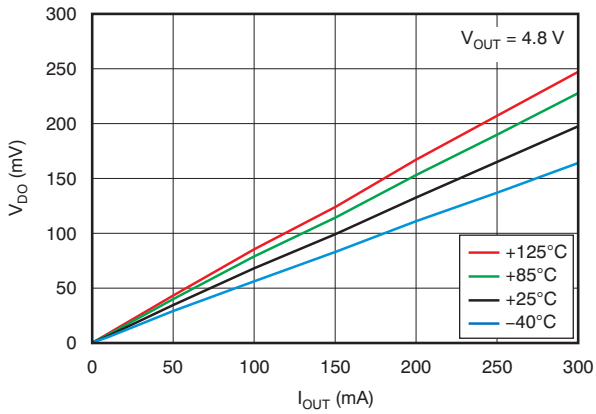


Figure 5. Dropout Voltage vs Output Current

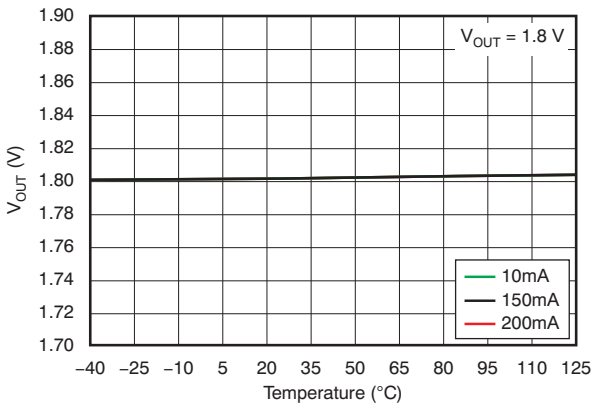


Figure 6. Output Voltage vs Temperature

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Typical Characteristics (continued)

Over operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2 V, whichever is greater; I_{OUT} = 10 mA, V_{EN} = V_{IN}, C_{OUT} = 1 µF, unless otherwise noted. Typical values are at T_J = 25°C.

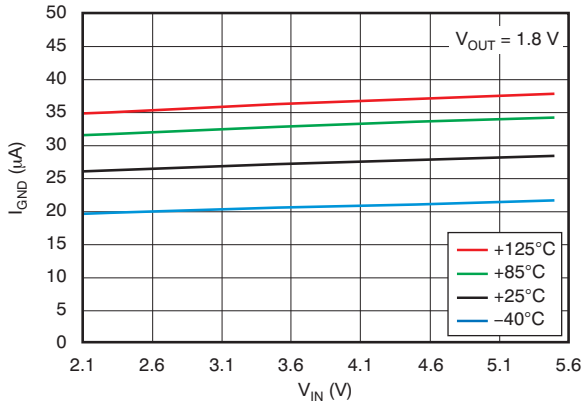


Figure 7. Ground Pin Current vs Input Voltage

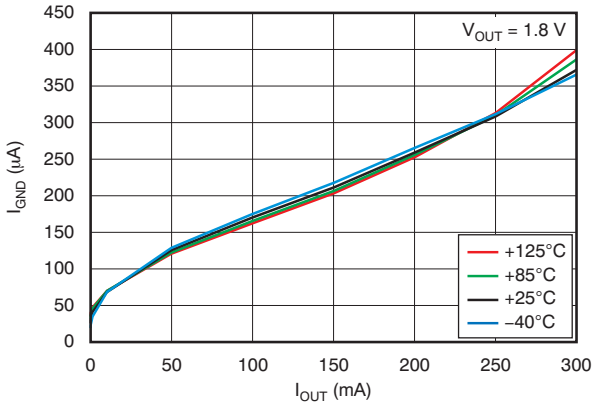


Figure 8. Ground Pin Current vs Load

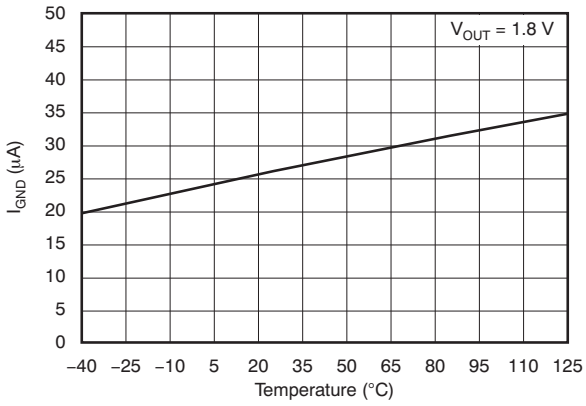


Figure 9. Ground Pin Current vs Temperature

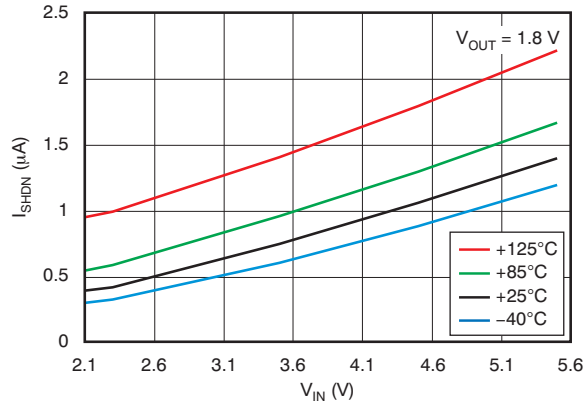


Figure 10. Shutdown Current vs Input Voltage

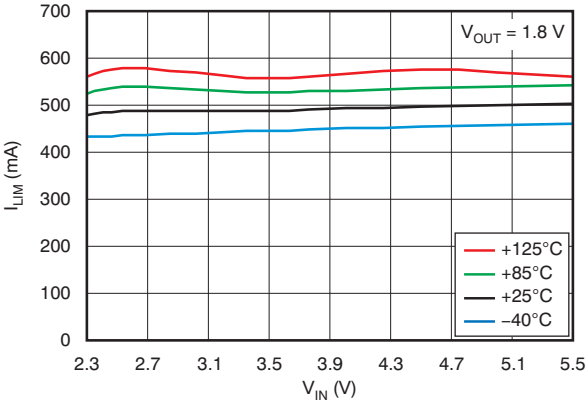


Figure 11. Current Limit vs Input Voltage

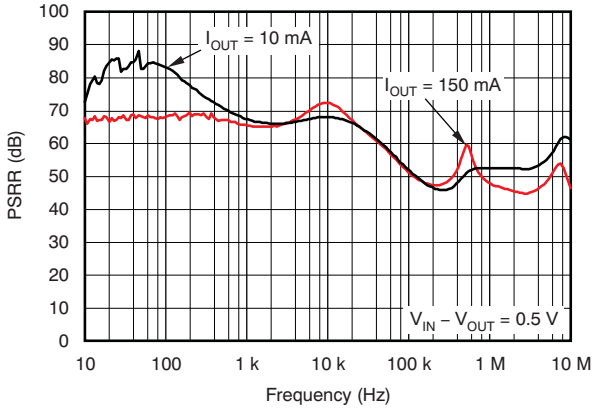


Figure 12. Power-Supply Ripple Rejection vs Frequency

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Typical Characteristics (continued)

Over operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2 V, whichever is greater; I_{OUT} = 10 mA, V_{EN} = V_{IN}, C_{OUT} = 1 µF, unless otherwise noted. Typical values are at T_J = 25°C.

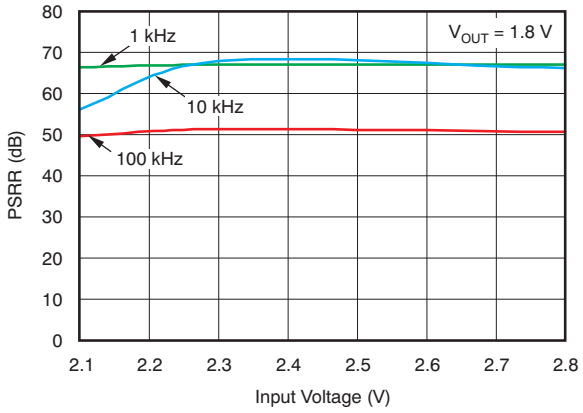


Figure 13. Power-Supply Ripple Rejection vs Input Voltage

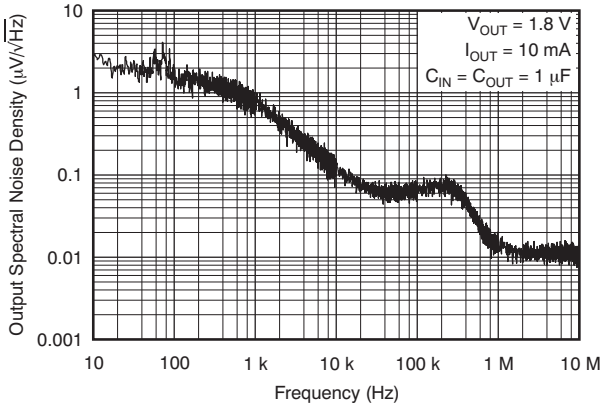


Figure 14. Output Spectral Noise Density vs Frequency

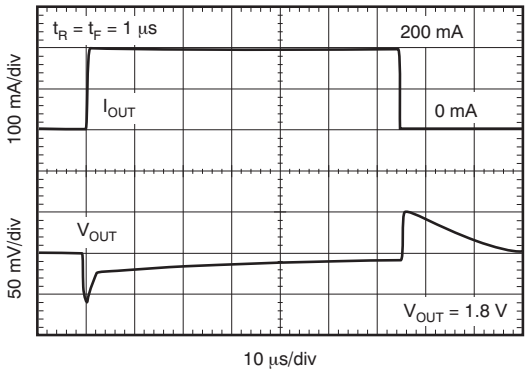


Figure 15. Load Transient Response

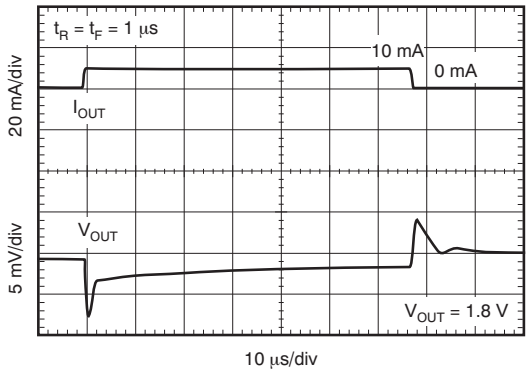


Figure 16. Load Transient Response

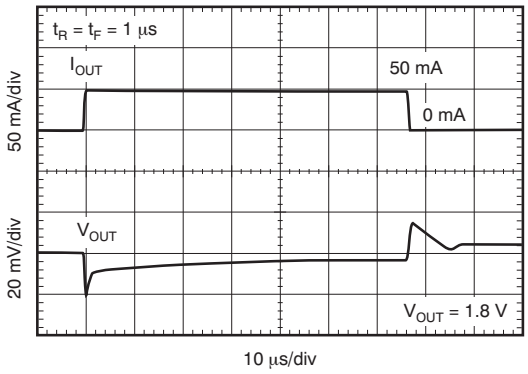


Figure 17. Load Transient Response

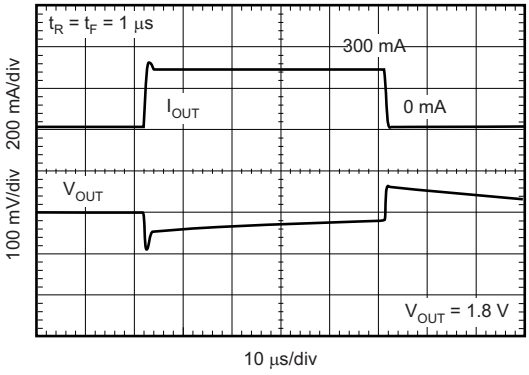


Figure 18. Load Transient Response

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Typical Characteristics (continued)

Over operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2 V, whichever is greater; I_{OUT} = 10 mA, V_{EN} = V_{IN}, C_{OUT} = 1 µF, unless otherwise noted. Typical values are at T_J = 25°C.

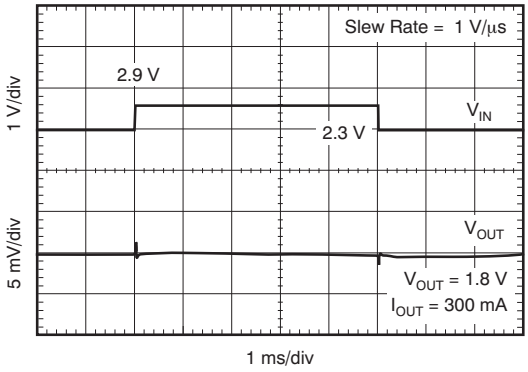


Figure 19. Line Transient Response

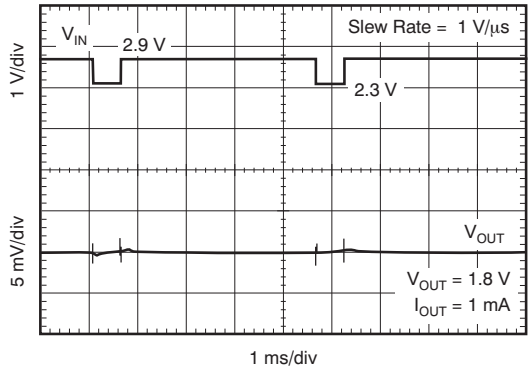


Figure 20. Line Transient Response

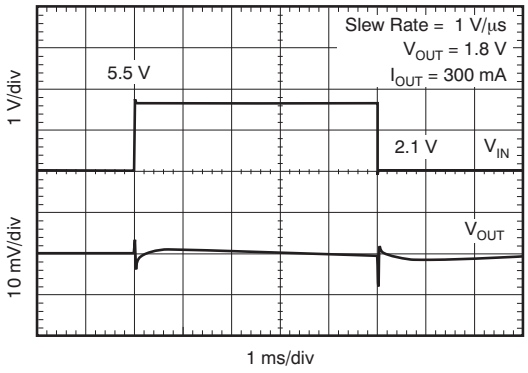


Figure 21. Line Transient Response

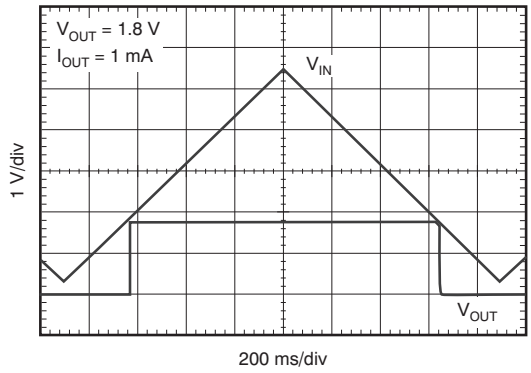


Figure 22. V_{IN} Ramp Up, Ramp Down Response

7 Detailed Description

7.1 Overview

The TLV702 series of low-dropout (LDO) linear regulators are low quiescent current devices with excellent line and load transient performance. These LDOs are designed for power-sensitive applications. A precision bandgap and error amplifier provides overall 2% accuracy. Low output noise, very high power-supply rejection ratio (PSRR), and low dropout voltage make this series of devices ideal for most battery-operated handheld equipment. All device versions have integrated thermal shutdown, current limit, and undervoltage lockout (UVLO).

7.2 Functional Block Diagrams

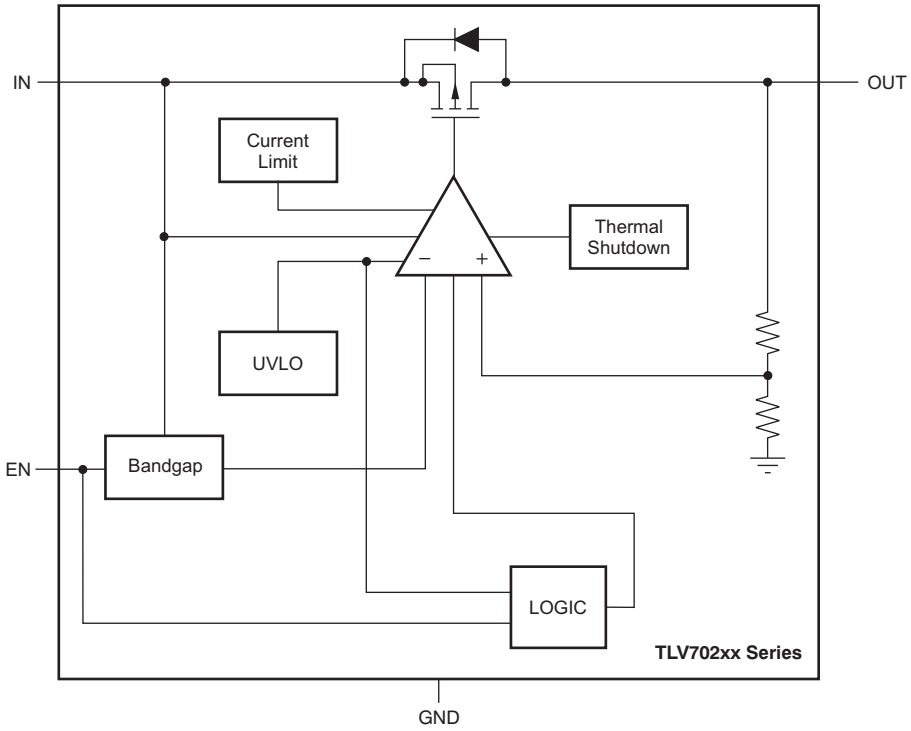


Figure 23. TLV702 Block Diagram

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Functional Block Diagrams (continued)

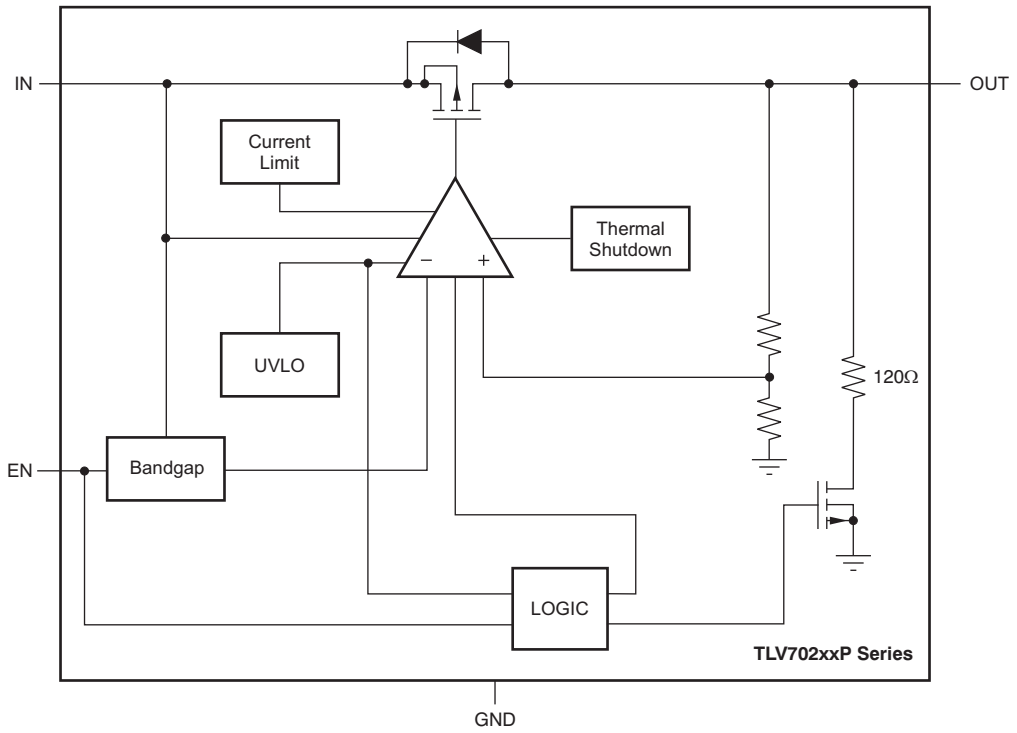


Figure 24. TLV702P Block Diagram

7.3 Feature Description

7.3.1 Internal Current Limit

The TLV702 internal current limit helps to protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of the output voltage. In such a case, the output voltage is not regulated, and is $V_{OUT} = I_{CL} \times R_{LOAD}$. The PMOS pass transistor dissipates $(V_{IN} – V_{OUT}) \times I_{CL}$ until thermal shutdown is triggered and the device turns off. As the device cools, it is turned on by the internal thermal shutdown circuit. If the fault condition continues, the device cycles between current limit and thermal shutdown. See *Thermal Consideration* for more details.

The PMOS pass element in the TLV702 has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting to 5% of the rated output current is recommended.

7.3.2 Shutdown

The enable pin (EN) is active high. The device is enabled when voltage at EN pin goes above 0.9 V. The device is turned off when the EN pin is held at less than 0.4 V. When shutdown capability is not required, EN can be connected to the IN pin.

The TLV702P version has internal active pulldown circuitry that discharges the output with a time constant of:

$$\tau = \frac{(120 \bullet R_L)}{(120 + R_L)} \bullet C_{OUT} \quad (1)$$

where:

- R_L = Load resistance
- C_{OUT} = Output capacitor

Feature Description (continued)

7.3.3 Dropout Voltage

The TLV702 uses a PMOS pass transistor to achieve low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the PMOS pass device is in the linear (triode) region of operation and the input-to-output resistance is the $R_{DS(on)}$ of the PMOS pass element. V_{DO} scales approximately with output current because the PMOS device behaves as a resistor in dropout.

As with any linear regulator, PSRR and transient response are degraded as (V_{IN} – V_{OUT}) approaches dropout. This effect is shown in Figure 13.

7.3.4 Undervoltage Lockout

The TLV702 uses a UVLO circuit to keep the output shut off until internal circuitry is operating properly.

7.4 Device Functional Modes

7.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage is greater than the nominal output voltage added to the dropout voltage.
- The output current is less than the current limit.
- The input voltage is greater than the UVLO voltage.

7.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this condition, the output voltage is the same as the input voltage minus the dropout voltage. The transient performance of the device is significantly degraded because the pass device is in a triode state and no longer regulates the output voltage of the LDO. Line or load transients in dropout may result in large output voltage deviations.

Table 1 lists the conditions that lead to the different modes of operation.

Table 1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER	
	V_{IN}	I_{OUT}
Normal mode	$V_{IN} > V_{OUT\ (nom)} + V_{DO}$	$I_{OUT} < I_{CL}$
Dropout mode	$V_{IN} < V_{OUT\ (nom)} + V_{DO}$	$I_{OUT} < I_{CL}$
Current limit	$V_{IN} >$ UVLO	$I_{OUT} > I_{CL}$

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TLV702 belongs to a new family of next-generation value LDO regulators. These devices consume low quiescent current and deliver excellent line and load transient performance. These characteristics, combined with low noise and very good PSRR with little (V_{IN} – V_{OUT}) headroom, make this family of devices ideal for portable RF applications. This family of regulators offers current limit and thermal protection, and is specified from –40°C to +125°C.

8.2 Typical Application

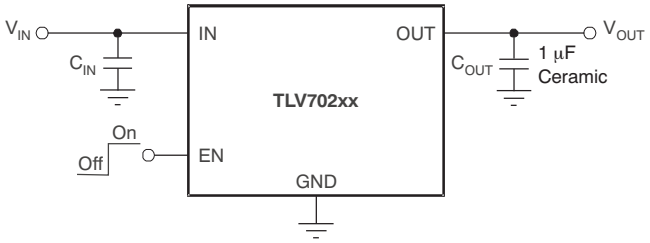


Figure 25. Typical Application Circuit

8.2.1 Design Requirements

Table 2 lists the design parameters.

Table 2. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Input voltage	2.5 V to 3.3 V
Output voltage	1.8 V
Output current	100 mA

8.2.2 Detailed Design Procedure

8.2.2.1 Input and Output Capacitor Requirements

1-µF X5R- and X7R-type ceramic capacitors are recommended because these capacitors have minimal variation in value and equivalent series resistance (ESR) overtemperature.

However, the TLV702 is designed to be stable with an *effective capacitance* of 0.1 µF or larger at the output. Thus, the device is stable with capacitors of other dielectric types as well, as long as the effective capacitance under operating bias voltage and temperature is greater than 0.1 µF. This effective capacitance refers to the capacitance that the LDO sees under operating bias voltage and temperature conditions; that is, the capacitance after taking both bias voltage and temperature derating into consideration. In addition to allowing the use of lower-cost dielectrics, this capability of being stable with 0.1-µF effective capacitance also enables the use of smaller footprint capacitors that have higher derating in size- and space-constrained applications.

Using a 0.1-µF rated capacitor at the output of the LDO does not ensure stability because the effective capacitance under the specified operating conditions must not be less than 0.1 µF. Maximum ESR should be less than 200 mΩ.

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Although an input capacitor is not required for stability, it is good analog design practice to connect a 0.1-μF to 1-μF, low ESR capacitor across the IN pin and GND pin of the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated, or if the device is not located close to the power source. If source impedance is more than 2 Ω, a 0.1-μF input capacitor may be necessary to ensure stability.

8.2.2.2 Transient Response

As with any regulator, increasing the size of the output capacitor reduces overshoot and undershoot magnitude but increases the duration of the transient response.

8.2.3 Application Curves

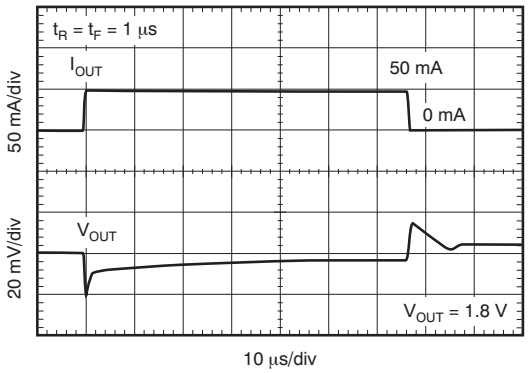


Figure 26. Load Transient Response

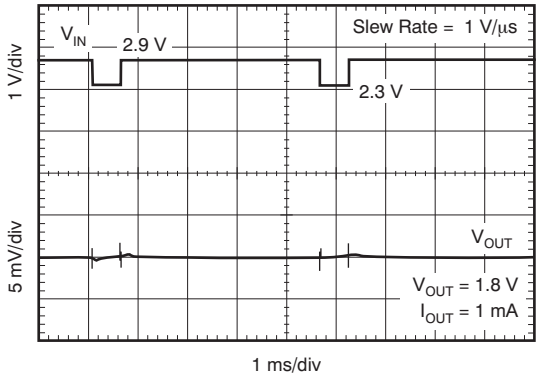


Figure 27. Line Transient Response

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9 Power Supply Recommendations

Connect a low output impedance power supply directly to the INPUT pin of the TLV702. Inductive impedances between the input supply and the INPUT pin can create significant voltage excursions at the INPUT pin during start-up or load transient events.

9.1 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the printed-circuit-board (PCB) layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air.

Refer to *Thermal Information* for thermal performance on the TLV702 evaluation module (EVM). The EVM is a two-layer board with two ounces of copper per side.

Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) is equal to the product of the output current and the voltage drop across the output pass element, as shown in Equation 2.

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (2)$$

10 Layout

10.1 Layout Guidelines

Input and output capacitors should be placed as close to the device pins as possible. To improve AC performance such as PSRR, output noise, and transient response, TI recommends designing the board with separate ground planes for V_{IN} and V_{OUT}, with the ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor should be connected directly to the GND pin of the device. High ESR capacitors may degrade PSRR performance.

10.1.1 Thermal Consideration

Thermal protection disables the output when the junction temperature rises to approximately 165°C, allowing the device to cool. When the junction temperature cools to approximately 145°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to 125°C maximum.

To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions.

The internal protection circuitry of the TLV702 has been designed to protect against overload conditions. It was not intended to replace proper heatsinking. Continuously running the TLV702 into thermal shutdown degrades device reliability.

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Layout Guidelines (continued)

10.1.2 Package Mounting

Solder pad footprint recommendations for the TLV702 are available from the TI website at www.ti.com. The recommended land pattern for the DBV and DSE packages are shown in Figure 28 and Figure 29, respectively.

10.2 Layout Examples

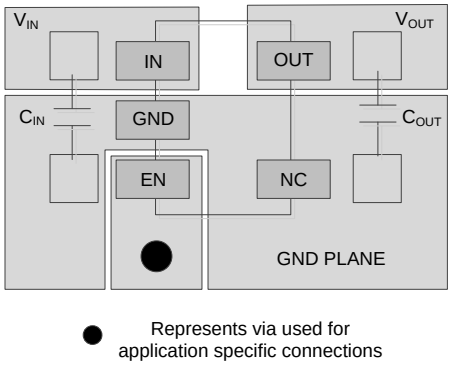


Figure 28. Layout Example for the DBV Package

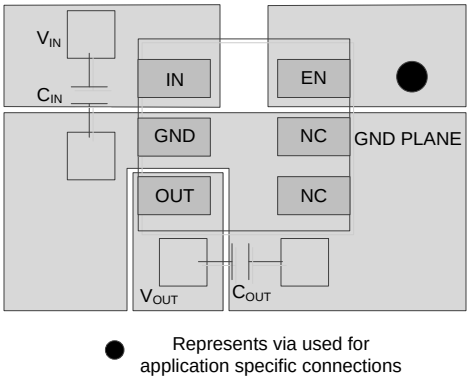


Figure 29. Layout Example for the DSE Package

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11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TLV702 is available through the product folders under *Tools & Software*.

11.1.2 Device Nomenclature

Table 3. Ordering Information(1)

PRODUCT	V_{OUT} (2)
TLV702**xx** ***yyyz***	**XX** is nominal output voltage (for example, 28 = 2.8 V). **YYY** is the package designator. **Z** is tape and reel quantity (R = 3000, T = 250).

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.
(2) Output voltages from 1.2 V to 4.8 V in 50-mV increments are available. Contact factory for details and availability.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

Texas Instruments, *Using the TLV700xxEVM-503* user's guide

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

E2E is a trademark of Texas Instruments.
Bluetooth is a registered trademark of Bluetooth SIG.
ZigBee is a registered trademark of the ZigBee Alliance.
All other trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV70212DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	QVN	Samples
TLV70212DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	QVN	Samples
TLV70213DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	12UW	Samples
TLV70213DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	12UW	Samples
TLV70215DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SIR	Samples
TLV70215DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SIR	Samples
TLV70215PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SLG	Samples
TLV70215PDBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SLG	Samples
TLV70218DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	QUW	Samples
TLV70218DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	QUW	Samples
TLV70220PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	QXL	Samples
TLV70220PDBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	QXL	Samples
TLV70225DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	QVF	Samples
TLV70225DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	QVF	Samples
TLV70225DSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	SY	Samples
TLV70225DSET	ACTIVE	WSON	DSE	6	250	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	SY	Samples
TLV70228DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	QUX	Samples
TLV70228DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	QUX	Samples
TLV70228DSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	VY	Samples
TLV70228DSET	ACTIVE	WSON	DSE	6	250	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	VY	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV70228PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	QVA	Samples
TLV70228PDBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	QVA	Samples
TLV70229DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SJW	Samples
TLV70229DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SJW	Samples
TLV70229DSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	SZ	Samples
TLV70229DSET	ACTIVE	WSON	DSE	6	250	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	SZ	Samples
TLV70230DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	QUY	Samples
TLV70230DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	QUY	Samples
TLV70231DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	QUZ	Samples
TLV70231DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	QUZ	Samples
TLV70233DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	QVD	Samples
TLV70233DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	QVD	Samples
TLV70233DSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	WK	Samples
TLV70233DSET	ACTIVE	WSON	DSE	6	250	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	WK	Samples
TLV70233PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SLH	Samples
TLV70233PDBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SLH	Samples
TLV70235DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SDT	Samples
TLV70235DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SDT	Samples
TLV70236DSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	VZ	Samples
TLV70236DSET	ACTIVE	WSON	DSE	6	250	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	VZ	Samples
TLV70237DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	QXR	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV70237DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	QXR	Samples
TLV70237DSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	D8	Samples
TLV70237DSET	ACTIVE	WSON	DSE	6	250	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	D8	Samples
TLV70242PDSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	B9	Samples
TLV70242PDSET	ACTIVE	WSON	DSE	6	250	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	B9	Samples
TLV70243DSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	5Q	Samples
TLV70243DSET	ACTIVE	WSON	DSE	6	250	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	5Q	Samples
TLV70245DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SCK	Samples
TLV70245DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SCK	Samples
TLV702475DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	QWJ	Samples
TLV702475DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	QWJ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLV702 :

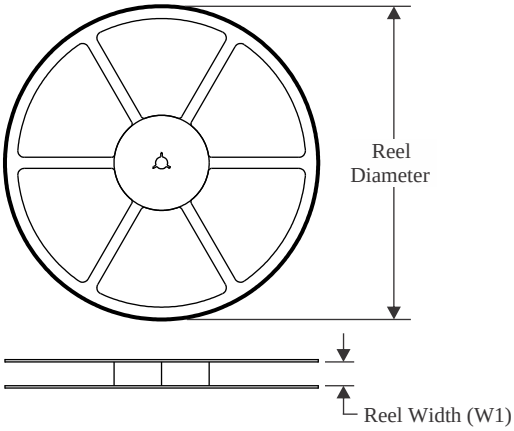
- Automotive : TLV702-Q1

NOTE: Qualified Version Definitions:

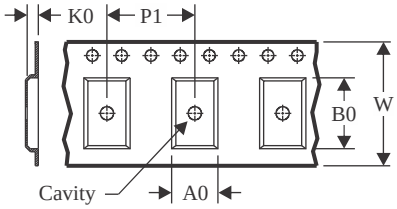
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

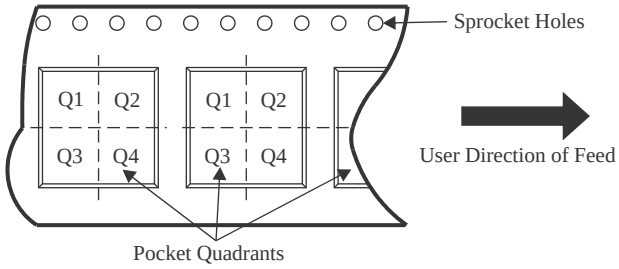


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



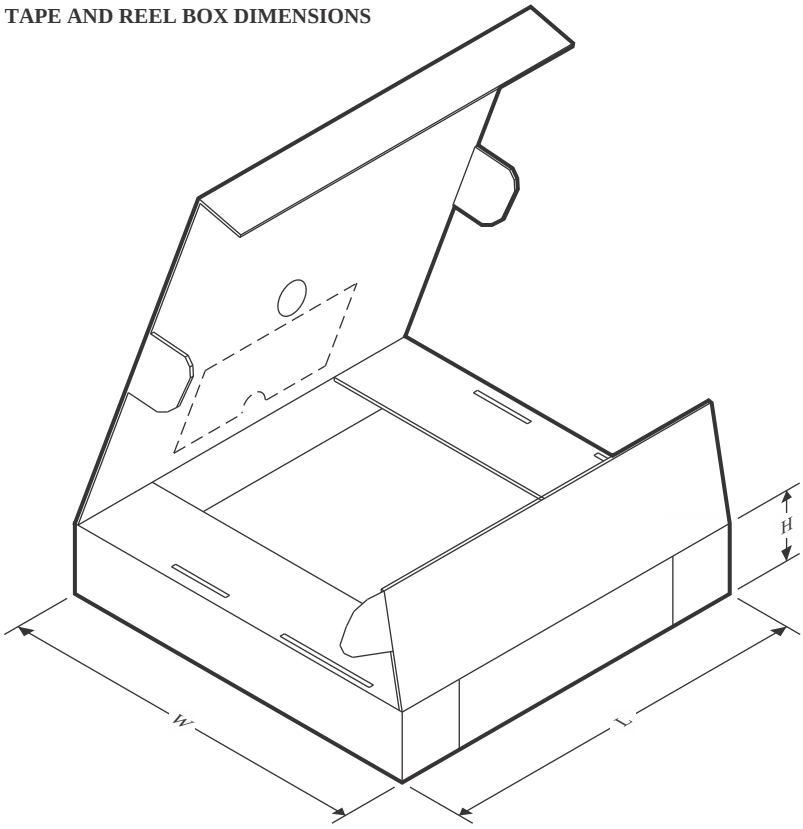
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV70212DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV70212DBVT	SOT-23	DBV	5	250	178.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV70212DBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV70213DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV70213DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV70213DBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV70213DBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV70215DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV70215DBVT	SOT-23	DBV	5	250	178.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV70215DBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV70215PDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV70215PDBVT	SOT-23	DBV	5	250	178.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV70218DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV70218DBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV70218DBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV70220PDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV70220PDBVT	SOT-23	DBV	5	250	178.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV70225DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV70225DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV70225DBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV70225DBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV70225DSER	WSON	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV70225DSET	WSON	DSE	6	250	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV70228DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV70228DBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV70228DSER	WSON	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV70228DSET	WSON	DSE	6	250	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV70228PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV70228PDBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV70229DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV70229DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV70229DBVT	SOT-23	DBV	5	250	178.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV70229DBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV70229DSER	WSON	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TLV70229DSET	WSON	DSE	6	250	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TLV70230DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV70230DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV70230DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV70230DBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV70230DBVT	SOT-23	DBV	5	250	178.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV70231DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV70231DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV70231DBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV70231DBVT	SOT-23	DBV	5	250	178.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV70233DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV70233DBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV70233DSER	WSON	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV70233DSET	WSON	DSE	6	250	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV70233PDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV70233PDBVT	SOT-23	DBV	5	250	178.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV70235DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV70235DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV70235DBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV70235DBVT	SOT-23	DBV	5	250	178.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV70236DSER	WSON	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV70236DSET	WSON	DSE	6	250	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV70237DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV70237DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV70237DBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV70237DBVT	SOT-23	DBV	5	250	178.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV70237DSER	WSON	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TLV70237DSET	WSON	DSE	6	250	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TLV70242PDSER	WSON	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TLV70242PDSET	WSON	DSE	6	250	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TLV70243DSER	WSON	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TLV70243DSET	WSON	DSE	6	250	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TLV70245DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV70245DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV70245DBVT	SOT-23	DBV	5	250	178.0	8.4	3.3	3.2	1.4	4.0	8.0	Q3
TLV70245DBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV702475DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV702475DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV702475DBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV702475DBVT	SOT-23	DBV	5	250	178.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV70212DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV70212DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV70212DBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
TLV70213DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV70213DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV70213DBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
TLV70213DBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
TLV70215DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV70215DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV70215DBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
TLV70215PDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV70215PDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV70218DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV70218DBVT	SOT-23	DBV	5	250	183.0	183.0	20.0
TLV70218DBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
TLV70220PDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV70220PDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV70225DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV70225DBVR	SOT-23	DBV	5	3000	183.0	183.0	20.0
TLV70225DBVT	SOT-23	DBV	5	250	183.0	183.0	20.0
TLV70225DBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
TLV70225DSER	WSON	DSE	6	3000	200.0	183.0	25.0
TLV70225DSET	WSON	DSE	6	250	200.0	183.0	25.0
TLV70228DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV70228DBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
TLV70228DSER	WSON	DSE	6	3000	200.0	183.0	25.0
TLV70228DSET	WSON	DSE	6	250	200.0	183.0	25.0
TLV70228PDBVR	SOT-23	DBV	5	3000	183.0	183.0	20.0
TLV70228PDBVT	SOT-23	DBV	5	250	183.0	183.0	20.0
TLV70229DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV70229DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV70229DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV70229DBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
TLV70229DSER	WSON	DSE	6	3000	183.0	183.0	20.0
TLV70229DSET	WSON	DSE	6	250	183.0	183.0	20.0
TLV70230DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV70230DBVR	SOT-23	DBV	5	3000	183.0	183.0	20.0
TLV70230DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV70230DBVT	SOT-23	DBV	5	250	183.0	183.0	20.0
TLV70230DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV70231DBVR	SOT-23	DBV	5	3000	183.0	183.0	20.0
TLV70231DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV70231DBVT	SOT-23	DBV	5	250	183.0	183.0	20.0
TLV70231DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV70233DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV70233DBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
TLV70233DSER	WSON	DSE	6	3000	200.0	183.0	25.0
TLV70233DSET	WSON	DSE	6	250	200.0	183.0	25.0
TLV70233PDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV70233PDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV70235DBVR	SOT-23	DBV	5	3000	183.0	183.0	20.0
TLV70235DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV70235DBVT	SOT-23	DBV	5	250	183.0	183.0	20.0
TLV70235DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV70236DSER	WSON	DSE	6	3000	200.0	183.0	25.0
TLV70236DSET	WSON	DSE	6	250	203.0	203.0	35.0
TLV70237DBVR	SOT-23	DBV	5	3000	183.0	183.0	20.0
TLV70237DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV70237DBVT	SOT-23	DBV	5	250	183.0	183.0	20.0
TLV70237DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV70237DSER	WSON	DSE	6	3000	183.0	183.0	20.0

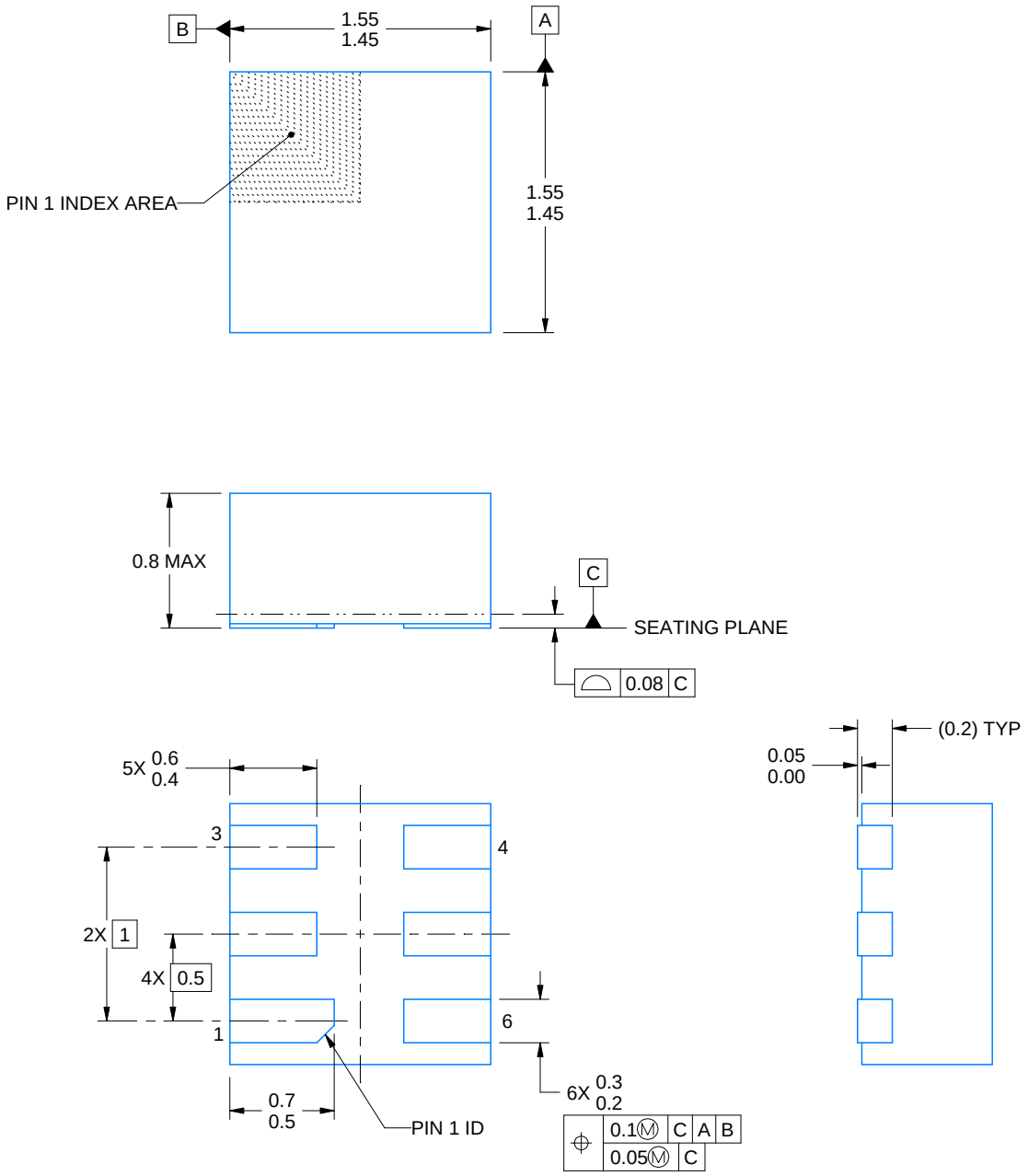
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV70237DSET	WSON	DSE	6	250	183.0	183.0	20.0
TLV70242PDSER	WSON	DSE	6	3000	183.0	183.0	20.0
TLV70242PDSET	WSON	DSE	6	250	183.0	183.0	20.0
TLV70243DSER	WSON	DSE	6	3000	183.0	183.0	20.0
TLV70243DSET	WSON	DSE	6	250	183.0	183.0	20.0
TLV70245DBVR	SOT-23	DBV	5	3000	183.0	183.0	20.0
TLV70245DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV70245DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV70245DBVT	SOT-23	DBV	5	250	183.0	183.0	20.0
TLV702475DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV702475DBVR	SOT-23	DBV	5	3000	183.0	183.0	20.0
TLV702475DBVT	SOT-23	DBV	5	250	183.0	183.0	20.0
TLV702475DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0

DSE0006A

PACKAGE OUTLINE

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



4220552/B 01/2024

NOTES:

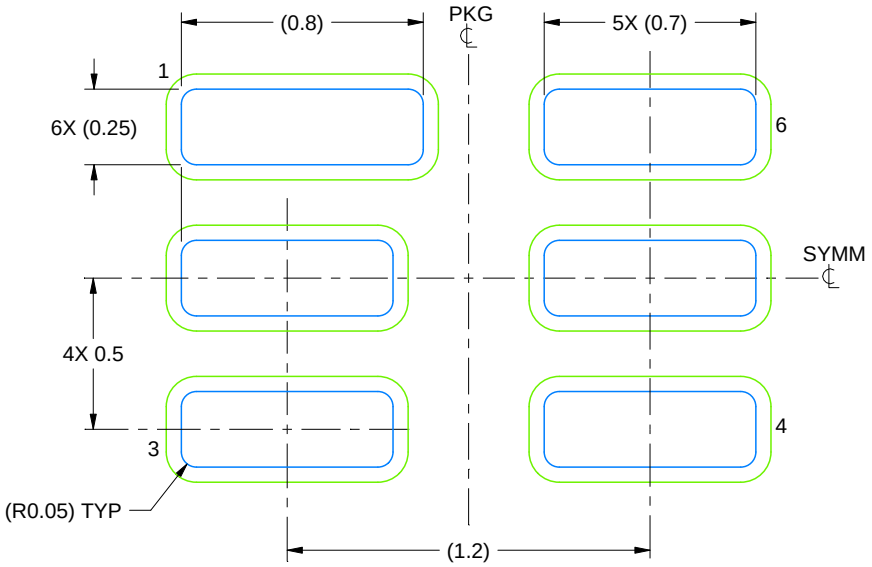
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

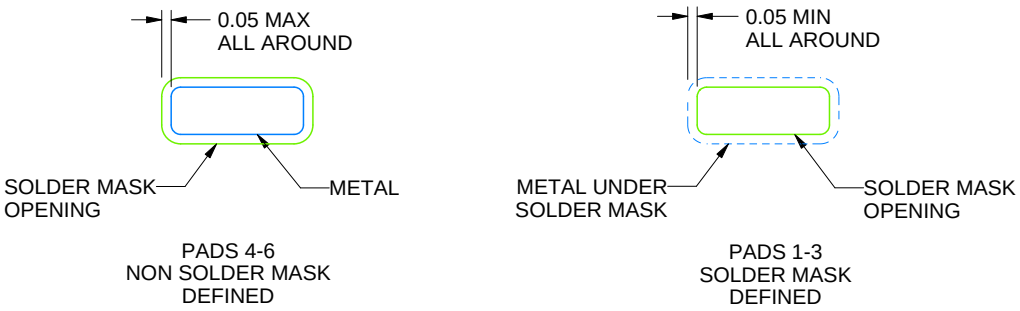
DSE0006A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SCALE:40X



SOLDER MASK DETAILS

4220552/B 01/2024

NOTES: (continued)

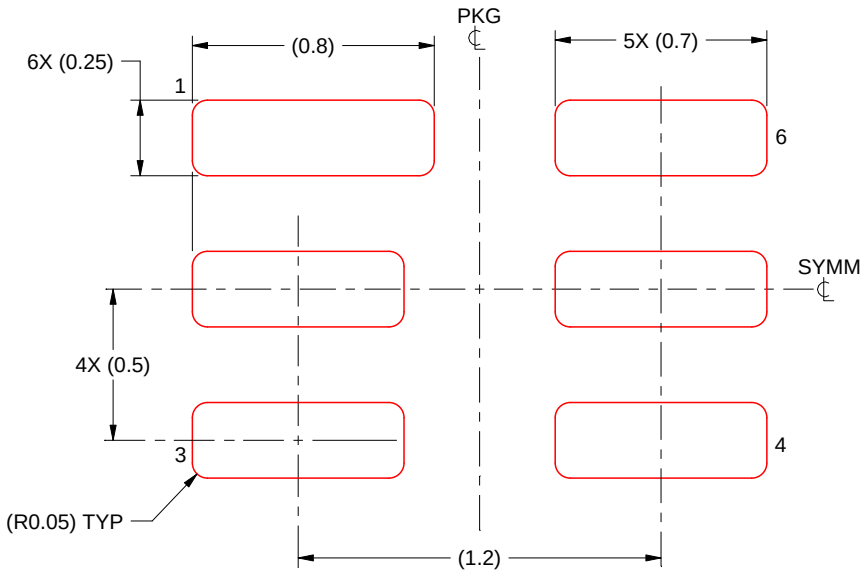
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DSE0006A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:40X

NOTES: (continued)

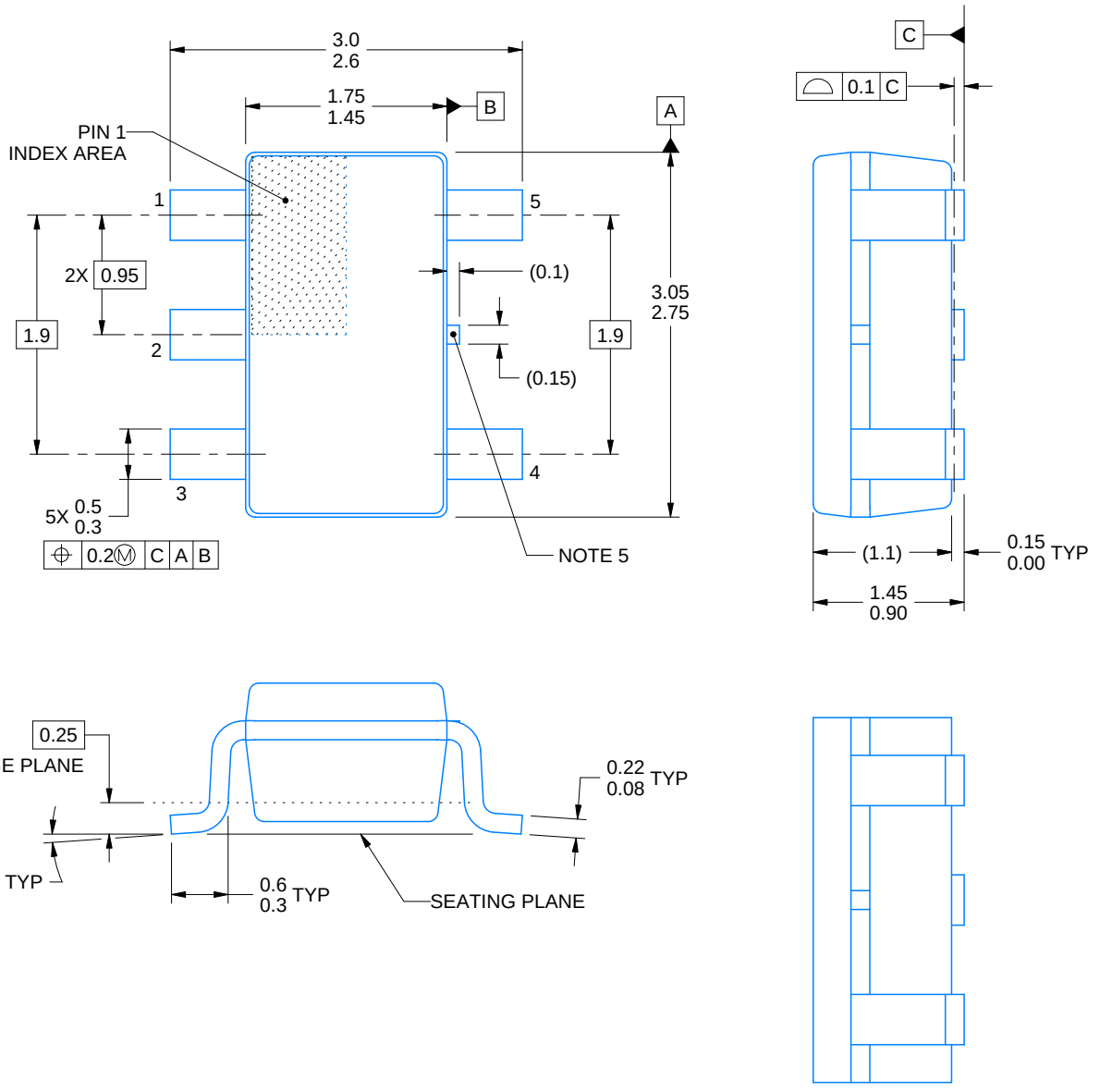
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

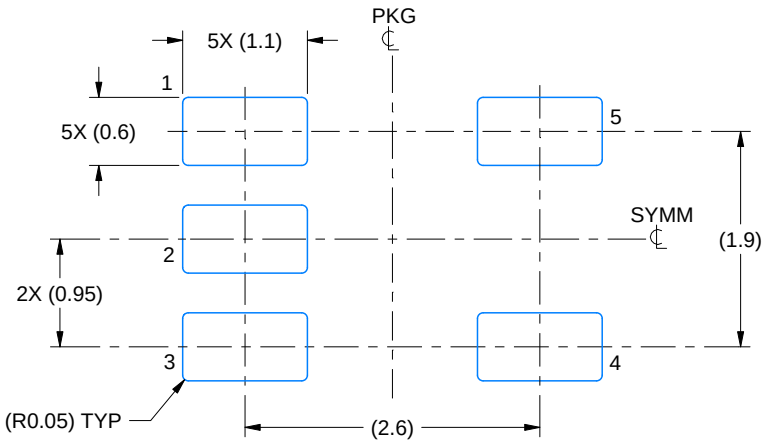


ALTERNATIVE PACKAGE SINGULATION VIEW

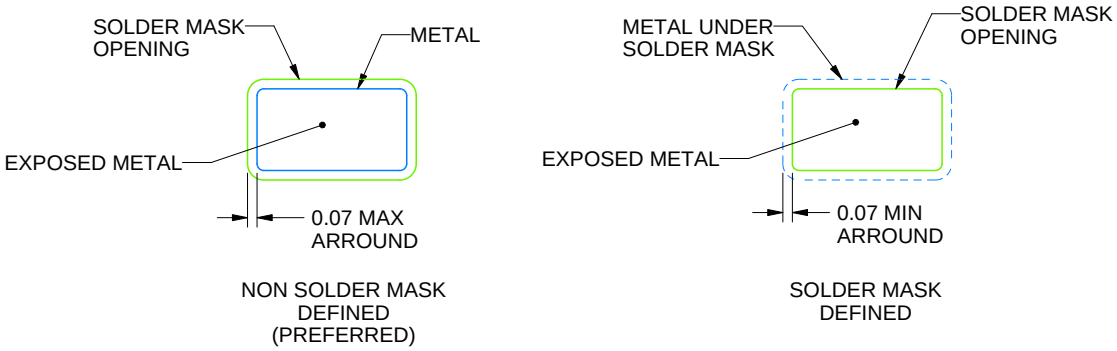
4214839/J 02/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

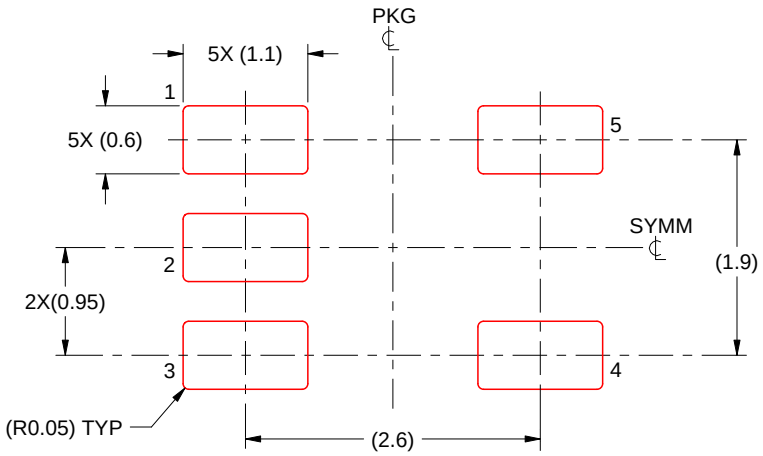


SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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