TMP75C-Q1 1.8-V Digital Temperature Sensor with Two-Wire Interface and Alert

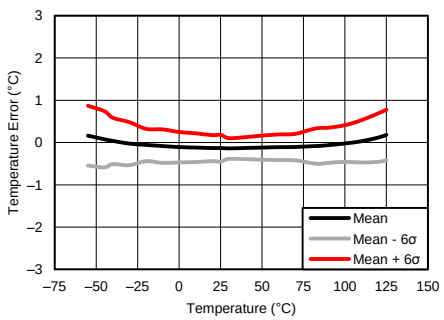
1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classification Level C5
- Low-Voltage Alternative to NCT75 and ADT75
- Digital Output with Two-Wire Serial Interface
- Up to 8 Pin-Programmable Bus Addresses
- Overtemperature ALERT Pin with Programmable Trip Values
- Shutdown Mode for Battery Power Saving
- One-Shot Conversion Mode
- Operating Temperature Range: –40°C to +125°C
- Operating Supply Range: 1.4 V to 3.6 V
- Quiescent Current:
  15 μA Active (typ), 0.3 μA Shutdown (typ)
- Accuracy:
  - ±0.25°C (typ) from 0°C to +70°C
  - ±0.5°C (typ) from –20°C to +85°C
  - ±1°C (typ) from –40°C to +125°C
- Resolution: 12 Bits (0.0625°C)
- Packages: SOIC-8 and VSSOP-8

2 Applications

- Server and Computer Thermal Management
- Telecommunication Equipment
- Office Machines, Set-Top Boxes, Thermostat Controls
- Video Game Consoles
- Power Supply and Battery Thermal Protection
- Environmental Monitoring and HVAC
- Electrical Motor Driver Thermal Protection

Temperature Accuracy (Error) vs Ambient Temperature



3 Description

The TMP75C-Q1 is an integrated digital temperature sensor with a 12-bit analog-to-digital converter (ADC) that can operate at a 1.8-V supply, and is pin and register compatible with the NCT75 and ADT75. This device is available in SOIC-8 and VSSOP-8 packages and requires no external components to sense the temperature. The TMP75C-Q1 is capable of reading temperatures with a resolution of 0.0625°C and is specified over a temperature range of –40°C to +125°C.

The TMP75C-Q1 features SMBus and two-wire interface compatibility, and allows up to eight devices on the same bus with the SMBus overtemperature alert function. The programmable temperature limits and the ALERT pin allow the sensor to operate as a stand-alone thermostat, or an overtemperature alarm for power throttling or system shutdown.

The factory-calibrated temperature accuracy and the noise-immune digital interface make the TMP75C-Q1 the preferred solution for temperature compensation of other sensors and electronic components, without the need for additional system-level calibration or elaborate board layout for distributed temperature sensing.

The TMP75C-Q1 is ideal for thermal management and protection of a variety of consumer, computer, communication, industrial, and environmental applications.

Device Information(1)

DEVICE NAME	PACKAGE	BODY SIZE (NOM)
TMP75C-Q1	SOIC (8)	4.90 mm × 3.90 mm
	VSSOP (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the package option addendum at the end of the datasheet.

Simplified Schematic

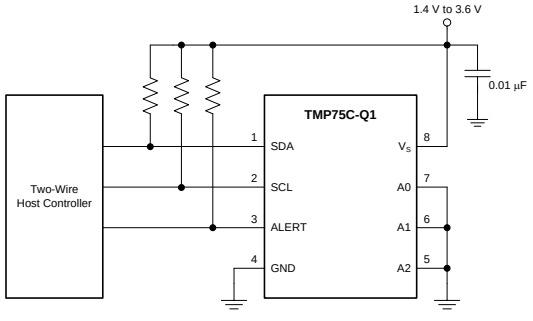


Table of Contents

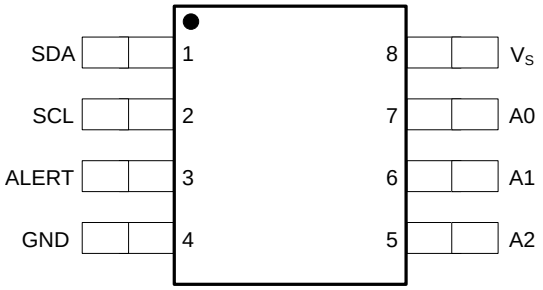
1 Features ... 1
2 Applications ... 1
3 Description ... 1
4 Revision History ... 2
5 Pin Configuration and Functions ... 3
6 Specifications ... 4
6.1 Absolute Maximum Ratings ... 4
6.2 ESD Ratings ... 4
6.3 Recommended Operating Conditions ... 4
6.4 Thermal Information ... 4
6.5 Electrical Characteristics ... 5
6.6 Typical Characteristics ... 6
7 Detailed Description ... 7
7.1 Overview ... 7
7.2 Functional Block Diagram ... 7
7.3 Feature Description ... 8
7.4 Device Functional Modes ... 15
7.5 Programming ... 16
7.6 Register Map ... 16
8 Application and Implementation ... 19
8.1 Application Information ... 19
8.2 Typical Application ... 19
9 Power Supply Recommendations ... 20
10 Layout ... 21
10.1 Layout Guidelines ... 21
10.2 Layout Example ... 21
11 Device and Documentation Support ... 22
11.1 Documentation Support ... 22
11.2 Receiving Notification of Documentation Updates 22
11.3 Community Resources ... 22
11.4 Trademarks ... 22
11.5 Electrostatic Discharge Caution ... 22
11.6 Glossary ... 22
12 Mechanical, Packaging, and Orderable Information ... 22

4 Revision History

DATE	REVISION	NOTES
November 2016	*	Initial release.

5 Pin Configuration and Functions

D and DGK Packages
8-Pin SOIC and VSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
A0	7	I	Address select. Connect to GND or V_S.
A1	6	I	Address select. Connect to GND or V_S.
A2	5	I	Address select. Connect to GND or V_S.
ALERT	3	O	Overtemperature alert. Open-drain output; requires a pull-up resistor.
GND	4	—	Ground.
SCL	2	I	Serial clock.
SDA	1	I/O	Serial data. Open-drain output; requires a pull-up resistor.
V_S	8	I	Supply voltage, 1.4 V to 3.6 V.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Supply voltage, V_S			4	V
Input voltage	SDA, SCL, ALERT, A2, A1	–0.3	4	V
	A0	–0.3	(V_S) + 0.3	V
Sink current	SDA, ALERT		10	mA
Operating junction temperature		–40	150	°C
Storage temperature, T_{stg}		–60	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 (1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage	1.4	1.8	3.6	V
Operating free-air temperature, T_A	–40		125	°C

6.4 Thermal Information

THERMAL METRIC (1)		TMP75C-Q1		UNIT
		D (SOIC)	DGK (VSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	125.4	188.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	71.5	79.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	65.8	109.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	21.1	15.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	65.3	108	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

At T_A = –40°C to +125°C and V_S = +1.4 V to +3.6 V, unless otherwise noted. Typical values at T_A = 25°C and V_S = +1.8 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TEMPERATURE INPUT						
	Temperature range		–40		125	°C
	Temperature resolution			0.0625		°C
	Temperature accuracy (error)	0°C to +70°C		±0.25	±1	°C
		–20°C to +85°C		±0.5	±2	
		–40°C to +125°C		±1	±3	
DIGITAL INPUT/OUTPUT						
V_{IH}	High-level input voltage		0.7(V_S)		V_S	V
V_{IL}	Low-level input voltage		-0.3		0.3(V_S)	V
I_{IN}	Input current	0 V < V_{IN} < (V_S) + 0.3 V			1	µA
V_{OL}	Low-level output voltage	V_S ≥ 2 V, I_{OUT} = 3 mA			0.4	V
		V_S < 2 V, I_{OUT} = 3 mA			0.2(V_S)	
	ADC resolution			12		Bit
	Conversion time	One-shot mode	20	27	35	ms
	Update Rate			80		ms
	Bus timeout time		16	22	29	ms
POWER SUPPLY						
	Operating supply range		1.4		3.6	V
I_Q	Quiescent current	Serial bus inactive		15	37	µA
		Serial bus active, SCL frequency = 400 kHz		25		
		Serial bus active, SCL frequency = 3.4 MHz		95		
I_{SD}	Shutdown current	Serial bus inactive		0.3	8	µA
		Serial bus active, SCL frequency = 400 kHz		10		
		Serial bus active, SCL frequency = 3.4 MHz		80		

6.6 Typical Characteristics

At T_A = 25°C and V_S = +1.8 V (unless otherwise noted).

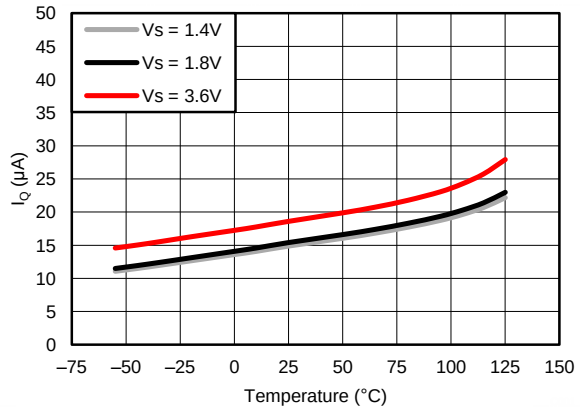


Figure 1. Quiescent Current vs Temperature

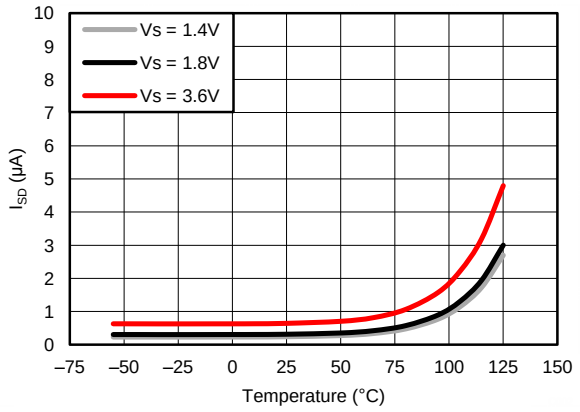


Figure 2. Shutdown Current vs Temperature

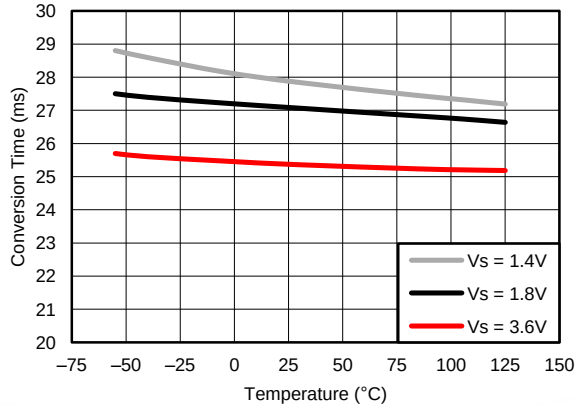


Figure 3. Conversion Time vs Temperature

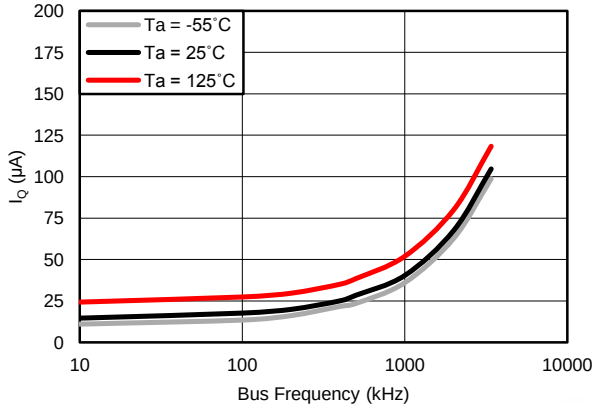


Figure 4. Quiescent Current vs Bus Frequency

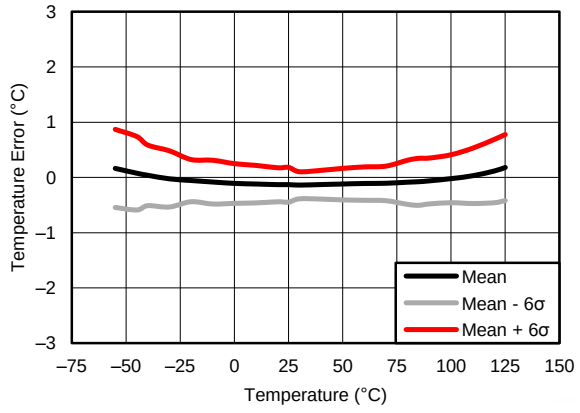


Figure 5. Temperature Error vs Temperature

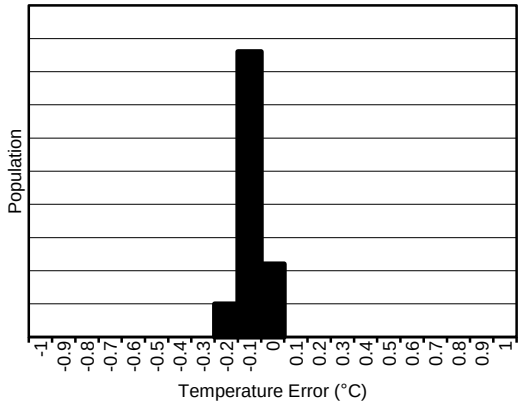


Figure 6. Temperature Error at 25°C

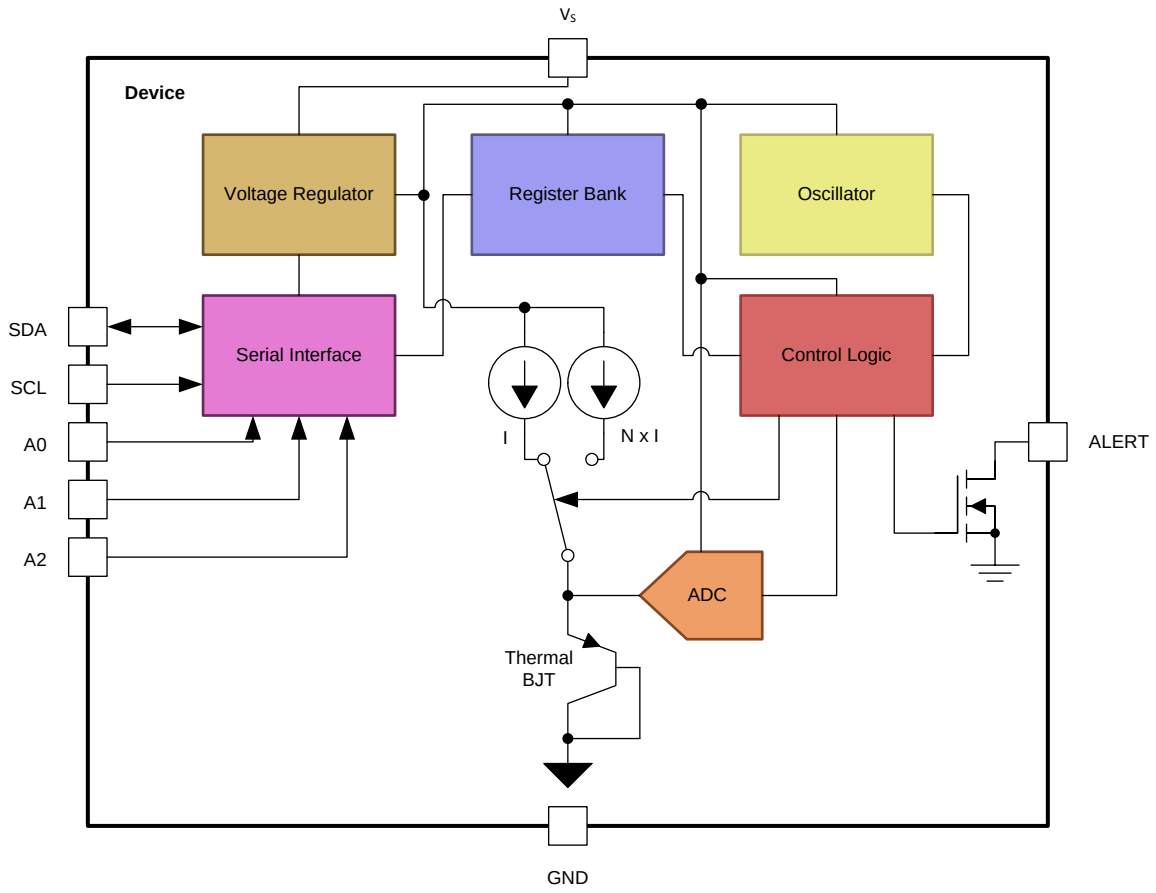
7 Detailed Description

7.1 Overview

The TMP75C-Q1 is a digital temperature sensor optimal for thermal management and thermal protection applications. The TMP75C-Q1 is two-wire and SMBus interface compatible, and is specified over a temperature range of –40°C to +125°C.

The temperature sensing device for the TMP75C-Q1 is the chip itself. A bipolar junction transistor (BJT) inside the chip is used in a band-gap configuration to produce a voltage proportional to the chip temperature. The voltage is digitized and converted to a 12-bit temperature result in degrees Celsius, with resolution of 0.0625°C. The package leads provide the primary thermal path because of the lower thermal resistance of the metal. Thus, the temperature result is equivalent to the local temperature of the printed circuit board (PCB) where the sensor is mounted.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Digital Temperature Output

The 12-bit digital output from each temperature measurement conversion is stored in the read-only temperature register. Two bytes must be read to obtain the data, as shown in Figure 14. Note that byte 1 is the most significant byte, followed by byte 2, the least significant byte. The temperature result is left-justified with the 12 most significant bits used to indicate the temperature. There is no need to read the second byte if resolution below 1°C is not required. Table 1 summarizes the temperature data format. One LSB equals 0.0625°C. Negative numbers are represented in binary twos complement format.

Table 1. Temperature Data Format(1)

TEMPERATURE (°C)	DIGITAL OUTPUT	
	BINARY	HEX
128	0111 1111 1111	7FF
127.9375	0111 1111 1111	7FF
100	0110 0100 0000	640
80	0101 0000 0000	500
75	0100 1011 0000	4B0
50	0011 0010 0000	320
25	0001 1001 0000	190
0.25	0000 0000 0100	004
0	0000 0000 0000	000
–0.25	1111 1111 1100	FFC
–25	1110 0111 0000	E70
–40	1101 1000 0000	D80

(1) The temperature sensor resolution is 0.0625°C/LSB.

Table 1 does not supply a full list of all temperatures. Use the following rules to obtain the digital data format for a given temperature, and vice versa.

To convert positive temperatures to a digital data format:

Divide the temperature by the resolution. Then, convert the result to binary code with a 12-bit, left-justified format, and MSB = 0 to denote a positive sign.

Example: (+50°C) / (0.0625°C / LSB) = 800 = 320h = 0011 0010 0000

To convert a positive digital data format to temperature:

Convert the 12-bit, left-justified binary temperature result, with the MSB = 0 to denote a positive sign, to a decimal number. Then, multiply the decimal number by the resolution to obtain the positive temperature.

Example: 0011 0010 0000 = 320h = 800 × (0.0625°C / LSB) = +50°C

To convert negative temperatures to a digital data format:

Divide the absolute value of the temperature by the resolution, and convert the result to binary code with a 12-bit, left-justified format. Then, generate the twos complement of the result by complementing the binary number and adding one. Denote a negative number with MSB = 1.

Example: (|–25°C|) / (0.0625°C / LSB) = 400 = 190h = 0001 1001 0000

Two's complement format: 1110 0110 1111 + 1 = 1110 0111 0000

To convert a negative digital data format to temperature:

Generate the twos compliment of the 12-bit, left-justified binary number of the temperature result (with MSB = 1, denoting negative temperature result) by complementing the binary number and adding one. Convert to decimal number and multiply by the resolution to get the absolute temperature, then multiply by –1 for the negative sign.

Example: 1110 0111 0000 has twos complement of 0001 1001 0000 = 0001 1000 1111 + 1

Convert to temperature: 0001 1001 0000 = 190h = 400; 400 × (0.0625°C / LSB) = 25°C = (|–25°C|); (|–25°C|) × (–1) = –25°C

7.3.2 Temperature Limits and Alert

The temperature limits are stored in the T_{LOW} and T_{HIGH} registers (Table 7 and Table 8) in the same format as the temperature result, and their values are compared to the temperature result on every conversion. The outcome of the comparison drives the behavior of the ALERT pin, which can operate as a comparator output or an interrupt, and is set by the TM bit in the Configuration register (Table 6).

In comparator mode (TM = 0, default), the ALERT pin becomes active when the temperature is equal to or exceeds the value in T_{HIGH} (fault conditions) for a consecutive number of conversions as set by the FQ bits of the configuration register. ALERT clears when the temperature falls below T_{LOW} for the same consecutive number of conversions. The difference between the two limits acts as a hysteresis on the comparator output, and a fault counter prevents false alerts as a result of environmental noise.

In interrupt mode (TM = 1), the ALERT pin becomes active when the temperature equals or exceeds the value in T_{HIGH} for a consecutive number of fault conditions. The ALERT pin remains active until a read operation of any register occurs. After the ALERT pin is cleared, this pin becomes active again only when temperature falls below T_{LOW} for a consecutive number of fault conditions, and remains active until cleared by a read operation of any register. The cycle repeats with the ALERT pin becoming active when the temperature equals or exceeds T_{HIGH}, and so on. The ALERT pin is cleared also when the device is placed in shutdown mode (see Shutdown Mode for shutdown mode description). This action also clears the fault counter memory.

The active state of the ALERT pin is set by the POL bit in the configuration register. When POL = 0 (default), the ALERT pin is active low. When POL = 1, the ALERT pin is active high. The operation of the ALERT pin in the various modes is illustrated in Figure 7.

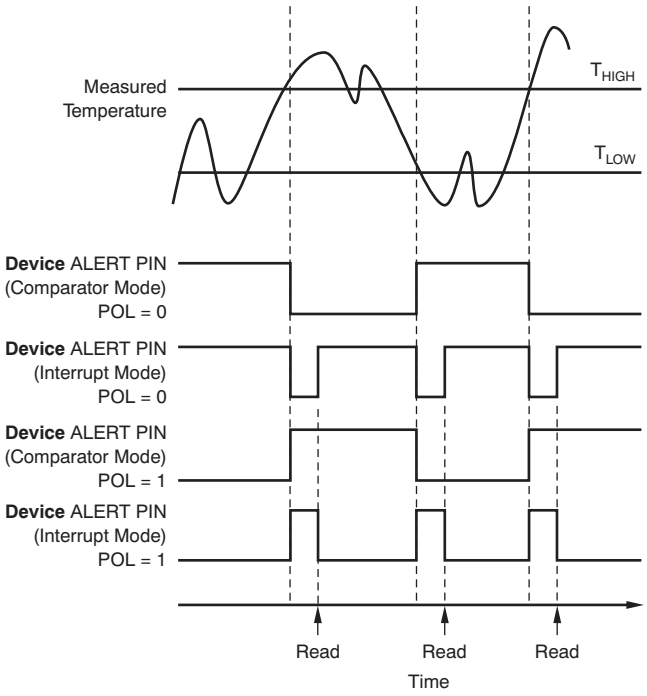


Figure 7. ALERT Pin Modes of Operation

7.3.3 Serial Interface

The TMP75C-Q1 operates as a slave device only on the two-wire bus and SMBus. Connections to the bus are made using the open-drain I/O lines, SDA and SCL. The SDA and SCL pins feature integrated spike-suppression filters and Schmitt triggers to minimize the effects of input spikes and bus noise. The TMP75C-Q1 supports the transmission protocol for both fast (1 kHz to 400 kHz) and high-speed (1 kHz to 3 MHz) modes. All data bytes are transmitted MSB first.

7.3.3.1 Bus Overview

The device that initiates the transfer is called a *master*, and the devices controlled by the master are *slaves*. The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the start and stop conditions.

To address a specific device, initiate a start condition by pulling the data line (SDA) from a high to a low logic level while SCL is high. All slaves on the bus shift in the slave address byte; the last bit indicates whether a read or write operation follows. During the ninth clock pulse, the slave being addressed responds to the master by generating an acknowledge bit and pulling SDA low.

Data transfer is then initiated and sent over eight clock pulses followed by an acknowledge bit. During data transfer, SDA must remain stable while SCL is high because any change in SDA while SCL is high is interpreted as a start or stop signal.

After all data have been transferred, the master generates a stop condition indicated by pulling SDA from low to high, while SCL is high.

7.3.3.2 Serial Bus Address

To communicate with the TMP75C-Q1, the master must first communicate with slave devices using a slave address byte. The slave address byte consists of seven address bits, and a direction bit indicating the intent of executing either a read or write operation. The TMP75C-Q1 features three address pins that allow up to eight devices to be addressed on a single bus. The TMP75C-Q1 latches the status of the address pins at the start of a communication. Table 2 describes the pin logic levels and the corresponding address values.

Table 2. Address Pin Connections and Slave Addresses

DEVICE TWO-WIRE ADDRESS	A2	A1	A0
1001000	GND	GND	GND
1001001	GND	GND	V_S
1001010	GND	V_S	GND
1001011	GND	V_S	V_S
1001100	V_S	GND	GND
1001101	V_S	GND	V_S
1001110	V_S	V_S	GND
1001111	V_S	V_S	V_S

7.3.3.3 Writing and Reading Operation

Accessing a particular register on the TMP75C-Q1 is accomplished by writing the appropriate value to the pointer register. The value for the pointer register is the first byte transferred after the slave address byte with the R/$\overline{W}$ bit low. Every write operation to the TMP75C-Q1 requires a value for the pointer register (see Figure 9).

When reading from the TMP75C-Q1, the last value stored in the pointer register by a write operation is used to determine which register is read by a read operation. To change the register pointer for a read operation, a new value must be written to the pointer register. This action is accomplished by issuing a slave address byte with the R/$\overline{W}$ bit low, followed by the pointer register byte. No additional data are required. The master can then generate a start condition and send the slave address byte with the R/$\overline{W}$ bit high to initiate the read command. See Figure 10 for details of this sequence. If repeated reads from the same register are desired, there is no need to continually send the pointer register bytes because the TMP75C-Q1 stores the pointer register value until it is changed by the next write operation.

Note that register bytes are sent with the most significant byte first, followed by the least significant byte.

7.3.3.4 Slave Mode Operations

The TMP75C-Q1 can operate as a slave receiver or slave transmitter.

7.3.3.4.1 Slave Receiver Mode:

The first byte transmitted by the master is the slave address, with the R/$\overline{W}$ bit low. The TMP75C-Q1 then acknowledges reception of a valid address. The next byte transmitted by the master is the pointer register. The TMP75C-Q1 then acknowledges reception of the pointer register byte. The next byte or bytes are written to the register addressed by the pointer register. The TMP75C-Q1 acknowledges reception of each data byte. The master can terminate data transfer by generating a start or stop condition.

7.3.3.4.2 Slave Transmitter Mode:

The first byte transmitted by the master is the slave address, with the R/$\overline{W}$ bit high. The slave acknowledges reception of a valid slave address. The next byte is transmitted by the slave and is the most significant byte of the register indicated by the pointer register. The master acknowledges reception of the data byte. The next byte transmitted by the slave is the least significant byte. The master acknowledges reception of the data byte. The master can terminate data transfer by generating a not-acknowledge bit on reception of any data byte, or by generating a start or stop condition.

7.3.3.5 High-Speed (Hs) Mode

In order for the two-wire bus to operate at frequencies above 400 kHz, the master device must issue an SMBus Hs-mode master code (00001xxx) as the first byte after a start condition to switch the bus to high-speed operation. The TMP75C-Q1 does not acknowledge this byte, but does switch its input filters on SDA and SCL and its output filters on SDA to operate in Hs-mode, allowing transfers at up to 3 MHz. After the Hs-mode master code has been issued, the master transmits a two-wire slave address to initiate a data-transfer operation. The bus continues to operate in Hs-mode until a stop condition occurs on the bus. Upon receiving the stop condition, the TMP75C-Q1 switches the input and output filters back to fast-mode operation.

7.3.3.6 Timeout Function

The TMP75C-Q1 resets the serial interface if SCL or SDA are held low for 22 ms (typ) between a start and stop condition. If the TMP75C-Q1 is pulled low, it releases the bus and then waits for a start condition. To avoid activating the timeout function, it is necessary to maintain a communication speed of at least 1 kHz for the SCL operating frequency.

7.3.3.7 Two-Wire Timing

The TMP75C-Q1 is two-wire and SMBus compatible. Figure 8 to Figure 10 describe the various operations on the TMP75C-Q1. Parameters for Figure 8 are defined in Table 3. Bus definitions are:

Bus Idle Both SDA and SCL lines remain high.

Start Data Transfer A change in the state of the SDA line, from high to low, while the SCL line is high defines a start condition. Each data transfer is initiated with a start condition.

Stop Data Transfer A change in the state of the SDA line from low to high while the SCL line is high defines a stop condition. Each data transfer is terminated with a repeated start or stop condition.

Data Transfer The number of data bytes transferred between a start and a stop condition is not limited, and is determined by the master device.

The receiver acknowledges the transfer of data. It is also possible to use the TMP75B for single-byte updates. To update only the MS byte, terminate communication by issuing a start or stop condition on the bus.

Acknowledge Each receiving device, when addressed, must generate an acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse so that the SDA line is stable low during the high period of the acknowledge clock pulse. Setup and hold times must be taken into account. When a master receives data, the termination of the data transfer can be signaled by the master generating a *not-acknowledge* (1) on the last byte transmitted by the slave.

Table 3. Timing Diagram Requirements

			FAST MODE		HIGH-SPEED MODE		
			MIN	MAX	MIN	MAX	UNIT
$f_{(SCL)}$	SCL operating frequency	$V_S \geq 1.8$ V	0.001	0.4	0.001	3	MHz
		$V_S < 1.8$ V	0.001	0.4	0.001	2.5	MHz
$t_{(BUF)}$	Bus free time between stop and start conditions	$V_S \geq 1.8$ V	1300		160		ns
		$V_S < 1.8$ V	1300		260		ns
$t_{(HDSTA)}$	Hold time after repeated start condition. After this period, the first clock is generated.		600		160		ns
$t_{(SUSTA)}$	Repeated start condition setup time		600		160		ns
$t_{(SUSTO)}$	Stop condition setup time		600		160		ns
$t_{(HDDAT)}$	Data hold time	$V_S \geq 1.8$ V	0	900	0	100	ns
		$V_S < 1.8$ V	0	900	0	140	ns
$t_{(SUDAT)}$	Data setup time	$V_S \geq 1.8$ V	100		10		ns
		$V_S < 1.8$ V	100		20		ns
$t_{(LOW)}$	SCL clock low period	$V_S \geq 1.8$ V	1300		190		ns
		$V_S < 1.8$ V	1300		240		ns
$t_{(HIGH)}$	SCL clock high period		600		60		ns
$t_{R(SDA)}$, $t_{F(SDA)}$	Data rise and fall time			300		80	ns
$t_{R(SCL)}$, $t_{F(SCL)}$	Clock rise and fall time			300		40	ns
t_R	Clock and data rise time for SCLK ≤ 100 kHz			1000			ns

7.3.3.8 Two-Wire Timing Diagrams

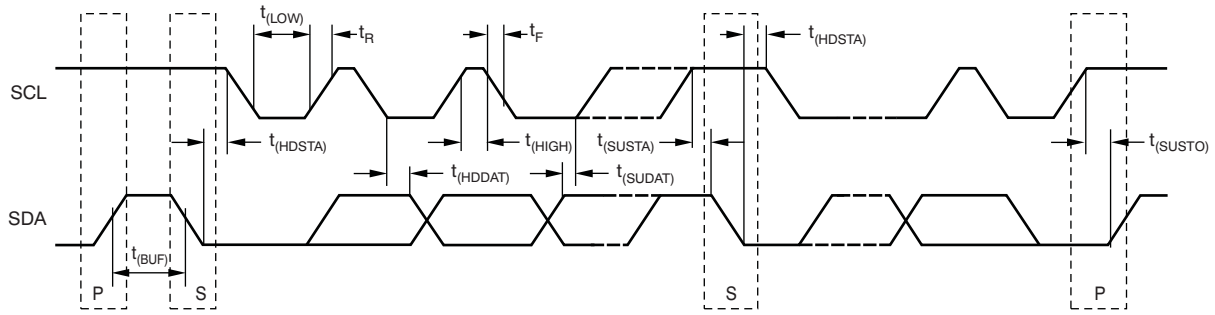
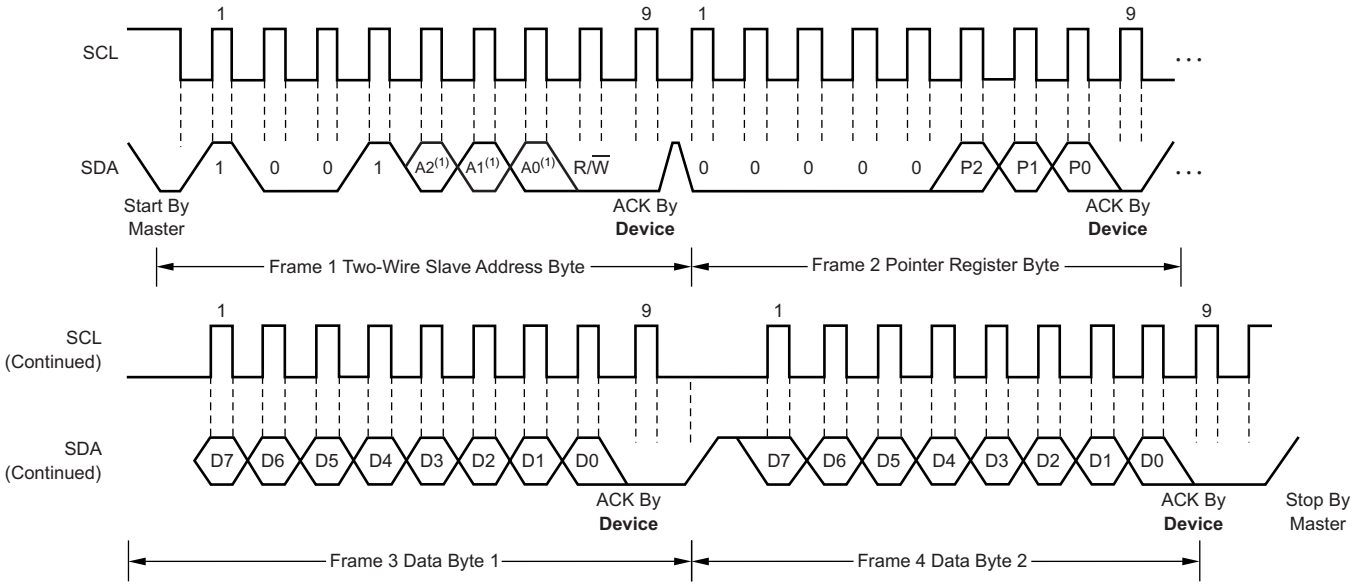
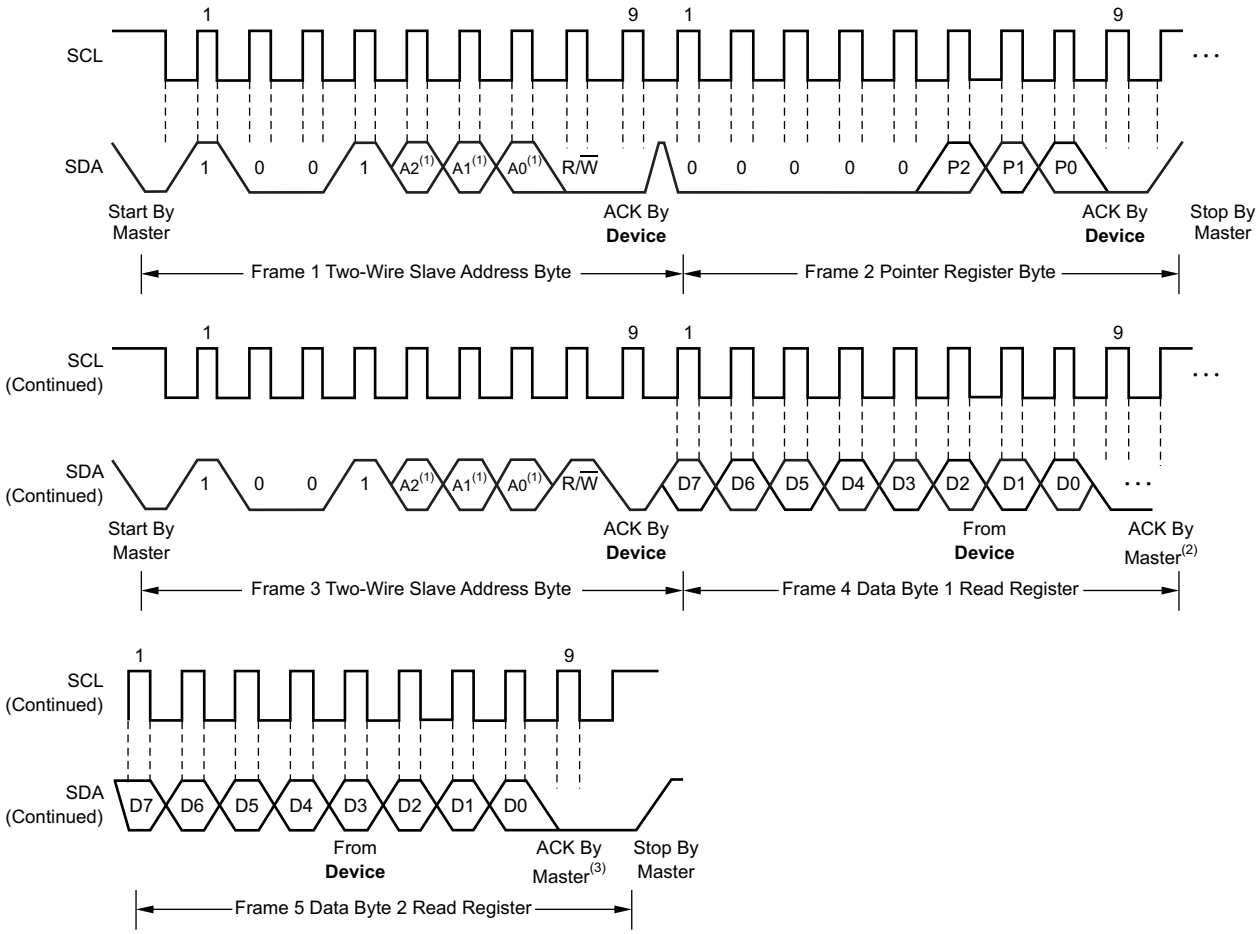


Figure 8. Two-Wire Timing Diagram



(1) The value of A0, A1, and A2 are determined by the connections of the corresponding pins.

Figure 9. Two-Wire Timing Diagram for Write Word Format



(1) The value of A0, A1, and A2 are determined by the connections of the corresponding pins.

(2) Master should leave SDA high to terminate a single-byte read operation.

(3) Master should leave SDA high to terminate a two-byte read operation.

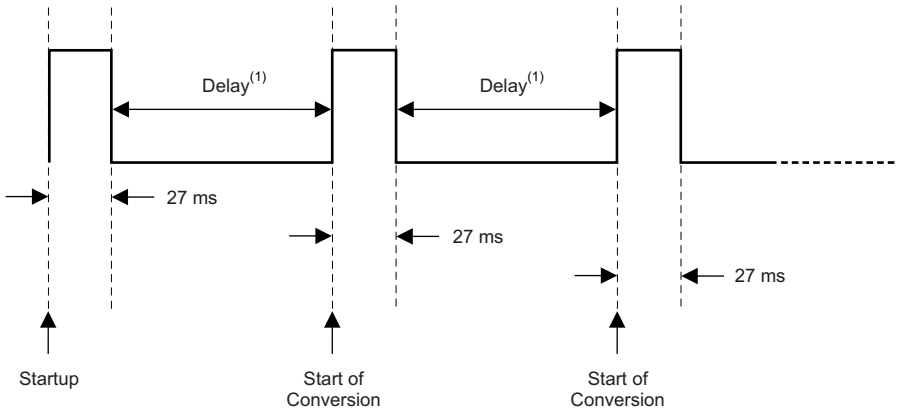
Figure 10. Two-Wire Timing Diagram for Read Word Format

7.4 Device Functional Modes

7.4.1 Continuous-Conversion Mode

The default mode of the TMP75C-Q1 is continuous conversion, where the ADC performs continuous temperature conversions and stores each result to the Temperature register, overwriting the result from the previous conversion. The typical conversion rate of TMP75C-Q1 is 12 Hz, with 80 ms between the start of each consecutive conversion. The TMP75C-Q1 has a typical conversion time of 27 ms. To achieve its conversion rates, the TMP75C-Q1 makes a conversion, and then powers down and waits for a delay 53 ms.

After power-up, the TMP75C-Q1 immediately starts a conversion, as shown in Figure 11. The first result is available after 27 ms (typical). The active quiescent current during conversion is 45 μA (typical at +25°C). The quiescent current during delay is 1 μA (typical at +25°C).



(1) Delay is set to 53 ms (typ).

Figure 11. Conversion Start

7.4.2 Shutdown Mode

The shutdown mode saves maximum power by shutting down all device circuitry other than the serial interface, and reduces current consumption to typically less than 0.3 μA. Shutdown mode is enabled when the SD bit in the configuration register is set to 1; the device shuts down and terminates a conversion if it is ongoing. When SD is equal to 0, the device operates in continuous-conversion mode. When shutdown mode is enabled, the ALERT pin and fault counter clear in both comparator and interrupt modes. The ALERT pin and the fault counter remain clear until the SD bit is set.

7.4.3 One-Shot Mode

The TMP75C-Q1 features a one-shot temperature measurement mode. When the device is in continuous conversion (SD = 0), writing a 1 to the OS bit enables shutdown mode, where any write to the one-shot register triggers a single temperature conversion. The device returns to the shutdown state at the completion of the single conversion, and a subsequent write to the one-shot register triggers another single conversion followed by a return to shutdown state. This mode reduces power consumption in the TMP75C-Q1 when continuous temperature monitoring is not required.

When the device is in complete shutdown (SD = 1), the one-shot mode is not active regardless of the state of the OS bit, and a write to the one-shot register has no effect.

7.5 Programming

Figure 12 shows the internal register structure of the TMP75C-Q1. Use the 8-bit pointer register to address a given data register. The pointer register uses the three LSBs to identify which of the data registers respond to a read or write command. Figure 13 identifies the bits of the pointer register byte.

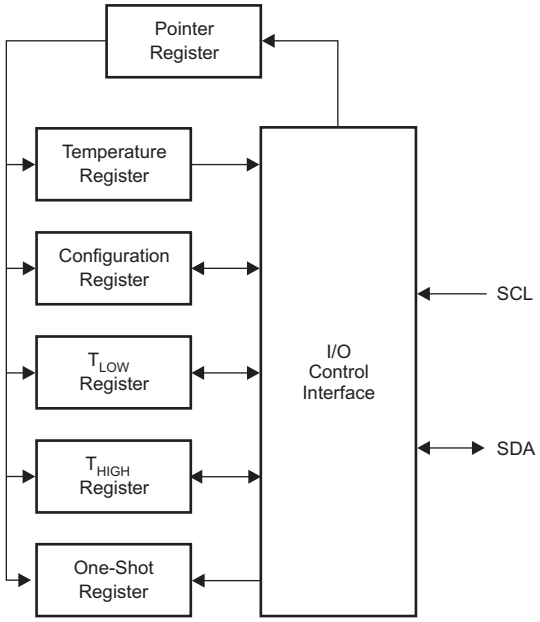


Figure 12. Internal Register Structure

7.6 Register Map

Table 4 describes the registers available in the TMP75C-Q1 with their pointer addresses, followed by the description of the bits in each register.

Table 4. Register Map and Pointer Addresses

P2	P1	P0	REGISTER
0	0	0	Temperature register (read only, default)
0	0	1	Configuration register (read/write)
0	1	0	T_{LOW} register (read/write)
0	1	1	T_{HIGH} register (read/write)
1	0	0	One-Shot register (write only; write any value to start a conversion)

Figure 13. Pointer Register (pointer = N/A) [reset = 00h]

7	6	5	4	3	2	1	0
Reserved					P2	P1	P0
W-0h					W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

Figure 14. Temperature Register (pointer = 0h) [reset = 0000h]

15	14	13	12	11	10	9	8
T11	T10	T9	T8	T7	T6	T5	T4
R-00h							
7	6	5	4	3	2	1	0
T3	T2	T1	T0	Reserved			
R-0h				R-0h			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 5. Temperature Register Description

Name	Description
T11 to T4	The 8 MSBs of the temperature result (resolution of 1°C)
T3 to T0	The 4 LSBs of the temperature result (resolution of 0.0625°C)

Figure 15. Configuration Register (pointer = 1h) [reset = 0000h]

15	14	13	12	11	10	9	8
Reserved		OS	FQ		POL	TM	SD
R/W-0h		R/W-0h	R/W-0h		R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
Reserved							
R-00h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6. Configuration Register Description

Name	Description
Reserved	Reserved bits Write 0 to these bits on configuration register update.
OS	One-shot control SD = 0 and OS = 0: Continuous conversion mode (default) SD = 0 and OS = 1: One-shot mode; the device is in shutdown mode but writing any value to the one-shot register initiates a conversion. The device returns to shutdown mode at the end of the conversion. SD = 1 and OS = x: The device is in shutdown mode and the status of the OS bit has no effect. Writing to the one-shot register does not start a conversion.
FQ	Fault queue to trigger the ALERT pin FQ = 0h: 1 fault (default) FQ = 1h: 2 faults FQ = 2h: 4 faults FQ = 3h: 6 faults
POL	ALERT polarity control POL = 0: ALERT is active low (default) POL = 1: ALERT is active high
TM	ALERT thermostat mode control TM = 0: ALERT is in comparator mode (default) TM = 1: ALERT is in interrupt mode
SD	Shutdown control bit SD = 0: Device is in continuous conversion mode (default) SD = 1: Device is in shutdown mode

Figure 16. T_{LOW} - Temperature Low Limit Register (pointer = 2h) [reset = 4B00h](1)

15	14	13	12	11	10	9	8
L11	L10	L9	L8	L7	L6	L5	L4
R/W-4Bh							
7	6	5	4	3	2	1	0
L3	L2	L1	L0	Reserved			
R/W-0h				R-0h			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

(1) 4B00h = 75°C.

Table 7. T_{LOW} Register Description

Name	Description
L11 to L4	The 8 MSBs of the temperature low limit (resolution of 1°C)
L3 to L0	The 4 LSBs of the temperature low limit (resolution of 0.0625°C)

Figure 17. T_{HIGH} - Temperature High Limit Register (pointer = 3h) [reset = 5000h](1)

15	14	13	12	11	10	9	8
H11	H10	H9	H8	H7	H6	H5	H4
R/W-50h							
7	6	5	4	3	2	1	0
H3	H2	H1	H0	Reserved			
R/W-0h				R-0h			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

(1) 5000h = 80°C.

Table 8. T_{HIGH} Register Description

Name	Description
H11 to H4	The 8 MSBs of the temperature high limit (resolution of 1°C)
H3 to H0	The 4 LSBs of the temperature high limit (resolution of 0.0625°C)

8 Application and Implementation

8.1 Application Information

The TMP75C-Q1 is used to measure the PCB temperature of the location it is mounted. The programmable address options allow up to eight locations on the board to be monitored on a single serial bus. Connecting the ALERT pins together and programming the temperature limit registers to desired values allows for a temperature watchdog operation of all devices, interrupting the host controller only if the temperature exceeds the limits.

8.2 Typical Application

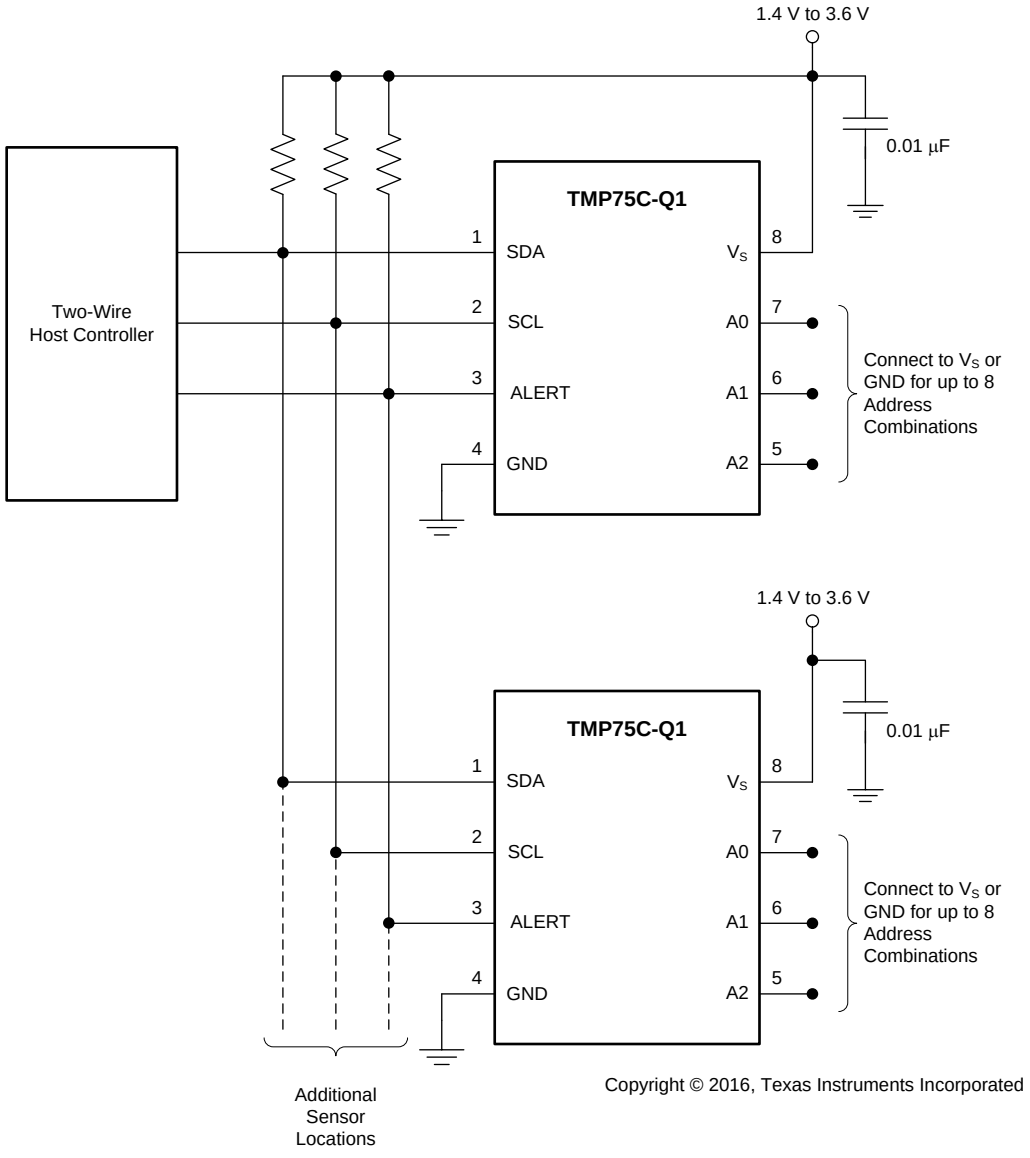


Figure 18. Temperature Monitoring of Multiple Locations on a PCB

Typical Application (continued)

8.2.1 Design Requirements

The TMP75C-Q1 only requires pull-up resistors on SDA and ALERT, although a pull-up resistor is typically present on the SCL as well. A 0.01-μF bypass capacitor on the supply is recommended, as shown in Figure 18. The SCL, SDA, and ALERT lines can be pulled up to a supply that is equal to or higher than V_S through the pull-up resistors. To configure one of eight different addresses on the bus, connect A0, A1, and A2 to either V_S or GND.

8.2.2 Detailed Design Procedure

The TMP75C-Q1 should be placed in close proximity to the heat source to be monitored, with a proper layout for good thermal coupling. This ensures that temperature changes are captured within the shortest possible time interval.

8.2.3 Application Curves

Figure 19 shows the step response of the TMP75C-Q1 to a submersion in an oil bath of 100°C from room temperature (27°C). The time-constant, or the time for the output to reach 63% of the input step, is 1.5 seconds.

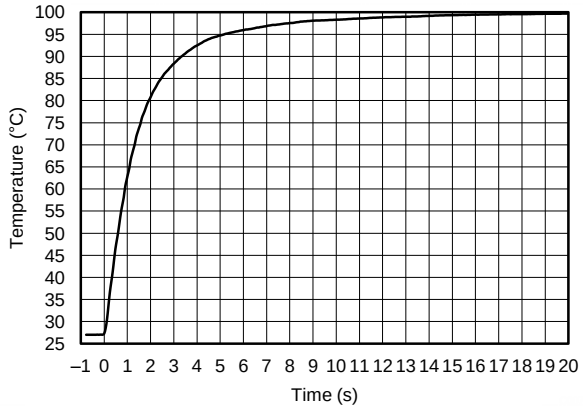


Figure 19. Temperature Step Response

9 Power Supply Recommendations

The TMP75C-Q1 operates with a power supply in the range of 1.4 V to 3.6 V. It is optimized for operation at 1.8-V supply but can measure temperature accurately in the full supply range.

A power-supply bypass capacitor is required for stability; place this capacitor as close as possible to the supply and ground pins of the device. A typical value for this supply bypass capacitor is 0.01 μF. Applications with noisy or high-impedance power supplies may require additional decoupling capacitors to reject power-supply noise.

10 Layout

10.1 Layout Guidelines

Place the power-supply bypass capacitor as close as possible to the supply and ground pins. The recommended value of this bypass capacitor is 0.01 μF. Additional decoupling capacitance can be added to compensate for noisy or high-impedance power supplies.

Pull up the open-drain output pins (SDA and ALERT) to a supply voltage rail (V_S or higher but up to 3.6 V) through 10-kΩ pull-up resistors.

10.2 Layout Example

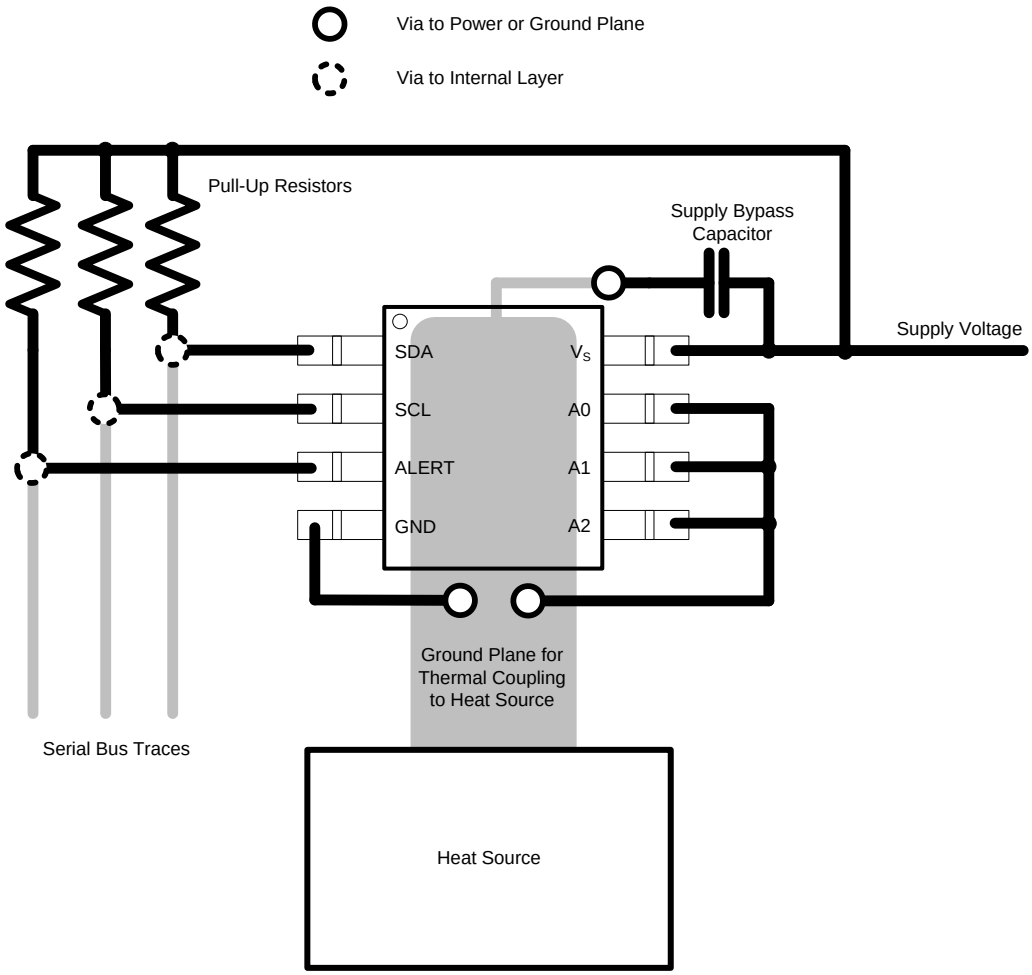


Figure 20. Layout Example

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

TMP75BEVM and TMP75CEVM User Guide (SBOU141)

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMP75CQDGKRQ1	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	T75CQ	Samples
TMP75CQDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU-DCC	Level-2-260C-1 YEAR	-40 to 125	T75CQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TMP75C-Q1 :

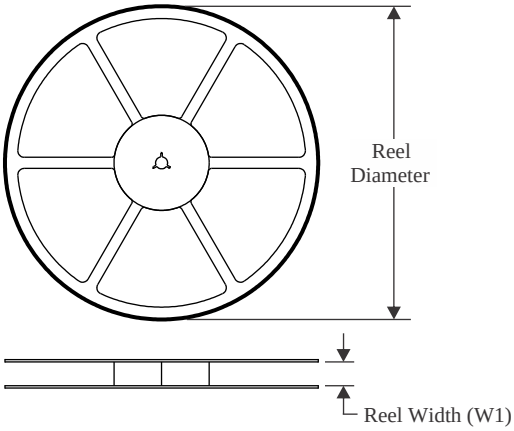
- Catalog: TMP75C

NOTE: Qualified Version Definitions:

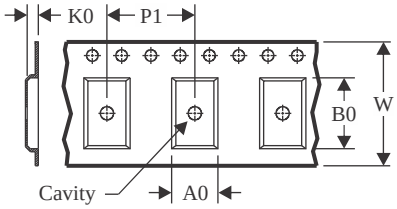
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

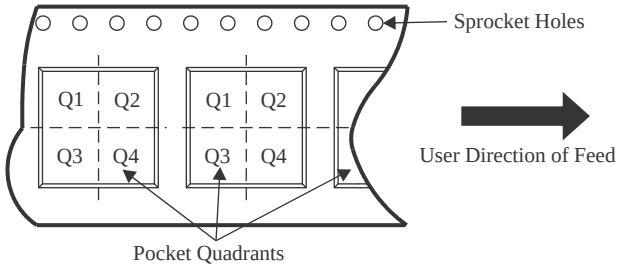


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

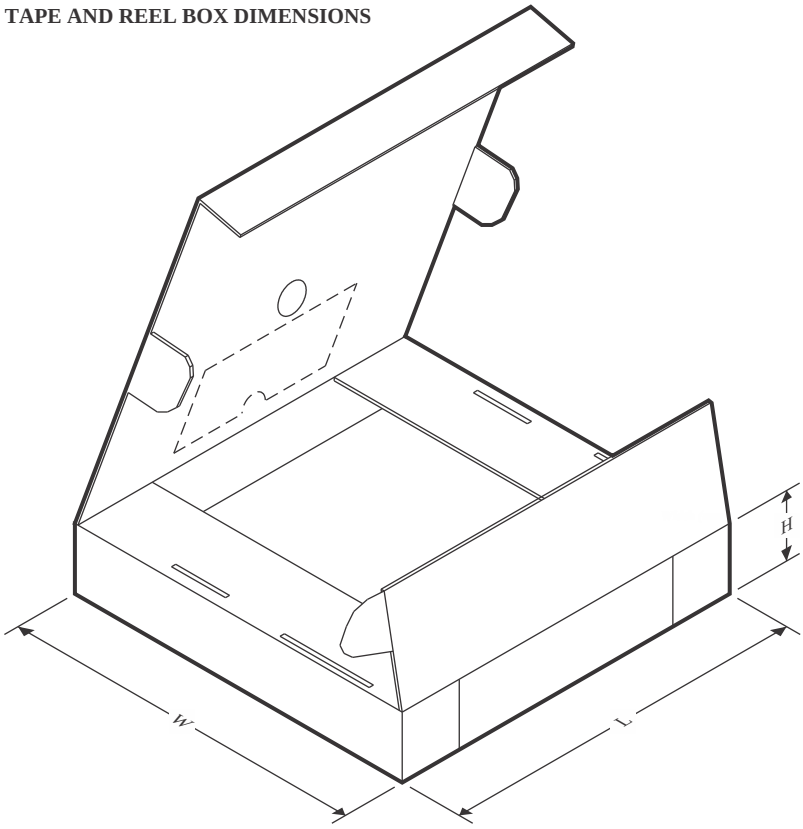
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

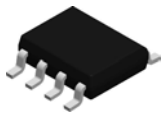
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMP75CQDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TMP75CQDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMP75CQDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
TMP75CQDRQ1	SOIC	D	8	2500	356.0	356.0	35.0

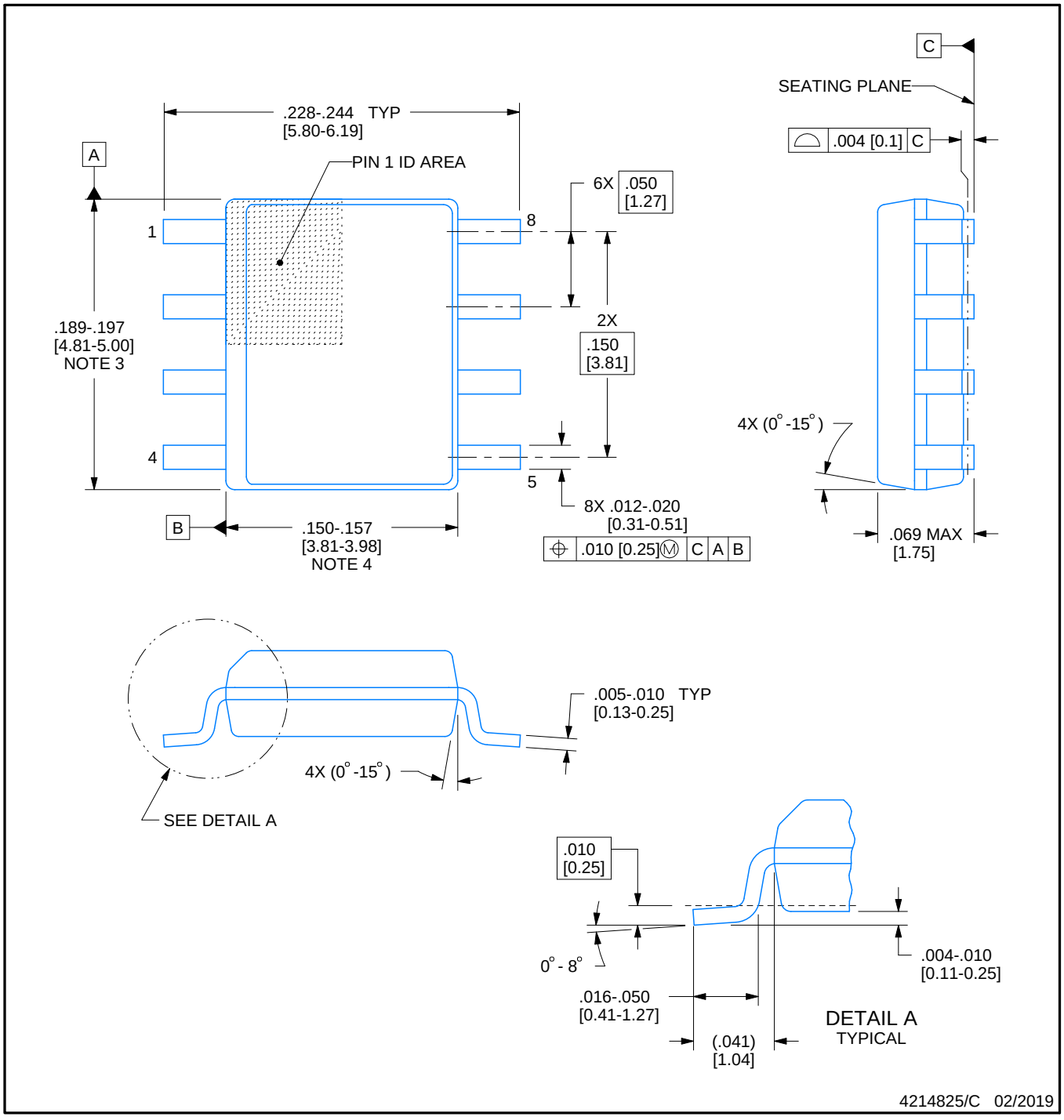


PACKAGE OUTLINE

D0008A

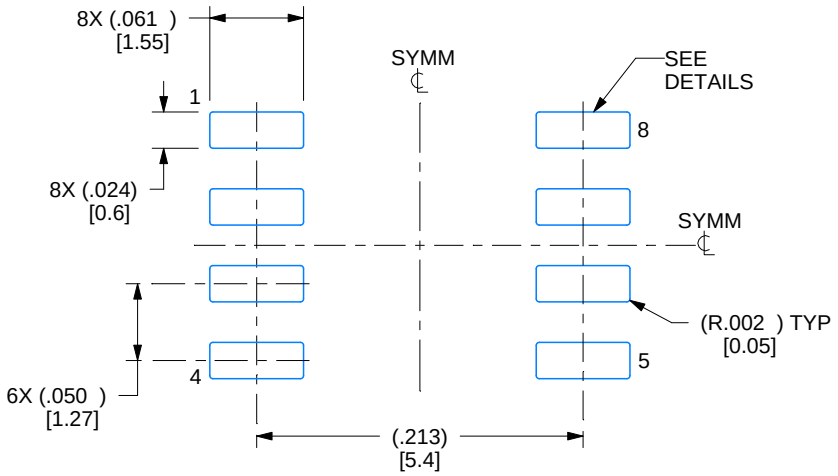
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

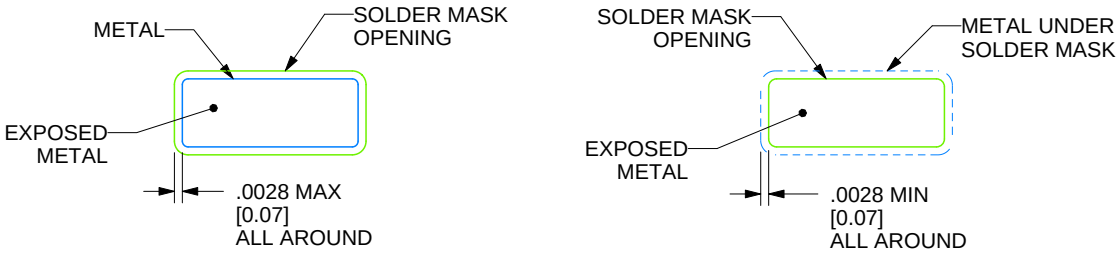


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

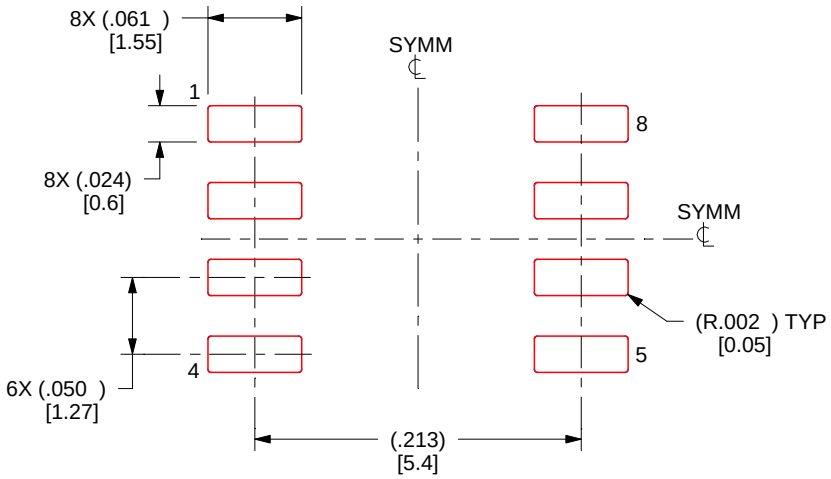
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

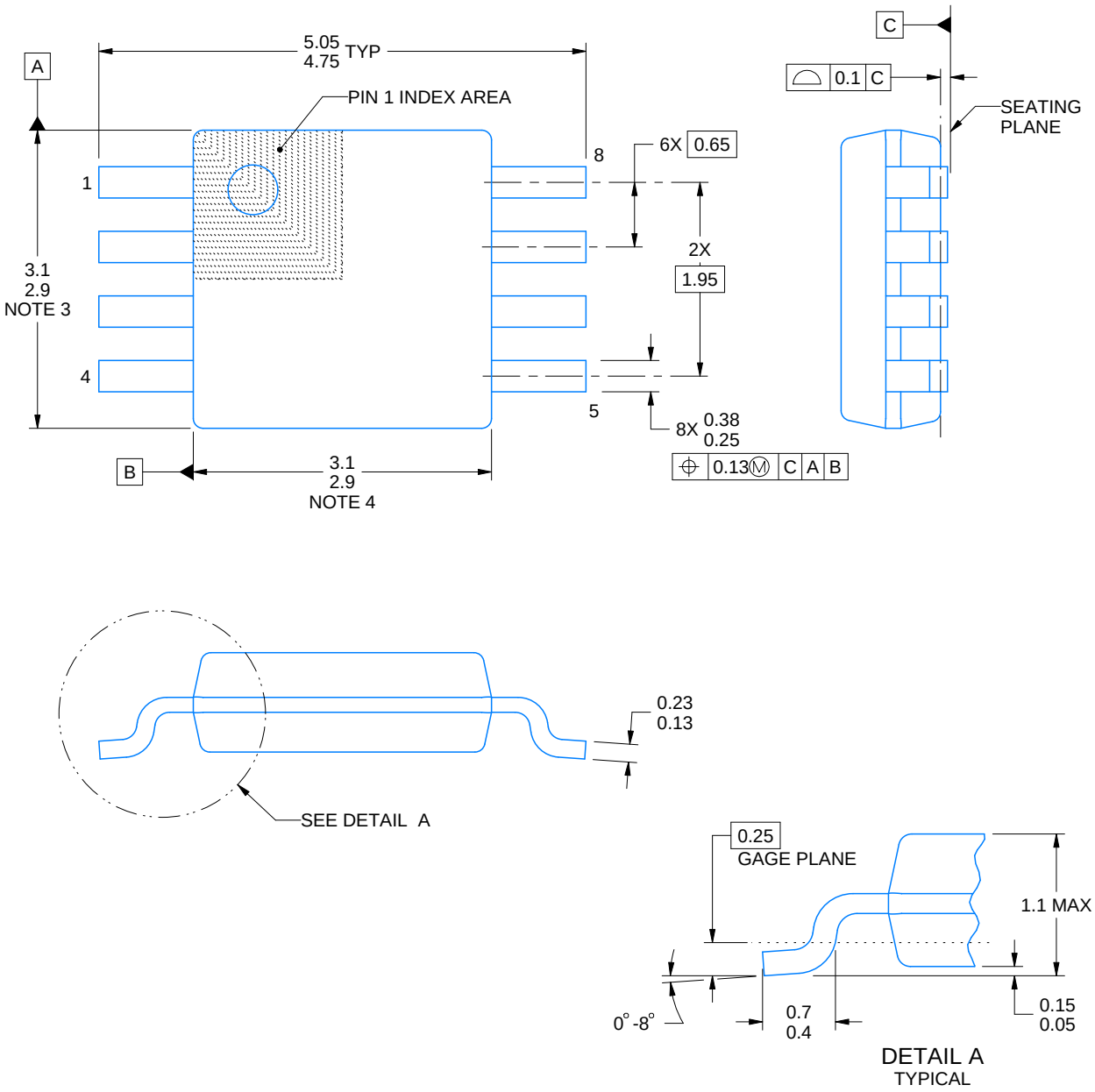
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

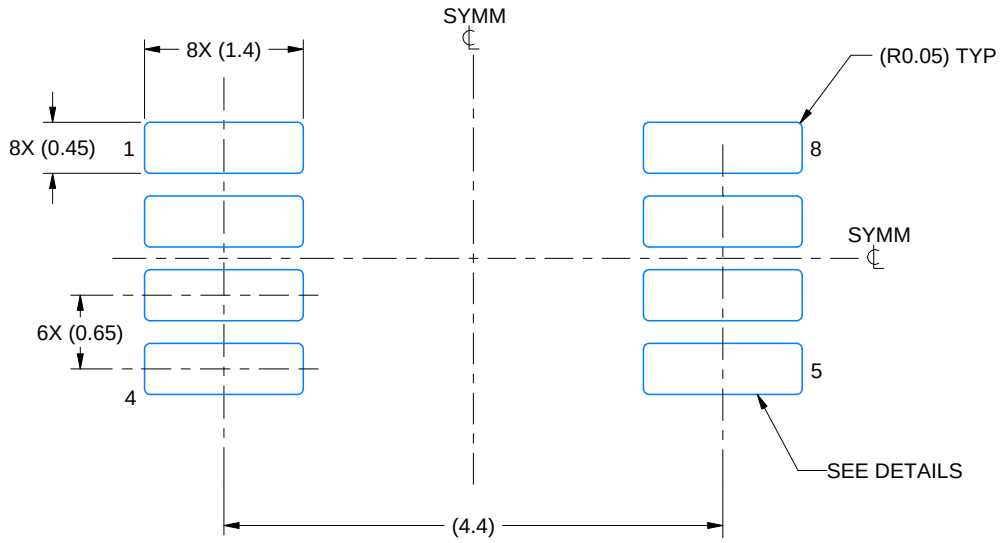
SMALL OUTLINE PACKAGE



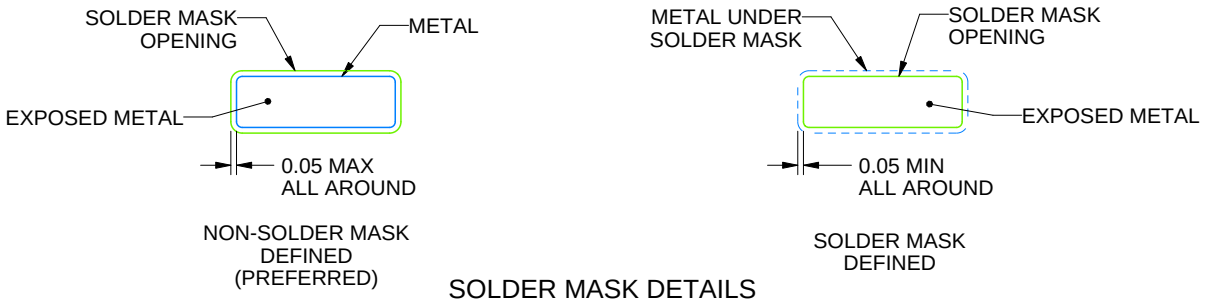
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

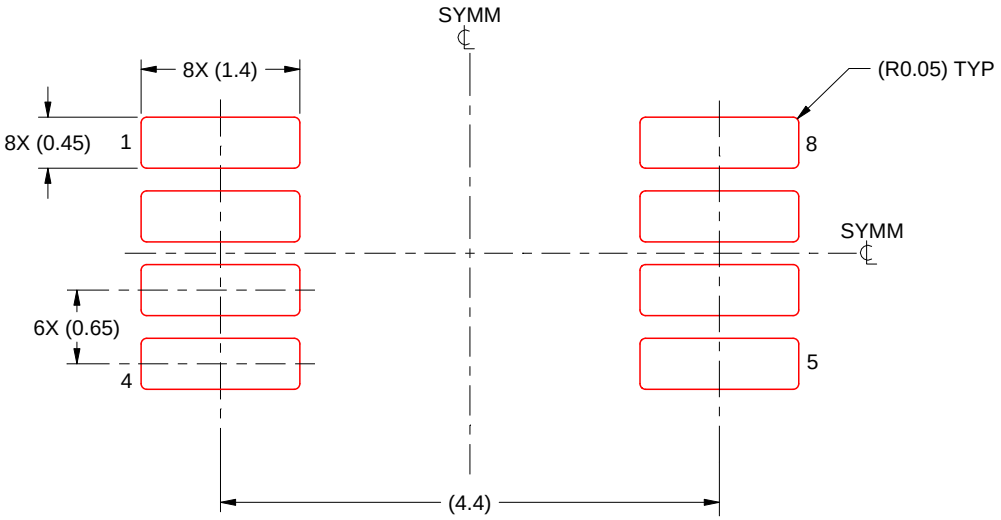


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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