XTR117 4-20mA Current-Loop Transmitter

1 Features

- Low quiescent current: 130 µA
- 5-V regulator for external circuits
- Low span error: 0.05%
- Low nonlinearity error: 0.003%
- Wide-loop supply range: 7.5 V to 36 V
- Temperature range: –40°C to +125°C
- Packages: VSON-8 and VSSOP-8

2 Applications

- Two-wire, 4-20mA current-loop transmitter
- Smart transmitter
- Industrial process control
- Test systems
- Current amplifier
- Voltage-to-current amplifier

3 Description

The XTR117 is a precision current output converter designed to transmit analog 4-mA-to-20-mA signals over an industry-standard current loop. The device provides accurate current scaling and output current limit functions.

The on-chip voltage regulator (5 V) can be used to power external circuitry. A current return pin (I_{RET}) senses any current used in external circuitry to provide an accurate control of the output current.

The XTR117 is a fundamental building block of smart sensors using 4-mA-to-20-mA current transmission.

The XTR117 is specified for operation over the extended industrial temperature range, –40°C to +125°C.

Package Information

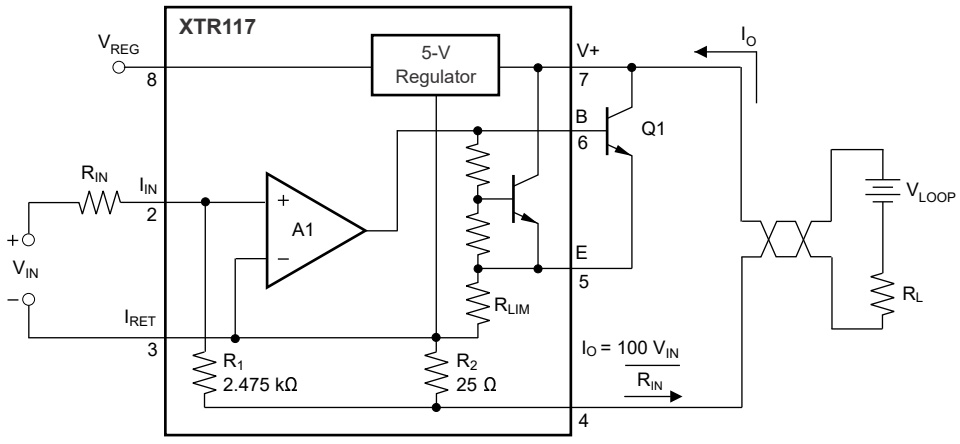
PRODUCT	PACKAGE(1)	PACKAGE SIZE(2)
XTR117	DGK (VSSOP, 8)	3 mm × 4.9 mm
	DRB (VSON, 8)	3 mm × 3 mm

(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

Related 4-20mA Devices(1)

DEVICE	DESCRIPTION
XTR115	5-V regulator output and 2.5-V reference output
XTR116	5-V regulator output and 4.096-V reference output

(1) For complete 4-20mA bridge and RTO conditioner solutions, see the XTR product family at www.ti.com.



Typical Application

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4 Pin Configuration and Functions

Figure 4-1. DGK Package, 8-Pin VSSOP (Top View)

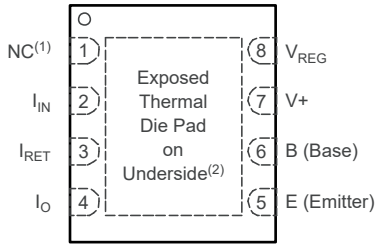


Figure 4-2. DRB Package, 8-Pin VSON (Top View)

(1) NC = No connection.
(2) Connect thermal die pad to I_{RET} or leave unconnected on PCB.

Table 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
I_{IN}	2	I	Current input pin
I_{RET}	3	I	Local ground return pin for V_{REG}
I_O	4	O	Regulated 4-mA to 20-mA current-loop output
E (Emitter)	5	I	Emitter connection for external transistor
B (Base)	6	O	Base connection for external transistor
V+	7	P	Loop power supply
V_{REG}	8	O	5-V regulator voltage output
NC	1	—	Not connected.
Thermal Pad	Pad	—	Thermal Pad. Connect to IRET or leave floating.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

5 Specifications

5.1 Absolute Maximum Ratings[1]

		MIN	MAX	UNIT
V+	Power supply (referenced to I_O pin)		40	V
	Input voltage (referenced to I_{RET} pin)	0	V+	V
	Output current limit	Continuous		
	V_{REG}, short-circuit	Continuous		
	Operating temperature	–40	125	℃
	Storage temperature	–55	150	℃
	Junction temperature		165	℃

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM)	2000	V
		Charged device model (CDM)	1000	

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V+	Power supply voltage	7.5	24	40	V
T_A	Specified temperature	–40		125	°C

5.4 Thermal Information

THERMAL METRIC[1]		XTR117		UNIT
		DGK (VSSOP)	DRB (VSON)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	173.9	60.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	95.2	33.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	11.1	4.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	93.7	33.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	66.3	70.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (bottom) thermal resistance	N/A	17.8	°C/W

(1) For information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

5.5 Electrical Characteristics

at T_A = 25°C, V+ = 24 V, R_{IN} = 20 kΩ, and TIP29C external transistor (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
I_O	Output current equation			$I_O = I_{IN} \times 100$		
	Output current, linear range		0.20		25	mA
I_{LIM}	Overscale limit			32		mA
I_{MIN}	Underscale limit	I_{REG} = 0		0.13	0.20	mA
SPAN						
S	Span (current gain)			100		A/A
	Error(1)	I_O = 200 µA to 25 mA		±0.05	±0.4	%
		I_O = 200 µA to 25 mA, T_A = –40 °C to +125°C		±3	±20	ppm/°C
	Nonlinearity	I_O = 200 µA to 25 mA		±0.003	±0.02	%
INPUT						
V_{OS}	Offset voltage (op amp)	I_{IN} = 40 µA		±100	±500	µV
		I_{IN} = 40 µA, T_A = –40 °C to +125°C		±0.7	±6	µV/°C
		I_{IN} = 40 µA, V+ = 7.5 V to 36 V		0.1	2	µV/V
I_B	Bias current			–35		nA
		T_A = –40 °C to +125°C		300		pA/°C
θ_n	Noise	0.1 Hz to 10 Hz		0.6		μV_{pp}
DYNAMIC RESPONSE						
	Small-signal bandwidth	C_{LOOP} = 0, R_L = 0		380		kHz
	Slew rate			3.2		mA/µs
V_{REG}(2)						
	Voltage			5		V
	Voltage accuracy	I_{REG} = 0 mA		±0.05	±0.1	V
		I_{REG} = 0 mA, T_A = –40 °C to +125°C		±0.1		mV/°C
		I_{REG} = 0 mA, V+ = 7.5 V to 36 V		1		mV/V
	Voltage accuracy vs V_{REG} current			See Figure 5-4		
	Short-circuit current			12		mA
POWER SUPPLY						
I_Q	Quiescent current			130	200	µA
		T_A = –40 °C to +125°C			250	

(1) Does not include initial error or temperature coefficient of R_{IN}.
(2) Voltage measured with respect to I_{RET} pin.

5.6 Typical Characteristics

At T_A = +25°C, V+ = 24 V, R_{IN} = 20 kΩ, and TIP29C external transistor (unless otherwise noted)

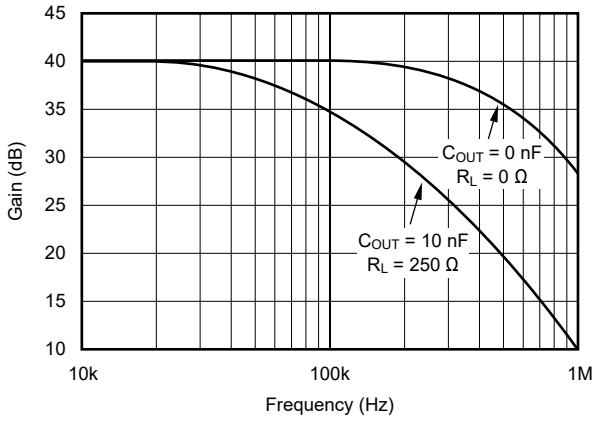


Figure 5-1. Current Gain vs Frequency

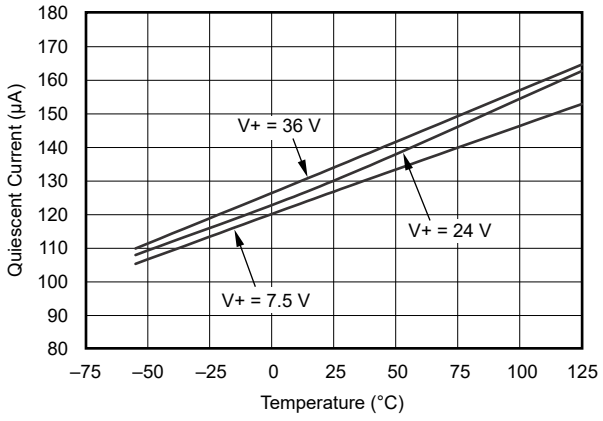


Figure 5-2. Quiescent Current vs Temperature

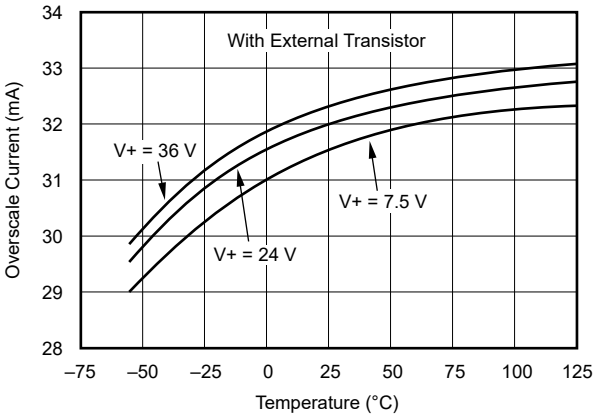


Figure 5-3. Overscale Current vs Temperature

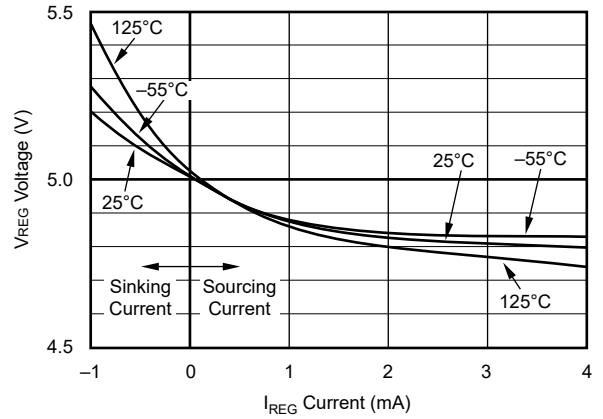


Figure 5-4. V_{REG} Voltage vs V_{REG}Current

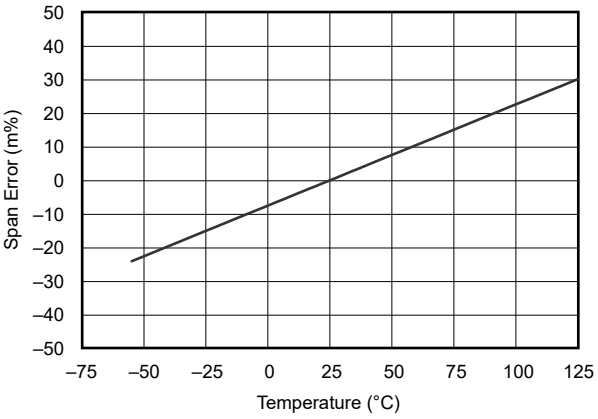


Figure 5-5. Span Error vs Temperature

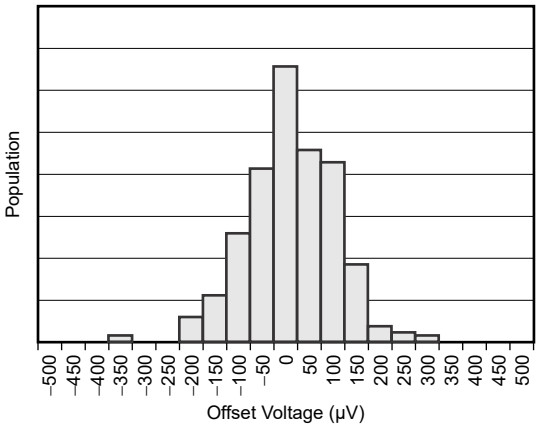


Figure 5-6. Offset Voltage Distribution

6 Detailed Description

6.1 Overview

The XTR117 is a precision current output converter designed to transmit analog 4 mA to 20 mA signals over an industry-standard current loop. Figure 6-1 shows basic circuit connections with representative simplified input circuitry. The XTR117 is a two-wire current transmitter. The input current (pin 2) controls the output current. A portion of the output current flows into the V+ power supply, pin 7. The remaining current flows in Q_1. External input circuitry connected to the XTR117 can be powered from V_{REG}. Current drawn from these terminals must be returned to I_{RET}, pin 3. The I_{RET} pin is a *local ground* for input circuitry driving the XTR117.

The XTR117 is a current-input device with a gain of 100. A current flowing into pin 2 produces $I_O = 100 \times I_{IN}$. The input voltage at the I_{IN} pin is zero (referred to the I_{RET} pin). A voltage input is converted to an input current with an external input resistor, R_{IN}, as shown in Figure 6-1. Typical full-scale input voltages range from 1 V and upward. Full-scale inputs greater than 0.5 V are recommend to minimize the effects of offset voltage and drift of A1.

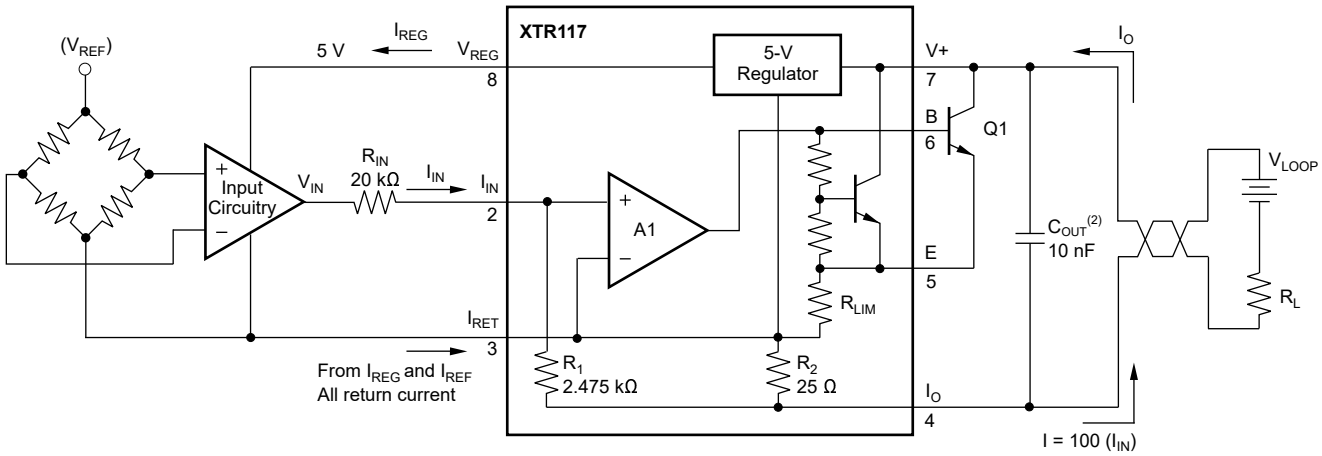
For improved precision use an external voltage reference:

DEVICE	VOLTAGE
REF35409	4.096 V
REF35300	3.0 V
REF35250	2.5 V

Use REF34xx for lower drift.

Possible choices for Q1(1)

TYPE	PACKAGE
2N4922G	TO-126
FCX690BTA	SOT-89-3
MMBTA28-7-F	SOT-23-3

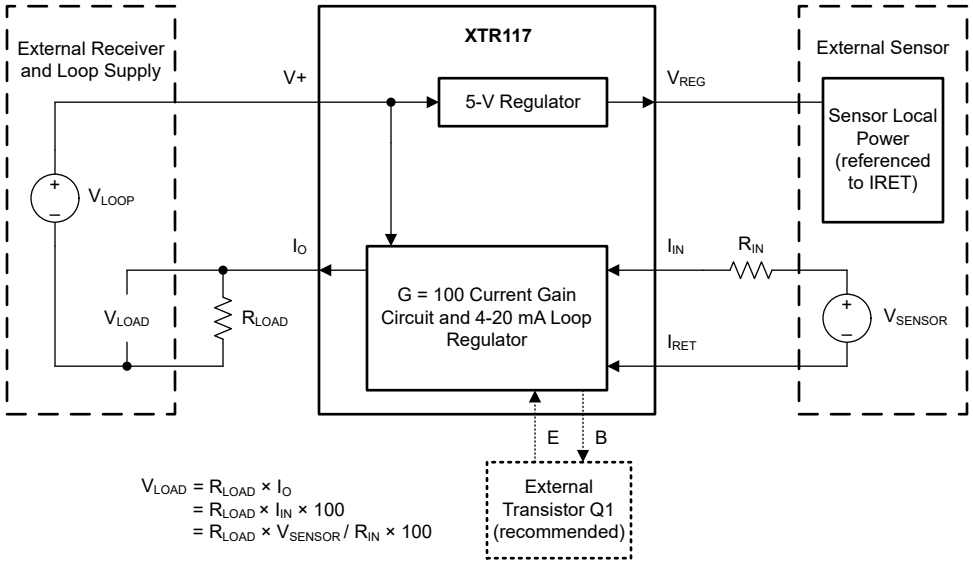


(1) See Section 7.1.1.

(2) See Section 7.1.6.

Figure 6-1. Basic Circuit Connections

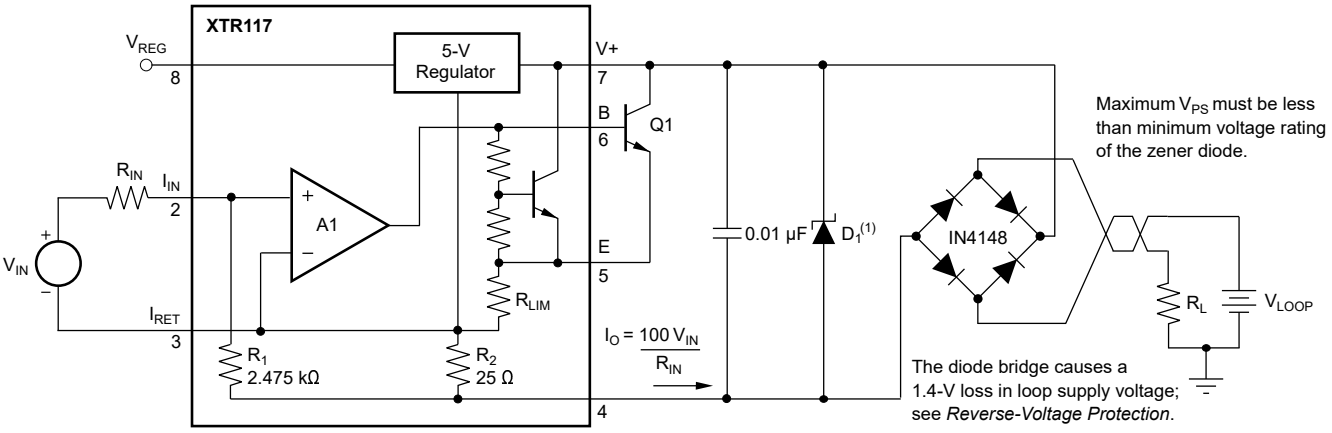
6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Reverse-Voltage Protection

The XTR117 low compliance voltage rating (minimum operating voltage) of 7.5 V permits the use of various voltage protection methods without compromising operating range. Figure 6-2 shows a diode bridge circuit that allows normal operation even when the voltage connection lines are reversed. The bridge causes a two-diode drop (approximately 1.4 V) loss in loop supply voltage. This voltage drop results in a compliance voltage of approximately 9 V—satisfactory for most applications. A diode can be inserted in series with the loop supply voltage and the V+ pin to protect against reverse output connection lines with only a 0.7-V loss in loop supply voltage.



(1) 36-V Zener diode, such as 1N4753A or P6KE39A. Use lower-voltage Zener diodes with loop power-supply voltages < 30 V for increased protection; see Section 6.3.2.

Figure 6-2. Reverse Voltage Operation and Over-Voltage Surge Protection

6.3.2 Overvoltage Surge Protection

Remote connections to current transmitters can sometimes be subjected to voltage surges. Best practice is to limit the maximum surge voltage applied to the XTR117 to as low as practical. Various Zener diode and surge clamping diodes are specially designed for this purpose. Select a clamp diode with as low a voltage rating as possible for best protection. The absolute maximum power-supply rating on the XTR117 is specified at 40 V. Keep overvoltages and transients less than 40 V to maintain reliable operation when the supply returns to normal (7.5 V to 36 V).

Most surge protection Zener diodes have a diode characteristic in the forward direction that conducts excessive current, possibly damaging receiving-side circuitry if the loop connections are reversed. If a surge-protection diode is used, use a series diode or diode bridge for protection against reversed connections.

6.3.3 VSON Package

The XTR117 is offered in a VSON-8 package (also known as SON or DFN). The VSON is a QFN package with lead contacts on only two sides of the bottom of the package. This leadless package maximizes board space and enhances thermal and electrical characteristics through an exposed pad.

VSON packages are physically small, have a smaller routing area, improved thermal performance, and improved electrical parasitics. Additionally, the absence of external leads eliminates bent-lead issues.

The VSON package can be easily mounted using standard printed circuit board (PCB) assembly techniques. See the *QFN/SON PCB Attachment* and *Quad Flatpack No-Lead Logic Packages* application notes, both available for download at www.ti.com.

Connect the exposed leadframe die pad on the bottom of the package to I_{RET} or leave unconnected.

6.4 Device Functional Modes

The device has one mode of operation that applies when operated within the *Recommended Operating Conditions*.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

7.1.1 External Transistor

The external transistor, Q_1, conducts the majority of the full-scale output current. Power dissipation in this transistor can approach 0.8 W with high loop voltage (40 V) and 20-mA output current. The XTR117 is designed to use an external transistor to avoid on-chip, thermal-induced errors. Heat produced by Q_1 still causes ambient temperature changes that can influence the XTR117 performance. To minimize these effects, locate Q_1 away from sensitive analog circuitry, including the XTR117. Mount Q_1 so that heat is conducted to the outside of the transducer housing.

The XTR117 is designed to use virtually any NPN transistor with sufficient voltage, current, and power rating. Case style and thermal mounting considerations often influence the choice for any given application. Several possible choices are listed in Figure 6-1. A MOSFET transistor does not improve the accuracy of the XTR117 and is not recommended. Although the XTR117 can be used without an additional external transistor, this configuration is not always practical at higher loop voltages and currents because of self-heating concerns.

7.1.2 Minimum Output Current

The quiescent current of the XTR117 (typically 130 µA) is the lower limit of the output current. Zero input current (I_{IN} = 0) produces an I_O equal to the quiescent current. Output current does not begin to increase until I_{IN} I_Q/ 100. Current drawn from V_{REG} is added to this minimum output current. Up to 3.8 mA is available to power external circuitry while still allowing the output current to go to less than 4 mA.

7.1.3 Offsetting the Input

A low-scale output of 4 mA is produced by creating a 40-µA input current. Figure 7-1 shows how this input current is created with the proper value resistor from an external reference voltage (V_{REF}). V_{REG} is used as shown in Figure 7-1, but does not have the temperature stability of a high-quality reference, such as the REF3425.

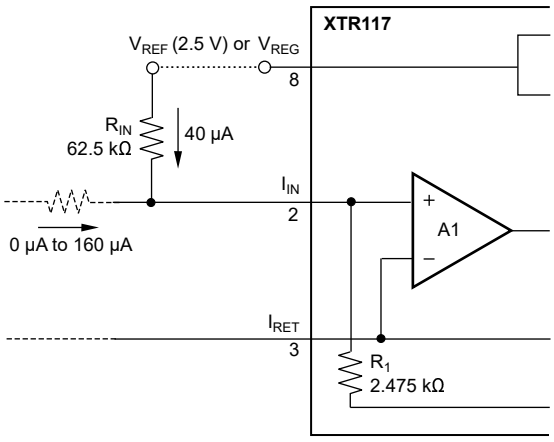


Figure 7-1. Creating Low-Scale Offset

7.1.4 Radio Frequency Interference

The long wire lengths of current loops invite radio-frequency (RF) interference. RF interference can be rectified by the input circuitry of the XTR117 or preceding circuitry. This effect generally appears as an unstable output current that varies with the position of loop supply or input wiring. Interference cab also enter at the input terminals. For integrated transmitter assemblies with short connections to the sensor, the interference more likely comes from the current-loop connections.

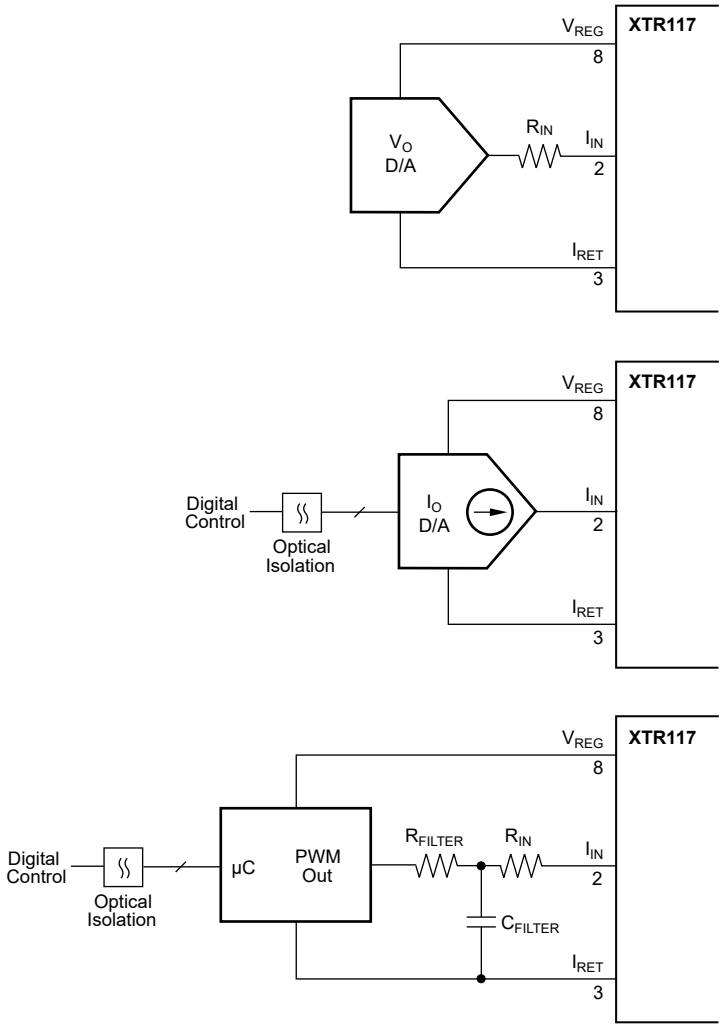


Figure 7-2. Digital Control Methods

7.1.5 Maximum Output Current

The XTR117 provides accurate, linear output up to 25 mA. Internal circuitry limits the output current to approximately 32 mA to protect the transmitter and loop power or measurement circuitry.

Extending the output current range of the XTR117 is possible by connecting an external resistor from pin 3 to pin 5 to change the current limit value.

CAUTION

All output current must flow through internal resistors; therefore, damage is possible with excessive current. Output currents greater than 45 mA can cause permanent damage.

7.1.6 Circuit Stability

The 4-20 mA control-loop stability must be evaluated for any XTR117 design. A 10-nF decoupling capacitor between V+ and I_O is recommended for most applications. As this capacitance appears in parallel with the load resistance R_{LOAD} from a stability perspective, the capacitor and resistor form a filter corner that can limit the bandwidth of the system. Therefore, for HART applications, use a bypass capacitance of 2 nF to 3 nF instead.

For applications with EMI and EMC concerns, use a bypass capacitor with sufficiently low ESR to decouple any ripple voltage from the V_{LOOP} supply. Otherwise, the ripple voltage couples onto the 4-mA to 20-mA current source, and appears as noise across R_{LOAD} after the current-to-voltage conversion.

7.2 Typical Application

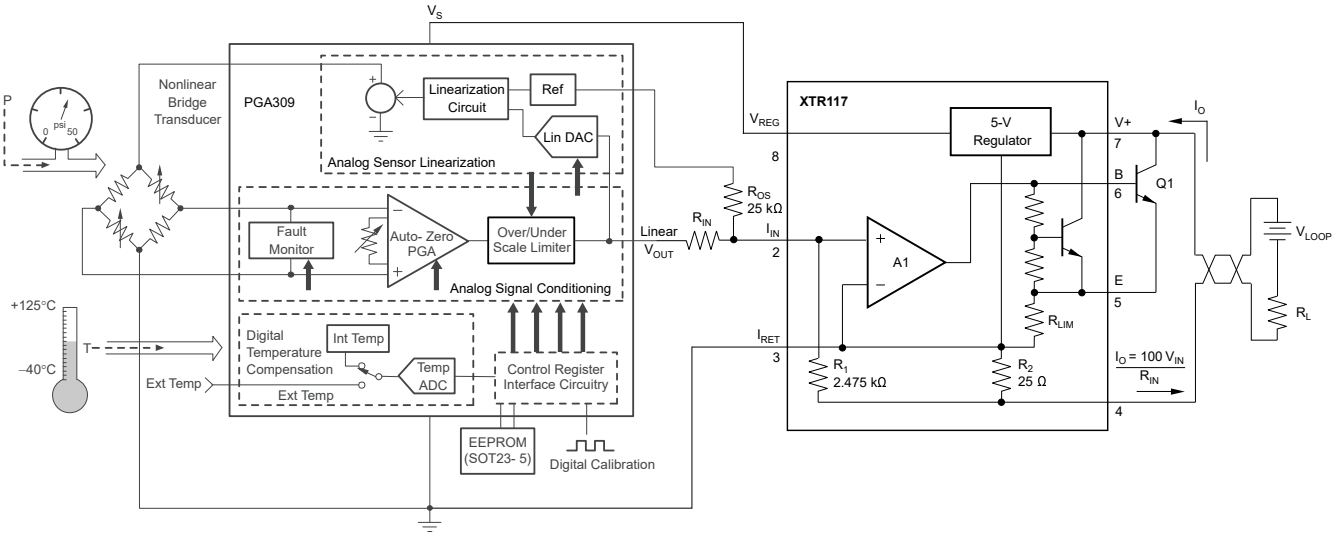


Figure 7-3. Complete 4 mA-20 mA Pressure Transducer Solution With PGA309 and XTR117

7.3 Layout

7.3.1 Layout Guidelines

The exposed leadframe die pad on the VSON packages can be soldered to a thermal pad on the PCB. A mechanical drawing showing an example layout is attached at the end of this data sheet. Refinements to this layout can be required based on assembly process requirements. Mechanical drawings located at the end of this data sheet list the physical dimensions for the package and pad. The five holes in the landing pattern are optional, and are intended for use with thermal vias that connect the leadframe die pad to the heat-sink area on the PCB.

Soldering the exposed pad significantly improves board-level reliability during temperature cycling, key push, package shear, and similar board-level tests. Even with applications that have low power dissipation, solder the exposed pad to the PCB to provide structural integrity and long-term stability.

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Special Function Amplifiers* Precision Labs video series on Current Loop Transmitters
- Texas Instruments, *TIPD126* Bridge Sensor Signal Conditioner with Current Loop Output and EMC Protection Reference Design with XTR117

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (May 2012) to Revision D (November 2023)	Page

- Updated the numbering format for tables, figures, and cross-references throughout the document. 1
- Changed maximum recommended loop supply voltage range from 40 V to 36 V in *Features*, *Specifications*, and throughout the document. 1
- Changed package name MSOP to VSSOP and DFN to VSON throughout the document. 1
- Changed Device Information table title to Package Information and updated contents. 1
- Added *Pin Configurations and Functions*, *ESD Ratings*, *Recommended Operating Conditions*, *Thermal Information*, *Detailed Description*, *Overview*, *Functional Block Diagram*, *Feature Description*, *Application and Implementation Typical Application*, *Device and Documentation Support*, *Related Documentation*, and *Mechanical, Packaging, and Orderable Information* sections. 2
- Changed absolute maximum loop supply voltage range from 50 V to 40 V in *Absolute Maximum Ratings* and throughout the document. 3
- Changed operating temperature minimum value from –55°C to –40°C in *Absolute Maximum Ratings* and *Electrical Characteristics*. 3
- Moved thermal resistance content from *Electrical Characteristics* to new *Thermal Information*. 3
- Changed thermal resistance from θ_{JA} = 150°C/W (MSOP) and 53 °C/W (DFN) to $R_{\theta JA}$ = 173.9 °C/W (VSSOP) and 60.7 °C/W (VSON), respectively. 3
- Changed bias current vs temperature from 150 pA/°C to 300 pA/°C in *Electrical Characteristics*. 4
- Changed V_{REG} vs output current parameter name to Voltage accuracy vs V_{REG} current, in *Electrical Characteristics*. 4
- Deleted redundant temperature range content already stated in the *Absolute Maximum Ratings* and new *Recommended Operating Conditions*. 4
- Updated *Typical Characteristics* title to remove typo. 5
- Changed Figure 7-1, *Basic Circuit Connections*. 6
- Changed suggested Zener diode part numbers in Figure 7-2, *Reverse Voltage Operation and Overvoltage Surge Protection*. 7
- Changed *External Transistor* applications information section to incorporate additional guidance regarding transistor power dissipation and thermal concerns. 9
- Added *Circuit Stability* section. 11

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
XTR117AIDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	Call TI | NIPDAUAG | NIPDAU	Level-3-260C-168 HR	-40 to 125	BOZ	Samples
XTR117AIDGKT	OBSOLETE	VSSOP	DGK	8		TBD	Call TI	Call TI	-40 to 125	BOZ	
XTR117AIDRBR	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	BOY	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

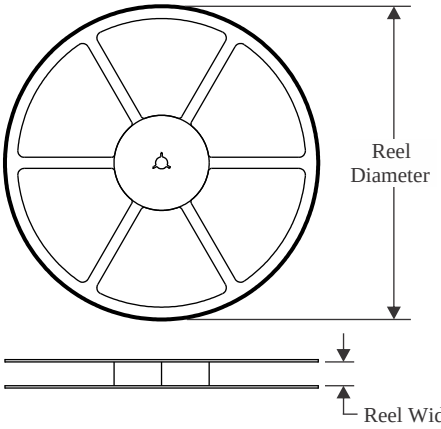
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

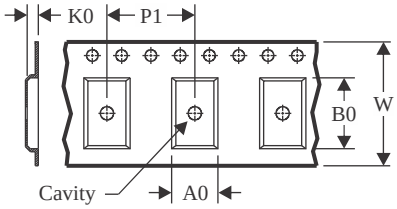
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

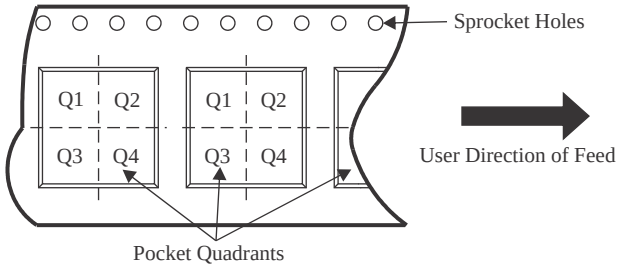


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

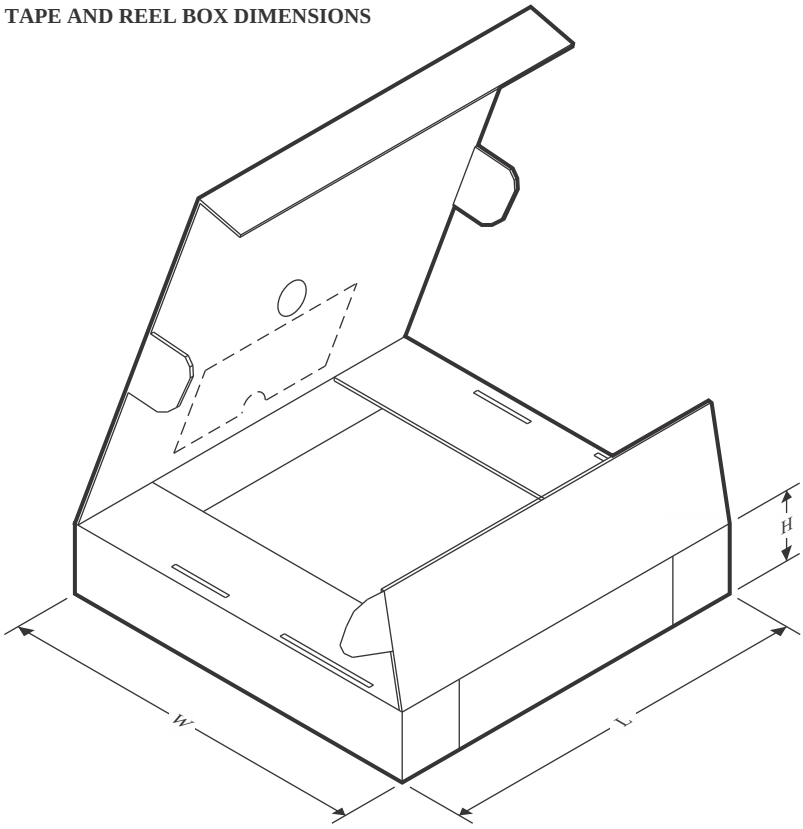
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
XTR117AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
XTR117AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
XTR117AIDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
XTR117AIDRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
XTR117AIDGKR	VSSOP	DGK	8	2500	356.0	356.0	35.0
XTR117AIDGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
XTR117AIDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
XTR117AIDRBR	SON	DRB	8	3000	356.0	356.0	35.0

GENERIC PACKAGE VIEW

DRB 8

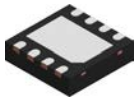
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4203482/L

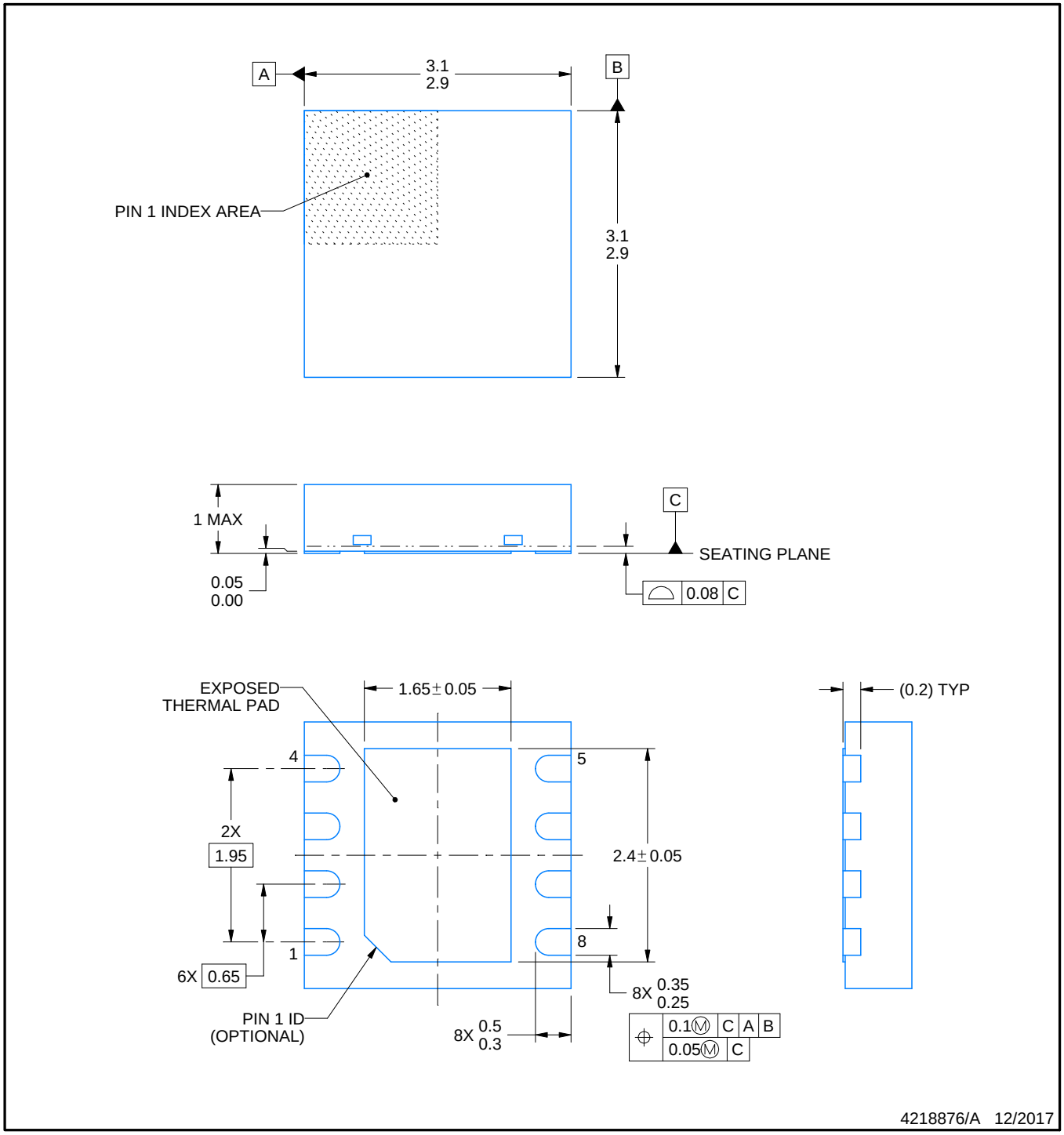
DRB0008B



PACKAGE OUTLINE

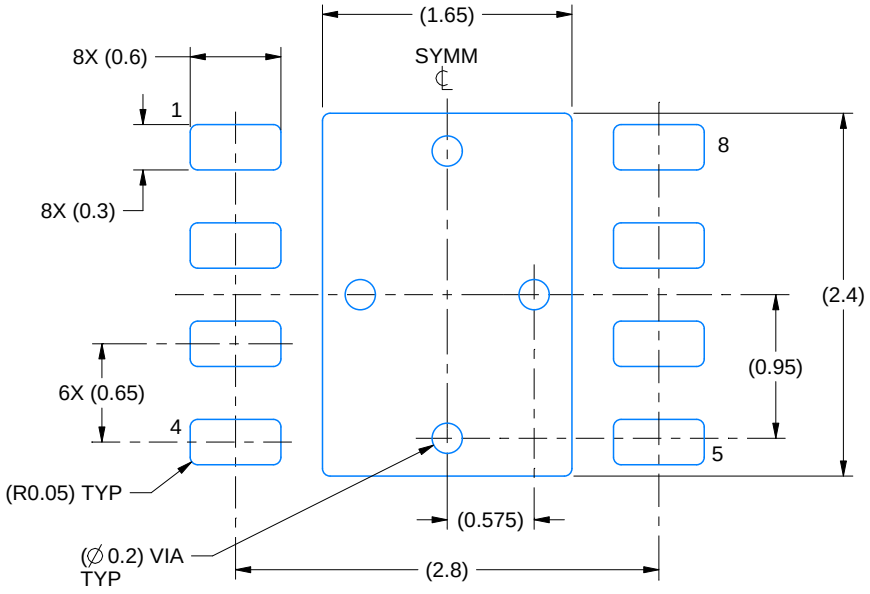
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

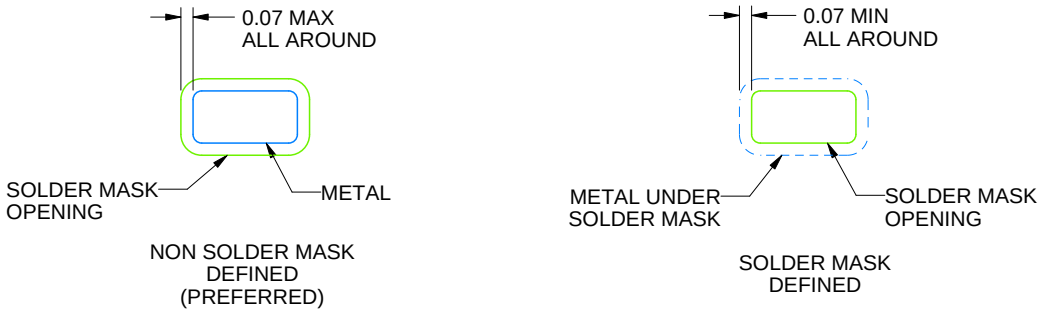


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

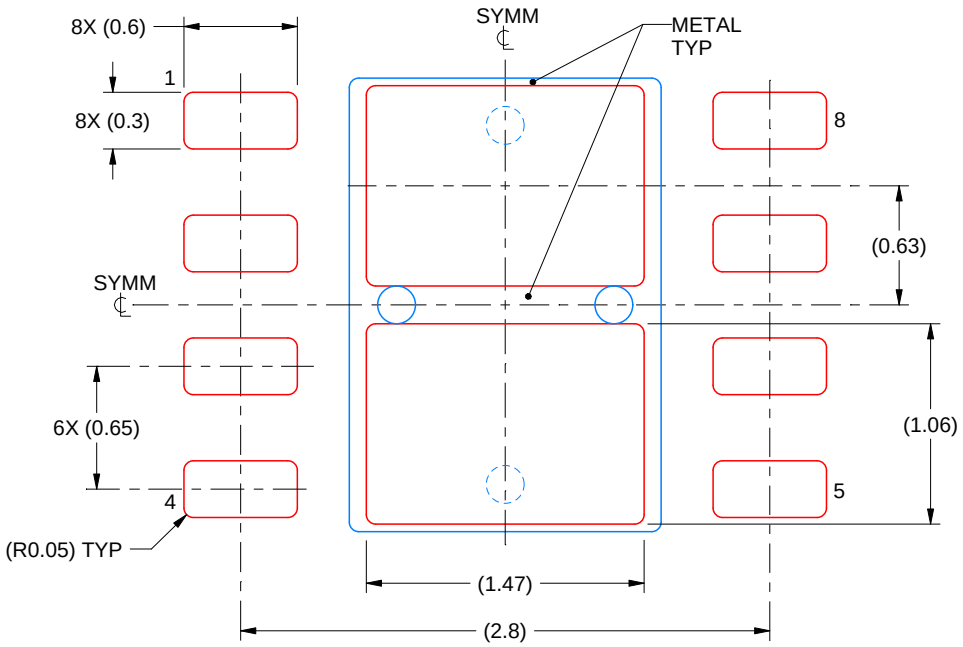


SOLDER MASK DETAILS

4218876/A 12/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
81% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218876/A 12/2017

NOTES: (continued)

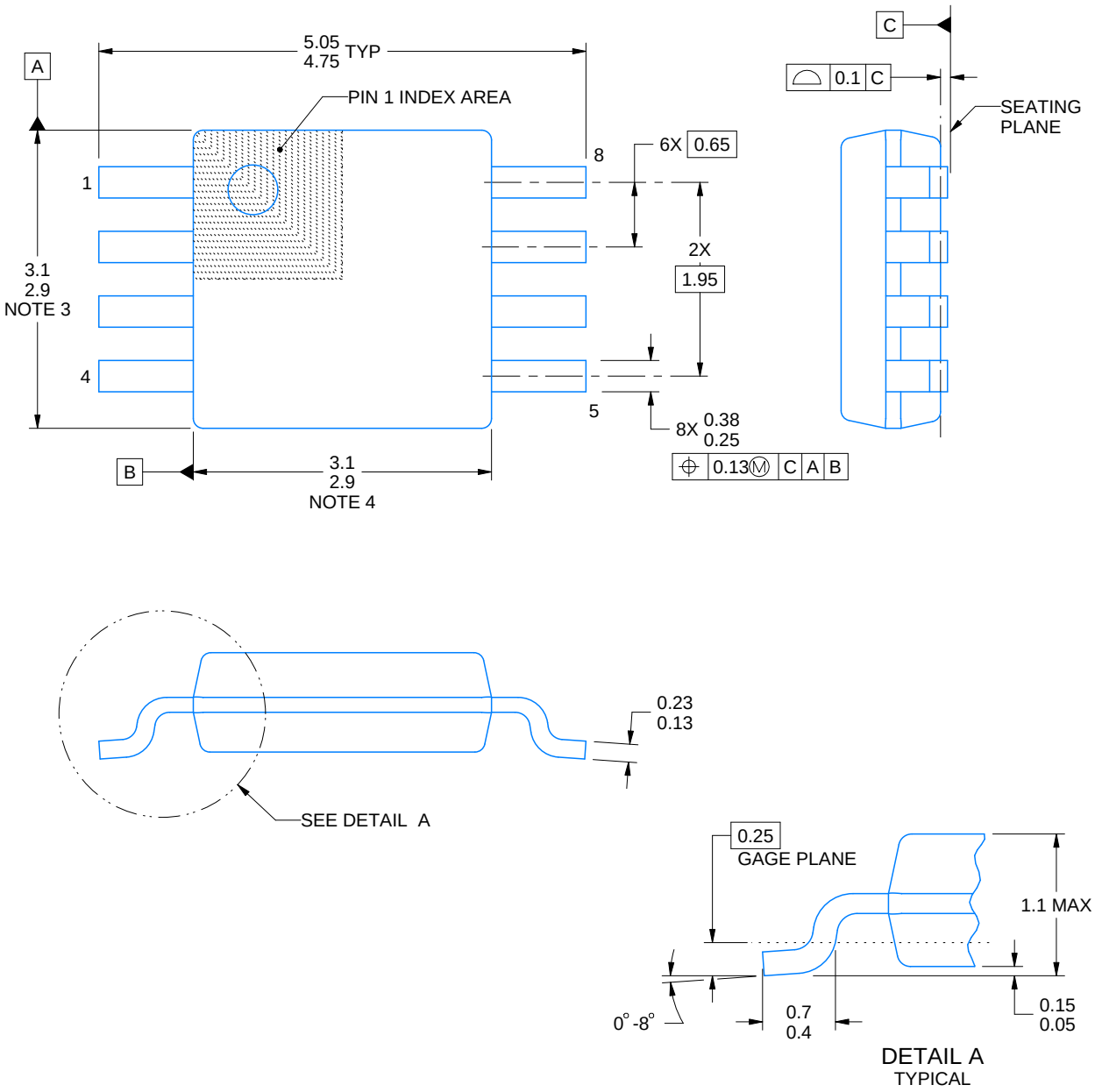
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

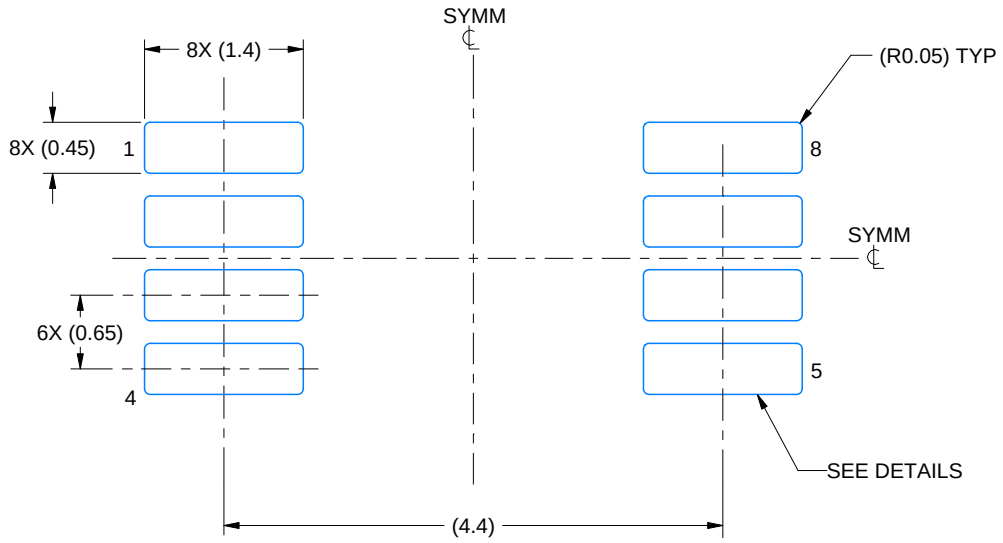
SMALL OUTLINE PACKAGE



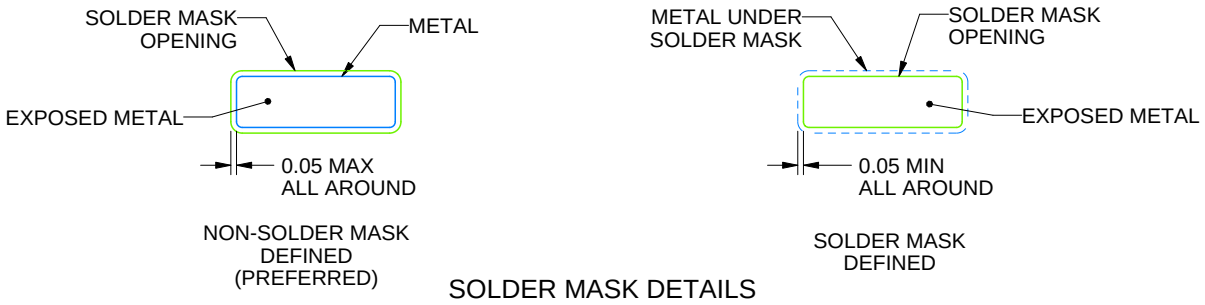
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

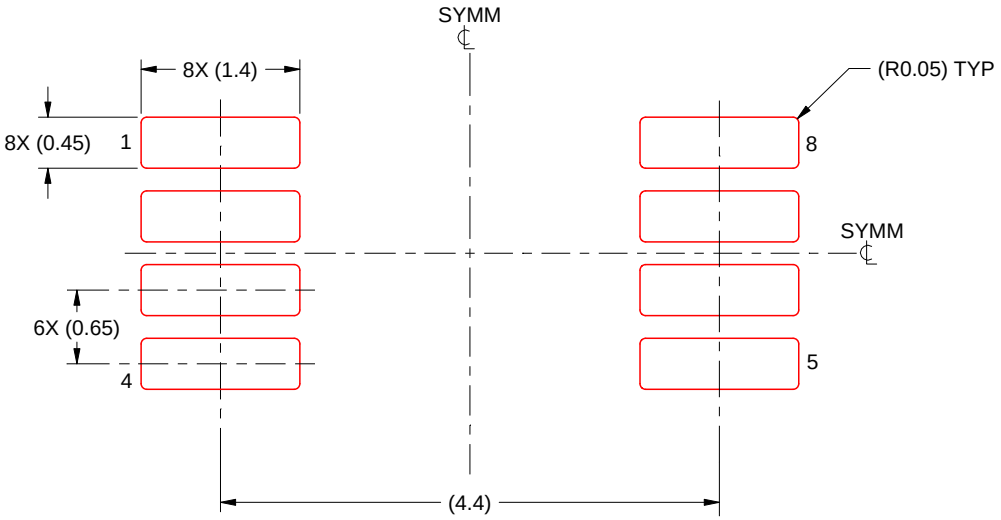


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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