IEEE 1149.1 Use in Design for Verification and Testability at Texas Instruments

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Abstract

Texas Instruments' hierarchical testability efforts have produced several new products aimed at standardization and cost reduction of IC and system test and debug[1]. These new products are compatible with the IEEE 1149.1 scan protocols and standards.[2,3] Included are ASIC cells, standard interface ICs, a bus master IC, a controller interface board for IBM compatibles, a high-speed scan interface, and software to control the scan bus. In this paper, I will introduce these products and explain a little about each. A detailed evaluation of some trade-offs to be looked at when using the IEEE 1149.1 standard for ASIC testability is also presented. Future products are currently under consideration.

Introduction

Let's take a quick look at design and manufacturing on the cutting edge. Your system is to perform supercomputing activities in engineering environments. To keep your boards from overheating, a complex liquid thermal transfer system is in place. Each board is a multilayer, controlled impedance, conformally coated unit comprised of ECL and BiCMOS fine-pitch surface-mounted components in the 10K to 100K gate range. Interconnects are kept to a minimum to improve system performance and reliability. Your task is to diagnose a fault in this system without totally disassembling it.

Not all system testability- and fault-diagnosis problems will be this complex. But each new design will have its own special set of constraints.

System densities are increasing and manufacturing processes are improving to the point where "in-circuit" probing of components is no longer feasible. Higher frequency circuits react with surrounding devices, dictating that they must be tested from within their functional environments. The complexity of today's electronics leaves little room for conventional ad-hoc testability features or design verification "hooks". The time for standardization of a test approach is now.

Inception

The Defense Systems and Equipment Group (DSEG) of Texas Instruments (TI) has always worked on the leading edge of many technologies. As circuit densities increased, and new manufacturing techniques permitted higher package counts, the need to integrate IC, board, and system test and verification circuitry within each of these respective levels of a design became necessary. From a system standpoint, it became obvious that whatever the method used to achieve this testability, a standard approach had to be taken. A method by which all levels of a system could be tested–from the pre-packaged bar to the system in field. The modular approach of this test and verification system became known as Hierarchical Testability.

Momentum

In 1986, Texas Instruments became an active member in the Joint Test Action Group (JTAG). This international organization, composed of semiconductor users and vendors from Europe and North America, had as its charter to define a testability strategy that would solve many of the problems design and manufacturing groups were facing. The solution of choice was boundary scan—a system whereby each I/O pin of a device may be observed or controlled via a four-wire scan interface and associated protocols. This system, now known as the JTAG or IEEE 1149.1 scan bus, enables large modules to be tested and evaluated from the IC-level up, while configured in their normal operating environments.

Solution

Texas Instruments has been a strong leader and proponent of a system solution to testability. TI's solution is an IEEE 1149.1-compatible one. But it goes further than simple

boundary scan. The System Controllability, Observability, and Partitioning Environment (SCOPE)[4] architecture and associated family of products has given the designer new tools to achieve the desired results of easy Design-For-Testability (DFT), as well as verification and debug features. Via the scan path, a virtual pattern generator/logic analyzer is created. This pattern generator/logic analyzer can, via the scan path, control and observe the inputs and outputs of a device.

To Probe Further

Parts of the Whole

There are many components that make up the SCOPE family of products. Each part works well within the architecture to help solve many design test and verification problems. Beginning with the most basic element, each component will be described and its many uses touched upon.

SCOPE Cells: The basic building block of the IEEE 1149.1 boundary scan architecture is the scan cell. The scan cell can control or observe a net in an ASIC. The version of this cell provided in TI SCOPE workstation libraries for use in ASIC Standard Cell and Gate Array designs is both compact and very versatile. By placing the scan cell between the I/O buffer and core logic, complete isolation of the device is achieved–a desirable goal for device and system testability.

There are currently 14 SCOPE Cells in the TI workstation libraries[5]. They range in functionality from simple controllability/observability cells to more complex cells used in Built-In Self-Test (BIST) applications. All cells offer the ability to control and observe a node at the same time. This feature can be used to the test engineer's advantage. He can execute internal device tests on the ASIC while performing exhaustive manufacturing tests on the board or system. This saves valuable test execution time. The advanced BIST functions built into some SCOPE Cells can be used to generate a pseudo-random set of patterns from each cell, or develop a signature within several cells based on the data observed by those cells. These are powerful functions and timesaving tools for the design/test engineer.

To enable communications to each ASIC via the four-wire IEEE 1149.1 interface, a Test Access Port (TAP) is included in the workstation libraries as a soft macro. TI's TAP (TS002), like all TAPs, is controlled by the TMS and TCK signals of the scan interface. The signals output by the TS002 are compatible with all the scan cells in the SCOPE library. Because the TS002 is a soft macro, any circuitry associated with an unused output can be removed.

To equip an ASIC with SCOPE, first complete the design of the chip's core application logic. Next, choose I/O buffers. The last step will be to add the SCOPE Cells to the design at each I/O pin along with the control circuitry necessary for IEEE 1149.1-compatible designs. The SCOPE circuitry should not interfere with the ASIC core logic design. Figure 1 illustrates the basic model for an ASIC design with SCOPE circuitry.

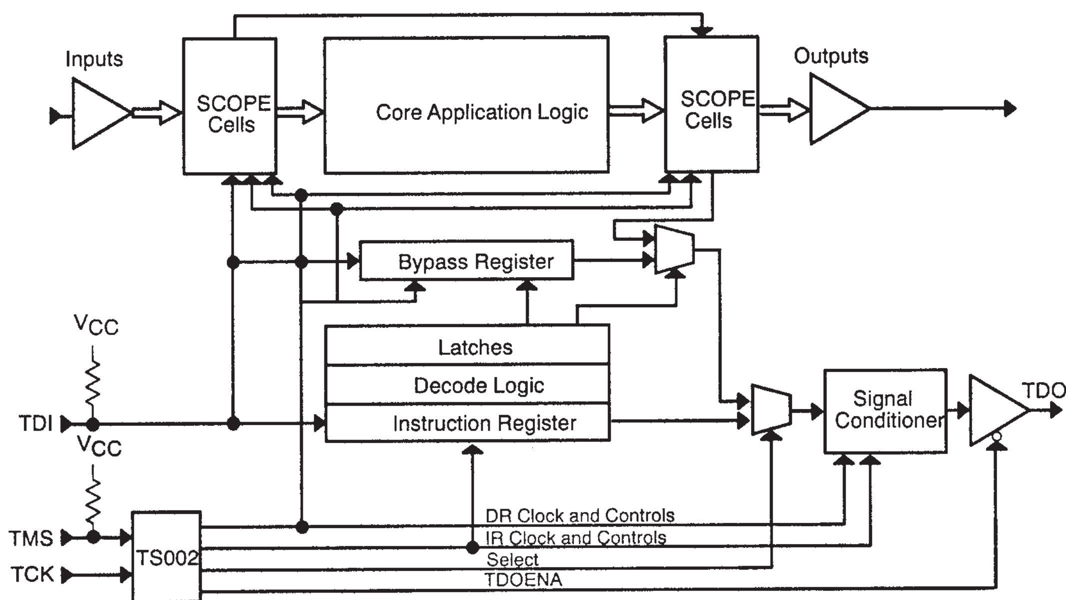

Figure 1. An ASIC with SCOPE

Several designs have been completed using the SCOPE libraries. Each works well and responds predictably to IEEE 1149.1 stimuli.

SCOPE Octal Test ICs: Many of today's designs still rely on standard octal bus interface devices for buffering signals between functional blocks of a system. Even in future designs, buffering signals at board edge connectors will continue to be a good idea to isolate complex devices from harmful off-board voltage spikes and to maintain backplane signal integrity. Typically, microprocessor and ASIC devices do not deliver the high drive necessary to push signals onto a backplane or into large blocks of RAM. Backplanes, microprocessors, and RAM have typically presented testability roadblocks to design engineers. With TI's SCOPE Octal Test ICs[6], a designer can incorporate boundary scan features (controllability/observability) into any or all octal devices on a board.

Currently, TI offers four SCOPE Octals: the 54/74BCT8244 octal buffer, 54/74BCT8245 octal transceiver, 54/74BCT8373 octal latch, and 54/74BCT8374 octal D flip-flop. All test features are accessed from the IEEE 1149.1 scan interface on each IC. In addition to controlling outputs and observing inputs of these devices, a pseudo-random pattern of data can be generated from the device outputs and a parallel signature analysis of the inputs can be made at the frequency of the Test Clock (TCK).

Future products are under consideration, but their availability will be driven by market demand and acceptance of the IEEE 1149.1 specification in general. Among the candidates for such new devices may include inverting bus functions, latches and flip-flops with alternate control inputs, and scannable field-programmable logic. Also being considered are bus monitoring devices that would enable observation of digital signals via the IEEE 1149.1 four-wire test bus.

SCOPE Test Bus Controller: To control the scan bus, a bus master IC has been developed. The SCOPE Test Bus Controller (TBC or 74ACT8990) receives commands and data from its host, and delivers IEEE 1149.1 control signals to the scan bus along with serial data. This device offloads the host from having to understand the scan protocol and speeds scan throughput. The TBC will be offered as part of TI's SCOPE family of components as an integral part of the testability and verification system. The TBC function may also be included in a future release of the ASIC workstation libraries as a soft macro or megacell.

Scan Controller Module: The TBC has been placed on the Scan Controller Module (SCM) card that fits inside an IBM PC/XT/AT compatible. The SCM is a half-length card composed of clock generation circuitry, discrete I/O circuitry, and the TBC device. With a cable connected between the SCM and the target system, fault diagnosis, system debug, and manufacturing verification can proceed.

High Speed Pod: Using TI's SCM, high speed scan operations can be implemented. Test clock speeds as high as 20 MHz have been tested with the TBC scanning to a demonstration system composed of four boards using prototype SCOPE Octal Test ICs. Depending on the system configuration, one or many high speed pods may be used to increase the distance of the target system from the test host.

Microprocessor Emulation: Texas Instruments TMS320C30 Digital Signal Processor[7] has built-in emulation functions accessible via a scan path. Plans for other application-specific microprocessors to incorporate emulation features accessible via an IEEE 1149.1 scan interface are in place. The advantages of this technology to the system, software, and design engineers are numerous. Specifically, the same four pins on a board edge connector used for testability purposes can be used for emulation purposes. One no longer has to remove the processor and insert a bulky emulator pod in its place for software development and system debug. All peripheral elements accessible by the processor are available through the emulator because the processor and emulator are one in the same. The customer no longer has to buy a separate emulator for each software development station. And, the emulator's speed is always that of the processor; no wait states need to be inserted.

ASSET Software: Tying the SCOPE hardware together is a software package tailored to serial scan test and debug strategies. The Advanced Support System for Emulation and Test (ASSET)[8] software development package was designed to help the engineer control test sequences through the scannable modules in the system without the tedium of handling scan protocols and keeping track of a dynamically changing scan path length.

The ASSET language is based on C++ functions and attributes but contains library functions tailored to scan test and debug scenarios. Included in the ASSET function libraries is a means to collect and view nodes sampled by the SCOPE Octals and scannable ASICs in a display format similar to a logic analyzer user interface. ASSET can be programmed to understand the architecture and testability features of an ASIC. It can take functional test patterns developed for an ASIC and scan them into the device to test it while the device is in the system. With the proper test program, faults from manufacturing or from environmental stress can be diagnosed.

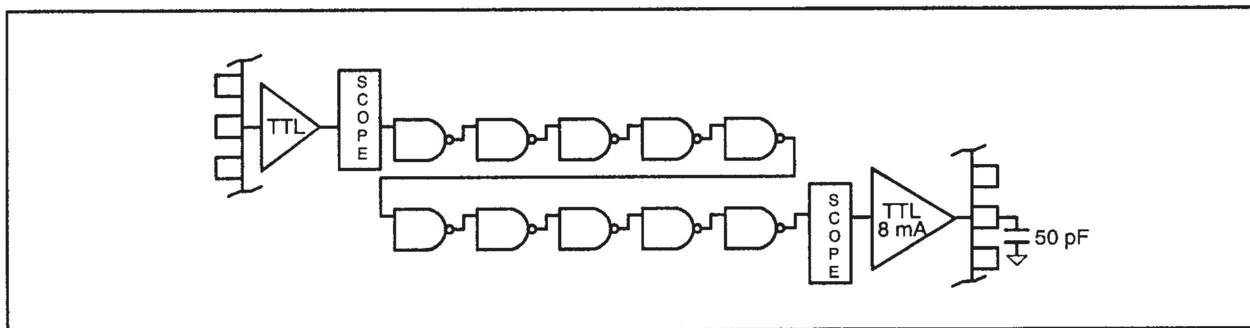

Figure 2. Delay Path with SCOPE Cells

ASSET is a modular and hierarchical package, and its routines can be called from other software packages. An interesting application could be written to extract data from design and manufacturing data bases of a particular system, and generate a test for all components in that system, as well as interconnections between components.

The ASIC Application

After completing several designs, some useful statistics can be shown.

Gate Overhead

To roughly calculate the number of extra gates necessary to add the SCOPE architecture to a 1-µm Standard Cell design using TI's TSC500 library components,[9] use the following formula:

$$G = IO \times 14.5 + IB \times 11 + TAP + N$$

where G = # gates to add
IO = # unidirectional I/Os
IB = # instruction register bits
TAP = # gates in TS002 Cell
N = variable from 50 to 300

This scenario assumes that an IEEE 1149.1-compatible design is to be achieved. Texas Instruments has standardized the Instruction Register length to be 8 bits. For IEEE 1149.1-only designs, only 2 bits are required. The TAP with all its outputs is 183 gates. The gate count drops to 154 after removing some specialized outputs. To complete the SCOPE architecture, an instruction decode circuit with latched outputs needs to be added along with TDO (Test Data Output) signal muxing and conditioning circuitry. The variable N in the equation accounts for this circuitry.

Speed Penalty

Adding the SCOPE circuitry to an ASIC design also exacts a speed penalty. Consider a SCOPE Cell placed between an input buffer and a 2-input NAND gate, or between a 2-input NAND gate and an output buffer: for all environmental conditions, one can say that in general, a 40 percent degradation in speed will be exacted on that net due to the inclusion of a 2:1 mux in the data path. For example, if the delay associated with a net driven by an input buffer to a 2-input NAND gate is 1.6 nanoseconds (typical for TI's 1-µm Standard Cell), then, after adding a SCOPE Cell to the net, the delay between the input buffer and NAND gate would typically be about 2.3 nanoseconds.

To further illustrate the small speed degradation of a device using the SCOPE architecture, let us assume an ASIC device with SCOPE cells is designed as illustrated in Figure 2.

Without the SCOPE Cells, the typical device propagation delay would be 8.42 nanoseconds. Adding the SCOPE Cells at the input and output buffers increases the typical propagation delay to 10.09 nanoseconds. Adding the SCOPE Cells to the boundary added only 1.67 nanoseconds to the typical device propagation delay. The typical propagation delay through a SCOPE Cell is 0.7 nanoseconds.

Internal Scan

Partitioning: Because the SCOPE Cell component is transparent in nature when the device is in a normal functional mode, SCOPE Cells can be used internal to the ASIC to control and observe internal nodes of the circuit. The IEEE 1149.1 architecture allows for as many user data paths as a designer sees fit to include in the design. These internal paths may be used to surround and isolate an internal function in much the same manner as boundary scan is used to isolate the ASIC itself from the rest of the system for testing, fault diagnostic, and debugging purposes.

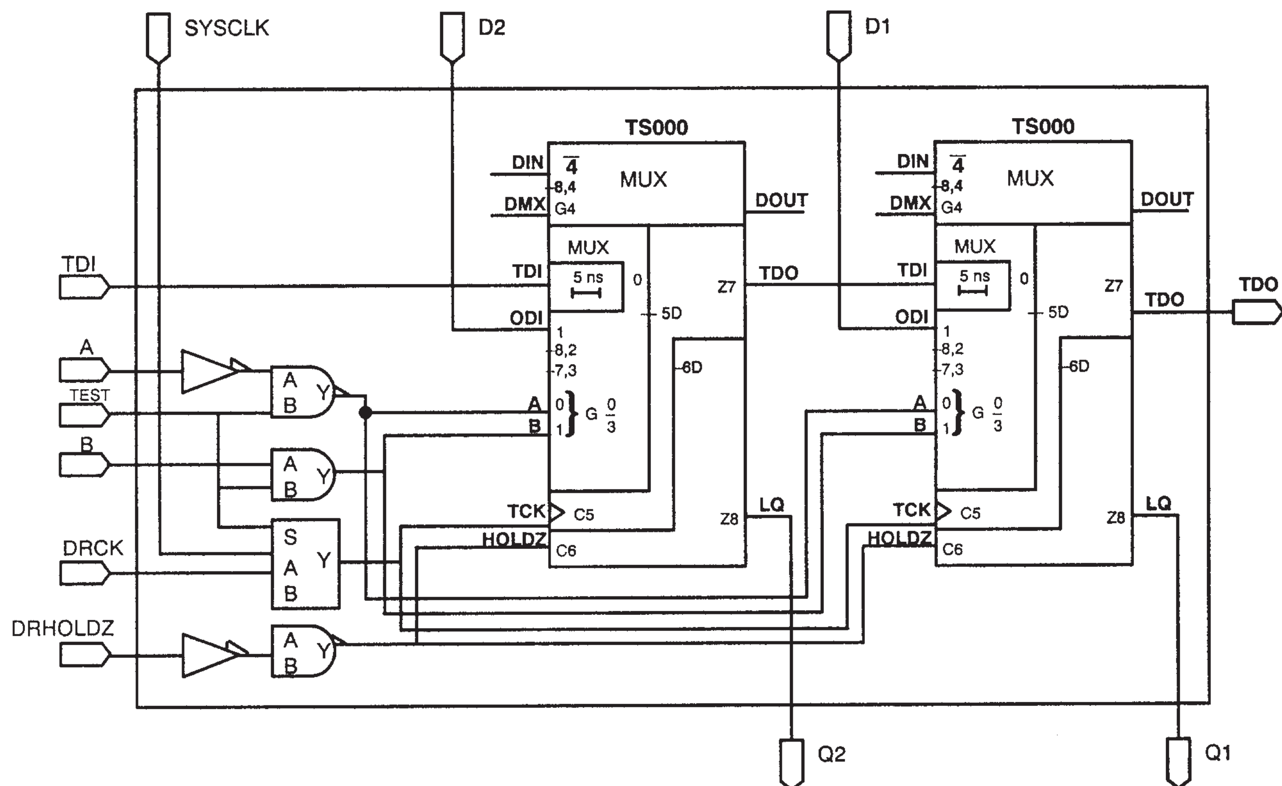

Figure 3. D-Flip-Flops

Scannable Register: The SCOPE Base Cell (TS000) may be used as a scannable flip-flop. This is a useful application of the SCOPE Cell to gain the controllability/observability functions in the core-application sequential logic. Figure 3 shows a typical application of this methodology.

The TEST signal comes from the test instruction decode logic, or an IEEE 1149.1 User Data Register. It controls the mode of the flip-flops. Signals on each side of the D-Flip-Flops box come from SCOPE test logic circuitry. Signals above and below the box represent normal function inputs and outputs.

Conclusions

The SCOPE boundary scan architecture can be used in conjunction with the post-packaging test vector set to perform a complete, high-confidence test of the ASIC. By also incorporating internal scan-between functional circuit blocks, higher controllability/observability partitions can result in better fault coverage, smaller vector sets, and shorter test times. In addition, these scan paths may be used to emulate peripheral functions to aid in the system debugging and verification processes.

After SCOPEing a system, each scannable node can become a virtual logic analyzer probe or pattern generator clip. With ASSET software controlling your system, the design, manufacturing, test, field service, and software engineers can leverage their own testing, diagnostic, and development needs from the same circuitry–all without physically touching the system.

Future developments within Texas Instruments and other industry leaders should produce new and valuable additions to the IEEE 1149.1-compatible product lines. As interest and knowledge increases, integration of this technology will become a matter of course for IC, board, and system vendors.

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