

Migrating from the MSP430F5xx and MSP430F6xx Family to the MSP430FR58xx/FR59xx/68xx/69xx Family

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ABSTRACT

This application report helps enable easy migration from MSP430F5xx and MSP430F6xx flash-based MCUs to the MSP430FR58xx/FR59xx/68xx/69xx FRAM-based MCUs. For the migration guide to MSP430FR57xx, see [Migrating From the MSP430F2xx Family to the MSP430FR57xx Family](#). It covers programming, system, and peripheral considerations when migrating firmware. The intent is to highlight differences between the two families; for more information on the use of the MSP430FR58xx/FR59xx/68xx/69xx features, see the [MSP430FR58xx, MSP430FR59xx, MSP430FR68xx, and MSP430FR69xx Family User's Guide](#).

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1 Introduction

The purpose of this application report is to highlight the key differences between the MSP430F5xx and MSP430F6xx family and the MSP430FR58xx/FR59xx/68xx/69xx family to ensure a smoother migration.

This application report is divided into the following sections:

- System-level considerations such as power management
- Changes when handling nonvolatile memory
- Peripheral modifications

With respect to the instruction set, the MSP430FR58xx/FR59xx/68xx/69xx family is fully backward code compatible with all other MSP430™ microcontroller families. Any code migration is therefore impacted only by register or peripheral feature changes; the instruction set remains the same.

NOTE: For the purpose of this application report, the term *F5xx* indicates the MSP430F5xx and MSP430F6xx family, and the term *FR59xx* indicates the MSP430FR58xx/FR59xx/68xx/69xx family.

2 In-System Programming of Nonvolatile Memory

2.1 Ferroelectric RAM (FRAM) Overview

Using FRAM nonvolatile memory is very similar to using static RAM (SRAM). FRAM's first introduction as an embedded memory in a general-purpose ultra-low power MCU was on Texas Instruments 16-bit MSP430 product line, the MSP430FR57xx family.

Some of the key attributes of FRAM are:

- FRAM is nonvolatile; that is, it retains its contents on loss of power.
- The embedded FRAM on MSP430 devices can be accessed (read or write) at up to a maximum speed of 8 MHz. Above 8 MHz, wait states are used when accessing FRAM.
- Writing to FRAM and reading from FRAM requires no setup or preparation such as pre-erase before write or unlocking of control registers (unless the MPU is used to protect the FRAM against write access).
- FRAM is not segmented and each bit is individually erasable, writable, and addressable.
- FRAM does not require an erase before a write.
- FRAM write accesses are low power, because writing to FRAM does not require a charge pump.
- FRAM writes can be performed across the full supply voltage range of the device.
- FRAM write speeds can reach up to 8 MBps with a typical write speed of approximately 2 MBps. The high speed of writes is inherent to the technology and is aided by the elimination of the erase bottleneck that is prevalent in other nonvolatile memory technologies [1]. In comparison, typical MSP430 flash write speed including the erase time is approximately 14 kBps [6].

2.2 FRAM Cell

A single FRAM cell can be considered a dipole capacitor that consists of a film of ferroelectric material (ferroelectric crystal) between two electrode plates. Storing a 1 or 0 (writing to FRAM) simply requires polarizing the crystal in a specific direction using an electric field. This makes FRAM very fast, easy to write to, and capable of meeting high endurance requirements. Reading from FRAM requires applying an electric field across the capacitor similar to a write. Depending on the state of the crystal, it may be repolarized, thereby emitting a large induced charge. This charge is then compared to a known reference to estimate the state of the crystal. The stored data bit 1 or 0 is inferred from the induced charge. In the process of reading the data, the crystal that is polarized in the direction of the applied field loses its current state. Hence, every read is accompanied by a write-back to restore the state of the memory location. With TI's MSP430 FRAM MCUs, this is inherent to the FRAM implementation and is completely transparent to

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the application. The write-back mechanism is also protected from power loss and is ensured to complete safely under all power-fail events. The FR59xx power management system achieves this by isolating the FRAM power rails from the device supply rails in the event of a power loss. The FRAM power circuitry also uses built-in low-dropout regulator (LDO) and a capacitor that store sufficient charge to complete the current write-back in the event of a power loss.

2.3 Protecting FRAM Using the Memory Protection Unit (MPU)

Because FRAM is very easy to reprogram, it also makes it easy for erroneous code execution to unintentionally overwrite application code, just as it could if executing from RAM. To safeguard against erroneous overwriting of FRAM, a Memory Protection Unit (MPU) is provided. It is recommended to set up boundaries between code and data memory to increase code security and protect against accidental writes or erasures. The MPU allows users to separate blocks of FRAM and assign unique privileges to each block based on the application's requirement. For example, if a memory block is assigned read-only status, any write access to that block is prevented, and an error is flagged. This is useful for storing constant data or application code that is not expected to change over the device lifetime. Code examples that show how to configure the MPU are provided in the [MSP430FR5969 product folder](#) and are also included in [MSP430Ware™ software](#).

2.3.1 Dynamically Partitioning FRAM

One of the more unique properties of FRAM is that, when it is used in conjunction with the MPU, it provides the user the ability to dynamically shift the boundaries of code, data, and constant memory. This is done by setting up the MPU to establish read only (constant), read-write only (variable), and read-execute only (code) segments. The resolution of each block is fixed to 4KB blocks [2].

See [MSP430 FRAM Technology – How To and Best Practices](#) on how to partition and enable the MPU.

2.4 FRAM Memory Wait States

The maximum FRAM memory access speed is 8 MHz. If the MCLK is operating faster than 8 MHz, wait states are required to ensure reliable FRAM access. When using $MCLK \geq 8$ MHz, configure the FRAM wait states in software before configuring the MCLK frequency.

- Configure the appropriate wait states.

```
FRCTL0 = FRCTLPW | NWAITS_x
```

- Configure $MCLK \geq 8$ MHz.

For more information, see the *Wait State Control* section of the *FRAM Controller (FRCTRL)* chapter in the [MSP430FR58xx, MSP430FR59xx, MSP430FR68xx, and MSP430FR69xx Family User's Guide](#).

2.5 Bootloader (BSL)

The BSL is software that is used to reprogram the MCU; for example, during field firmware updates. On the F5xx family of devices, the default BSL uses the hardware UART or the USB module (on devices with USB). The BSL software is located in flash memory from location 0x1000 to 0x17FF. This flash-based BSL is erasable and the flash memory can be reused for the user application.

Having a flash-based BSL also provides the user the option to customize the BSL by adding or removing features.

In the FR59xx family, the BSL software is located in ROM. It occupies the same address range as the flash BSL (that is, 0x1000 to 0x17FF) but it cannot be erased or reprogrammed, because it resides in ROM.

The FR59xx BSL hardware interface is implemented using the UART protocol. Device variants that use an I²C hardware interface for the BSL are also available. However, for a given device variant, only the factory-configured interface can be used, and it cannot be changed as in the F5xx family.

The BSL can be disabled by programming a signature to the BSL signature location. Details on the BSL signature location and how to program the signature are available in the *SYS* chapter in the [MSP430FR58xx, MSP430FR59xx, MSP430FR68xx, and MSP430FR69xx Family User's Guide](#). The procedure is similar to the one used for F5xx devices.

2.6 JTAG and Security

On the F5xx devices, the JTAG mechanism is disabled by programming the electronic fuse at the addresses 0x17FC to 0x17FF. This is still possible on the FR59xx devices by accessing the JTAG signature locations at 0xFF80 and 0xFF82. The procedure is described in detail in the *SYS* chapter in the [MSP430FR58xx, MSP430FR59xx, MSP430FR68xx, and MSP430FR69xx Family User's Guide](#).

The FR59xx devices have an additional feature that allows the user to lock the JTAG with a password. The password itself is located at FRAM location 0xFF88 and can be up to 4 words in length. To access JTAG, the tool chain must first provide the password, and then the device grants JTAG access. Any access with an incorrect password prevents JTAG access. When a password is verified, complete JTAG access is possible until the next BOR event.

When using the IAR Embedded Workbench™ IDE, the option for providing the JTAG password is described in the *IAR Embedded Workbench C-SPY Debugging Guide for MSP430 Microcontroller Family*, which is available in the IAR installation directory under \430\doc.

When using the Code Composer Studio IDE V5.2 or higher, this option is available by editing the MSP430Fxxx.CCXML file under Target Configurations in the Advanced Setup Section, Advanced target Configuration. The procedure is documented in the [Code Composer Studio User's Guide for MSP430](#).

2.7 Production Programming

MSP-GANG430 does not support FR69xx. The [MSP-GANG](#) production programmer supersedes the MSP-GANG430 and supports FR69xx.

3 System Level Considerations

3.1 Power Management Module (PMM)

The PMM manages all functions related to the core voltage and its supervision. Its primary functions are first, to generate a supply voltage for the core logic, and second, to provide several mechanisms for the supervision of both the voltage supplied to the device (DV_{CC}) and the voltage generated for the core (V_{CORE}).

The power management module (PMM) of the F5xx family shares some features with the FR59xx family:

- Both families use a split supply. The high side or supply side on the DVCC pin is fed to an internal low-dropout voltage regulator that supplies the CPU, memories, and digital modules. The AVCC pin supplies the analog modules.
- The supervision (SVS) for the high side is integrated in the PMM.

However there are some significant improvements in the FR59xx PMM:

- The FR59xx core side supports only a single core voltage; that is, the core voltage is not programmable. The reason for this change is to reduce complexity for the user. Also, the highly flexible clock system allows for the maximum system frequency (16 MHz) to be used at the lowest system voltage of 1.8 V. This removes the need for programmable core voltages, and a single core voltage is maintained across the supply range of 1.8 V to 3.6 V for all operating frequencies.
- The external low-side core capacitance in the F5xx devices is no longer required. Instead, the FR59xx devices integrate the core capacitor in the device.
- Because the core voltage does not need to be buffered by an external capacitance, the V_{CORE} voltage is not available externally on a pin.
- The core voltage is monitored and maintained internally, and the user is not required to set up the core side (low side) monitor (SVML) and supervisor (SVSL).
- The SVS high side (SVSH) is highly simplified. It is on by default at power-up and stays on in the active, LPM0, LPM1, and LPM2 modes. It can be turned off in LPM3, LPM4, and LPMx.5 modes, if required.
- The SVS threshold tracks directly with the device minimum supply of 1.8 V, and there is no need to program SVS high side levels as in the F5xx family.
- A useful feature in the FR59xx family is the ability to trigger an NMI when the supply falls below the SVS level. This is useful, for example, if the application is powered by a dying battery; an interrupt can

be used to configure ports to consume the least power and set the device in LPM3.5, consuming approximately 500 nA to maximize battery life while preserving RTC for as long as possible.

3.2 Clock System (CS)

The FR59xx clock system uses an internal digitally controlled oscillator (DCO) to provide precalibrated frequencies.

A significant difference with the FR59xx DCO is that it can be configured only to the factory-provided calibrated frequencies and does not provide all of the in-between frequency steps that the DCO + FLL based system in the F5xx family allowed.

While the FR59xx can source MCLK at 16 MHz, FRAM access is limited to 8 MHz by the FRAM controller and wait-states are required. For configuring wait-states, see [Section 2.4](#). Code execution from RAM, accesses to peripherals, and DMA accesses between peripherals and RAM can be carried out at 16 MHz.

Note that, due to the architectural changes implemented to lower power in standby modes, ACLK is restricted to low-frequency clock sources (less than 50 kHz) in the FR59xx family. For sourcing high-frequency clock sources, SMCLK or MCLK can be used instead.

In regards to accuracy, the DCO in the FR59xx family provides a fixed accuracy for the precalibrated frequencies as specified in the device data sheet. This is typically $\pm 2\%$ for a limited temperature range and $\pm 3.5\%$ across the temperature range of the device.

In comparison, the accuracy of a DCO+FLL based system, as in the F5xx family, is dependent on the accuracy of the FLL reference source. For example, if REFO is used as the reference for the FLL, then the output of the DCO depends on the accuracy of the REFO. Now consider an application using a high-frequency highly accurate crystal—this, in turn, improves the accuracy of the FLL-based system.

[Table 1](#) lists some important differences in the clock systems between the families.

EnergyTrace++™ Technology can be used to verify or diagnose if the clock sources are turned on or off as expected during LPMx. To learn more about EnergyTrace++ Technology, see [MSP430 Advanced Power Optimizations: ULP Advisor SW and EnergyTrace Technology](#).

Table 1. Comparison of Clock Systems

Parameter	FR59xx	F5xx
Maximum f_{SYSTEM}	16 MHz	25 MHz
DCO range	Calibrated frequencies only	0.06 MHz to 135 MHz
Production calibrated frequencies	1 MHz, 5.33 MHz, 6.67 MHz, 8 MHz, 16 MHz, 20 MHz, and 24 MHz	None
Clock sources for ACLK	LFXTCLK, VLOCLK, LFMODCLK	Any system clock
LFMODCLK (MODOSC / 128)	Available	Not Available
REFO	Not available	Available
External crystal fail-safe options	LFXT: LFMODCLK HFXT: MODCLK	LFXT: REFO HFXT: DCOCLK
Registers	CSCTL0 through CSCTL6	UCSCTL0 through UCSCTL8
VLO control	Available through VLOFF bit	Not available
Internal load capacitors for XT1 oscillator	Not available	Available

3.3 Operating Modes, Wakeup, and Reset

Table 2 compares the various operating modes available in the two families and the wake-up times from LPMs.

Table 2. Comparison of Operating Modes and Wake-up Times

Parameter	FR59xx	F5xx
LPM0, LPM1, LPM2, LPM3, LPM4	Available	Available
LPM3.5	Available	Available on some devices
LPM4.5	Available	Available on some devices
Wake-up time from LPM0	$1.5 / f_{\text{DCO}} \approx 1.5 \mu\text{s}$ ($f_{\text{DCO}} = 1 \text{ MHz}$)	5 μs (high-performance mode) 150 μs (normal mode)
Wake-up time from LPM1 or LPM2 ⁽¹⁾	6 μs	5 μs (high-performance mode) 150 μs (normal mode)
Wake-up time from LPM3 or LPM4 ⁽¹⁾	7 μs	5 μs (high-performance mode) 150 μs (normal mode)
Wake-up time from LPM3.5 ⁽¹⁾	250 μs	2 ms
Wake-up time from BOR event ⁽¹⁾	1 ms	2 ms

⁽¹⁾ The values in this table are approximations. See the device-specific data sheet for the exact values for each device.

The code flow for entry into LPM0 through LPM4 and the LPMx.5 modes remains the same in the FR59xx family as in the F5xx family.

Similar to the F5xx family, the FR59xx can initiate all levels of reset in software.

The TLV or device descriptor table in the FR59xx family includes an extra field to store a random number seed that is generated on a per device basis at production. It is useful for encryption and decryption algorithms.

3.4 Using LPM3.5 on the FR59xx

While LPM3.5 mode is available on certain F5xx devices, it is important to note that FRAM brings added flexibility to this mode. Because FRAM is preserved when the core regulator is turned off and the use of FRAM is similar to RAM, the state of the application that is preserved in the form of application variables can be maintained or backed up in FRAM, which allows the application to start up more quickly and initialize fewer variables from an LPM3.5 wakeup event.

3.5 FRAM Controller

3.5.1 Flash and FRAM Overview Comparison

The F5xx family flash controller is replaced by the FRAM controller in the FR59xx family.

The most significant differences between using FRAM and Flash pertain to (1) timing and (2) power requirements (see Table 3).

Table 3. Comparison of Flash and FRAM on MSP430 MCUs

Parameter	FRAM (FR5969) ⁽¹⁾	Flash (F5438A) ⁽¹⁾
Program time for byte or word (max)	120 ns	85 μs (approximately)
Erase time for segment (max)	Not applicable (pre-erase not required)	18 ms
Supply current during program (max)	No extra current during write (included in active power specification)	5 mA
Supply current during erase (max)	Not applicable (pre-erase not required)	2 mA
Nonvolatile memory maximum read frequency	8 MHz	25 MHz

⁽¹⁾ The values in this table are approximations. See the device-specific data sheet for the exact values for each device.

3.5.2 Cache Architecture

The FRAM controller uses a 2-way associative cache that has a 64-bit line size. The cache stores prefetched instructions. The function of the FRAM controller is to prefetch four instruction words depending on the current PC location. The actual execution of these instructions is carried out in the cache. When the end of the cache buffer is reached, the FRAM controller preserves the four current words in the same cache line and fetches the next four words. If at the end of a 2-way associative cache line, a code discontinuity is encountered, the cache is refreshed, and the following four words of instruction are retrieved from FRAM. However, if at the end of the cache, the application code loops back to a location already present in the cache, the relevant instruction is simply executed directly from the cache instead of fetching the code from FRAM again.

Note that only FRAM accesses are subject to the 8-MHz access limitation. When executing from cache, a system clock of up to 16-MHz can be used. Thus the cache is useful in (1) overcoming the 8-MHz limitation and increasing the average system throughput and (2) reducing overall active power by ensuring that most instructions are executed from it.

The cached execution of instructions in the FR59xx family is different from the F5xx family where instructions are pre-fetched and placed in a 32-bit pipeline. This affects the relationship between MCLK and instruction execution. For example, on an F5xx device with MCLK = 16 MHz, eight 2-cycle instructions can be executed in 16 clocks. For the FR59xx family, this relationship is application dependent. The 1:1 relationship holds true only up to MCLK = 8 MHz. For MCLK > 8 MHz, the number of inserted wait states (directly proportional to how many times FRAM is accessed) determines the MCLK:instruction-execution ratio.

To provide another application example, with MCLK = 16 MHz, a JMP \$ instruction (single cycle) is executed at the same rate in both F5xx and FR59xx families. This is because the FR59xx fetches this instruction and stores it in cache where it can be executed at the maximum MCLK speed. However, a loop that has more than 8 instruction words would require accessing the FRAM every time a cache refresh is needed. These FRAM accesses take place at MCLK/2 (that is, 8 MHz) thereby reducing the overall throughput of the system when compared to an F5xx device.

3.6 RAM Controller (RAMCTL)

The RCRSyOFF bit in the RCCTL0 register for the F5/6xx MCUs is now called RCRSyOFF0, where y is the sector number.

The RCCTL0 register also has fewer sectors (up to 4 sectors for FR58xx, FR59xx, FR68xx and FR69xx MCUs), whereas the F5/6x device family has up to 8 sectors.

The FR5962/4 and FR5992/4 MCUs have 8KB of SRAM. The SRAM is made up of three sectors. Sector 0 = 2KB, Sector 1 = 2KB, and Sector 2 = 4KB. Each sector can be individually powered down in LPM3 and LPM4 to save leakage. Note that data is lost when sectors are powered down in LPM3 and LPM4.

The 4KB of Sector 2 is shared with the Low-Energy Accelerator (LEA) peripheral when the LEA module is activated. When the LEA module is not activated, Sector 2 SRAM can be used normally. See device-specific data sheets for more information.

3.7 Summary of Important Device Specifications

Table 4 summarizes the most important differences in the device-level specifications between these families.

Table 4. Summary of Device Specifications

Parameter	FR59xx	F5xx
Supply voltage range	1.8 V to 3.6 V ⁽¹⁾	1.8 V to 3.6 V
Maximum system frequency, f_{SYSTEM}	16 MHz	25 MHz 20 MHz on some devices
Maximum ACLK frequency	50 kHz	f_{SYSTEM}
Analog supply voltage for ADC operation	1.8 V to 3.6 V	2.2 V to 3.6 V

⁽¹⁾ The minimum operating voltage is dependent on the SVSH voltage levels.

Note that the most significant impact that migrating to an FR59xx device brings to your system is in terms of the power consumption. The FR59xx demonstrates significant improvements in active and standby power, both typical and across the voltage and temperature range of the device. The same is also true for peripherals in the FR59xx family, such as the ADC12_B, which show significant power improvements when compared to their F5xx counterparts. The device-specific data sheets can be used to obtain a detailed listing of the power consumption for each peripheral and of the device in active and standby modes.

4 Peripheral Considerations

Some of the peripherals in the FR59xx family have new features or existing features that are implemented differently. This section highlights the peripheral differences.

4.1 Digital Input/Output

The main differences in the general-purpose I/O (GPIO) pins are:

- P3 and P4 ports are also interruptible (this is available in some devices in the F5xx family).
- Peripheral function select uses two registers PxSEL0 and PxSEL1. These two registers can be set or cleared simultaneously using the PxSELC register to avoid intermediate configurations.

NOTE: GPIOs will not function after reset until this change has been made to firmware.

By default, after BOR, all digital I/O are set as high-impedance with Schmitt triggers and their module functions disabled to prevent any cross current. This enables reduced power consumption when the device starts up.

The following code sequence is required to initialize GPIOs on reset and wakeup from LPMx.5:

1. Initialize all port pin registers as required for function: Port x Direction Register (PxDIR), Port x Pullup or Pulldown Resistor Enable Register (PxREN), Port x Output Register (PxOUT), Port x Select Register 0 (PxSEL0), Port x Select Register 1 (PxSEL1), and Port x Interrupt Edge Select Register (PxIES).
2. Clear the LOCKLPM5 bit.

```
PM5CTL0 &= ~LOCKLPM5
```
3. If not waking up from LPMx.5, clear all Port x Interrupt Flag Register (PxIFG) to avoid erroneous port interrupts.
4. Enable port interrupts using Interrupt Port x Interrupt Enable Register (PxIE).

For more information, see the *Configuration After Reset* section of the *Digital I/O* chapter in the [MSP430FR58xx, MSP430FR59xx, MSP430FR68xx, and MSP430FR69xx Family User's Guide](#).

4.1.1 Capacitive Touch I/O

The FR59xx family enables easy setup of capacitive touch implementation by using the internal pullup resistor in combination with an external capacitor to form an oscillator by feeding back the inverted input voltage sensed by the input Schmitt triggers to the pullup and pulldown control.

All GPIO pins can be used for cap sense. The cap sense functionality is implemented through the CAPSIOCTLx registers. For more information, see the *CapSense I/O* chapter in the [MSP430FR58xx, MSP430FR59xx, MSP430FR68xx, and MSP430FR69xx Family User's Guide](#).

4.2 ADC12_B

The ADC12_B module in the FR59xx family has been redesigned for lower power and also includes some new features and enhancements over the ADC12_A commonly found in F5xx devices. For parametric comparisons such as power consumption, linearity, and sample time considerations, see the device-specific data sheet.

Some of the significant differences between the ADC12_A and the ADC12_B module are:

- The ADC12_B module supports 16 single-ended external input channels that can be combined to form 8 differential external input channels.
- The ADC12_B provides a new feature called the Window Comparator that allows the user to set threshold levels and compare conversion results to the thresholds. The thresholds are set in LSB units, and if a conversion result falls within the range of preset low and high threshold levels, an interrupt is triggered. Interrupts are also provided for when conversion results fall above or below the preset threshold levels. Note that the same window comparator thresholds are shared among all channels, and conversion results from different channels are compared against the same threshold levels when the feature is enabled. This feature is extremely useful for saving power, because it allows the device to stay in a low-power mode until the ADC input reaches a specific threshold. All other conversion results are discarded automatically, and the device only wakes up on threshold triggers.
- The F5xx ADC12_A requires 9, 11, and 13 ADC12CLK cycles for 8-bit, 10-bit, and 12-bit resolutions, respectively. In contrast, the FR59xx ADC12_B requires 10, 12, and 14 ADC12CLK cycles for 8-bit, 10-bit, and 12-bit resolutions, respectively.
- The formula for calculating the minimum sample time as highlighted in the section *Sample Timing Considerations* has changed. For more details, see the [MSP430FR58xx](#), [MSP430FR59xx](#), [MSP430FR68xx](#), and [MSP430FR69xx Family User's Guide](#).
- 32 ADC12MEMCTLx (memory control) registers are available for sequenced channel operation; 32 dedicated interrupts are available for reading the conversion memory.
- The following changes were made to the ADC12_B registers:

ADC12CTL0:

- ADC12OVIE and ADC12TOVIE bits were moved to the ADC12IER2 register.
- REF control was removed from the ADC module registers and can be accessed through the REF control registers.

ADC12CTL1:

- Additional predividers for ADC clock control (ADC12PDIVx) were moved to this register (previously found in ADC12CTL2).

ADC12CTL2:

- REFBURST feature is no longer available.
- REFOUT control was moved to REFCTL0 register.
- ADC12SR bit (in the F5xx family) was replaced by the ADC12PWRMD bit.

ADC12CTL3:

- Includes additional bits that allow mapping of internal channels.
- Conversion start address bits setting (CSTARTADDx) was added to this register.

The ADC12IE and ADC12IFG registers in the F5xx family have been replaced by ADC12IER0, ADC12IER1, ADC12IFG0, and ADC12IFG1 registers.

4.3 REF_A Module

The FR59xx REF_A module provides 1.2-V, 2.0-V, and 2.5-V references. The 1.5-V reference from the F5xx REF module is no longer available.

The following additional features are available in the REF_A module:

- Status indicators for the reference generator have been added through the REFGENACT and the REFBGACT bits.
- The REFGENRDY bit can be queried to determine if the REF_A has settled.
- The REFGENBUSY is useful in detecting when it is safe to change the REF_A settings. For example, the setting must not be changed when the ADC is in the middle of an active conversion.

4.4 Enhanced Universal Serial Communication Interface (eUSCI)

The architecture and internal state machine of the eUSCI is very similar to the USCI module in the F5xx family. However there are a host of new features added in the eUSCI as well as changes made to the existing features. While the firmware may continue to be compatible, it is recommended to review the register names and differences in features. [Table 5](#) highlights most of the significant differences between the families. See [Migrating from the USCI to the eUSCI](#) for detailed information.

Table 5. Comparison of USCI and eUSCI Modules

Parameter or Feature	USCI (F5xx, F6xx)	eUSCI (FR58xx, FR59xx)
UART		
Enhanced baud rate generation	No	Yes
TXEPT interrupt (similar to USART)	No	Yes
Start edge interrupt	No	Yes
Selectable glitch filter	No	Yes
Interrupt vector generator	No	Yes
SPI		
Maximum baud rate	4 MHz to 6 MHz	7 MHz
Interrupt vector generator	No	Yes
I²C		
Preload of transmit buffer	No	Yes
Clock low timeout	No	Yes
Byte counter	No	Yes
Multiple slave addressing	No	Yes
Address bit mask	No	Yes
Hardware clear of interrupt flags	Yes	No
Interrupt vector generator	No	Yes

4.5 DMA Controller

The DMA controller allows movement of data from one memory address to another without CPU intervention. The main difference for the DMA between the MSP430x4xx and the MSP430FR5/6xx MCUs is the number of DMA channels available. FRAM MCUs that contain a DMA controller can have up to 8 DMA channels available.

DMA trigger selection depends on the device. See the device-specific data sheet for the number of channels and the trigger assignments.

4.6 Low-Energy Accelerator (LEA) for Signal Processing

The LEA module is a hardware engine designed for operations that involve vector-based arithmetic and signal processing for the MSP430FR599x MCUs. Compared to using the CPU for these operations, the LEA module offers up to 19 times faster performance and up to 20 times less energy consumption when performing vector-based digital signal processing computations such as FIR or IIR filtering, correlation, and FFT calculations. The LEA module requires MCLK to be operational; therefore, the LEA module is enabled in active mode or LPM0. When the LEA module is used, data operations are performed and shared on 4KB of SRAM. The MSP CPU and the LEA module can run simultaneously and independently unless they access the same system RAM.

The LEA operations are abstracted within the Digital Signal Processing (DSP) Library for MSP MCUs for ease-of-use. DSP Library functions can be used on any MSP device; however, if the LEA module is available on the device, DSP Library automatically uses the LEA module for vector math operations.

Before using the DSP Library APIs, first specify the input and output memory locations by allocating an array in which the locations need to reside within the shared 4KB of LEA SRAM memory. For example, to perform 256-point complex FFT with the LEA module, the data input array consists of 256-word real and 256-word complex values which totals to 512 words (1024 bytes).

For more information on the LEA module, see the following links:

- [Low-Energy Accelerator \(LEA\) Frequently Asked Questions \(FAQ\)](#)
- [Benchmarking the Signal Processing Capabilities of the Low-Energy Accelerator](#)
- [Digital Signal Processing \(DSP\) Library for MSP MCUs](#)
- [MSP430FR5994 product page](#)
- [MSP430FR58xx, MSP430FR59xx, MSP430FR68xx, and MSP430FR69xx Family User's Guide](#)

5 Conclusion

This application report addresses many of the key feature changes and new modules in the MSP430FR59xx family. While it is intended to be comprehensive, there may be a few minor differences between the F5xx and the FR59xx families that have not been covered here. For details specific to a device, the device-specific data sheet is always the best source of information. For details on module functionality and use, see the [MSP430FR58xx, MSP430FR59xx, MSP430FR68xx, and MSP430FR69xx Family User's Guide](#).

For developers working with the FR59xx devices, two useful resources for getting started include [MSP430Ware software](#) and [Grace™ graphical configuration tool](#), a plug-in for Code Composer Studio IDE.

6 References

1. [Migrating From the MSP430F2xx Family to the MSP430FR57xx Family](#)
2. [MSP430FR58xx, MSP430FR59xx, MSP430FR68xx, and MSP430FR69xx Family User's Guide](#)
3. [MSP430F5xx and MSP430F6xx Family User's Guide](#)
4. [MSP430F543xA, MSP430F541xA Mixed-Signal Microcontrollers](#)
5. [MSP430FR59xx Mixed-Signal Microcontrollers](#)
6. [Migrating from the USCI to the eUSCI](#)
7. [Maximizing FRAM Write Speed on the MSP430FR5739](#)

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