Application Report
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Thermal Considerations of the PGA411

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ABSTRACT

This application report covers thermal performance of the PGA411-Q1 through the testing of two boards, the PGA411-Q1 Evaluation Module (EVM) and the industrial EMC Compliant Single-Chip Resolver-to-Digital Converter (RDC) Reference Design. Tests included parameter changes of boost voltage, peak-to-peak output voltage, and load currents. The tests were evaluated by observing the temperature changes for each adjusted parameter. Results show that the board layout was a major factor in thermal performance.

Contents

List of Figures

List of Tables

Trademarks

1 Introduction

In environments with high ambient temperatures, managing the junction temperature on integrated circuits is crucial. Keeping the heat across the device in check will extend the life of the device and ensure that the device will not fail due to exceeding its maximum operating limit. The PGA411-Q1 is an automotive qualified device with a junction temperature operation range from -40°C to +150°C and with an ambient operating temperature of -40°C to +125°C. To ensure the device does not exceed the 150°C junction rating, knowing which parameter settings affect the heating of the device is important to help minimize the heat across the device. Testing was done between two boards, the PGA411-Q1 Evaluation Module and the industrial EMC Compliant Single-Chip Resolver-to-Digital Converter (RDC) Reference Design, to see how board layout affected the thermal performance. The results show that the industrial design outperformed the EVM, with one test showing a difference of about 10°C between the two boards for the same power across the PGA411 device.

2 Set Up

The goal of this application report is to provide insight on parameters which affect the thermal performance of the PGA411-Q1 and to understand how to minimize the thermal dissipation with proper board layout practices. The power of an ideal system can be stated as the power in being equal to the power out. Figure 1 shows how the power is represented in the system of this application report. The power supply unit provides all of the input power of the system, whereas the consumed power will be from the PGA411-Q1 device, the load, and the external components from the boost converter. The load is tied to the PGA411-Q1's exciter amplifier outputs, OE1 and OE2. Normally the load is the resolver's stator coil, though for testing, it will be a variable resistor to test various parameters.

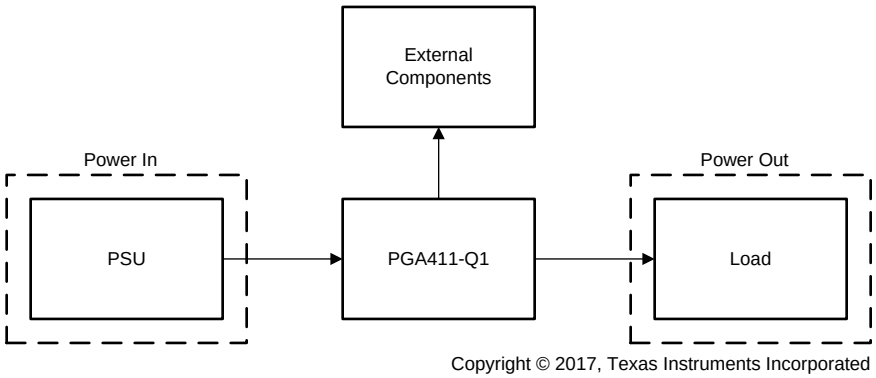

Figure 1. Power Flow Overview of System

$$P_{in} = P_{out\,total} \quad (1)$$

$$P_{in} = V_{in} \times I_{in} \quad (2)$$

$$P_{out\,total} = P_{load} + P_{device} + P_{external\_components} \quad (3)$$

$$P_{load} = V_{rms} \times I_{rms} \quad (4)$$

$$P_{device} = V_{in} \times I_{in} - V_{rms} \times I_{rms} \quad (5)$$

$$efficiency = \frac{P_{out\,avg}}{P_{in}} \times 100\% \quad (6)$$

Equation 1 shows the overall power of the system. Equation 2 calculates the input power by taking the supply current and multiplying it by the input voltage of the PGA411-Q1. Equation 3 shows that the total output power can be calculated by summing the power of the load, the power across the device, and the power dissipated through the boost converter's external components. The power on the external components is expected to be significantly low and will be assumed to be zero. Equation 4 shows that the power across the load can be found by multiplying the RMS voltage across the load by the RMS current through the load. To find the power across the load, use equations 1, 2, 3, and 4 to isolate for P_{load} to get Equation 5. It is important to solve for P_{device} because most of the power across the device will dissipate as heat and a small amount will dissipate to the external components of the boost converter.

All tests done in this application report were done using the PGA411-Q1 Evaluation Module and the EMC Compliant Single-Chip Resolver-to-Digital Converter (RDC) Reference Design with the intention of seeing how both designs relate in terms of thermal dissipation. The power efficiencies are expected to be the same for both boards because the same device being tested will be used in both designs. However, the heat at the junction is expected to different.

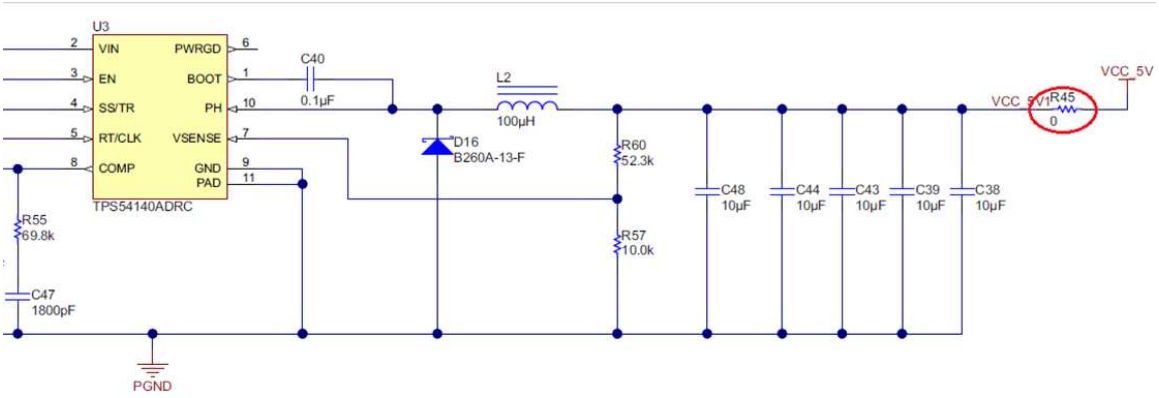

Figure 2. Buck Converter Schematic of Industrial TI Design

The industrial board does not use a 5-V input like the EVM board and instead uses the TPS54140A buck converter which requires a 12-V to 42-V input. To get more accurate data, the R45 resistor from the industrial board was removed, and a wire was soldered directly to the 5-V rail to supply the 5-V input from an external power supply. This procedure allows for a more similar set up to the EVM because it bypasses the buck converter, which otherwise would introduce power loss on the input due to the buck converter's power efficiency. Figure 2 shows the R45 resistor circled in red, placed directly after the buck converter to the 5-V rail.

Table 1. Instruments Used For Testing

Device	Model
Digital Multimeter (Voltage reading)	HP 34401A
Digital Multimeter (Current reading)	HP3448A
Infrared Thermal Imaging Camera	Flir i50
Power Supply Unit	Agilent E3646A
Resistor box	Clarostate model number 240-C

3 Boost Voltage's Relation to Power

Understanding which parameters affect power input and output is important for intentionally lowering heat seen by the device. The first parameter for consideration will be the boosted voltage of the exciter amplifier. This test was done with a constant load resistance of 150 Ω. This resistance was chosen to mimic a real resolver sensor's resistance and allowed for testing with both 4-V_{rms} and 7-V_{rms} modes without exceeding the current output limits on OE1 and OE2. The offset value was chosen to ensure the 7-V_{rms} mode would not clip and kept constant for the 4-V_{rms} mode, as well as to ensure the same supply current draw due to the offset parameter. For the test, the boosted voltage was changed from 10 V to 17 V in 1-V steps for both 7-V_{rms} and 4-V_{rms} mode, and the input power and output power were measured for each step. For the 4-V_{rms} mode, a typical pre-gain value was used. However, for the 7-V_{rms} mode, 1.50-V/V pre-gain was used to avoid clipping on the upper bounds of the output at 10 V of boosted voltage. The offset value was chosen to avoid clipping on the lower bounds of the output for the 7-V_{rms} mode. The efficiency was calculated by using Equation 6 as the ratio of output power to input power.

Table 2. Parameter of Constants for Boosted Voltage Test

	4-V_{rms} Mode	7-V_{rms} Mode
Offset	1.2 V	1.2 V
Pre-gain	1.55	1.50
Frequency	10 KHz	10 KHz
Resistance	150 Ω	150 Ω

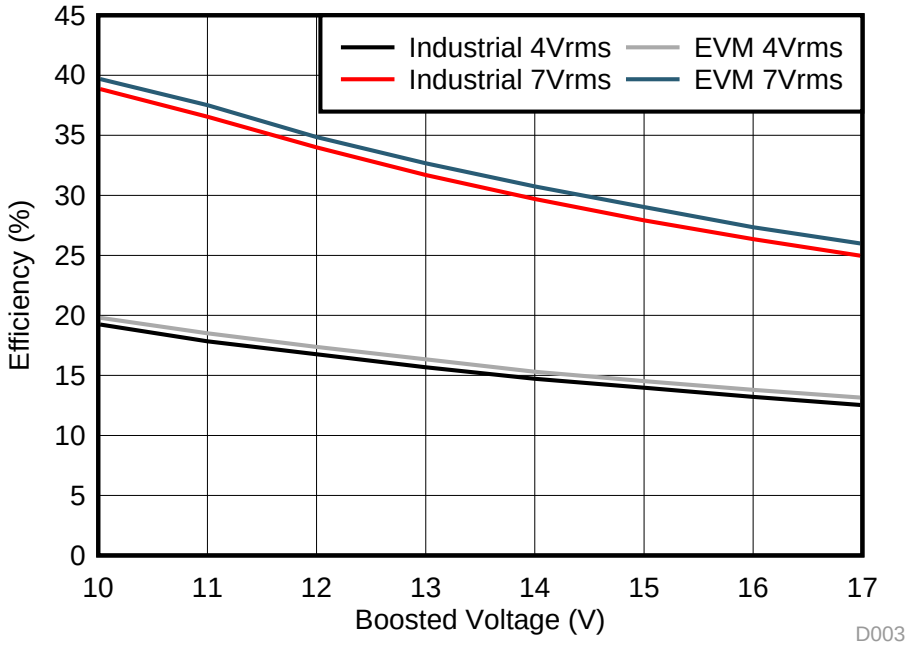

Figure 3. Efficiency versus Boosted Voltage Graph

From 10 V to 17 V, the efficiency decreases over each step for both 4-V_{rms} and 7-V_{rms} mode. The reason for this is because the current, resistance, and peak-to-peak voltage are constant, so from 10 V to 17 V, the output power does not increase, but the supply current to the device increases for each step up in voltage, therefore increasing the input power.

Table 3. Board Temperature versus Boosted Voltage at Ambient Temperature of 22.4°C

Boosted Voltage (V)	EVM 4-V_{rms} Temperature (°C)	Industrial 4-V_{rms} Temperature (°C)	EVM 7-V_{rms} Temperature (°C)	Industrial 7-V_{rms} Temperature (°C)
10	37.6	36.8	37.5	36.5
11	38.7	37.5	39.4	37.8
12	40.2	38.7	40.9	39
13	41.7	39.5	42.5	40.8
14	43.3	40.6	44.7	42
15	44.6	41.9	46.7	43.9
16	46.1	43.2	49.1	45.4
17	47.3	44.3	51.2	47.1

The temperature of the device being tested will also be affected by the output power remaining constant but the input power increasing. Table 3 shows how both boards and both output modes experience a temperature increase as the boosted voltage increases. The increase in temperature for the EVM board for 4-V_{rms} mode and 7-V_{rms} mode are 9.7°C and 13.7°C respectively. For the industrial design, at 4-V_{rms} mode and 7-V_{rms} mode, the temperature increases were 7.5°C and 10.6°C respectively. The industrial board has a lower temperature than the EVM board for all boosted voltages when compared to the same output mode. The ambient temperature of the room where the testing occurred was about 22.4°C.

3.1 Take Away Due to Boosted Voltage

By understanding that the boosted voltage decreases efficiency and affects the device's temperature, the boosted voltage should be kept as low as possible to minimize efficiency loss and unnecessary increases in temperature. Keeping the boosted voltage at 10 V would be optimal but not always possible due to the load resistance and load current under operation. In a typical case, the peak-to-peak output voltage is preferred to be set higher because it results in a higher signal-to-noise ratio. The boosted voltage must be adjusted higher to meet this requirement. In this case, TI recommends selecting the minimal boosted voltage required to avoid clipping. Doing so will minimize efficiency losses and unnecessary temperature increases in the PGA411.

4 Peak-to-Peak Voltage Output in Relation to Power

The peak-to-peak output voltage is a parameter which can be fine-tuned by adjusting the pre-gain setting and then largely amplified by the 4-V_{rms} and 7-V_{rms} stage. Making changes to the pre-gain and final-gain stage affects the peak-to-peak output voltage and therefore also affects the power efficiency and heating of the device. Testing was done to see how much of a difference the peak-to-peak output voltage had on power efficiency for all steps of the pre-gain stage with both 4-V_{rms} and 7-V_{rms} mode. Temperature measurements were taken at every five-step increment.

The boosted voltage parameters selected were picked based on commonly-used values. The load selected was 150 Ω for both output modes to simulate a real resolver sensor. Offset and frequency were held constant at 2.0 V and 10 KHz respectively.

Table 4. Parameter Constants for Peak-to-Peak Output Voltage Test

	4-V_{rms} Mode	7-V_{rms} Mode
Offset	2.0 V	2.0 V
Frequency	10 KHz	10 KHz
Boosted Voltage	12 V	15 V
Resistance	150 Ω	150 Ω

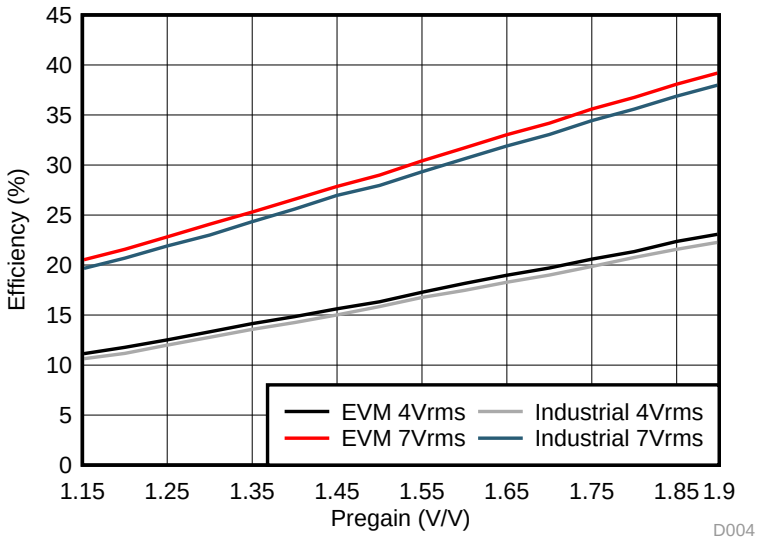

Figure 4. Efficiency versus Pre-gain Graph

Table 5. Board Temperature in Regard to Pre-gain Setting

Pre-gain	4-V_{rms} EVM Temperature (°C)	7-V_{rms} EVM Temperature (°C)	4-V_{rms} Industrial Temperature (°C)	7-V_{rms} Industrial Temperature (°C)
1.15	39.3	46	37.4	42.2
1.40	39.9	46.7	38.1	43
1.65	40.7	47	38.7	43.7
1.90	41	47	39	43.7

From Table 5, it can be observed that for both boards with higher peak-to-peak output voltage, temperature increases occurred. When the 7-V_{rms} mode was used to amplify the peak-to-peak output voltage, both boards stopped increasing in temperature at the 1.65 pre-gain setting and the temperature remained constant to 1.90 pre-gain. Due to the output power increasing at about the same rate as the input power, the power seen across the device stays constant, therefore the temperature remains at a constant. This observation, however, would differ depending on the boosted voltage used due to its effect on input power.

Comparing the EVM board and the industrial board, it can be observed the industrial board has lower temperatures for all peak-to-peak output voltage settings when comparing the same output modes. The difference for the 4-V_{rms} mode is about 2°C and for the 7-V_{rms} mode the difference is from 3.8°C to 3.3°C. When adjusting the peak-to-peak output voltage with the 4-V_{rms} mode and 7-V_{rms} mode, the temperatures for both boards were higher for the 7-V_{rms} mode. This increase is due to the power across the device being greater at a higher peak-to-peak output voltage that the 7-V_{rms} mode provided.

4.1 Take Away From Peak-to-Peak Output Voltage

With a higher peak-to-peak output voltage, the power efficiency increases as expected, but a more important observation is that with a lower peak-to-peak output voltage, there is lower power across the device and thus lower temperature on the device when compared to higher peak-to-peak output voltages. For a more sensitive application where device temperature is more of a concern due to a high ambient temperature, using lower peak-to-peak output voltage with the 4-V_{rms} output mode may be considered. In applications which temperature is less of a concern, using a higher peak-to-peak output voltage may be considered to get the most out of the power efficiency with relatively low increases to temperature. The peak-to-peak output voltage should be kept at a level that allows for the sine and cosine differential inputs to stay within the range of 600 mVpp to 1.5 Vpp.

5 Load Current's Relation to Power

To observe thermal dissipation of both boards, doing a current sweep by adjusting the load resistance was done. The load current is a parameter which is related to the load impedance and is dependent on the resolver sensor. This data provides understanding on how both boards behave in terms of thermal dissipation. The test will cover peak load current values from 25 mA_{peak} to 145 mA_{peak}, where the 145-mA_{peak} upper limit was chosen due to the OE1 and OE2 maximum recommended operating conditions. The temperatures, power in and power out, were measured for each current load change. The power across the device was calculated and graphed against the temperature across the device seen in Figure 5.

Table 6 shows the parameters set for the initial test. The offset value was chosen to be kept at default to allow for more footroom and avoid clipping at the bottom of the output waveform. The gain and boosted voltage setting was selected on which output mode was considered. With the 7-V_{rms} mode, a boosted voltage of 15 V and gain of 1.90 was chosen as an expected typical value of use. The same reasoning was used for the 4-V_{rms} mode with a gain of 1.55 and boosted voltage of 12 V.

Table 6. Parameter Constants for Load Current Sweep Test

	4-V_{rms} Mode	7-V_{rms} Mode
Offset	2.0 V	2.0 V
Gain	1.55	1.90
Frequency	10 KHz	10 KHz
Boosted Voltage	12 V	15 V

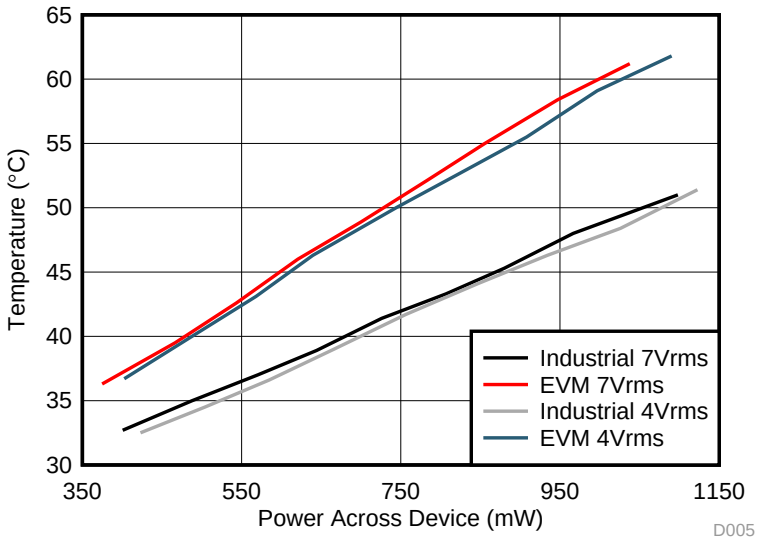

Figure 5. Temperature versus Power Across Device Graph

5.1 Take Away From Load Current

The data in Figure 5 shows the temperature of the device is linear with respect to the power across the device. Regarding the EVM and industrial board, the temperature on the device is higher for the EVM board than it is for the industrial board. The 7-V_{rms} and 4-V_{rms} modes both show the same results with very similar slopes for both boards. The main difference between these two boards is the layout and therefore the temperature across the device is influenced by the board layout.

6 PCB Thermal Analysis

From the previous tests done, it was observed that the industrial board was more efficient at dispersing the heat across the device than the EVM board. The reason behind the temperature differences in both boards is due to the printed-circuit board (PCB) layout.

From a thermal standpoint, Ohm's law is similar to Equation 7. This means temperature, power, and thermal resistance can be related to electrical voltage, current, and resistance respectively. The thermal resistance from the junction to the ambient air can be found by readjusting Equation 7, where T_j -T_a is the "voltage drop" or the temperature across the thermal resistance. This is represented in Equation 8. The temperature at the junction can be found by solving for T_j in Equation 8 and is shown in Equation 9.

$$T = P \times \theta \tag{7}$$

$$\theta ja = \frac{Tj - Ta}{Pd} \tag{8}$$

$$Tj = Pd \times \theta ja + Ta \tag{9}$$

Table 7. Definition of Symbols

Symbol	Definition
T	Temperature (°C)
P	Power (W)
θ	Thermal resistance (°C/W)
θ_{ja}	Thermal resistance between ambient air and junction (°C/W)
T_j	Junction Temperature (°C)
T_a	Ambient Temperature (°C)
P_d	Power across device (W)

From Equation 9, it is now possible to quantitatively analyze why a temperature difference between the EVM board and the industrial board occurred. The temperatures measured during the tests were measured from an IR camera at junction T_j. For all tests done, the ambient temperature, T_a, stayed relatively constant. It was observed that the temperature was different for about the same power across the device, therefore the variable, which was different between the two boards, was the thermal resistance between the junction and the ambient air, θ_{ja}. Therefore, the thermal resistance between the junction and the ambient air for the industrial board must be lower than the EVM board to produce a lower junction temperature. From collected data where the power across both board's device was about 1 W, the ambient temperature at around 22.4°C, and the board temperatures at 61.2°C and 52°C for the EVM and industrial, respectively, the thermal resistance from junction to ambient air can be calculated. For the EVM board, θ_{ja} is found to be 38.8°C/W while the industrial board has a value of 29.6°C/W. From this, it can be concluded that to achieve better thermal performance, the thermal resistance between the junction and the ambient air should be kept as low as possible. The θ_{ja} found for both cases was from one set of data points and is only an estimation. To get a more accurate number, multiple samples on multiple devices should be collected.

The θ_{ja} calculation differs from the one found in the PGA411-Q1 Resolver Sensor Interface Data Sheet at 25.5°C/W. This number was found by using the Joint Electron Device Engineering Council (JEDEC) standards and therefore allows designers to compare packages from different companies to each other assuming both companies followed the JEDEC standard. This standard uses a different layout design and therefore the θ_{ja} parameter will differ from the EVM and industrial board.

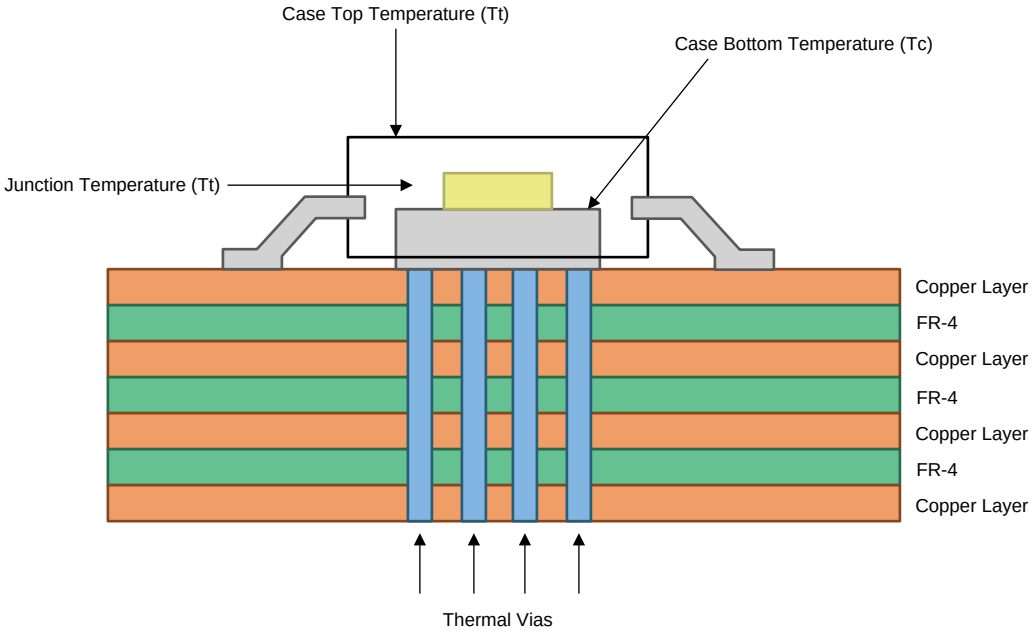

Figure 6. Model of Package on PCB

It is necessary to understand what contributes to the thermal resistance between the junction and the ambient air to minimize it. Figure 6 models an integrated circuit sitting on top of a PCB. The model shows what is in contact with the junction and the ambient air, which is important for modeling the thermal resistance.

Figure 7 shows how the thermal model of the junction to ambient air is usually done with a resistive network and follows the path from the junction to ambient air. The reason for two resistor paths seen in Figure 7 is due to the junction being able to pass heat to the top of the case to the ambient air as well as passing heat through the bottom of the case, through the PCB, to the ambient air.

Table 8. Thermal Symbol Definitions

Symbol	Definition
T_j	Junction temperature (°C)
T_c	Bottom of case temperature (°C)
T_t	Top of case temperature (°C)
T_a	Ambient air temperature (°C)
θ_{jc}	Junction to bottom of case thermal resistance (°C/W)
θ_{jt}	Junction to top of case thermal resistance (°C/W)
θ_{ca}	Bottom of case to ambient air thermal resistance (°C/W)
θ_{ta}	Top of case to ambient air thermal resistance (°C/W)
θ_{ja}	Junction to ambient air thermal resistance (°C/W)

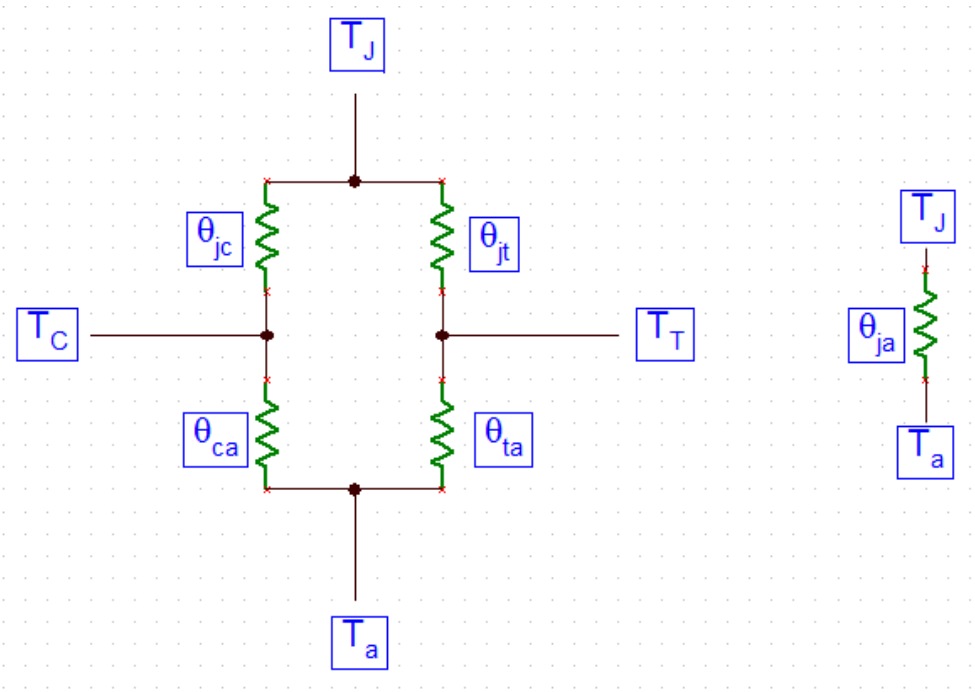

Figure 7. Resistive Network of Thermal Model

The resistive network on the left of Figure 7 can be simplified to the single resistor seen on the right. The result is θ_{ja}, which is what is needed to be kept low. However, to do so requires manipulating the resistance network seen on the left of Figure 7. From the four thermal resistances in the network, three cannot be altered. The θ_{jc}, θ_{jt}, and θ_{ta} are all determined by the package of the integrated circuit. The θ_{ca}, therefore, is the only thermal resistance which can be manipulated and by observation, with θ_{ca} in series with θ_{jc} and parallel with θ_{jt} and θ_{ta}, to get a lower θ_{ja}, then θ_{ca} should be kept as small as possible. θ_{ca} is the thermal resistance from the bottom of the case through the PCB layers to the ambient air. The PCB is made up of multiple layers. There are usually four layers for the PGA411-Q1 device and several layers of dielectric. The bottom of the case is also usually in contact with thermal vias. Therefore, to minimize θ_{ca}, it is necessary to design the PCB with proper thermal practices.

The following list includes examples of proper thermal PCB practices:

- Use as many thermal vias on the thermal pad of the PCB as allowable.
- Use the second layer for the ground plane to be closer to the source of heat.
- Make the mid-layer ground plane stretch as wide as possible (edge-to-edge of PCB).
- Allow for more area to stretch across the ground plane with a larger PCB; although this may not always be possible due to cost or size constraints.
- Use the bottom layer for ground and make it as wide as possible.
- Avoid discontinuity in the thermal path.
- Because heat flows laterally outwards from the center of the heat source to the edges of the ground planes, make necessary breaks due to traces or other reasons in the thermal path run in the same direction as the heat flow rather than perpendicular to it. An example can be seen in Figure 8.
- Use thicker copper layers to help better dissipate heat.

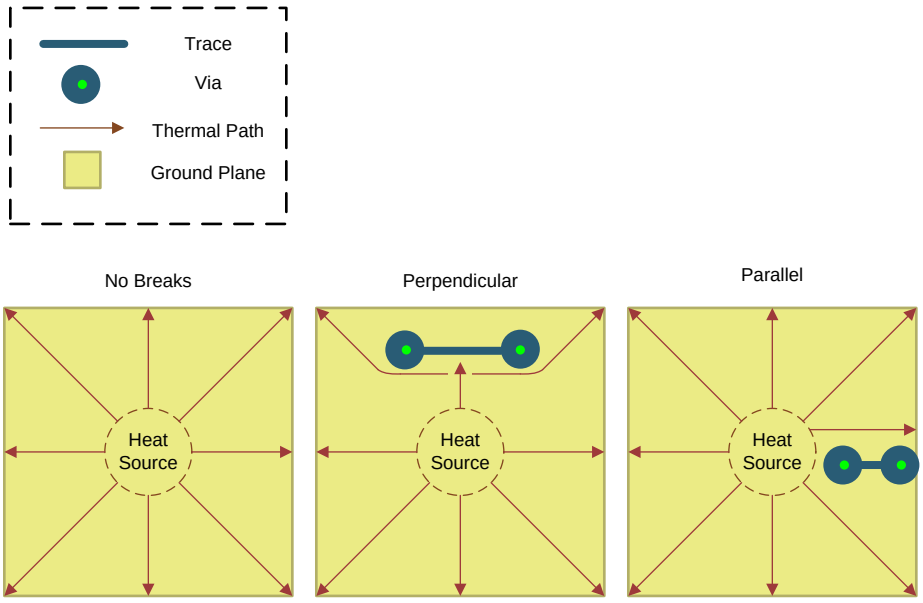

Figure 8. Heat Flow Diagram in Regard to Parallel and Perpendicular Breaks

7 EVM versus Industrial Board Comparison

Figure 9 and Figure 10 are images taken from an IR camera with a load of about 1000 mW across the PGA411 at an ambient temperature of 22.4°C. The EVM image shows the thermal energy concentrated at the center, evenly dispersed outwards, while the industrial image has more heat flowing away from the center and is much less uniform. With proper thermal layout practices, the industrial board is capable of reducing the temperature rise of the device by 11.2°C. In terms of thermal performance, this shows the industrial board is about 29% better at dissipating heat compared to the EVM board.

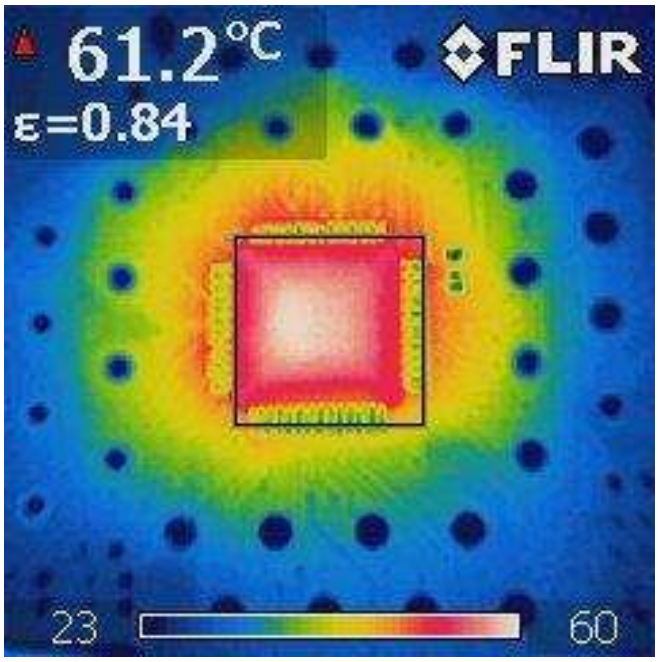

Figure 9. EVM Infrared Image

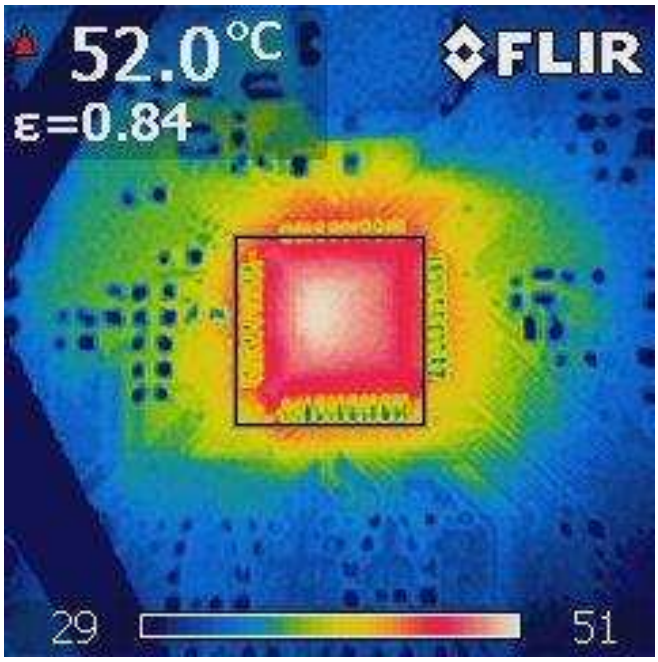

Figure 10. Industrial Infrared Image

Figure 11 shows exactly how the EVM and industrial boards are laid out. Looking at the EVM board, the PGA411 sits directly on top of the thermal pad, which is only a small piece of exposed copper meant to just fit the device on. The industrial board sits on the thermal pad but also has thermal vias in the middle of the thermal pad. The thermal vias connect to the digital ground plane in the middle of the board and also to the bottom ground plane. Figure 13 and Figure 14 show the digital ground plane and bottom ground plane.

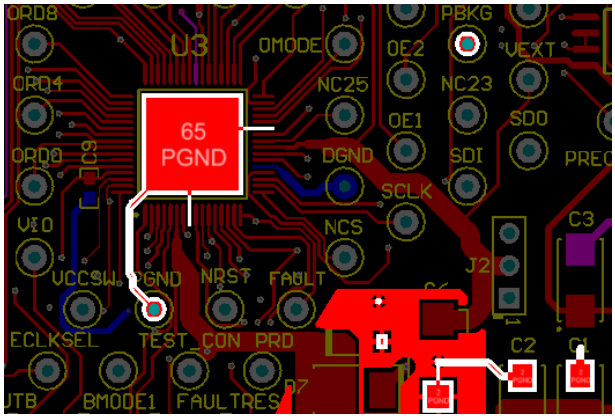

Figure 11. EVM Layout

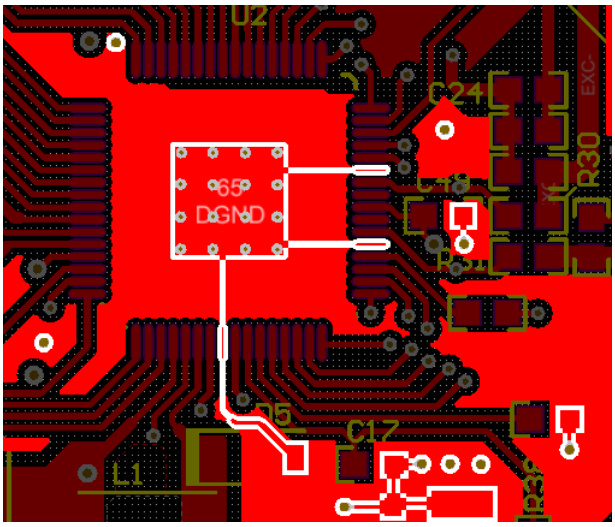

Figure 12. Industrial Layout

Figure 13 and Figure 14 show the amount of area both planes use. The digital ground plane in Figure 13 goes from edge to edge of the board to help disperse the heat across the entire board. The bottom layer also uses a lot of the area on the board and is exposed to the ambient air which helps disperse the heat into the air, making it important for this area to be large.

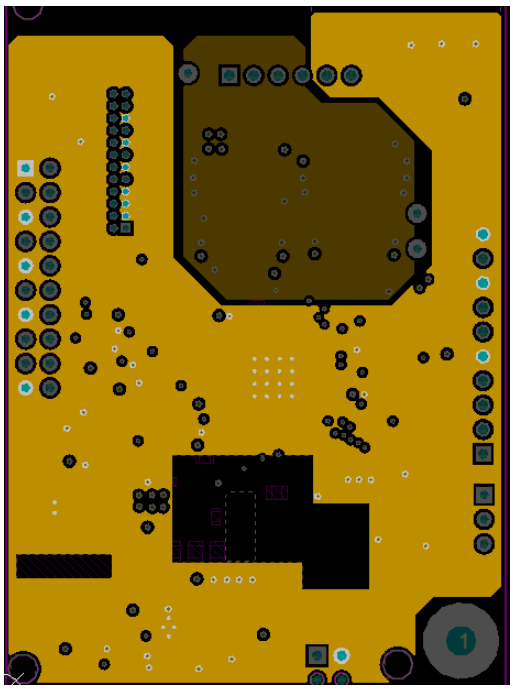

Figure 13. Industrial Mid-layer Ground Plane

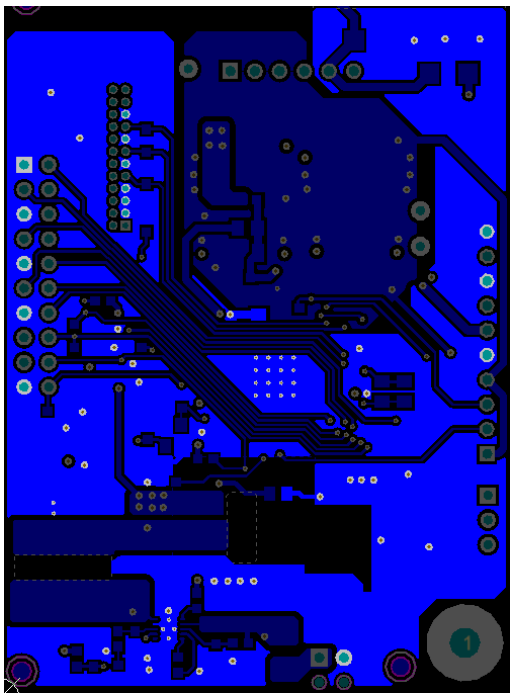

Figure 14. Industrial Bottom Layer Ground Plane

8 Conclusion

Thermal performance is an important consideration for any design and is essential for heat-sensitive applications with high ambient temperatures. From a power efficiency standpoint and in regard to the boosted voltage parameter, it was found that using the lowest boosted voltage setting would minimize power efficiency loss and unnecessary increases on device temperature. When considering pre-gain, using higher pre-gain values allowed for better power efficiency at the cost of minor temperature increases, where for thermal sensitive applications, the 4-V_{rms} mode should be considered to minimize heat across the device. In regard to thermal performance, the industrial design proved to outperform the EVM due to the use of multiple thermal vias and the use of large ground planes on both the middle and bottom layer of the PCB.

9 References

- Texas Instruments, AN-2020 Thermal Design By Insight, Not Hindsight Application Report
- Texas Instruments, AN-1520 A Guide to Board Layout for Best Thermal Resistance for Exposed Packages Application Report

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