Application Report

SLAA863–November 2018

AFE76xx as a Single-Chip Wideband Repeater Using Loopback Mode

Yusuf Agoro

ABSTRACT

This application report evaluates the performance of the AFE7686 as an RF sampling wideband repeater capable of operating with a frequency bandwidth as wide as 130 MHz and above. 5G networks demand RF repeaters that can support very large signal bandwidth. The AFE7686 includes dual- and quad-channel 14-bit, RF-sampling analog front ends (AFEs) that integrate four digital-to-analog converters (DAC) and four analog-to-digital converters (ADC) capable of sampling up to 9 GHz and 3 GHz, respectively.

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Trademarks

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1 Introduction

This application report evaluates the performance of the AFE7686 as an RF sampling wideband repeater capable of operating with a frequency bandwidth as wide as 130 MHz and above. 5G networks demand RF repeaters that can support very large signal bandwidth. The AFE7686 includes dual- and quad-channel 14-bit, RF-sampling analog front ends (AFEs) that integrate four digital-to-analog converters (DAC) and four analog-to-digital converters (ADC) capable of sampling up to 9 GHz and 3 GHz, respectively.

Features include:

- No FPGA or ASIC required
- No requirement of JESD link establishment
- No physical SerDes receiver and SerDes transmitter lanes needed
- Single-chip operation
- Wide-RF instantaneous bandwidth supporting 130 MHz–500 MHZ

Applications include:

- 5G Wideband RF repeater

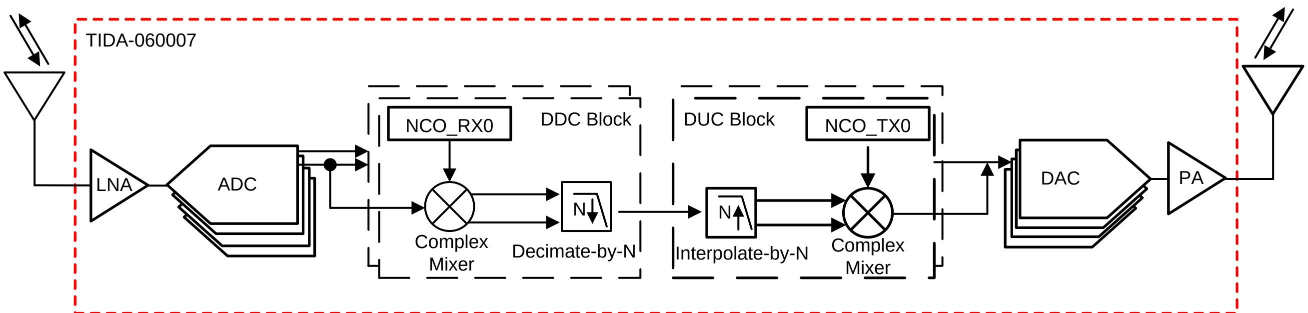

Figure 1. Block Diagram

2 System Description

The TIDA-060007 utilizes the loopback feature of the AFE7686 device to function as a direct sampling, single-chip 4T4R wideband RF repeater. The application focus is 5G signals with bandwidths of 130 MHz and above.

The goal for all wireless communication systems is to effectively distribute signals to and from users while providing optimum coverage. Such goals have driven the demand for systems to operate at higher data rates. Though not set in stone, 5G will supposedly support peak data rates in the Gbps range and average user data rates of up to 100 Mbps. To achieve these data rates, wide signal bandwidths of 500 MHz, 1 GHz and even up to 2 GHz will be required. The demand for wide-band RF repeaters capable of operating with such high bandwidths is sure to increase in order to achieve optimum coverage for wireless systems. In general, RF repeaters are located throughout cells where RF signal-path obstructions exist between users and base stations. A few different repeater types follow:

- Analog: performs analog processing on received signal
- Digital: performs digital processing on received signal
- On-frequency: retransmits frequency on the same frequency in which it was received
- Off-frequency: retransmits frequency on frequency other than received signal

Typical repeater systems configurations are 4T4R made up of four 1T1R or two 2T2R subsystems. This application report is designed to showcase the AFE7686 as an integrated single-chip 4T4R digital wideband repeater.

2.1 Key System Specification

Table 1. Key System Specifications

Parameter	Specifications
Selectivity	–50 dBc at +23 MHz offset from effective decimation bandwidth –70 dBc + 30 MHz offset from effective decimation bandwidth
Effective decimation bandwidth	131.07 MHz
Adjacent-channel power ratio (ACPR) degradation	approximately 9.5 dB
Latency	1.12 µs
Maximum gain	9 dBm

3 System Overview

3.1 Block Diagram

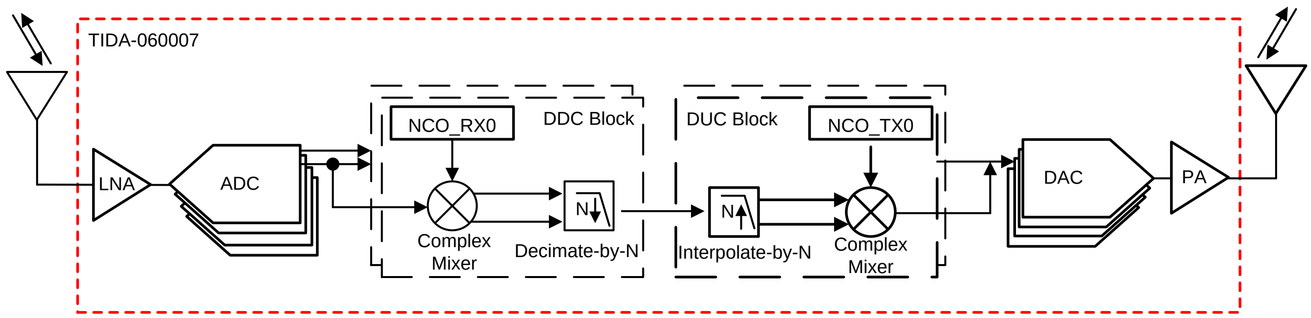

Figure 2. TIDA-060007 Block Diagram

3.2 Design Considerations

Important metrics when evaluating the performance of a repeater include isolation, selectivity, AC performance degradation, maximum gain and latency. Selectivity is easily one of the most important metrics when it comes to defining overall repeater system performance. The idea is to eliminate unwanted signals from being transmitted within the desired signals pass band of the repeater. This is crucial to reducing interference to operators in other bands. Antenna isolation is also very important because the output signal at the donor antenna can easily feedback to the service antenna, ultimately interfering with the input signal. The isolation between the donor antenna and the service antenna should be at least 30 dB. Repeaters introduce delay due to digital processing and filtering. The time it takes for an input signal to travel from RX input to TX output is referred to as input to output group delay and is usually denoted in terms of microseconds. Ideal repeaters are 100% transparent to the overall communication system, so latency is desired to be as low as possible. Typical latency can range from 2–6 µs depending on the architecture. Repeaters are transparent user and base station, meaning that ideally the repeated signal should be an exact, amplified replica of the input signal. Poor ACPR performance, poor antenna isolation, and poor selectivity in a repeater can undesirably distort the input signal before it reaches its final destination. Therefore, a good repeater will introduce minimum performance degradation atthe input signal.

3.3 Highlighted Products

The AFE768x family has an integrated (DSA) on the receiver channels and also supports DSA equivalent functionality on the transmitter channels. Each receiver channel has one analog RF peak power detector and various digital power detectors to assist in automatic gain control (AGC) for receiver channels, and two RF overload detectors for device reliability protection. The AFE768x family has 8 JESD204B compatible SerDes transceivers running up to 15 Gbps. The devices have up to two DUCs per TX channel and two digital downconverters (DDC) per RX channel, with multiple interpolation and decimation rates, and digital quadrature modulators and demodulators with independent, frequency flexible NCOs. The devices support up to 600-MHz RF signal bandwidth in single-band mode, and up to 300-MHz RF signal bandwidth per band in dual-band mode. A low-jitter phase-locked loop (PLL) voltage-controlled oscllator (VCO) simplifies the sampling clock generation by allowing use of a lower frequency reference clock. The primary components discussed in this TI Design are the AFE7683 and AFE7685 (4T4R capable). As a 4T4R system, this repeater has the ability to operate on two separate bands using a 2T2R configuration for each repeating link.

3.3.1 LMK04828

The LMK04828 is a dual-PLL jitter cleaner and clock generator. An onboard 122.88-MHz voltage-controlled crystal oscillator (VCXO) provides the reference frequency. This can be locked to an external 10-MHz reference if desired. The LMK04828 supplies the JESD204B SYSREF clocks to the ADC and FPGA and passes the 122.88-MHz reference signal to the LMX2582 for its reference.

3.4 System Design Theory

A digital RF repeater accomplishes the following goals:

1. Shows good selectivity by eliminating unwanted signals from being transmitted within the desired signals pass band which reduces interference in other bands.
2. Shows good antenna isolation between the donor and the service antenna
3. Has low RX to TX latency
4. Shows low AC performance degradation.

Figure 3 shows the basic traditional RF repeater design architecture.

The traditional repeater architecture first conditions the input signal using filters and LNAs. The LO-mixer downconverts the band to an intermediate frequency. The signal is filtered, sampled, and then sent to an FPGA for digital processing. The down-mixing process is then reversed and the final signal is output through the donor antenna to the desired base station.

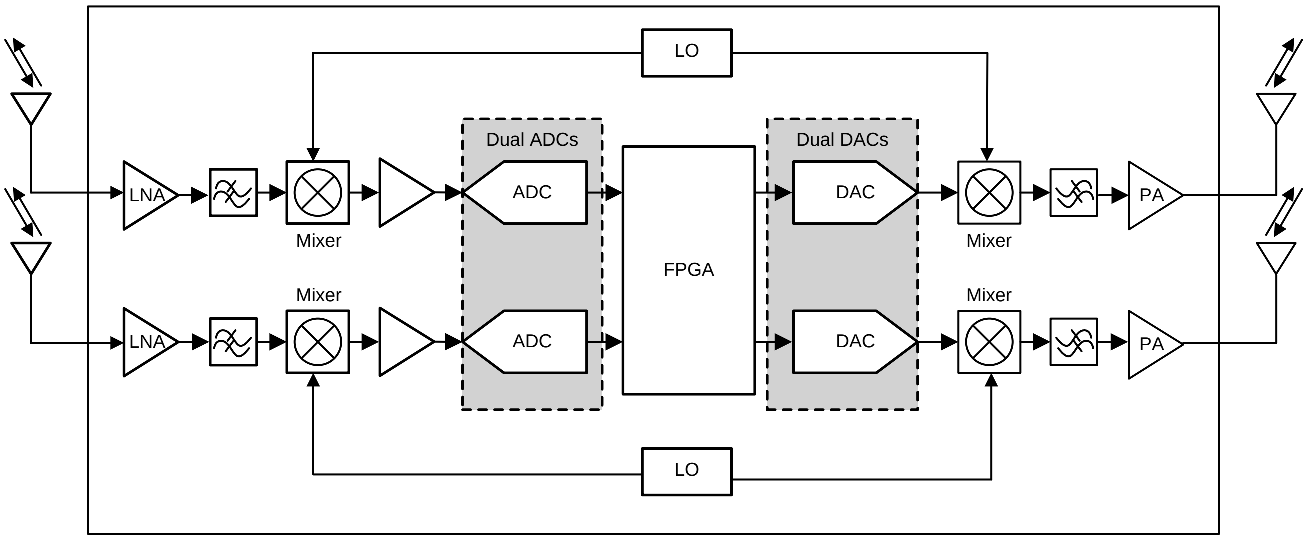

Figure 3. Traditional Digital RF Repeater

All of the frequency translation functions of the traditional RF repeater are performed in the digital domain of the integrated AFE7686 solution, replacing the need for discrete mixers, IF filters, and LOs (PLLs) from the analog-signal chain to achieve direct synthesis.

4 Hardware, Software, Testing Requirements, and Test Results

4.1 Hardware

The hardware used to test is as follows:

- Rohde and Schwarz SMA 100 Signal Generator
- DAC38RF82 RF DAC EVM
- Agilent E4443A Spectrum Analyzer
- Agilent E5071B Network Analyzer

4.2 Measured Latency and Gain

The goal of this measurement is to evaluate the group delay and maximum gain of the RX - TX repeater using an Agilent E5071B network analyzer.

4.2.1 Test Setup and Results

Figure 4 shows the setup. Port 1 drove the input of the repeater with frequencies ranging from 1900 MHz to 1920 MHz and port 2 received the signals from port 1 documenting the time of flight from Port 1 to Port 2. The average group delay is about 1.12 µs. Figure 4 shows a graph of latency as a function of frequencies between 1900 MHz and 1920 MHz.

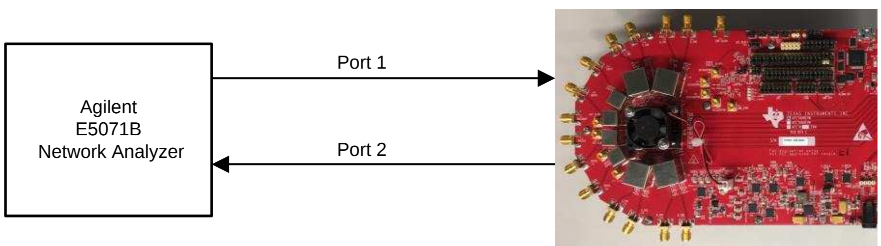

Figure 4. Latency and Gain Test Setup

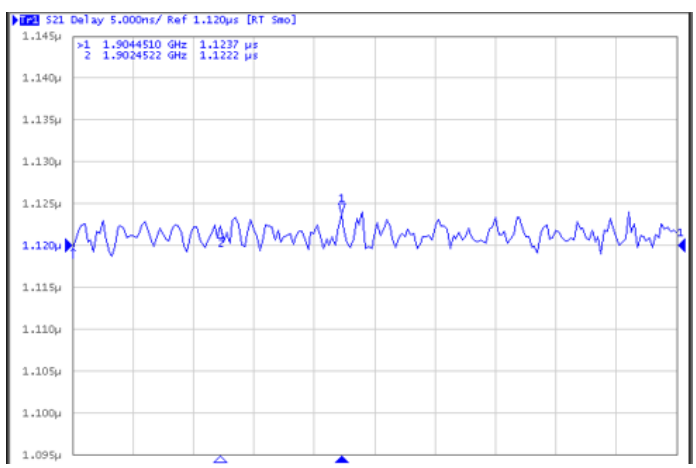

Figure 5. Latency Measurement, Average Latency = 1.12 µs

The maximum gain was determined using the same setup as group delay and is approximately 9 dBm when both of the RX and TX DSA settings are set to 0. Figure 6 shows a graph of gain verses frequencies between 1900 MHz and 1910 MHz.

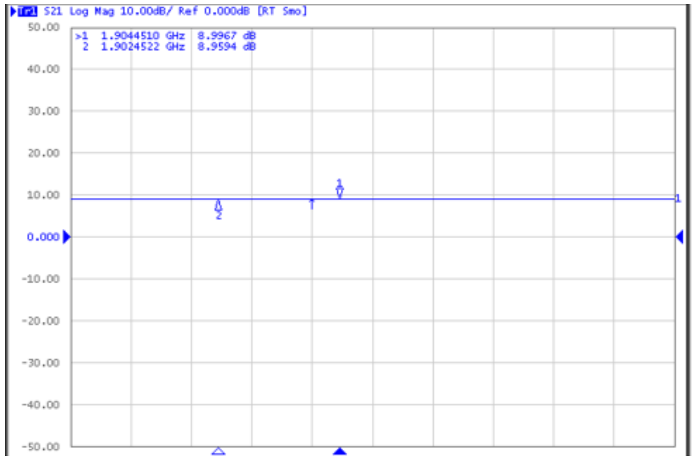

Figure 6. Gain Measurement: Gain is Flat at 9 dBm With TX/RX DSA set to 0

4.3 *Measured Linearity Performance*

The goal of this measurement is to evaluate the transparency of the repeater by showing the ACPR degradation of a signal through loopback.

4.3.1 Hardware and Test Setup

The DAC38RF82 is an RF DAC that generates the signal of the ACPR performance measurements. When measuring ACPR degradation, the RF DAC outputs a clean 20-MHz long-term evolution (LTE) signal centered at 1907MHz. The output signal of the DAC first passes through a band-pass filter before being connected to the input of the repeater. Figure 7 shows a block diagram of the setup. The ACPR of the LTE waveform is measured directly at the output of the DAC and also at the output of the repeater using the spectrum analyzer. The comparative difference in ACPR is the degradation of the LTE waveform due to the repeater.

Figure 7 shows the test setup for ACPR degradation.

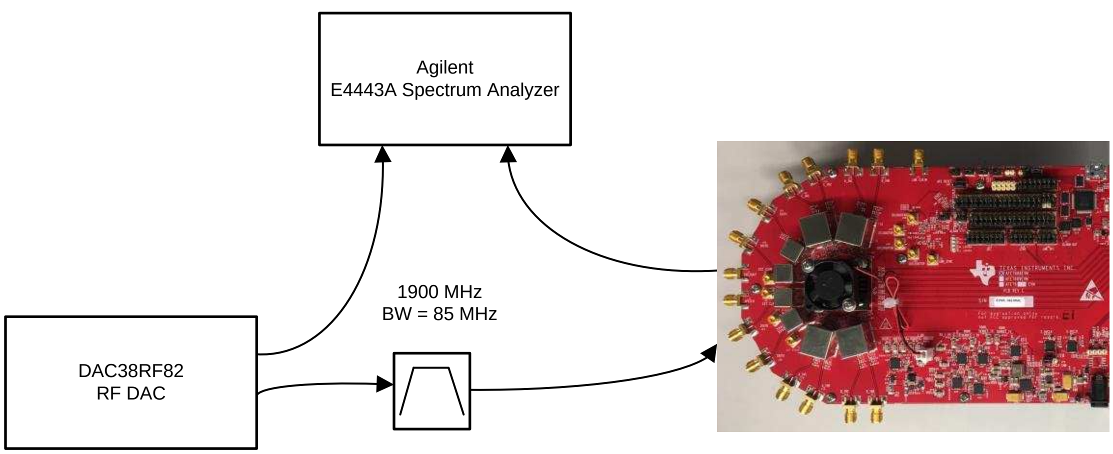

Figure 7. Test Setup for ACPR Degradation

4.3.2 Test Results

Figure 8 and Figure 9 show the before and after LTE ACPR measurements of the repeater are approximately 73 dB and 65 dB, respectively The ACPR degradation due to the receiver is approximately 9 dBm. Notice that the reference level offset in Figure 9 has increased by 2 dB to account for the loss due to the filter and the extra SMA cables. The RX and TX DSAs were set to 1 and 0 respectively to yield an overall gain of 6 dB.

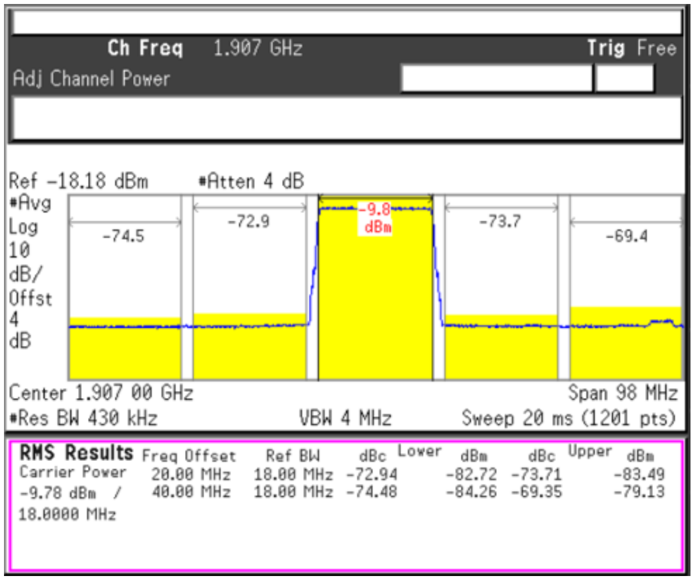

Figure 8. Clean ACPR Measurement Directly From DAC38RF82

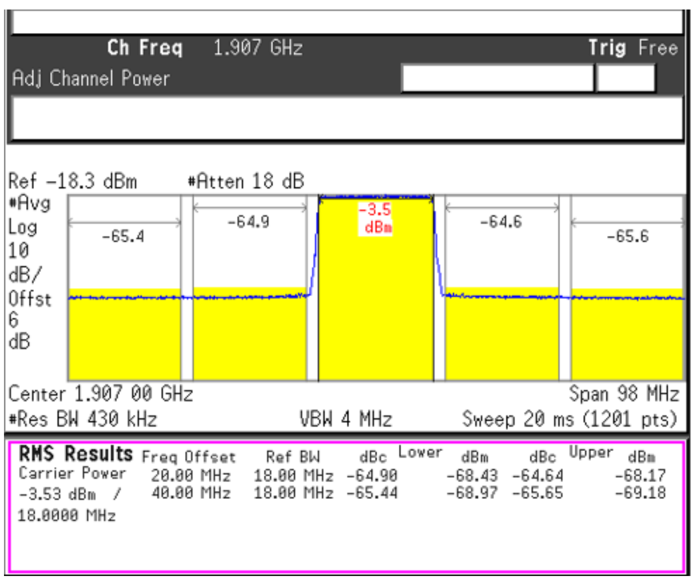

Figure 9. Repeater ACPR Measurement From Output Shows 6-dB Gain of Waveform and 8-dB ACPR Degradation

4.4 Measured Selectivity (Out-of-Band Jammer)

The goal of this measurement is to characterize the in-band selectivity by sweeping a jammer in the transition band of the repeater and recording the roll-off. Digital processing takes place in the on-chip DDC and digital upconverter (DUC). Therefore, the transition band roll-off is fully dependent on the interpolation and decimation filters.

4.4.1 Hardware and Test Setup

A DAC38RF82 is used to generate two 20-MHz LTE carriers spaced at 100 MHz and centered at 1870MHz. The LTE carriers simulate a 120-MHz wideband signal. A jammer signal is simulated by a CW tone produced by a SMA Rhode and Schwartz signal generator. A 350-MHz to 6-GHz, mini-circuits power splitter combines the wideband signal and CW tone to the input of the repeater. Figure 10 shows a block diagram of the setup.

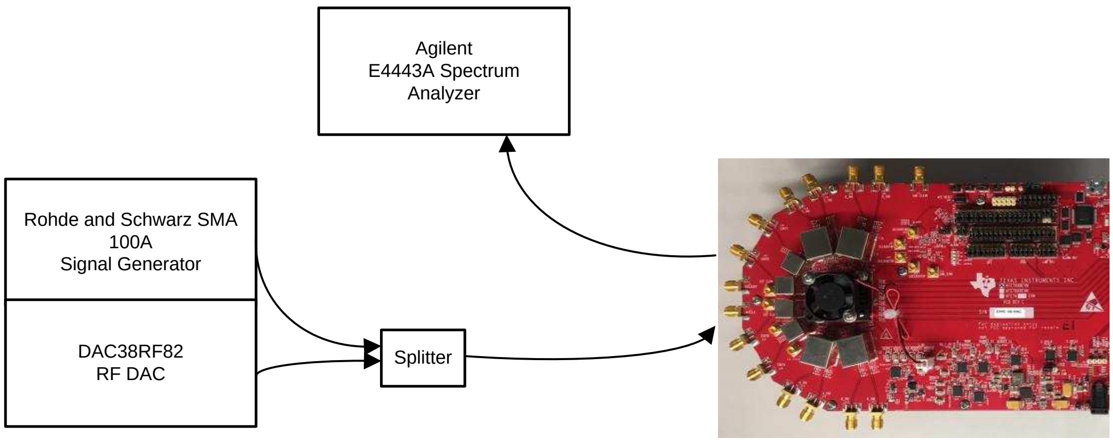

Figure 10. Hardware Setup for Jammer Simulation

4.4.2 Test Results

Figure 11 shows a repeated 120-MHz wideband signal at the output of the repeater without the jammer present. Figure 12 shows the jammer swept from the edge of the effective decimation pass band, through the transition band until the jammer is fully attenuated. The resulting measurement shows –50 dBc of attenuation at +23 MHz as denoted by marker 2.

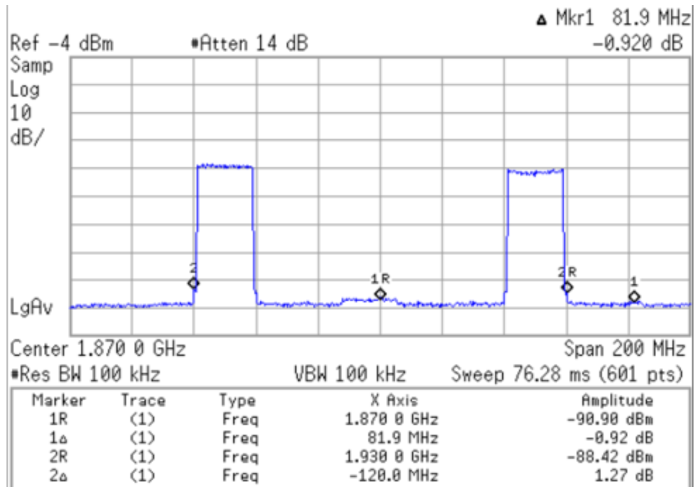

Figure 11. Repeated Wideband Signal Simulating a 120-MHz Carrier

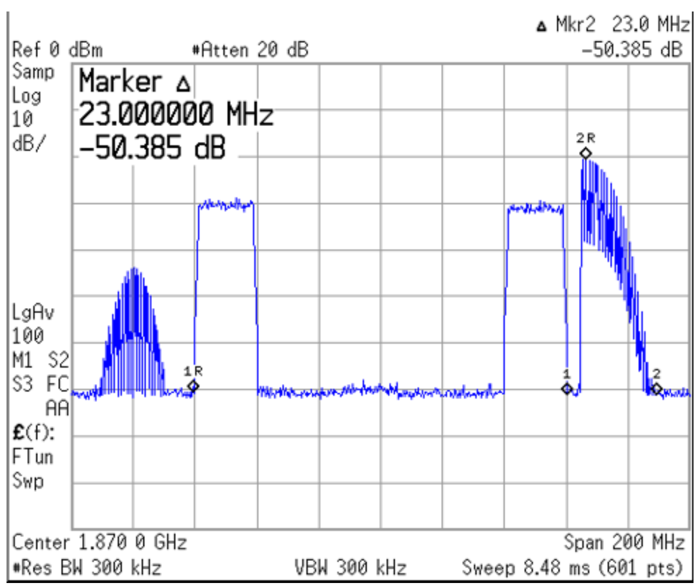

Figure 12. –50-dBc Attenuation at 23-MHz Outside Decimation Bandwidth

5 Terminology

Downlink: the traffic transmitter for the communication link, with respective to the main data source at the service provider

TX: Traffic Transmitter for the communication link

TXDAC: digital-to-analog converter used for traffic transmitter

Uplink: the traffic receiver for the communication link, with respective to the main data source at the service provider.

RX: Traffic Receiver for the communication link

RXADC: analog-to-digital converter used for traffic receiver or feedback receiver

DPD: digital pre-distortion for power amplifier linearization

PA: power amplifier for transmitter link

LNA: low noise amplifier for receiver link

DAS: Distributed Antenna System

MU: Master Unit in DAS

RU: Remote Unit in DAS

BTS: Base Station Unit

MIMO: Multiple-Input-Multiple-Output

JESD204B: JEDEC Standard for High Speed Serial Link for Data Converters.

PLL: Phase Locked Loop