Design considerations for resolver-to-digital converters in electric vehicles

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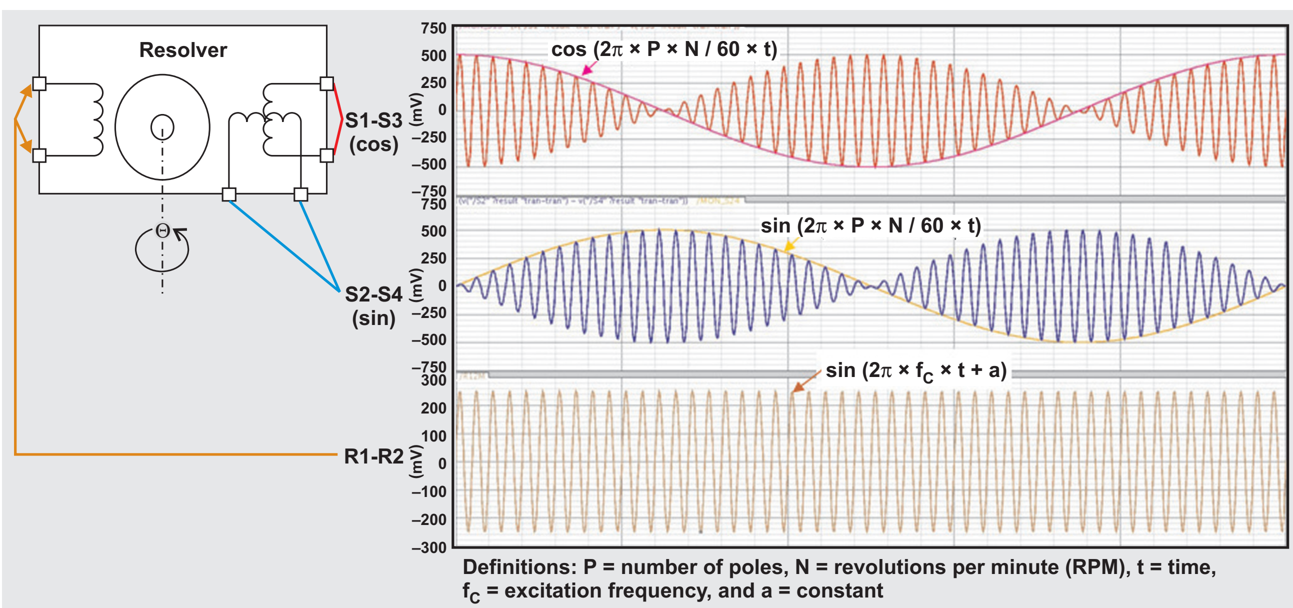
Introduction

A resolver is an angular position sensor that is commonly used in harsh, rugged environments. A fully electric vehicle (EV) may use multiple resolvers for a variety of control systems that perform rotary motion and additional resolvers may be required to create system redundancy for safety.[1] A resolver-to-digital converter (RDC) interface processes the analog output of the resolver sensor and communicates it in digital format to the engine control unit (ECU) in an EV. When designing an RDC interface, it is important to select the right RDC architecture to ensure that the circuit operates consistently under stringent conditions (such as vehicle acceleration). This article presents an overview for the architecture of a RDC interface circuit. The PGA411-Q1 is an example of the RDC interface circuit described.[2] Included is a review of the basic principles involved in designing an RDC interface, a discussion of RDC architecture that is based on a digital tracking loop, and special design considerations are covered for an EV application. Also included is a performance comparison of the PGA411-Q1 with RDC architecture versus a 19-bit optical encoder.

Resolver-to-digital conversion principle

As shown in Figure 1, a resolver sensor has one rotor winding (R1-R2) with the exciter sine wave that is AC-coupled to two stator windings. The stator windings, a sine coil (S2-S4) and a cosine coil (S1-S3), are mechanically positioned 90 degrees out-of-phase. As the rotor spins, the rotor position angle (Θ) changes with respect to the stator windings. The rotor and stator windings have a turns ratio in the order of 30%. The resulting amplitude-modulated signals shown in Figure 1 are typical resolver output signals. These signals must be gained, demodulated and post processed to extract angle and velocity information.

Figure 1. Representation of resolver signals: exciter, sine, and cosine



RDC architecture

Figure 2 shows an RDC architecture that converts analog resolver signals into digital angle and velocity outputs. The analog front end (AFE) consists of programmable gain amplifiers and a comparator. The AFE block conditions the output signals of the resolver by removing noise, sets correct input DC bias, and appropriately gains up the AC signal to be used by the subsequent blocks. A digital feedback loop is the main part of the RDC conversion. It starts by assuming a digital angle, phi. This angle is digitally processed using the sine and cosine lookup tables stored in memory. This in turn is fed to the corresponding sine and cosine digital-to-analog converters (DACs). The DAC outputs are multiplied with the amplitude-modulated resolver signals (Equations 1 and 2), which are the sine and cosine inputs to the RDC.

$$\text{Resolver sensor sine signal} = \sin \Theta \times \sin \omega t \quad (1)$$

$$\text{Resolver sensor cosine signal} = \cos \Theta \times \sin \omega t \quad (2)$$

where Θ = resolver shaft angle and ω = excitation frequency applied at R1-R2.

The main objective of the RDC architecture is to calculate the rotation angle (Θ) and the velocity of the resolver shaft. As shown in Figure 1, angular position information is extracted from the envelope or voltage peaks of the input sine and cosine signals. In order to calculate the angle, sine Θ is multiplied by a feedback signal (cosine φ), where φ is the assumed angle resulting from the lookup table in the memory. Similarly, cosine Θ is multiplied by the feedback signal (sine φ). The purpose of this multiplication is to solve the general formula:
$(\sin A \times \cos B) - (\sin B \times \cos A)$ and create $\sin (A - B)$.

$$\begin{aligned}\varepsilon_{pulse} &= \sin (A - B), \text{ or} \\ &= (K \times \sin \Theta \times \sin \omega t \times \cos \varphi) \\ &\quad - (K \times \cos \Theta \times \sin \omega t \times \sin \varphi) \quad (3) \\ \varepsilon_{pulse} &\equiv K \times \sin \omega t \times (\sin \Theta \times \cos \varphi - \cos \Theta \times \sin \varphi) \\ &= K \times \sin \omega t \times \sin (\Theta - \varphi)\end{aligned}$$

where φ = approximation of the resolver angle and K = a constant.

The output of the differential comparator is in digital form and is directly fed into the digital blocks to eliminate the carrier wave or the $\sin \omega t$ component with a synchronous detection circuit. This synchronous detection block uses the exciter feedback signal as the reference. The resulting output, $V_{\varphi ERR}$, goes into the digital tracking control loop to generate the desired angle output.

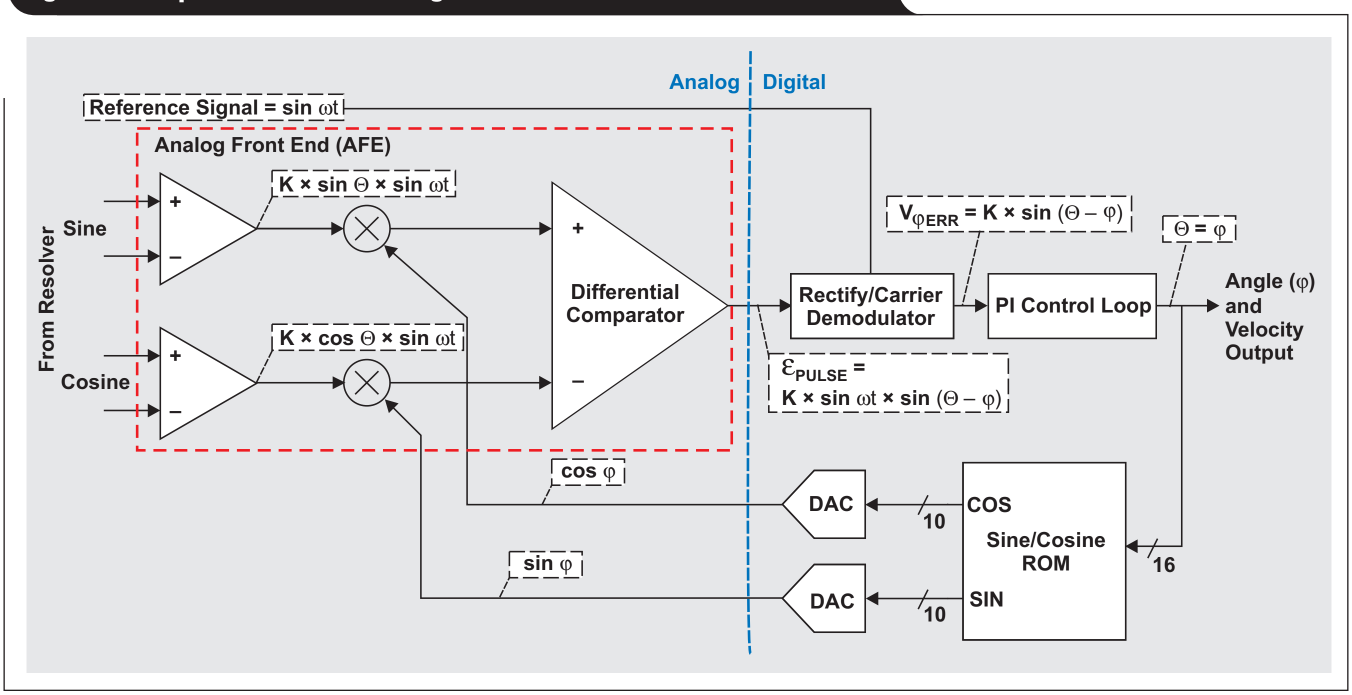
$$V_{\varphi ERR} = K \times \sin (\Theta - \varphi) \quad (4)$$

The negative feedback of the control-loop configuration employed in this RDC architecture helps to continuously reduce the $V_{\varphi ERR}$ signal to be very close to zero. For small values of $\Theta - \varphi$, $V_{\varphi ERR}$ is very near zero. Thus, the digital feedback loop continuously corrects itself, making the error close to zero so that the assumed RDC output angle (φ) is equal to the resolver shaft angle (Θ).

As shown in Figure 2, the $V_{\varphi ERR}$ signal is fed into a PI-control loop (Type II direct servo loop). Many control topologies for implementing loop tracking are possible.

One of the commonly used feedback control configurations is known as integral action.[3, 4] The advantage of this control configuration is its ability to reduce the steady-state tracking error to nearly zero. However, precautions must be taken because slightly excessive integral gain can cause oscillations in the system or even instability. This

Figure 2. Simplified resolver-to-digital converter (RDC) architecture



issue is addressed by adding another widely used proportional control known as proportional plus integral control (PI).

PI control is typically implemented as shown in Figure 3.[5] It helps bring steady-state error to zero and has improved transient response. Because of the added benefit of proportional control, it also does not cause any offset and leads to faster response than integral control alone.

Example application: Electric vehicle

Motor control action is an integral part of an EV. Communicating the motor position information accurately and quickly is essential. The resolver attached to a motor shaft tends to change its output very quickly. Hence, the RDC architecture must be designed to follow this change. Typically, the most critical component of the RDC architecture that determines how fast this can happen is the digital tracking loop.

To determine the behavior of the tracking loop, it is important to understand a key term, settling time. When the resolver output signal changes rapidly, the converter's step response is determined by the phase margin and gain margin of the control loop.[3] Settling time is a quick performance indicator of the RDC's control system. Figure 4 shows a settling-time example of an RDC feedback control system with a step-input change shown in black. The blue signal shows normal-mode response for the circuit in Figure 3 and the red signal shows response during acceleration mode (rapid change in angle), which is described on the following page.

Figure 3. Example of a PI control loop

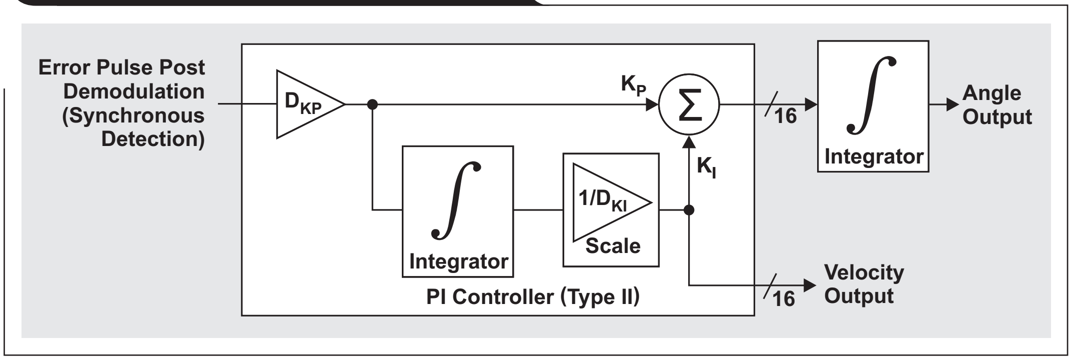
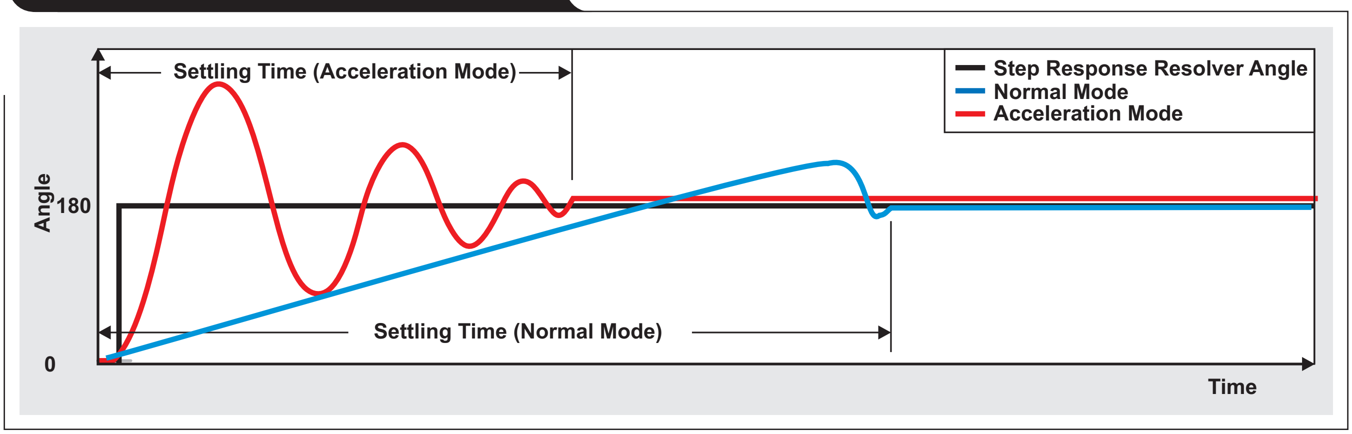


Figure 4. RDC step-response settling time



In order to follow the rotation angle under rapidly changing conditions, another loop-acceleration block is added in Figure 5 that can change the control-loop feedback gain. The higher-gain option helps the control loop to track a fast rotation angle much easier. In the acceleration mode (red signal in Figure 4), the proportional gain is increased by several times compared to the normal mode. Several diagnostic features are also added to alert the system if the signal integrity of the exciter and sine/cosine coils have been compromised.

Error sources that affect system accuracy

The errors can be categorized into three groups:

Group 1: Resolver sensor placement

- Sensor's mechanical construction: Static error is generated by manufacturing variations.
- Coil imbalance: The output voltages of the sine and cosine coils could be imbalanced and result in an error.
- Misalignment of resolver sensor: The resolver may be incorrectly mounted and lead to static error in the system.

Group 2: RDC architecture

The RDC architecture can cause static and dynamic errors in the system. The time delay from the input of the resolver signal to the output of the angle data also can cause errors in the system. For example, the input filter is used to decouple noise from the system. The delay caused by the filter circuit or the filter time constant may result in angular displacement during high-speed resolver operation. Therefore, be careful when selecting any common-mode capacitors that are added to the circuit to filter out noise. These common-mode capacitors can significantly affect phase relationship of the resolver signals and cause an imbalance between sine and cosine outputs, which can cause an error in the RDC output angle.

In addition, offset drifts in the AFE and linearity of the DACs can significantly affect the accuracy of the converted angle.

Group 3: Environmental factors

The external magnetic field from the motor-control circuit and high-voltage support in the EV can affect the resolver sensor's magnetic-coupling action and cause an error. Cable shielding is commonly used to prevent resolver signals from becoming affected, along with filter design at the input of the resolver converter to cut off any unwanted signals. The ability of the RDC architecture to reject common-mode noise is critical. Otherwise, the noise shows up on the signal-to-noise floor of the RDC, affecting the signal-to-noise ratio (SNR) and total harmonic distortion (THD) performance.

Figure 5. PI control with acceleration block

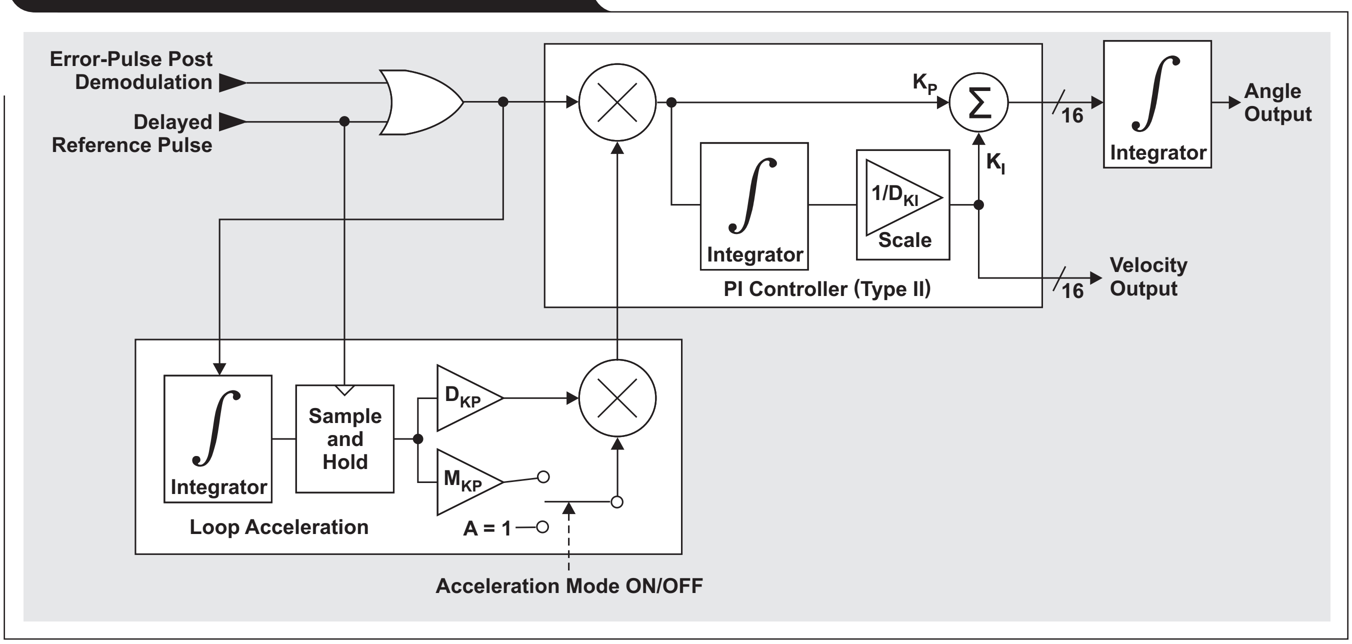
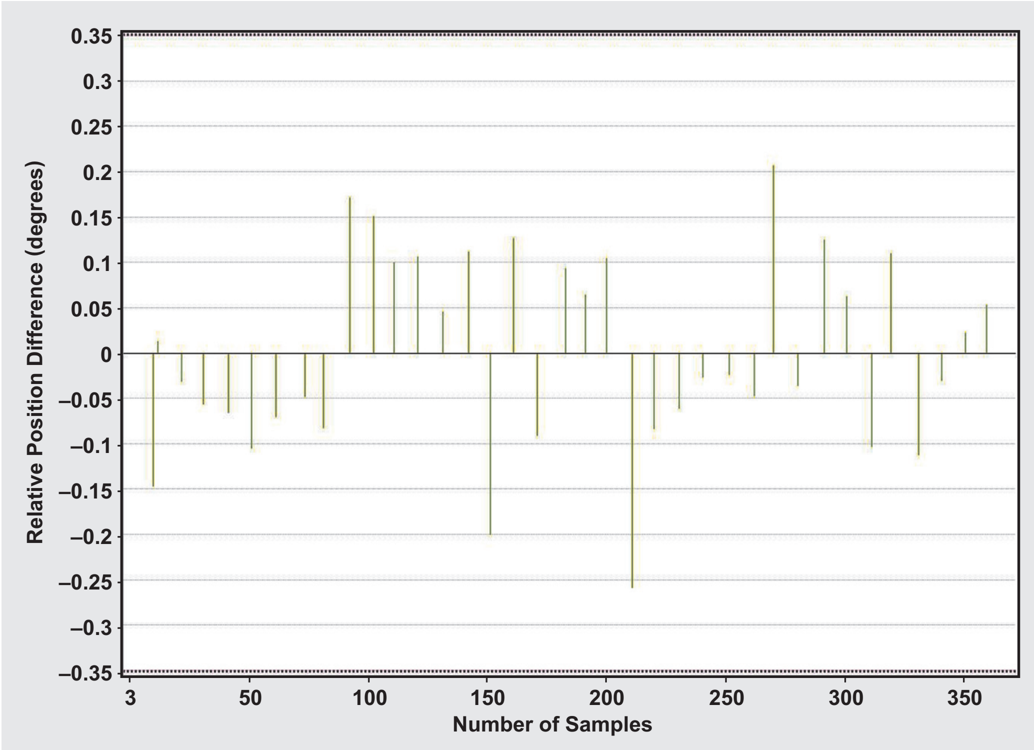


Figure 6. Measured RDC performance compared to a 19-bit optical encoder



RDC performance versus a 19-bit optical encoder

To better understand the performance of the resolver system, the results of a 12-bit RDC were compared to a 19-bit optical encoder. The mechanical set up included an example resolver and optical encoder mounted on the same shaft. Relative position difference was measured and plotted (Figure 6). The relative difference rules out any common-mode noise in the system that may cause the absolute values to misalign. The errors between the absolute angle deviation of the measured 16-bit RDC and the 19-bit optical encoder are less than ±0.25 degrees.

Acknowledgement

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Related Web sites

Product information:
PGA411-Q1
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