Charged-Coupled Devices (CCD) and CMOS Imagers in Space: Signal Processing Challenges and Solutions

The analog outputs of CCD and CMOS imaging chips, used in space applications such as earth observation or star tracking, require signal conditioning and digitization for processing by an FPGA or ASIC. In space, there are special challenges such as power, weight, temperature range, reliability and radiation environment. An Analog Front End (AFE), such as the LM98640QML-SP (5962R1820301VXC), is a solution to these challenges.

CCD Output Signal and Correlated Double Sampling (CDS)

A typical CCD output signal is shown in Figure 1 where the y-axis is voltage and the x-axis is time. A pixel period starts with a reset pulse, followed by a reference or black level signal, and then the actual data or video signal level. The amount of light sensed is the difference between the reference and data levels. The reference level may not be the same from pixel to pixel and variations in the reset pulse can cause additional noise in that level. It may be necessary to measure the reference level in each pixel period to produce an accurate output for each pixel.

One solution for processing CCD signals is correlated double sampling (CDS) where the reference level and data levels are individually sampled and the difference is outputted for further processing (Figure 1).

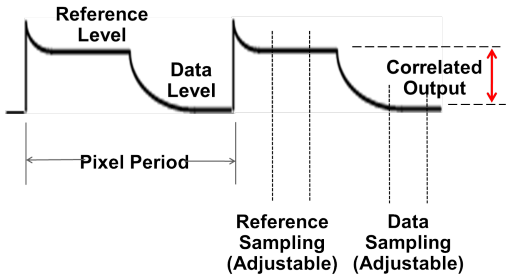

Figure 1. CCD Output and Correlated Doubling Sampling

Since the output of an imaging sensor is not a simple static signal it is necessary to be able to adjust the sampling window length and position based on the output curve. If CDS is used, two adjustable sampling windows are required as shown in Figure 1.

Post CDS, but prior to digitizing, there may be additional offsets between sensors that must be compensated before gaining the signal to match the dynamic range of the analog-to-digital converter (ADC).

Special Requirements and Challenges for Space Applications

Most space applications require higher reliability components than normal commercial applications. The temperatures can range from -55°C to +125°C. Rugged, hermetic packaging can be required. Components used in space must survive cosmic radiation. Also of concern for space applications is power consumption and weight.

Perhaps the biggest challenge to designing a space imaging system is that there are relatively few components available that are qualified for space systems and can withstand the cosmic radiation. Even many space grade products are not radiation tolerant and require extra mitigation for radiation effects. A product that is not total ionizing dose (TID) tolerant may require extra shielding. Many CMOS ADCs will experience single event latch-up (SEL) where a heavy ion strike from cosmic radiation can cause the part to go into a latch-up state drawing enough current to destroy the part. In these cases, over current detection and reset circuits must be added to the system.

A discrete solution for digitizing an image sensor's analog output using available space grade, radiation tolerant products would require a number of individual components and compromises. The use of space grade products in hermetic packaging will add weight to the system and require significantly more board space. The additional trace lengths and wiring add noise to the system and degrade the performance.

To do CDS either two sample-and-hold circuits or two ADCs are required, or the sampling must be run at double the pixel rate to do CDS in the digital domain. Any of these options will result in additional error in the CDS calculation.

AFE Solution

An Analog Front End (AFE) is a highly integrated ADC that contains the circuitry for conditioning the imaging signal prior to digitization. Figure 2 is a block diagram for the dual channel LM98640QML-SP designed for space imaging applications. Each channel has a 14b ADC with an input range of 2 V.

The first section of the AFE is the track and hold, capable of performing CDS. In the block diagram, only a single input (OS-) will be active for each channel. For low input signals, the LM98640 has the option of a 2X gain by doubling of the track and hold capacitor arrays. The sampling windows are adjustable to 1/64 of the pixel period.

The LM98640 can also be programmed to clamp on the reference level at the beginning of a pixel column.

Any systemic offsets in the CCD sensors can be corrected by applying the fine and course DACs. There is also a programmable gain amplifier (PGA) to amplify the signal to match the dynamic range of the on chip ADCs.

Finally, the digitized output of the ADCs are serialized for input to an FPGA or ASIC. The serializer has the option of running on two or four lanes. In four lane mode the data rate on each lane is halved to accommodate slower FPGAs or ASICs.

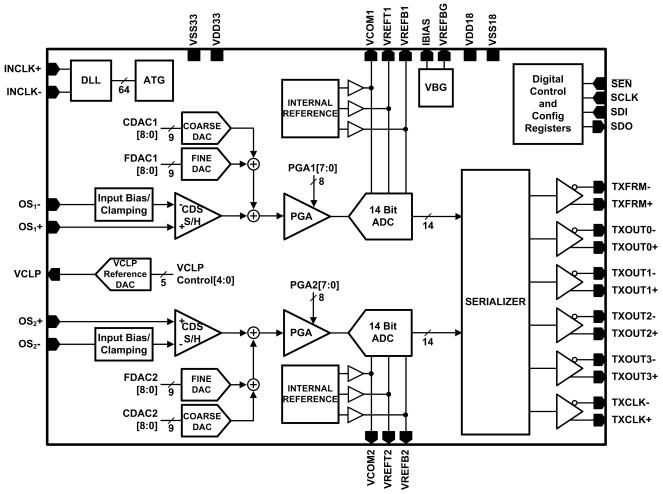

Figure 2. LM98640 Block Diagram

Advantages of the LM98640QML-SP Solution

With an AFE, all components are moved to a single chip. This reduces the weight and the power consumption of the system. The total power consumption of the LM98640QML-SP at 15 MSPS is only 125 mW per channel.

With all the components integrated, the signal path has shrunk improving the performance of the system. CDS is now done in the analog domain, using a single track and hold circuit resulting in less noise. The total noise flow of the LM98640QML-SP is -79 dB typical.

A major advantage of using an AFE is that it can be mounted on the focal plane board, moving the signal digitization close to the CCD, greatly reducing the analog signal path, reducing the noise and improving the system performance. Figure 3 compares an old solution to one that was replaced by the LM98640.

Solutions for CMOS Imagers

There is a wider variety in the output signals in CMOS imaging ICs. On some CMOS imaging chips, the output signal is very similar to that of a CCD. In some cases, the reference level is lower than the signal level. In many cases, the reference level is fairly consistent and does not need to be individually measured on each pixel. On some CMOS imagers, some or all of the signal processing has been integrated on the chip so that less downstream processing is required.

Typically, CDS is not required for a CMOS imager, but the video signal does need to be compared to a fixed reference voltage. The LM98640 has the flexibility to also support most CMOS imaging sensors. In cases where CDS is not required, the LM98640 can be configured in “sample-and-hold” or pseudo differential mode. In this case both inputs (OS- and OS+) now become active and one of the inputs is used as a reference. The reference voltage can be supplied by the on chip DAC ("VCLP Reference DAC" in Figure 2).

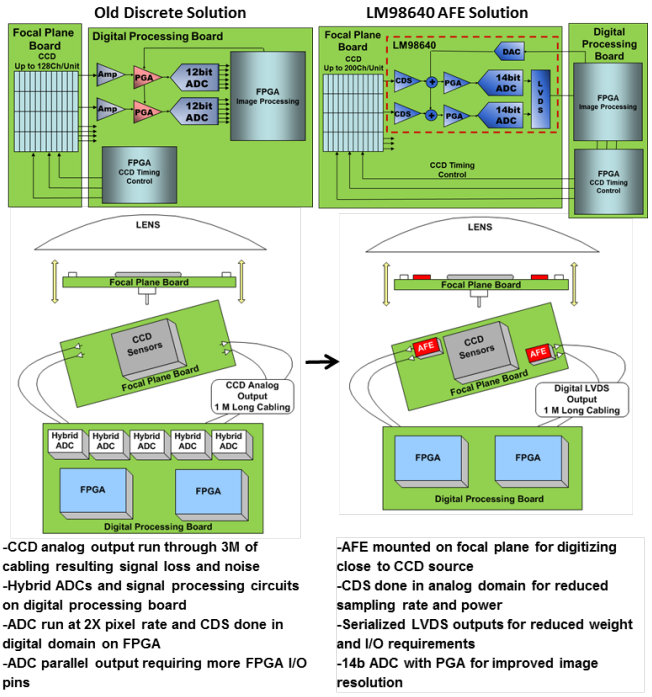

Figure 3. Discrete Solution vs AFE Solution

Summary

The LM98640QML-SP is a fully qualified, space grade, RHA QMLV AFE with the flexibility to support signal conditioning and digitization of CCD and CMOS imager outputs at pixel rates from 5 MHz to 40 MHz. It comes in a thermally enhanced ceramic quad flatpack power package and is rated from -55°C to +125°C. It is qualified to 100 krad(Si) and is single event latch-up (SEL) and single event functional interrupt (SEFI) immune. It has an internal delayed lock loop (DLL) clocking system that self recovers in one clock cycle from an ion strike. The flight grade LM98640QML-SP is orderable under the SMD number 5962R1820301VXC.

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