Latching a Voltage Supervisor (Reset IC)

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Introduction

The normal operation of a voltage supervisor (also called a reset IC) is to monitor a voltage rail and activate the $\overline{\text{RESET}}$ output to logic low for active-low devices when the voltage rail being monitored drops below a defined voltage threshold. When the voltage rail being monitored rises back above the threshold, traditional voltage supervisors deactivate this output by pulling the output high for active-low devices, signaling a normal condition.

This under-voltage event, however, could require further review before the system is allowed to resume. In such cases, the output must stay latched in the fault state even if the monitored voltage rail rises back up above the threshold. In order to clear this latched state, user intervention is required.

Such a requirement can often be found in industrial applications (e.g., motor drive, servo drive, PLC) and automotive safety critical applications to meet SIL or ASIL safety ratings. As applications require higher safety ratings, such as SIL3, PLe, CAT3, or higher, the mean time between dangerous failure ($MTTF_D$) must be high. This can be accomplished by using a monitoring solution that latches when a fault is detected until the fault is known to be fixed for example.

Latching a Supervisor Circuit

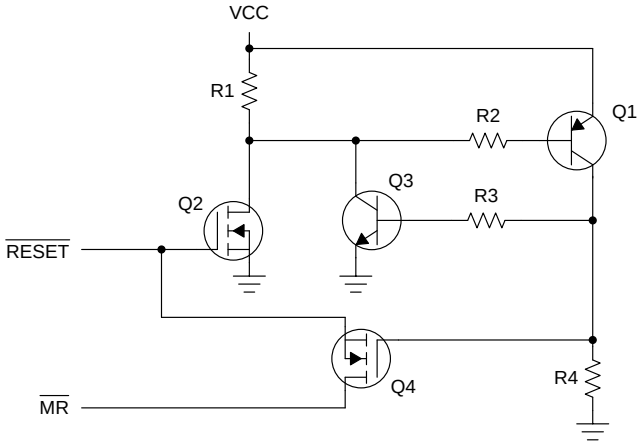

Figure 1. External Latch Circuitry

One way to implement such a solution is by using a supervisor with a manual reset ($\overline{\text{MR}}$) input and a voltage-sense output (called $\overline{\text{RESET}}$ for this particular device) in conjunction with external latch circuitry. The latch circuitry includes four active components (two N-Channel MOSFETs, one NPN transistor, and one PNP transistor) along with four resistors as shown in Figure 1.

This circuit configuration uses Q1 (PNP) and Q3 (NPN) transistors to create a latch, Q2 (N-MOSFET) to activate the latch after $\overline{\text{RESET}}$ goes high the first time, and Q4 (N-MOSFET) to utilize the $\overline{\text{MR}}$ pin to keep the device in a latched state.

When voltage rail V_{DD} ramps up and crosses V_{IT} (voltage threshold of the supervisor) for the first time, 3 events happen:

1. The $\overline{\text{MR}}$ pin pulls high by an internal pull-up resistor in the supervisor. This is the default logic level for $\overline{\text{MR}}$.
2. $\overline{\text{RESET}}$ will pull high to V_{DD}. This turns on Q2 which creates a voltage potential across R1 setting a voltage across the base-emitter junction of Q1 turning the transistor on. With Q1 turned on, a voltage potential is created across R4 that turns on Q3. Q3 will conduct current through R1 keeping Q1 turned on, regardless of the state of Q2. This creates a latch because Q1 and Q3 remain on regardless of the logic level of $\overline{\text{RESET}}$.
3. The voltage across R4 also sets up a voltage potential at the gate of Q4 but Q4 does not turn on until an undervoltage fault causes $\overline{\text{RESET}}$ to pull logic low. When a fault does occur and $\overline{\text{RESET}}$ pulls to logic low, this creates enough gate-to-source potential on Q4 to turn the transistor on.

When an under voltage event occurs, $\overline{\text{RESET}}$ pulls low effectively connecting the source pin of Q4 to GND through the internal output MOSFET inside the voltage supervisor. This sets enough gate-to-source voltage across Q4 to turn it on, connecting $\overline{\text{RESET}}$ to $\overline{\text{MR}}$ via Q4. Because the $\overline{\text{MR}}$ pin is connected to $\overline{\text{RESET}}$ via Q4 and $\overline{\text{RESET}}$ is connected to GND via the internal MOSFET, $\overline{\text{RESET}}$ can not go back logic high, even if the voltage rail rises back above the threshold, keeping the circuit in a latched state. Figure 2 shows a simplified block diagram of the $\overline{\text{RESET}}$ and $\overline{\text{MR}}$ interaction with the latch block and the internals of the voltage supervisor to provide additional detail.

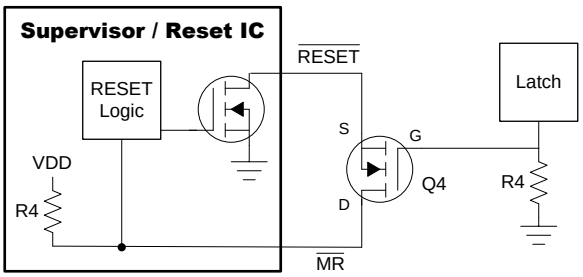

Figure 2. Voltage Supervisor Operation with Latch

Removing this circuit from a latched state can only happen in two ways - to reset the circuit or manually unlatch the output. The first way is to drop the supply voltage (VDD) of the system so that either Q3 or Q1 transistors turn off thus deactivating their latched state. This releases the voltage potential across R4 at the gate of Q4 which disconnects the $\overline{MR}$ pin from $\overline{RESET}$ pin which is logic low during this time. Another way is by utilizing a switch to open the gate at Q4 to manually release the $\overline{MR}$ pin from being connected to $\overline{RESET}$ pin. In either case, a disconnection must occur between $\overline{RESET}$ and $\overline{MR}$ to allow the voltage supervisor to operate normally without latching functionality.

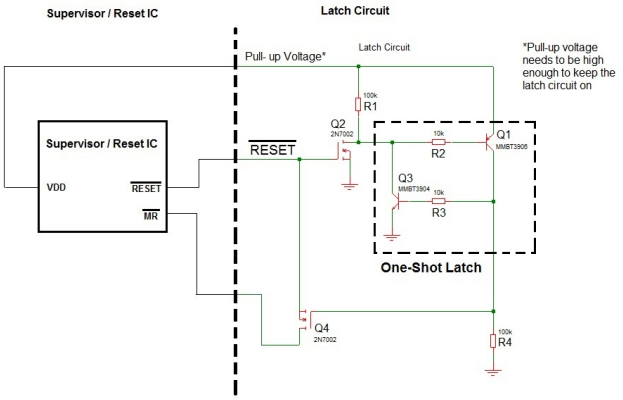

Figure 3. Voltage Supervisor Latch Circuit

Figure 3 shows the complete solution which uses a Texas Instruments supervisor with a manual reset ($\overline{MR}$) feature such as the TPS3890. By connecting the external circuit shown in Figure 1 to the TPS3890, the $\overline{RESET}$ output of the TPS3890 will now be a latching reset output.

Figure 4 shows the timing diagram of the normal operation without the latch circuitry and the latched operation with the latch circuitry. Notice that the $\overline{RESET}$ signal returns to logic high when SENSE rises above V_{INP} during normal operation but remains logic low during latched operation until the device is powered down then powered up.

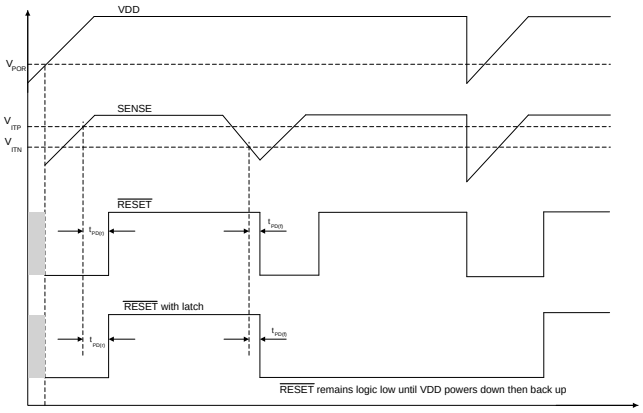

Figure 4. Normal vs Latched Operation Timing Diagram

Latching a Window Voltage Supervisor

A latching feature is provided in the window voltage supervisor, TPS3703-Q1, as shown in Figure 5. The TPS3703-Q1 features a voltage latch mode on the $\overline{RESET}$ pin when connecting the CT pin to ground. In the latch mode, the $\overline{RESET}$ pins remains low once it triggers to active logic low state regardless of the V_{SENSE} pin status. Putting TPS3703-Q1 into latch mode by connecting the CT pin to ground does not initiate a fault condition or activate the $\overline{RESET}$ pin to logic low, but only causes the $\overline{RESET}$ pin to latch logic low once a fault does occur. To unlatch the device, provide a voltage to the CT pin that is greater than the CT pin threshold voltage, V_{CT}. To ensure the device is out of latch mode, provide at least 1.2 V to CT pin. A pull-down resistor along with a series resistor on the CT pin are recommended to limit current consumption of the system.

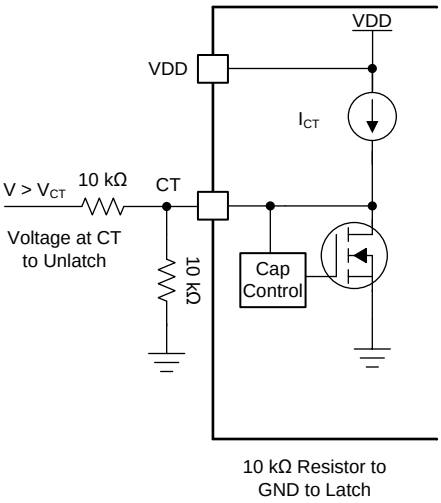

Figure 5. TPS3703-Q1 Window Voltage Supervisor Latch Feature

Figure 6 shows the latching functionality. As the voltage at the SENSE pin ramps up from 0V, the $\overline{\text{RESET}}$ output initially indicates a fault because the TPS3703-Q1 is in undervoltage condition. Once the SENSE voltage rises above the undervoltage threshold plus hysteresis ($V_{IT-(UV)}$ + V_{HYS}) of TPS3703-Q1, the $\overline{\text{RESET}}$ output indicates no fault because SENSE is in the acceptable voltage range. Once the SENSE voltage rises above the overvoltage threshold ($V_{IT+(OV)}$), the $\overline{\text{RESET}}$ output indicates a fault again and since the CT pin is grounded during this time due to external control circuitry, this fault condition remains latched even after the SENSE voltage enters the acceptable voltage range. The $\overline{\text{RESET}}$ output remains latched until the voltage at the CT pin is allowed to rise up again above the internal CT pin reference voltage (V_{CT}) by disconnecting the CT pin from the control circuitry that holds the CT pin logic low.

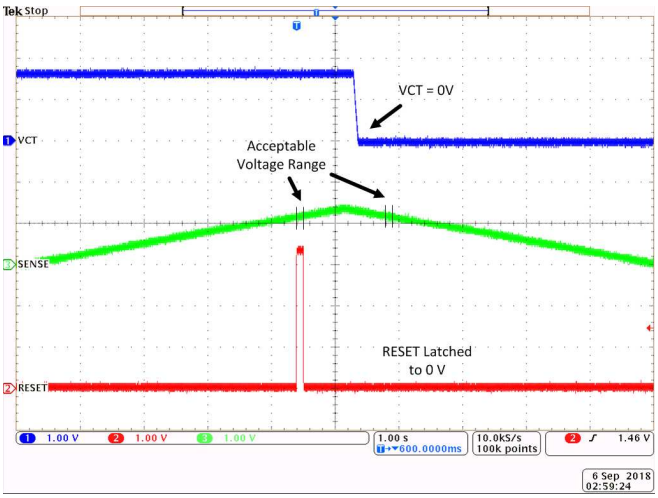

Figure 6. Fault Causing Latching Functionality

Table 1. Alternative Device Recommendations

Device	Description
TPS3808	Low Iq, High Accuracy, Programmable time delay, SOT package type
TPS3831	150uA Nano-Iq, X2SON (1mm x 1mm) small footprint size
TPS389x	1% Accuracy, Programmable time delay, Multiple voltage variants and topologies, USON (1.45mm x 1mm) small footprint size
TPS3703-Q1	High Accuracy Overvoltage and Undervoltage Reset IC with Time Delay and Manual Reset

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