1 特長

1.1 12、14、16ビットでピンおよびソフトウェア互換のADCファミリ
1.2 チャネルごとの最大データ転送速度:
- ADS8528: 650kSPS (PAR) または 480kSPS (SER)
- ADS8548: 600kSPS (PAR) または 450kSPS (SER)
- ADS8568: 510kSPS (PAR) または 400kSPS (SER)

1.3 優れたAC特性
- 信号対雑音比: ADS8528: 73.9dB、ADS8548: 85dB、ADS8568: 91.5dB
- 全高調波歪み: ADS8528: -89dB、ADS8548: -91dB、ADS8568: -94dB

1.4 プログラム可能なバッファ付き内部基準電圧: 0.5V～2.5Vまたは0.5V～3.0Vで、±12Vまでの入力電圧範囲をサポート

1.5 パラレルまたはシリアルのインターフェイスを選択可能

1.6 自動スリープ・モードの使用によるスケーリングな低消費電力動作: 10kSPSでわずか32mW

2 アプリケーション

2.1 保護リレー
2.2 電力品質測定
2.3 多軸モータ制御
2.4 プログラマブル・ロジック・コントローラ
2.5 工業用データ収集

3 概要

ADS85x8は、低消費電力で12、14、16ビットの8つの逐次比較型(SAR)アナログ/デジタル・コンバータ(ADC)が搭載されており、真のバイポーラー入力を受け付けます。これら12と16ビットの4つのパラメータがグループ化されているため、最大650kSPSの高速な信号を同時に取得できます。

これらのデバイスはパラレルまたはシリアルのインターフェイスを選択でき、デイジー・チェーン機能に対応します。基準電圧をプログラム可能ため、最大±12Vの振幅でアナログ入力を処理できます。

ADS85x8は、自動スリープ・モードをサポートして消費電力を最小限に抑えており、64ピンのVQFNおよびLQFPパッケージで供給されます。ファミリのすべての製品は、-40℃〜+125℃の温度範囲で動作が規定されています。

製品情報(1)

<table>
<thead>
<tr>
<th>型番</th>
<th>パッケージ</th>
<th>本体サイズ(公称)</th>
</tr>
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<tbody>
<tr>
<td>ADS85x8</td>
<td>VQFN (64)</td>
<td>9.00mm×9.00mm</td>
</tr>
<tr>
<td></td>
<td>LQFP (64)</td>
<td>10.00mm×10.00mm</td>
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</tbody>
</table>

(1) 提供されているすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

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4 改訂履歴
資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision B (November 2015) から Revision C に変更

<table>
<thead>
<tr>
<th></th>
<th>Page</th>
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<tr>
<td>• Changed Figure 45: changed capacitor values from 820 nF to 820 pF</td>
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</table>

Revision A (October 2011) から Revision B に変更

<table>
<thead>
<tr>
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<th>Page</th>
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<tr>
<td>• 「ESD定格」表、「推奨動作条件」表、「機能説明」セクション、「デバイスの機能モード」セクション、「レジスタ・マップ」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加</td>
<td>1</td>
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<tr>
<td>• Changed title of Device Comparison Table, deleted footnote 1</td>
<td>4</td>
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<tr>
<td>• Added Storage temperature parameter to Absolute Maximum Ratings table</td>
<td>9</td>
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<tr>
<td>• Changed Clock cycles per conversion to be a single parameter instead of part of ( f_{\text{CONV}} ) parameter in Serial Interface Timing Requirements table</td>
<td>16</td>
</tr>
<tr>
<td>• Changed ( t_{\text{LENS}} ) parameter in Serial Interface Timing Requirements table</td>
<td>16</td>
</tr>
<tr>
<td>• Added footnote 3 to Serial Interface Timing Requirements table</td>
<td>16</td>
</tr>
<tr>
<td>• Changed Clock cycles per conversion to be a single parameter instead of part of ( f_{\text{CONV}} ) parameter in Parallel Interface Timing Requirements (Read Access) table</td>
<td>17</td>
</tr>
<tr>
<td>• Changed ( t_{\text{BUS}} ) parameter in Parallel Interface Timing Requirements (Read Access) table</td>
<td>17</td>
</tr>
<tr>
<td>• Added footnote 3 to Parallel Interface Timing Requirements (Read Access) table</td>
<td>17</td>
</tr>
<tr>
<td>• Changed Data Readout and BUSY/INT Signal section</td>
<td>30</td>
</tr>
<tr>
<td>• Added Sequential Operation section</td>
<td>31</td>
</tr>
<tr>
<td>• Changed description of initiating a new conversion in Reset and Power-Down Modes section</td>
<td>38</td>
</tr>
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</table>
2011年8月発行のものから更新  

| Deleted INL column from Family/Ordering Information table | 4 |
| Changed DC Accuracy, INL parameter in ADS8568 Electical Characteristics table | 15 |

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5 Device Comparison Table

<table>
<thead>
<tr>
<th>PRODUCT</th>
<th>RESOLUTION (Bits)</th>
<th>MAXIMUM DATA RATE: PAR, SER (kSPS per Channel)</th>
<th>SNR (dB, Typ)</th>
<th>THD (dB, Typ)</th>
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<tbody>
<tr>
<td>ADS8528</td>
<td>12</td>
<td>650, 480</td>
<td>73.9</td>
<td>–89</td>
</tr>
<tr>
<td>ADS8548</td>
<td>14</td>
<td>600, 450</td>
<td>85</td>
<td>–91</td>
</tr>
<tr>
<td>ADS8568</td>
<td>16</td>
<td>510, 400</td>
<td>91.5</td>
<td>–94</td>
</tr>
</tbody>
</table>

6 Pin Configuration and Functions

![RGC Package 64-Pin VQFN Top View](image)

7.3-mm x 7.3-mm Exposed Thermal Pad
### PM Package
#### 64-Pin LQFP

**Top View**

<table>
<thead>
<tr>
<th>Pin</th>
<th>Description</th>
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<tbody>
<tr>
<td>1</td>
<td>HVSS</td>
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<tr>
<td>2</td>
<td>CH_D1</td>
</tr>
<tr>
<td>3</td>
<td>REFDN</td>
</tr>
<tr>
<td>4</td>
<td>AVDD</td>
</tr>
<tr>
<td>5</td>
<td>AGND</td>
</tr>
<tr>
<td>6</td>
<td>CH_D0</td>
</tr>
<tr>
<td>7</td>
<td>CH_A0</td>
</tr>
<tr>
<td>8</td>
<td>PAR/SER</td>
</tr>
<tr>
<td>9</td>
<td>STBY</td>
</tr>
<tr>
<td>10</td>
<td>RESET</td>
</tr>
<tr>
<td>11</td>
<td>REFEN/WR</td>
</tr>
<tr>
<td>12</td>
<td>RD</td>
</tr>
<tr>
<td>13</td>
<td>CS/FS</td>
</tr>
<tr>
<td>14</td>
<td>AVDD</td>
</tr>
<tr>
<td>15</td>
<td>AGND</td>
</tr>
<tr>
<td>16</td>
<td>DB15/SDO_D</td>
</tr>
<tr>
<td>17</td>
<td>DB14/SDO_C</td>
</tr>
<tr>
<td>18</td>
<td>DB13/SDO_B</td>
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<td>19</td>
<td>DB12/SDO_A</td>
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<td>20</td>
<td>DB11/REFBUFEN</td>
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<td>21</td>
<td>DB10/CLK</td>
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<td>DB9/SO</td>
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<td>DB8/DCEN</td>
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<td>DB6/SEL_B</td>
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<td>26</td>
<td>DB5/SEL_C</td>
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<td>27</td>
<td>DB4</td>
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<td>28</td>
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<td>DB1/DCIN_C</td>
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<td>31</td>
<td>DB0/DCIN_D</td>
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<td>32</td>
<td>HVD0</td>
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<tr>
<td>33</td>
<td>CH_A1</td>
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<tr>
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<td>REFAN</td>
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<td>AVDD</td>
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<td>CH_A1</td>
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<tr>
<td>48</td>
<td>HVD0</td>
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</tbody>
</table>

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**ADS8528, ADS8548, ADS8568**

[www.ti.com](http://www.ti.com)

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### Pin Functions

<table>
<thead>
<tr>
<th>PIN</th>
<th>TYPE(1)</th>
<th>NAME</th>
<th>NO.</th>
<th>PARALLEL INTERFACE (PAR/SER = 0)</th>
<th>SERIAL INTERFACE (PAR/SER = 1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>AGND</td>
<td>P</td>
<td>Analog ground; connect to the analog ground plane.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ASLEEP</td>
<td>DI</td>
<td>Auto-sleep enable input. When low, the device operates in normal mode. When high, the device functions in auto-sleep mode where the hold mode and the actual conversion is activated six conversion clock cycles after issuing a conversion start using a CONVST_x. This mode is recommended to save power if the device runs at a lower data rate; see the Reset and Power-Down Modes section for more details.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>AVDD</td>
<td>P</td>
<td>Analog power supply. Decouple according to the Power Supply Recommendations section.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>BUSY/INT</td>
<td>DO</td>
<td>When CONFIG bit C27 = 0 (BUSY/INT), this pin is a converter busy status output. This pin transitions high when a conversion is started and transitions low for a single conversion clock cycle (t_{CLK}) whenever a channel pair conversion is completed and stays low when the conversion of the last channel pair completes. When bit C27 = 1 (BUSY/INT in CONFIG), this pin is an interrupt output. This pin transitions high after a conversion completes and remains high until the next read access. This mode can only be used if all eight channels are sampled simultaneously (all CONVST_x tied together). The polarity of the BUSY/INT output can be changed using the C26 bit (BUSY L/H) in the Configuration register.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CH_A0</td>
<td>AI</td>
<td>Analog input of channel A0; channel A is the master channel pair that is always active. The input voltage range is controlled by the RANGE pin in hardware mode or by Configuration register (CONFIG) bit C24 (RANGE_A) in software mode. In cases where channel pairs of the device are used at different data rates, channel pair A must always run at the highest data rate.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CH_A1</td>
<td>AI</td>
<td>Analog input of channel A1; channel A is the master channel pair that is always active. The input voltage range is controlled by the RANGE pin in hardware mode or by CONFIG bit C24 (RANGE_A) in software mode. In cases where channel pairs of the device are used at different data rates, channel pair A must always run at the highest data rate.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CH_B0</td>
<td>AI</td>
<td>Analog input of channel B0. The input voltage range is controlled by the RANGE pin in hardware mode or by CONFIG bit C23 (RANGE_B) in software mode.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CH_B1</td>
<td>AI</td>
<td>Analog input of channel B1. The input voltage range is controlled by the RANGE pin in hardware mode or by CONFIG bit C23 (RANGE_B) in software mode.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CH_C0</td>
<td>AI</td>
<td>Analog input of channel C0. The input voltage range is controlled by the RANGE pin in hardware mode or by CONFIG bit C21 (RANGE_C) in software mode.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CH_C1</td>
<td>AI</td>
<td>Analog input of channel C1. The input voltage range is controlled by the RANGE pin in hardware mode or by CONFIG bit C21 (RANGE_C) in software mode.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CH_D0</td>
<td>AI</td>
<td>Analog input of channel D0. The input voltage range is controlled by the RANGE pin in hardware mode or by CONFIG bit C19 (RANGE_D) in software mode. This pin can be powered down using CONFIG bit C18 (PD_D) in software mode.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CH_D1</td>
<td>AI</td>
<td>Analog input of channel D1. The input voltage range is controlled by the RANGE pin in hardware mode or by CONFIG bit C19 (RANGE_D) in software mode. This pin can be powered down using CONFIG bit C18 (PD_D) in software mode.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CONVST_A</td>
<td>DI</td>
<td>Conversion start of channel pair A. The rising edge of this signal initiates simultaneous conversion of analog signals at inputs CH_A[1:0]. This signal resets the internal channel state machine that causes the data output to start with conversion results of channel A0 with the next read access.</td>
<td></td>
<td></td>
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</tr>
<tr>
<td>CONVST_B</td>
<td>DI</td>
<td>Conversion start of channel pair B. The rising edge of this signal initiates simultaneous conversion of analog signals at inputs CH_B[1:0].</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CONVST_C</td>
<td>DI</td>
<td>Conversion start of channel pair C. The rising edge of this signal initiates simultaneous conversion of analog signals at inputs CH_C[1:0].</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CONVST_D</td>
<td>DI</td>
<td>Conversion start of channel pair D. The rising edge of this signal initiates simultaneous conversion of analog signals at inputs CH_D[1:0].</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CS/FS</td>
<td>DI, DI</td>
<td>Chip-select input. When low, the parallel interface is enabled. When high, the interface is disabled. Frame synchronization. The FS falling edge controls the frame transfer.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DB0/DCIN_D</td>
<td>DIO, DI</td>
<td>Data bit 0 (LSB) input/output</td>
<td>When DCEN = 1 and SEL_CD = 1, this pin is the daisy-chain data input for SDO_D of the previous device in the chain. When DCEN = 0, connect to DGND.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DB1/DCIN_C</td>
<td>DIO, DI</td>
<td>Data bit 1 input/output</td>
<td>When DCEN = 1 and SEL_CD = 1, this pin is the daisy-chain data input for SDO_C of the previous device in the chain. When DCEN = 0, connect to DGND.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DB2/DCIN_B</td>
<td>DIO, DI</td>
<td>Data bit 2 input/output</td>
<td>When DCEN = 1 and SEL_B = 1, this pin is the daisy-chain data input for SDO_B of the previous device in the chain. When DCEN = 0, connect to DGND.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DB3/DCIN_A</td>
<td>DIO, DI</td>
<td>Data bit 3 input/output</td>
<td>When DCEN = 1, this pin is the daisy-chain data input for SDO_A of the previous device in the chain. When DCEN = 0, connect to DGND.</td>
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</tbody>
</table>

(1) AI = analog input; AIO = analog input/output; DI = digital input; DIO = digital input/output; DO = digital output; and P = power supply.
## Pin Functions (continued)

<table>
<thead>
<tr>
<th>PIN</th>
<th>TYPE(1)</th>
<th>DESCRIPTION</th>
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<tbody>
<tr>
<td><strong>NAME</strong></td>
<td><strong>NO.</strong></td>
<td><strong>PARALLEL INTERFACE (PAR/SER = 0)</strong></td>
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<td>DB4</td>
<td>29</td>
<td>DIO Data bit 4 input/output</td>
</tr>
<tr>
<td>DB5/SEL_CD</td>
<td>28</td>
<td>DIO, DI Data bit 5 input/output</td>
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<td></td>
</tr>
<tr>
<td>DB6/SEL_B</td>
<td>27</td>
<td>DIO, DI Data bit 6 input/output</td>
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<tr>
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<td>DB7</td>
<td>26</td>
<td>DIO Data bit 7 input/output</td>
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<tr>
<td>DB8/DCEN</td>
<td>23</td>
<td>DIO, DI Data bit 8 input/output</td>
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<td></td>
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<tr>
<td>DB9/SDI</td>
<td>22</td>
<td>DIO, DI Data bit 9 input/output</td>
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<tr>
<td>DB10/SCLK</td>
<td>21</td>
<td>DIO, DI Data bit 10 input/output</td>
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<tr>
<td>DB11/REFBUFEN</td>
<td>20</td>
<td>DIO, DI Data bit 11 input/output. Output is MSB for the ADS8528.</td>
</tr>
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<tr>
<td>DB12/SDO_A</td>
<td>19</td>
<td>DIO, DO Data bit 12 input/output. Output is sign extension for the ADS8528.</td>
</tr>
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<tr>
<td>DB13/SDO_B</td>
<td>18</td>
<td>DIO, DO Data bit 13 input/output. Output is sign extension for the ADS8528 and SDOB for the ADS8548.</td>
</tr>
<tr>
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<tr>
<td>DB14/SDO_C</td>
<td>17</td>
<td>DIO, DO Data bit 14 input/output. Output is sign extension for the ADS8528 and SDOB for the ADS8548.</td>
</tr>
<tr>
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</tr>
<tr>
<td>DB15/SDO_D</td>
<td>16</td>
<td>DIO, DO Data bit 15 (MSB) input/output. Output is sign extension for the ADS8528 and SDOB for the ADS8548.</td>
</tr>
<tr>
<td></td>
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<tr>
<td>DGND</td>
<td>24</td>
<td>P Buffer I/O ground, connect to digital ground plane</td>
</tr>
<tr>
<td>DVDD</td>
<td>25</td>
<td>P Buffer I/O supply, connect to digital supply.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>HVDD</td>
<td>48</td>
<td>P Positive supply voltage for the analog inputs.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>HVSS</td>
<td>1</td>
<td>P Negative supply voltage for the analog inputs.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>HW/SW</td>
<td>41</td>
<td>DI Mode selection input.</td>
</tr>
<tr>
<td></td>
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</tr>
<tr>
<td>PAR/SER</td>
<td>8</td>
<td>DI Interface mode selection input.</td>
</tr>
<tr>
<td></td>
<td></td>
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</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>RANGE/XCLK</td>
<td>34</td>
<td>DI/DI/DO Hardware mode (HW/SW = 0): analog input voltage range select input.</td>
</tr>
<tr>
<td></td>
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</tr>
<tr>
<td>RD</td>
<td>12</td>
<td>DI/DI Read data input.</td>
</tr>
<tr>
<td></td>
<td></td>
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</tr>
<tr>
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</tr>
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</table>

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### Pin Functions (continued)

<table>
<thead>
<tr>
<th>PIN</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>NAME</strong></td>
<td><strong>NO.</strong></td>
<td><strong>PARALLEL INTERFACE (PAR/SER = 0)</strong></td>
</tr>
<tr>
<td>REFAN</td>
<td>46</td>
<td>Al Decoupling capacitor input for reference of channel pair A. Connect to the decoupling capacitor and AGND according to the Power Supply Recommendations section.</td>
</tr>
<tr>
<td>REFAP</td>
<td>43</td>
<td>Al Decoupling capacitor input for reference of channel pair A. Connect to the decoupling capacitor according to the Power Supply Recommendations section.</td>
</tr>
<tr>
<td>REFBN</td>
<td>53</td>
<td>Al Decoupling capacitor input for reference of channel pair B. Connect to the decoupling capacitor and AGND according to the Power Supply Recommendations section.</td>
</tr>
<tr>
<td>REFBP</td>
<td>50</td>
<td>Al Decoupling capacitor input for reference of channel pair B. Connect to the decoupling capacitor according to the Power Supply Recommendations section.</td>
</tr>
<tr>
<td>REFCN</td>
<td>60</td>
<td>Al Decoupling capacitor input for reference of channel pair C. Connect to the decoupling capacitor and AGND according to the Power Supply Recommendations section.</td>
</tr>
<tr>
<td>REFCP</td>
<td>63</td>
<td>Al Decoupling capacitor input for reference of channel pair C. Connect to the decoupling capacitor according to the Power Supply Recommendations section.</td>
</tr>
<tr>
<td>REFDN</td>
<td>3</td>
<td>Al Decoupling capacitor input for reference of channel pair D. Connect to the decoupling capacitor and AGND according to the Power Supply Recommendations section.</td>
</tr>
<tr>
<td>REFDP</td>
<td>6</td>
<td>Al Decoupling capacitor input for the channel pair D reference. Connect to the decoupling capacitor according to the Power Supply Recommendations section.</td>
</tr>
<tr>
<td><strong>REFEN/WR</strong></td>
<td><strong>11</strong></td>
<td>Di/Di Hardware mode (HW/SW = 0): internal reference enable input. When high, the internal reference is enabled (the reference buffers are also enabled). When low, the internal reference is disabled and an external reference is applied at REFI. Software mode (HW/SW = 1): write input. The parallel data input is enabled when C5 and WR are low. The internal reference is enabled by CONFIG bit C15 (REFEN). Hardware mode (HW/SW = 0): internal reference enable input. When high, the internal reference is enabled (the reference buffers are also enabled). When low, the internal reference is disabled and an external reference is applied at REFI. Software mode (HW/SW = 1): connect to DGND or DVDD. The internal reference is enabled by CONFIG bit C15 (REFEN).</td>
</tr>
<tr>
<td><strong>REFIO</strong></td>
<td><strong>56</strong></td>
<td>AIO Reference voltage input/output. The internal reference is enabled by the REFEN/WR pin in hardware mode or by CONFIG bit C15 (REFEN) in software mode. The output value is controlled by the internal digital-to-analog converter (DAC), CONFIG bits C[9:0]. Connect to a decoupling capacitor according to the Power Supply Recommendations section.</td>
</tr>
<tr>
<td><strong>REFN</strong></td>
<td><strong>55</strong></td>
<td>Al Negative reference input/output pin. Connect to a decoupling capacitor and AGND according to the Power Supply Recommendations section.</td>
</tr>
<tr>
<td><strong>RESET</strong></td>
<td><strong>10</strong></td>
<td>Di Reset input, active high. This pin aborts any ongoing conversions and resets the internal Configuration register (CONFIG) to 000003FFh. A valid reset pulse must be at least 50 ns long.</td>
</tr>
<tr>
<td><strong>STBY</strong></td>
<td><strong>9</strong></td>
<td>Di Hardware mode (HW/SW = 0): standby mode input. When low, the entire device is powered down (including the internal conversion clock source and reference). When high, the device operates in normal mode. Software mode (HW/SW = 1): connect to DGND or DVDD. The standby mode can be activated using CONFIG bit C25 (STBY).</td>
</tr>
</tbody>
</table>
7 Specifications

7.1 Absolute Maximum Ratings
over operating free-air temperature range (unless otherwise noted)\(^{(1)}\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>HVDD to AGND</td>
<td>-0.3</td>
<td>18</td>
<td>V</td>
</tr>
<tr>
<td>HVSS to AGND</td>
<td>-18</td>
<td>0.3</td>
<td>V</td>
</tr>
<tr>
<td>AVDD to AGND</td>
<td>-0.3</td>
<td>6</td>
<td>V</td>
</tr>
<tr>
<td>DVDD to DGND</td>
<td>-0.3</td>
<td>6</td>
<td>V</td>
</tr>
<tr>
<td>Analog input voltage</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>HVSS – 0.3</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>HVDD + 0.3</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Reference input voltage with respect to AGND</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>AGND – 0.3</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>AVDD + 0.3</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Digital input voltage with respect to DGND</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DGND – 0.3</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>DVDD + 0.3</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Ground voltage difference AGND to DGND</td>
<td>±0.3</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Input current to all pins except supply</td>
<td>±10</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>Maximum virtual junction temperature, (T_J)</td>
<td></td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>Storage temperature, (T_{\text{stg}})</td>
<td>-65</td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>

\(^{(1)}\) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

<table>
<thead>
<tr>
<th>(V_{(ESD)}) Electrostatic discharge</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(^{(1)})</td>
<td>±2500</td>
<td>V</td>
</tr>
<tr>
<td>Charged-device model (CDM), per JEDEC specification JESD22-C101(^{(2)})</td>
<td>±500</td>
<td>V</td>
</tr>
</tbody>
</table>

\(^{(1)}\) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

\(^{(2)}\) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions
over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>AVDD</td>
<td>4.5</td>
<td>5.0</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>DVDD</td>
<td>2.7</td>
<td>3.3</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>HVDD</td>
<td>5.0</td>
<td>15.0</td>
<td>16.5</td>
<td>V</td>
</tr>
<tr>
<td>HVSS</td>
<td>-16.5</td>
<td>-15.0</td>
<td>-5.0</td>
<td>V</td>
</tr>
<tr>
<td>(T_A) Operating ambient temperature range</td>
<td>-40</td>
<td>25</td>
<td>125</td>
<td>°C</td>
</tr>
</tbody>
</table>

7.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC(^{(1)})</th>
<th>ADS85x8</th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>RGC (VQFN)</td>
<td>PM (LQFP)</td>
<td>UNIT</td>
</tr>
<tr>
<td>(R_{JA}) Junction-to-ambient thermal resistance</td>
<td>22</td>
<td>48.5</td>
<td>°C/W</td>
</tr>
<tr>
<td>(R_{JC(top)}) Junction-to-case (top) thermal resistance</td>
<td>9.0</td>
<td>9.4</td>
<td>°C/W</td>
</tr>
<tr>
<td>(R_{JB}) Junction-to-board thermal resistance</td>
<td>3.6</td>
<td>21.9</td>
<td>°C/W</td>
</tr>
<tr>
<td>(\psi_{JT}) Junction-to-top characterization parameter</td>
<td>0.1</td>
<td>0.3</td>
<td>°C/W</td>
</tr>
<tr>
<td>(\psi_{JB}) Junction-to-board characterization parameter</td>
<td>2.9</td>
<td>21.4</td>
<td>°C/W</td>
</tr>
<tr>
<td>(R_{JC(bot)}) Junction-to-case (bottom) thermal resistance</td>
<td>0.3</td>
<td>n/a</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

\(^{(1)}\) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.
### 7.5 Electrical Characteristics: General

All minimum and maximum specifications are at $T_A = –40°C$ to $+125°C$, specified supply voltage range, $V_{REF} = 2.5$ V (internal), $V_{IN} = ±10$ V, and $I_{DATA} = \text{max}$, unless otherwise noted. Typical values are at $T_A = 25°C$, $HVDD = 15$ V, $HVSS = –15$ V, $AVDD = 5$ V, and $DVDD = 3.3$ V.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>ANALOG INPUT</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CHXX Bipolar full-scale range</td>
<td>RANGE pin, RANGE bit = 0</td>
<td>–4 VREF</td>
<td>4 VREF</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>RANGE pin, RANGE bit = 1</td>
<td>–2 VREF</td>
<td>2 VREF</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Input capacitance</td>
<td>Input range = ±4 VREF</td>
<td>10</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td></td>
<td>Input range = ±2 VREF</td>
<td>20</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>Input leakage current</td>
<td>No ongoing conversion</td>
<td>–1</td>
<td></td>
<td>1</td>
<td>µA</td>
</tr>
<tr>
<td>Aperture delay</td>
<td>5</td>
<td></td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Aperture delay matching</td>
<td>Common CONVST for all channels</td>
<td>100</td>
<td></td>
<td></td>
<td>ps</td>
</tr>
<tr>
<td>Aperture jitter</td>
<td>50</td>
<td></td>
<td></td>
<td></td>
<td>ps</td>
</tr>
<tr>
<td><strong>PSRR</strong></td>
<td>Power-supply rejection ratio</td>
<td>At output code FFFFh, related to HVDD and HVSS</td>
<td>–78</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td><strong>REFERENCE VOLTAGE OUTPUT (REF\text{OUT})</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{REF}$ Reference voltage</td>
<td>2.5-V operation, REFDAC = 3FFh</td>
<td>2.485</td>
<td>2.5</td>
<td>2.515</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>2.5-V operation, REFDAC = 3FFh at 25°C</td>
<td>2.496</td>
<td>2.5</td>
<td>2.504</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>3.0-V operation, REFDAC = 3FFh</td>
<td>2.985</td>
<td>3.0</td>
<td>3.015</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>3.0-V operation, REFDAC = 3FFh at 25°C</td>
<td>2.995</td>
<td>3.0</td>
<td>3.005</td>
<td>V</td>
</tr>
<tr>
<td>$dV_{REF}/dT$ Reference voltage drift</td>
<td>±10</td>
<td>ppm/°C</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>PSRR</strong></td>
<td>Power-supply rejection ratio</td>
<td>At output code FFFFh, related to AVDD</td>
<td>–77</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>I\text{REF\text{OUT}}</td>
<td>Output current</td>
<td>At dc current</td>
<td>–2</td>
<td>2</td>
<td>mA</td>
</tr>
<tr>
<td>I\text{REF}\text{SC}</td>
<td>Short-circuit current (^{(1)})</td>
<td>50</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>I\text{REF\text{ON}}</td>
<td>Turn-on settling time</td>
<td>10</td>
<td></td>
<td></td>
<td>ms</td>
</tr>
<tr>
<td>External load capacitance</td>
<td>At REF\text{xP}, REF\text{xN} pins</td>
<td>4.7</td>
<td>10</td>
<td></td>
<td>µF</td>
</tr>
<tr>
<td></td>
<td>At REFIO pin</td>
<td>100</td>
<td>470</td>
<td></td>
<td>nF</td>
</tr>
<tr>
<td><strong>REFDAC</strong> Tuning range</td>
<td>Internal reference output voltage range</td>
<td>0.2 VREF</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>REFDAC resolution</td>
<td>10</td>
<td></td>
<td></td>
<td></td>
<td>Bits</td>
</tr>
<tr>
<td>DN\text{DAC}</td>
<td>REFDAC differential nonlinearity</td>
<td>–1</td>
<td>±0.1</td>
<td>1 LSB</td>
<td></td>
</tr>
<tr>
<td>IN\text{DAC}</td>
<td>REFDAC integral nonlinearity</td>
<td>–2</td>
<td>±0.1</td>
<td>2 LSB</td>
<td></td>
</tr>
<tr>
<td>$V_{\text{OSDAC}}$ REFDAC offset error</td>
<td>VREF = 0.5 V (DAC = 0CDh)</td>
<td>–4</td>
<td>±0.65</td>
<td>4 LSB</td>
<td></td>
</tr>
<tr>
<td><strong>REFERENCE VOLTAGE INPUT (REF\text{IN})</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{\text{REF\text{IN}}}$ Reference input voltage</td>
<td>0.5</td>
<td>2.5</td>
<td>3.025</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Input resistance</td>
<td>100</td>
<td></td>
<td></td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td>Input capacitance</td>
<td>5</td>
<td></td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>Reference input current</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td><strong>DIGITAL INPUTS(^{(2)}) (CMOS with Schmitt-Trigger Logic Family)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>High-level input voltage</td>
<td>0.7 DVDD</td>
<td>DVDD + 0.3</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Low-level input voltage</td>
<td>DGND – 0.3</td>
<td>0.3 DVDD</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input current</td>
<td>$V_i = $ DVDD to DGND</td>
<td>–50</td>
<td>50</td>
<td>nA</td>
<td></td>
</tr>
<tr>
<td>Input capacitance</td>
<td>5</td>
<td></td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td><strong>DIGITAL OUTPUTS(^{(2)})</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output capacitance</td>
<td>5</td>
<td></td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>Load capacitance</td>
<td>30</td>
<td></td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>High-impedance-state output current</td>
<td>–50</td>
<td>50</td>
<td>nA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Logic family</td>
<td>CMOS</td>
<td></td>
<td></td>
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</tr>
<tr>
<td>$V_{\text{OH}}$ High-level output voltage</td>
<td>$I_{OH} = 100$ µA</td>
<td>DVDD – 0.6</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{\text{OL}}$ Low-level output voltage</td>
<td>$I_{OH} = –100$ µA</td>
<td>DGND + 0.4</td>
<td>V</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

\(^{(1)}\) Reference output current is not limited internally.
\(^{(2)}\) Specified by design.
Electrical Characteristics: General (continued)

All minimum and maximum specifications are at \( T_A = -40^\circ C \) to +125°C, specified supply voltage range, \( V_{REF} = 2.5 \) V (internal), \( V_{IN} = \pm 10 \) V, and \( f_{DATA} = \text{max} \), unless otherwise noted. Typical values are at \( T_A = 25^\circ C \), \( HVDD = 15 \) V, \( HVSS = -15 \) V, \( AVDD = 5 \) V, and \( DVDD = 3.3 \) V.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>AVDD</td>
<td>Analog supply voltage</td>
<td>4.5</td>
<td>5.0</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>DVDD</td>
<td>Buffer I/O supply voltage</td>
<td>2.7</td>
<td>3.3</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>HVDD</td>
<td>Input positive supply voltage</td>
<td>5.0</td>
<td>15.0</td>
<td>16.5</td>
<td>V</td>
</tr>
<tr>
<td>HVSS</td>
<td>Input negative supply voltage</td>
<td>–16.5</td>
<td>–15.0</td>
<td>–5.0</td>
<td>V</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>IAVDD</td>
<td>Analog supply current</td>
<td>( f_{DATA} ) = maximum</td>
<td>37.9</td>
<td>50.1</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>( f_{DATA} ) = maximum</td>
<td>37.3</td>
<td>49.3</td>
<td></td>
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</tr>
<tr>
<td></td>
<td>( f_{DATA} ) = maximum</td>
<td>36.6</td>
<td>48.4</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>( f_{DATA} ) = 250 kSPS, auto-sleep mode</td>
<td>20.3</td>
<td>30.0</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>( f_{DATA} ) = 200 kSPS, auto-sleep mode</td>
<td>17</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>( f_{DATA} ) = 10 kSPS, normal operation</td>
<td>30</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>( f_{DATA} ) = 10 kSPS, auto-sleep mode</td>
<td>4.6</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Auto-sleep mode, no ongoing conversion, internal conversion clock</td>
<td>7.0</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Power-down mode</td>
<td>0.03</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

| IDVDD     | Buffer I/O supply current | \( f_{DATA} \) = maximum | 0.5 | 2.0 | mA |
|           | \( f_{DATA} \) = maximum | 0.5 | 1.4 | |
|           | \( f_{DATA} \) = 250 kSPS | 0.5 | | |
|           | \( f_{DATA} \) = 200 kSPS | 0.4 | | |
|           | \( f_{DATA} \) = 10 kSPS | | | |
|           | Auto-sleep mode, no ongoing conversion, internal conversion clock | 0.35 | | |
|           | Power-down mode | 0.01 | | |

| HVDD      | Input positive supply current | \( f_{DATA} \) = maximum | 3.0 | 4.2 | mA |
|           | \( f_{DATA} \) = maximum | 2.8 | 3.9 | |
|           | \( f_{DATA} \) = maximum | 2.3 | 3.2 | |
|           | \( f_{DATA} \) = 250 kSPS | 1.8 | 2.4 | |
|           | \( f_{DATA} \) = 200 kSPS | 1.5 | | |
|           | \( f_{DATA} \) = 10 kSPS | 0.4 | | |
|           | Auto-sleep mode, no ongoing conversion, internal conversion clock | 0.45 | | |
|           | Power-down mode | 0.01 | | |
Electrical Characteristics: General (continued)

All minimum and maximum specifications are at $T_A = -40^\circ$C to $+125^\circ$C, specified supply voltage range, $V_{REF} = 2.5$ V (internal), $V_{IN} = \pm 10$ V, and $f_{DATA} = \text{max}$, unless otherwise noted. Typical values are at $T_A = 25^\circ$C, $HVDD = 15$ V, $HVSS = -15$ V, $AVDD = 5$ V, and $DVDD = 3.3$ V.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>POWER-SUPPLY REQUIREMENTS (continued)</td>
<td>ADS8528, $f_{DATA} = \text{maximum}$</td>
<td>3.4</td>
<td>4.5</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>ADS8548, $f_{DATA} = \text{maximum}$</td>
<td>3.3</td>
<td>4.4</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>ADS8568, $f_{DATA} = \text{maximum}$</td>
<td>2.7</td>
<td>3.6</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$f_{DATA} = 250$ kSPS</td>
<td>2.1</td>
<td>2.6</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$f_{DATA} = 200$ kSPS</td>
<td>1.7</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$f_{DATA} = 10$ kSPS</td>
<td>0.4</td>
<td></td>
<td></td>
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<tr>
<td></td>
<td>Auto-sleep mode, no ongoing conversion, internal conversion clock</td>
<td>0.35</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Power-down mode</td>
<td>0.01</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>HVSS</td>
<td>Input negative supply current</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>ADS8528, $f_{DATA} = \text{maximum}$</td>
<td>267.1</td>
<td>430.1</td>
<td></td>
<td>mW</td>
</tr>
<tr>
<td></td>
<td>ADS8548, $f_{DATA} = \text{maximum}$</td>
<td>279.7</td>
<td>419.1</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>ADS8568, $f_{DATA} = \text{maximum}$</td>
<td>259.7</td>
<td>389.4</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$f_{DATA} = 250$ kSPS, auto-sleep mode</td>
<td>161.7</td>
<td>255.2</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$f_{DATA} = 200$ kSPS, auto-sleep mode</td>
<td>151.2</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$f_{DATA} = 10$ kSPS, normal operation</td>
<td>163.3</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$f_{DATA} = 10$ kSPS, auto-sleep mode</td>
<td>36.3</td>
<td></td>
<td></td>
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</tr>
<tr>
<td></td>
<td>Auto-sleep mode, no ongoing conversion, internal conversion clock</td>
<td>53.6</td>
<td></td>
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<td></td>
</tr>
<tr>
<td></td>
<td>Power-down mode</td>
<td>0.6</td>
<td></td>
<td></td>
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</tr>
</tbody>
</table>

(3) Maximum power dissipation values are specified with $HVDD = 15$ V and $HVSS = -15$ V.
### 7.6 Electrical Characteristics: ADS8528

All minimum and maximum specifications are at $T_A = -40^\circ C$ to $+125^\circ C$, specified supply voltage range, $V_{REF} = 2.5 \, V$ (internal), $V_{IN} = \pm 10 \, V$, and $f_{DATA} = \text{max}$, unless otherwise noted. Typical values are at $T_A = 25^\circ C$, $HVDD = 15 \, V$, $HVSS = -15 \, V$, $AVDD = 5 \, V$, and $DVDD = 3.3 \, V$.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>SAMPLING DYNAMICS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Conversion time</td>
<td>Internal conversion clock</td>
<td>1.33</td>
<td></td>
<td></td>
<td>$\mu s$</td>
</tr>
<tr>
<td>$f_{DATA}$ Throughput rate</td>
<td>Serial interface, all four SDOx active</td>
<td>480</td>
<td></td>
<td></td>
<td>kSPS</td>
</tr>
<tr>
<td></td>
<td>Parallel interface</td>
<td>650</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>DC ACCURACY</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Resolution</td>
<td></td>
<td>12</td>
<td></td>
<td></td>
<td>Bits</td>
</tr>
<tr>
<td>No missing codes</td>
<td></td>
<td>12</td>
<td></td>
<td></td>
<td>Bits</td>
</tr>
<tr>
<td>INL Integral linearity error$^{(1)}$</td>
<td></td>
<td>$-0.75$</td>
<td>$\pm 0.2$</td>
<td>$0.75$</td>
<td>LSB</td>
</tr>
<tr>
<td>DNL Differential linearity error</td>
<td></td>
<td>$-0.5$</td>
<td>$\pm 0.2$</td>
<td>$0.5$</td>
<td>LSB</td>
</tr>
<tr>
<td>Offset error</td>
<td></td>
<td>$-1.5$</td>
<td>$\pm 0.5$</td>
<td>$1.5$</td>
<td>mV</td>
</tr>
<tr>
<td>Offset error matching</td>
<td>Referenced to voltage at REFIO</td>
<td>$-0.65$</td>
<td></td>
<td>$0.65$</td>
<td>mV</td>
</tr>
<tr>
<td>Offset error drift</td>
<td>$\pm 3.5$</td>
<td></td>
<td></td>
<td></td>
<td>$\mu V/^\circ C$</td>
</tr>
<tr>
<td>Gain error</td>
<td>Referenced to voltage at REFIO</td>
<td>$-0.5%$</td>
<td>$\pm 0.25%$</td>
<td>$0.5%$</td>
<td></td>
</tr>
<tr>
<td>Gain error matching</td>
<td>Between channels of any pair</td>
<td>$-0.2%$</td>
<td></td>
<td>$0.2%$</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Between any two channels</td>
<td>$-0.4%$</td>
<td></td>
<td>$0.4%$</td>
<td></td>
</tr>
<tr>
<td>Gain error drift</td>
<td>Referenced to voltage at REFIO</td>
<td>$\pm 6$</td>
<td></td>
<td></td>
<td>ppm$/^\circ C$</td>
</tr>
<tr>
<td><strong>AC ACCURACY</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SNR Signal-to-noise ratio</td>
<td>At $f_{IN} = 10 , kHz$</td>
<td>73</td>
<td>73.9</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>SINAD Signal-to-noise ratio + distortion</td>
<td>At $f_{IN} = 10 , kHz$</td>
<td>73</td>
<td>73.8</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>THD Total harmonic distortion$^{(2)}$</td>
<td>At $f_{IN} = 10 , kHz$</td>
<td>$-89$</td>
<td>$-84$</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>SFDR Spurious-free dynamic range</td>
<td>At $f_{IN} = 10 , kHz$</td>
<td>84</td>
<td>92</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Channel-to-channel isolation</td>
<td>At $f_{IN} = 10 , kHz$</td>
<td>120</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>BW –3-dB small-signal bandwidth</td>
<td>In 4-VREF mode</td>
<td>48</td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td>In 2-VREF mode</td>
<td>24</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(1) Integral nonlinearity is defined as the maximum deviation from a straight line passing through the end-points of the ideal ADC transfer function expressed as the number of LSBs or percentage of the specified full-scale range.

(2) Calculated on the first nine harmonics of the input frequency.
7.7 Electrical Characteristics: ADS8548

All minimum and maximum specifications are at $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$, specified supply voltage range, $V_{\text{REF}} = 2.5$ V (internal), $V_{\text{IN}} = \pm 10$ V, and $f_{\text{DATA}} = \text{max}$, unless otherwise noted. Typical values are at $T_A = 25^\circ\text{C}$, $HVDD = 15$ V, $HVSS = -15$ V, $AVDD = 5$ V, and $DVDD = 3.3$ V.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
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<tbody>
<tr>
<td><strong>SAMPLING DYNAMICS</strong></td>
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<td></td>
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<td></td>
</tr>
<tr>
<td>Conversion time</td>
<td>Internal conversion clock</td>
<td>1.45</td>
<td>µs</td>
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<tr>
<td>$f_{\text{DATA}}$</td>
<td>Throughput rate</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Serial interface, all four SDOx active</td>
<td></td>
<td>450</td>
<td>kSPS</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Parallel interface</td>
<td></td>
<td>600</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>DC ACCURACY</strong></td>
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<td></td>
<td></td>
</tr>
<tr>
<td>Resolution</td>
<td></td>
<td>14</td>
<td>Bits</td>
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<td></td>
</tr>
<tr>
<td>No missing codes</td>
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<td>14</td>
<td>Bits</td>
<td></td>
<td></td>
</tr>
<tr>
<td>INL</td>
<td>Integral linearity error$^{(1)}$</td>
<td>$-1$</td>
<td>±0.5</td>
<td>1</td>
<td>LSB</td>
</tr>
<tr>
<td>DNL</td>
<td>Differential linearity error</td>
<td>$-1$</td>
<td>±0.25</td>
<td>1</td>
<td>LSB</td>
</tr>
<tr>
<td>Offset error</td>
<td></td>
<td>$-1.5$</td>
<td>±0.5</td>
<td>1.5</td>
<td>mV</td>
</tr>
<tr>
<td>Offset error matching</td>
<td>Referenced to voltage at REFIO</td>
<td>$-0.65$</td>
<td>±3.5</td>
<td>0.65</td>
<td>mV</td>
</tr>
<tr>
<td>Offset error drift</td>
<td></td>
<td>±3.5</td>
<td>µV/°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gain error</td>
<td>Referenced to voltage at REFIO</td>
<td>$-0.5%$</td>
<td>±0.25%</td>
<td>0.5%</td>
<td></td>
</tr>
<tr>
<td>Gain error matching</td>
<td>Between channels of any pair</td>
<td>$-0.2%$</td>
<td>0.2%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gain error drift</td>
<td>Referenced to voltage at REFIO</td>
<td>±6</td>
<td>ppm/°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>AC ACCURACY</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SNR</td>
<td>Signal-to-noise ratio</td>
<td>84</td>
<td></td>
<td>85</td>
<td>dB</td>
</tr>
<tr>
<td>SINAD</td>
<td>Signal-to-noise ratio + distortion</td>
<td>83</td>
<td></td>
<td>84</td>
<td>dB</td>
</tr>
<tr>
<td>THD</td>
<td>Total harmonic distortion$^{(2)}$</td>
<td>At $f_{\text{IN}} = 10$ kHz</td>
<td>−91</td>
<td>−86</td>
<td>dB</td>
</tr>
<tr>
<td>SFDR</td>
<td>Spurious-free dynamic range</td>
<td>At $f_{\text{IN}} = 10$ kHz</td>
<td>86</td>
<td>92</td>
<td>dB</td>
</tr>
<tr>
<td>Channel-to-channel isolation</td>
<td></td>
<td>At $f_{\text{IN}} = 10$ kHz</td>
<td>120</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>BW</td>
<td>−3-dB small-signal bandwidth</td>
<td>In 4-VREF mode</td>
<td>48</td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>In 2-VREF mode</td>
<td>24</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(1) Integral nonlinearity is defined as the maximum deviation from a straight line passing through the end-points of the ideal ADC transfer function expressed as the number of LSBs or percentage of the specified full-scale range.

(2) Calculated on the first nine harmonics of the input frequency.
7.8 Electrical Characteristics: ADS8568

All minimum and maximum specifications are at \( T_A = –40^\circ \text{C} \) to \(+125^\circ \text{C} \), specified supply voltage range, VREF = 2.5 V (internal), \( V_{\text{IN}} = \pm 10 \text{ V} \), and \( f_{\text{DATA}} = \text{max} \), unless otherwise noted. Typical values are at \( T_A = 25^\circ \text{C} \), HVDD = 15 V, HVSS = –15 V, AVDD = 5 V, and DVDD = 3.3 V.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>SAMPLING DYNAMICS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Conversion time</td>
<td>Internal conversion clock</td>
<td>1.7</td>
<td>( \mu \text{s} )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( f_{\text{DATA}} ) Throughput rate</td>
<td>Serial interface, all four SDOx active</td>
<td>400</td>
<td>kSPS</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Parallel interface</td>
<td>510</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>DC ACCURACY</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Resolution</td>
<td></td>
<td>16</td>
<td>Bits</td>
<td></td>
<td></td>
</tr>
<tr>
<td>No missing codes</td>
<td></td>
<td>16</td>
<td>Bits</td>
<td></td>
<td></td>
</tr>
<tr>
<td>INL</td>
<td>Integral linearity error(^{(1)})</td>
<td>–3</td>
<td>±1.5</td>
<td>3</td>
<td>LSB</td>
</tr>
<tr>
<td></td>
<td>At ( T_A = –40^\circ \text{C} ) to (+85^\circ \text{C} ), VQFN package (RGC)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>At ( T_A = –40^\circ \text{C} ) to (+125^\circ \text{C} ), VQFN package (RGC)</td>
<td>–4</td>
<td>±1.5</td>
<td>4</td>
<td>LSB</td>
</tr>
<tr>
<td></td>
<td>At ( T_A = –40^\circ \text{C} ) to (+85^\circ \text{C} ), LQFP package (PM)</td>
<td>–4</td>
<td>±1.5</td>
<td>4</td>
<td>LSB</td>
</tr>
<tr>
<td></td>
<td>At ( T_A = –40^\circ \text{C} ) to (+125^\circ \text{C} ), LQFP package (PM)</td>
<td>–4.5</td>
<td>±1.5</td>
<td>4.5</td>
<td>LSB</td>
</tr>
<tr>
<td>DNL</td>
<td>Differential linearity error</td>
<td>–1</td>
<td>±0.75</td>
<td>1.75</td>
<td>LSB</td>
</tr>
<tr>
<td></td>
<td>At ( T_A = –40^\circ \text{C} ) to (+85^\circ \text{C} )</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>At ( T_A = –40^\circ \text{C} ) to (+125^\circ \text{C} )</td>
<td>–1</td>
<td>±0.75</td>
<td>2</td>
<td>LSB</td>
</tr>
<tr>
<td>Offset error</td>
<td></td>
<td>–1.5</td>
<td>±0.5</td>
<td>1.5</td>
<td>mV</td>
</tr>
<tr>
<td>Offset error drif</td>
<td></td>
<td>–0.65</td>
<td>0.65</td>
<td></td>
<td>mV/°C</td>
</tr>
<tr>
<td>Gain error</td>
<td>Referenced to voltage at REFIO</td>
<td>–0.5%</td>
<td>±0.25%</td>
<td>0.5%</td>
<td></td>
</tr>
<tr>
<td>Gain error mach</td>
<td>Between channels of any pair</td>
<td>–0.2%</td>
<td>0.2%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gain error drift</td>
<td>Referenced to voltage at REFIO</td>
<td>–0.4%</td>
<td>0.4%</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

| **AC ACCURACY**   |                                      |       |       |       |      |
| SNR               | Signal-to-noise ratio                | 90    | 91.5  |       | dB  |
|                   | At \( f_{\text{IN}} = 10 \text{ kHz} \), \( T_A = –40^\circ \text{C} \) to \(+85^\circ \text{C} \) |       |       |       |      |
|                   | At \( f_{\text{IN}} = 10 \text{ kHz} \), \( T_A = –40^\circ \text{C} \) to \(+125^\circ \text{C} \) | 89    | 91.5  |       |      |
| SINAD             | Signal-to-noise ratio + distortion   | 87    | 90    |       | dB  |
|                   | At \( f_{\text{IN}} = 10 \text{ kHz} \), \( T_A = –40^\circ \text{C} \) to \(+85^\circ \text{C} \) |       |       |       |      |
|                   | At \( f_{\text{IN}} = 10 \text{ kHz} \), \( T_A = –40^\circ \text{C} \) to \(+125^\circ \text{C} \) | 86.5  | 90    |       |      |
| THD               | Total harmonic distortion\(^{(2)}\)  | –94   | –90   |       | dB  |
|                   | At \( f_{\text{IN}} = 10 \text{ kHz} \), \( T_A = –40^\circ \text{C} \) to \(+85^\circ \text{C} \) |       |       |       |      |
|                   | At \( f_{\text{IN}} = 10 \text{ kHz} \), \( T_A = –40^\circ \text{C} \) to \(+125^\circ \text{C} \) | –94   | –89.5 |       |      |
| SFDR              | Spurious-free dynamic range          | 90    | 95    |       | dB  |
|                   | At \( f_{\text{IN}} = 10 \text{ kHz} \), \( T_A = –40^\circ \text{C} \) to \(+85^\circ \text{C} \) |       |       |       |      |
|                   | At \( f_{\text{IN}} = 10 \text{ kHz} \), \( T_A = –40^\circ \text{C} \) to \(+125^\circ \text{C} \) | 89.5  | 95    |       |      |
| Channel-to-channel isolation | At \( f_{\text{IN}} = 10 \text{ kHz} \) | 120   |       |       | dB  |
| BW                | –3-dB small-signal bandwidth         | 48    |       |       | MHz |
|                   | In 4-VREF mode                       |       |       |       |      |
|                   | In 2-VREF mode                       | 24    |       |       |      |

\(^{(1)}\) Integral nonlinearity is defined as the maximum deviation from a straight line passing through the end-points of the ideal ADC transfer function expressed as the number of LSBs or percentage of the specified full-scale range.

\(^{(2)}\) Calculated on the first nine harmonics of the input frequency.
### 7.9 Serial Interface Timing Requirements

Over recommended operating free-air temperature range ($T_A$), AVDD = 5 V, and DVDD = 2.7 V to 5.5 V (unless otherwise noted)\(^{(1)}\)

<table>
<thead>
<tr>
<th></th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{SCVX}$ CONVST_x high to XCLK rising edge setup time (CLKSEL = 1)</td>
<td></td>
<td>6</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{XCLK}$ External conversion clock period</td>
<td>ADS8528</td>
<td>66.67</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>ADS8548</td>
<td>72.46</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>ADS8568</td>
<td>85.11</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{CONV}$ Conversion time</td>
<td>ADS8528, CLKSEL = 0</td>
<td>1.33</td>
<td></td>
<td>$\mu$s</td>
</tr>
<tr>
<td></td>
<td>ADS8548, CLKSEL = 0</td>
<td>1.45</td>
<td></td>
<td>$\mu$s</td>
</tr>
<tr>
<td></td>
<td>ADS8568, CLKSEL = 0</td>
<td>1.7</td>
<td></td>
<td>$\mu$s</td>
</tr>
<tr>
<td>$t_{SCV}$ CONVST_x high to BUSY high delay</td>
<td>ADS85x8, t_{CCLK} or t_{XCLK}</td>
<td>19</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>20</td>
<td></td>
<td>20 Cycles</td>
<td></td>
</tr>
<tr>
<td>$t_{CVL}$ CONVST_x low time</td>
<td>ADS85x8, t_{CCLK} or t_{XCLK}</td>
<td>0</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>ADS8528, CLKSEL = 0</td>
<td>67</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>ADS8548, CLKSEL = 0</td>
<td>73</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>ADS8568, CLKSEL = 0</td>
<td>86</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{SCLK}$ Serial clock period</td>
<td>ADS8528</td>
<td>0.022</td>
<td>10</td>
<td>$\mu$s</td>
</tr>
<tr>
<td></td>
<td>ADS8548</td>
<td>0.1</td>
<td></td>
<td>45 MHz</td>
</tr>
<tr>
<td></td>
<td>ADS8568</td>
<td>0.1</td>
<td></td>
<td>45 MHz</td>
</tr>
<tr>
<td>$t_{SCLK}$ Serial clock frequency</td>
<td>ADS8528</td>
<td>0.022</td>
<td>10</td>
<td>$\mu$s</td>
</tr>
<tr>
<td></td>
<td>ADS8548</td>
<td>0.1</td>
<td></td>
<td>45 MHz</td>
</tr>
<tr>
<td></td>
<td>ADS8568</td>
<td>0.1</td>
<td></td>
<td>45 MHz</td>
</tr>
<tr>
<td>$t_{MSB}$ BUSY low to $FS$ low time</td>
<td>ADS85x8, CLKSEL = 1</td>
<td>0</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>ADS8528, CLKSEL = 0</td>
<td>67</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>ADS8548, CLKSEL = 0</td>
<td>73</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>ADS8568, CLKSEL = 0</td>
<td>86</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{FSCV}$ Bus access finished to next conversion start time</td>
<td>ADS8528</td>
<td>0</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>ADS8548</td>
<td>20</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>ADS8568</td>
<td>40</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{SUDI}$ Input data to SCLK falling edge setup time</td>
<td>ADS8528</td>
<td>3</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>ADS8548</td>
<td>5</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>ADS8568</td>
<td>5</td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

### Notes

1. All input signals are specified with $t_R = t_F = 1.5$ ns (10% to 90% of DVDD) and timed from a voltage level of $(V_{IL} + V_{IH}) / 2$.
2. The device runs with an internal conversion clock. Data can be retrieved after the maximum conversion time $t_{CONV(max)}$, independently from the BUSY signal. When referring the data readout to the falling edge of the BUSY signal, $t_{BUFS(min)}$ must be taken into account (see the Data Readout and BUSY/INT Signal section).
7.10 Parallel Interface Timing Requirements (Read Access)  
over recommended operating free-air temperature range (T_A), AVDD = 5 V, and DVDD = 2.7 V to 5.5 V (unless otherwise noted)\(^{(1)}\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>t_{CVL}</td>
<td>20</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t_{ACQ}</td>
<td>280</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t_{CONV}</td>
<td></td>
<td>1.33</td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>t_{DCVB}</td>
<td></td>
<td>25</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t_{BUCS}</td>
<td></td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t_{CSVF}</td>
<td></td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t_{CSD}</td>
<td>0</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t_{RDCS}</td>
<td>0</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t_{RDH}</td>
<td>0</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t_{PDO}</td>
<td>20</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t_{SODI}</td>
<td>5</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t_{TRI}</td>
<td>10</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

(1) All input signals are specified with \(t_R = t_F = 1.5\) ns (10% to 90% of DVDD) and timed from a voltage level of \((V_{IL} + V_{IH}) / 2\).
(2) The device runs with an internal conversion clock. Data can be retrieved after the maximum conversion time \(t_{CONV_{max}}\), independently from the BUSY signal. When referring the data readout to the falling edge of the BUSY signal, \(t_{BUCS_{min}}\) must be taken into account (see the Data Readout and BUSY/INT Signal section).
(3) See the CS signal or RD, whichever occurs first.

7.11 Parallel Interface Timing Requirements (Write Access)  
over recommended ambient temperature range (T_A), AVDD = 5 V, and DVDD = 2.7 V to 5.5 V (unless otherwise noted)\(^{(1)}\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>t_{CSWR}</td>
<td>0</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t_{WRL}</td>
<td>15</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t_{WRH}</td>
<td>10</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t_{WCS}</td>
<td>0</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t_{SUDI}</td>
<td>5</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t_{DI}</td>
<td>5</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

(1) All input signals are specified with \(t_R = t_F = 1.5\) ns (10% to 90% of DVDD) and timed from a voltage level of \((V_{IL} + V_{IH}) / 2\).
Figure 1. Serial Operation Timing Diagram (All Four SDO_x Active)
Figure 2. Parallel Read Access Timing Diagram

Figure 3. Parallel Write Access Timing Diagram
7.12 Typical Characteristics

graphs are valid for all devices of the family, at $T_A = 25^\circ C$, HVDD = 15 V, HVSS = –15 V, AVDD = 5 V, DVDD = 3.3 V, VREF = 2.5 V (internal), $V_{IN} = \pm 10$ V, and $f_{DATA} = $ maximum (unless otherwise noted)
Typical Characteristics (continued)

graphs are valid for all devices of the family, at $T_A = 25^\circ C$, HVDD = 15 V, HVSS = –15 V, AVDD = 5 V, DVDD = 3.3 V, VREF = 2.5 V (internal), $V_{IN} = \pm 10$ V, and $f_{DATA} = \text{maximum (unless otherwise noted)}$
Typical Characteristics (continued)

graphs are valid for all devices of the family, at \( T_A = 25^\circ \text{C} \), HVDD = 15 V, HVSS = –15 V, AVDD = 5 V, DVDD = 3.3 V, VREF = 2.5 V (internal), \( V_{\text{IN}} = \pm 10 \text{ V} \), and \( t_{\text{DATA}} = \text{maximum} \) (unless otherwise noted).

Figure 16. PSRR vs Supply Noise Frequency

Figure 17. Conversion Time vs Temperature

Figure 18. Code Histogram
(ADS8568, 16390 Hits)

Figure 19. SNR vs Temperature

Figure 20. SINAD vs Temperature

Figure 21. THD vs Temperature
Typical Characteristics (continued)

graphs are valid for all devices of the family, at $T_A = 25°C$, HVDD = 15 V, HVSS = −15 V, AVDD = 5 V, DVDD = 3.3 V, VREF = 2.5 V (internal), $V_{IN} = \pm 10$ V, and $f_{DATA} = \text{maximum (unless otherwise noted)}$

Figure 22. SFDR vs Temperature

Figure 23. Frequency Spectrum (ADS8568, 2048-Point FFT, $f_{IN} = 10$ kHz, $\pm 10$-V$_{IN}$ Range)

Figure 24. Frequency Spectrum (ADS8568, 2048-Point FFT, $f_{IN} = 10$ kHz, $\pm 5$-V$_{IN}$ Range)

Figure 25. Channel-to-Channel Isolation vs Input Noise Frequency

Figure 26. Internal Reference Voltage vs Analog Supply Voltage (2.5-V Mode)

Figure 27. Internal Reference Voltage vs Temperature (2.5-V Mode)
Typical Characteristics (continued)

graphs are valid for all devices of the family, at $T_A = 25^\circ C$, HVDD = 15 V, HVSS = −15 V, AVDD = 5 V, DVDD = 3.3 V, VREF = 2.5 V (internal), $V_{IN} = \pm 10$ V, and $f_{DATA} = \text{maximum}$ (unless otherwise noted)
Typical Characteristics (continued)

graphs are valid for all devices of the family, at $T_A = 25^\circ C$, $HVDD = 15 V$, $HVSS = –15 V$, $AVDD = 5 V$, $DVDD = 3.3 V$, $VREF = 2.5 V$ (internal), $V_{IN} = \pm 10 V$, and $f_{DATA} = \text{maximum (unless otherwise noted)}$

Figure 34. ADS8568 Input Supply Current vs Data Rate
8 Parameter Measurement information

8.1 Equivalent Circuits

Figure 35. Equivalent Input Circuits

9 Detailed Description

9.1 Overview

The ADS85x8 series includes eight 12-, 14-, and 16-bit analog-to-digital converters (ADCs) that operate based on the successive approximation register (SAR) architecture. This architecture is designed on the charge redistribution principle that inherently includes a sample-and-hold function. The eight analog inputs are grouped into four channel pairs. These channel pairs can be sampled and converted simultaneously, preserving the relative phase information of the signals of each pair. Separate conversion start signals allow simultaneous sampling on each channel pair of four, six, or eight channels. These devices accept single-ended, bipolar analog input signals in the selectable ranges of ±4 VREF or ±2 VREF with an absolute value of up to ±12 V; see the Analog Inputs section.

The devices offer an internal 2.5-V or 3-V reference source followed by a 10-bit digital-to-analog converter (DAC) that allows the reference voltage VREF to be adjusted in 2.44-mV or 2.93-mV steps, respectively.

The ADS85x8 also offer a selectable parallel or serial interface that can be used in hardware or software mode; see the Device Configuration section for details. The Analog and Digital sections describe the functionality and control of the device in detail.
9.2 Functional Block Diagram

Clock Generator

Control Logic

Config Register

I/O

BUSY/INT
RANGE/XCLK
RW/SW
REFEN/WR
STBY
RESET

CS/FS
RD
DB[15:0]
ASLEEP
PAR/SER
SCLK

String DAC

2.5 VREF

CH_A0
AGND

CONVST_A

REFAP
CH_A1
AGND

CH_B0
AGND

CONVST_B

REFBP
CH_B1
AGND

CH_C0
AGND

CONVST_C

REFCP
CH_C1
AGND

CH_D0
AGND

CONVST_D

REFDP
CH_D1
AGND

REFIO

AGND

DGND
9.3 Feature Description

9.3.1 Analog

This section addresses the analog input circuit, the ADCs and control signals, and the reference design of the device.

9.3.1.1 Analog Inputs

The inputs and the converters are of single-ended bipolar type. The absolute voltage range can be selected using the RANGE pin (in hardware mode) or RANGE_x bits (in software mode) in the Configuration (CONFIG) register to either ±4 VREF or ±2 VREF. With the internal reference set to 2.5 V (VREF bit C13 = 0 in the CONFIG register), the input voltage range can be ±10 V or ±5 V. With the internal reference source set to 3 V (CONFIG bit C13 = 1), an input voltage range of ±12 V or ±6 V can be configured. The logic state of the RANGE pin is latched with the falling edge of BUSY (if CONFIG bit C26 = 0).

The input current on the analog inputs depends on the actual sample rate, input voltage, and signal source impedance. Essentially, the current into the analog inputs charges the internal capacitor array only during the sampling period (t_{ACQ}). The source of the analog input voltage must be able to charge the input capacitance of 10 pF in ±4-VREF mode or of 20 pF in ±2-VREF mode to a 12-, 14-, or 16-bit accuracy level within the acquisition time; see Figure 35. During the conversion period, there is no further input current flow and the input impedance is greater than 1 MΩ. To ensure a defined start condition, the sampling capacitors of the ADS85x8 are pre-charged to a fixed internal voltage before switching into sampling mode.

To maintain the linearity of the converter, the inputs must always remain within the specified range defined in the Electrical Characteristics table. The minimum –3-dB bandwidth of the driving operational amplifier can be calculated using Equation 1:

\[
f_{3dB} = \frac{\ln(2)(n + 1)}{2\pi t_{ACQ}}
\]

where

\[
\text{• } n = 12, 14, \text{ or } 16; n \text{ is the resolution of the ADS85x8} \quad (1)
\]

With a minimum acquisition time of t_{ACQ} = 280 ns, the required minimum bandwidth of the driving amplifier is 5.2 MHz for the ADS8528, 6.0 MHz for the ADS8548, or 6.7 MHz for the ADS8568. The required bandwidth can be lower if the application allows a longer acquisition time. A gain error occurs if a given application does not fulfill the bandwidth requirement shown in Equation 1.

A driving operational amplifier may not be required if the impedance of the signal source (R_{SOURCE}) fulfills the requirement of Equation 2:

\[
R_{SOURCE} < \frac{t_{ACQ}}{C_{S}\ln(2)(n + 1)} - (R_{SER} + R_{SW})
\]

where

\[
\text{• } n = 12, 14, \text{ or } 16; n \text{ is the resolution of the ADC}
\]

\[
\text{• } C_{S} = 10 \text{ pF is the sample capacitor value in } V_{IN} = \pm 4\text{-VREF mode}
\]

\[
R_{SER} = 200 \Omega \text{ is the input resistor value}
\]

\[
R_{SW} = 130 \Omega \text{ is the switch resistance value}
\]

(2)

With a minimum acquisition time of t_{ACQ} = 280 ns, the maximum source impedance must be less than 2.7 kΩ for the ADS8528, 2.3 kΩ for the ADS8548, and 2.0 kΩ for the ADS8568 in ±4V-REF mode, or less than 1.2 kΩ for the ADS8528, 1.0 kΩ for the ADS8548, and 0.8 kΩ for the ADS8568 in ±2-VREF mode. The source impedance can be higher if the application allows a longer acquisition time.

9.3.1.2 Analog-to-Digital Converter (ADC)

The device includes eight ADCs that operate with either an internal or an external conversion clock.
Feature Description (continued)

9.3.1.3 Conversion Clock

The device uses either an internally-generated (CCLK) or an external (XCLK) conversion clock signal (in software mode only). In default mode, the device generates an internal clock. In this case, a complete conversion including the pre-charging of the sample capacitors takes 19 to 20 clock cycles, depending on the setup time of the incoming CONVST_x signal with relation to the CCLK rising edge.

When the CLKSEL bit is set high (CONFIG bit C29), an external conversion clock can be applied on pin 34. A complete conversion process requires 19 clock cycles in this case if the tSCVX timing requirement is fulfilled. The external clock can remain low between conversions.

If the application requires lowest power dissipation at low data rates, using the auto-sleep mode activated with pin 36 (ASLEEP) is recommended. In this case, a conversion cycle takes up to 26 clock cycles (see the Reset and Power-Down Modes section for more details).

9.3.1.4 CONVST_x

The analog inputs of each channel pair (CH_x0, CH_x1) are held with the rising edge of the corresponding CONVST_x signal. The conversion automatically starts with the next rising edge of the conversion clock. CONVST_A is a master conversion start that resets the internal state machine and causes the data output to start with the result of channel A0. In cases where channel pairs of the device are used at different data rates, CONVST_A must always be the one used at the highest frequency.

A conversion start must not be issued during an ongoing conversion on the corresponding channel pair. However, conversions are allowed to be initiated on other input pairs; see the Sequential Operation section for more details.

If a parallel interface is used, the content of the output port depends on which CONVST_x signals are issued. Figure 36 shows examples of different scenarios with all channel pairs active.

![Figure 36. Data Output versus CONVST_x (All Channels Active)](image-url)
Feature Description (continued)

9.3.1.5 Data Readout and BUSY/INT Signal

The BUSY signal indicates if a conversion is in progress. The BUSY signal goes high with a rising edge of any CONVST_x signal and returns low again when the last channel pair completes the conversion cycle.

When operating the device with an external clock (CONFIG bit 29, CLKSEL = 1), data readout can be initiated immediately after the falling edge of the BUSY signal or after 19 complete conversion clock cycles (XCLK), respectively.

When using the device with an internal conversion clock (CONFIG bit 29, CLKSEL = 0), data can be retrieved after \( t_{\text{CONV(max)}} \) independently from the BUSY signal. In case the data readout is referred to the falling edge of the BUSY signal, the readout sequence cannot start before \( t_{\text{BUFS/BUCS}} \) after the falling edge, corresponding to 1 CCLK cycle (for example, 86 ns for the ADS8568).

In contrast, the INT signal goes high when a new conversion result is loaded in the output register (which occurs when the conversion completes) and remains high until the next read access, as shown in Figure 37.

The polarity of the BUSY/INT signal can be changed using CONFIG bit C26. The mode of pin 35 can be controlled using CONFIG bit C27.

![Figure 37. BUSY versus INT Behavior of Pin 35](image-url)
Feature Description (continued)

9.3.1.6 Sequential Operation

The four channel pairs of the ADS8528, ADS8548, and ADS8568 can run in sequential mode, with the corresponding CONVST_x signals interleaved. In this case, the BUSY output transitions low for a single conversion clock cycle (t_CCLK) whenever a channel pair completes a conversion. BUSY finally remains low when the conversion of the last channel pair completes. Figure 38 shows the behavior of the BUSY output in this mode.

![Sequential Operation Timing Diagram](image)

NOTE: EOC = end of conversion (internal signal).

**Figure 38. Sequential Operation Timing Diagram**

For best performance, operation with an external clock is recommended (CONFIG bit 29, CLKSEL = 1). Initiate each conversion start during the high phase of the external clock; see Figure 40.

The time between two CONVST_x pulses must be at least one conversion clock cycle. In case the skew of the CONVST_x signals is less than one conversion clock cycle, the data readout cannot be started before t_CCLK after the falling edge of the BUSY signal.

9.3.1.7 Reference

The ADS85x8 provides an internal, low-drift, 2.5-V reference source. To increase the input voltage range, the reference voltage can be switched to 3-V mode using the VREF bit (CONFIG bit C13). The reference feeds a 10-bit string-DAC controlled by the REFDAC[9:0] bits in the Configuration (CONFIG) register. The buffered DAC output is connected to the REFIO pin. In this way, the voltage at this pin is programmable in 2.44-mV steps (2.92 mV in 3-V mode) and adjustable to the applications needs without additional external components. The actual output voltage can be calculated using Equation 3:

$$V_{REF} = \frac{\text{Range} \times (\text{Code} + 1)}{1024}$$

where

- Range = the chosen maximum reference voltage output range (2.5 V or 3 V)
- Code = the decimal value of the DAC register content

Equation 3
Feature Description (continued)

Table 1 lists some examples of internal reference DAC settings with a reference range set to 2.5 V. However, to ensure proper performance, the DAC output voltage must not be programmed below 0.5 V.

Decouple the buffered output of the DAC with a 100-nF capacitor (minimum); for best performance, a 470-nF capacitor is recommended. If the internal reference is placed into power-down (default), an external reference voltage can drive the REFIO pin.

Table 1. DAC Settings Examples (2.5-V Operation)

<table>
<thead>
<tr>
<th>VREFOUT</th>
<th>DECIMAL CODE</th>
<th>BINARY CODE</th>
<th>HEXADECIMAL CODE</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.5 V</td>
<td>204</td>
<td>00 1100 1100</td>
<td>CCh</td>
</tr>
<tr>
<td>1.25 V</td>
<td>511</td>
<td>01 1111 1111</td>
<td>1FFh</td>
</tr>
<tr>
<td>2.5 V</td>
<td>1023</td>
<td>11 1111 1111</td>
<td>3FFh</td>
</tr>
</tbody>
</table>

The voltage at the REFIO pin is buffered with four internal amplifiers, one for each ADC pair. The output of each buffer must be decoupled with a 10-µF capacitor between the pin pairs of 3 and 6, 43 and 46, 50 and 53, and 60 and 63. The 10-µF capacitors are available as ceramic 0805-SMD components and in X5R quality.

The internal reference buffers can be powered down to decrease the power dissipation of the device. In this case, external reference drivers can be connected to the REFAP, REFBP, REFCP, and REFDP pins. With 10-µF decoupling capacitors, the minimum required bandwidth can be calculated using Equation 4:

\[
\frac{\ln(2)}{2\pi t_{\text{CONV}}}
\]

With the minimum \( t_{\text{CONV}} \) of 1.33 µs, the external reference buffers require a minimum bandwidth of 83 kHz.

9.3.2 Digital

This section describes the digital control and the timing of the device in detail.

9.3.2.1 Device Configuration

Depending on the desired mode of operation, the ADS85xx can be configured using the external pins or the Configuration register (CONFIG), as shown in Table 2.

Table 2. ADS85xx Configuration Settings

<table>
<thead>
<tr>
<th>INTERFACE MODE</th>
<th>HARDWARE MODE (HW/SW = 0)</th>
<th>SOFTWARE MODE (HW/SW = 1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Parallel (PAR/SER = 0)</td>
<td>Configuration using pins and (optionally) Configuration register bits C30, C29, C[27:26], C22, C20, C18, C14, C13, and C[9:0]</td>
<td>Configuration using Configuration register bits C[31:0] only; status of pins 9, 11, 20, and 34 are disregarded (if C29 = C29 = 0)</td>
</tr>
<tr>
<td>Serial (PAR/SER = 1)</td>
<td>Configuration using pins and (optionally) Configuration register bits C30, C29, C[27:26], C22, C20, C18, C13, and C[9:0]</td>
<td>Configuration using Configuration register bits C[31:0] only; status of pins 9, 11, 20, and 34 are disregarded (if C29 = C29 = 0)</td>
</tr>
</tbody>
</table>
9.3.2.2 Parallel Interface
To use the device with the parallel interface, hold the PAR/SER pin low. The maximum achievable data throughput rate is 650 kSPS for the ADS8528, 600 kSPS for the ADS8548, and 510 kSPS for the ADS8568 in this case.

Access to the ADS85x8 is controlled as illustrated in Figure 2 and Figure 3.

9.3.2.3 Serial Interface

The serial interface mode is selected by setting the PAR/SER pin high. In this case, each data transfer starts with the falling edge of the frame synchronization input (FS). The conversion results are presented on the serial data output pins SDO_A (always active), SDO_B, SDO_C, and SDO_D, depending on the selections made using the SEL_xx pins. Starting with the most significant bit (MSB), the output data are changed with the SCLK falling edge. The ADS8528 and ADS8548 output data maintain the LSB-aligned, 16-bit format with leading bits containing the extended sign (see Table 3). Serial data input SDI are latched with the SCLK falling edge.

The serial interface can be used with one, two, or four output ports. Port SDO_B can be enabled using pin 27 (SEL_B) and ports SDO_C and SDO_D are enabled using pin 28 (SEL_CD). If all four serial data output ports are selected, data can be read with either two 16-bit data transfers or with a single 32-bit data transfer. The data of channels CH_x0 are available first, followed by data from channels CH_x1. The maximum achievable data throughput rate is 480 kSPS for the ADS8528, 450 kSPS for the ADS8548, and 400 kSPS for the ADS8568 in this case.

If the application allows a data transfer using two ports only, the SDO_A and SDO_B outputs are used. The device outputs data from channel CH_A0 followed by CH_A1, CH_C0, and CH_C1 on SDO_A; data from channel CH_B0 followed by CH_B1, CH_D0, and CH_D1 occur on SDO_B. In this case, a data transfer of four 16-bit words, two 32-bit words, or one continuous 64-bit word is supported. The maximum achievable data throughput rate is 360 kSPS for the ADS8528, 345 kSPS for the ADS8548, and 315 kSPS for the ADS8568 in this case.

The output SDO_A is always active and exclusively used if only one serial data port is used in the application. Data are available in the following order: CH_A0, CH_A1, CH_B0, CH_B1, CH_C0, CH_C1, CH_D0, and CH_D1. Data can be read using eight 16-bit transfers, four 32-bit transfers, two 64-bit transfers, or a single 128-bit transfer. The maximum achievable data throughput rate is 235 kSPS for the ADS8528, 230 kSPS for the ADS8548 and 215 kSPS for the ADS8568 in this case. Figure 1 and Figure 39 illustrate all possible scenarios in more detail.

![Figure 39](image-url)
9.3.2.4 Output Data Format

The data output format of the ADS85x8 is binary two's complement, as shown in Table 3. For the ADS8528 and ADS8548 (that deliver 12-bit or 14-bit conversion results, respectively), the leading bits of either the 16-bit frame (serial interface) or the output pins (DB[15:12] for the ADS8528 or DB[15:14] for the ADS8548 in parallel mode) deliver a sign extension.

<table>
<thead>
<tr>
<th>DESCRIPTION</th>
<th>INPUT VOLTAGE VALUE</th>
<th>ADS8528</th>
<th>ADS8548</th>
<th>ADS8568</th>
</tr>
</thead>
<tbody>
<tr>
<td>Positive full-scale</td>
<td>4 VREF or 2 VREF</td>
<td>0000 0111 1111 1111 07FFh</td>
<td>0001 1111 1111 1111 1FFFh</td>
<td>0111 1111 1111 1111 7FFFh</td>
</tr>
<tr>
<td>Midscale 0.5 LSB</td>
<td>VREF / (2 × resolution)</td>
<td>0000 0000 0000 0000 0000h</td>
<td>0000 0000 0000 0000 0000h</td>
<td>0000 0000 0000 0000 0000h</td>
</tr>
<tr>
<td>Midscale –0.5 LSB</td>
<td>–VREF / (2 × resolution)</td>
<td>1111 1111 1111 1111 FFFFh</td>
<td>1111 1111 1111 1111 FFFFh</td>
<td>1111 1111 1111 1111 FFFFh</td>
</tr>
<tr>
<td>Negative full-scale</td>
<td>–4 VREF or –2 VREF</td>
<td>1111 1000 0000 0000 F800h</td>
<td>1110 0000 0000 0000 E000h</td>
<td>1000 0000 0000 0000 8000h</td>
</tr>
</tbody>
</table>

9.4 Device Functional Modes

9.4.1 Hardware Mode

With the HW/SW input (pin 41) set low, the device functions are controlled via the pins and, optionally, Configuration register bits C30, C29, C[27:26], C22, C20, C18, C14 (in parallel interface mode only), C13, and C[9:0].

The device can generally be used in hardware mode but can be switched to software mode to initialize or adjust the Configuration register settings (for example, the internal reference DAC) and back to hardware mode thereafter.

9.4.2 Software Mode

When the HW/SW input is set high, the device operates in software mode with functionality set only by the Configuration register bits (corresponding pin settings are ignored).

If the parallel interface is used, an update of all Configuration register settings is performed by issuing two 16-bit write accesses on pins DB[15:0] (to avoid losing data, the entire sequence must be finished before starting a new conversion). Do not hold CS low during these two accesses. To enable the actual update of the register settings, the first bit (C31) must be set to 1 during the access.

If the serial interface is used, the update of the register contents can be performed continuously (combined read/write access). Optionally, to reduce the data transfer on the SDI line and the electromagnetic interference (EMI) of the system, the SDI input can be pulled low when a register update is not required. Figure 40 illustrates the different Configuration register update options.
Device Functional Modes (continued)

RESET
(or Power Up)

BUSY
(C20 = C21 = 0)

PAR/SER = 1

FS

SDI

Content Update

C[31:0]

Initialization Data

No Content Update

PAR/SER = 0

CS

WR

Initialization Data

Update

DB[15:0]

C [31:16] C [15:0]

C [31:16] C [15:0]

Figure 40. Configuration Register Update Options
Device Functional Modes (continued)

9.4.3 Daisy-Chain Mode

The serial interface of the ADS85x8 supports a daisy-chain feature that allows cascading of multiple devices to minimize the board space requirements and simplify routing of the data and control lines. In this case, the DB3/DCIN_A, DB2/DCIN_B, DB1/DCIN_C, and DB0/DCIN_D pins are used as serial data inputs for channels A, B, C, and D, respectively. Figure 41 shows an example of a daisy-chain connection of three devices sharing a common CONVST line to allow simultaneous sampling of 24 analog channels along with the corresponding timing diagram.

To activate the daisy-chain mode, the DCEN pin must be pulled high. However, the DCEN of the first device in the chain must remain low.

In applications where not all channel pairs are used, declaring the device with disabled channel pairs to be the first in the daisy-chain is recommended.

Figure 41. Example of Daisy-Chaining Three Devices

9.4.4 Reset and Power-Down Modes

The device supports two reset mechanisms: a power-on reset (POR) and a pin-controlled reset (RESET) that can be issued using pin 10. Both the POR and RESET function as a master reset that causes any ongoing conversion to be interrupted, the Configuration register content to be set to the default value, and all channels to be switched into sample mode.

When the device is powered up, POR sets the device in default mode when AVDD reaches 1.2 V. In normal operation, glitches on the AVDD supply below this threshold trigger a device reset.
Device Functional Modes (continued)

The entire device, except for the digital interface, can be powered down by pulling the STBY pin low (pin 9). Data can be retrieved when in standby mode because the digital interface section remains active. To power the device on again, the STBY pin must be brought high. The device is ready to start a new conversion after the 10 ms required to activate and settle the internal circuitry. This user-controlled approach can be used in applications that require lower data throughput rates at lowest power dissipation. The content of CONFIG is not changed during standby mode and is not required to perform a reset after returning to normal operation.

Although standby mode affects the entire device, each device channel pair (except channel pair A, which is the master channel pair and is always active) can also be individually switched off by setting the Configuration register bits C22, C20, and C18 (PD_x). If a certain channel pair is powered-down in this manner, the output register is disabled as shown in Figure 42. When reactivated, the relevant channel pair requires 10 ms to fully settle before starting a new conversion.

(1) Channel pair C disabled (PD_C = 1), CS = 0.

NOTE: Boxed areas indicate the minimum required frame to acquire all new conversion results. The read access can be interrupted, thereafter.

Figure 42. Example of Data Output Order With Channel Pair C Powered Down(1)
Device Functional Modes (continued)

Auto-sleep mode is enabled by pulling pin 36 (ASLEEP) high. If auto-sleep mode is enabled, the ADS85x8 automatically reduce the current requirement to 7 mA (IAVDD) after finishing a conversion; thus, the end of conversion actually activates this power-down mode. Triggering a new conversion by applying a positive CONVST_x edge starts the wake-up sequence to put the device back into normal operation. At the beginning, all required building blocks power-up and the sampling switches close again. This sequence takes six to seven conversion clock cycles of either the internal or external clock. During this time, the sampling capacitance must be recharged to the input signal with the required 12-bit, 14-bit, or 16-bit accuracy level. The bandwidth requirements of the driving operational amplifier described in the Analog Inputs section must be fulfilled. At the end of the sequence, the new sample is taken and the conversion starts automatically, as shown in Figure 43. Therefore, a complete conversion process takes 25 to 26 conversion clock cycles; thus, the maximum throughput rate in auto-sleep mode is reduced to a maximum of 400 kSPS for the ADS8528, 375 kSPS for the ADS8548, and 330 kSPS for the ADS8568 in serial interface mode. In parallel mode, the maximum data rates are 510 kSPS for the ADS8528, 470 kSPS for the ADS8548, and 400 kSPS for the ADS8568. If enabled, the internal reference remains active during auto-sleep mode. Table 4 compares the analog current requirements of the device in different modes.

![Figure 43. Auto-Sleep Power-Down Mode](image)

<table>
<thead>
<tr>
<th>OPERATIONAL MODE</th>
<th>ANALOG CURRENT (IAVDD)</th>
<th>ENABLED, DISABLED BY</th>
<th>ACTIVATED BY</th>
<th>NORMAL OPERATION TO POWER-DOWN DELAY</th>
<th>RESUMED BY</th>
<th>POWER-UP TO NORMAL OPERATION DELAY</th>
<th>POWER-UP TO NEXT CONVERSION START TIME</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal operation</td>
<td>12.5 mA/ch pair at maximum data rate</td>
<td>Power on</td>
<td>CONVST_x</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>Auto-sleep</td>
<td>1.75 mA/ch pair</td>
<td>ASLEEP = 1</td>
<td>Each end of conversion</td>
<td>At BUSY falling edge</td>
<td>CONVST_x</td>
<td>Immediate</td>
<td>$7 \times t_{CCLK}$ max</td>
</tr>
<tr>
<td>Power-down of channel pair X</td>
<td>16 µA (channel pair X)</td>
<td>RW/SW = 1 PD_x = 1 (CONFIG bit)</td>
<td>Immediate</td>
<td>PD_x = 0 (CONFIG bit)</td>
<td>Immediate after completing CONFIG update</td>
<td>10 ms</td>
<td></td>
</tr>
<tr>
<td>Power-down (entire device)</td>
<td>30 µA</td>
<td>Power on</td>
<td>STBY = 0</td>
<td>Immediate</td>
<td>STBY = 1</td>
<td>Immediate</td>
<td>10 ms</td>
</tr>
</tbody>
</table>
9.5 Register Maps

9.5.1 Configuration (CONFIG) Register

The Configuration register settings can only be changed in software mode and are not affected when switching to hardware mode thereafter. The register values are independent from input pin settings. Changes are active with the second WR rising edge in parallel interface mode or with the 32nd SCLK falling edge of the access where the register content is updated in serial mode. The CONFIG content is defined in CONFIG: Configuration Register (default = 000003FFh).

9.5.1.1 CONFIG: Configuration Register (default = 000003FFh)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>WRITE_EN: Register update enable</td>
</tr>
<tr>
<td></td>
<td>This bit is not active in hardware mode.</td>
</tr>
<tr>
<td></td>
<td>0 = Register content update disabled (default)</td>
</tr>
<tr>
<td></td>
<td>1 = Register content update enabled</td>
</tr>
<tr>
<td>30</td>
<td>READ_EN: Register read-out access enable</td>
</tr>
<tr>
<td></td>
<td>This bit is not active in hardware mode.</td>
</tr>
<tr>
<td></td>
<td>0 = Normal operation (conversion results available on SDO_A)</td>
</tr>
<tr>
<td></td>
<td>1 = Configuration register contents output on SDO_A with next two accesses</td>
</tr>
<tr>
<td>(READ_EN automatically resets to 0 thereafter)</td>
<td></td>
</tr>
<tr>
<td>29</td>
<td>CLKSEL: Conversion clock selector</td>
</tr>
<tr>
<td></td>
<td>This bit is active in hardware mode.</td>
</tr>
<tr>
<td></td>
<td>0 = Normal operation with internal conversion clock; mandatory in hardware mode (default)</td>
</tr>
<tr>
<td></td>
<td>1 = External conversion clock applied through pin 34 (XCLK) is used (conversion takes 19 clock cycles)</td>
</tr>
<tr>
<td>28</td>
<td>CLKOUT: Internal conversion clock output enable</td>
</tr>
<tr>
<td></td>
<td>This bit is not active in hardware mode.</td>
</tr>
<tr>
<td></td>
<td>0 = Normal operation (default)</td>
</tr>
<tr>
<td></td>
<td>1 = Internal conversion clock is available at pin 34</td>
</tr>
<tr>
<td>27</td>
<td>BUSY/INT: Busy/interrupt selector</td>
</tr>
<tr>
<td></td>
<td>This bit is active in hardware mode.</td>
</tr>
<tr>
<td></td>
<td>0 = BUSY/INT pin is in BUSY mode (default)</td>
</tr>
<tr>
<td></td>
<td>1 = BUSY/INT pin is in interrupt mode (INT); can only be used if all eight channels are sampled simultaneously (all CONVST_x tied together)</td>
</tr>
<tr>
<td>26</td>
<td>BUSY POL: BUSY/INT polarity selector</td>
</tr>
<tr>
<td></td>
<td>This bit is active in hardware mode.</td>
</tr>
<tr>
<td></td>
<td>0 = BUSY/INT active high (default)</td>
</tr>
<tr>
<td></td>
<td>1 = BUSY/INT active low</td>
</tr>
</tbody>
</table>

Figure 44. CONFIG Register

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
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<td></td>
<td>This bit is not active in hardware mode.</td>
</tr>
<tr>
<td></td>
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</tr>
<tr>
<td></td>
<td>1 = Register content update enabled</td>
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<tr>
<td>30</td>
<td>READ_EN: Register read-out access enable</td>
</tr>
<tr>
<td></td>
<td>This bit is not active in hardware mode.</td>
</tr>
<tr>
<td></td>
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<tr>
<td></td>
<td>1 = Configuration register contents output on SDO_A with next two accesses</td>
</tr>
<tr>
<td>(READ_EN automatically resets to 0 thereafter)</td>
<td></td>
</tr>
<tr>
<td>29</td>
<td>CLKSEL: Conversion clock selector</td>
</tr>
<tr>
<td></td>
<td>This bit is active in hardware mode.</td>
</tr>
<tr>
<td></td>
<td>0 = Normal operation with internal conversion clock; mandatory in hardware mode (default)</td>
</tr>
<tr>
<td></td>
<td>1 = External conversion clock applied through pin 34 (XCLK) is used (conversion takes 19 clock cycles)</td>
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<tr>
<td>28</td>
<td>CLKOUT: Internal conversion clock output enable</td>
</tr>
<tr>
<td></td>
<td>This bit is not active in hardware mode.</td>
</tr>
<tr>
<td></td>
<td>0 = Normal operation (default)</td>
</tr>
<tr>
<td></td>
<td>1 = Internal conversion clock is available at pin 34</td>
</tr>
<tr>
<td>27</td>
<td>BUSY/INT: Busy/interrupt selector</td>
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<td></td>
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<td>0 = BUSY/INT pin is in BUSY mode (default)</td>
</tr>
<tr>
<td></td>
<td>1 = BUSY/INT pin is in interrupt mode (INT); can only be used if all eight channels are sampled simultaneously (all CONVST_x tied together)</td>
</tr>
<tr>
<td>26</td>
<td>BUSY POL: BUSY/INT polarity selector</td>
</tr>
<tr>
<td></td>
<td>This bit is active in hardware mode.</td>
</tr>
<tr>
<td></td>
<td>0 = BUSY/INT active high (default)</td>
</tr>
<tr>
<td></td>
<td>1 = BUSY/INT active low</td>
</tr>
</tbody>
</table>
Bit 25  
STBY: Power-down enable  
This bit is not active in hardware mode.  
0 = Normal operation (default)  
1 = Entire device is powered down (including the internal clock and reference)

Bit 24  
RANGE_A: Input voltage range selector for channel pair A  
This bit is not active in hardware mode.  
0 = Input voltage range: 4 VREF (default)  
1 = Input voltage range: 2 VREF

Bit 23  
RANGE_B: Input voltage range selector for channel pair B  
This bit is not active in hardware mode.  
0 = Input voltage range: 4 VREF (default)  
1 = Input voltage range: 2 VREF

Bit 22  
PD_B: Power-down enable for channel pair B  
This bit is active in hardware mode.  
0 = Normal operation (default)  
1 = Channel pair B is powered down

Bit 21  
RANGE_C: Input voltage range selector for channel pair C  
This bit is not active in hardware mode.  
0 = Input voltage range: 4 VREF (default)  
1 = Input voltage range: 2 VREF

Bit 20  
PD_C: Power-down enable for channel pair C  
This bit is active in hardware mode.  
0 = Normal operation (default)  
1 = Channel pair C is powered down

Bit 19  
RANGE_D: Input voltage range selector for channel pair D  
This bit is not active in hardware mode.  
0 = Input voltage range: 4 VREF (default)  
1 = Input voltage range: 2 VREF

Bit 18  
PD_D: Power-down enable for channel pair D  
This bit is active in hardware mode.  
0 = Normal operation (default)  
1 = Channel pair D is powered down

Bits 17-16  
Not used (default = 0)

Bit 15  
REF_EN: Internal reference enable  
This bit is not active in hardware mode.  
0 = Internal reference source disabled (default)  
1 = Internal reference source enabled

Bit 14  
REFBUF: Internal reference buffers disable  
This bit is active in hardware mode if the parallel interface is used.  
0 = Internal reference buffers enabled (default)  
1 = Internal reference buffers disabled

Bit 13  
VREF: Internal reference voltage selector  
This bit is active in hardware mode.  
0 = Internal reference voltage set to 2.5 V (default)  
1 = Internal reference voltage set to 3.0 V

Bits 12-10  
Not used (default = 0)
Bits 9-0  D[9:0]: REFDAC setting bits
These bits are active in hardware mode.
These bits correspond to the settings of the internal reference DACs (compare to the Reference section). Bit 9 is the MSB of the DAC. Default value is 3FFh (2.5 V, typ).

10 Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information
The ADS85x8 enables high-precision measurement of up to eight analog signals simultaneously. The Typical Application section summarizes some of the typical use cases for the ADS85x8 and the main steps and components used around the analog-to-digital converter (ADC).

10.2 Typical Application
The accurate measurement of electrical variables in a power grid is extremely critical because this measurement helps determine the operating status and running quality of the grid. Such accurate measurements also help diagnose problems with the power network, thereby enabling prompt solutions and minimizing down time. The key electrical variables measured in 3-phase power systems are the three line voltages, the neutral voltage at the load, the three line currents, and the neutral return current; see Figure 45. These variables enable metrology and power automation systems to determine the amplitude, frequency, and phase information in order to perform harmonic analysis, power factor calculations, and power quality assessment, among others.
Figure 45. Simultaneous Acquisition of Voltage and Current in a 3-Phase Power System
Typical Application (continued)

10.2.1 Design Requirements

To begin the design process, a few parameters must be decided upon. The designer must know the following:

- Output range of the potential transformers (elements labeled PT1, PT2, and PT3 in Figure 45)
- Output range of the current transformers (elements labeled CT1, CT2, and CT3 in Figure 45)
- Input impedance required from the analog front-end for each channel
- Fundamental frequency of the power system
- Number of harmonics that must be acquired, and
- Type of signal conditioning required from the analog front-end for each channel

10.2.2 Detailed Design Procedure

Figure 46 shows the topology chosen to meet the design requirements.

\[ V_{out} \big|_{Low\, f} = -\frac{R_F}{R_{IN}} V_{in} = -\frac{100\, k\Omega}{100\, k\Omega} V_{in} = -V_{in} \]  
\( (5) \)

The primary goal of the acquisition system depicted in Figure 45 is to measure up to 20 harmonics in a 60-Hz power network. With this goal in mind, the analog front-end must have sufficient bandwidth to measure signals up to 1260 Hz as shown in Equation 6.

\[ f_{MAX} = (20 + 1)60\, Hz = 1260\, Hz \]  
\( (6) \)

Based on the bandwidth from in Equation 6, the ADS8568 is set to simultaneously sample all six channels at 15.36 kSPS, thus providing enough samples to clearly resolve even the highest harmonic required.

The passband of the configuration shown in Figure 46 is determined by the –3-dB frequency according to Equation 7. The value of \( C_F \) is selected as 820 pF because \( C_F \) is a standard capacitance value available in 0603 size (surface-mount component) and such values, combined with that of \( R_F \), result in sufficient bandwidth to accommodate the required 20 harmonics (at 60 Hz).
Typical Application (continued)

\[ f_{-3\text{dB}} = \frac{1}{2\pi R F C_F} = \frac{1}{2\pi (100 \text{ k}\Omega)(820 \text{ p}\text{F})} = 1940 \text{ Hz} \]  

(7)

The value of \( R_1 \) is selected as the parallel combination of \( R_{\text{IN}} \) and \( R_F \) to prevent the input bias current of the operational amplifier from generating an offset error.

The value of component \( C_1 \) is chosen as 0.1 \( \mu \text{F} \) to provide a low-impedance path for noise signals that can be picked up by \( R_1 \), thus improving the EMI robustness and noise performance of the system.

The OPA2277 is chosen for its low input offset voltage, low drift, bipolar swing, sufficient gain-bandwidth product, and low quiescent current. For additional information on the procedure to select SAR ADC input drivers, see the TIPD151 verified design guide, 16-Bit 100-KSPS 4-Channel Multiplexed Data Acquisition System Design Guide.

The charge injection damping circuit is composed by \( R_2 \) (49.9 \( \Omega \)) and \( C_2 \) (370 \( \text{pF} \)); these components reject high-frequency noise and meet the settling requirements of the ADS8568 input.

Figure 47 shows the reference block used in this design.

Figure 47. Reference Block

For more information on the design of charge injection damping circuits and reference driving circuits for SAR ADCs, see the TIPD149 verified design reference guide, Power-Optimized 16-Bit 1-MSPS Data Acquisition Block for Lowest Distortion and Noise.
Typical Application (continued)

10.2.3 Application Curve

Figure 48 shows the frequency spectrum of the data acquired by the ADS8568 for a sinusoidal, 20-V_{pp} input at 60 Hz.

The ac performance parameters are:
- SNR: 91.16 dB
- THD: −94.34 dB
- SNDR: 89.45 dB
- SFDR: 96.56 dB
11 Power Supply Recommendations

The ADS85x8 require four separate supplies: an analog supply for the ADC (AVDD), the buffer I/O supply for the digital interface (DVDD), and the two high-voltage supplies driving the analog input circuitry (HVDD and HVSS). Generally, there are no specific requirements with regard to the power sequencing of the device. However, when HVDD is supplied before AVDD, the internal electrostatic discharge (ESD) structure conducts, increasing the IHVDD beyond the specified value until AVDD is applied.

The AVDD supply provides power to the internal circuitry of the ADC. If run at maximum data rate, the IAVDD is too high to allow use of a passive filter between the digital board supply of the application and the AVDD pins. A linear regulator is recommended to generate the analog supply voltage. Decouple each AVDD pin to AGND with a 100-nF ceramic capacitor. In addition, place a single 10-µF capacitor close to the device but without compromising the placement of the smaller capacitors. Optionally, each supply pin can be decoupled using a 1-µF ceramic capacitor without the requirement of the additional 10-µF capacitor.

The DVDD supply is only used to drive the digital I/O buffers and allows seamless interface with most state-of-the-art processors and controllers. Resulting from the low IDVDD value, a 10-Ω series resistor can be used on the DVDD pin to reduce the noise energy from the external digital circuitry influencing the performance of the device. Place a 1-µF bypass ceramic capacitor (or alternatively, a pair of 100-nF and 10-µF capacitors) between pins 24 and 25.

The high-voltage supplies (HVSS and HVDD) are connected to the analog inputs. These supplies are not required to be of symmetrical nature with regard to AGND. Noise and glitches on these supplies directly couple into the input signals. Place a 100-nF ceramic decoupling capacitor, located as close to the device as possible, between pins 1, 48, and AGND. An additional 10-µF capacitor is used that must be placed close to the device but without compromising the placement of the smaller capacitors.

12 Layout

12.1 Layout Guidelines

All ground pins must be connected to a clean ground reference. Keep this connection as short as possible to minimize the inductance of these paths. Using vias is recommended to connect the pads directly to the corresponding ground plane. In designs without ground planes, keep the ground trace as wide and as short as possible to reduce inductance. Avoid connections that are too close to the grounding point of a microcontroller or digital signal processor.

Depending on the circuit density on the board, placement of the analog and digital components, and the related current loops, a single solid ground plane for the entire printed circuit board (PCB) or dedicated analog and digital ground areas can be used. In case of separated ground areas, ensure that a low-impedance connection is between the analog and digital ground of the ADC by placing a bridge underneath (or next to) the ADC. Otherwise, even short undershoots on the digital interface with a value less than –300 mV lead to the conduction of ESD diodes, causing current to flow through the substrate and either degrading the analog performance or even damaging the device. Using a common ground plane underneath the device is recommended as a local ground reference for all xGND pins; see Figure 49. During PCB layout, care must be taken to avoid any return currents crossing sensitive analog areas or signals.
12.2 Layout Example

Figure 49 shows a layout recommendation for the ADS85x8 along with the proper decoupling and reference capacitors placement and connections. The layout recommendation takes into account the actual size of the components used.

(1) All AVDD and DVDD decoupling capacitors are placed on the bottom layer underneath the device power-supply pins and are connected by vias. All 100-nF ceramic capacitors are placed as close as possible to the device and the 10-µF capacitors are also placed close but without compromising the placement of the smaller capacitors.

Figure 49. Layout Recommendation
13 デバイスおよびドキュメントのサポート

13.1 ドキュメントのサポート

13.1.1 関連資料
関連資料については、以下を参照してください:

- OPA2277データシート、SBOS079
- REF5025データシート、SBOS410
- TIPD151検証済み設計ガイド、『16ビット、100KSPS、4チャネル、多重化データ取得システムの設計ガイド』
- TIPD149検証済み設計リファレンス・ガイド、『歪みとノイズを最小限にする、電力最適化された16ビット、1MSPSデータ取得ブロック』

13.2 関連リンク
次の表に、クイック・アクセス・リンクを示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびサンプル注文またはご購入へのクイック・アクセスが含まれます。

表 5. 関連リンク

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13.3 コミュニティ・リソース
The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™オンライン・コミュニティ 『Engineer-to-Engineer (E2E)』 は、エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識共有し、アイディアを検討して、問題解決に役立てることができます。

設計サポート 『Engineer-to-Engineer (E2E)』 フォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

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13.6 Glossary
SLYZ022 — Ti Glossary.
This glossary lists and explains terms, acronyms, and definitions.

14 メカニカル、パッケージ、および注文情報
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<th>Package Qty</th>
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<th>Lead/Ball Finish</th>
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(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBsolete: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
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**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) **Lead/Ball Finish** - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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### TAPE AND REEL INFORMATION

#### TAPE DIMENSIONS

| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W  | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

#### REEL DIMENSIONS

- **Reel Diameter**
- **Reel Width (W1)**

#### PACKAGE MATERIALS INFORMATION

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<th>Device</th>
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*All dimensions are nominal.*
### TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal*

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<th>Package Drawing</th>
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Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026
D. May also be thermally enhanced plastic with leads connected to the die pads.
PM (S-PQFP-G64)  PLASTIC QUAD FLATPACK

Example Board Layout

Stencil Openings
Based on a stencil thickness of .127mm (.005 inch).

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
D. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
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