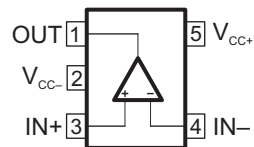


## LOW-POWER SINGLE OPERATIONAL AMPLIFIER

### FEATURES

- **Qualified for Automotive Applications**
- **Wide Power-Supply Range**
  - **Single Supply: 3 V to 30 V**
  - **Dual Supply:  $\pm 1.5$  V to  $\pm 15$  V**
- **Large Output Voltage Swing:**  
**0 V to 3.5 V (Min) ( $V_{CC} = 5$  V)**
- **Low Supply Current: 500  $\mu$ A (Typ)**
- **Low Input Bias Current: 20 nA (Typ)**
- **Stable With High Capacitive Loads**

**DBV (SOT-23-5) PACKAGE  
(TOP VIEW)**


### DESCRIPTION/ORDERING INFORMATION

The TS321 is a bipolar operational amplifier for cost-sensitive applications in which space savings are important.

#### ORDERING INFORMATION<sup>(1)</sup>

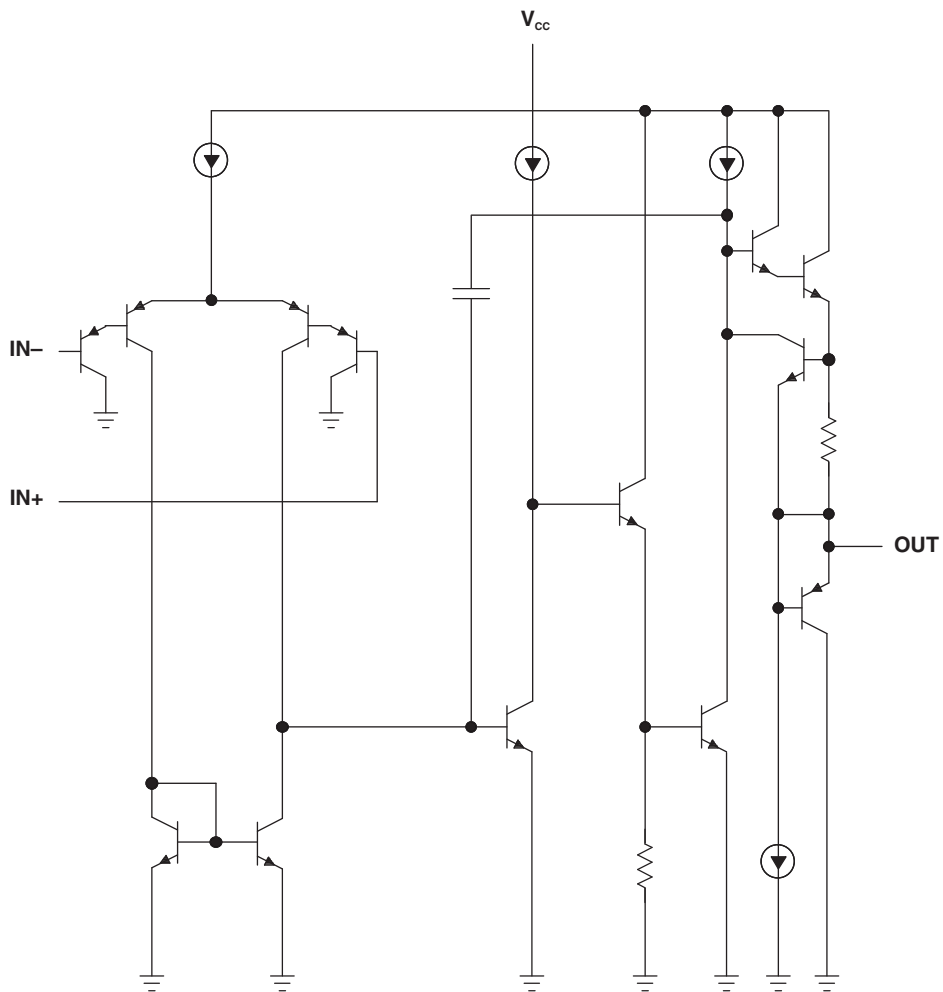
$T_A$	PACKAGE <sup>(2)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	SOT-23-5 – DBV	Reel of 3000	TS321QDBVRQ1	9CNS

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).
- (2) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).



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SCHMATIC DIAGRAM



## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage <sup>(2)</sup>	Single	32	V
		Dual	±16	
V <sub>ID</sub>	Differential input voltage <sup>(3)</sup>		32	V
V <sub>I</sub>	Input voltage range <sup>(2)(4)</sup>	–0.3	32	V
I <sub>I</sub>	Input current <sup>(4)</sup>		50	mA
t <sub>short</sub>	Duration of output short circuit to ground		Unlimited	
θ <sub>JA</sub>	Package thermal impedance, junction to free air <sup>(5)(6)</sup>	DBV package	206	°C/W
T <sub>J</sub>	Operating virtual junction temperature		150	°C
T <sub>stg</sub>	Storage temperature range	–65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) These voltage values are with respect to the midpoint between V<sub>CC+</sub> and V<sub>CC–</sub>.
- (3) Differential voltages are at IN+ with respect to IN–.
- (4) Neither input must ever be more positive than V<sub>CC+</sub> or more negative than V<sub>CC–</sub>.
- (5) Maximum power dissipation is a function of T<sub>J(max)</sub>, θ<sub>JA</sub>, and T<sub>A</sub>. The maximum allowable power dissipation at any allowable ambient temperature is P<sub>D</sub> = (T<sub>J(max)</sub> – T<sub>A</sub>)/θ<sub>JA</sub>. Selecting the maximum of 150°C can affect reliability.
- (6) The package thermal impedance is calculated in accordance with JESD 51-7.

## RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	Single supply	3	V
		Dual supply	±1.5	
T <sub>A</sub>	Operating free-air temperature	–40	125	°C

**ELECTRICAL CHARACTERISTICS**

V<sub>CC+</sub> = 5 V, V<sub>CC-</sub> = GND, V<sub>O</sub> = 1.4 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T <sub>A</sub>	MIN	TYP	MAX	UNIT	
V <sub>IO</sub>	Input offset voltage	R <sub>S</sub> = 0, 5 V < V <sub>CC+</sub> < 30 V, 0 < V <sub>IC</sub> < (V <sub>CC+</sub> – 1.5 V)	25°C		0.5	4	mV	
			Full range			5		
I <sub>IO</sub>	Input offset current		25°C		2	30	nA	
			Full range			50		
I <sub>IB</sub>	Input bias current <sup>(1)</sup>		25°C		20	150	nA	
			Full range			200		
A <sub>VD</sub>	Large-signal differential voltage amplification	V <sub>CC</sub> = 15 V, R <sub>L</sub> = 2 kΩ, V <sub>O</sub> = 1.4 V to 11.4 V	25°C	50	100		V/mV	
			Full range	25				
V <sub>ICR</sub>	Common-mode input voltage <sup>(2)</sup>	V <sub>CC</sub> = 30 V	25°C	0		V <sub>CC+</sub> – 1.5	V	
			Full range	0		V <sub>CC+</sub> – 2		
V <sub>OH</sub>	High-level output voltage	V <sub>CC</sub> = 30 V	R <sub>L</sub> = 2 kΩ	25°C	26	27	V	
				Full range	25.5			
			R <sub>L</sub> = 10 kΩ	25°C	27	28		
				Full range	26.5			
		V <sub>CC</sub> = 5 V	R <sub>L</sub> = 2 kΩ	25°C	3.5			
				Full range	3			
V <sub>OL</sub>	Low-level output voltage	R <sub>L</sub> = 10 kΩ	25°C		5	15	mV	
			Full range			20		
GBP	Gain bandwidth product	V <sub>CC</sub> = 30 V, V <sub>I</sub> = 10 mV, R <sub>L</sub> = 2 kΩ, f = 100 kHz, C <sub>L</sub> = 100 pF	25°C		0.8		MHz	
SR	Slew rate	V <sub>CC</sub> = 15 V, V <sub>I</sub> = 0.5 V to 3 V, R <sub>L</sub> = 2 kΩ, C <sub>L</sub> = 100 pF, unity gain	25°C		0.4		V/μs	
φ <sub>m</sub>	Phase margin		25°C		60		°	
CMRR	Common-mode rejection ratio	R <sub>S</sub> ≤ 10 kΩ	25°C	65	85		dB	
I <sub>SOURCE</sub>	Output source current	V <sub>CC</sub> = 15 V, V <sub>O</sub> = 2 V, V <sub>ID</sub> = 1 V	25°C	20	40		mA	
I <sub>SINK</sub>	Output sink current	V <sub>CC</sub> = 15 V, V <sub>ID</sub> = 1 V	V <sub>O</sub> = 2 V	25°C	10	20	mA	
			V <sub>O</sub> = 0.2 V	25°C	12	50	μA	
I <sub>O</sub>	Short-circuit to GND	V <sub>CC</sub> = 15 V	25°C		40	60	mA	
SVR	Supply-voltage rejection ratio	V <sub>CC</sub> = 5 V to 30 V	25°C	65	110		dB	
I <sub>CC</sub>	Total supply current	No load	25°C	V <sub>CC</sub> = 5 V		500	800	μA
				V <sub>CC</sub> = 30 V		600	900	
			Full range	V <sub>CC</sub> = 5 V		600	900	
				V <sub>CC</sub> = 30 V			1000	
THD	Total harmonic distortion	V <sub>CC</sub> = 30 V, V <sub>O</sub> = 2 V <sub>pp</sub> , A <sub>V</sub> = 20 dB, R <sub>L</sub> = 2 kΩ, f = 1 kHz, C <sub>L</sub> = 100 pF	25°C		0.015		%	
e <sub>N</sub>	Equivalent input noise voltage	V <sub>CC</sub> = 30 V, f = 1 kHz, R <sub>S</sub> = 100 Ω	25°C		50		nV/√Hz	

- (1) The direction of the input current is out of the device. This current essentially is constant, independent of the state of the output, so no loading change exists on the input lines.
- (2) The input common-mode voltage of either input signal should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is V<sub>CC+</sub> – 1.5 V, but either or both inputs can go to 32 V without damage.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TS321QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	9CNS	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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**OTHER QUALIFIED VERSIONS OF TS321-Q1 :**

- Catalog: [TS321](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS321QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS321QDBVRQ1	SOT-23	DBV	5	3000	202.0	201.0	28.0



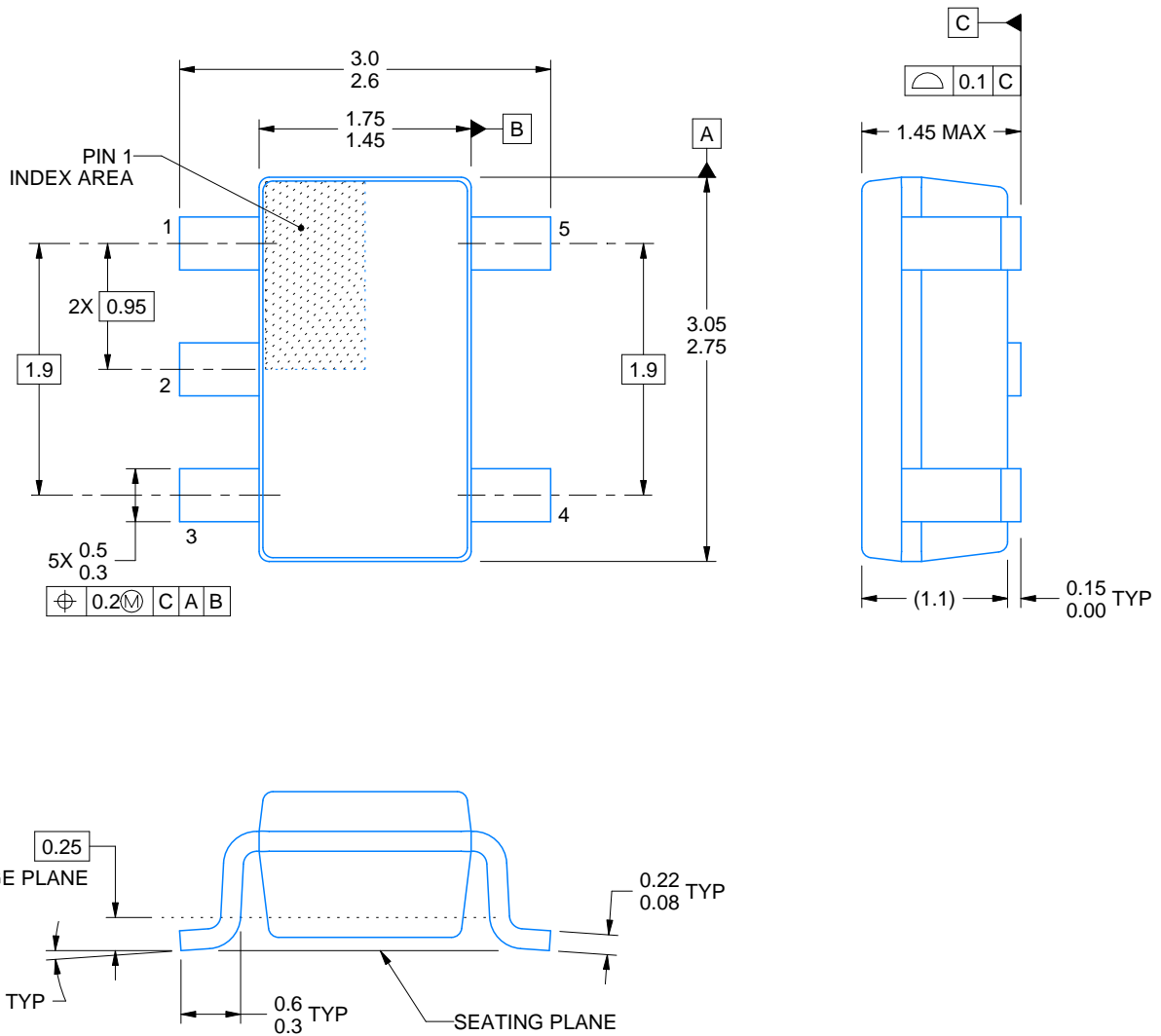
DBV0005A



# PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/D 11/2018

NOTES:

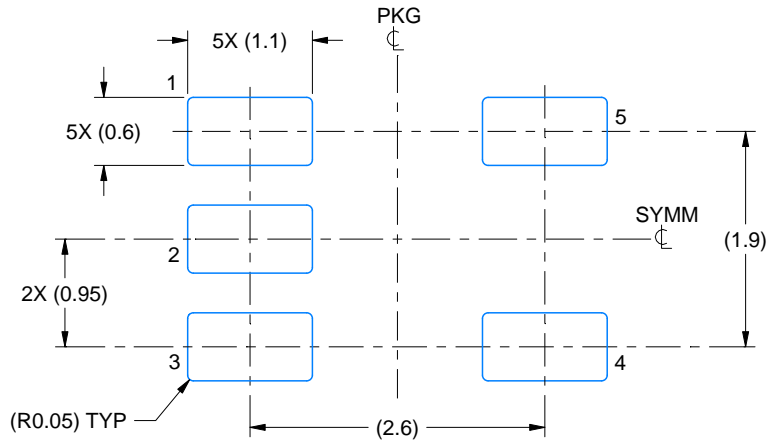
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

# EXAMPLE BOARD LAYOUT

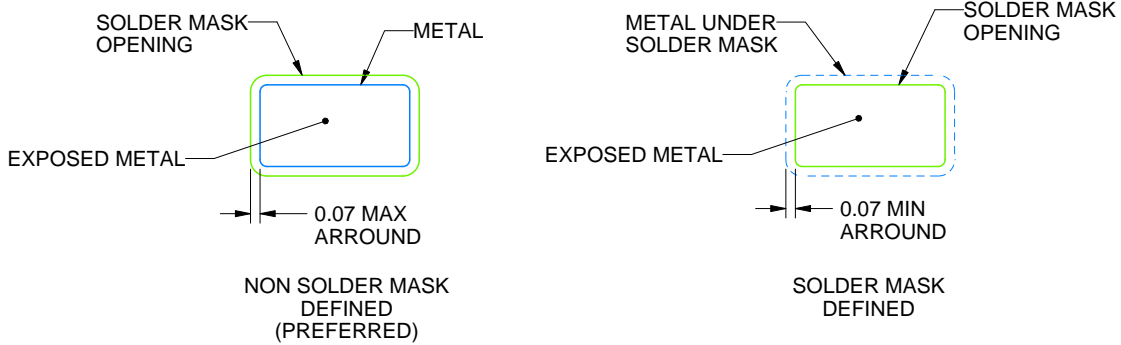
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

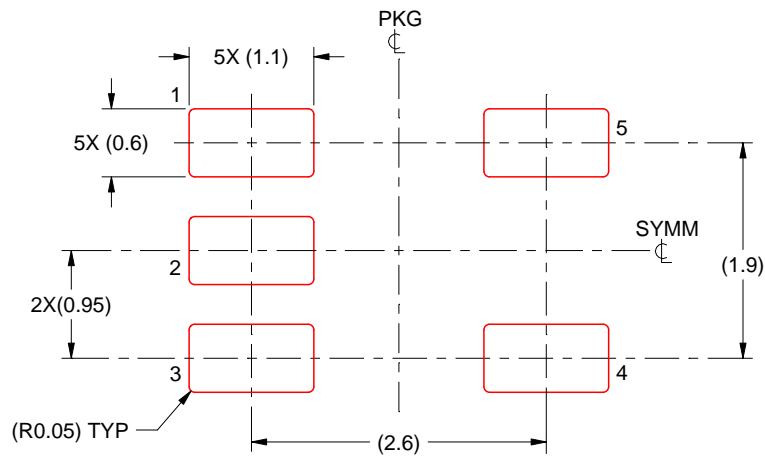
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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