μA741汎用オペアンプ

1 特長
• 短絡保護
• オフセット電圧のNull機能
• 広い同相および差動電圧範囲
• 周波数補償が不要
• ラッチアップなし

2 アプリケーション
• DVDレコーダーおよびプレーヤー
• プロ用オーディオ・ミキサー

3 概要
μA741デバイスは汎用オペアンプで、オフセット電圧のNull機能が搭載されています。

同相入力電圧範囲が広く、ラッチアップがないため、このアンプは電圧フォロワー・アプリケーションに最適です。このデバイスは短絡保護されており、内部の周波数補償により、外部部品なしに安定が保証されます。

図12に示すように、値の低いポテンショメータをオフセットNull入力の間に接続して、オフセット電圧を打ち消すことができます。

μA741Cデバイスは、0℃～70℃での動作が規定されています。

製品情報(1)

<table>
<thead>
<tr>
<th>型番</th>
<th>パッケージ</th>
<th>本体サイズ(公称)</th>
</tr>
</thead>
<tbody>
<tr>
<td>µA741CD</td>
<td>SOIC (8)</td>
<td>4.90mm×3.91mm</td>
</tr>
<tr>
<td>µA741CP</td>
<td>PDIP (8)</td>
<td>9.81mm×6.35mm</td>
</tr>
<tr>
<td>µA741CPS</td>
<td>SO (8)</td>
<td>6.20mm×5.30mm</td>
</tr>
</tbody>
</table>

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

概略回路図

OFFSET N1
IN +
OUT
IN –
OFFSET N2
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4 改訂履歴

Revision F (May 2017) から Revision G に変更

Page

- Changed supply voltage unit from "°C" to "V" in Absolute Maximum Ratings table ........................................ 5

Revision E (January 2015) から Revision F に変更

Page

- 最新のドキュメントおよび翻訳標準に合わせて、データシートのテキストを更新 .............................................. 1
- 「概要」セクションからμA741M (製造終了パッケージ)に関するテキストを削除 .............................................. 1
- 「製品情報」表にμA741CD、μA741GP、μA741CPSデバイスを追加 .............................................. 1
- 「製品情報」表からμA741Xデバイスを削除 .............................................. 1
- Updated pinout diagrams and Pin Functions tables in the Pin Configurations and Functions section ........................................ 4
- Deleted μA741M pinout drawings information from Pin Configurations and Functions section ........................................ 4
- Deleted Electrical Characteristics: μA741M table from Specifications section ........................................ 5
- Added operating junction temperature (Tj) and values to Absolute Maximum Ratings table ........................................ 5
- Deleted text regarding μA741M from Absolute Maximum Ratings table ........................................ 5
- Deleted text regarding μA741M device from Recommended Operating Conditions table ........................................ 5
- Deleted Dissipation Ratings table ........................................ 5
- Added Thermal Information table and values ........................................ 5
- Deleted μA741M in Switching Characteristics table ........................................ 7
- Correct typo in 図 1 ........................................ 8
- 削除 text regarding μA741M device from Detailed Description section ........................................ 10
- Updated text in Overview section ........................................ 10
- 追加 2017 copyright to Functional Block Diagram ........................................ 10
- 追加 caption to 図 11 in Device Functional Modes section ........................................ 11
- 変更 pins 1 and 5 from "NC" to "Offset N1" and "Offset N2" in 図 18 ........................................ 15
Revision D (February 2014) から Revision E に変更

- 「アプリケーション」セクション、「製品情報」表、「ピン機能」表、「ESD定格」表、「熱に関する情報」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加。1
- Moved Typical Characteristics into Specifications section. .................................................. 8

Revision C (January 2014) から Revision D に変更

- Fixed Typical Characteristics graphs to remove extra lines. ........................................... 8

Revision B (September 2000) から Revision C に変更

- 新しいTIデータシート・フォーマットにドキュメントを更新 - 仕様変更なし。1
- 「注文情報」表を削除。1
5 Pin Configurations and Functions

uA741C D, P, or PS Package
8-Pin SOIC, PDIP, SO
Top View

OFFSET N1 1 8 NC
IN– 2 7 VCC+
IN+ 3 6 OUT
VCC– 4 5 OFFSET N2

NC- no internal connection

Pin Functions

<table>
<thead>
<tr>
<th>PIN</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>IN+</td>
<td>3</td>
<td>I Noninverting input</td>
</tr>
<tr>
<td>IN–</td>
<td>2</td>
<td>I Inverting input</td>
</tr>
<tr>
<td>NC</td>
<td>8</td>
<td>— No internal connection</td>
</tr>
<tr>
<td>OFFSET N1</td>
<td>1</td>
<td>I External input offset voltage adjustment</td>
</tr>
<tr>
<td>OFFSET N2</td>
<td>5</td>
<td>I External input offset voltage adjustment</td>
</tr>
<tr>
<td>OUT</td>
<td>6</td>
<td>O Output</td>
</tr>
<tr>
<td>VCC+</td>
<td>7</td>
<td>— Positive supply</td>
</tr>
<tr>
<td>VCC–</td>
<td>4</td>
<td>— Negative supply</td>
</tr>
</tbody>
</table>
6 Specifications

6.1 Absolute Maximum Ratings

over virtual junction temperature range (unless otherwise noted)\(^{(1)}\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage, (V_{\text{CC}})(^{(2)})</td>
<td>(\mu A741C)</td>
<td>–18</td>
<td>18</td>
</tr>
<tr>
<td>Differential input voltage, (V_{\text{di}})(^{(3)})</td>
<td>(\mu A741C)</td>
<td>–15</td>
<td>15</td>
</tr>
<tr>
<td>Input voltage, (V_I) (any input) (^{(2)(4)})</td>
<td>(\mu A741C)</td>
<td>–15</td>
<td>15</td>
</tr>
<tr>
<td>Voltage between offset null (either OFFSET N1 or OFFSET N2) and (V_{\text{CC}})–</td>
<td>(\mu A741C)</td>
<td>–15</td>
<td>15</td>
</tr>
<tr>
<td>Duration of output short circuit(^{(5)})</td>
<td>Unlimited</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Continuous total power dissipation</td>
<td>See <a href="#">Thermal Information</a></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Case temperature for 60 seconds</td>
<td>(\mu A741C)</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>Lead temperature 1.6 mm (1/16 inch) from case for 60 seconds</td>
<td>(\mu A741C)</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds</td>
<td>D, P, or PS package</td>
<td>(\mu A741C)</td>
<td>260</td>
</tr>
<tr>
<td>Operating junction temperature, (T_J)</td>
<td></td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>Storage temperature range, (T_{\text{stg}})</td>
<td></td>
<td>(\mu A741C)</td>
<td>–65</td>
</tr>
</tbody>
</table>

\(^{(1)}\) Stresses beyond those listed under **Absolute Maximum Ratings** may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under **Recommended Operating Conditions** is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

\(^{(2)}\) All voltage values, unless otherwise noted, are with respect to the midpoint between \(V_{\text{CC}+}\) and \(V_{\text{CC}–}\).

\(^{(3)}\) Differential voltages are at \(I_{\text{IN}+}\) with respect to \(I_{\text{IN}–}\).

\(^{(4)}\) The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.

\(^{(5)}\) The output may be shorted to ground or either power supply.

6.2 Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{\text{CC}+})</td>
<td></td>
<td>5</td>
<td>15</td>
</tr>
<tr>
<td>(V_{\text{CC}–})</td>
<td></td>
<td>–5</td>
<td>–15</td>
</tr>
<tr>
<td>(T_A)</td>
<td></td>
<td>0</td>
<td>70</td>
</tr>
</tbody>
</table>

6.3 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC(^{(1)})</th>
<th>(\mu A741)</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(R_{\text{JA}}) Junction-to-ambient thermal resistance</td>
<td>D (SOIC)</td>
<td>P (PDIP)</td>
</tr>
<tr>
<td>8 PINS</td>
<td>8 PINS</td>
<td>8 PINS</td>
</tr>
<tr>
<td>129.2</td>
<td>87.4</td>
<td>119.7</td>
</tr>
<tr>
<td>(R_{\text{JUC(top)}}) Junction-to-case (top) thermal resistance</td>
<td></td>
<td></td>
</tr>
<tr>
<td>73.6</td>
<td>89.3</td>
<td>66</td>
</tr>
<tr>
<td>(R_{\text{JB}}) Junction-to-board thermal resistance</td>
<td></td>
<td></td>
</tr>
<tr>
<td>72.4</td>
<td>64.4</td>
<td>70</td>
</tr>
<tr>
<td>(\psi_{\text{JT}}) Junction-to-top characterization parameter</td>
<td></td>
<td></td>
</tr>
<tr>
<td>25.9</td>
<td>49.8</td>
<td>27.2</td>
</tr>
<tr>
<td>(\psi_{\text{JB}}) Junction-to-board characterization parameter</td>
<td></td>
<td></td>
</tr>
<tr>
<td>71.7</td>
<td>64.1</td>
<td>69</td>
</tr>
</tbody>
</table>

\(^{(1)}\) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.
### 6.4 Electrical Characteristics: µA741C

at specified virtual junction temperature, $V_{CCx} = \pm 15$ V (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS(1)</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IC}$ Input offset voltage</td>
<td>$V_O = 0$</td>
<td>25°C</td>
<td>1</td>
<td>6</td>
<td>mV</td>
</tr>
<tr>
<td>$\Delta V_{IO(adj)}$ Offset voltage adjust range</td>
<td>$V_O = 0$</td>
<td>25°C</td>
<td>±15</td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>$I_{IO}$ Input offset current</td>
<td>$V_O = 0$</td>
<td>25°C</td>
<td>20</td>
<td>200</td>
<td>nA</td>
</tr>
<tr>
<td>$I_{IB}$ Input bias current</td>
<td>$V_O = 0$</td>
<td>25°C</td>
<td>80</td>
<td>500</td>
<td>nA</td>
</tr>
<tr>
<td>$V_{ICR}$ Common-mode input voltage range</td>
<td>25°C</td>
<td>±12</td>
<td>±13</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{OM}$ Maximum peak output voltage swing</td>
<td>$R_L = 10$ kΩ</td>
<td>25°C</td>
<td>±12</td>
<td>±14</td>
<td>V</td>
</tr>
<tr>
<td>$A_{V0}$ Large-signal differential voltage amplification</td>
<td>$R_L \geq 2$ kΩ</td>
<td>25°C</td>
<td>±10</td>
<td></td>
<td>V/mV</td>
</tr>
<tr>
<td>$r_i$ Input resistance</td>
<td>25°C</td>
<td>0.3</td>
<td>2</td>
<td></td>
<td>MΩ</td>
</tr>
<tr>
<td>$C_i$ Input capacitance</td>
<td>25°C</td>
<td>1.4</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>CMRR Common-mode rejection ratio</td>
<td>$V_{IC} = V_{CRin}$</td>
<td>25°C</td>
<td>70</td>
<td>90</td>
<td>dB</td>
</tr>
<tr>
<td>$k_{SVS}$ Supply voltage sensitivity ($\Delta V_O/\Delta V_{CC}$)</td>
<td>$V_{CC} = \pm 9$ V to $\pm 15$ V</td>
<td>25°C</td>
<td>30</td>
<td>150</td>
<td>µV/V</td>
</tr>
<tr>
<td>$I_{OS}$ Short-circuit output current</td>
<td>25°C</td>
<td>±25</td>
<td>±40</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>$I_{CC}$ Supply current</td>
<td>$V_O = 0$; no load</td>
<td>25°C</td>
<td>1.7</td>
<td>2.8</td>
<td>mA</td>
</tr>
<tr>
<td>$P_D$ Total power dissipation</td>
<td>$V_O = 0$; no load</td>
<td>25°C</td>
<td>50</td>
<td>85</td>
<td>mW</td>
</tr>
</tbody>
</table>

(1) All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range for the µA741C is 0°C to 70°C.

(2) This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.
### 6.5 Electrical Characteristics: μA741Y

at specified virtual junction temperature, $V_{CCX} = ±15$ V, $T_A = 25^\circ$C (unless otherwise noted)\(^{(1)}\)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS (^{(2)})</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IO}$</td>
<td>$V_O = 0$</td>
<td>1</td>
<td>5</td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>$\Delta V_{IO(adj)}$</td>
<td>$V_O = 0$</td>
<td>±15</td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>$I_O$</td>
<td>$V_O = 0$</td>
<td>20</td>
<td>200</td>
<td></td>
<td>nA</td>
</tr>
<tr>
<td>$I_{IB}$</td>
<td>$V_O = 0$</td>
<td>80</td>
<td>500</td>
<td></td>
<td>nA</td>
</tr>
<tr>
<td>$V_{ICR}$</td>
<td></td>
<td>±12</td>
<td>±13</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{OM}$</td>
<td>$R_L = 10$ kΩ $\leq 2$ kΩ</td>
<td>±12</td>
<td>±14</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$A_{VO}$</td>
<td>$R_I = 2$ kΩ $\leq 2$ kΩ</td>
<td>20</td>
<td>200</td>
<td></td>
<td>V/mV</td>
</tr>
<tr>
<td>$r_i$</td>
<td>$V_O = 0$; see (^{(1)})</td>
<td>0.3</td>
<td>2</td>
<td></td>
<td>MΩ</td>
</tr>
<tr>
<td>$r_o$</td>
<td></td>
<td>75</td>
<td></td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td>$C_i$</td>
<td></td>
<td>1.4</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>CMRR</td>
<td>$V_{IC} = V_{CRHP}$</td>
<td>70</td>
<td>90</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>$k_{SVS}$</td>
<td>$V_{CC} = ±19$ V to ±15 V</td>
<td>30</td>
<td>150</td>
<td></td>
<td>µV/V</td>
</tr>
<tr>
<td>$I_{OS}$</td>
<td></td>
<td>±25</td>
<td>±40</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>$I_{CC}$</td>
<td>$V_O = 0$; no load</td>
<td>1.7</td>
<td>2.8</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>$P_D$</td>
<td>$V_O = 0$; no load</td>
<td>50</td>
<td>85</td>
<td></td>
<td>mW</td>
</tr>
</tbody>
</table>

\(^{(1)}\) This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.

\(^{(2)}\) All characteristics are measured under open-loop conditions with zero common-mode voltage unless otherwise specified.

### 6.6 Switching Characteristics: μA741C

over operating free-air temperature range, $V_{CCX} = ±15$ V, $T_A = 25^\circ$C (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_r$</td>
<td>$V_I = 20$ mV, $R_L = 2$ kΩ $C_L = 100$ pF; see (\text{図} 1)</td>
<td>0.3</td>
<td></td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>$Overshoot$</td>
<td></td>
<td>5%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$SR$</td>
<td>$V_I = 10$ V, $R_L = 2$ kΩ $C_L = 100$ pF; see (\text{図} 1)</td>
<td>0.5</td>
<td></td>
<td></td>
<td>V/µs</td>
</tr>
</tbody>
</table>

### 6.7 Switching Characteristics: μA741Y

over operating free-air temperature range, $V_{CCX} = ±15$ V, $T_A = 25^\circ$C (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_r$</td>
<td>$V_I = 20$ mV, $R_L = 2$ kΩ $C_L = 100$ pF; see (\text{図} 1)</td>
<td>0.3</td>
<td></td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>$Overshoot$</td>
<td></td>
<td>5%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$SR$</td>
<td>$V_I = 10$ V, $R_L = 2$ kΩ $C_L = 100$ pF; see (\text{図} 1)</td>
<td>0.5</td>
<td></td>
<td></td>
<td>V/µs</td>
</tr>
</tbody>
</table>
6.8 Typical Characteristics

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

![Test Circuit Diagram](image)

**図 1. Rise Time, Overshoot, and Slew Rate**

**図 2. Input Offset Current vs Free-Air Temperature**

**図 3. Input Bias Current vs Free-Air Temperature**

**図 4. Maximum Output Voltage vs Load Resistance**

**図 5. Maximum Peak Output Voltage vs Frequency**
Typical Characteristics (continued)

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

![Graphs showing various characteristics](image-url)

- **Graph 6. Open-Loop Signal Differential Voltage Amplification vs Supply Voltage**
- **Graph 7. Open-Loop Large-Signal Differential Voltage Amplification vs Frequency**
- **Graph 8. Common-Mode Rejection Ratio vs Frequency**
- **Graph 9. Output Voltage vs Elapsed Time**
- **Graph 10. Voltage-Follower Large-Signal Pulse Response**
7 Detailed Description

7.1 Overview
The μA741 has been a popular operational amplifier for over four decades. Typical open loop gain is 106 dB while driving a 2000-Ω load. Short circuit tolerance, offset voltage trimming, and unity-gain stability makes the μA741 useful for many applications.

7.2 Functional Block Diagram

7.3 Feature Description
7.3.1 Offset-Voltage Null Capability
The input offset voltage of operational amplifiers (op amps) arises from unavoidable mismatches in the differential input stage of the op-amp circuit caused by mismatched transistor pairs, collector currents, current-gain betas (β), collector or emitter resistors and so forth. The input offset pins allow the designer to adjust for mismatches caused by external circuitry. See Application and Implementation for more details on design techniques.
Feature Description (continued)

7.3.2 Slew Rate
The slew rate is the rate at which an operational amplifier can change an output when there is a change on the input. The µA741 device has a 0.5-V/\mu s slew rate. Parameters that vary significantly with operating voltages or temperature are shown in *Typical Characteristics*.

7.4 Device Functional Modes
The µA741 device is powered on when the power supply is connected. The device can operate as a single-supply or dual-supply operational amplifier depending on the application.

7.5 µA741Y Chip Information
When properly assembled, this chip displays characteristics similar to the µA741C device. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips can be mounted with conductive epoxy or a gold-silicon preform.

![BONDING PAD ASSIGNMENTS](image)

**CHIP THICKNESS:** 15 TYPICAL
**BONDING PADS:** 4 x 4 MINIMUM

\[ T_{J_{\text{max}}} = 150 \, ^\circ \text{C}. \]

**TOLERANCES ARE \pm 10\%.

**ALL DIMENSIONS ARE IN MILS.**

*図 11. Bonding Pad Assignments*
8 Application and Implementation

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The input offset voltage of operational amplifiers (op amps) arises from unavoidable mismatches in the differential input stage of the op-amp circuit caused by mismatched transistor pairs, collector currents, current-gain betas ($\beta$), collector or emitter resistors and so forth. The input offset pins allow the designer to adjust for mismatches resulting from external circuitry. These input mismatches can be adjusted by placing resistors or a potentiometer between the inputs as shown in 图 12. A potentiometer can fine-tune the circuit during testing or for applications which require precision offset control. For more information about designing using the input-offset pins, see Nulling Input Offset Voltage of Operational Amplifiers.

图 12. Input Offset Voltage Null Circuit

8.2 Typical Application

The voltage follower configuration of the operational amplifier is used for applications where a weak signal drives a relatively high current load. This circuit is also called a buffer amplifier or unity-gain amplifier. The inputs of an operational amplifier have a very high resistance which puts a negligible current load on the voltage source. The output resistance of the operational amplifier is almost negligible, so the resistance can provide as much current as necessary to the output load.

图 13. Voltage Follower Schematic
Typical Application (continued)

8.2.1 Design Requirements
- Output range from 2 V to 11.5 V
- Input range from 2 V to 11.5 V
- Resistive feedback to negative input

8.2.2 Detailed Design Procedure

8.2.2.1 Output Voltage Swing
The output voltage of an operational amplifier is limited by the internal circuitry to some level below the supply rails. For this amplifier, the output voltage swing is within ±12 V, which accommodates the input and output voltage requirements.

8.2.2.2 Supply and Input Voltage
For correct operation of the amplifier, neither input must be higher than the recommended positive supply rail voltage or lower than the recommended negative supply rail voltage. The selected amplifier must be able to operate at the supply voltage that accommodates the inputs. Because the input for this application goes up to 11.5 V, the supply voltage must be 12 V. Using a negative voltage on the lower rail rather than ground allows the amplifier to maintain linearity for inputs below 2 V.

8.2.3 Application Curves for Output Characteristics

- **図14. Output Voltage vs Input Voltage**
- **図15. Current Drawn Input of Voltage Follower (I<sub>IO</sub>) vs Input Voltage**
- **図16. Current Drawn from Supply (I<sub>CC</sub>) vs Input Voltage**
9 Power Supply Recommendations

The μA741 device is specified for operation from ±5 to ±15 V; many specifications apply from 0°C to 70°C. Typical Characteristics presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

Place 0.1-μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies. For more detailed information on bypass capacitor placement, see Layout Guidelines.

Supply voltages larger than ±18 V can permanently damage the device (see Absolute Maximum Ratings).

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and the operational amplifier. Bypass capacitors reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-μF ceramic bypass capacitors between each supply pin and ground, placed as close as possible to the device. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, see Circuit Board Layout Techniques.
- To reduce parasitic coupling, run the input traces as far away as possible from the supply or output traces. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close as possible to the device. Keeping RF and RG close to the inverting input minimizes parasitic capacitance, as shown in Layout Example.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

10.2 Layout Example

![Operational Amplifier Schematic for Noninverting Configuration](image-url)
Run the input traces as far away from the supply lines as possible.

Only needed for dual-supply operation.

Place components close to device and to each other to reduce parasitic errors.

Use low-ESR, ceramic bypass capacitor

Ground (GND) plane on another layer.

**図 18. Operational Amplifier Board Layout for Noninverting Configuration**
11 デバイスおよびドキュメントのサポート

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11.4 Glossary
SLYZ022 — Ti Glossary.
This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報
以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。これらの情報は、指定のデバイスに対して提供されている最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。このデータシートのブラウザ対応版については、左側にあるナビゲーションを参照してください。
### Packaging Information

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>UA741CD</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>75</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>0 to 70</td>
<td>UA741C</td>
<td></td>
</tr>
<tr>
<td>UA741CDR</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>2500</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>0 to 70</td>
<td>UA741C</td>
<td></td>
</tr>
<tr>
<td>UA741CDRG4</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>2500</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>0 to 70</td>
<td>UA741C</td>
<td></td>
</tr>
<tr>
<td>UA741CP</td>
<td>ACTIVE</td>
<td>PDIP</td>
<td>P</td>
<td>8</td>
<td>50</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>N / A for Pkg Type</td>
<td>0 to 70</td>
<td>UA741CP</td>
<td></td>
</tr>
<tr>
<td>UA741CPE4</td>
<td>ACTIVE</td>
<td>PDIP</td>
<td>P</td>
<td>8</td>
<td>50</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>N / A for Pkg Type</td>
<td>0 to 70</td>
<td>UA741CP</td>
<td></td>
</tr>
<tr>
<td>UA741CPSR</td>
<td>ACTIVE</td>
<td>SO</td>
<td>PS</td>
<td>8</td>
<td>2000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>0 to 70</td>
<td>U741</td>
<td></td>
</tr>
<tr>
<td>UA741CPSRE4</td>
<td>ACTIVE</td>
<td>SO</td>
<td>PS</td>
<td>8</td>
<td>2000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>0 to 70</td>
<td>U741</td>
<td></td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

(2) **RoHS**: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
- **RoHS Exempt**: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
- **Green**: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.** - Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**REEL DIMENSIONS**

**TAPE DIMENSIONS**

A0  | Dimension designed to accommodate the component width
B0  | Dimension designed to accommodate the component length
K0  | Dimension designed to accommodate the component thickness
W   | Overall width of the carrier tape
P1  | Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>UA741CDR</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>2500</td>
<td>330.0</td>
<td>12.4</td>
<td>6.4</td>
<td>5.2</td>
<td>2.1</td>
<td>8.0</td>
<td>12.0</td>
<td>Q1</td>
</tr>
</tbody>
</table>
## TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>UA741CDR</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>2500</td>
<td>340.5</td>
<td>338.1</td>
<td>20.6</td>
</tr>
</tbody>
</table>
NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.
MECHANICAL DATA

PS (R-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.15.
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
MECHANICAL DATA

P (R-PDIP-T8)  PLASTIC DUAL-IN-LINE PACKAGE

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001 variation BA.
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