SNx4AC240 3 ステート出力、オクタル・バッファ / ドライバ

1 特長

- 2V～6V の V_{CC} で動作
- 最大 t_{pd} 6.5ns (5V 時)
- 6V までの入力電圧に対応

2 アプリケーション

- ハンドセット：スマートフォン
- ネットワーク・スイッチ
- 健康管理およびフィットネス / ウェアラブル

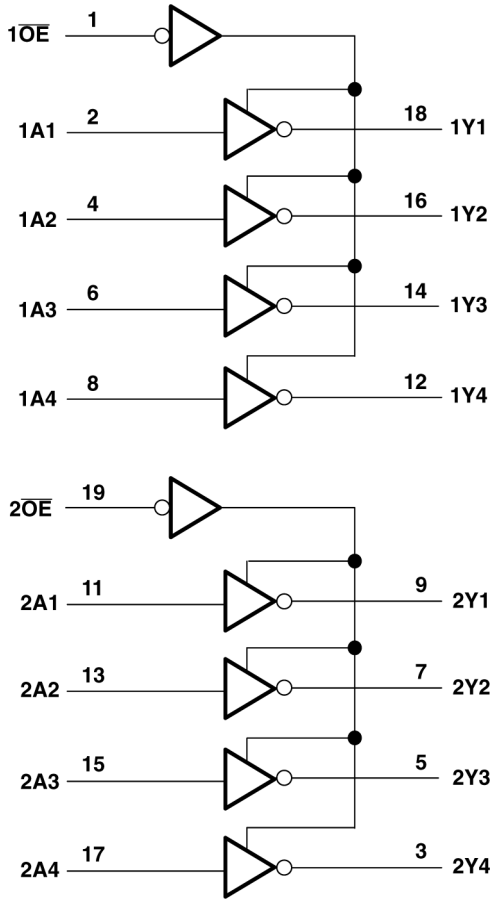
3 概要

これらのオクタル・バッファ / ライン・ドライバは、3 ステート・メモリ・アドレス・ドライバ、クロック・ドライバ、バス用レシーバ / トランスミッタの性能と密度を向上することに特化して設計されています。

パッケージ情報

部品番号	パッケージ(1)	本体サイズ (公称)
SN54AC240	J (CDIP、20)	24.2mm × 6.92mm
	W (CFP、20)	13.09mm × 6.92mm
	FK (LCCC、20)	8.89mm × 8.89mm
SN74AC240	N (PDIP、20)	24.33mm × 6.35mm
	DW (SOIC、20)	12.8mm × 7.5mm
	NS (SOP、20)	12.6mm × 5.3mm
	DB (SSOP、20)	7.2mm × 5.3mm
	PW (TSSOP、20)	6.5mm × 4.4mm

(1) パッケージ図、標準梱包数量、熱データ、記号、PCB 設計ガイドラインは、www.tij.co.jp/sc/package で入手できます。



論理図 (正論理)

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Table of Contents

1 特長 ... 1
2 アプリケーション ... 1
3 概要 ... 1
4 Revision History ... 2
5 Pin Configuration and Functions ... 3
6 Specifications ... 4
6.1 Absolute Maximum Ratings ... 4
6.2 ESD Ratings ... 4
6.3 Recommended Operating Conditions ... 4
6.4 Thermal Information ... 5
6.5 Electrical Characteristics ... 5
6.6 Switching Characteristics, V_{CC} = 3.3 V ± 0.3 V ... 6
6.7 Switching Characteristics, V_{CC} = 5 V ± 0.5 V ... 6
6.8 Operating Characteristics ... 6
7 Parameter Measurement Information ... 7
8 Detailed Description ... 8
8.1 Overview ... 8
8.2 Functional Block Diagram ... 8
8.3 Device Functional Modes ... 8
9 Application and Implementation ... 9
9.1 Power Supply Recommendations ... 9
9.2 Layout ... 9
10 Detailed Description ... 10
10.1 Device and Documentation Support ... 10
10.2 ドキュメントの更新通知を受け取る方法 ... 10
10.3 サポート・リソース ... 10
10.4 Trademarks ... 10
10.5 静電気放電に関する注意事項 ... 10
10.6 用語集 ... 10
11 Mechanical, Packaging, and Orderable Information ... 10

4 Revision History

Changes from Revision E (October 2003) to Revision F (April 2023)	Page
• 「アプリケーション」、「パッケージ情報」表、「ピンの機能」表、「ESD 定格」表、「熱に関する情報」表、「デバイスの機能モード」、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、および「メカニカル、パッケージ、および注文情報」セクションを追加	1

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5 Pin Configuration and Functions

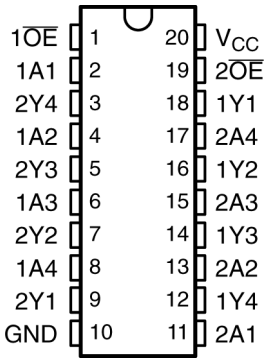


図 5-1. SN54AC240 J or W Package; SN74AC240 DB, DW, N, NS, or PW Package (Top View)

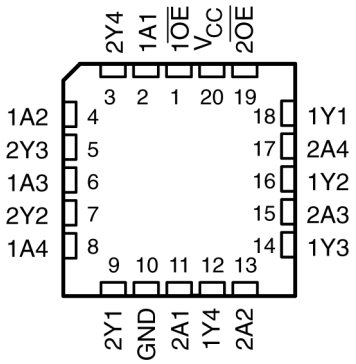


図 5-2. SN54AC240 FK Package (Top View)

表 5-1. Pin Functions

NAME[1]	PIN	TYPE	DESCRIPTION
1OE	1	I	Output enable 1
1A1	2	I	1A1 input
2Y4	3	O	2Y4 output
1A2	4	I	1A2 input
2Y3	5	O	2Y3 output
1A3	6	I	1A3 input
2Y2	7	O	2Y2 output
1A4	8	I	1A4 input
2Y1	9	O	2Y1 output
GND	10	—	Ground pin
2A1	11	I	2A1 input
1Y4	12	O	1Y4 output
2A2	13	I	2A2 input
1Y3	14	O	1Y3 output
2A3	15	I	2A3 input
1Y2	16	O	1Y2 output
2A4	17	I	2A4 input
1Y1	18	O	1Y1 output
2OE	19	I	Output enable 2
VCC	20	—	Power pin

(1) Signal Types: I = Input, O = Output, I/O = Input or Output

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	–0.5	7	V
V_I [2]	Input voltage range	-0.5	V_{CC}+0.5	V
V_O [2]	Output voltage range	-0.5	V_{CC}+0.5	V
I_{IK} (V_I < 0 or V_I > V_{CC})	Input clamp current		±20	mA
I_{OK} (V_O < 0 or V_O > V_{CC})	Output clamp current		±20	mA
I_O (V_O = 0 or V_{CC})	Continuous output current		±50	mA
	Continuous current through V_{CC} or GND		±200	mA
T_{stg}	Storage temperature range	-65	150	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	
		Machine model (A115-A)	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

(see Note[1])

			SN54AC240		SN74AC240		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	6	2	6	V
V_{IH}	High-level input voltage	V_{cc} = 3 V	2.1		2.1		V
		V_{cc} = 4.5 V	1.15		1.15		
		V_{cc} = 5.5 V	1.85		1.85		
V_{IL}	Low-level input voltage	V_{cc} = 3 V		0.9		0.9	V
		V_{cc} = 4.5 V		1.35		1.35	
		V_{cc} = 5.5 V		1.65		1.65	
V_I	Input voltage		0	V_{cc}	0	V_{cc}	V
V_O	Output voltage		0	V_{cc}	0	V_{cc}	V
I_{OH}	High-level output current	V_{cc} = 3 V		-12		-12	mA
		V_{cc} = 4.5 V		-24		-24	
		V_{cc} = 5.5 V		-24		-24	
I_{OL}	Low-level output current	V_{cc} = 3 V		12		12	mA
		V_{cc} = 4.5 V		24		24	
		V_{cc} = 5.5 V		24		24	
Δt/Δv	Input transition rise or fall rate			8		8	ns/V

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(see Note[1])

		SN54AC240		SN74AC240		UNIT
		MIN	MAX	MIN	MAX	
T_a	Operating free-air temperature	-55	125	-40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

6.4 Thermal Information

THERMAL METRIC[1]		DB	DW	N	NS	PW	UNIT
		20 PINS	20 PINS	20 PINS	20 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance[2]	70	58	69	60	83	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54AC240		SN74AC240		UNIT
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		I_{oh} = -50 µA		3 V	2.9			2.9		2.9		V
				4.5 V	4.4			4.4		4.4		
				5.5 V	5.4			5.4		5.4		
		I_{oh} = -12 mA		3 V	2.56			2.4		2.46		
		I_{oh} = -24 mA		4.5 V	3.86			3.7		3.76		
				5.5 V	4.86			4.7		4.76		
		I_{oh} = -50 mA[(1)]		5.5 V				3.85				
		I_{oh} = -75 mA[(1)]		5.5 V						3.85		
V_{OL}		I_{ol} = 50 µA		3 V			0.1		0.1		0.1	V
				4.5 V			0.1		0.1		0.1	
				5.5 V			0.1		0.1		0.1	
		I_{ol} = 12 mA		3 V			0.36		0.5		0.44	
		I_{ol} = 24 mA		4.5 V			0.36		0.5		0.44	
				5.5 V			0.36		0.5		0.44	
		I_{ol} = 50 mA[(1)]		5.5 V					1.65			
		I_{ol} = 75 mA[(1)]		5.5 V							1.65	
I_I	Data inputs	$V_I = V_{CC}$ or GND		5.5 V			±0.1		±1		±1	µA
	Control inputs	$V_I = V_{CC}$ or GND					±0.1		±1		±1	
I_{OZ}[(2)]		$V_O = V_{cc}$ or GND, V_I(OE) = V_{IL} or V_{IH}		5.5 V			±0.25		±5		±2.5	µA
I_{CC}		$V_I = V_{CC}$ or GND,	I_O = 0	5.5 V			4		80		40	µA
C_i		$V_I = V_{CC}$ or GND		5 V		2.5						pF

(1) Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
(2) For I/O ports, the parameter I_{OZ} includes the input leakage current.

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6.6 Switching Characteristics, V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see 図 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			SN54AC240		SN74AC240		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1.5	6	8	1	11	1	9	ns
t_{PHL}			1.5	5.5	8	1	10.5	1	8.5	
t_{PZH}	$\overline{OE}$	Y	1.5	6	10.5	1	11.5	1	11	ns
t_{PZL}			1.5	7	10	1	13	1	11	
t_{PHZ}	$\overline{OE}$	Y	1.5	7	10	1	12.5	1	10.5	ns
t_{PLZ}			1.5	7.5	10.5	1	13.5	1	11.5	

6.7 Switching Characteristics, V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see 図 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			SN54AC240		SN74AC240		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1.5	4.5	6.5	1	8.5	1	7	ns
t_{PHL}			1.5	4.5	6	1	8	1	6.5	
t_{PZH}	$\overline{OE}$	Y	1.5	5	7	1	9	1	8	ns
t_{PZL}			1.5	5.5	8	1	10.5	1	8.5	
t_{PHZ}	$\overline{OE}$	Y	2.5	6.5	9	1	10.5	1	9.5	ns
t_{PLZ}			2	6.5	9	1	11	1	9.5	

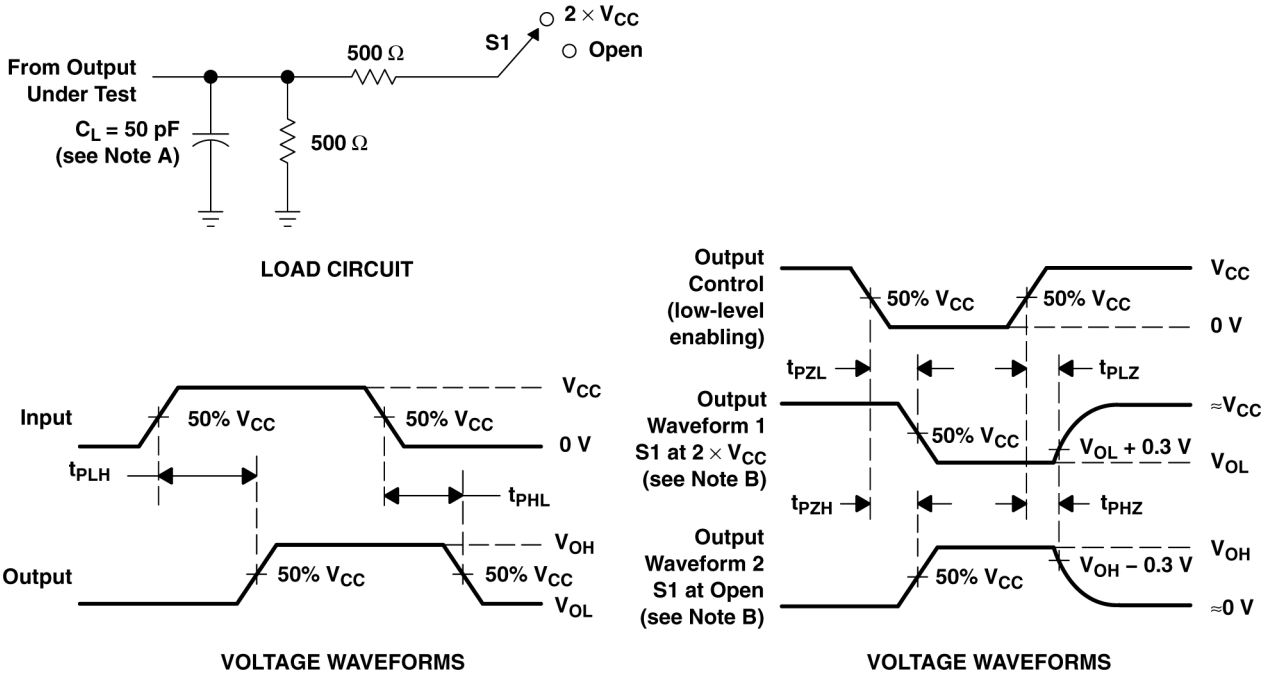
6.8 Operating Characteristics

V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance per buffer/driver	C_l = 50 pF,	f = 1 MHz	45	pF

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7 Parameter Measurement Information



A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one input transition per measurement.

図 7-1. Load Circuit and Voltage Waveforms

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	Open

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8 Detailed Description

8.1 Overview

The 'AC240 devices are organized as two 4-bit buffers/drivers with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the device passes inverted data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

To ensure the high-impedance state during power

up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

8.2 Functional Block Diagram

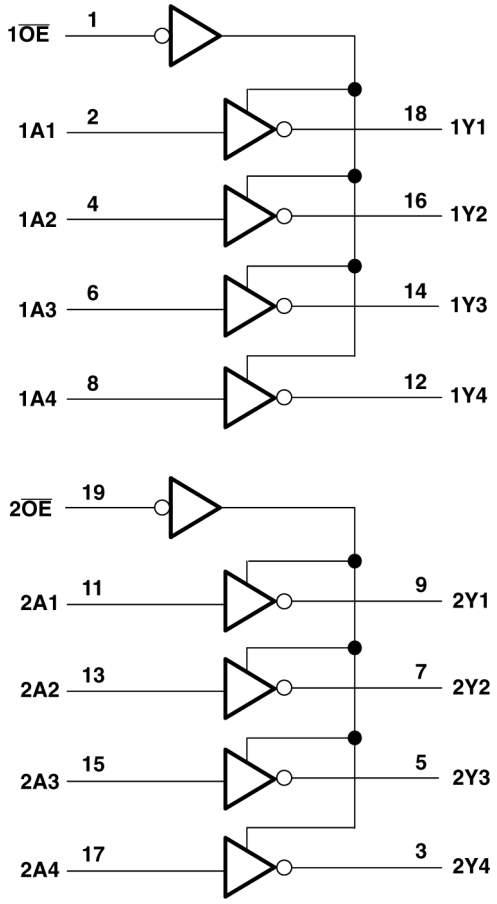


図 8-1. Logic Diagram (Positive Logic)

8.3 Device Functional Modes

表 8-1. Function Table (Each Buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	L
L	L	H
H	X	Z

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9 Application and Implementation

注

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9.1 Power Supply Recommendations

The power supply can be any voltage between the min and max supply voltage rating located in *セクション 6.3*.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends 0.1 µF and if there are multiple V_{CC} terminals, then TI recommends .01 µF or .022 µF for each power terminal. It is okay to parallel multiple bypass capacitors to reject different frequencies of noise. A 0.1 µF and 1 µF are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

9.2 Layout

9.2.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} whichever make more sense or is more convenient. It is generally okay to float outputs unless the part is a transceiver. If the transceiver has an output enable pin it will disable the outputs section of the part when asserted. This does not disable the input section of the IOs so they cannot float when disabled.

9.2.1.1 Layout Example

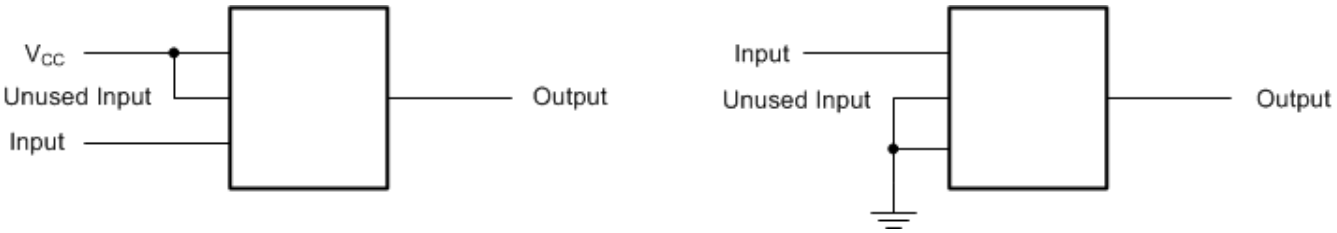


図 9-1. Layout Recommendation

10 Detailed Description

10.1 Device and Documentation Support

10.1.1 Documentation Support

10.1.1.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 10-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54AC240	Click here	Click here	Click here	Click here	Click here
SN74AC240	Click here	Click here	Click here	Click here	Click here

10.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

10.3 サポート・リソース

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10.4 Trademarks

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10.5 静電気放電に関する注意事項



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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

10.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-87550012A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-87550012A SNJ54AC 240FK	Samples
5962-8755001RA	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8755001RA SNJ54AC240J	Samples
5962-8755001SA	ACTIVE	CFP	W	20	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8755001SA SNJ54AC240W	Samples
SN74AC240DBR	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC240	Samples
SN74AC240DWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC240	Samples
SN74AC240N	ACTIVE	PDIP	N	20	20	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74AC240N	Samples
SN74AC240NSR	ACTIVE	SO	NS	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC240	Samples
SN74AC240PWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC240	Samples
SN74AC240PWRE4	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC240	Samples
SNJ54AC240FK	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-87550012A SNJ54AC 240FK	Samples
SNJ54AC240J	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8755001RA SNJ54AC240J	Samples
SNJ54AC240W	ACTIVE	CFP	W	20	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8755001SA SNJ54AC240W	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54AC240, SN74AC240 :

- Catalog : SN74AC240
- Automotive : SN74AC240-Q1, SN74AC240-Q1
- Military : SN54AC240

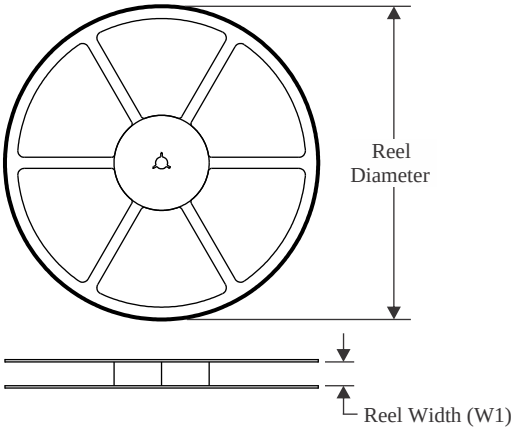
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

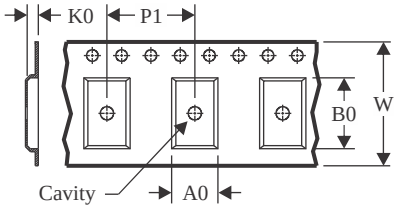
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

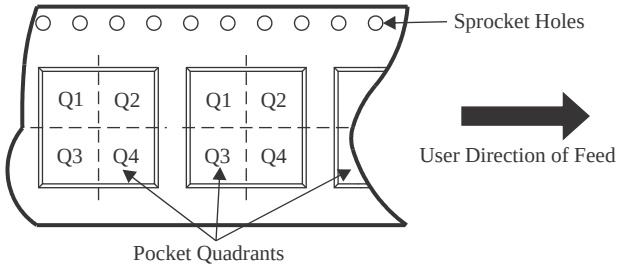


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

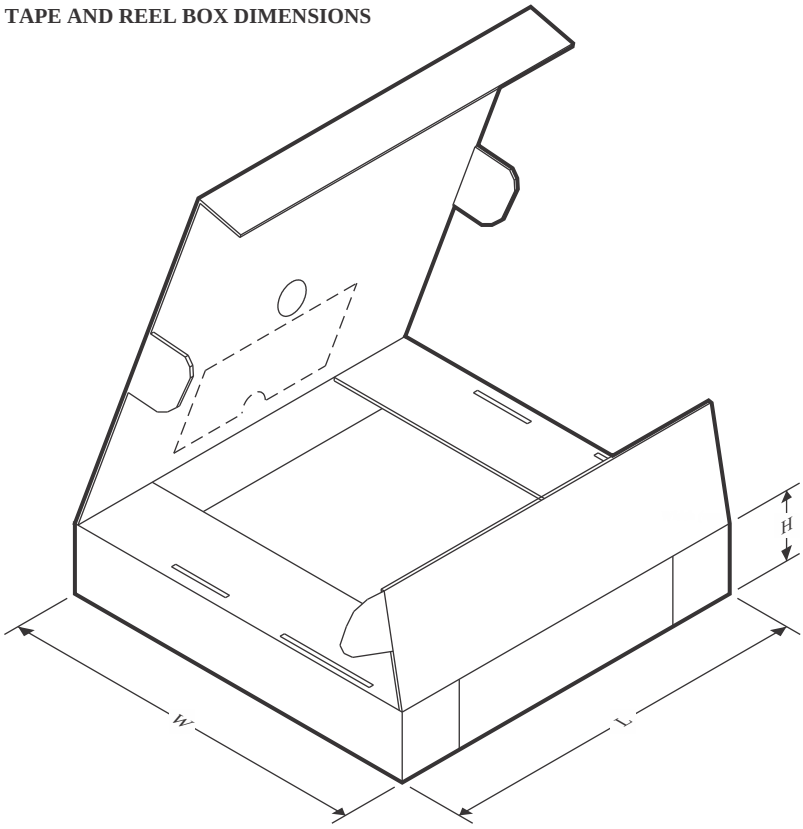
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AC240DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74AC240DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74AC240NSR	SO	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74AC240PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

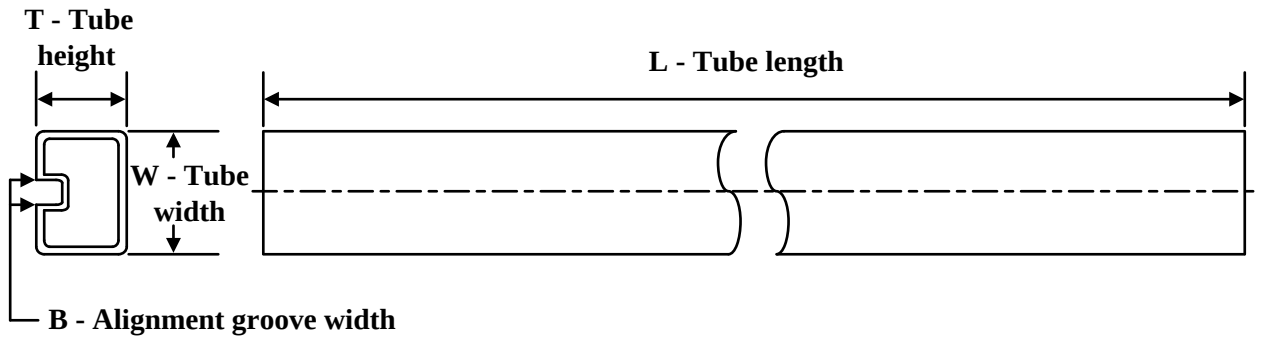
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AC240DBR	SSOP	DB	20	2000	356.0	356.0	35.0
SN74AC240DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74AC240NSR	SO	NS	20	2000	367.0	367.0	45.0
SN74AC240PWR	TSSOP	PW	20	2000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

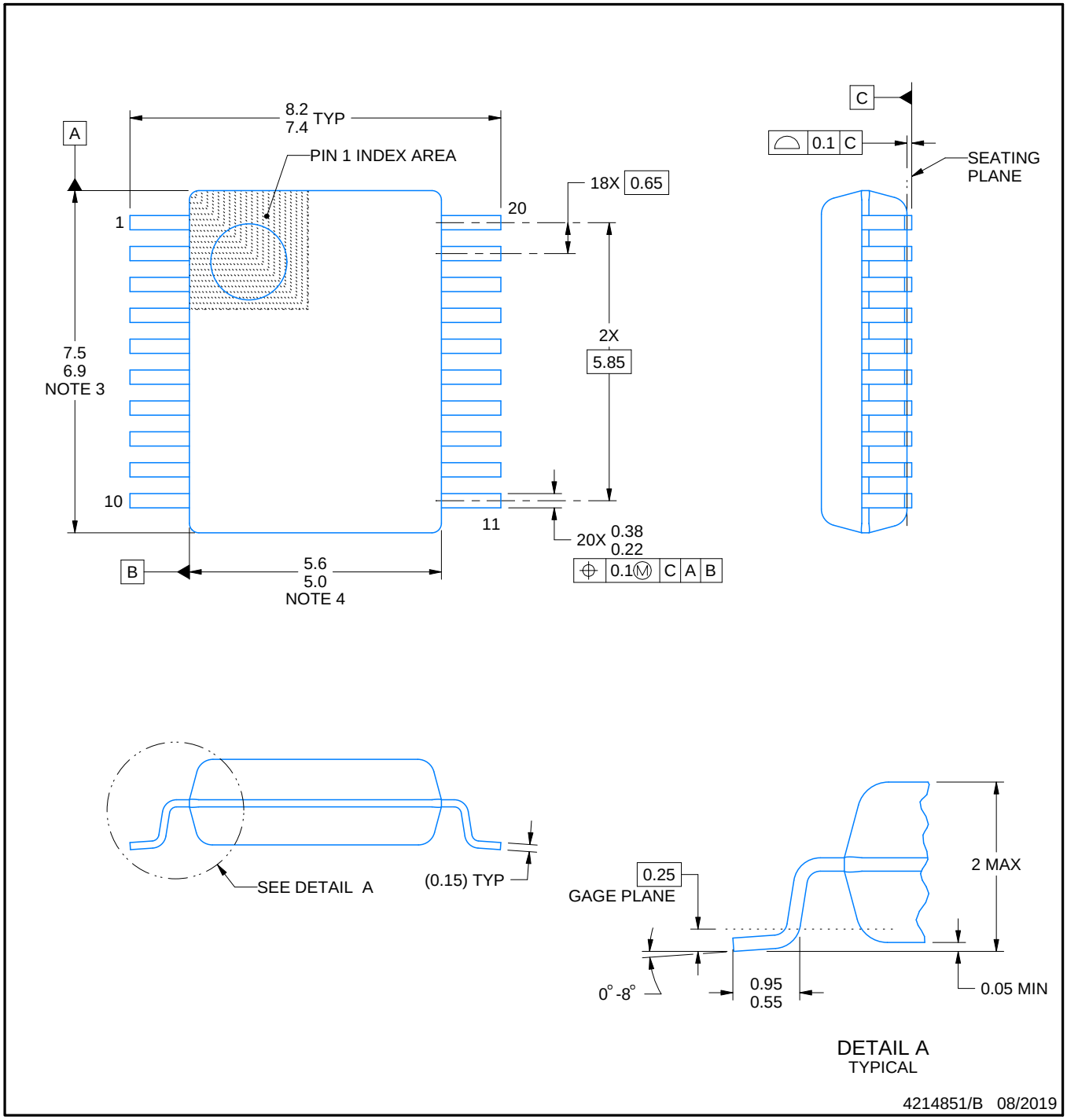
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-87550012A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-8755001SA	W	CFP	20	25	506.98	26.16	6220	NA
SN74AC240N	N	PDIP	20	20	506	13.97	11230	4.32
SNJ54AC240FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54AC240W	W	CFP	20	25	506.98	26.16	6220	NA

PACKAGE OUTLINE

DB0020A

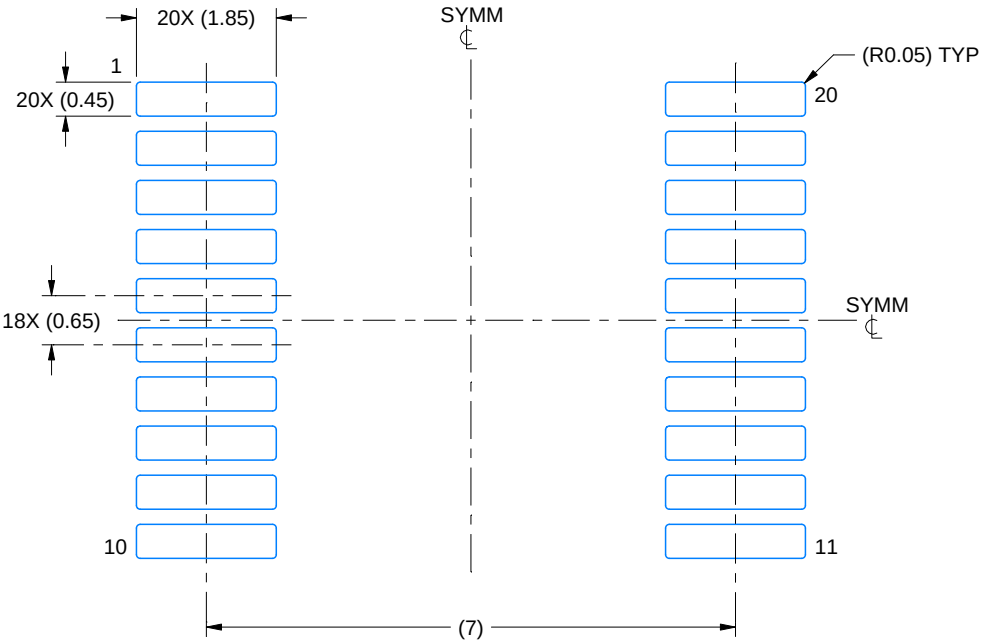
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

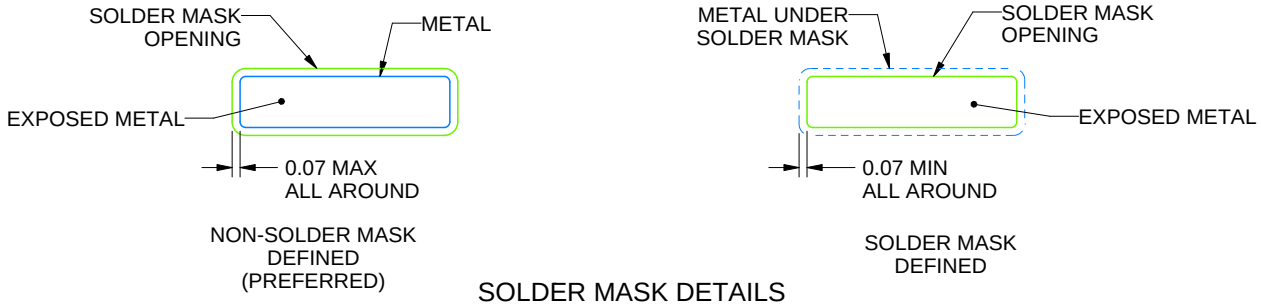


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

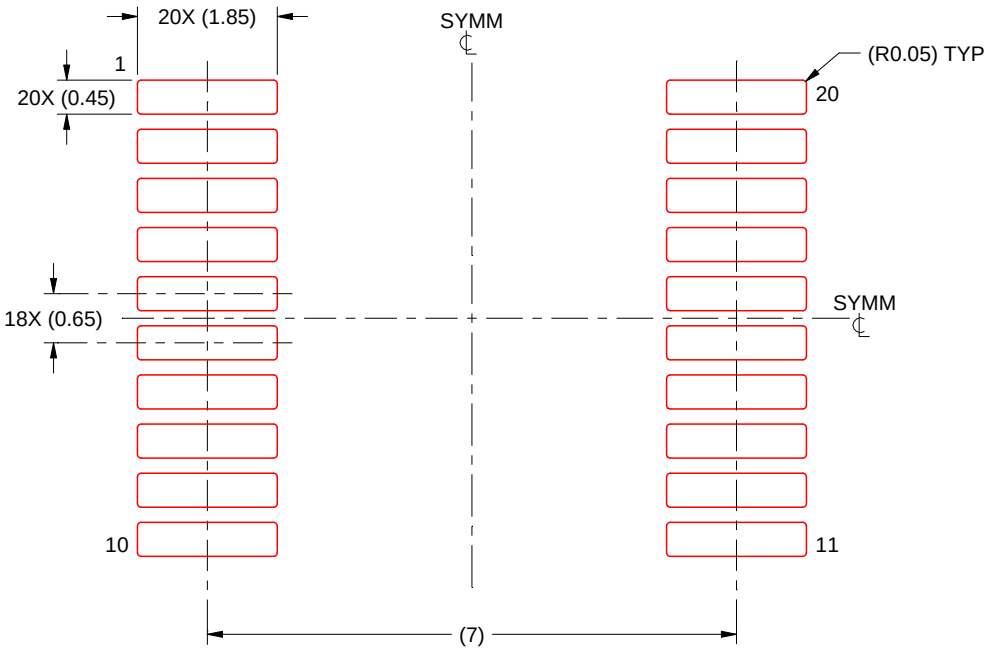
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

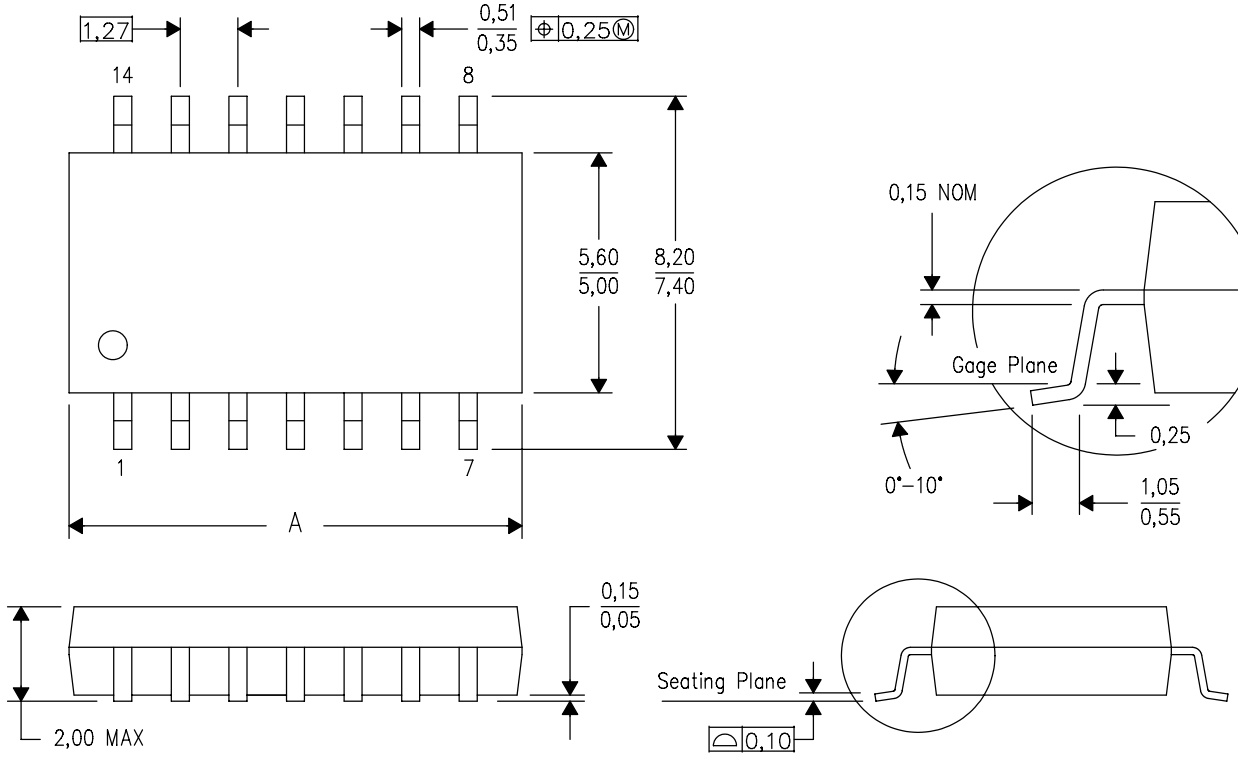
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

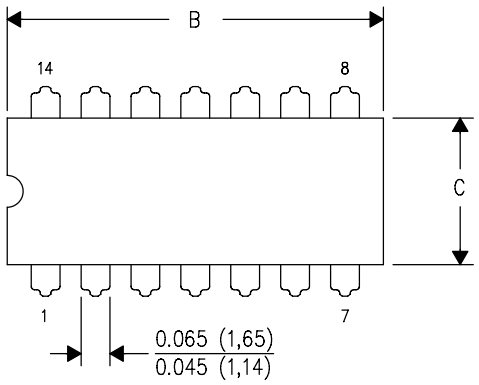
4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

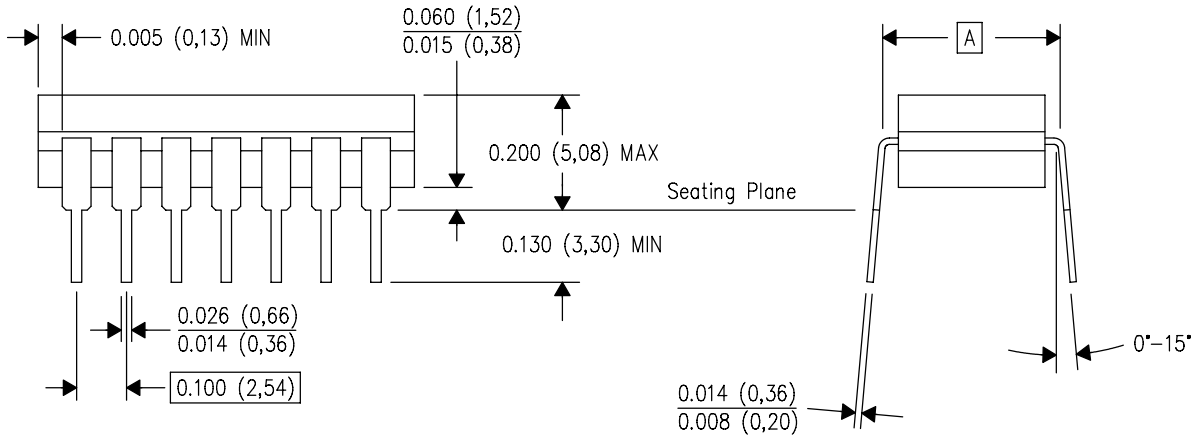
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

GENERIC PACKAGE VIEW

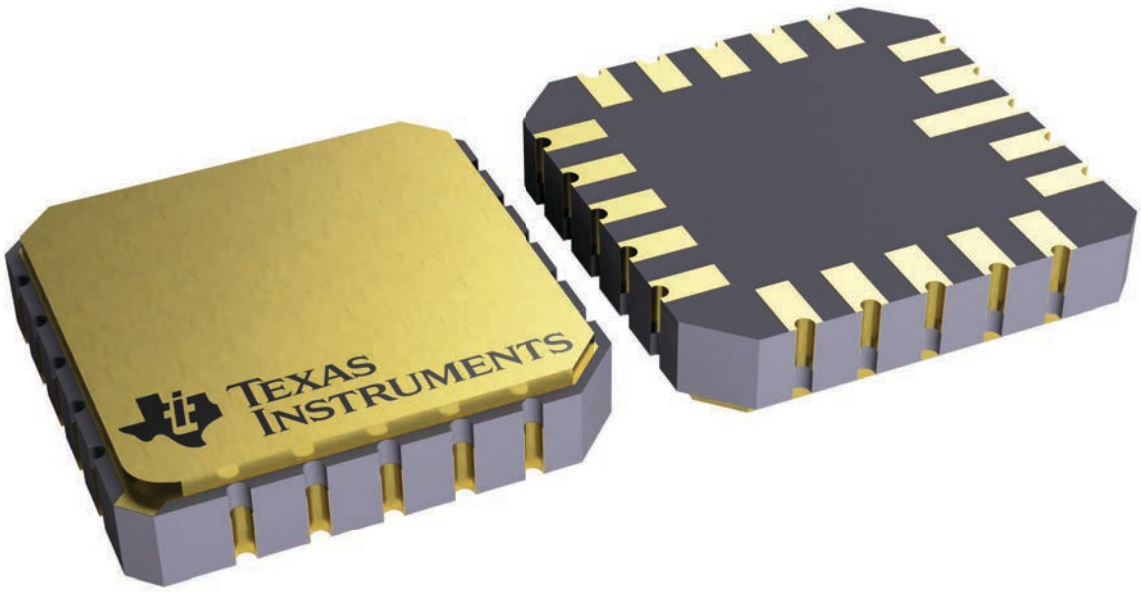
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

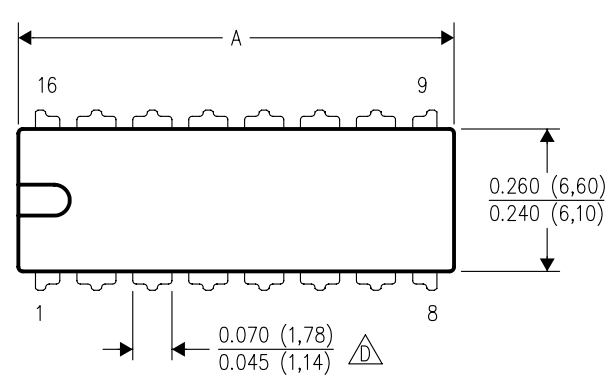


4229370VA\

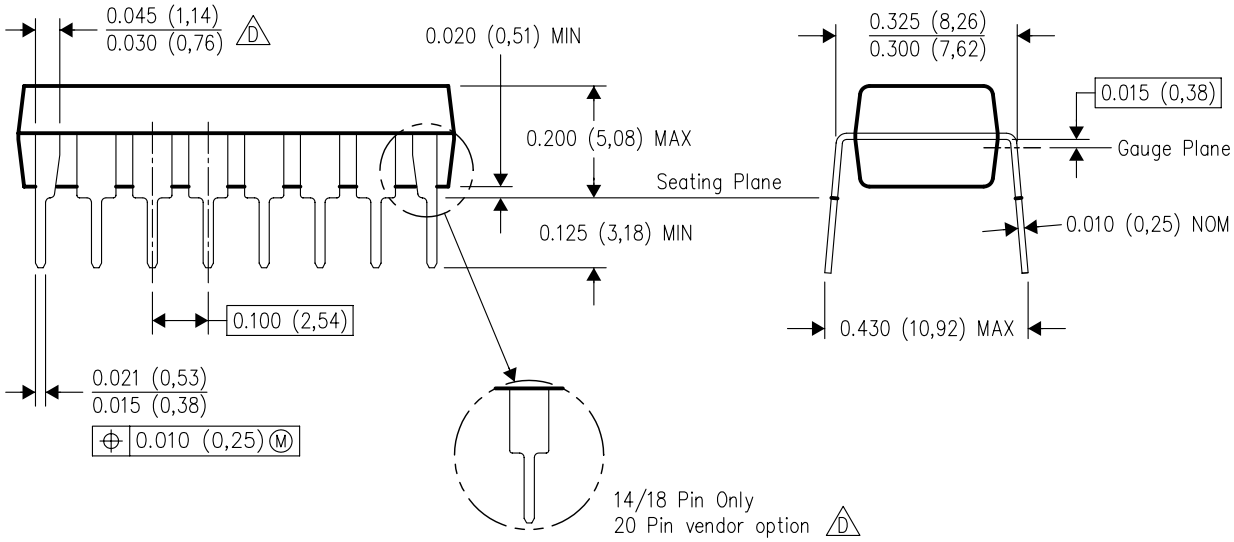
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

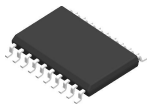


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

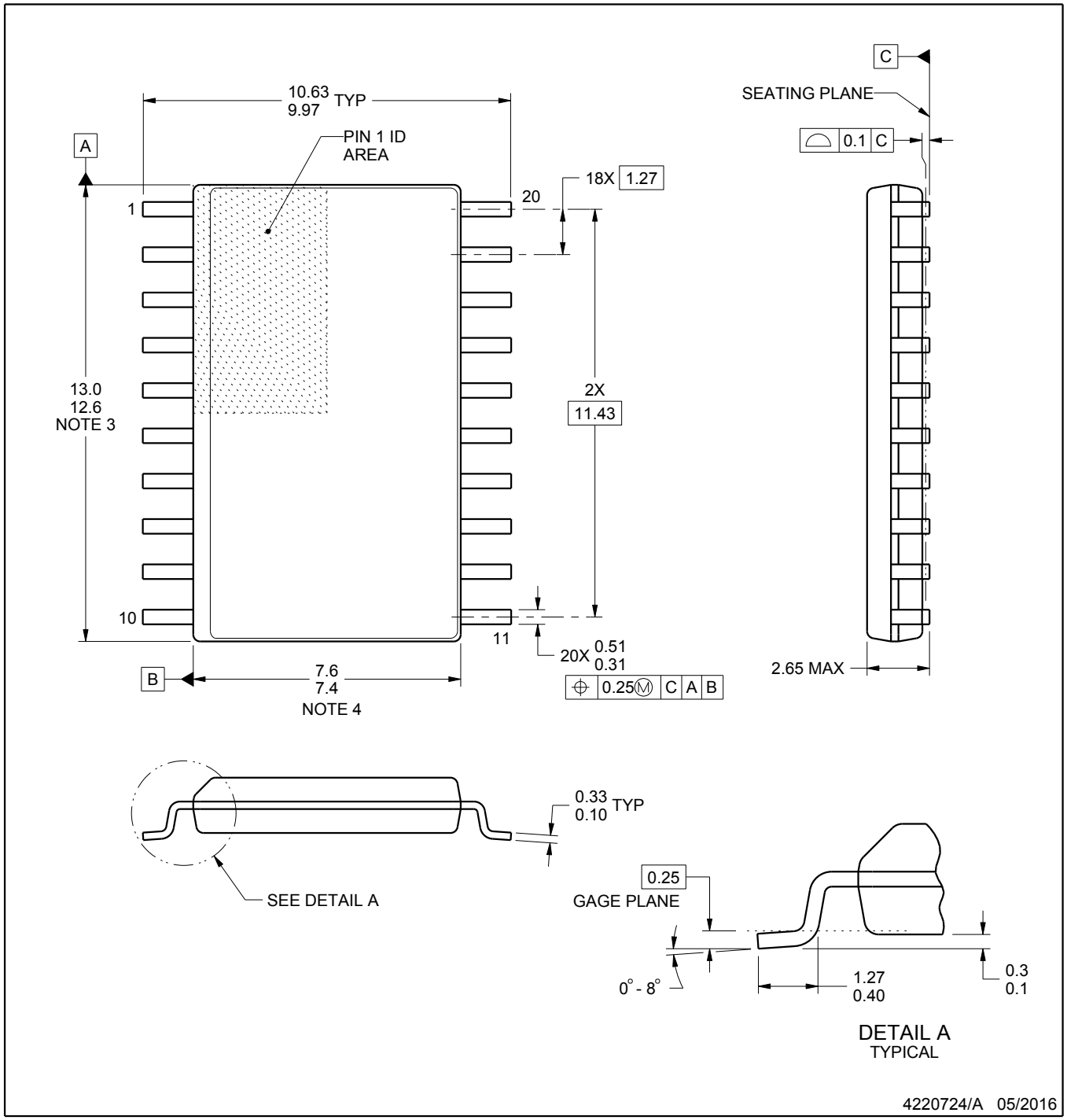


PACKAGE OUTLINE

DW0020A

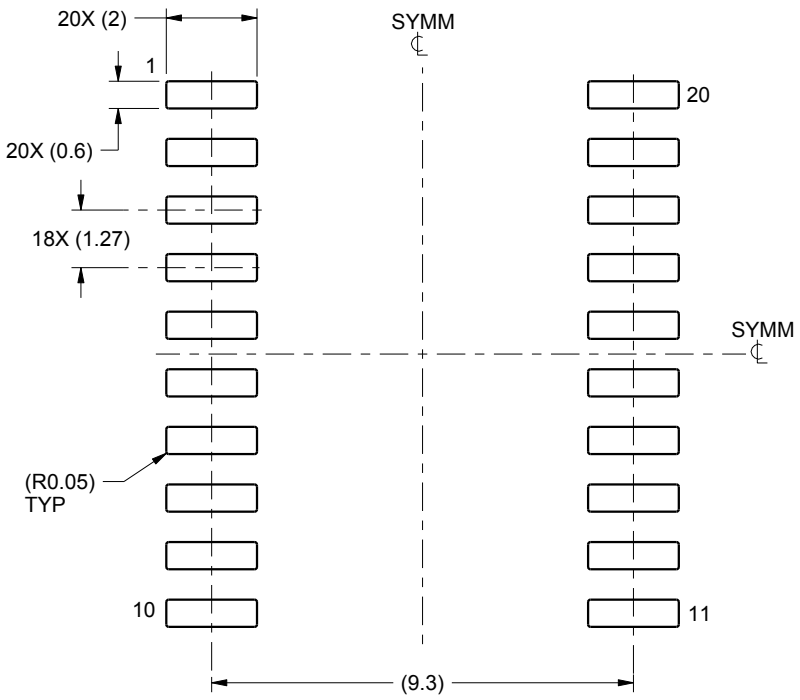
SOIC - 2.65 mm max height

SOIC

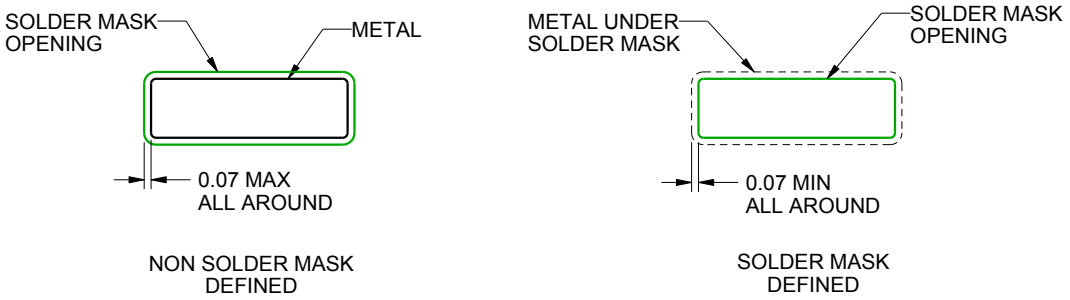


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

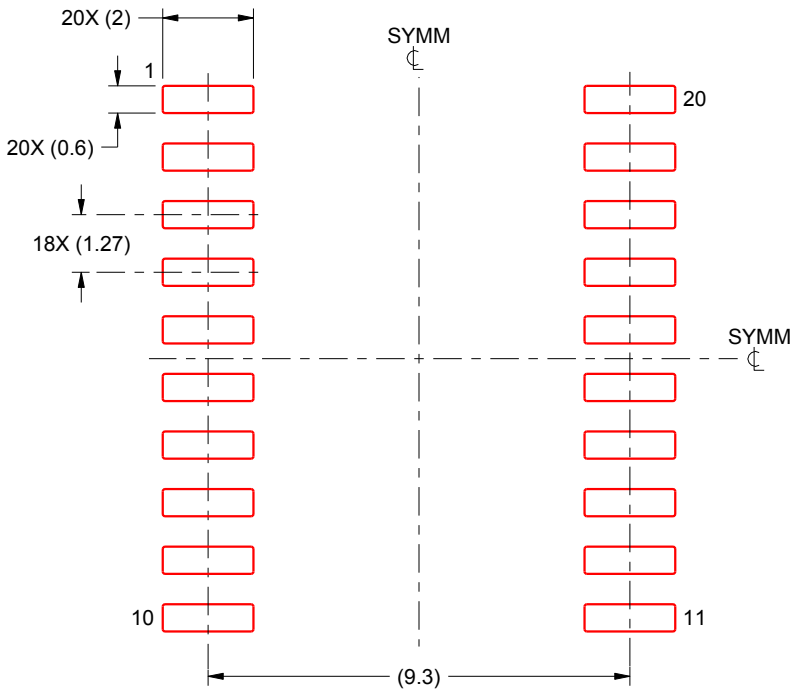


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



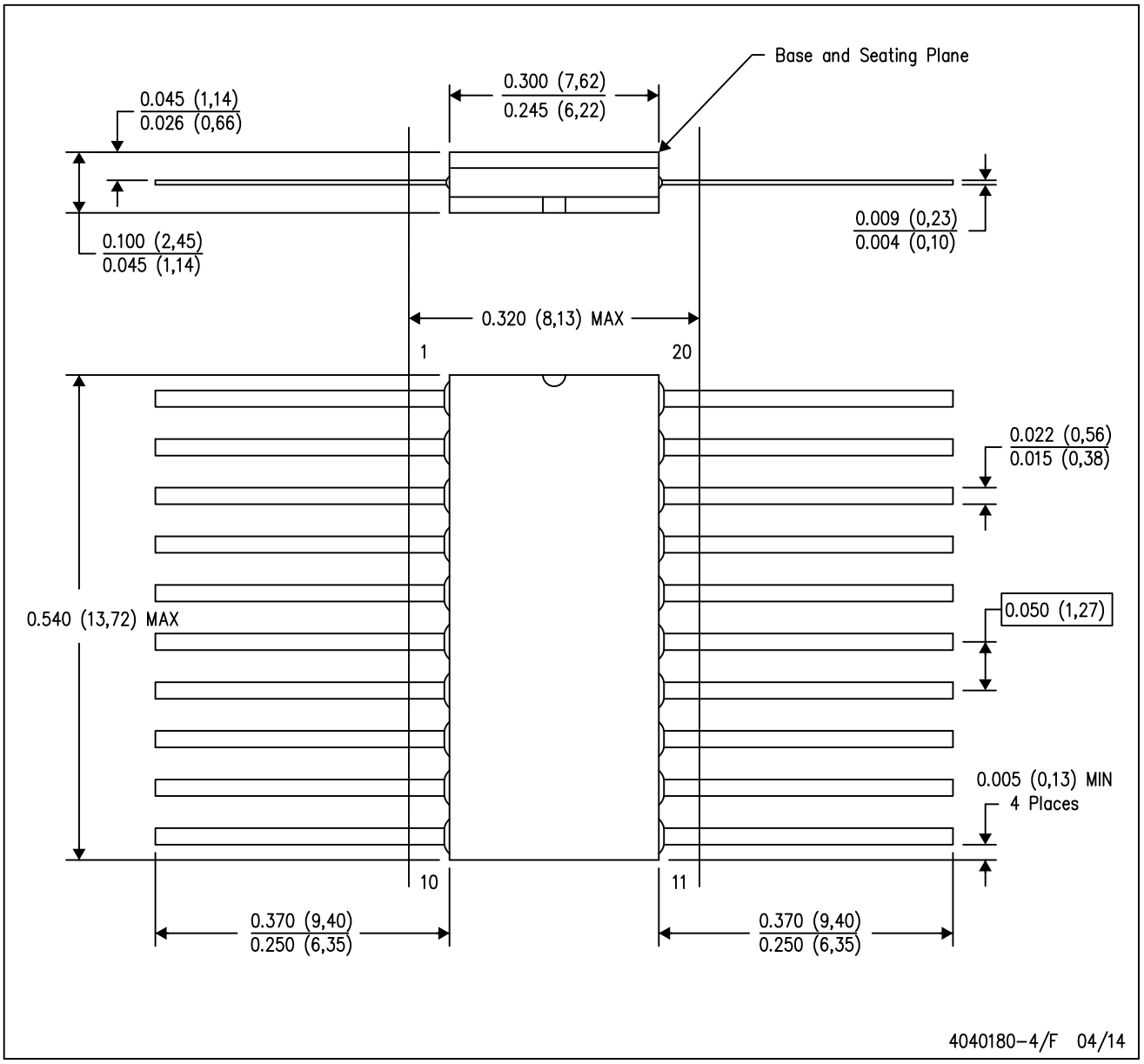
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

W (R–GDFP–F20) CERAMIC DUAL FLATPACK



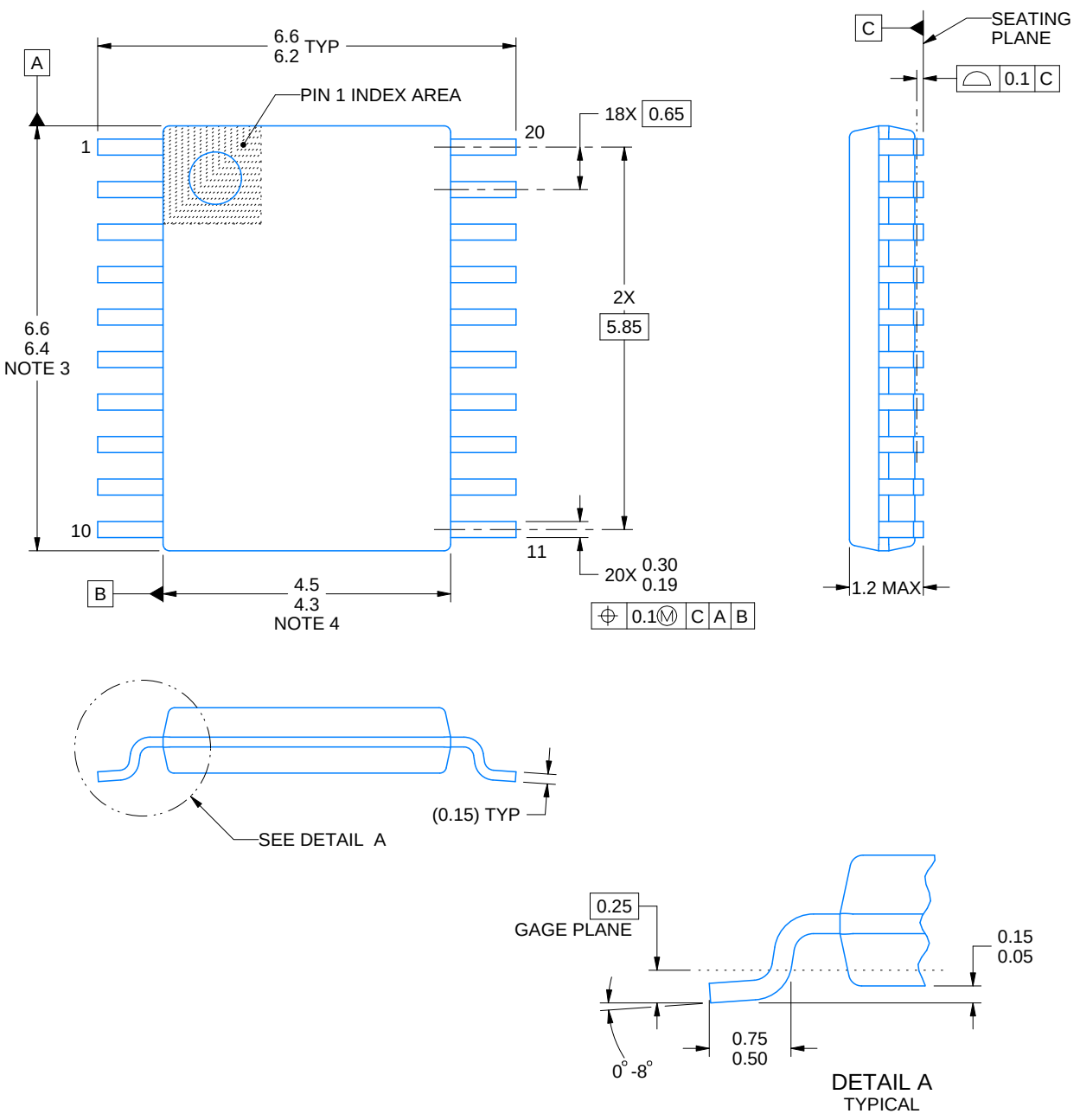
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within Mil–Std 1835 GDFP2–F20

PACKAGE OUTLINE

PW0020A

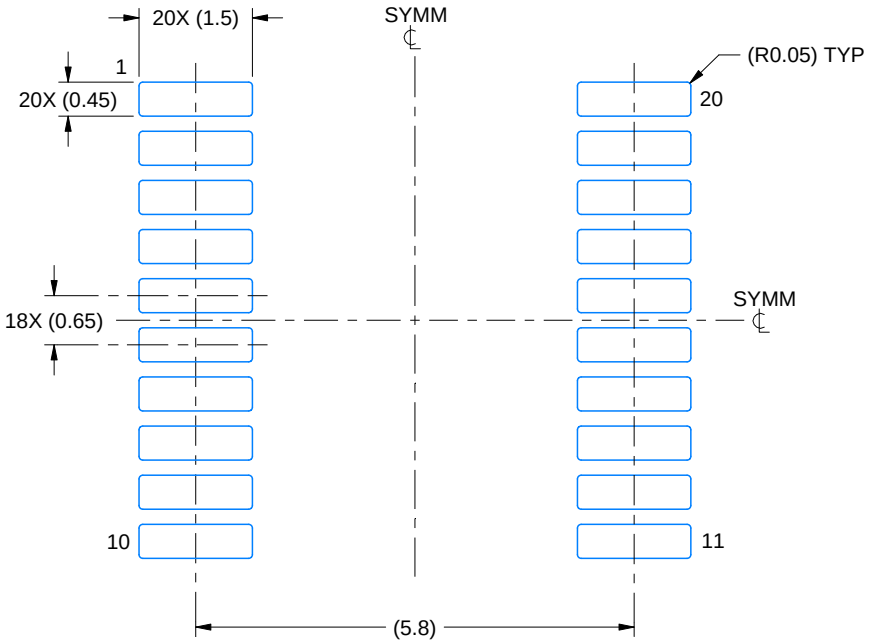
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

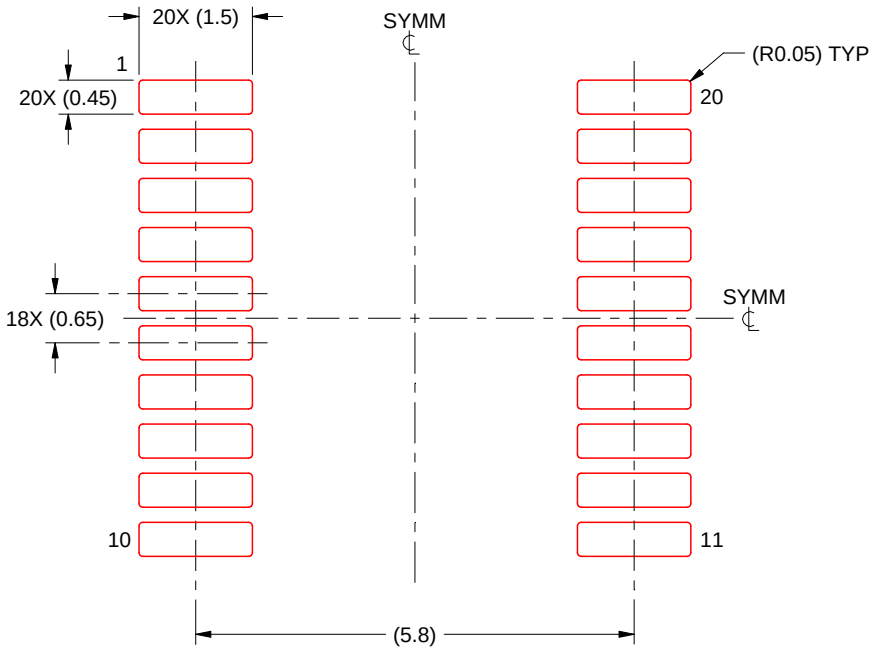


SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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