参考資料

CSD86360Q5D 同期整流降圧型NexFET™パワー・ブロック

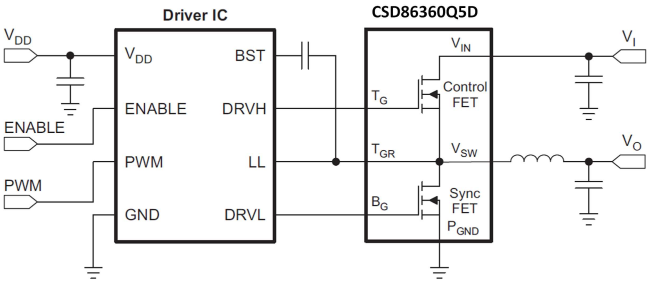
1 特長

- ハーフ・ブリッジ・パワー・ブロック
- 25A時に91%のシステム効率
- 最大50Aで動作
- 高周波数での動作(最高1.5MHz)
- 高密度SON、占有面積5mm×6mm
- 5Vゲートの駆動に最適化
- 低いスイッチング損失
- インダクタンスの非常に低いパッケージ
- RoHS準拠
- ハロゲン不使用
- 鉛フリーの端子メッキ処理

2 アプリケーション

- 同期整流降圧コンバータ
  - 高周波数のアプリケーション
  - 大電流、低デューティ・サイクルのアプリケーション
- マルチフェーズの同期整流降圧コンバータ
- POL DC/DCコンバータ
- IMVP、VRM、VRDアプリケーション

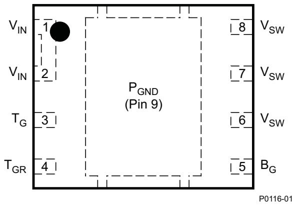
回路例



3 概要

CSD86360Q5D NexFET™パワー・ブロックは、同期整流降圧アプリケーション向けに最適化された設計で、大電流、高効率、高周波数の能力を小さな5mm×6mmの外形に収めています。この製品は5Vのゲート駆動アプリケーション用に最適化された柔軟なソリューションであり、外部のコントローラ/ドライバからの任意の5Vゲート・ドライブと組み合わせて、高密度の電源を実現できます。

図 1. 上面図

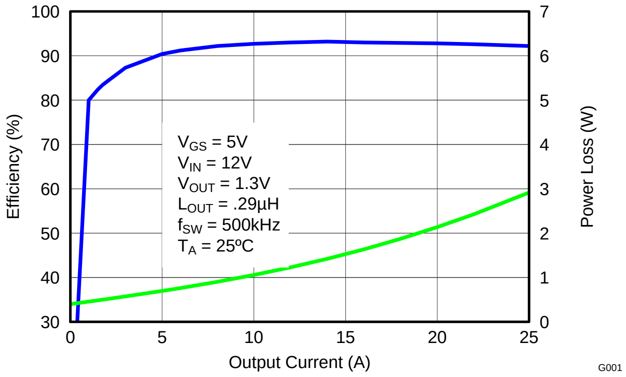


製品情報(1)

デバイス	メディア	数量	パッケージ	出荷
CSD86360Q5D	13インチ・リール	2500	SON 5.00mm×6.00mm プラスチック・パッケージ	テープ・アンド・リール

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

標準的なパワー・ブロックの効率と電力損失との関係



English Data Sheet: SLPS327

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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision A (May 2013) から Revision B に変更 **Page**

- Changed Recommended PCB Design Overview section to *Layout* section 16
- 追加 「*デバイスおよびドキュメントのサポート*」セクション 18
- 変更 「*メカニカル・データ*」セクションを「*メカニカル、パッケージ、および注文情報*」セクションに 19
- 「*Q5Dパッケージの寸法*」セクションを更新 19
- 「*推奨ランド・パターン*」の図を更新 20
- 「*推奨ステンシル*」の図を更新 21

2012年9月発行のものから更新 **Page**

- Changed the footnote notations in the THERMAL INFORMATION table 3
- Updated Figure 7 6
- Updated Figure 8 6
- Updated Figure 9 6
- Updated Figure 10 6

5 Specifications

5.1 Absolute Maximum Ratings

T_A = 25°C (unless otherwise noted) (1)

PARAMETER	CONDITIONS	MIN	MAX	UNIT
Voltage	V_{IN} to P_{GND}		25	V
	V_{SW} to P_{GND}		25	
	V_{SW} to P_{GND} (10 ns)		27	
	T_G to T_{GR}	–8	10	
	B_G to P_{GND}	–8	10	
Pulsed current rating, I_{DM} (2)			120	A
Power dissipation, P_D (3)			13	W
Avalanche energy, E_{AS}	Sync FET, I_D = 110 A, L = 0.1 mH		605	mJ
	Control FET, I_D = 61 A, L = 0.1 mH		186	
Operating junction, T_J		–55	150	°C
Storage temperature, T_{STG}		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Pulse duration ≤ 50 μs. Duty cycle ≤ 0.01%.
(3) T_{PCB} ≤ 95°C.

5.2 Recommended Operating Conditions

T_A = 25°C (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	MAX	UNIT
V_{GS}	Gate drive voltage		4.5	8	V
V_{IN}	Input supply voltage			22	V
f_{SW}	Switching frequency	C_{BST} = 0.1 μF (min)	200	1500	kHz
	Operating current			50	A
T_J	Operating temperature			125	°C

5.3 Power Block Performance

T_A = 25°C (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
P_{LOSS}	Power loss (1)	V_{IN} = 12 V, V_{GS} = 5 V, V_{OUT} = 1.3 V, I_{OUT} = 25 A, f_{SW} = 500 kHz, L_{OUT} = 0.3 μH, T_J = 25°C		2.6		W
I_{QVIN}	V_{IN} quiescent current	T_G to T_{GR} = 0 V B_G to P_{GND} = 0 V		10		μA

(1) Measurement made with six 10-μF (TDK C3216X5R1C106KT or equivalent) ceramic capacitors placed across V_{IN} to P_{GND} pins and using a high current 5-V driver IC.

5.4 Thermal Information

T_A = 25°C (unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (min Cu) (1)			102	°C/W
	Junction-to-ambient thermal resistance (max Cu) (1) (2)			50	

(1) $R_{\theta JC}$ is determined with the device mounted on a 1-in^2 (6.45-cm^2), 2-oz (0.071-mm) thick Cu pad on a 1.5-in × 1.5-in (3.81-cm × 3.81-cm), 0.06-in (1.52-mm) thick FR4 board. $R_{\theta JC}$ is specified by design while $R_{\theta JA}$ is determined by the user's board design.
(2) Device mounted on FR4 material with 1-in^2 (6.45-cm^2) Cu.

Thermal Information (continued)

T_A = 25°C (unless otherwise stated)

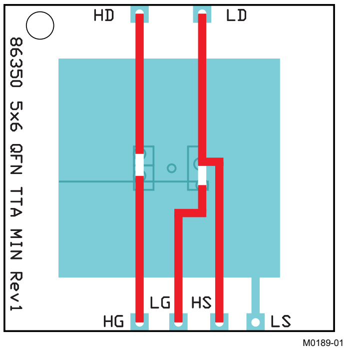
THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-case thermal resistance (top of package)(1)			20	°C/W
	Junction-to-case thermal resistance (P_{GND} pin)(1)			2	

5.5 Electrical Characteristics

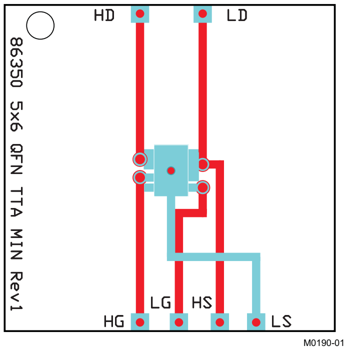
T_A = 25°C (unless otherwise stated)

PARAMETER		TEST CONDITIONS	Q1 Control FET			Q2 Sync FET			
			MIN	TYP	MAX	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS									
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0 V, I_{DS} = 250 μA	25			25			V
I_{DSS}	Drain-to-source leakage current	V_{GS} = 0 V, V_{DS} = 20 V			1			1	μA
I_{GSS}	Gate-to-source leakage current	V_{DS} = 0 V, V_{GS} = +10 / –8 V			100			100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_{DS} = 250 μA	1		2.1	0.75		1.15	V
$Z_{DS(on)}$	Drain-to-source on-impedance	V_{IN} = 12 V, V_{DD} = 5 V, V_{OUT} = 1.3 V I_{OUT} = 25 A, f_{SW} = 500 kHz, L_{OUT} = 0.3 μH		3.7			0.7		mΩ
g_{fs}	Transconductance	V_{DS} = 10 V, I_{DS} = 20 A		113			169		S
DYNAMIC CHARACTERISTICS									
C_{ISS}	Input capacitance(1)	V_{GS} = 0 V, V_{DS} = 12.5 V, f = 1 MHz		1590	2060		3910	5080	pF
C_{OSS}	Output capacitance(1)			840	1090		1970	2560	pF
C_{RSS}	Reverse transfer capacitance(1)			42	54		53	69	pF
R_G	Series gate resistance(1)			1.2	2.5		1.1	2.2	Ω
Q_g	Gate charge total (4.5 V)(1)	V_{DS} = 12.5 V, I_{DS} = 20 A		9.7	12.6		23	30	nC
Q_{gd}	Gate charge gate-to-drain			2.3			3.6		nC
Q_{gs}	Gate charge gate-to-source			3.5			6.0		nC
$Q_{g(th)}$	Gate charge at Vth			1.9			3.5		nC
Q_{OSS}	Output charge	V_{DS} = 12.5 V, V_{GS} = 0 V		15.1			33		nC
$t_{d(on)}$	Turnon delay time	V_{DS} = 12.5 V, V_{GS} = 4.5 V, I_{DS} = 20 A, R_G = 2 Ω		8.4			9.5		ns
t_r	Rise time			20.4			14.8		ns
$t_{d(off)}$	Turnoff delay time			14.5			29.3		ns
t_f	Fall time			4.3			6.6		ns
DIODE CHARACTERISTICS									
V_{SD}	Diode forward voltage	I_{DS} = 20 A, V_{GS} = 0 V		0.85	1		0.75	0.82	V
Q_{rr}	Reverse recovery charge	V_{dd} = 12 V, I_F = 20 A, di/dt = 300 A/μs		27			50		nC
t_{rr}	Reverse recovery time			22			34		ns

(1) Specified by design.



Max $R_{\theta JA}$ = 50°C/W when mounted on 1 in^2 ($6.45\ cm^2$) of 2-oz (0.071-mm) thick Cu.



Max $R_{\theta JA}$ = 102°C/W when mounted on minimum pad area of 2-oz (0.071-mm) thick Cu.

5.6 Typical Power Block Device Characteristics

T_J = 125°C, unless stated otherwise.

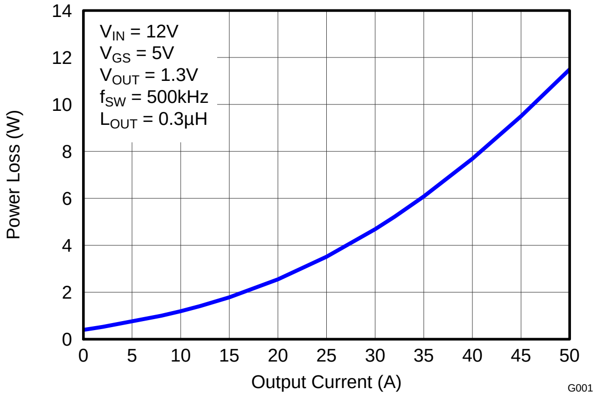


Figure 2. Power Loss vs Output Current

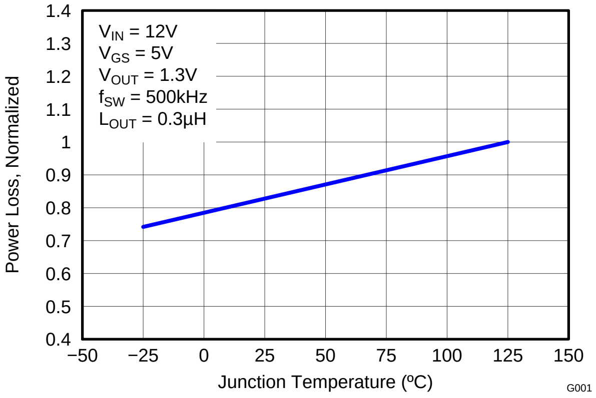


Figure 3. Normalized Power Loss vs Temperature

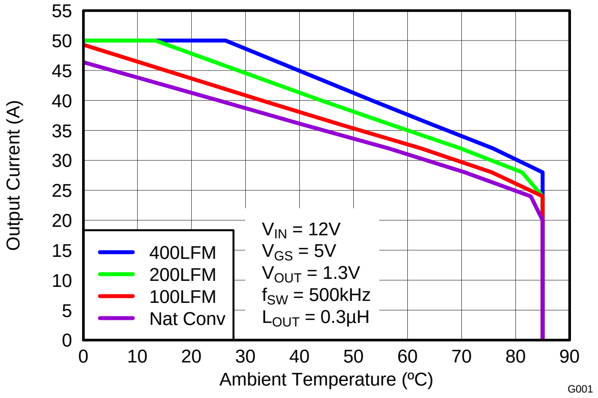


Figure 4. Safe Operating Area – PCB Vertical Mount (1)

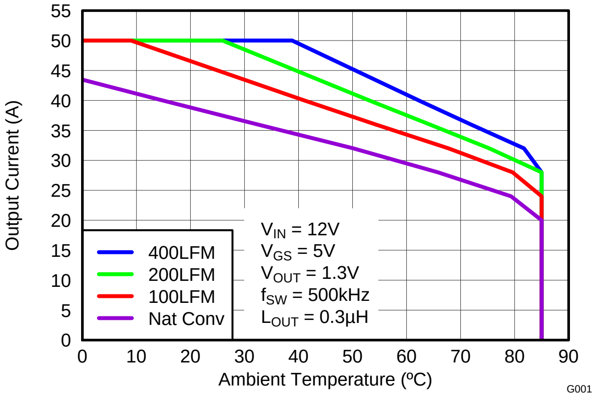


Figure 5. Safe Operating Area – PCB Horizontal Mount (1)

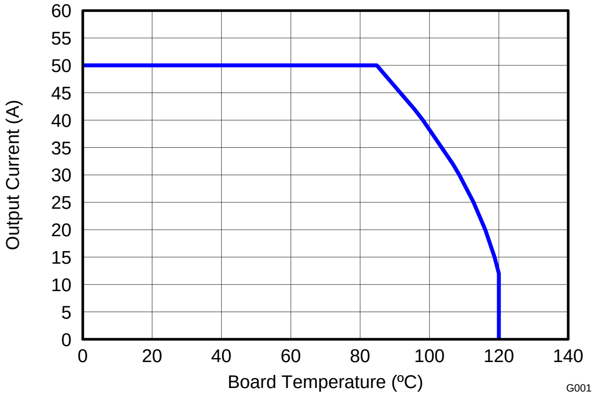


Figure 6. Typical Safe Operating Area(1)

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(1) The Typical Power Block System Characteristic curves are based on measurements made on a PCB design with dimensions of 4 in (W) × 3.5 in (L) × 0.062 in (H) and 6 copper layers of 1-oz copper thickness. See *Application and Implementation* section for detailed explanation.

Typical Power Block Device Characteristics (continued)

T_J = 125°C, unless stated otherwise.

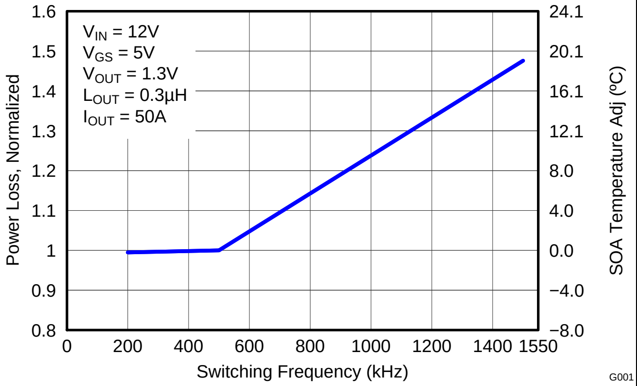

Figure 7. Normalized Power Loss vs Switching Frequency

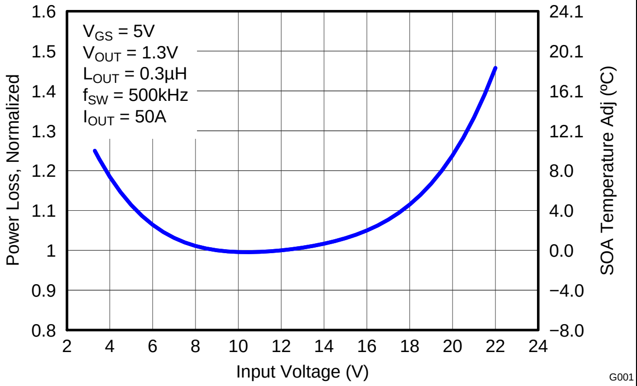

Figure 8. Normalized Power Loss vs Input Voltage

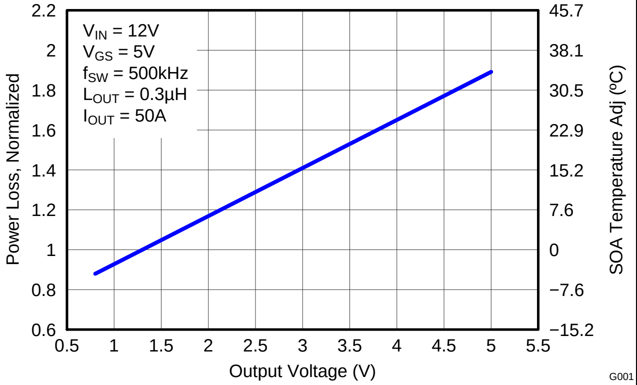

Figure 9. Normalized Power Loss vs Output Voltage

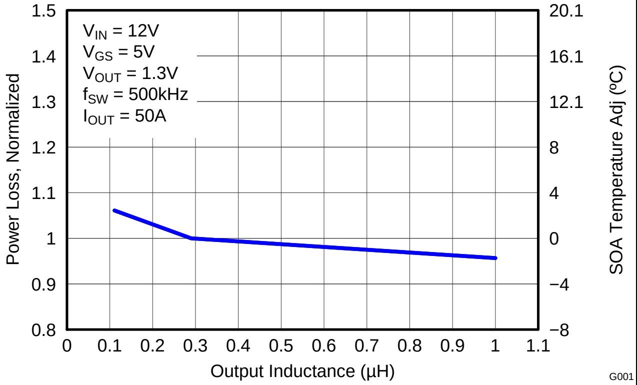

Figure 10. Normalized Power Loss vs Output Inductance

5.7 Typical Power Block MOSFET Characteristics

T_A = 25°C, unless stated otherwise.

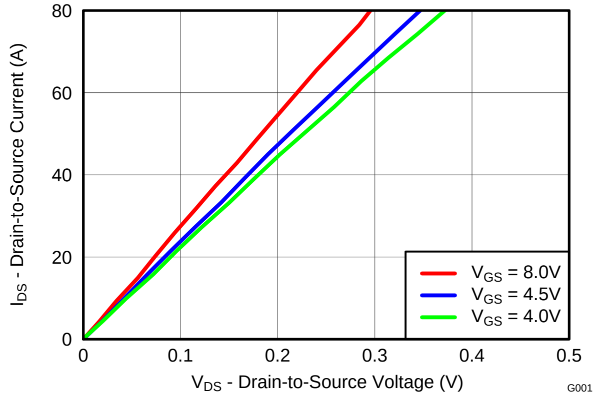

Figure 11. Control MOSFET Saturation

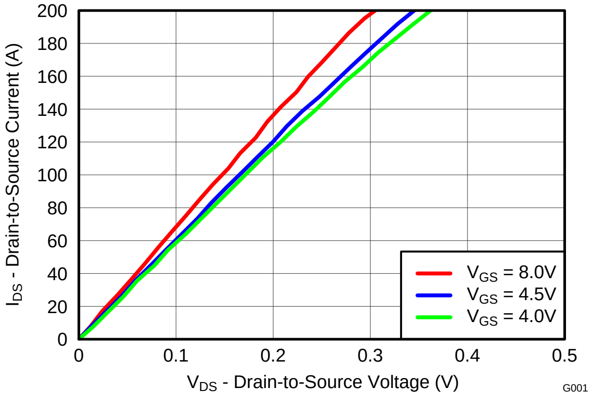

Figure 12. Sync MOSFET Saturation

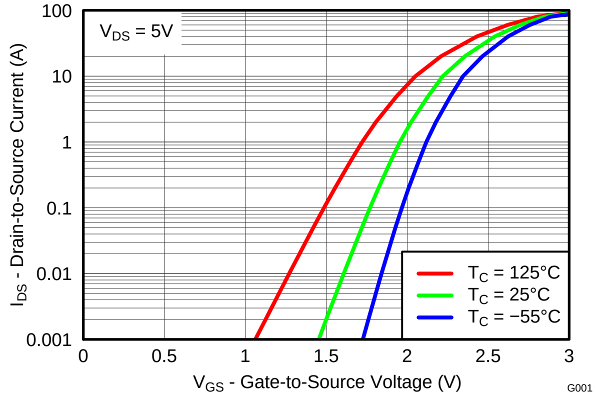

Figure 13. Control MOSFET Transfer

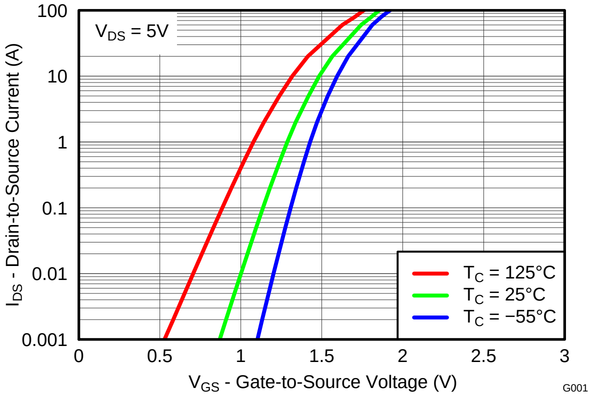

Figure 14. Sync MOSFET Transfer

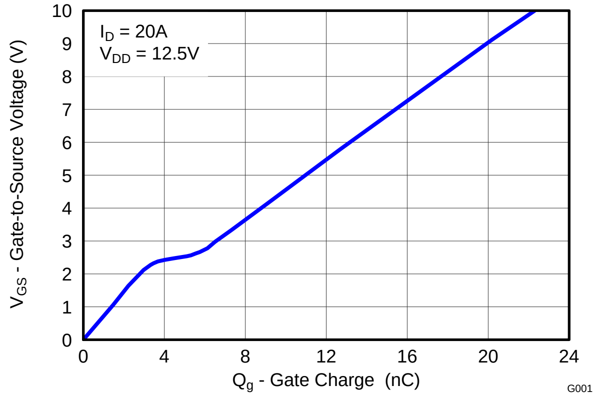

Figure 15. Control MOSFET Gate Charge

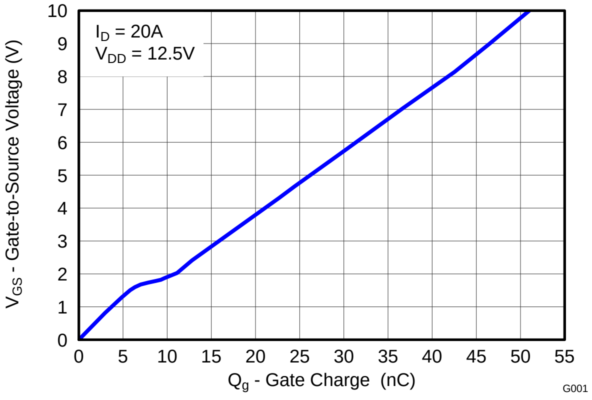

Figure 16. Sync MOSFET Gate Charge

Typical Power Block MOSFET Characteristics (continued)

T_A = 25°C, unless stated otherwise.

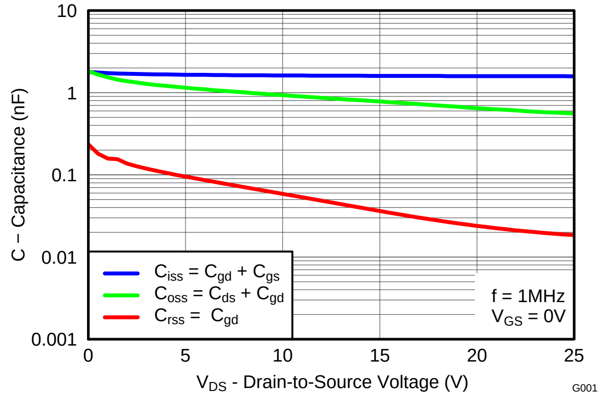

Figure 17. Control MOSFET Capacitance

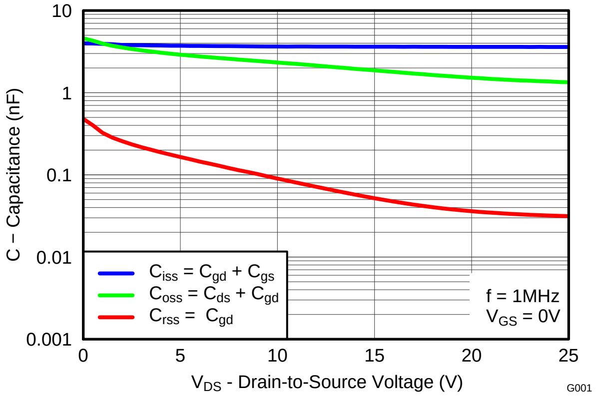

Figure 18. Sync MOSFET Capacitance

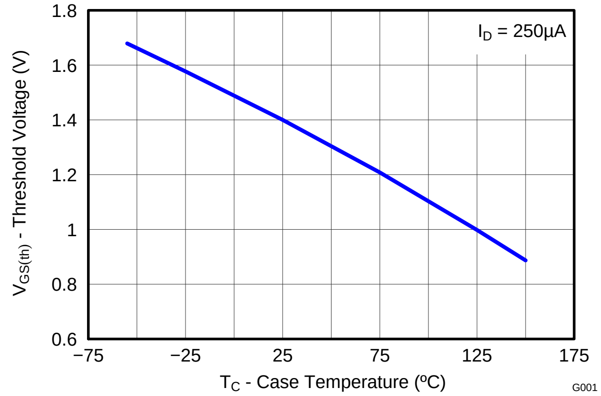

Figure 19. Control MOSFET $V_{GS(th)}$

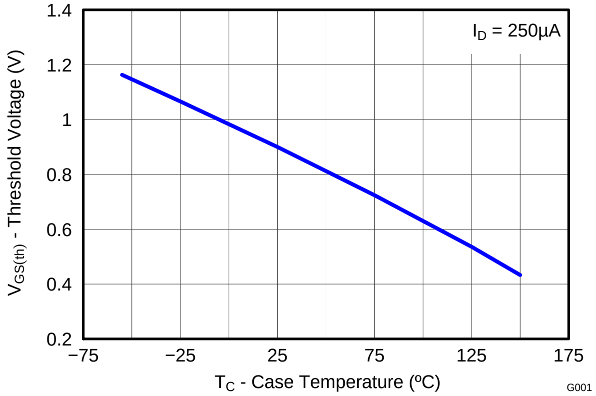

Figure 20. Sync MOSFET $V_{GS(th)}$

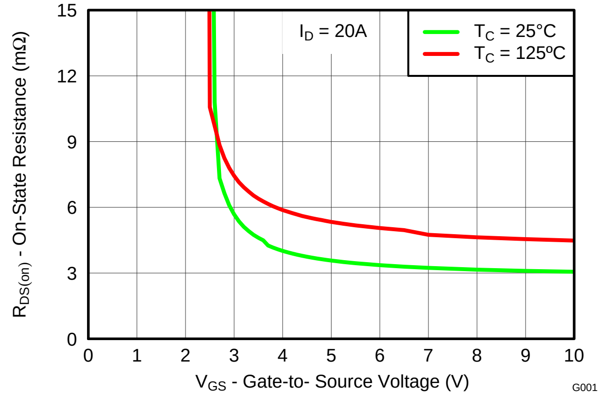

Figure 21. Control MOSFET $R_{DS(on)}$ vs V_{GS}

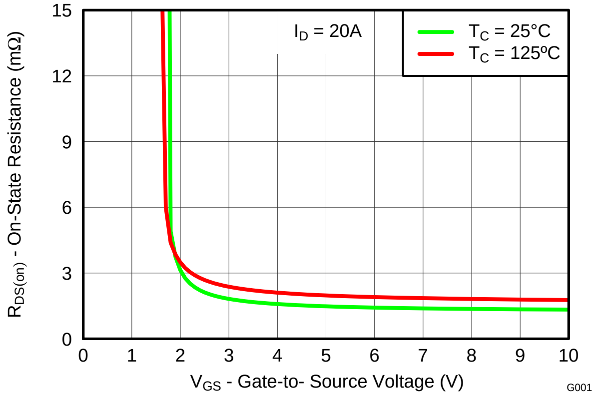

Figure 22. Sync MOSFET $R_{DS(on)}$ vs V_{GS}

Typical Power Block MOSFET Characteristics (continued)

T_A = 25°C, unless stated otherwise.

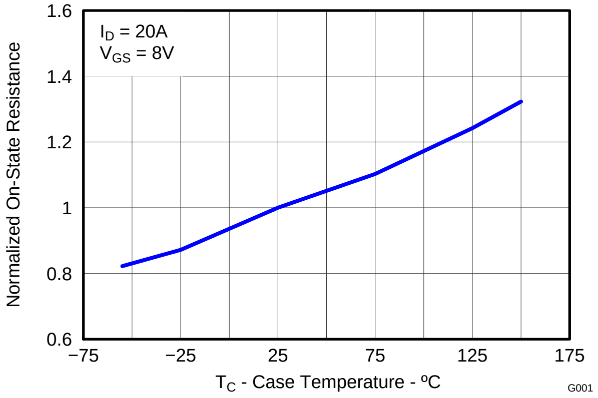

Figure 23. Control MOSFET Normalized $R_{DS(on)}$

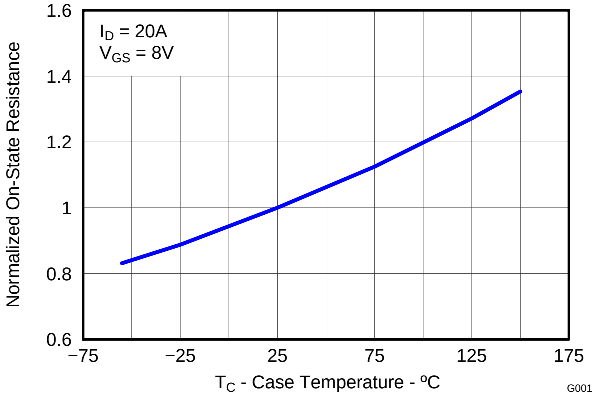

Figure 24. Sync MOSFET Normalized $R_{DS(on)}$

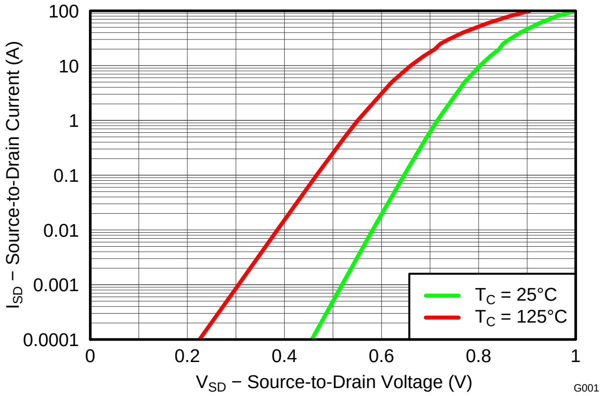

Figure 25. Control MOSFET Body Diode

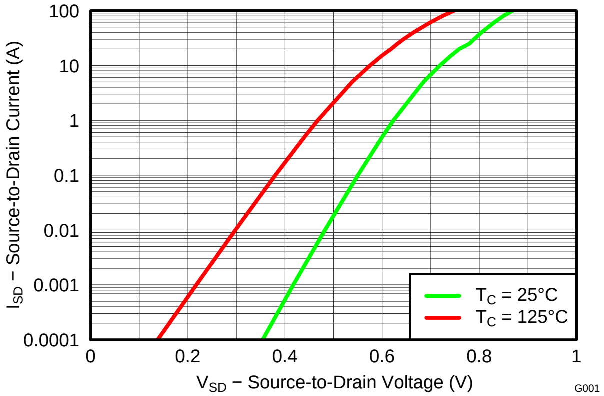

Figure 26. Sync MOSFET Body Diode

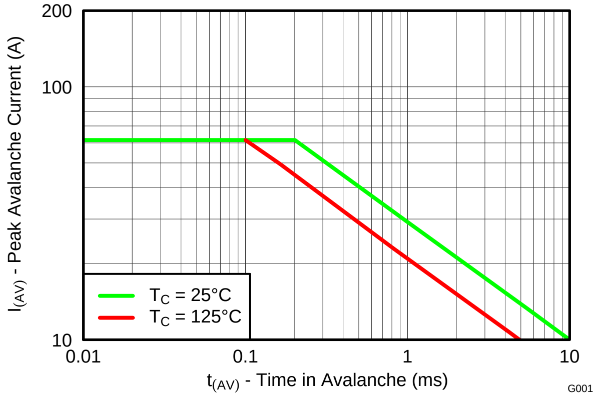

Figure 27. Control MOSFET Unclamped Inductive Switching

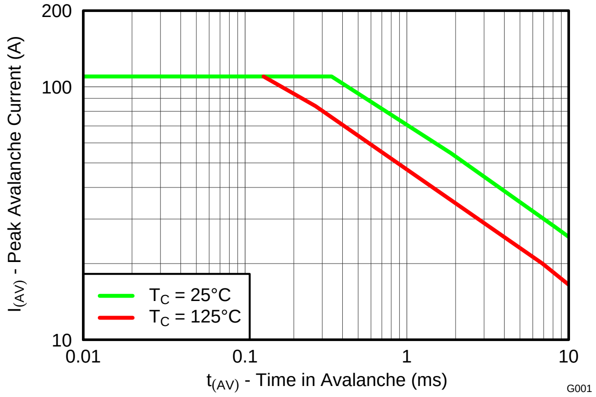

Figure 28. Sync MOSFET Unclamped Inductive Switching

6 Application and Implementation

NOTE

Information in the following Application section is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI customers are responsible for determining suitability of components selection for their designs. Customers should validate and test their design implementation to confirm system functionality.

6.1 Application Information

6.1.1 Equivalent System Performance

Many of today's high-performance computing systems require low-power consumption in an effort to reduce system operating temperatures and improve overall system efficiency. This has created a major emphasis on improving the conversion efficiency of today's synchronous buck topology. In particular, there has been an emphasis in improving the performance of the critical power semiconductor in the power stage of this application (see Figure 29). As such, optimization of the power semiconductors in these applications, needs to go beyond simply reducing $R_{DS(ON)}$.

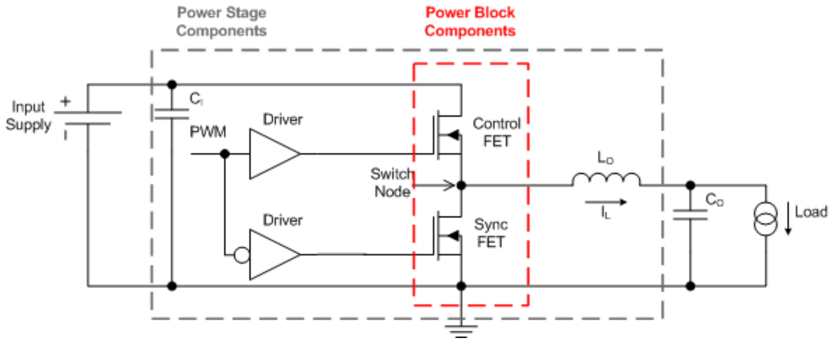

Figure 29. Equivalent System Schematic

The CSD86360Q5D is part of TI's power block product family, which is a highly optimized product for use in a synchronous buck topology requiring high current, high efficiency, and high frequency. It incorporates TI's latest generation silicon, which has been optimized for switching performance, as well as minimizing losses associated with Q_{GD}, Q_{GS}, and Q_{RR}. Furthermore, TI's patented packaging technology has minimized losses by nearly eliminating parasitic elements between the control FET and sync FET connections (see Figure 30). A key challenge solved by TI's patented packaging technology is the system level impact of Common Source Inductance (CSI). CSI greatly impedes the switching characteristics of any MOSFET, which in turn increases switching losses and reduces system efficiency. As a result, the effects of CSI need to be considered during the MOSFET selection process. In addition, standard MOSFET switching loss equations used to predict system efficiency need to be modified in order to account for the effects of CSI. Further details behind the effects of CSI and modification of switching loss equations are outlined in *Power Loss Calculation With CSI Consideration for Synchronous Buck Converters* (SLPA009).

Application Information (continued)

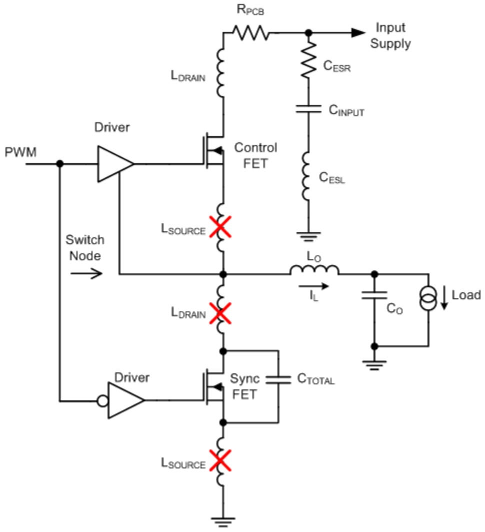

Figure 30. Elimination of Parasitic Inductances

The combination of TI's latest generation silicon and optimized packaging technology has created a benchmarking solution that outperforms industry standard MOSFET chipsets of similar $R_{DS(ON)}$ and MOSFET chipsets with lower $R_{DS(ON)}$. Figure 31 and Figure 32 compare the efficiency and power loss performance of the CSD86360Q5D versus industry standard MOSFET chipsets commonly used in this type of application. This comparison purely focuses on the efficiency and generated loss of the power semiconductors only. The performance of CSD86360Q5D clearly highlights the importance of considering the effective AC on-impedance ($Z_{DS(ON)}$) during the MOSFET selection process of any new design. Simply normalizing to traditional MOSFET $R_{DS(ON)}$ specifications is not an indicator of the actual in-circuit performance when using TI's power block technology.

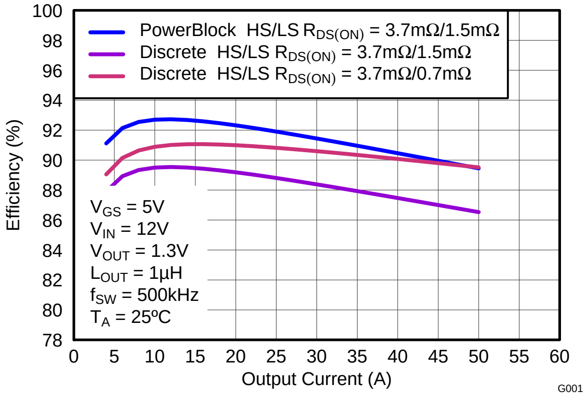

Figure 31. Efficiency Comparison for Discrete Parts vs Power Block

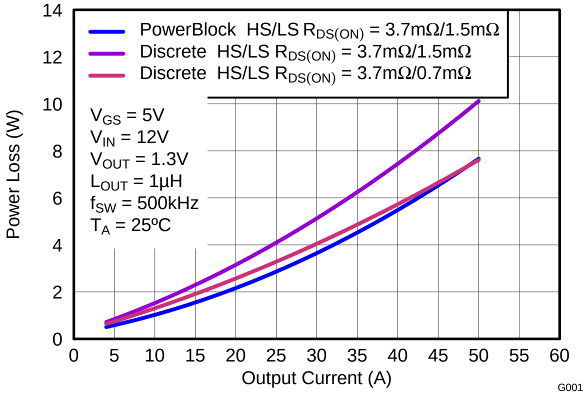

Figure 32. Power Loss Comparison for Discrete Parts vs Power Block

Application Information (continued)

Table 1 below compares the traditional DC measured $R_{DS(ON)}$ of CSD86360Q5D versus its $Z_{DS(ON)}$. This comparison takes into account the improved efficiency associated with TI’s patented packaging technology. As such, when comparing TI’s power block products to individually packaged discrete MOSFETs or dual MOSFETs in a standard package, the in-circuit switching performance of the solution must be considered. In this example, individually packaged discrete MOSFETs or dual MOSFETs in a standard package would need to have DC measured $R_{DS(ON)}$ values that are equivalent to CSD86360Q5D’s $Z_{DS(ON)}$ value in order to have the same efficiency performance at full load. Mid to light-load efficiency will still be lower with individually packaged discrete MOSFETs or dual MOSFETs in a standard package.

Table 1. Comparison of $R_{DS(ON)}$ vs $Z_{DS(ON)}$

PARAMETER	HS		LS	
	TYP	MAX	TYP	MAX
Effective AC on-impedance $Z_{DS(ON)}$ (V_{GS} = 5 V)	3.7	—	0.7	—
DC measured $R_{DS(ON)}$ (V_{GS} = 4.5 V)	3.7	4.5	1.5	1.9

The CSD86360Q5D NexFET™ power block is an optimized design for synchronous buck applications using 5-V gate drive. The control FET and sync FET silicon are parametrically tuned to yield the lowest power loss and highest system efficiency. As a result, a new rating method is needed, which is tailored towards a more systems-centric environment. System-level performance curves such as power loss, Safe Operating Area (SOA), and normalized graphs allow engineers to predict the product performance in the actual application.

6.1.2 Power Loss Curves

MOSFET centric parameters such as $R_{DS(ON)}$ and Q_{gd} are needed to estimate the loss generated by the devices. In an effort to simplify the design process for engineers, Texas Instruments has provided measured power loss performance curves. Figure 2 plots the power loss of the CSD86360Q5D as a function of load current. This curve is measured by configuring and running the CSD86360Q5D as it would be in the final application (see Figure 33).The measured power loss is the CSD86360Q5D loss and consists of both input conversion loss and gate drive loss. Equation 1 is used to generate the power loss curve.

$$(V_{IN} \times I_{IN}) + (V_{DD} \times I_{DD}) - (V_{SW\_AVG} \times I_{OUT}) = \text{Power loss} \quad (1)$$

The power loss curve in Figure 2 is measured at the maximum recommended junction temperatures of 125°C under isothermal test conditions.

6.1.3 Safe Operating Area (SOA) Curves

The SOA curves in the CSD86360Q5D data sheet provides guidance on the temperature boundaries within an operating system by incorporating the thermal resistance and system power loss. Figure 4 to Figure 6 outline the temperature and airflow conditions required for a given load current. The area under the curve dictates the safe operating area. All the curves are based on measurements made on a PCB design with dimensions of 4 in (W) × 3.5 in (L) × 0.062 in (T) and 6 copper layers of 1-oz copper thickness.

6.1.4 Normalized Curves

The normalized curves in the CSD86360Q5D data sheet provides guidance on the power loss and SOA adjustments based on their application specific needs. These curves show how the power loss and SOA boundaries will adjust for a given set of systems conditions. The primary Y-axis is the normalized change in power loss and the secondary Y-axis is the change is system temperature required in order to comply with the SOA curve. The change in power loss is a multiplier for the power loss curve and the change in temperature is subtracted from the SOA curve.

6.2 Typical Application

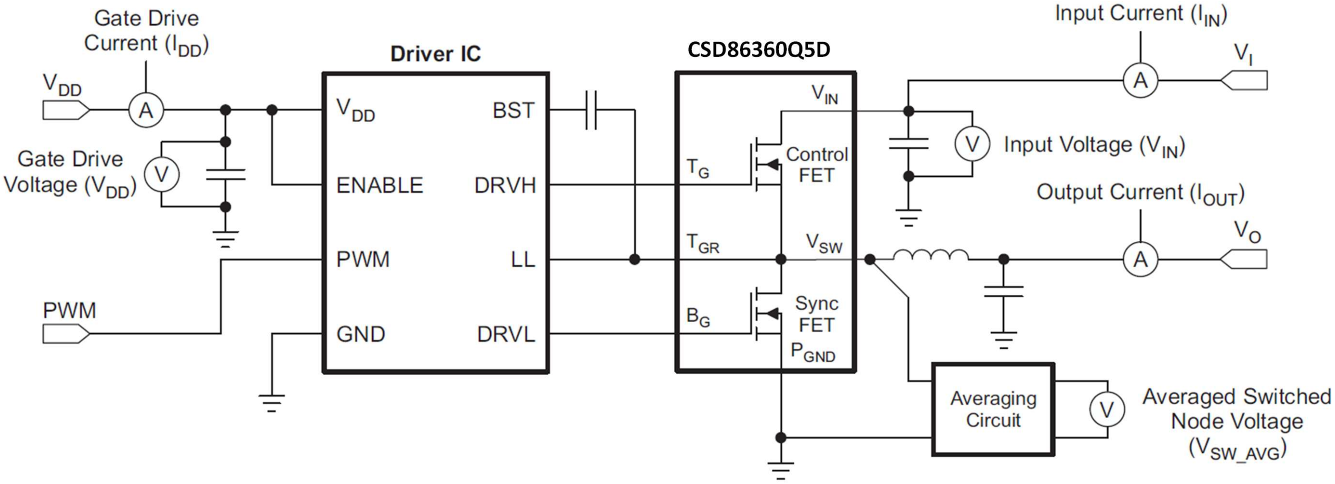

Figure 33. Typical Application

Typical Application (continued)

6.2.1 Design Example: Calculating Power Loss and SOA

The user can estimate product loss and SOA boundaries by arithmetic means (see *Operating Conditions* section). Though the power loss and SOA curves in this data sheet are taken for a specific set of test conditions, the following procedure will outline the steps the user should take to predict product performance for any set of system conditions.

6.2.1.1 Operating Conditions

- Output current = 25 A
- Input voltage = 7 V
- Output voltage = 1 V
- Switching frequency = 800 kHz
- Inductor = 0.2 µH

6.2.1.2 Calculating Power Loss

- Power loss at 25 A = 3.5 W (Figure 2)
- Normalized power loss for input voltage ≈ 1.03 (Figure 8)
- Normalized power loss for output voltage ≈ 0.90 (Figure 9)
- Normalized power loss for switching frequency ≈ 1.15 (Figure 7)
- Normalized power loss for output inductor ≈ 1.03 (Figure 10)
- **Final calculated power loss = 3.5 W × 1.03 × 0.90 × 1.15 × 1.03 ≈ 3.84 W**

6.2.1.3 Calculating SOA Adjustments

- SOA adjustment for input voltage ≈ 1.3°C (Figure 8)
- SOA adjustment for output voltage ≈ –2.5°C (Figure 9)
- SOA adjustment for switching frequency ≈ 6.0°C (Figure 7)
- SOA adjustment for output inductor ≈ 1.3°C (Figure 10)
- **Final calculated SOA adjustment = 1.3 + (–2.5) + 6.0 + 1.3 ≈ 6.1°C**

In the design example above, the estimated power loss of the CSD86360Q5D would increase to 3.84 W. In addition, the maximum allowable board and/or ambient temperature would have to decrease by 6.1°C. Figure 34 graphically shows how the SOA curve would be adjusted accordingly.

1. Start by drawing a horizontal line from the application current to the SOA curve.
2. Draw a vertical line from the SOA curve intercept down to the board/ambient temperature.
3. Adjust the SOA board/ambient temperature by subtracting the temperature adjustment value.

In the design example, the SOA temperature adjustment yields a reduction in allowable board/ambient temperature of 6.1°C. In the event the adjustment value is a negative number, subtracting the negative number would yield an increase in allowable board/ambient temperature.

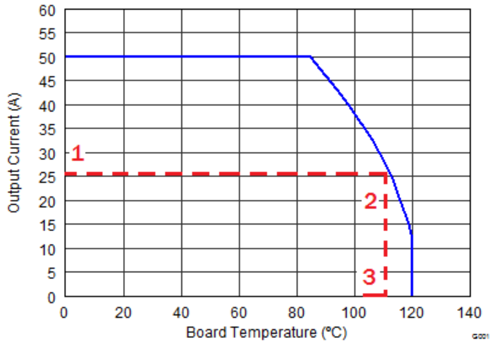

Figure 34. Power Block SOA

7 Layout

7.1 Layout Guidelines

There are two key system-level parameters that can be addressed with a proper PCB design: electrical and thermal performance. Properly optimizing the PCB layout will yield maximum performance in both areas. A brief description on how to address each parameter is provided.

7.1.1 Electrical Performance

The power block has the ability to switch voltages at rates greater than 10 kV/µs. Special care must be then taken with the PCB layout design and placement of the input capacitors, driver IC, and output inductor.

- The placement of the input capacitors relative to the power block's VIN and PGND pins should have the highest priority during the component placement routine. It is critical to minimize these node lengths. As such, ceramic input capacitors need to be placed as close as possible to the VIN and PGND pins (see Figure 35). The example in Figure 35 uses 6 × 10-µF ceramic capacitors (TDK Part # C3216X5R1C106KT or equivalent). Notice there are ceramic capacitors on both sides of the board with an appropriate amount of vias interconnecting both layers. In terms of priority of placement next to the power block, C5, C7, C19, and C8 should follow in order.
- The driver IC should be placed relatively close to the power block gate pins. T_G and B_G should connect to the outputs of the driver IC. The T_{GR} pin serves as the return path of the high-side gate drive circuitry and should be connected to the phase pin of the IC (sometimes called LX, LL, SW, PH, etc.). The bootstrap capacitor for the driver IC will also connect to this pin.
- The switching node of the output inductor should be placed relatively close to the power block VSW pins. Minimizing the node length between these two components will reduce the PCB conduction losses and actually reduce the switching noise level. In the event the switch node waveform exhibits ringing that reaches undesirable levels, the use of a boost resistor or RC snubber can be an effective way to easily reduce the peak ring level. The recommended boost resistor value will range between 1 Ω to 4.7 Ω depending on the output characteristics of driver IC used in conjunction with the power block. The RC snubber values can range from 0.5 Ω to 2.2 Ω for the R and 330 pF to 2200 pF for the C. Please refer to TI App Note *Snubber Circuits: Theory, Design and Application* (SLUP100) for more details on how to properly tune the RC snubber values. The RC snubber should be placed as close as possible to the VSW node and PGND see Figure 35 (1)

7.1.2 Thermal Performance

The power block has the ability to utilize the GND planes as the primary thermal path. As such, the use of thermal vias is an effective way to pull away heat from the device and into the system board. Concerns of solder voids and manufacturability problems can be addressed by the use of three basic tactics to minimize the amount of solder attach that will wick down the via barrel:

- Intentionally space out the vias from each other to avoid a cluster of holes in a given area.
- Use the smallest drill size allowed in your design. The example in Figure 35 uses vias with a 10-mil drill hole and a 16-mil capture pad.
- Tent the opposite side of the via with solder-mask.

In the end, the number and drill size of the thermal vias should align with the end user's PCB design rules and manufacturing capabilities.

---

(1) Keong W. Kam, David Pommerenke, "EMI Analysis Methods for Synchronous Buck Converter EMI Root Cause Analysis", University of Missouri – Rolla

7.2 Layout Example

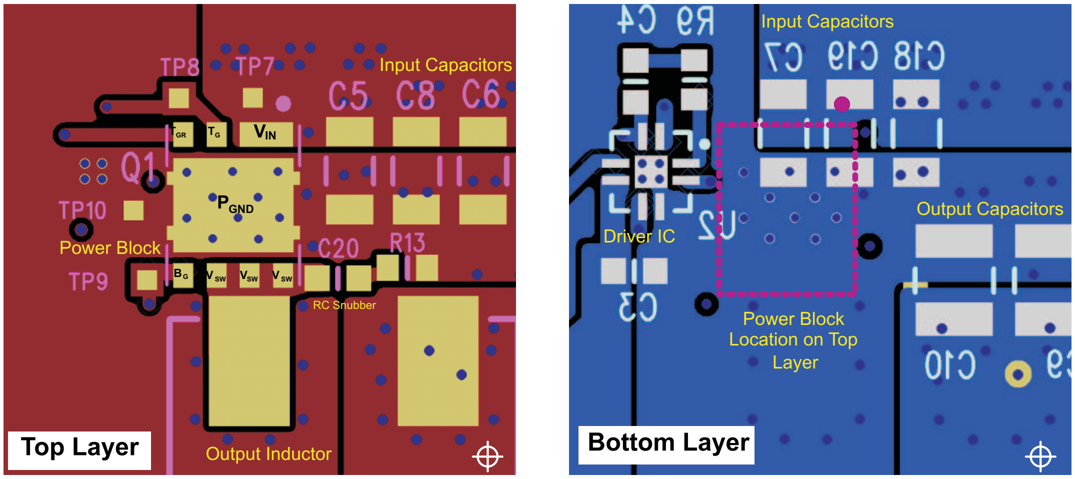

Figure 35. Recommended PCB Layout (Top Down View)

8 デバイスおよびドキュメントのサポート

8.1 ドキュメントのサポート

8.1.1 関連資料

関連資料については、以下を参照してください。

- *『同期整流降圧コンバータにおける共通ソース・インダクタンスでの電力損失計算の考慮事項』*(SLPA009)
- *『スナバ回路: 理論、設計、応用』*(SLUP100)

8.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

8.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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設計サポート ***TIの設計サポート*** 役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

8.4 商標

NexFET, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

8.5 静電気放電に関する注意事項

これらのデバイスは、限定的なESD（静電破壊）保護機能を内 蔵しています。保存時または取り扱い時は、MOSゲートに対す る静電破壊を防止するために、リード線同士をショートさせて おくか、デバイスを導電フォームに入れる必要があります。

8.6 Glossary

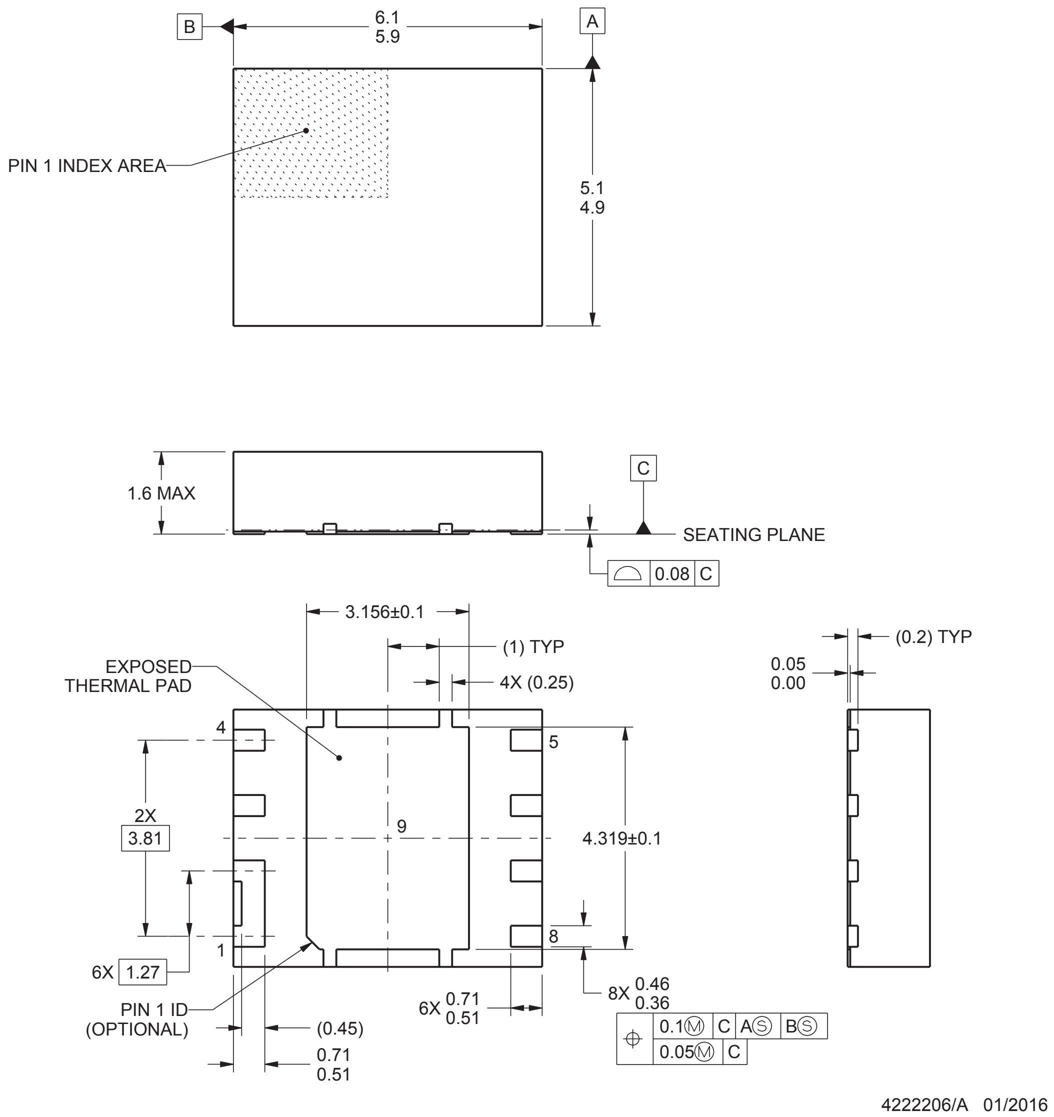
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

9 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

9.1 Q5Dパッケージの寸法

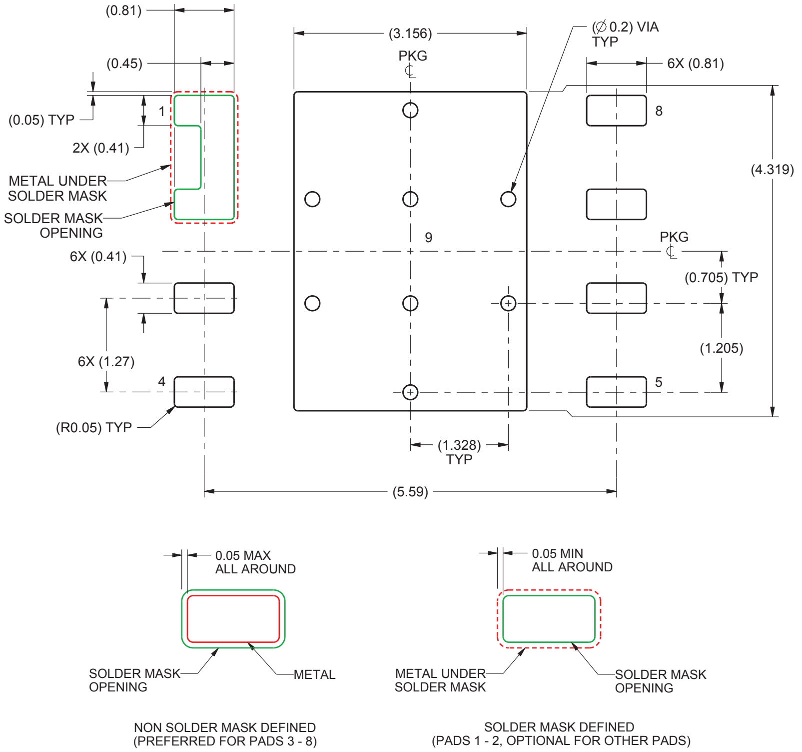


1. すべての直線寸法はミリメートル(mm)単位です。括弧内のすべての寸法は、参照のみを目的としたものです。寸法と許容誤差は、ASME Y14.5M準拠です。
2. この図面は、予告なく変更される可能性があります。
3. 熱特性および機械的な性能を実現するため、パッケージのサーマル・パッドはプリント基板にハンダ付けする必要があります。

Q5Dパッケージの寸法 (continued)

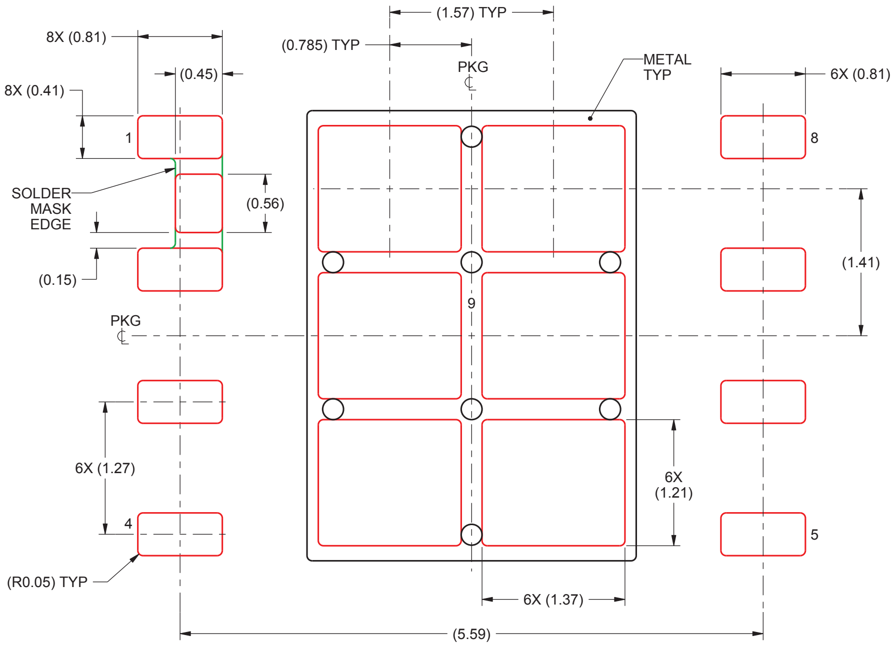
寸法	ミリメートル		インチ	
	最小	最大	最小	最大
a	1.40	1.5	0.055	0.059
b	0.360	0.460	0.014	0.018
c	0.150	0.250	0.006	0.010
c1	0.150	0.250	0.006	0.010
d	1.630	1.730	0.064	0.068
d1	0.280	0.380	0.011	0.015
d2	0.200	0.300	0.008	0.012
d3	0.291	0.391	0.012	0.015
D1	4.900	5.100	0.193	0.201
D2	4.269	4.369	0.168	0.172
E	4.900	5.100	0.193	0.201
E1	5.900	6.100	0.232	0.240
E2	3.106	3.206	0.122	0.126
e	1.27 (標準値)		0.050	
f	0.396	0.496	0.016	0.020
L	0.510	0.710	0.020	0.028
θ	0.00	—	—	—
K	0.812		0.032	

9.2 推奨ランド・パターン



1. このパッケージは、基板上のサーマル・パッドにハンダ付けされるよう設計されています。詳細については、『QFN/SON PCBアタッチメント』(SLUA271)を参照してください。
2. ビアはアプリケーションに応じてのオプションです。デバイスのデータシートを参照してください。一部またはすべてを実装する場合に推奨されるビアの場所が示されています。

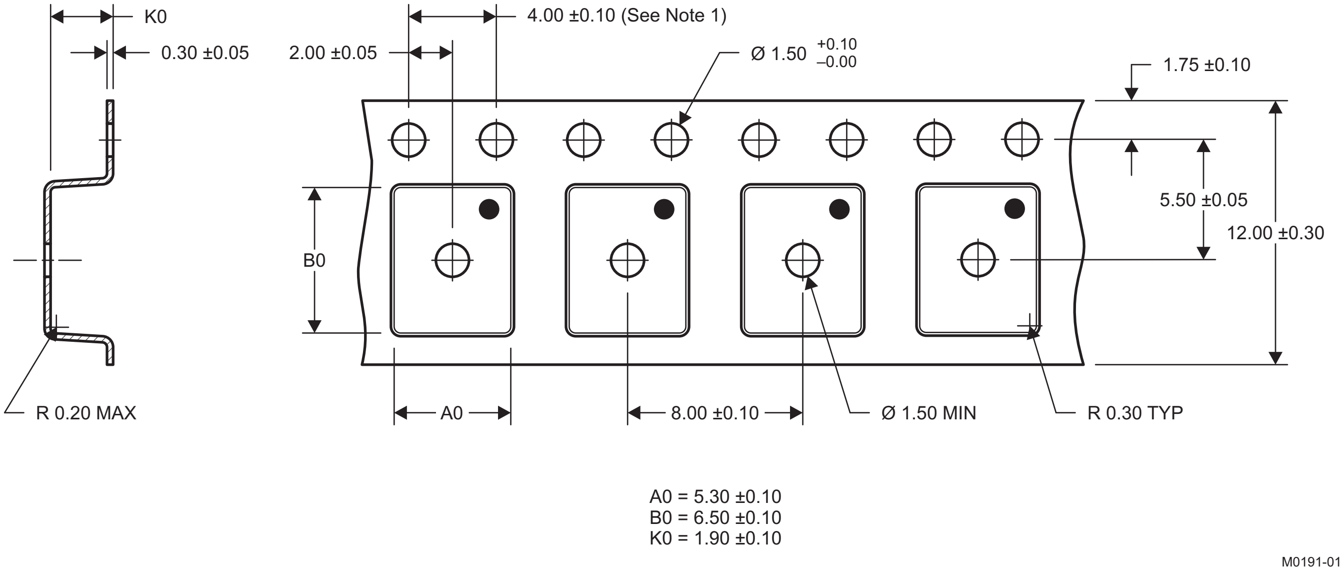
9.3 推奨ステンシル



1. レーザ・カット・アパーチャの壁面を台形にし、角に丸みを付けることで、ペースト離れが良くなります。IPC-7525には、別の設計推奨事項が存在する可能性があります。

PCB設計の推奨回路レイアウトについては、*『PCBレイアウト技法によるリンギングの低減』*(SLPA005)を参照してください。

9.4 Q5Dのテープ・アンド・リール情報



NOTES: 1.10スプロケット・ホール・ピッチの累積許容誤差は±0.2

2. キャンバーは100mm内に1mmを超えないこと(250mm以上では累積しない)。

3. 材質: 黒色の静電散逸性ポリスチレン。

4. すべての寸法は、特記されていない限りmm単位

5. 厚さ: 0.3±0.05mm

6. MSL1 260℃ (IRおよび対流方式) PbFリフロー互換

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD86360Q5D	ACTIVE	LSON-CLIP	DQY	8	2500	RoHS-Exempt & Green	NIPDAU | SN	Level-1-260C-UNLIM	-55 to 150	86360D	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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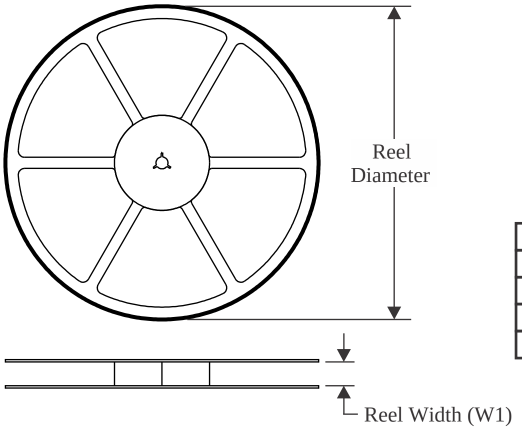
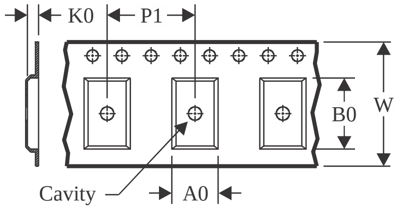
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

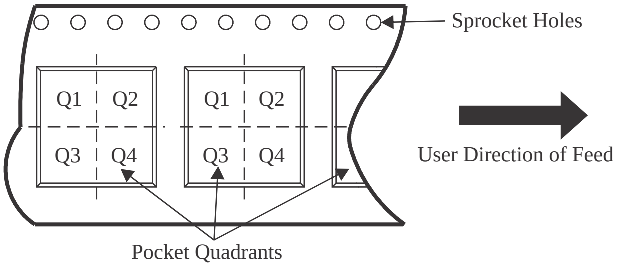


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

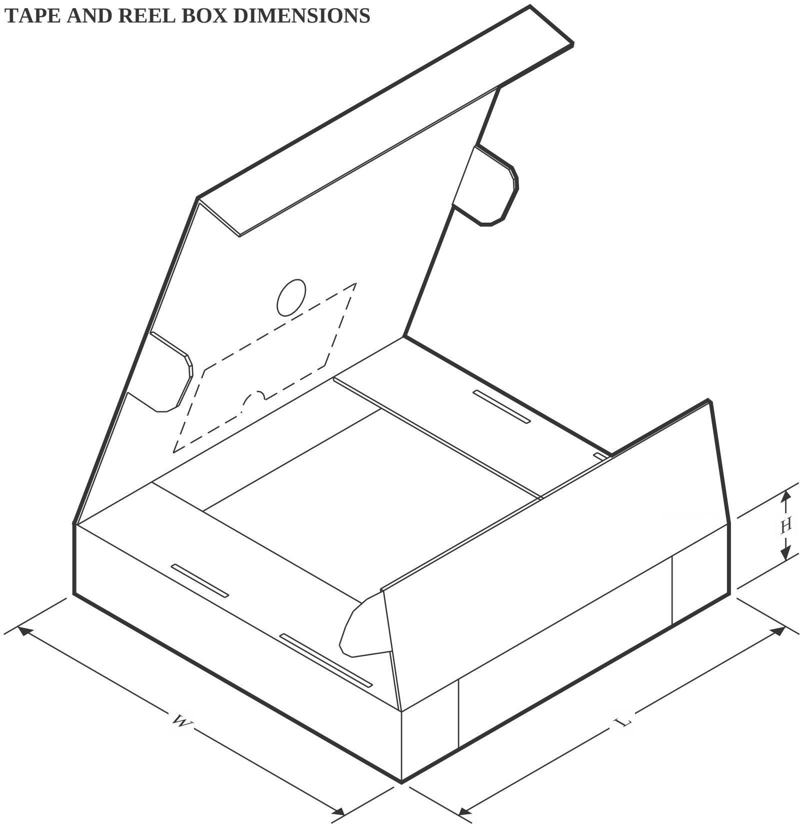
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

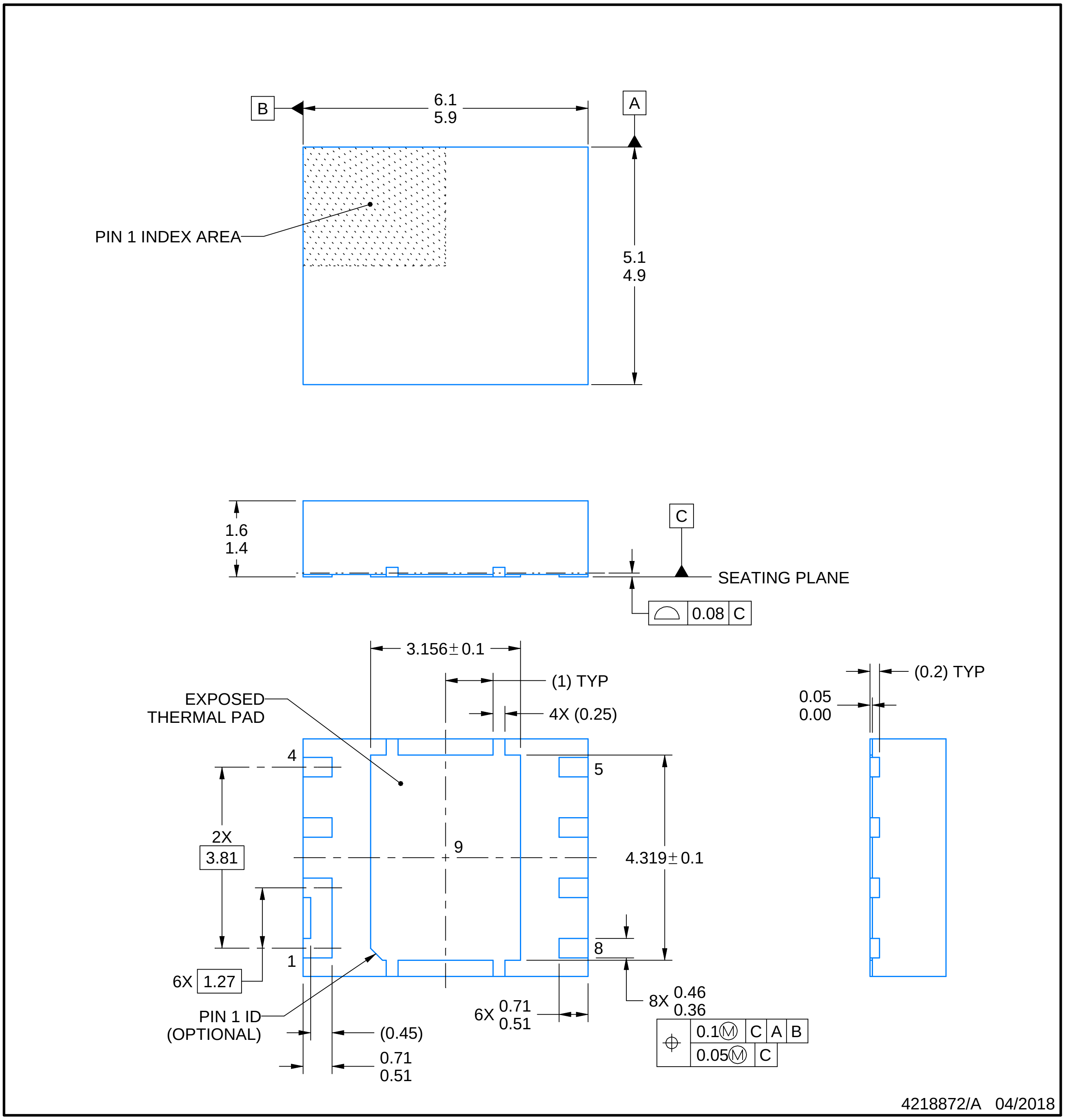
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD86360Q5D	LSON-CLIP	DQY	8	2500	330.0	12.4	5.3	6.3	1.8	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



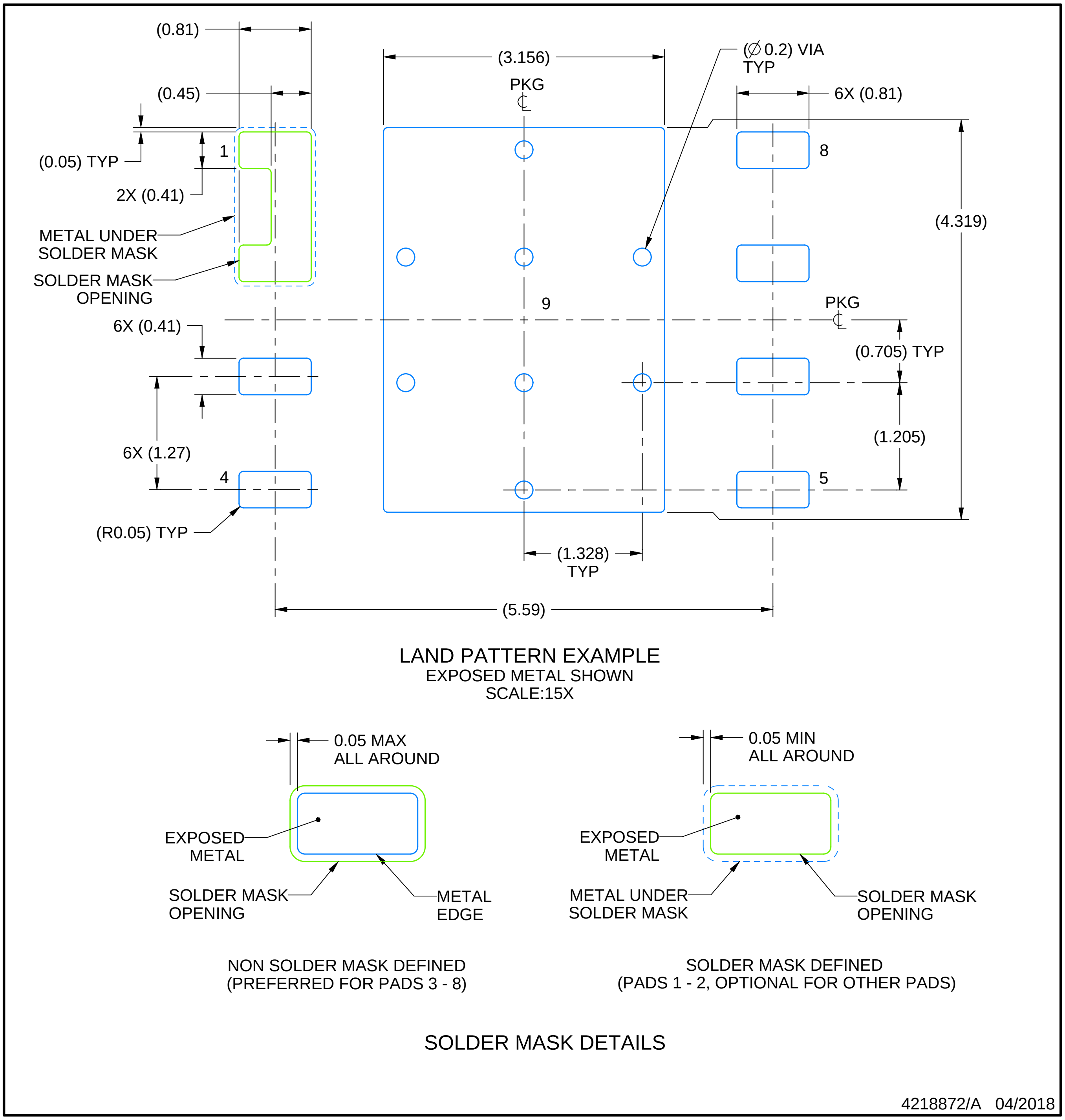
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD86360Q5D	LSON-CLIP	DQY	8	2500	346.0	346.0	33.0



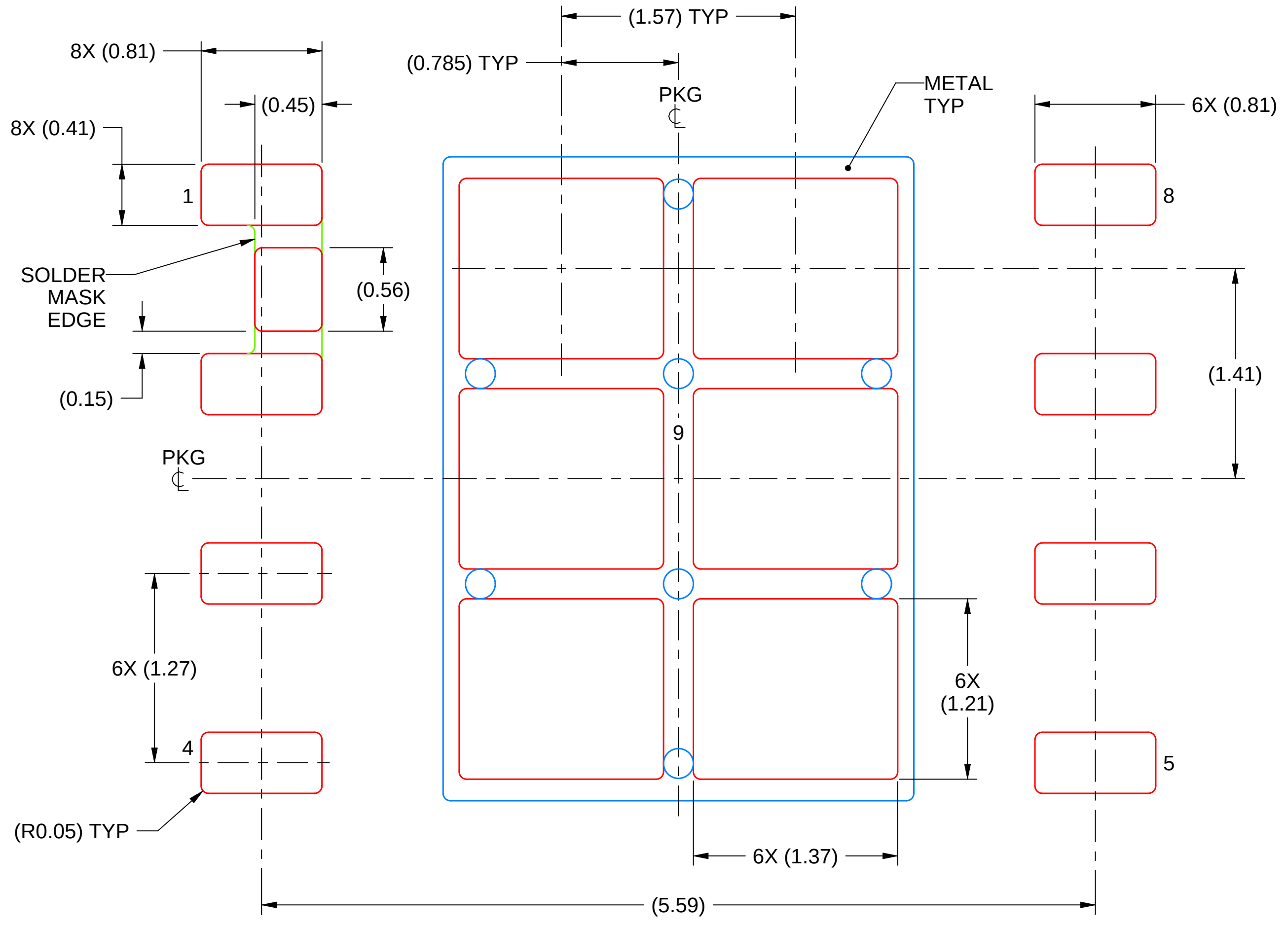
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
73% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要なお知らせと免責事項

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