TEXAS INSTRUMENTS
DRV8837C
JAJSCD0A – JULY 2016 – REVISED JULY 2016

DRV8837C 1A低電圧、Hブリッジ・ドライバ

1 特長

- Hブリッジ・モータ・ドライバ
  - DCモータまたは他の負荷を駆動
  - 低いMOSFETオン抵抗: HS + LS 1Ω
- 最大1Aの駆動電流
- 動作電源電圧範囲: 0～11V
- 標準PWMインターフェイス(IN1/IN2)
- 低消費電力のスリープ・モード、スリープ時の最大電流120nA
  - nSLEEPピン
- 小さなパッケージと占有面積
  - 8 WSON (サーマル・パッド付き)
  - 2.0×2.0mm
- 保護機能
  - VCC低電圧誤動作防止(UVLO)
  - 過電流保護(OCP)
  - サーマル・シャットダウン(TSD)

2 アプリケーション

- カメラ
- DSLRレンズ
- コンシューマ製品
- 玩具
- ロボティクス
- 医療機器

3 概要

DRV8837Cデバイスは、カメラ、コンシューマ製品、玩具、その他低電圧またはバッテリ駆動のモーション制御用途に使用される内蔵用モータ・ドライバ・ソリューションです。このデバイスは、1つのDCモータ、またはソレノイドなど他のデバイスを駆動できます。出力ドライバ・ブロックには、モータ巻線を駆動するHブリッジとして構成されたNチャネルのパワーMOSFETが搭載されています。内部のチャージ・ポンプにより、必要なゲート・ドライブ電圧が生成されます。

DRV8837Cデバイスは、最大1Aの出力電流を供給できます。このデバイスは、モータの電源電圧0～11Vで動作し、制御ロジックは1.8V～5Vレールで動作できます。

DRV8837Cデバイスには、PWM (IN/IN)入力インターフェイスが搭載されています。

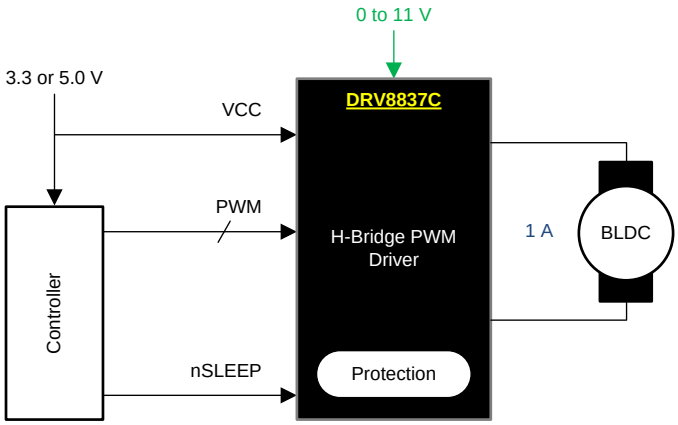
過電流保護、短絡保護、低電圧誤動作防止、および過熱保護のために、内部シャットダウン機能が用意されています。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
DRV8837C	WSON (8)	2.00mm×2.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

DRV8837Cの簡略ブロック図



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4 改訂履歴

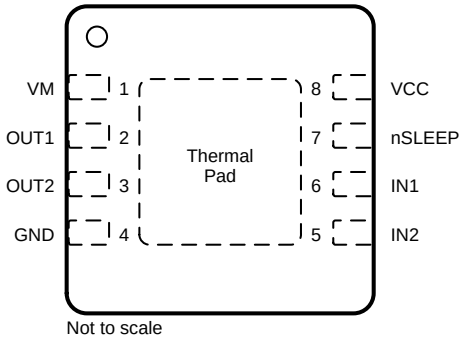
資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

2016年7月発行のものから更新 **Page**

- *デバイスのステータスを製品プレビューから量産データへ* 変更 ... 1

5 Pin Configuration and Functions

DSG Package
8-Pin WSON With Exposed Thermal Pad
Top View



Not to scale

Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
POWER AND GROUND			
GND	4	PWR	Device ground This pin must be connected to the PCB ground.
VCC	8	PWR	Logic power supply Bypass this pin to the GND pin with a 0.1-µF ceramic capacitor rated for VCC.
VM	1	PWR	Motor power supply Bypass this pin to the GND pin with a 0.1-µF ceramic capacitor rated for VM.
CONTROL			
IN1	6	I	IN1 input
IN2	5	I	IN2 input
nSLEEP	7	I	Sleep mode input When this pin is in logic low, the device enters low-power sleep mode. The device operates normally when this pin is logic high. The pin has an internal pulldown resistor to GND.
OUTPUT			
OUT1	2	O	Motor output Connect this pin to the motor winding.
OUT2	3	O	

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT
Motor power-supply voltage	VM	–0.3	12	V
Logic power-supply voltage	V_{CC}	–0.3	7	V
Control pin voltage	IN1, IN2, nSLEEP	–0.5	7	V
Peak drive current	OUT1, OUT2	Internally limited		A
Operating virtual junction temperature, T_J		–40	150	ºC
Storage temperature, T_{stg}		–60	150	ºC

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground pin.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{VM}	Motor power-supply voltage	0	11	V
V_{CC}	Logic power-supply voltage	1.8	7	V
I_{OUT}	Motor peak current	0	1	A
f_{PWM}	Externally applied PWM frequency	0	250	kHz
V_{LOGIC}	Logic level input voltage	0	5.5	V
T_A	Operating ambient temperature	–40	85	°C

6.4 Thermal Information

over operating free-air temperature range (unless otherwise noted)

THERMAL METRIC (1)		DRV8837C DSG (WSON) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	60.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	71.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	32.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	32.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	9.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

T_A = 25°C, over recommended operating conditions unless otherwise noted

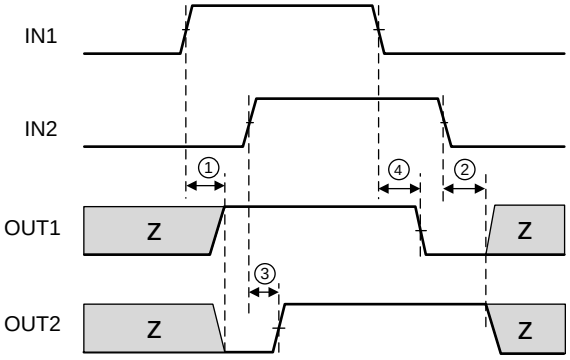
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (VM, V_{CC})						
V_{VM}	VM operating voltage		0		11	V
I_{VM}	VM operating supply current	V_{VM} = 5 V; V_{CC} = 3 V; No PWM		40	100	μA
		V_{VM} = 5 V; V_{CC} = 3 V; 50 kHz PWM		0.8	1.5	mA
I_{VMQ}	VM sleep mode supply current	V_{VM} = 5 V; V_{CC} = 3 V; nSLEEP = 0		30	95	nA
V_{CC}	V_{CC} operating voltage		1.8		7	V
I_{VCC}	V_{CC} operating supply current	V_{VM} = 5 V; V_{CC} = 3 V; No PWM		300	500	μA
		V_{VM} = 5 V; V_{CC} = 3 V; 50 kHz PWM		0.7	1.5	mA
I_{VCCQ}	V_{CC} sleep mode supply current	V_{VM} = 5 V; V_{CC} = 3 V; nSLEEP = 0		5	25	nA
CONTROL INPUTS (IN1/PH, IN2/EN, nSLEEP)						
V_{IL}	Input logic-low voltage				0.25 × V_{CC}	V
V_{IH}	Input logic-high voltage		0.5 × V_{CC}			V
V_{HYS}	Input logic hysteresis			0.08 × V_{CC}		V
I_{IL}	Input logic-low current	V_{INx} = 0 V	–5		5	μA
I_{IH}	Input logic-high current	V_{INx} = 3.3 V			50	μA
R_{PD}	Pulldown resistance			100		kΩ
MOTOR DRIVER OUTPUTS (OUT1, OUT2)						
$R_{DS(ON)}$	HS + LS FET on-resistance	V_{VM} = 5 V; V_{CC} = 3.3 V; I_O = 200 mA; T_J = 25°C		1000		mΩ
I_{OFF}	Off-state leakage current	V_{OUTx} = 0 V	–200		200	nA
PROTECTION CIRCUITS						
V_{UVLO}	V_{CC} undervoltage lockout	V_{CC} falling			1.7	V
		V_{CC} rising			1.8	V
I_{OCP}	Overcurrent protection trip level		1.2			A
t_{DEG}	Overcurrent deglitch time			1		μs
t_{RETRY}	Overcurrent retry time			1		ms
T_{TSD} (1)	Thermal shutdown temperature	Die temperature T_J	150	160	180	°C

(1) Not tested in production; limits are based on characterization data

6.6 Timing Requirements

T_A = 25°C, V_{VM} = 5 V, V_{CC} = 3 V, RL = 20 Ω

NO.				MIN	MAX	UNIT
1	t_7	Output enable time	See 図 1.		300	ns
2	t_8	Output disable time			300	ns
3	t_9	Delay time, INx high to OUTx high			160	ns
4	t_{10}	Delay time, INx low to OUTx low			160	ns
5	t_{11}	Output rise time		20	188	ns
6	t_{12}	Output fall time		20	188	ns
—	t_{wake}	Wake time, nSLEEP rising edge to part active			30	µs



DRV8837C

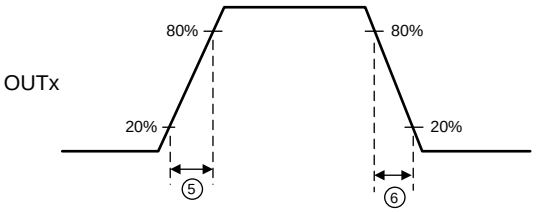


図 1. Input and Output Timing for DRV8837C

6.7 Typical Characteristics

Plots generated using characterization data.

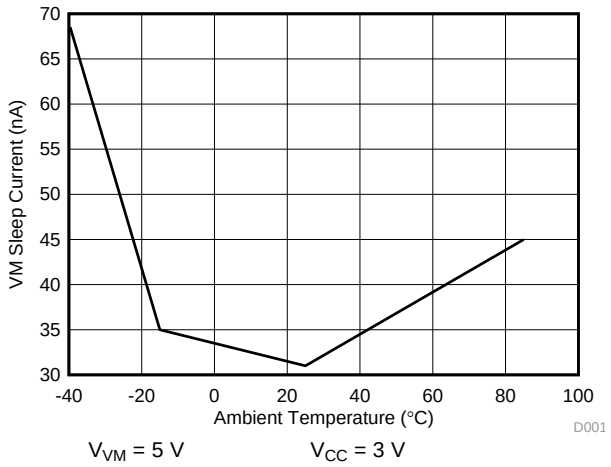


図 2. VM Sleep Current vs Ambient Temperature

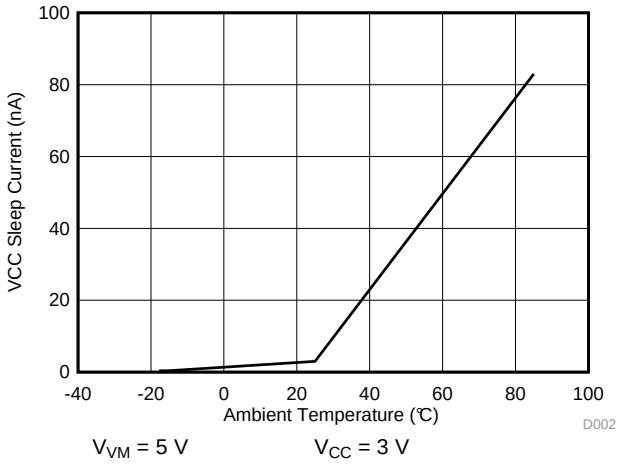


図 3. VCC Sleep Current vs Ambient Temperature

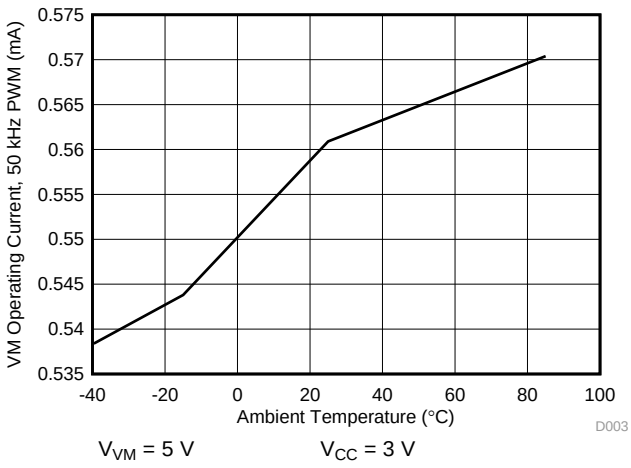


図 4. VM Operating Current vs Ambient Temperature

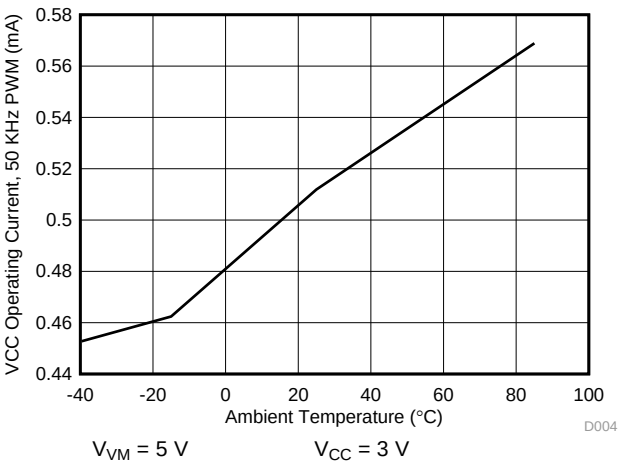


図 5. VCC Operating Current vs Ambient Temperature

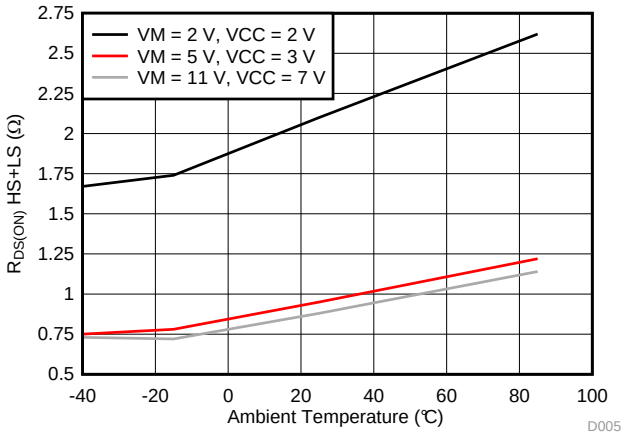


図 6. HS + LS $R_{DS(ON)}$ vs Ambient Temperature

7 Detailed Description

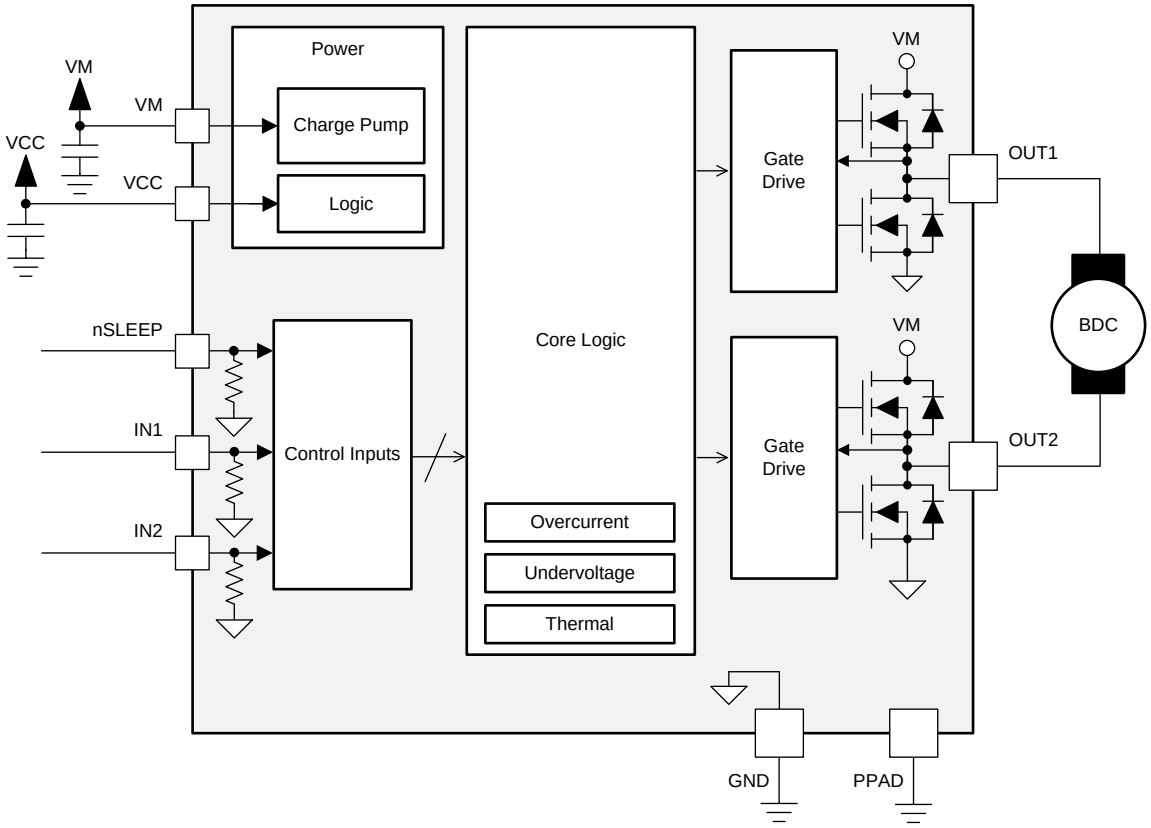
7.1 Overview

The DRV8837C device is an H-bridge driver that can drive one DC motor or other devices like solenoids. The outputs are controlled using a PWM interface (IN1/IN2).

A low-power sleep mode is included, which can be enabled using the nSLEEP pin.

This device greatly reduces the component count of motor driver systems by integrating the necessary driver FETs and FET control circuitry into a single device. In addition, the DRV8837C device adds protection features beyond traditional discrete implementations: undervoltage lockout, overcurrent protection, and thermal shutdown.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Bridge Control

The DRV8837C device is controlled using a PWM input interface, also called an IN/IN interface. Each output is controlled by a corresponding input pin.

表 1 shows the logic for the DRV8837C device.

表 1. DRV8837C Device Logic

nSLEEP	IN1	IN2	OUT1	OUT2	FUNCTION (DC MOTOR)
0	X	X	Z	Z	Coast
1	0	0	Z	Z	Coast
1	0	1	L	H	Reverse
1	1	0	H	L	Forward
1	1	1	L	L	Brake

7.3.2 Sleep Mode

If the nSLEEP pin is brought to a logic-low state, the DRV8837C device enters a low-power sleep mode. In this state, all unnecessary internal circuitry is powered down.

7.3.3 Power Supplies and Input Pins

The input pins can be driven within the recommended operating conditions with or without the VCC, VM, or both power supplies present. No leakage current path exists to the supply. Each input pin has a weak pulldown resistor (approximately 100 kΩ) to ground.

The VCC and VM supplies can be applied and removed in any order. When the VCC supply is removed, the device enters a low-power state and draws very little current from the VM supply. The VCC and VM pins can be connected together if the supply voltage is between 1.8 and 7 V.

The VM voltage supply does not have any undervoltage-lockout protection (UVLO). As long as V_{CC} > 1.8 V, the internal device logic remains active which means that the VM pin voltage can drop to 0 V, however, the load may not be sufficiently driven at low VM voltages.

7.3.4 Protection Circuits

The DRV8837C is fully protected against VCC undervoltage, overcurrent, and overtemperature events.

VCC undervoltage lockout If at any time the voltage on the VCC pin falls below the undervoltage lockout threshold voltage, all FETs in the H-bridge are disabled. Operation resumes when the VCC pin voltage rises above the UVLO threshold.

Overcurrent protection (OCP) An analog current-limit circuit on each FET limits the current through the FET by removing the gate drive. If this analog current limit persists for longer than t_{DEG}, all FETs in the H-bridge are disabled. Operation resumes automatically after t_{RETRY} has elapsed. Overcurrent conditions are detected on both the high-side and low-side devices. A short to the VM pin, GND, or from the OUT1 pin to theOUT2 pin results in an overcurrent condition.

Thermal shutdown (TSD) If the die temperature exceeds safe limits, all FETs in the H-bridge are disabled. After the die temperature falls to a safe level, operation automatically resumes.

表 2. Fault Behavior

FAULT	CONDITION	H-BRIDGE	RECOVERY
VCC undervoltage (UVLO)	VCC < 1.7 V	Disabled	VCC > 1.8 V
Overcurrent (OCP)	I_{OUT} > 1.2 A (MIN)	Disabled (retries automatically)	t_{RETRY} elapses
Thermal Shutdown (TSD)	T_J > 150°C (MIN)	Disabled (retries automatically)	T_J < 150°C

7.4 Device Functional Modes

The DRV8837C device is active unless the nSLEEP pin is brought logic low. In sleep mode the H-bridge FETs are disabled Hi-Z. The DRV8837C device is brought out of sleep mode automatically if nSLEEP is brought logic high.

The H-bridge outputs are disabled during undervoltage lockout, overcurrent, and overtemperature fault conditions.

表 3. Operation Modes

MODE	CONDITION	H-BRIDGE
Operating	nSLEEP pin = 1	Operating
Sleep mode	nSLEEP pin = 0	Disabled
Fault encountered	Any fault condition met	Disabled (retries automatically)

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DRV8837C device is device is used to drive one DC motor or other devices like solenoids. The following design procedure can be used to configure the DRV8837C device.

8.2 Typical Application

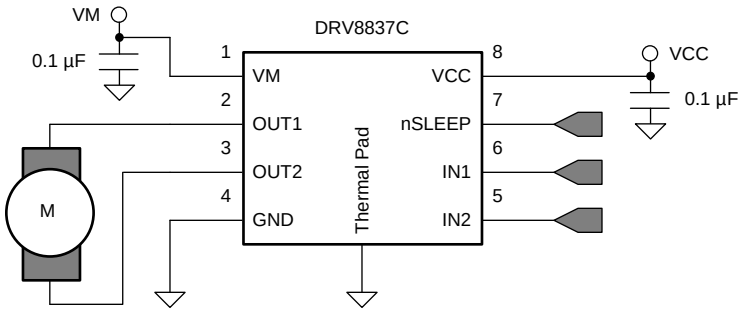


図 7. Schematic of DRV8837C Application

8.2.1 Design Requirements

表 4 lists the required parameters for a typical usage case.

表 4. System Design Requirements

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Motor supply voltage	VM	9 V
Logic supply voltage	VCC	3.3 V
Target RMS current	I_{OUT}	0.8 A

8.2.2 Detailed Design Procedure

8.2.2.1 Motor Voltage

The appropriate motor voltage depends on the ratings of the motor selected and the desired RPM. A higher voltage spins a brushed dc motor faster with the same PWM duty cycle applied to the power FETs. A higher voltage also increases the rate of current change through the inductive motor windings.

8.2.2.2 Low-Power Operation

When entering sleep mode, TI recommends setting all inputs as a logic low to minimize system power.

8.2.3 Application Curves

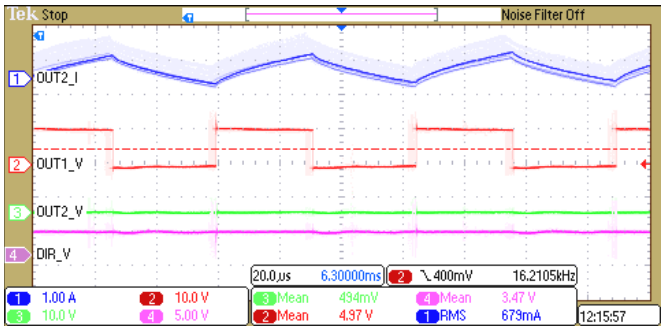


図 8. 50% Duty Cycle, Forward Direction

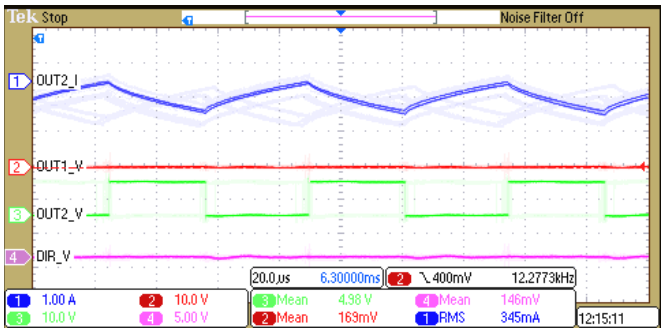


図 9. 50% Duty Cycle, Reverse Direction

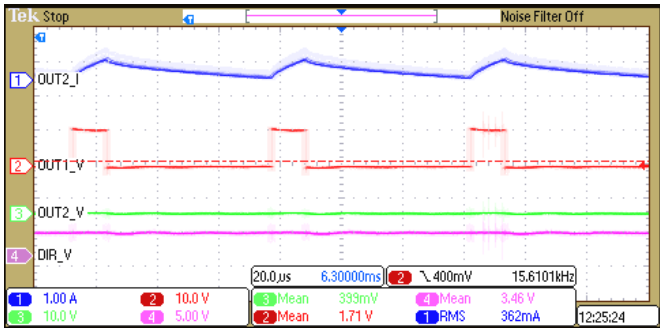


図 10. 20% Duty Cycle, Forward Direction

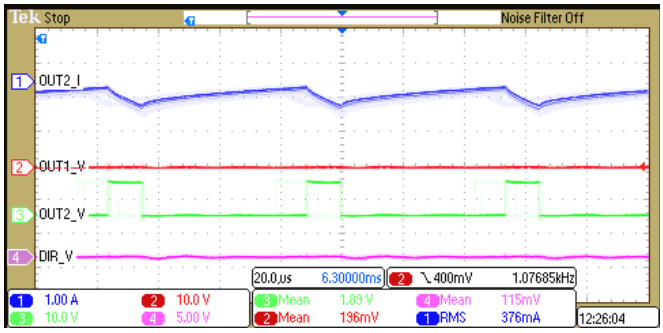


図 11. 20% Duty Cycle, Reverse Direction

9 Power Supply Recommendations

9.1 Bulk Capacitance

Having appropriate local bulk capacitance is an important factor in motor-drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system
- The power-supply capacitance and ability to source current
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple
- The type of motor used (brushed dc, brushless dc, stepper)
- The motor braking method

The inductance between the power supply and motor drive system limits the rate at which current can change from the power supply. If the local bulk capacitance is too small, the system responds to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate size of bulk capacitor.

Bulk Capacitance (continued)

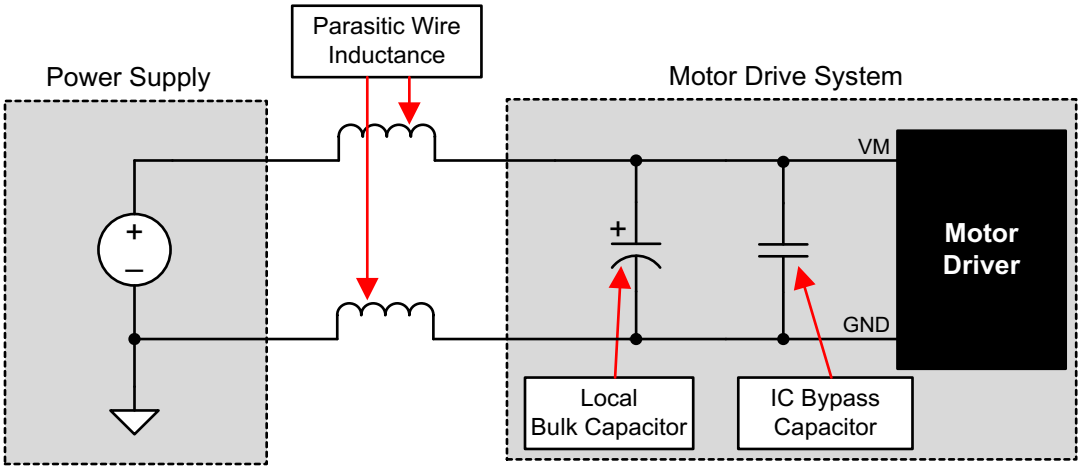


図 12. Example Setup of Motor Drive System With External Power Supply

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply

10 Layout

10.1 Layout Guidelines

The VM and VCC pins should be bypassed to GND using low-ESR ceramic bypass capacitors with a recommended value of 0.1 µF rated for the VM and VCC supplies. These capacitors should be placed as close to the VM and VCC pins as possible with a thick trace or ground plane connection to the device GND pin. In addition bulk capacitance is required on the VM pin.

10.2 Layout Example

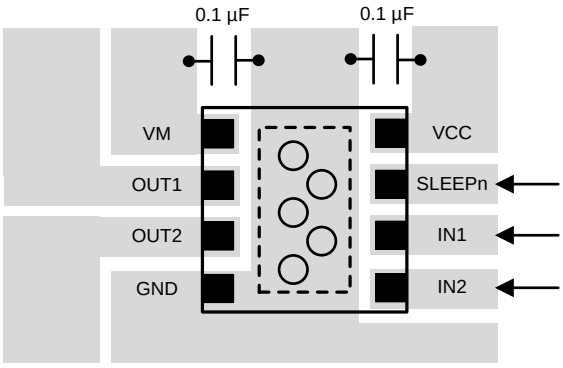


図 13. Simplified Layout Example

10.3 Power Dissipation

Power dissipation in the DRV8837C device is dominated by the power dissipated in the output FET resistance, or $R_{DS(ON)}$. Use 式 1 to estimate the average power dissipation when running a brushed-DC motor.

$$P_{TOT} = R_{DS(ON)} \times (I_{OUT(RMS)})^2 \quad (1)$$

where

- P_{TOT} is the total power dissipation
- $R_{DS(ON)}$ is the resistance of the HS plus LS FETs
- $I_{OUT(RMS)}$ is the RMS or DC output current being supplied to the load

The maximum amount of power that can be dissipated in the device is dependent on ambient temperature and heatsinking.

注

The value of $R_{DS(ON)}$ increases with temperature, so as the device heats, the power dissipation increases.

The DRV8837C device has thermal shutdown protection. If the die temperature exceeds approximately 150°C, the device is disabled until the temperature drops to a safe level.

Any tendency of the device to enter thermal shutdown is an indication of either excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

11 デバイスおよびドキュメントのサポート

11.1 ドキュメントのサポート

11.1.1 関連資料

関連資料については、以下を参照してください。

- *『モータ・ドライバの消費電力の計算』*(SLVA504)
- *『DRV8837C評価モジュール ユーザー・ガイド』*(SLVUAS3)
- *『モータ・ドライバの電流定格について』*(SLVA505)

11.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 商標

E2E is a trademark of Texas Instruments.
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11.5 静電気放電に関する注意事項

すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。これらの情報は、指定のデバイスに対して提供されている最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8837CDSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	837C	Samples
DRV8837CDSGT	LIFEBUY	WSON	DSG	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	837C	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

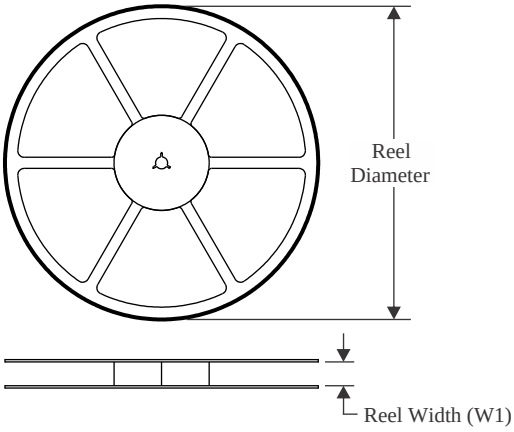
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

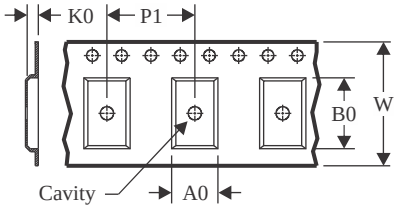
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

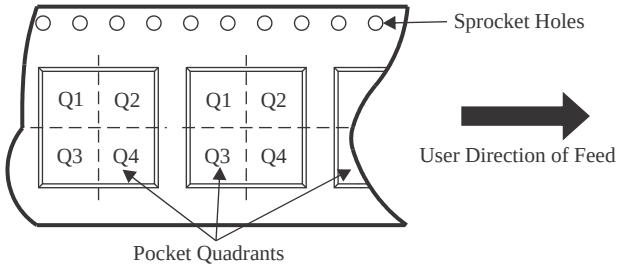


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

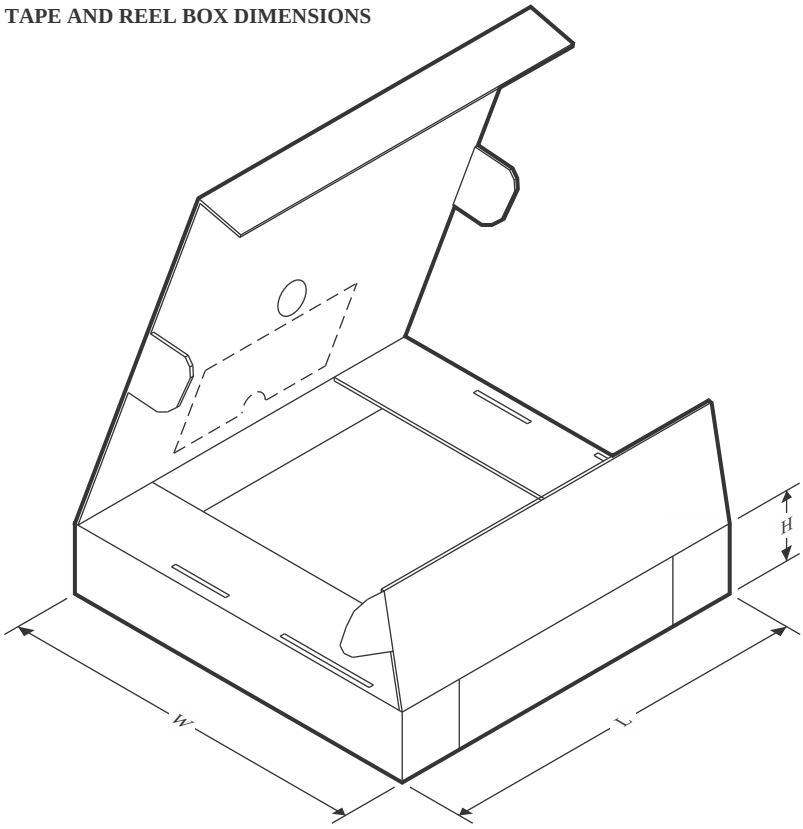
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8837CDSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
DRV8837CDSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
DRV8837CDSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
DRV8837CDSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8837CDSGR	WSON	DSG	8	3000	210.0	185.0	35.0
DRV8837CDSGR	WSON	DSG	8	3000	182.0	182.0	20.0
DRV8837CDSGT	WSON	DSG	8	250	182.0	182.0	20.0
DRV8837CDSGT	WSON	DSG	8	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

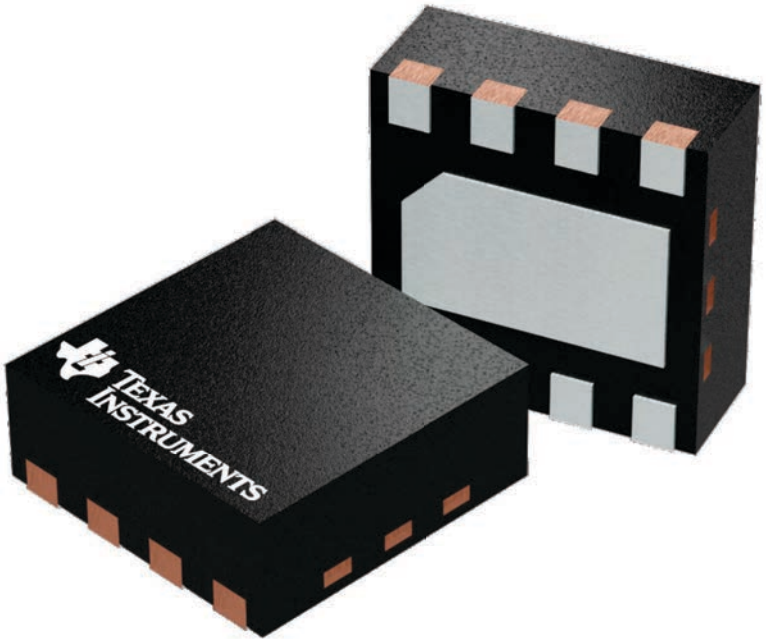
DSG 8

WSON - 0.8 mm max height

2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



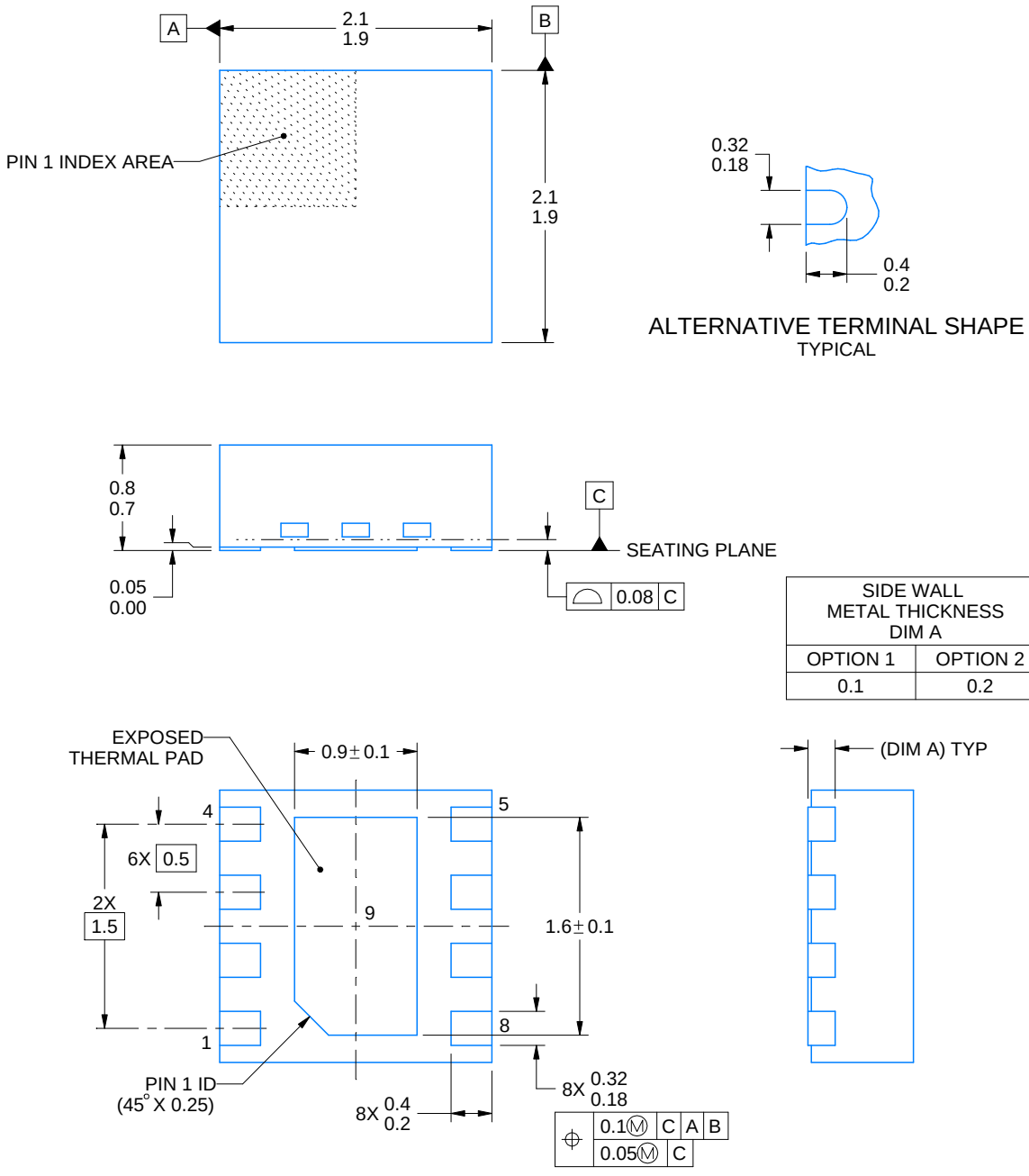
4224783/A

PACKAGE OUTLINE

DSG0008A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



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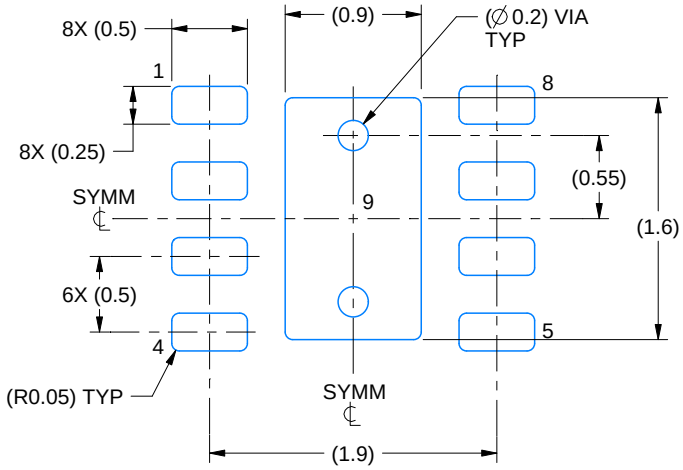
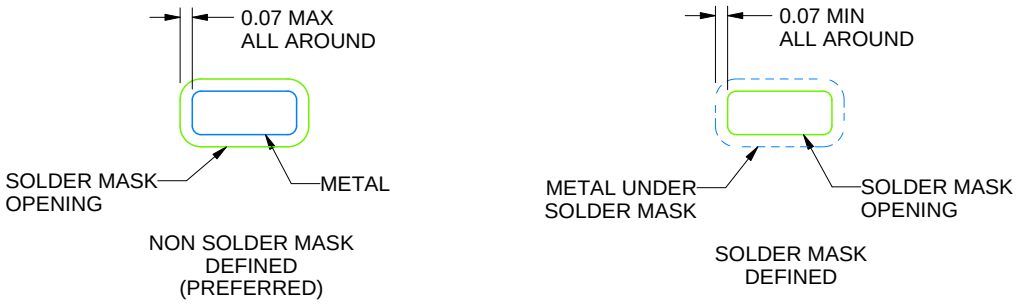
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

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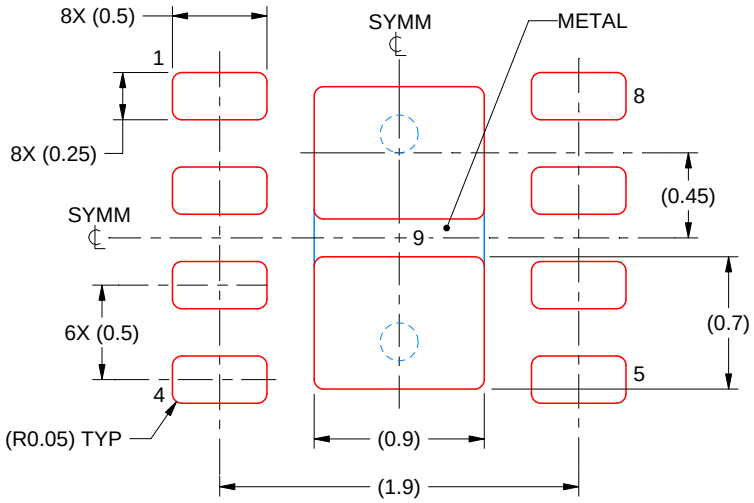
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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