



# DS90C187 低消費電力、1.8Vのデュアル・ピクセルFPD-Link (LVDS) シリアライザ

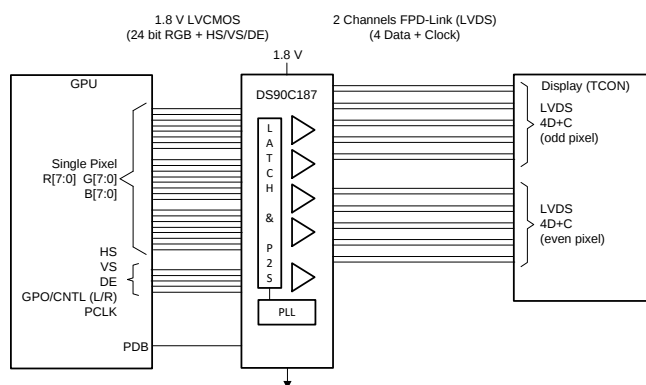
## 1 特長

- 185MHzでの標準消費電力100mW (SIDOモード)
- QXGAおよびWQXGAクラスのディスプレイを駆動
- 3つの動作モード
  - シングル・ピクセル・イン、シングル・ピクセル・アウト (SISO): 最高105MHz
  - シングル・ピクセル・イン、デュアル・ピクセル・アウト (SIDO): 最高 185MHz
  - デュアル・ピクセル・イン、デュアル・ピクセル・アウト (DIDO): 105MHz
- 24ビットRGBおよび48ビットRGBをサポート
- (オプション)低消費電力モードで18ビットRGBおよび36ビットRGBをサポート
- 3D+C、4D+C、6D+C、6D+2C、8D+C、8D+2CのLVDS構成をサポート
- FPD-Linkデシリアライザと互換
- 単一の1.8V電源で動作
- 1.8V LVCMOSと直接接続
- スリープ・モードでの消費電力1mW未満
- 拡散スペクトラム・クロック互換
- 小型の7mm×7mm×0.9mm、92ピン、2列のVQFNパッケージ

## 2 アプリケーション

- カメラ監視システム(CMS)
- 車載用ヘッド・ユニット
- スマート・ミラー
- クラスタ

### 代表的なアプリケーション



## 3 概要

DS90C187は、携帯用のバッテリー駆動型の低消費電力シリアライザで、ホストGPUとディスプレイ間のRGBインターフェースのサイズを低減できます。

DS90C187シリアライザは、ホストとフラット・パネル・ディスプレイとの間で60Hz、QXGA (2048x1536)までの解像度のデュアル・ピクセル・データ転送をサポートするよう設計されています。トランスミッタは48ビットまで(24ビット・カラーのデュアル・ピクセル)の1.8V LVCMOSデータを、2チャンネルの4データ+クロック(4D+C)、縮小幅インターフェースのLVDS互換データ・ストリームに変換します。

DS90C187は、3モードの動作をサポートしています。

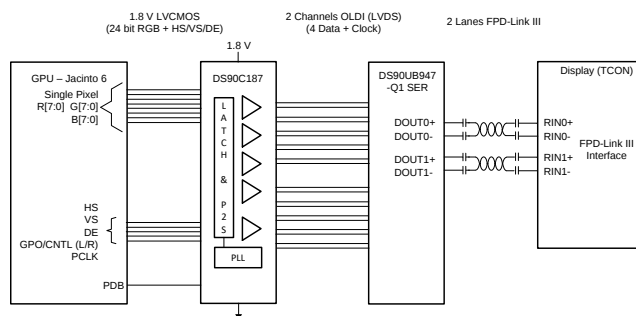
- シングル・ピクセル・イン/シングル・ピクセル・アウト・モードでは、60HzでSXGA+ (1400×1050)までのディスプレイを駆動できます。このモードでは、デバイスは1バンクの24ビットRGBデータを、1チャンネルの4D+C LVDSデータ・ストリームに変換します。
- シングル・ピクセル・イン/デュアル・ピクセル・アウト・モードでは、60HzでWUXGA+ (1920×1440)までのディスプレイを駆動できます。この構成で、デバイスはシングルからデュアルへのピクセル変換を行い、1バンクの24ビットRGBデータを、2チャンネルでピクセル・クロック速度が半分の4D+C LVDSストリームに変換します。

### 製品情報<sup>(1)</sup>

| 型番       | パッケージ        | 本体サイズ(公称)     |
|----------|--------------|---------------|
| DS90C187 | VQFN-MR (92) | 7.00mm×7.00mm |

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

### 代表的なアプリケーション



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## 4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

| Revision B (April 2013) から Revision C に変更                                                                                                                                 |  | Page      |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|-----------|
| • 「製品情報」表、「製品比較」表、「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加 ..... |  | <b>1</b>  |
| • Added Start Up / Phase Lock Loop Set Time timing diagram .....                                                                                                          |  | <b>10</b> |
| • Added content to the <i>Power Up Sequence</i> section .....                                                                                                             |  | <b>27</b> |

| Revision A (April 2013) から Revision B に変更       |  | Page     |
|-------------------------------------------------|--|----------|
| • ナショナル セミコンダクターのデータシートのレイアウトをTIフォーマットに変更 ..... |  | <b>1</b> |

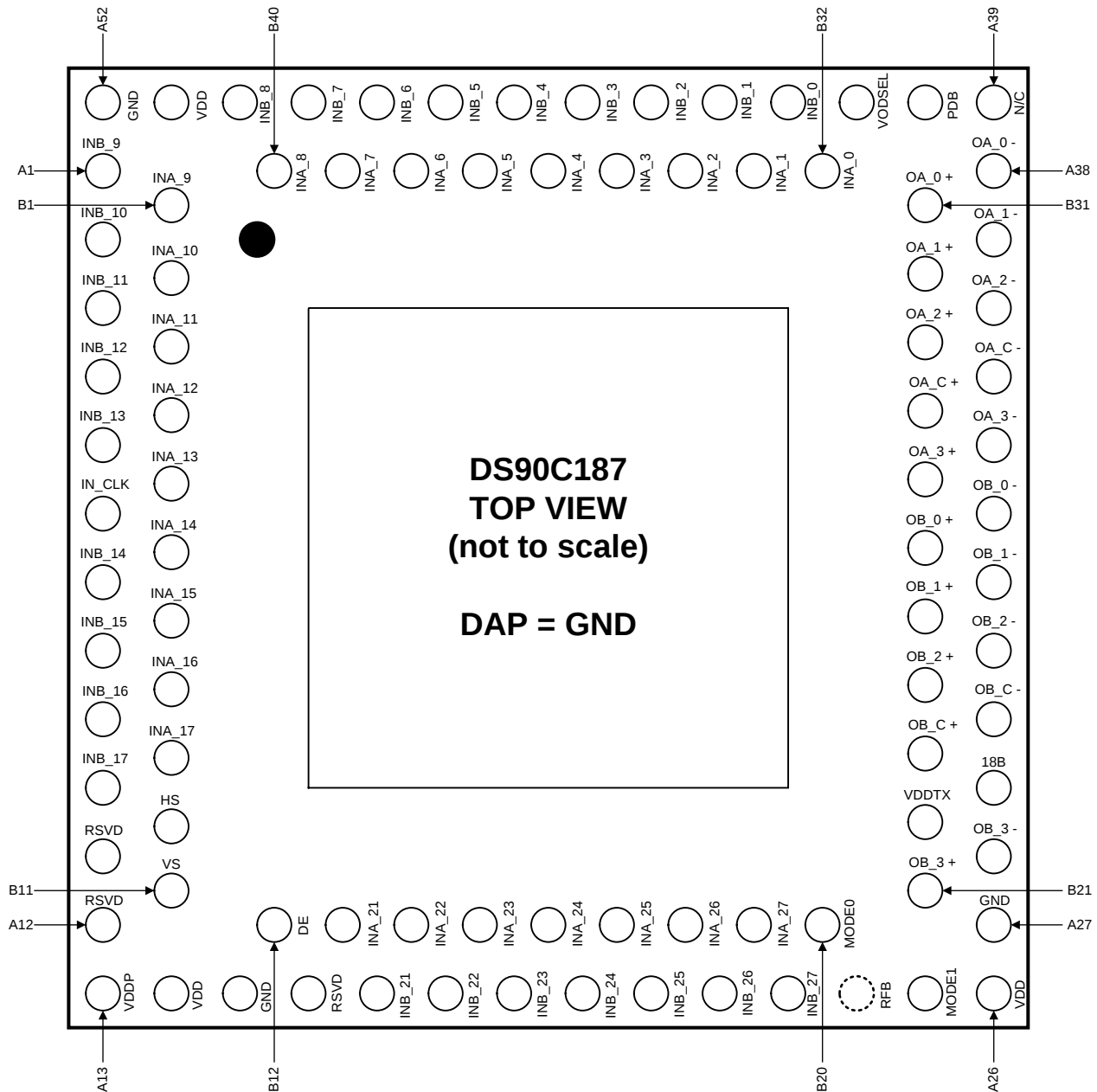
## 5 概要（続き）

デュアル・ピクセル・イン/デュアル・ピクセル・アウト・モードでは、60HzでQXGA 2048x1536、または30HzでQSXGA 2560x2048までのディスプレイを駆動できます。このモードでは、デバイスは2チャンネルの24ビットRGBデータを、2チャンネルの4D+C LVDSストリームに変換します。すべてのモードについて、デバイスは18bppおよび24bppカラーをサポートします。

DS90C187は、小型の92ピン2列VQFNパッケージで供給され、単一の1.8V電源で動作し、消費電力は最小限です。

## 6 Pin Configuration and Functions

**NLA Package  
92-Pin VQFN-MR  
Top View**



**DS90C187 Pin Descriptions — Serializer**

| NAME                                                   | PIN NO.                                  | I/O | DESCRIPTION                                                                                                                                               |
|--------------------------------------------------------|------------------------------------------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>1.8-V LVCMOS VIDEO INPUTS</b>                       |                                          |     |                                                                                                                                                           |
| INA_[27:21]<br>INA_[17:9]<br>NA_[8:0]                  | B19-B13,<br>B9-B1,<br>B40-B32            | I   | Channel A Data Inputs<br>Typically consists of 8 Red, 8 Green, 8 Blue and a general purpose or L/R control bit.<br>Includes pull down.                    |
| INB_[27:21]<br>INB_[17:14],<br>INB_[13:9]<br>INB_[8:0] | A23-A17,<br>A10-A7,<br>A5-A1,<br>A50-A42 | I   | Channel B Data Inputs<br>Typically consists of 8 Red, 8 Green, 8 Blue and a general purpose or L/R control bit.<br>Includes pull down.                    |
| HS (INA_18),<br>VS (INA_19),<br>DE (INA_20)            | B10,<br>B11,<br>B12                      | I   | Video Control Signal Inputs -<br>HS = Horizontal Sync, VS = Vertical SYNC, and DE = Data Enable                                                           |
| IN_CLK                                                 | A6                                       | I   | Pixel Input Clock<br>Includes pull down.                                                                                                                  |
| <b>1.8-V LVCMOS CONTROL INPUTS</b>                     |                                          |     |                                                                                                                                                           |
| MODE0,<br>MODE1                                        | B20,<br>A25                              | I   | Mode Control Input (MODE0)<br>00 = Single In / Single Out<br>01 = Single In / Dual Out<br>10 = Dual In / Dual Out<br>11 = Reserved<br>Includes pull down. |
| RFB                                                    | A24                                      | I   | Rising / Falling Clock Edge Select Input -<br>0 = Falling Edge, 1 = Rising Edge<br>Includes pull down.                                                    |
| PDB                                                    | A40                                      | I   | Power Down (Sleep) Control Input -<br>0 = Sleep (Power Down mode), 1 = device active (enabled)<br>Includes pull down.                                     |
| 18B                                                    | A29                                      | I   | 18 bit / 24 bit Control Input -<br>0 = 24 bit mode,<br>1 = 18 bit mode<br>Includes pull down.                                                             |
| VODSEL                                                 | A41                                      | I   | VOD Level Select Input -<br>0 = Low swing, 1 = Normal swing<br>Includes pull down.                                                                        |
| N/C                                                    | A39                                      | I   | <b>no connect pin — leave open</b>                                                                                                                        |
| RSVD                                                   | A11, A12, A16                            | I   | <b>Reserved - Tie to Ground.</b>                                                                                                                          |
| <b>LVDS OUTPUTS</b>                                    |                                          |     |                                                                                                                                                           |
| OA_C+<br>OA_C-                                         | B28,<br>A35                              | O   | Channel A LVDS Output Clock —<br>Expects 100 $\Omega$ DC load.                                                                                            |
| OA_[3:0]+,<br>OA_[3:0]-                                | B27, B29-B31<br>A34, A36-A38             | O   | Channel A LVDS Output Data —<br>Expects 100 $\Omega$ DC load.                                                                                             |
| OB_C+<br>OB_C-                                         | B23,<br>A30                              | O   | Channel B LVDS Output Clock —<br>Expects 100 $\Omega$ DC load.                                                                                            |
| OB_[3:0]+,<br>OB_[3:0]-                                | B21, B24-B26<br>A28, A16-A33             | O   | Channel B LVDS Output Data —<br>Expects 100 $\Omega$ DC load.                                                                                             |
| <b>POWER AND GROUND</b>                                |                                          |     |                                                                                                                                                           |
| V <sub>DDTX</sub>                                      | B22                                      | P   | Power supply for LVDS Drivers, 1.8V.                                                                                                                      |
| V <sub>DD</sub>                                        | A14, A26, A51                            | P   | Power supply pin for core, 1.8V.                                                                                                                          |
| V <sub>DDP</sub>                                       | A13                                      | P   | Power supply pin for PLL, 1.8V.                                                                                                                           |
| GND                                                    | A15, A27, A52                            | G   | Ground pins.                                                                                                                                              |
| DAP                                                    | DAP                                      | G   | <b>Connect DAP to Ground plane.</b>                                                                                                                       |

## 7 Specifications

### 7.1 Absolute Maximum Ratings

See <sup>(1)</sup>

|                                    | MIN        | MAX       | UNIT |
|------------------------------------|------------|-----------|------|
| Supply Voltage ( $V_{CC}$ )        | -0.3       | 2.5       | V    |
| LVCMOS Input Voltage               | -0.3       | VDD + 0.3 | V    |
| LVDS Driver Output Voltage         | -0.3       | 3.6       | V    |
| LVDS Output Short-Circuit Duration | Continuous |           |      |
| Junction Temperature               |            | 150       | °C   |
| Storage Temperature ( $T_{stg}$ )  | -65        | 150       | °C   |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 7.2 ESD Ratings

|                                     |                                                                                | VALUE | UNIT |
|-------------------------------------|--------------------------------------------------------------------------------|-------|------|
| $V_{(ESD)}$ Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>              | ±8000 | V    |
|                                     | Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup> | ±1250 |      |
|                                     | Machine model                                                                  | ±250  |      |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. **[Following sentence optional; see the wiki.]** Manufacturing with less than 500-V HBM is possible with the necessary precautions. **[Following sentence optional; see the wiki.]** Pins listed as ±XXX V may actually have higher performance.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. **[Following sentence optional; see the wiki.]** Manufacturing with less than 250-V CDM is possible with the necessary precautions. **[Following sentence optional; see the wiki.]** Pins listed as ±YYY V may actually have higher performance.

### 7.3 Recommended Operating Conditions

|                                          | MIN  | NOM  | MAX  | UNIT              |
|------------------------------------------|------|------|------|-------------------|
| Supply Voltage                           | 1.71 | 1.80 | 1.89 | V                 |
| Operating Free Air Temperature ( $T_A$ ) | -10  | +25  | +70  | °C                |
| Differential Load Impedance              | 80   | 100  | 120  | Ω                 |
| Supply Noise Voltage                     |      |      | <90  | mV <sub>p-p</sub> |

### 7.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |                                                       | DS90C187      | UNIT |
|-------------------------------|-------------------------------------------------------|---------------|------|
|                               |                                                       | NLA (VQFN-MR) |      |
|                               |                                                       | 92 PINS       |      |
| $R_{\theta JA}$               | Junction-to-ambient thermal resistance <sup>(2)</sup> | 35.1          | °C/W |
| $R_{\theta JC(top)}$          | Junction-to-case (top) thermal resistance             |               | °C/W |
| $R_{\theta JB}$               | Junction-to-board thermal resistance                  |               | °C/W |
| $\psi_{JT}$                   | Junction-to-top characterization parameter            |               | °C/W |
| $\psi_{JB}$                   | Junction-to-board characterization parameter          |               | °C/W |
| $R_{\theta JC(bot)}$          | Junction-to-case (bottom) thermal resistance          |               | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.
- (2) Above +22°C

### 7.5 Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

| PARAMETER                | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------------|-----------------|-----|-----|-----|------|
| LVCMOS DC SPECIFICATIONS |                 |     |     |     |      |

## Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

| PARAMETER                            |                                                              | TEST CONDITIONS                                                                                                      |                                                           | MIN          | TYP          | MAX          | UNIT                       |
|--------------------------------------|--------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------|--------------|--------------|--------------|----------------------------|
| $V_{IH}$                             | High Level Input Voltage                                     |                                                                                                                      |                                                           | $0.65V_{DD}$ |              | $V_{DD}$     | V                          |
| $V_{IL}$                             | Low Level Input Voltage                                      |                                                                                                                      |                                                           | GND          |              | $0.35V_{DD}$ | V                          |
| $I_{IN}$                             | Input Current                                                | $V_{IN} = 0V$ or $V_{DD} = 1.71V$ to $1.89V$                                                                         |                                                           | -10          | ±1           | +10          | μA                         |
| <b>LVDS DRIVER DC SPECIFICATIONS</b> |                                                              |                                                                                                                      |                                                           |              |              |              |                            |
| $V_{OD}$                             | Differential Output Voltage                                  | $R_L = 100\Omega$<br>ⓘ 3                                                                                             | $VODSEL = V_{IH}$                                         | 160<br>(320) | 300<br>(600) | 450<br>(900) | mV<br>(mV <sub>P-P</sub> ) |
|                                      |                                                              |                                                                                                                      | $VODSEL = V_{IL}$                                         | 110<br>(220) | 180<br>(360) | 300<br>(600) | mV<br>(mV <sub>P-P</sub> ) |
| $\Delta V_{OD}$                      | Change in $V_{OD}$ between Complimentary Output States       | $R_L = 100\Omega$<br>ⓘ 3                                                                                             |                                                           |              |              | 50           | mV                         |
| $V_{OS}$                             | Offset Voltage                                               | $R_L = 100\Omega$<br>ⓘ 3                                                                                             |                                                           | 0.8          | 0.9          | 1.0          | V                          |
| $\Delta V_{OS}$                      | Change in $V_{OS}$ between Complimentary Output States       | $R_L = 100\Omega$<br>ⓘ 3                                                                                             |                                                           |              |              | 50           | mV                         |
| $I_{OS}$                             | Output Short Circuit Current                                 | $V_{OUT} = GND$ , $VODSEL = V_{DD}$                                                                                  |                                                           | -45          | -35          | -25          | mA                         |
| <b>SUPPLY CURRENT</b>                |                                                              |                                                                                                                      |                                                           |              |              |              |                            |
| IDDT1                                | Serializer Worst Case Supply Current (includes load current) | Checkerboard pattern,<br>$R_L = 100\Omega$ ,<br>$18B = V_{IL}$ ,<br>$VODSEL = V_{IH}$ ,<br>$V_{DD} = 1.89V$ ,<br>ⓘ 1 | $f = 105\text{ MHz}$ ,<br>$MODE[1:0] = 00$ (SISO)         |              | 60           | 85           | mA                         |
| IDDT2                                |                                                              |                                                                                                                      | $f = 185\text{ MHz}$ ,<br>$MODE[1:0] = 01$ (SIDO)         |              | 95           | 140          | mA                         |
| IDDT3                                |                                                              |                                                                                                                      | $f = 105\text{ MHz}$ ,<br>$MODE[1:0] = 10$ (DIDO)         |              | 100          | 150          | mA                         |
| IDDTTP                               | Serializer Supply Current PRBS-7                             | $MODE[1:0] = 01$ (SIDO),<br>$f = 150\text{ MHz}$ ,<br>$R_L = 100\Omega$ ,<br>PRBS-7 Pattern<br>ⓘ 12                  | $18B = V_{IL}$ ,<br>$VODSEL = V_{IL}$ ,<br>$V_{DD} = 1.8$ |              | 55           |              | mA                         |
|                                      |                                                              |                                                                                                                      | $18B = V_{IL}$ ,<br>$VODSEL = V_{IH}$ ,<br>$V_{DD} = 1.8$ |              | 75           |              | mA                         |
|                                      |                                                              |                                                                                                                      | $18B = V_{IH}$ ,<br>$VODSEL = V_{IL}$ ,<br>$V_{DD} = 1.8$ |              | 49           |              | mA                         |
|                                      |                                                              |                                                                                                                      | $18B = V_{IH}$ ,<br>$VODSEL = V_{IH}$ ,<br>$V_{DD} = 1.8$ |              | 65           |              | mA                         |
| IDDTG                                | Serializer Supply Current 16 Grayscale                       | $MODE[1:0] = 01$ (SIDO),<br>$f = 150\text{ MHz}$ ,<br>$R_L = 100\Omega$ ,<br>16 Grayscale Pattern                    | $18B = V_{IL}$ ,<br>$VODSEL = V_{IL}$ ,<br>$V_{DD} = 1.8$ |              | 53           |              | mA                         |
|                                      |                                                              |                                                                                                                      | $18B = V_{IL}$ ,<br>$VODSEL = V_{IH}$ ,<br>$V_{DD} = 1.8$ |              | 71           |              | mA                         |
|                                      |                                                              |                                                                                                                      | $18B = V_{IH}$ ,<br>$VODSEL = V_{IL}$ ,<br>$V_{DD} = 1.8$ |              | 48           |              | mA                         |
|                                      |                                                              |                                                                                                                      | $18B = V_{IH}$ ,<br>$VODSEL = V_{IH}$ ,<br>$V_{DD} = 1.8$ |              | 63           |              | mA                         |
| IDDZ                                 | Power Down Supply Current                                    | $PDB = GND$                                                                                                          |                                                           |              | 18           | 200          | μA                         |

## 7.6 Recommended Input Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

| PARAMETER |                                               |                         | MIN   | TYP  | MAX   | UNIT |
|-----------|-----------------------------------------------|-------------------------|-------|------|-------|------|
| TCIT      | IN_CLK Transition Time<br><a href="#">§ 5</a> | MODE[1:0] = 00 or 10    | 1     | T    | 4     | ns   |
|           |                                               | MODE[1:0] = 01          | 1     |      | 2     | ns   |
| TCIP      | IN_CLK Period<br><a href="#">§ 6</a>          | MODE[1:0] = 00 or 10    | 9.53  | T    | 40    | ns   |
|           |                                               | MODE[1:0] = 01          | 5.40  | T    | 20    | ns   |
| TCIH      | IN_CLK High Time                              | See <a href="#">§ 6</a> | 0.35T | 0.5T | 0.65T | ns   |
| TCIL      | IN_CLK Low Time                               | See <a href="#">§ 6</a> | 0.35T | 0.5T | 0.65T | ns   |
| TXIT      | INA_x & INB_x Transition Time                 | See <a href="#">§ 5</a> | 1.5   |      | 0.3T  | ns   |

## 7.7 Switching Characteristics

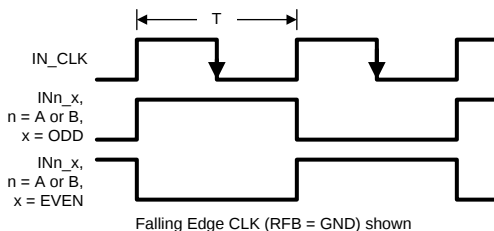
Over recommended operating supply and temperature ranges unless otherwise specified.

| PARAMETER |                                                                        |                                                                        | MIN | TYP               | MAX               | UNIT |
|-----------|------------------------------------------------------------------------|------------------------------------------------------------------------|-----|-------------------|-------------------|------|
| TSTC      | INn_x Setup to IN_CLK                                                  | See <a href="#">§ 6</a>                                                | 0   |                   |                   | ns   |
| THTC      | INn_x Hold from IN_CLK                                                 | See <a href="#">§ 6</a>                                                | 2.5 |                   |                   | ns   |
| LLHT      | LVDS Low-to-High Transition Time<br><a href="#">§ 4</a> <sup>(1)</sup> |                                                                        |     | 0.18              | 0.5               | ns   |
| LHLT      | LVDS High-to-Low Transition Time<br><a href="#">§ 4</a> <sup>(1)</sup> |                                                                        |     | 0.18              | 0.5               | ns   |
| TBIT      | LVDS Output Bit Width                                                  | MODE[1:0] = 00, or 10                                                  |     | 1/7 TCIP          |                   | ns   |
|           |                                                                        | MODE[1:0] = 01                                                         |     | 2/7 TCIP          |                   | ns   |
| TPPOS0    | Transmitter Output Pulse Positions Normalized for Bit 0                | See <a href="#">§ 9</a>                                                |     | 1                 |                   | UI   |
| TPPOS1    | Transmitter Output Pulse Positions Normalized for Bit 1                | See <a href="#">§ 9</a>                                                |     | 2                 |                   | UI   |
| TPPOS2    | Transmitter Output Pulse Positions Normalized for Bit 2                | See <a href="#">§ 9</a>                                                |     | 3                 |                   | UI   |
| TPPOS3    | Transmitter Output Pulse Positions Normalized for Bit 3                | See <a href="#">§ 9</a>                                                |     | 4                 |                   | UI   |
| TPPOS4    | Transmitter Output Pulse Positions Normalized for Bit 4                | See <a href="#">§ 9</a>                                                |     | 5                 |                   | UI   |
| TPPOS5    | Transmitter Output Pulse Positions Normalized for Bit 5                | See <a href="#">§ 9</a>                                                |     | 6                 |                   | UI   |
| TPPOS6    | Transmitter Output Pulse Positions Normalized for Bit 6                | See <a href="#">§ 9</a>                                                |     | 7                 |                   | UI   |
| ΔTPPOS    | Variation in Transmitter Pulse Position (Bit 6 — Bit 0)                | See <a href="#">§ 9</a>                                                |     | ±0.06             |                   | UI   |
| TCCS      | LVDS Channel to Channel Skew                                           |                                                                        |     | 110               |                   | ps   |
| TJCC      | Jitter Cycle-to-Cycle                                                  | MODE0, MODE1 = 0,<br>f = 105 MHz,<br><sup>(1)</sup>                    |     | 0.028             | 0.035             | UI   |
| TPLLS     | Phase Lock Loop Set (Enable Time)                                      | <a href="#">§ 7</a>                                                    |     |                   | 1                 | ms   |
| TPDD      | Powerdown Delay                                                        | <a href="#">§ 8</a><br><sup>(2)</sup>                                  |     |                   | 100               | ns   |
| TSD       | Latency Delay                                                          | MODE0 = 0,<br>MODE1 = 1 or 0<br><a href="#">§ 10</a><br><sup>(1)</sup> |     | 2*TCIP +<br>10.54 | 2*TCIP +<br>13.96 | ns   |
| TLAT      | Latency Delay for Single Pixel In / Dual Pixel Out Mode                | MODE0 = 1,<br>MODE1 = 0<br><a href="#">§ 10</a><br><sup>(1)</sup>      |     | 9*TCIP +<br>4.19  | 9*TCIP +<br>6.36  | ns   |

(1) Parameter is ensured by characterization and is not tested at final test.

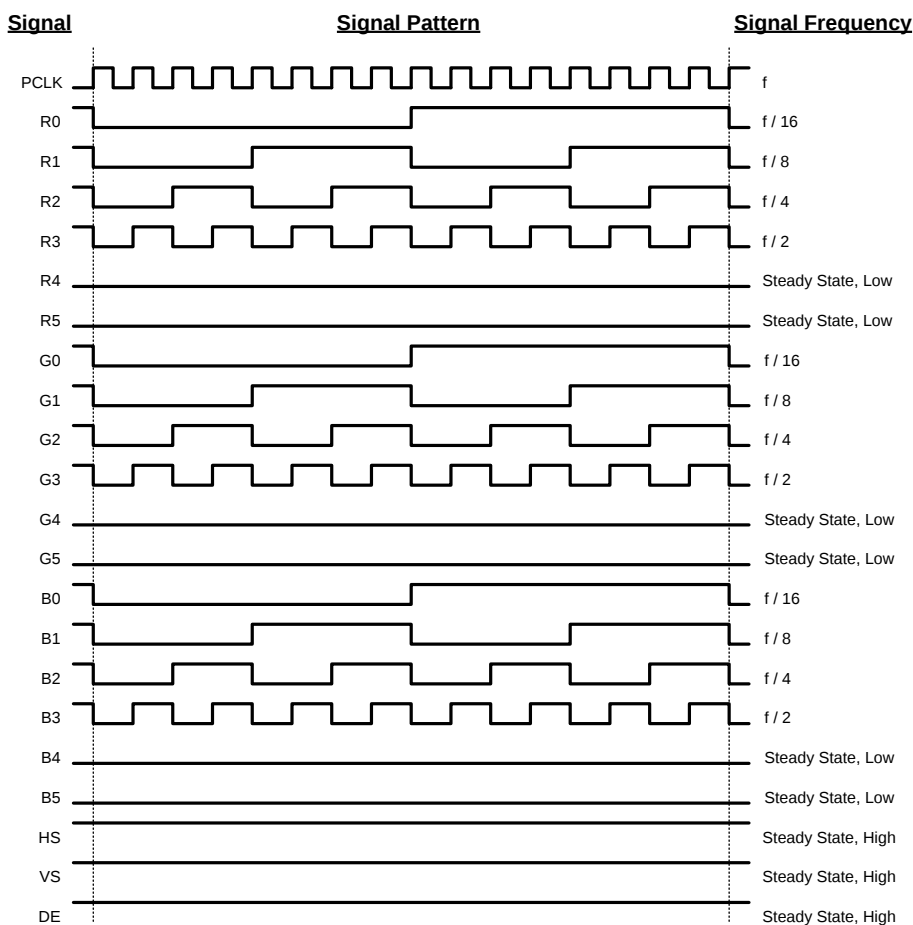
(2) Parameter is ensured by design and is not tested at final test.

## 7.8 AC Timing Diagrams



- A. The worst case test pattern produces a maximum toggling of digital circuits, LVDS I/O and LVCMOS/ I/O.
- B. [Figure 1](#) and [Figure 2](#) show a falling edge data strobe (IN\_CLK).

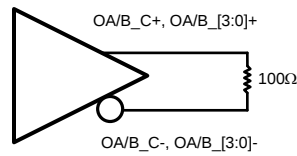
**Figure 1. Checker Board Test Pattern**



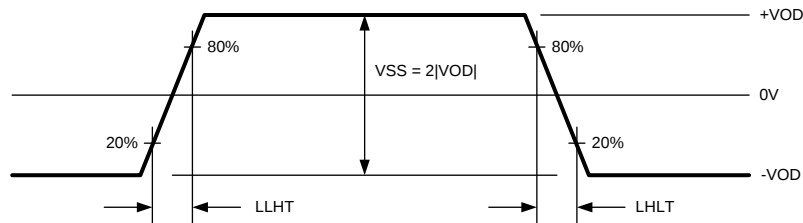
- A. The worst case test pattern produces a maximum toggling of digital circuits, LVDS I/O and LVCMOS/ I/O.
- B. Recommended pin to signal mapping for 18 bits per pixel, customer may choose to define differently. The 16 grayscale test pattern tests device power consumption for a "typical" LCD display pattern. The test pattern approximates signal switching needed to produce groups of 16 vertical stripes across the display.
- C. [Figure 2](#) shows a falling edge data strobe (IN\_CLK).

**Figure 2. "16 Gray Scale" Test Pattern (Falling Edge Clock shown)**

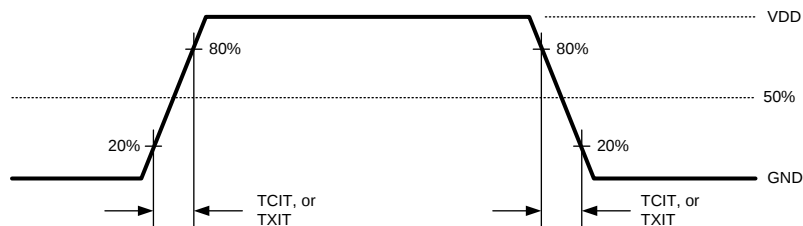
## AC Timing Diagrams (continued)



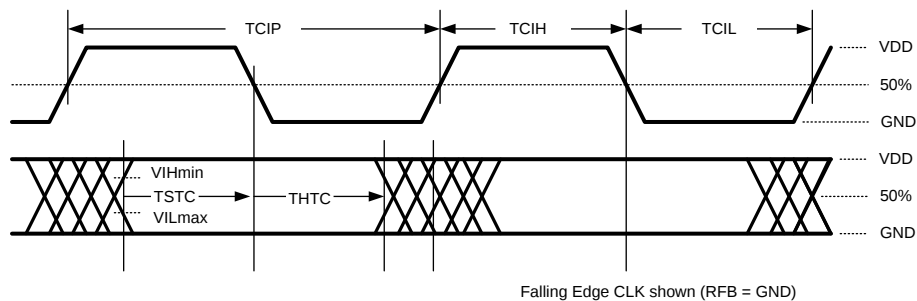
**图 3. DS90C187 (Transmitter) LVDS Output Load**



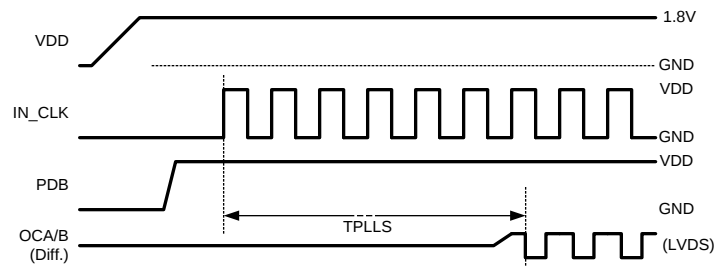
**图 4. LVDS Output Transition Times**



**图 5. LVC MOS Input Transition Times**

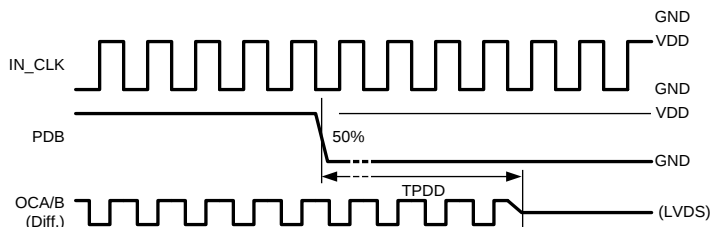


**图 6. LVC MOS Input Setup/Hold and Clock High/Low Times (Falling Edge Strobe)**

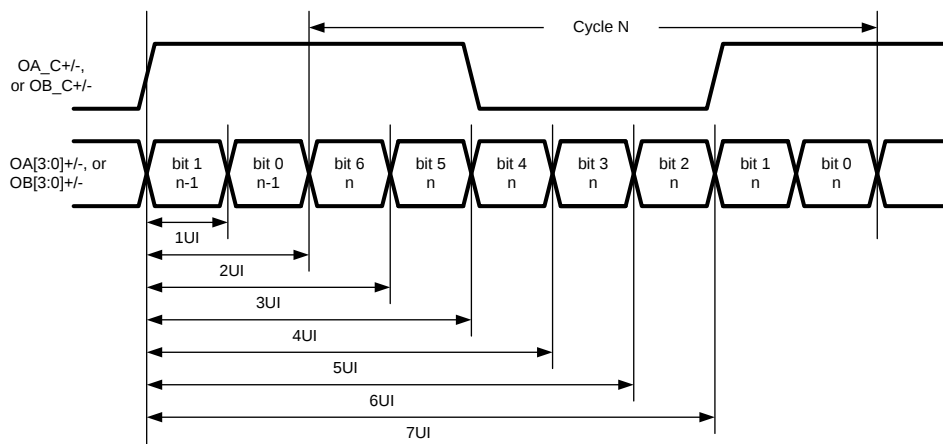


**图 7. Start Up / Phase Lock Loop Set Time**

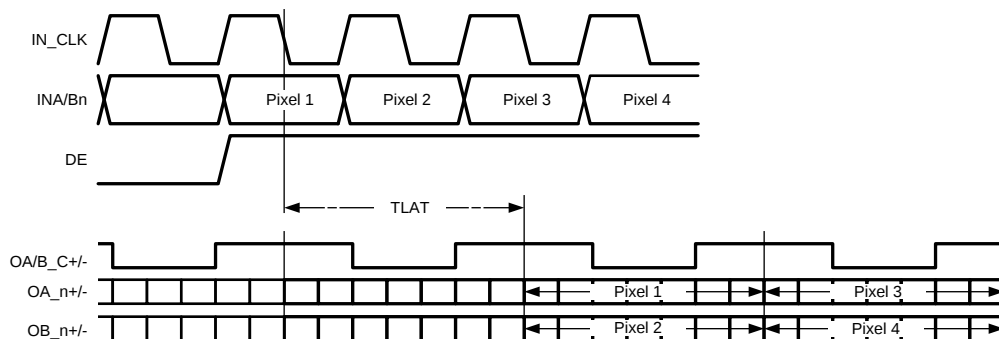
## AC Timing Diagrams (continued)



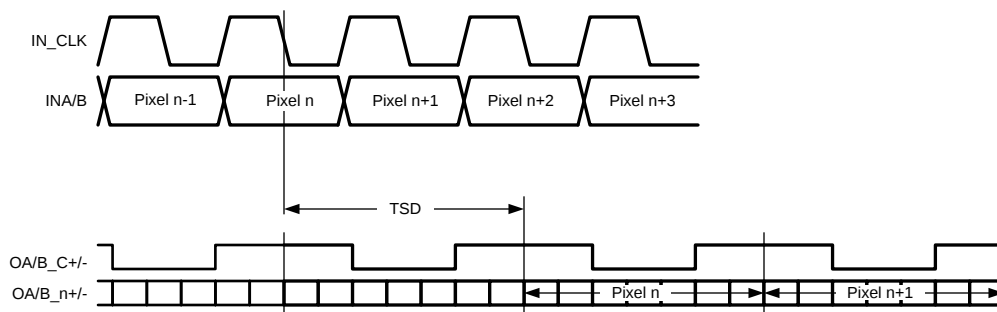
**Figure 8. Sleep Mode / Power Down Delay**



**Figure 9. LVDS Serial Bit Positions**



**Figure 10. Single In Dual Out Mode Timing and Latency**



**Figure 11. Single In Single Out / Dual In Dual Out Latency**

## 7.9 Typical Characteristics

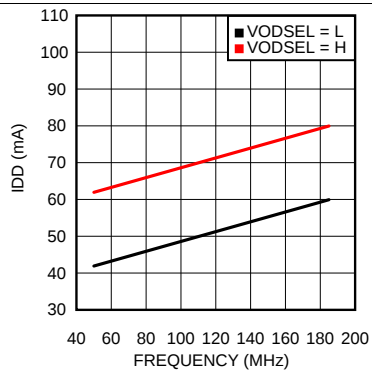


图 12. Typ Current Draw — Single In/Dual Out Mode — PRBS-7 Data Pattern

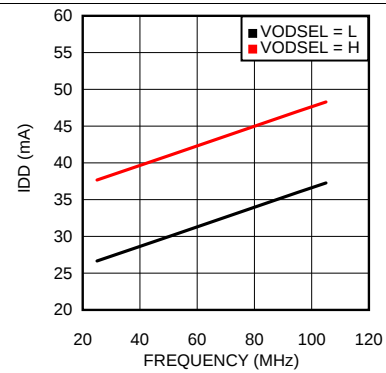


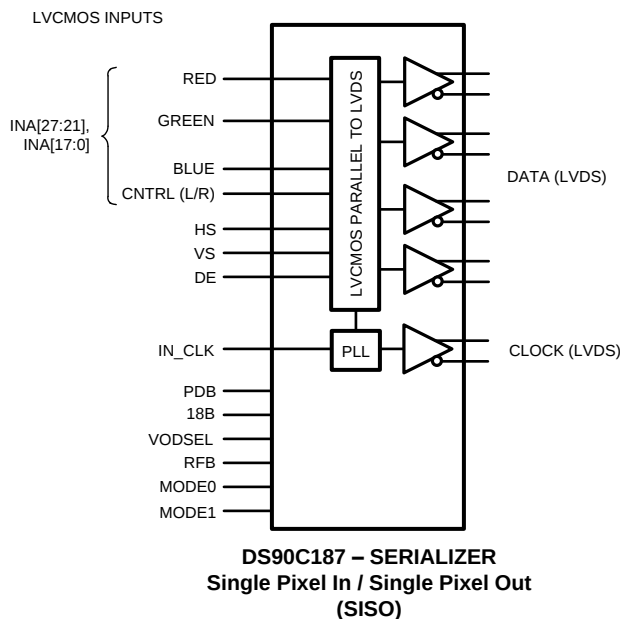
图 13. Typ Current Draw — Single In/Single Out Mode — PRBS-7 Data Pattern

## 8 Detailed Description

### 8.1 Overview

DS90C187 converts a wide parallel LVCMOS input bus into banks of FPD-Link LVDS data. The device can be configured to support RGB-888 (24-bit color) or RGB-666 (18 bit color) in three main configurations: single pixel in / single pixel out; single pixel in / dual pixel out; dual pixel in / dual pixel out. The DS90C187 has several power saving features including: selectable VOD, 18 bit / 24 bit mode select, and a power down pin control.

### 8.2 Functional Block Diagrams

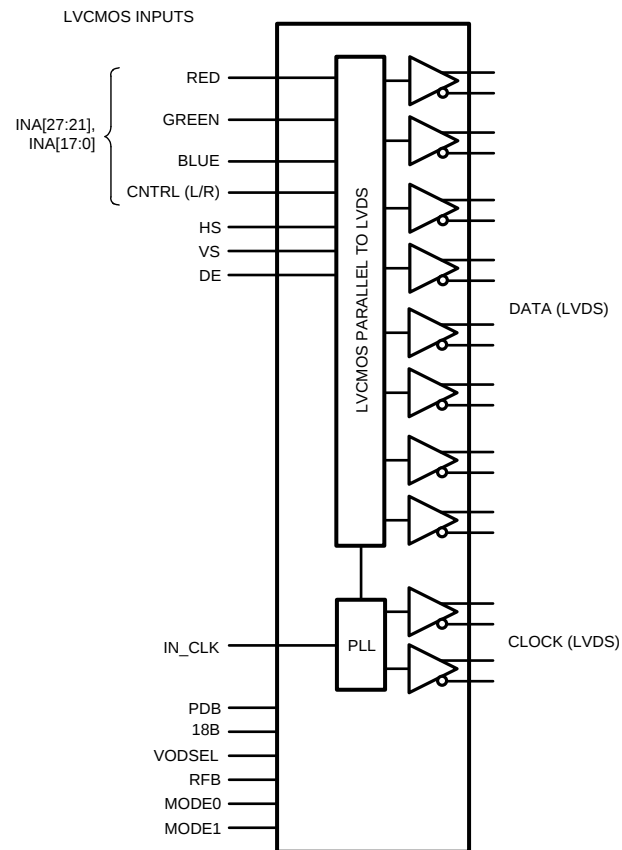


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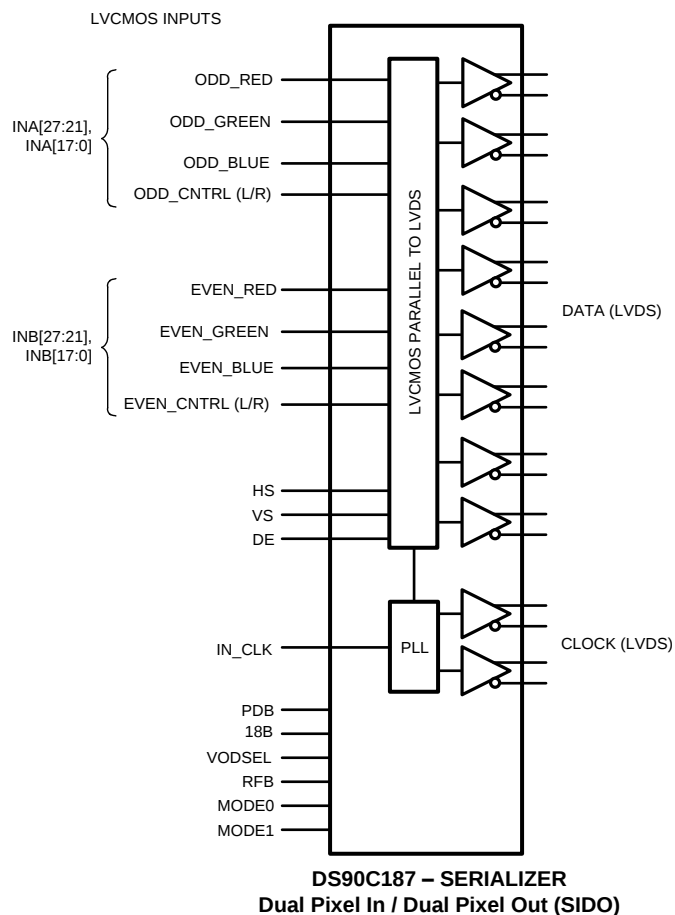
[www.tij.co.jp](http://www.tij.co.jp)

### Functional Block Diagrams (continued)



**DS90C187 – SERIALIZER**  
**Single Pixel In / Dual Pixel Out (SIDO)**

## Functional Block Diagrams (continued)



## 8.3 Device Functional Modes

### 8.3.1 Device Configuration

The MODE0 and MODE1 pins are used to configure the DS90C187 into the three main operation modes as shown in the table below.

**表 1. Mode Configurations**

| MODE1 | MODE0 | CONFIGURATION                                  |
|-------|-------|------------------------------------------------|
| 0     | 0     | Single Pixel Input, Single Pixel Output (SISO) |
| 0     | 1     | Single Pixel Input, Dual Pixel Output (SIDO)   |
| 1     | 0     | Dual Pixel Input, Dual Pixel Output (DIDO)     |
| 1     | 1     | RESERVED                                       |

### 8.3.2 Single Pixel Input / Single Pixel Output

When MODE0 and MODE1 are both set to low, data from INA\_[27:0], HS, VS and DE is serialized and driven out on OA\_[3:0]+/- with OA\_C+/- . If 18B\_MODE is LOW, then OA\_3+/- is powered down and the corresponding LVCMOS input signals are ignored.

In this configuration IN\_CLK can range from 25 MHz to 105 MHz, resulting in a total maximum payload of 700 Mbps (28 bits \* 25MHz) to 2.94 Gbps (28 bits \* 105 MHz). Each LVDS driver will operate at a speed of 7 bits per input clock cycle, resulting in a serial line rate of 175 Mbps to 735 Mbps. OA\_C+/- will operate at the same rate as IN\_CLK with a duty cycle ratio of 57:43.

### 8.3.3 Single Pixel Input / Dual Pixel Output

When MODE0 is HIGH and MODE1 is LOW, data from INA\_[27:0], HS, VS and DE is serialized and driven out on OA\_[3:0]+/- and OB\_[3:0]+/- with OA\_C+/- and OB\_C+/- . If 18B\_MODE is LOW, then OA\_3+/- and OB\_3+/- are powered down and the corresponding LVCMOS input signals are ignored. The input LVCMOS data is split into odd and even pixels starting with the odd (first) pixel outputs OA\_[3:0]+/- and then the even (second) pixel outputs OB\_[3:0]+/- . The splitting of the data signals starts with DE (data enable) transitioning from logic LOW to HIGH indicating active data (see [Figure 10](#)). **The number of clock cycles during blanking must be an EVEN number.** This configuration will allow the user to interface with two FPD-Link receivers or other dual pixel inputs.

In this configuration IN\_CLK can range from 50 MHz to 185 MHz, resulting in a total maximum payload of 1.4 Gbps (28 bits \* 50 MHz) to 5.18 Gbps (28 bits \* 185 MHz). Each LVDS driver will operate at a speed of 7 bits per 2 input clock cycles, resulting in a serial line rate of 175 Mbps to 647.5 Mbps. OA\_C+/- and OA\_B+/- will operate at ½ the rate as IN\_CLK with a duty cycle ratio of 57:43.

1. Disable the clock and data.
2. Toggle PDB to Low and then High.
3. After PDB settles reset the data pattern and enable the clock and data.

### 8.3.4 Dual Pixel Input / Dual Pixel Output

When MODE0 is LOW and MODE1 is set to HIGH, data from INA\_[27:0], HS, VS and DE is serialized and driven out on OA\_[3:0]+/- with OA\_C+/- , while data from INB\_[27:0], HS, VS and DE is serializer and driven out on OB\_[3:0]+/- with OB\_C+/- . If 18B\_MODE is LOW, then OA\_3+/- and OB\_3+/- is powered down and the corresponding LVCMOS input signals are ignored.

In this configuration IN\_CLK can range from 25 MHz to 105 MHz, resulting in a total maximum payload of 1.325 Gbps (53 bits \* 25 MHz) to 5.565 Gbps (53 bits \* 105 MHz). Each LVDS driver will operate at a speed of 7 bits per input clock cycle, resulting in a serial line rate of 175 Mbps to 735 Mbps. OA\_C+/- and OB\_C+/- will operate at the same rate as IN\_CLK with a duty cycle ratio of 57:43.

### 8.3.5 Pixel Clock Edge Select (RFB)

The RFB pin determines the edge that the input LVCMOS data is latched on. If RFB is HIGH, input data is latched on the RISING EDGE of the pixel clock (IN\_CLK). If RFB is LOW, the input data is latched on the FALLING EDGE of the pixel clock. Note: This can be set independently of receiver's output clock strobe.

**表 2. Pixel Clock Edge**

| RFB | Result       |
|-----|--------------|
| 0   | FALLING edge |
| 1   | RISING edge  |

### 8.3.6 Power Management

The DS90C187 has several features to assist with managing power consumption. The device can be configured through the MODE0 and MODE1 control pins to enable only the required number of LVDS drivers for each application. The 18B\_MODE pin allows the DS90C187 to power down the unused LVDS driver(s) for RGB-666 (18 bit color) applications for an additional level of power management. If no clock is applied to the IN\_CLK pin, the DS90C187 will enter a low power state. To place the DS90C187 in its lowest power state, the device can be powered down by driving the PDB pin to LOW.

### 8.3.7 Sleep Mode (PDB)

The DS90C187 provides a power down feature. When the device has been powered down, current draw through the supply pins is minimized and the PLL is shut down. The LVDS drivers are also powered down with their outputs pulled to GND through 100-Ω resistors (not tri-stated).

**表 3. Power Down Select**

| PDB | Result               |
|-----|----------------------|
| 0   | SLEEP Mode (default) |
| 1   | ACTIVE (enabled)     |

### 8.3.8 LVDS Outputs

The DS90C187's LVDS drivers are compatible with ANSI/TIA/EIA-644-A LVDS receivers. The LVDS drivers can output a power saving low  $V_{OD}$ , or a high  $V_{OD}$  to enable longer trace and cable lengths by configuring the VODSEL pin.

**表 4. VOD Select**

| VODSEL | Result             |
|--------|--------------------|
| 0      | ±220 mV (440 mVpp) |
| 1      | ±340 mV (680 mVpp) |

Any unused LVDS outputs that are not powered down or put into TRI-STATE® due to the MODE0, MODE1, or 18B pins should be externally terminated differentially with a 100 ohm resistor. For example, when driving a timing controller (TCON) that only requires an 8D + C LVDS interface, rather than 8D + 2C, the unused clock line should be terminated near the package of the DS90C187. For more information regarding the output state of unused LVDS drivers, refer to the next section, 18 bit / 24 bit Color Mode (18B). For more information regarding the electrical characteristics of the LVDS outputs, refer to the LVDS DC Characteristics and LVDS Switching Specifications.

### 8.3.9 18 bit / 24 bit Color Mode (18B)

The 18B pin can be used to further save power by powering down the 4th LVDS driver in each used bank when the application requires only 18 bit color or 3D+C LVDS. Set the 18B pin to logic HIGH to TRI-STATE® OA\_3+/- and OB\_3+/- (if the device is configured for dual pixel output). For 24 bit color applications this pin should be set to logic LOW. Note that the power down function takes priority over the TRI-STATE® function. So if the device is configured for 18 bit color Single Pixel In/Single Pixel Out, LVDS channel OB\_3+/- will be powered down and not TRI-STATE®. If an LVDS driver is powered down, each output terminal is pulled low by a 100 ohm resistor to ground.

**表 5. Color DepthConfigurations**

| 18B | Result                    |
|-----|---------------------------|
| 0   | 24bpp, LVDS 4D+C or 8D+2C |
| 1   | 18bpp, LVDS 3D+C or 6D+2C |

### 8.3.10 LVCMOS Inputs

The DS90C187 has two banks of 24 data inputs, one set of video control signal (HS, VS and DE) inputs and several device configuration LVCMOS pins. All LVCMOS input pins are designed for 1.8 V LVCMOS logic. All LVCMOS inputs, including clock, data and configuration pins, have an internal pull down resistor to set a default state. If any inputs are unused, they can be left as no connect (NC) or connected to ground.

## 8.4 Programming

### 8.4.1 LVDS Interface / TFT Color Data Recommended Mapping

Different color mapping options exist. Check with the color mapping of the Deserializer / TCON device that is used to ensure compatible mapping for the application. The DS90C187 supports three modes of operation for single and dual pixel applications supporting either 24bpp or 18bpp color depths.

## Programming (continued)

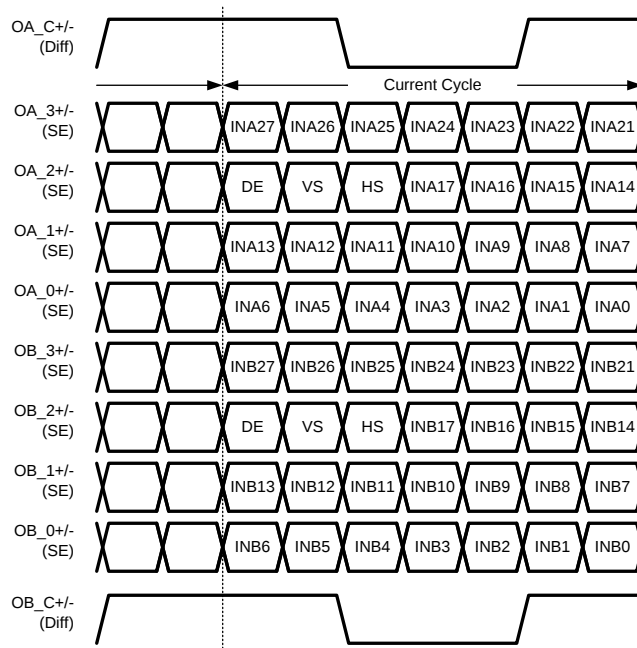
In the Dual Pixel / 24bpp mode, eight LVDS data lines are provided along with two LVDS clock lines (8D+2C). The Deserializer may utilize one or two clock lines. The 53 bit interface typically assigns 24 bits to RGB for the odd pixel, 24 bits to RGB for the even pixel, 3 bits for the video control signals (HS, VS and DE), 1 bit for odd pixel and 1 bit for even pixel which can be ignored or used for general purpose data, control or L/R signaling.

A reduced width input interface is also supported with a Single-to-Dual Pixel conversion where the data is presented at double rate (same clock edge, 2X speed, see ) and the DE transition is used to flag the first pixel. Also note in both 8D+2C configurations, the three video control signals are sent over **both** the A and B outputs. The DES / TCON may recover one set, or both depending upon its implementation. The Dual Pixel / 24bpp 8D+2C LVDS Interface Mapping is shown in .

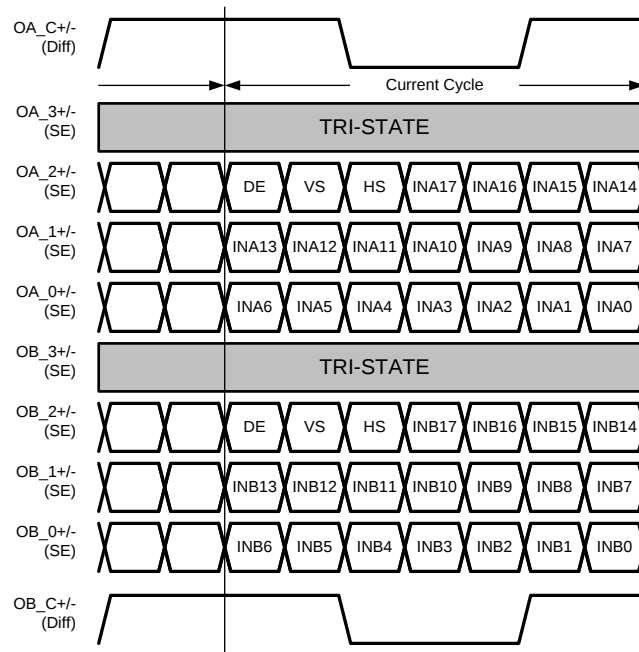
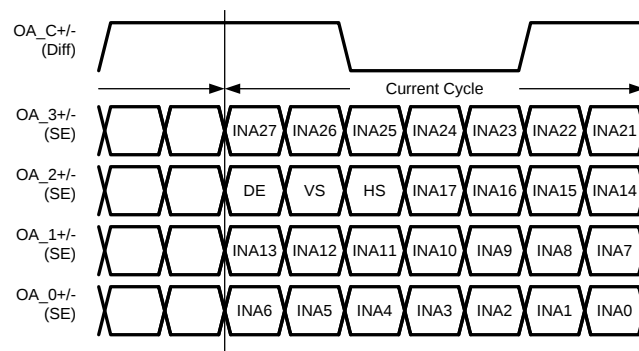
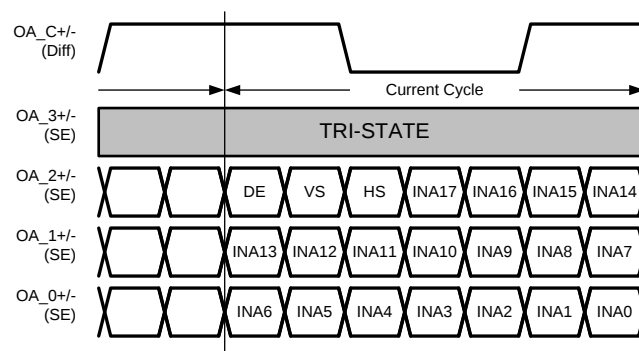
A Dual Pixel / 18bpp mode is also supported. In this configuration OA3 and OB3 LVDS output channels are placed in TRI-STATE® to save power. Their respective inputs are ignored. ( [15](#) )

In the Single Pixel / 24bpp mode, four LVDS data lines are provided along with a LVDS clock line (4D+C). The 28 bit interface typically assigns 24 bits to RGB color data, 3 bits to video control (HS, VS and DE) and one spare bit can be ignored, used for L/R signaling or function as a general purpose bit. The Single Pixel / 24bpp 4D+C LVDS Interface Mapping is shown in .

A Single Pixel / 18bpp mode is also supported. In this configuration the OA3 LVDS output channel is placed in TRI-STATE® to save power. Its respective inputs are ignored. ( [17](#) )



**14. Dual Pixel / 24bpp LVDS Mapping**

**Programming (continued)**

**15. Dual Pixel / 18bpp LVDS Mapping**

**16. Single Pixel / 24bpp LVDS Mapping**

**17. Single Pixel / 18bpp LVDS Mapping**

## Programming (continued)

### 8.4.1.1 Color Mapping Information

A defacto color mapping is shown next. Different color mapping options exist. Check with the color mapping of the Deserializer / TCON device that is used to ensure compatible mapping for the application.

**表 6. Single Pixel Input / 24bpp / MSB on CH3**

| DS90C187 Input | Color Mapping | Note            |
|----------------|---------------|-----------------|
| INA_22         | R7            | MSB             |
| INA_21         | R6            |                 |
| INA_5          | R5            |                 |
| INA_4          | R4            |                 |
| INA_3          | R3            |                 |
| INA_2          | R2            |                 |
| INA_1          | R1            |                 |
| INA_0          | R0            | LSB             |
| INA_24         | G7            | MSB             |
| INA_23         | G6            |                 |
| INA_11         | G5            |                 |
| INA_10         | G4            |                 |
| INA_9          | G3            |                 |
| INA_8          | G2            |                 |
| INA_7          | G1            |                 |
| INA_6          | G0            | LSB             |
| INA_26         | B7            | MSB             |
| INA_25         | B6            |                 |
| INA_17         | B5            |                 |
| INA_16         | B4            |                 |
| INA_15         | B3            |                 |
| INA_14         | B2            |                 |
| INA_13         | B1            |                 |
| INA_12         | B0            |                 |
| DE             | DE            | Data Enable*    |
| VS             | VS            | Vertical Sync   |
| HS             | HS            | Horizontal Sync |
| INA_27         | GP            | General Purpose |

**表 7. Single Pixel Input / 24bpp / LSB on CH3**

| DS90C187 Input | Color Mapping | Note |
|----------------|---------------|------|
| INA_5          | R7            | MSB  |
| INA_4          | R6            |      |
| INA_3          | R5            |      |
| INA_2          | R4            |      |
| INA_1          | R3            |      |
| INA_0          | R2            |      |
| INA_22         | R1            |      |
| INA_21         | R0            | LSB  |
| INA_11         | G7            | MSB  |
| INA_10         | G6            |      |
| INA_9          | G5            |      |

**表 7. Single Pixel Input / 24bpp / LSB on CH3 (continued)**

| DS90C187 Input | Color Mapping | Note            |
|----------------|---------------|-----------------|
| INA_8          | G4            |                 |
| INA_7          | G3            |                 |
| INA_6          | G2            |                 |
| INA_24         | G1            |                 |
| INA_23         | G0            | LSB             |
| INA_17         | B7            | MSB             |
| INA_16         | B6            |                 |
| INA_15         | B5            |                 |
| INA_14         | B4            |                 |
| INA_13         | B3            |                 |
| INA_12         | B2            |                 |
| INA_26         | B1            |                 |
| INA_25         | B0            |                 |
| DE             | DE            | Data Enable*    |
| VS             | VS            | Vertical Sync   |
| HS             | HS            | Horizontal Sync |
| INA_27         | GP            | General Purpose |

**表 8. Single Pixel Input / 18bpp**

| DS90C187 Input | Color Mapping | Note            |
|----------------|---------------|-----------------|
| INA_5          | R5            | MSB             |
| INA_4          | R4            |                 |
| INA_3          | R3            |                 |
| INA_2          | R2            |                 |
| INA_1          | R1            |                 |
| INA_0          | R0            | LSB             |
| INA_11         | G5            | MSB             |
| INA_10         | G4            |                 |
| INA_9          | G3            |                 |
| INA_8          | G2            |                 |
| INA_7          | G1            |                 |
| INA_6          | G0            | LSB             |
| INA_17         | B5            | MSB             |
| INA_16         | B4            |                 |
| INA_15         | B3            |                 |
| INA_14         | B2            |                 |
| INA_13         | B1            |                 |
| INA_12         | B0            |                 |
| DE             | DE            | Data Enable*    |
| VS             | VS            | Vertical Sync   |
| HS             | HS            | Horizontal Sync |

**表 9. Dual Pixel Input / 24bpp**

| DS90C187 Input | Color Mapping | Note |
|----------------|---------------|------|
| INA_22         | O_R7          | MSB  |
| INA_21         | O_R6          |      |

**表 9. Dual Pixel Input / 24bpp (continued)**

| DS90C187 Input | Color Mapping | Note         |
|----------------|---------------|--------------|
| INA_5          | O_R5          |              |
| INA_4          | O_R4          |              |
| INA_3          | O_R3          |              |
| INA_2          | O_R2          |              |
| INA_1          | O_R1          |              |
| INA_0          | O_R0          | LSB          |
| INA_24         | O_G7          | MSB          |
| INA_23         | O_G6          |              |
| INA_11         | O_G5          |              |
| INA_10         | O_G4          |              |
| INA_9          | O_G3          |              |
| INA_8          | O_G2          |              |
| INA_7          | O_G1          |              |
| INA_6          | O_G0          | LSB          |
| INA_26         | O_B7          | MSB          |
| INA_25         | O_B6          |              |
| INA_17         | O_B5          |              |
| INA_16         | O_B4          |              |
| INA_15         | O_B3          |              |
| INA_14         | O_B2          |              |
| INA_13         | O_B1          |              |
| INA_12         | O_B0          |              |
| INB_22         | E_R7          |              |
| INB_21         | E_R6          |              |
| INB_5          | E_R5          |              |
| INB_4          | E_R4          |              |
| INB_3          | E_R3          |              |
| INB_2          | E_R2          |              |
| INB_1          | E_R1          |              |
| INB_0          | E_R0          |              |
| INB_24         | E_G7          |              |
| INB_23         | E_G6          |              |
| INB_11         | E_G5          |              |
| INB_10         | E_G4          |              |
| INB_9          | E_G3          |              |
| INB_8          | E_G2          |              |
| INB_7          | E_G1          |              |
| INB_6          | E_G0          |              |
| INB_26         | E_B7          |              |
| INB_25         | E_B6          |              |
| INB_17         | E_B5          |              |
| INB_16         | E_B4          |              |
| INB_15         | E_B3          |              |
| INB_14         | E_B2          |              |
| INB_13         | E_B1          |              |
| INB_12         | E_B0          |              |
| DE             | DE            | Data Enable* |

表 9. Dual Pixel Input / 24bpp (continued)

| DS90C187 Input | Color Mapping | Note            |
|----------------|---------------|-----------------|
| VS             | VS            | Vertical Sync   |
| HS             | HS            | Horizontal Sync |
| INA_27         | GP            | General Purpose |
| INB_27         | GP            | General Purpose |

## 9 Application and Implementation

### 注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The DS90C187 is a Low Power Bridge for automotive application that reduces the size of the RGB interface between the host GPU and the Display. It is designed to support single pixel data transmission between Host and Flat Panel Display up to QXGA (2048x1536) at 60 Hz resolutions. The transmitter converts up to 24 bits (Single Pixel 24 bit color) of 1.8-V LVCMOS data into two channels of 4 data + clock (4D+C) reduced width interface LVDS compatible data streams.

### 9.2 Typical Application

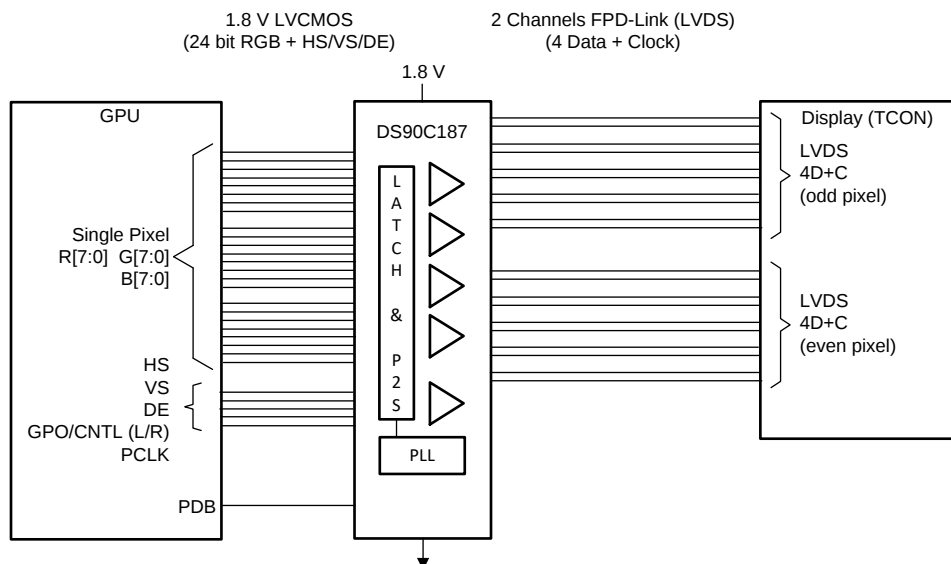


图 18. Single Pixel In Dual Pixel Out (SIDO) Mode

#### 9.2.1 Design Requirements

The DS90C187 is used to convert 24-bit color to two channels of LVDS datastreams.

表 10. Design Parameters

| DESIGN PARAMETER | VALUE         |
|------------------|---------------|
| Supply           | 1.8V          |
| Display Driven   | SXGA+, WUXGA+ |
| Pixel Depth      | 24 bits       |

## 9.2.2 Detailed Design Procedure

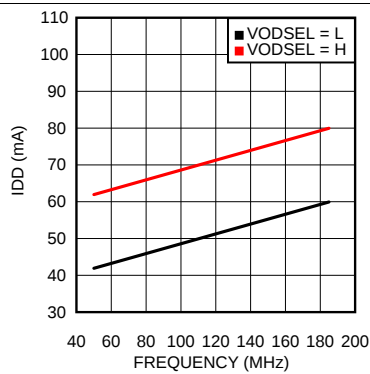
### 9.2.2.1 LVDS Interconnect Guidelines

Refer to the [AN-1108 Channel-Link PCB and Interconnect Design-In Guidelines](#) (SNLA008) and [Transmission Line RAPIDESIGNER Operation and Applications Guide](#) (SNLA035) for full details.

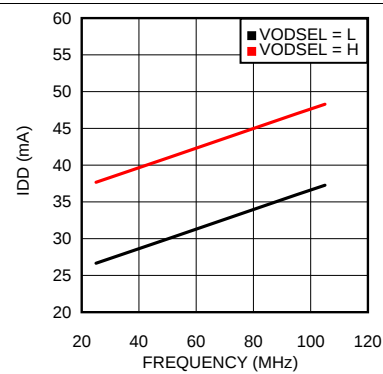
- Use 100-Ω coupled differential pairs
- Use differential connectors when above 500 Mbps
- Minimize skew within the pair
- Use the S/2S/3S rule in spacings
  - S = space between the pairs
  - 2S = space between pairs
  - 3S = space to LVCMOS signals
- Place ground vias next to signal vias when changing between layers
- When a signal changes reference planes, place a bypass cap and vias between the new and old reference plane

For more tips and detailed suggestions regarding high speed board layout principles, see the LVDS Owner's Manual at <http://www.ti.com/lvds>

## 9.2.3 Application Curves



⊗ 19. Typical Current Draw - Single In/Dual Out Mode - PRBS-7 Data Pattern



⊗ 20. Typical Current Draw - Single In/Single Out Mode - PRBS-7 Data Pattern

## 10 Power Supply Recommendations

### 10.1 Power Up Sequence

The  $V_{DD}$  power supply pins do not require a specific power on sequence and can be powered on in any order. However, the PDB pin should only be set to logic HIGH once the power sent to all supply pins is stable. Active data inputs should not be applied to the DS90C187 until all of the input power pins have been powered on, settled to the recommended operating voltage and the PDB pin has been set to logic HIGH.

The user experience can be impacted by the way a system powers up and powers down an LCD screen. The following sequence is recommended:

Power up sequence (DS90C187 PDB input initially LOW):

1. Ramp up LCD power (maybe 0.5ms to 10ms) but keep backlight turned off.
2. Toggle DS90C187 power down pin to PDB =  $V_{DD}$ .
3. Enable clock and wait for additional 0-200ms to ensure display noise won't occur.
4. Enable video source output; start sending black video data.
5. Send >1ms of black video data; this allows the DS90C187 to be phase locked, and the display to show black data first.
6. Start sending true image data.
7. Enable backlight.

Power Down sequence (DS90C187 PDB input initially HIGH):

1. Disable LCD backlight; wait for the minimum time specified in the LCD data sheet for the backlight to go low.
2. Video source output data switch from active video data to black image data (all visible pixel turn black); drive this for >2 frame times.
3. Set DS90C187 power down pin to PDB = GND.
4. Disable the video output of the video source.
5. Remove power from the LCD panel for lowest system power.

The DS90C187 is highly sensitive to the VDD input. Even small levels on the VDD pin prior to full power up should be avoided. The user should additionally take care to not drive or pull up the CMOS inputs to the device prior to device power up so as to ensure proper power on behavior.

### 10.2 Power Supply Filtering

The DS90C187 has several power supply pins at 1.8 V. It is important that these pins all be connected and properly bypassed. Bypassing should consist of at least one 0.1 $\mu$ F capacitor placed on each pin, with an additional 4.7  $\mu$ F - 22  $\mu$ F capacitor placed on the PLL supply pin (VDDP). 0.01  $\mu$ F capacitors are typically recommended for each pin. Additional filtering including ferrite beads may be necessary for noisy systems. It is recommended to place a 0 ohm resistor at the bypass capacitors that connect to each power pin to allow for additional filtering if needed. A large bulk capacitor is recommended at the point of power entry. This is typically in the 50  $\mu$ F — 100  $\mu$ F range.

## 11 Layout

### 11.1 Layout Guidelines

Circuit board layout and stack-up for the LVDS devices should be designed to provide low-noise power feed to the device. Good layout practice will also separate high frequency or high-level inputs and outputs to minimize unwanted stray noise pickup, feedback and interference. Power system performance may be greatly improved by using thin dielectrics (2 to 4 mils) for power / ground sandwiches. This arrangement provides plane capacitance for the PCB power system with low-inductance parasitics, which has proven especially effective at high frequencies, and makes the value and placement of external bypass capacitors less critical. This practice is easier to implement in dense pcbs with many layers and may not be practical in simpler boards. External bypass capacitors should include both RF ceramic and tantalum electrolytic types. RF capacitors may use values in the range of 0.01 uF to 0.1 uF. Tantalum capacitors may be in the 2.2 uF to 10 uF range. Voltage rating of the tantalum capacitors should be at least 5X the power supply voltage being used.

Surface mount capacitors are recommended due to their smaller parasitics. When using multiple capacitors per supply pin, locate the smaller value closer to the pin. It is recommended to connect power and ground pins directly to the power and ground planes with bypass capacitors connected to the plane with vias on both ends of the capacitor.

A small body size X7R chip capacitor, such as 0603, is recommended for external bypass. Its small body size reduces the parasitic inductance of the capacitor. The user must pay attention to the resonance frequency of these external bypass capacitors, usually in the range of 20-30 MHz. To provide effective bypassing, multiple capacitors are often used to achieve low impedance between the supply rails over the frequency of interest. At high frequency, it is also a common practice to use two vias from power and ground pins to the planes, reducing the impedance at high frequency. Some devices provide separate power and ground pins for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. Pin Description tables typically provide guidance on which circuit blocks are connected to which power pin pairs. In some cases, an external filter may be used to provide clean power to sensitive circuits such as PLLs.

Use at least a four layer board with a power and ground plane. Locate LVCMOS signals away from the LVDS lines to prevent coupling from the LVCMOS lines to the LVDS lines. Closely coupled differential lines of 100 Ohms are typically recommended for LVDS interconnect. The closely coupled lines help to ensure that coupled noise will appear as common mode and thus is rejected by the receivers. The tightly coupled lines will also radiate less.

For more information on the VQFN package, refer to the [AN-1187 Leadless Leadframe Package \(LLP\)](#) application note (SNOA401).

## 11.2 Layout Example

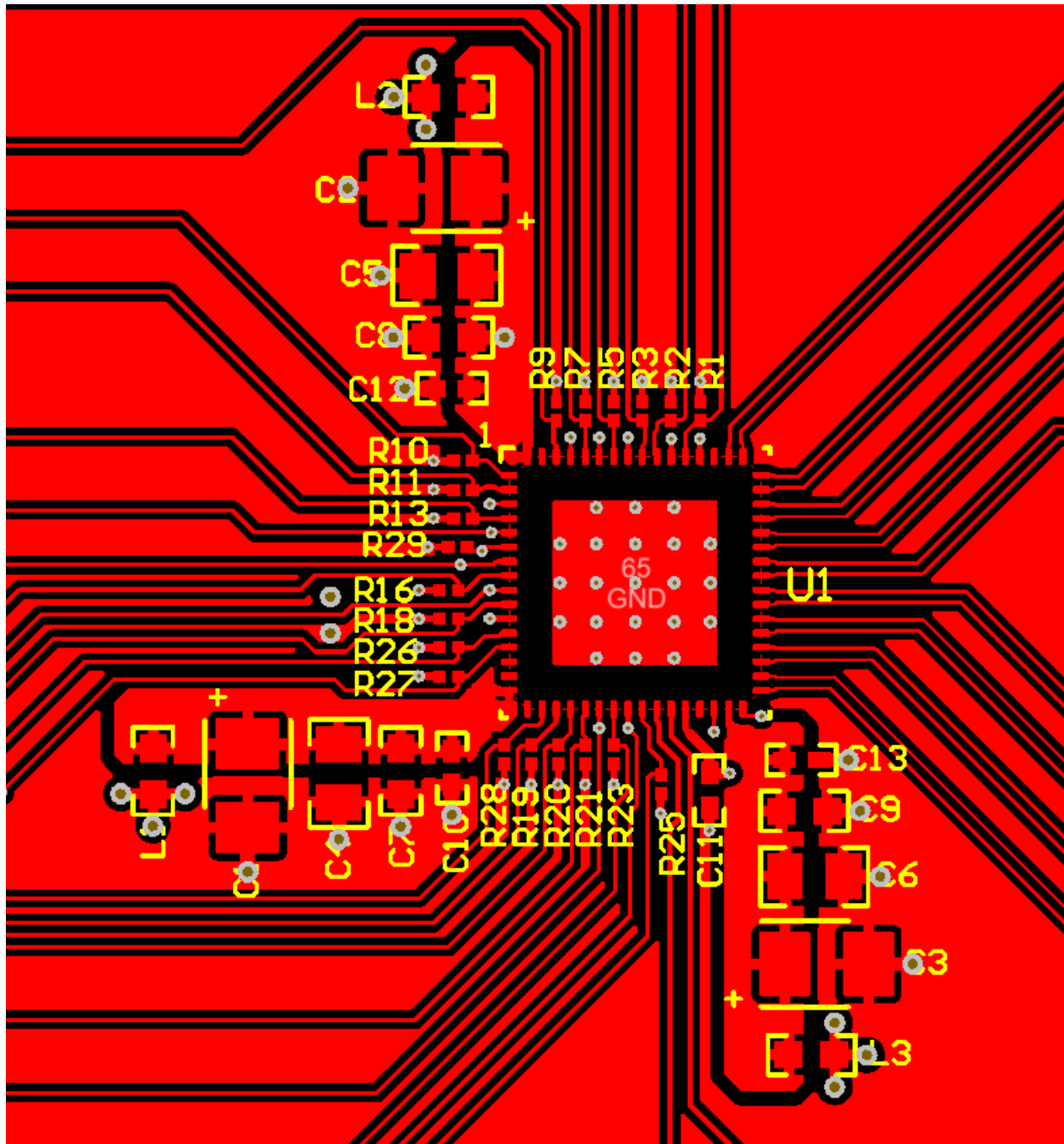


图 21. Layout Example

## 12 デバイスおよびドキュメントのサポート

### 12.1 ドキュメントのサポート

#### 12.1.1 関連資料

関連資料については、以下を参照してください。

- 『LVDSオーナー・マニュアル』(SNLA187)
- 『AN-1108 チャネル・リンクPCBと相互接続デザイン・インのガイドライン』(SNLA008)
- 『転送ラインRAPIDESIGNER操作およびアプリケーション・ガイド』(SNLA035)
- 『AN-1187 リードレス・リードフレーム・パッケージ(LLP)』(SNOA401)

### 12.2 ドキュメントの更新通知を受け取る方法

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### 12.3 コミュニティ・リソース

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### 12.6 Glossary

[SLYZ022](#) — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

## 13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| DS90C187LF/NOPB  | ACTIVE        | VQFN-MR      | NLA                | 92   | 1000           | RoHS & Green    | NIPDAU                               | Level-3-260C-168 HR  | -10 to 70    | 90C187LF                | <a href="#">Samples</a> |
| DS90C187LFE/NOPB | ACTIVE        | VQFN-MR      | NLA                | 92   | 250            | RoHS & Green    | NIPDAU                               | Level-3-260C-168 HR  | -10 to 70    | 90C187LF                | <a href="#">Samples</a> |
| DS90C187LFX/NOPB | ACTIVE        | VQFN-MR      | NLA                | 92   | 2500           | RoHS & Green    | NIPDAU                               | Level-3-260C-168 HR  | -10 to 70    | 90C187LF                | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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## PACKAGE OPTION ADDENDUM

10-Dec-2020

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## TAPE AND REEL INFORMATION



\*All dimensions are nominal

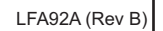
| Device           | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| DS90C187LF/NOPB  | VQFN-MR      | NLA             | 92   | 1000 | 330.0              | 16.4               | 7.3     | 7.3     | 1.3     | 12.0    | 16.0   | Q1            |
| DS90C187LFE/NOPB | VQFN-MR      | NLA             | 92   | 250  | 178.0              | 16.4               | 7.3     | 7.3     | 1.3     | 12.0    | 16.0   | Q1            |
| DS90C187LFX/NOPB | VQFN-MR      | NLA             | 92   | 2500 | 330.0              | 16.4               | 7.3     | 7.3     | 1.3     | 12.0    | 16.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device           | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| DS90C187LF/NOPB  | VQFN-MR      | NLA             | 92   | 1000 | 356.0       | 356.0      | 35.0        |
| DS90C187LFE/NOPB | VQFN-MR      | NLA             | 92   | 250  | 208.0       | 191.0      | 35.0        |
| DS90C187LFX/NOPB | VQFN-MR      | NLA             | 92   | 2500 | 356.0       | 356.0      | 35.0        |



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