

# LM74700-EP 低静止電流 (I<sub>q</sub>) 理想ダイオード・コントローラ

## 1 特長

- 3.2V～65V の入力範囲 (スタートアップ時 3.9V)
- 逆電圧定格: -65V
- 外部の N チャネル MOSFET 用のチャージ・ポンプ
- アノードからカソードへの順方向電圧降下レギュレーション: 20mV
- イネーブル・ピン機能
- シャットダウン時電流 (EN=LOW): 1μA
- 動作時静止電流 (EN=HIGH): 80μA
- ピーク・ゲート・ターンオフ電流: 2.3A
- 逆電流阻止に対する高速応答: < 0.75μs
- 適切な TVS ダイオードにより車載用 ISO7637 過渡要件に適合
- 8 ピンの SOT-23 パッケージ (2.90mm × 1.60mm) で供給
- 軍用温度範囲 (-55°C～+125°C)
- 単一の製造、アセンブリ、テスト施設
- 長い製品ライフ・サイクル
- 長期にわたる製品変更通知
- 製品のトレーサビリティ

## 2 アプリケーション

- 航空宇宙 / 防衛
- 医療用画像処理
- 冗長化電源用のアクティブ OR

## 3 概要

LM74700-EP は、外部の N チャネル MOSFET と組み合わせることで理想ダイオード整流器として動作し、20mV の順方向電圧降下で低損失逆極性保護を実現する理想ダイオード・コントローラです。入力電源電圧範囲が 3.2V～65V と広いため、12V、24V、48V のシステムなど多くの一般的な DC バス電圧を制御できます。このデバイスは、最低 -65V の負の電源電圧に耐えられ、負荷を保護できます。

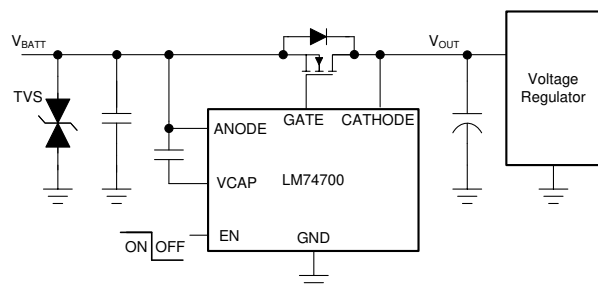
このデバイスは、MOSFET のゲートを制御し、順方向電圧降下を 20mV にレギュレートします。このレギュレーション方式により、逆電流発生時に MOSFET を穏やかにオフにでき、DC 逆電流を確実にゼロにします。このデバイスは、逆電流阻止への応答が高速 (0.75μs 未満) なため、電源障害および入力マイクロ短絡状況で出力電圧のホールドアップ要件を持つシステムに適しています。

LM74700-EP コントローラは、外部の N チャネル MOSFET に対してチャージ・ポンプによるゲート駆動を行います。LM74700-EP は電圧定格が高いため、車載用 ISO7637 保護のシステム設計が簡単になります。イネーブル・ピンが LOW のとき、コントローラはオフで、消費電流は約 1μA です。LM74700-EP は、T<sub>A</sub> = -55°C～+125°C の温度範囲で完全に動作が規定されています。

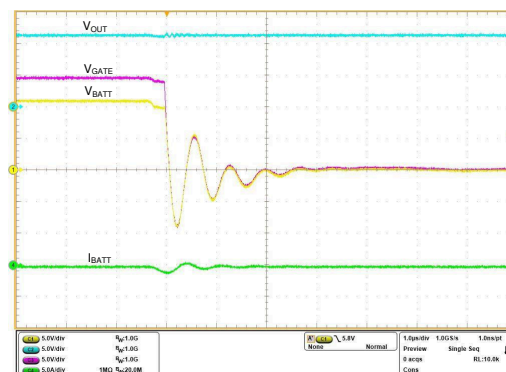
### 製品情報(1)

部品番号	パッケージ	本体サイズ (公称)
LM74700-EP	SOT-23 (8)	2.90mm × 1.60mm

- (1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



代表的なアプリケーション回路図



入力短絡時の逆電流阻止



## Table of Contents

<b>1 特長</b> .....	<b>1</b>	8.4 Device Functional Modes.....	<b>14</b>
<b>2 アプリケーション</b> .....	<b>1</b>	<b>9 Application and Implementation</b> .....	<b>15</b>
<b>3 概要</b> .....	<b>1</b>	9.1 Application Information.....	15
<b>4 Revision History</b> .....	<b>2</b>	9.2 Typical Application.....	15
<b>5 Pin Configuration and Functions</b> .....	<b>3</b>	9.3 OR-ing Application Configuration.....	21
<b>6 Specifications</b> .....	<b>4</b>	<b>10 Power Supply Recommendations</b> .....	<b>22</b>
6.1 Absolute Maximum Ratings .....	4	<b>11 Layout</b> .....	<b>23</b>
6.2 ESD Ratings .....	4	11.1 Layout Guidelines.....	23
6.3 Recommended Operating Conditions .....	4	11.2 Layout Example.....	23
6.4 Thermal Information .....	5	<b>12 Device and Documentation Support</b> .....	<b>24</b>
6.5 Electrical Characteristics .....	5	12.1 Receiving Notification of Documentation Updates..	24
6.6 Switching Characteristics .....	6	12.2 サポート・リソース.....	24
6.7 Typical Characteristics.....	7	12.3 Trademarks.....	24
<b>7 Parameter Measurement Information</b> .....	<b>10</b>	12.4 Electrostatic Discharge Caution.....	24
<b>8 Detailed Description</b> .....	<b>11</b>	12.5 Glossary.....	24
8.1 Overview.....	11	<b>13 Mechanical, Packaging, and Orderable Information</b> .....	<b>24</b>
8.2 Functional Block Diagram.....	11		
8.3 Feature Description.....	12		

## 4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
September 2021	*	Initial Release

## 5 Pin Configuration and Functions

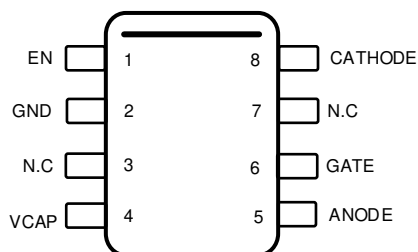


図 5-1. DDF Package 8-Pin SOT-23 Top View

表 5-1. Pin Functions

PIN		I/O <sup>(1)</sup>	DESCRIPTION
NO.	NAME		
1	EN	I	Enable pin. Can be connected to ANODE for always ON operation.
2	GND	G	Ground pin
3	N.C		No connection. Keep this pin floating.
4	VCAP	O	Charge pump output. Connect to external charge pump capacitor.
5	ANODE	I	Anode of the diode and input power. Connect to the source of the external N-channel MOSFET.
6	GATE	O	Gate drive output. Connect to gate of the external N-channel MOSFET.
7	N.C		No connection. Keep this pin floating.
8	CATHODE	I	Cathode of the diode. Connect to the drain of the external N-channel MOSFET.

(1) I = Input, O = Output, G = GND

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Input Pins	ANODE to GND	−65	65	V
	EN to GND, $V_{(ANODE)} > 0$ V	−0.3	65	V
	EN to GND, $V_{(ANODE)} \leq 0$ V	$V_{(ANODE)}$	$(65 + V_{(ANODE)})$	V
Output Pins	GATE to ANODE	−0.3	15	V
	VCAP to ANODE	−0.3	15	V
Output to Input Pins	CATHODE to ANODE	−5	75	V
Operating junction temperature <sup>(2)</sup>		−55	150	°C
Storage temperature, $T_{stg}$		−55	150	°C

- (1) Operation outside the Absolute Maximum Ratings can cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device can not be fully functional, and this can affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

### 6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per JEDEC JS-001 <sup>(1)</sup>	±2000	V
		Charged device model (CDM), per JEDEC JS-002 <sup>(2)</sup>	±750	
			±500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP155 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	NOM	MAX	UNIT
Input Pins	ANODE to GND	−60		60	V
	CATHODE to GND			60	
	EN to GND	−60		60	
Input to Output pins	ANODE to CATHODE	−70			V
External capacitance	ANODE	22			nF
	CATHODE, VCAP to ANODE	0.1			μF
External MOSFET max $V_{GS}$ rating	GATE to ANODE	15			V
$T_J$	Operating junction temperature range <sup>(2)</sup>	−55		125	°C

- (1) Recommended Operating Conditions are conditions under which the device is intended to be functional. For specifications and test conditions, see [Electrical Characteristics](#).
- (2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		LM74700-EP	UNIT
		DDF (SOT)	
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	189.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	103.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	45.8	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	19.4	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	45.5	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

## 6.5 Electrical Characteristics

$T_J = -55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ; typical values at  $T_J = 25^{\circ}\text{C}$ ,  $V_{(ANODE)} = 12\text{ V}$ ,  $C_{(VCAP)} = 0.1\text{ }\mu\text{F}$ ,  $V_{(EN)} = 3.3\text{ V}$ , over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>ANODE</sub> SUPPLY VOLTAGE						
V <sub>(ANODE)</sub>	Operating input voltage		4		60	V
V <sub>(ANODE POR)</sub>	VANODE POR Rising threshold				3.9	V
	VANODE POR Falling threshold		2.2	2.8	3.1	V
V <sub>(ANODE POR(Hys))</sub>	VANODE POR Hysteresis		0.39		0.7	V
I <sub>(SHDN)</sub>	Shutdown Supply Current	V <sub>(EN)</sub> = 0 V		0.9	1.5	μA
I <sub>(Q)</sub>	Operating Quiescent Current			80	140	μA
		V <sub>ANODE</sub> = 28 V		80	150	μA
ENABLE INPUT						
V <sub>(EN_IL)</sub>	Enable input low threshold		0.5	0.9	1.22	V
V <sub>(EN_IH)</sub>	Enable input high threshold		1.06	2	2.6	
V <sub>(EN_Hys)</sub>	Enable Hysteresis		0.52		1.42	V
I <sub>(EN)</sub>	Enable sink current	V <sub>(EN)</sub> = 12 V		3	5	μA
V <sub>ANODE</sub> to V <sub>CATHODE</sub>						
V <sub>(AK REG)</sub>	Regulated Forward V <sub>(AK)</sub> Threshold		13	20	30	mV
		V <sub>ANODE</sub> = 28 V	13	20	30	mV
V <sub>(AK)</sub>	V <sub>(AK)</sub> threshold for full conduction mode		34	55	70	mV
V <sub>(AK REV)</sub>	V <sub>(AK)</sub> threshold for reverse current blocking		−17	−11	−5	mV
		V <sub>ANODE</sub> = 28 V	−17	−11	−5	mV
G <sub>m</sub>	Regulation Error AMP Transconductance <sup>(1)</sup>		440	1800	4900	μA/V
GATE DRIVE						
I <sub>(GATE)</sub>	Peak source current	V <sub>(ANODE)</sub> − V <sub>(CATHODE)</sub> = 100 mV, V <sub>(GATE)</sub> − V <sub>(ANODE)</sub> = 5 V	3	11		mA
	Peak sink current	V <sub>(ANODE)</sub> − V <sub>(CATHODE)</sub> = −20 mV, V <sub>(GATE)</sub> − V <sub>(ANODE)</sub> = 5 V		2370		mA
	Regulation max sink current	V <sub>(ANODE)</sub> − V <sub>(CATHODE)</sub> = 0 V, V <sub>(GATE)</sub> − V <sub>(ANODE)</sub> = 5 V	2	26		μA
RDS <sub>ON</sub>	discharge switch RDS <sub>ON</sub>	V <sub>(ANODE)</sub> − V <sub>(CATHODE)</sub> = −20 mV, V <sub>(GATE)</sub> − V <sub>(ANODE)</sub> = 100 mV	0.4		2	Ω
CHARGE PUMP						

## 6.5 Electrical Characteristics (continued)

$T_J = -55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ; typical values at  $T_J = 25^{\circ}\text{C}$ ,  $V_{(\text{ANODE})} = 12\text{ V}$ ,  $C_{(\text{VCAP})} = 0.1\text{ }\mu\text{F}$ ,  $V_{(\text{EN})} = 3.3\text{ V}$ , over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(\text{VCAP})}$	Charge Pump source current (Charge pump on)	$V_{(\text{VCAP})} - V_{(\text{ANODE})} = 7\text{ V}$	162	300	600	$\mu\text{A}$
	Charge Pump sink current (Charge pump off)	$V_{(\text{VCAP})} - V_{(\text{ANODE})} = 14\text{ V}$		5	10	$\mu\text{A}$
$V_{(\text{VCAP})} - V_{(\text{ANODE})}$	Charge pump voltage at $V_{(\text{ANODE})} = 3.2\text{ V}$	$I_{(\text{VCAP})} \leq 30\text{ }\mu\text{A}$	8			V
	Charge pump turn on voltage		10.4	11.6	12.9	V
	Charge pump turn off voltage		11	12.4	13.9	V
	Charge Pump Enable comparator Hysteresis		0.54	0.8	1.36	V
$V_{(\text{VCAP UVLO})}$	$V_{(\text{VCAP})} - V_{(\text{ANODE})}$ UV release at rising edge	$V_{(\text{ANODE})} - V_{(\text{CATHODE})} = 100\text{ mV}$	5.6	6.6	8.7	V
	$V_{(\text{VCAP})} - V_{(\text{ANODE})}$ UV threshold at falling edge	$V_{(\text{ANODE})} - V_{(\text{CATHODE})} = 100\text{ mV}$	5.05	5.4	6	V
<b>CATHODE</b>						
$I_{(\text{CATHODE})}$	CATHODE sink current	$V_{(\text{ANODE})} = 12\text{ V}$ , $V_{(\text{ANODE})} - V_{(\text{CATHODE})} = -100\text{ mV}$		1.2	2	$\mu\text{A}$
		$V_{(\text{ANODE})} - V_{(\text{CATHODE})} = -100\text{ mV}$		1.6	2.2	$\mu\text{A}$
		$V_{(\text{ANODE})} = -12\text{ V}$ , $V_{(\text{CATHODE})} = 12\text{ V}$		1.25	2.06	$\mu\text{A}$

(1) Parameter guaranteed by design and characterization

## 6.6 Switching Characteristics

$T_J = -55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ; typical values at  $T_J = 25^{\circ}\text{C}$ ,  $V_{(\text{ANODE})} = 12\text{ V}$ ,  $C_{(\text{VCAP})} = 0.1\text{ }\mu\text{F}$ ,  $V_{(\text{EN})} = 3.3\text{ V}$ , over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\text{EN}_{\text{TDLY}}$	Enable (low to high) to Gate Turn On delay	$V_{(\text{VCAP})} > V_{(\text{VCAP UVLOR})}$		75	110	$\mu\text{s}$
$t_{\text{Reverse delay}}$	Reverse voltage detection to Gate Turn Off delay	$V_{(\text{ANODE})} - V_{(\text{CATHODE})} = 100\text{ mV to } -100\text{ mV}$		0.45	0.75	$\mu\text{s}$
		$V_{(\text{ANODE})} = 28\text{ V}$ , $V_{(\text{ANODE})} - V_{(\text{CATHODE})} = 100\text{ mV to } -100\text{ mV}$		0.45	0.75	$\mu\text{s}$
$t_{\text{Forward recovery}}$	Forward voltage detection to Gate Turn On delay	$V_{(\text{ANODE})} - V_{(\text{CATHODE})} = -100\text{ mV to } 700\text{ mV}$		1.4	3.1	$\mu\text{s}$
		$V_{(\text{ANODE})} = 28\text{ V}$ , $V_{(\text{ANODE})} - V_{(\text{CATHODE})} = -100\text{ mV to } 700\text{ mV}$		1.4	2.6	$\mu\text{s}$

## 6.7 Typical Characteristics

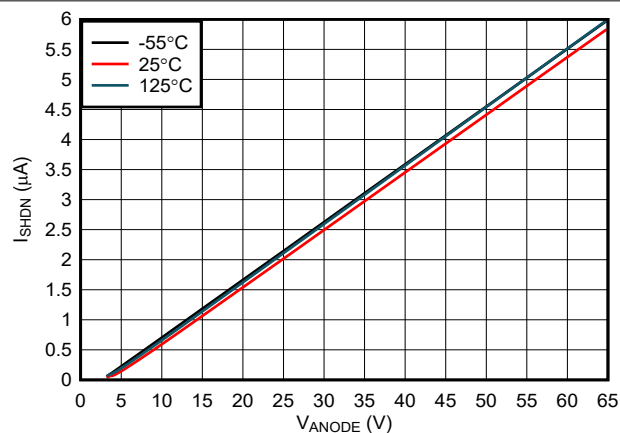


FIG 6-1. Shutdown Supply Current vs Supply Voltage

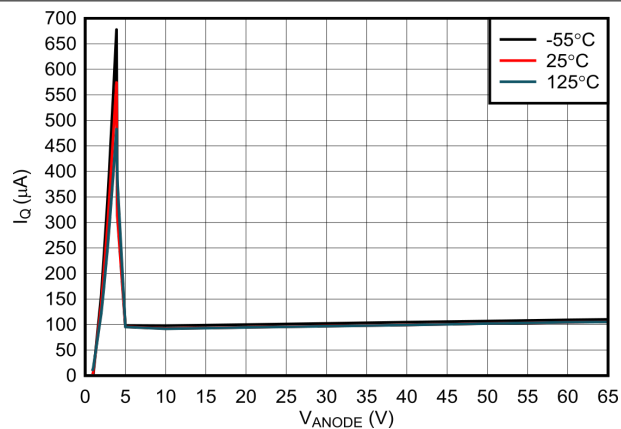


FIG 6-2. Operating Quiescent Current vs Supply Voltage

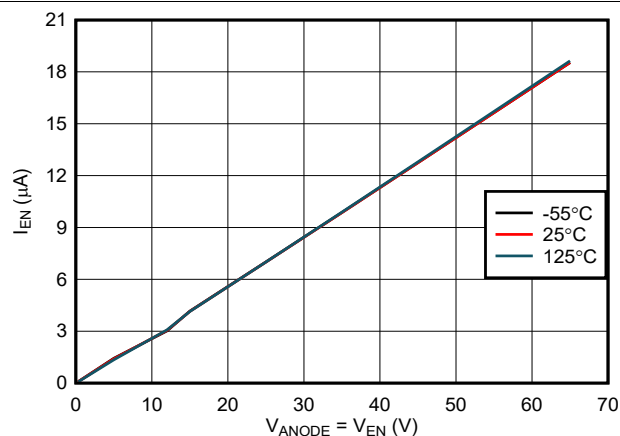


FIG 6-3. Enable Sink Current vs Supply Voltage

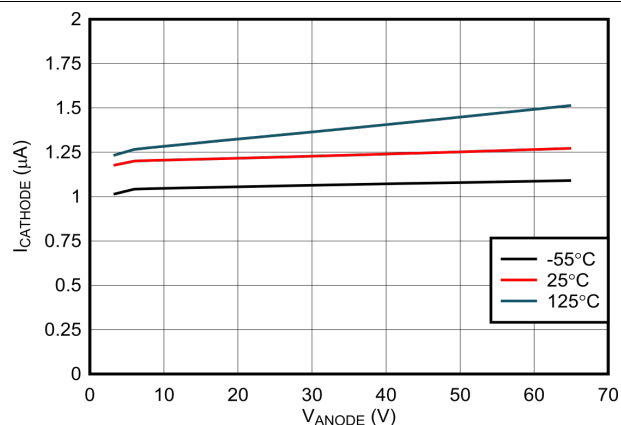


FIG 6-4. Cathode Sink Current vs Supply Voltage

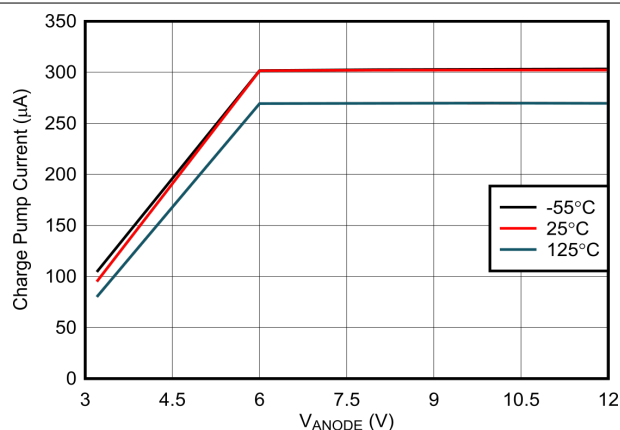


FIG 6-5. Charge Pump Current vs Supply Voltage at  $V_{CAP} = 6\text{ V}$

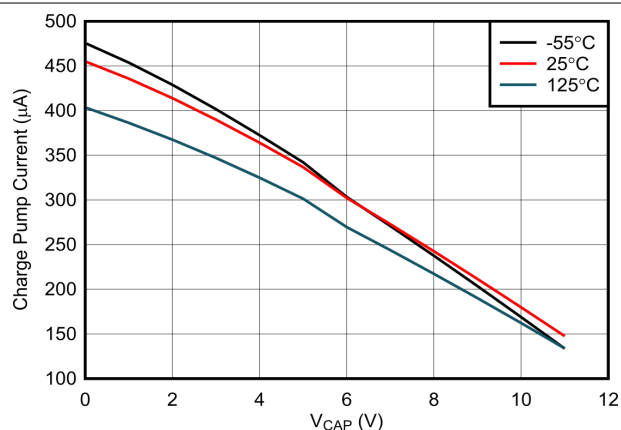


FIG 6-6. Charge Pump V-I Characteristics at  $V_{ANODE} \geq 12\text{ V}$

## 6.7 Typical Characteristics (continued)

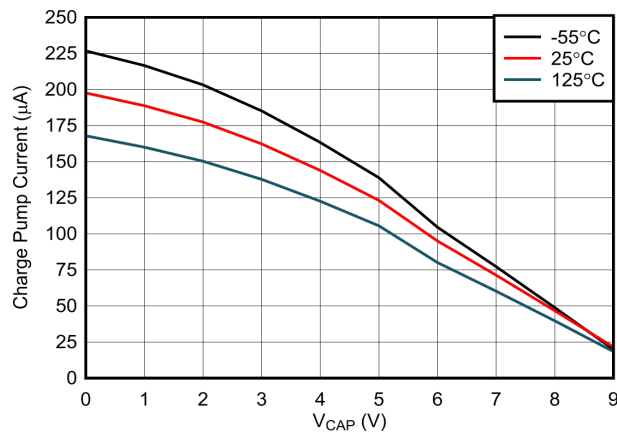


FIG 6-7. Charge Pump V-I Characteristics at VANODE = 3.2 V

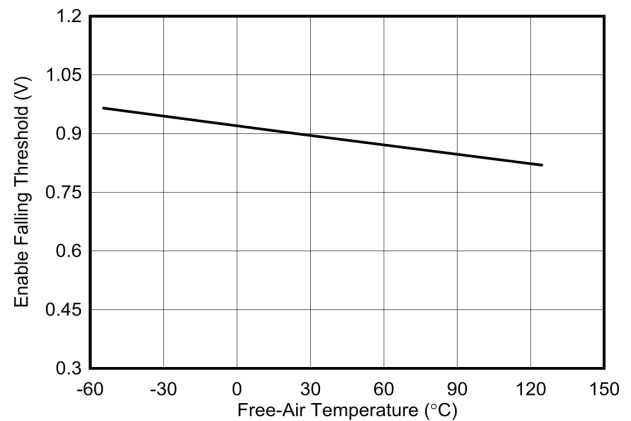


FIG 6-8. Enable Falling Threshold vs Temperature

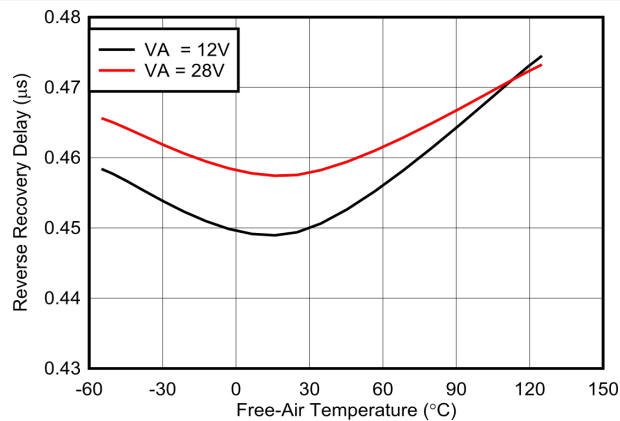


FIG 6-9. Reverse Current Blocking Delay vs Temperature

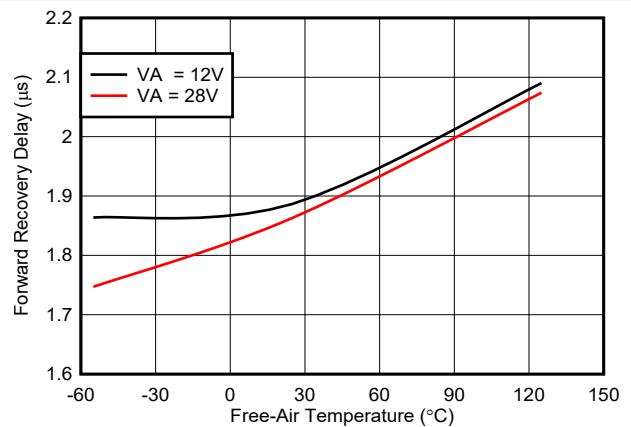


FIG 6-10. Forward Recovery Delay vs Temperature

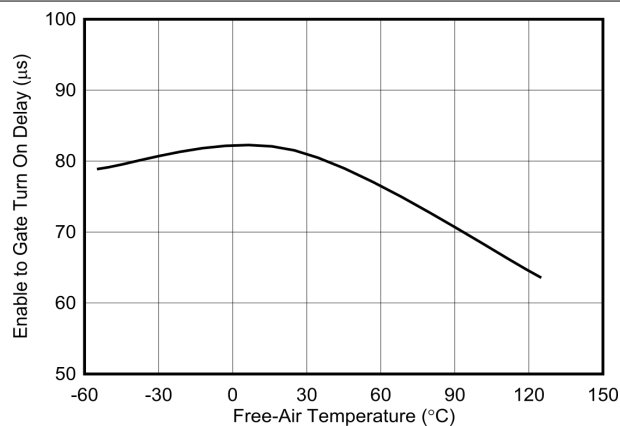


FIG 6-11. Enable to Gate Delay vs Temperature

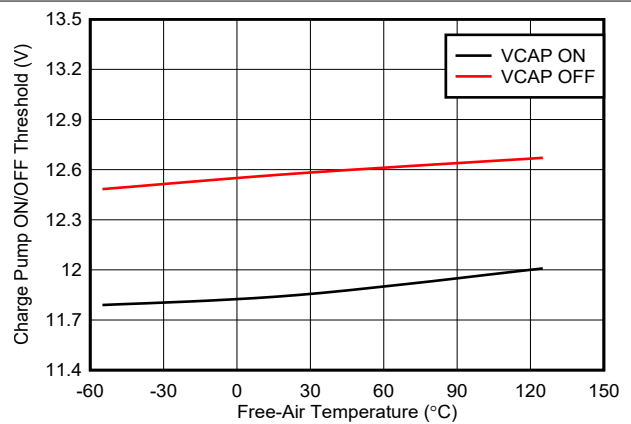
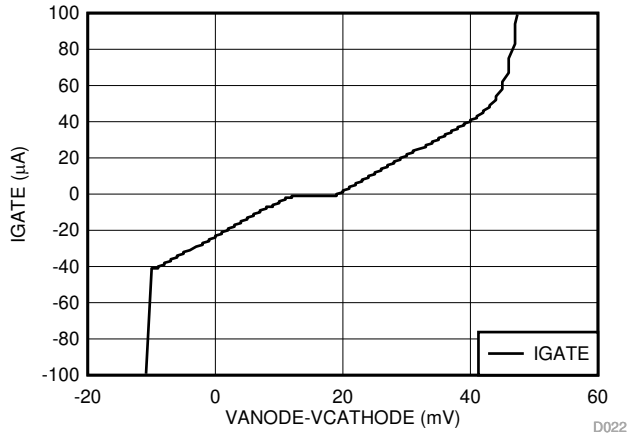


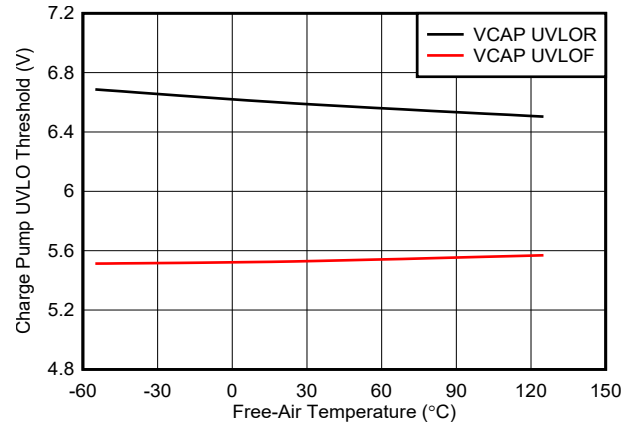
FIG 6-12. Charge Pump ON/OFF Threshold vs Temperature



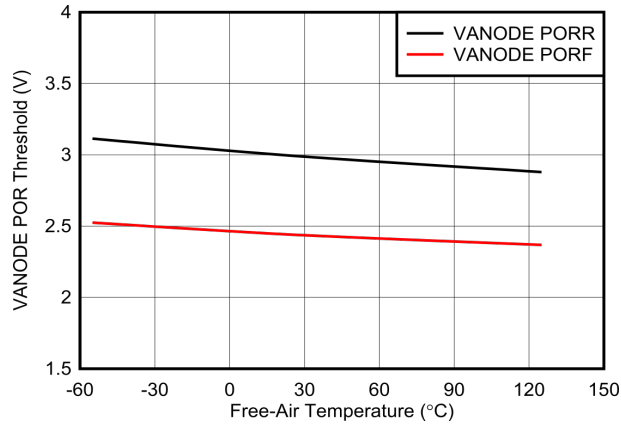
## 6.7 Typical Characteristics (continued)



6-13. Gate Current vs Forward Voltage Drop



6-14. Charge Pump UVLO Threshold vs Temperature



6-15. VANODE POR Threshold vs Temperature

## 7 Parameter Measurement Information

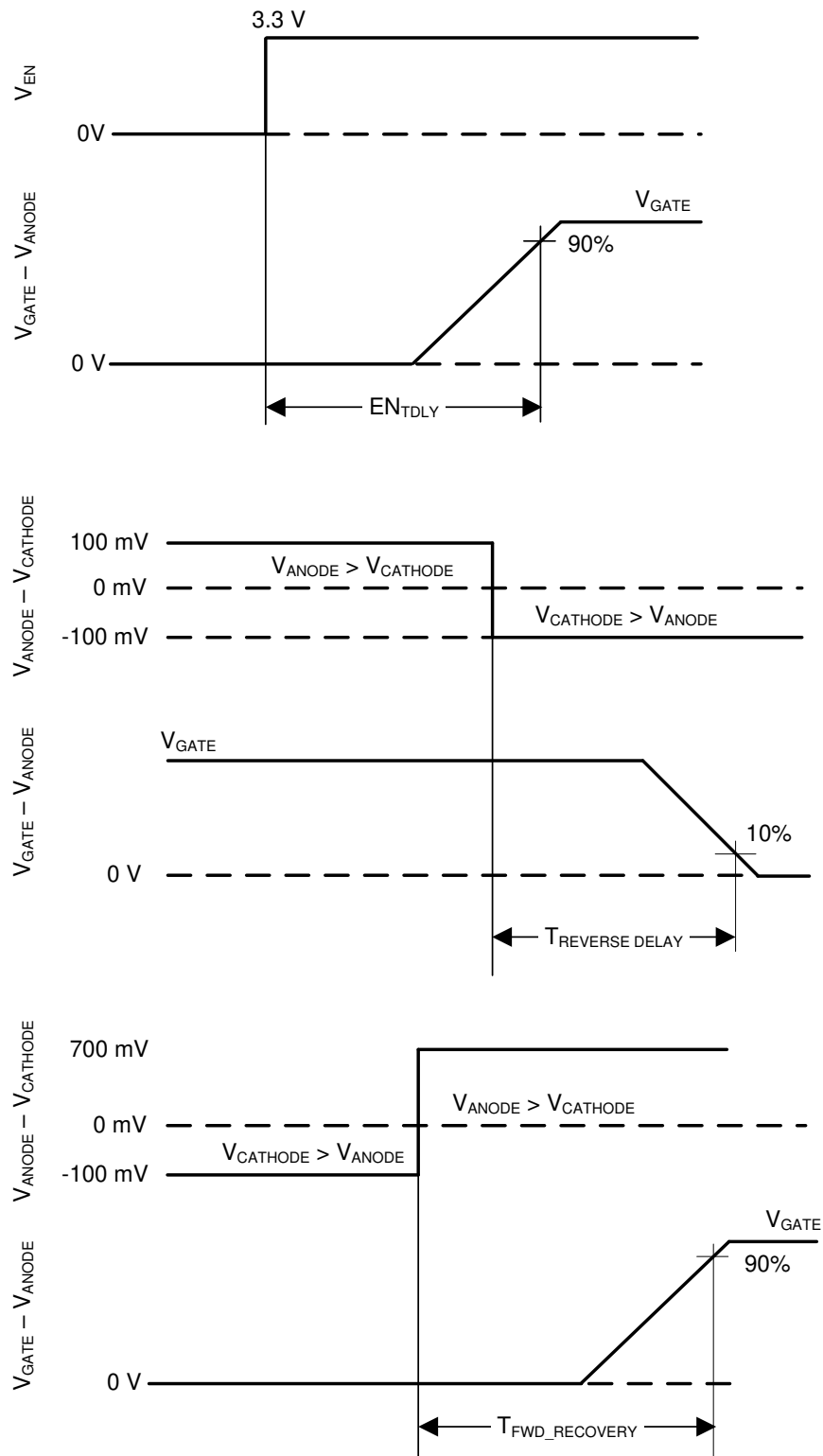


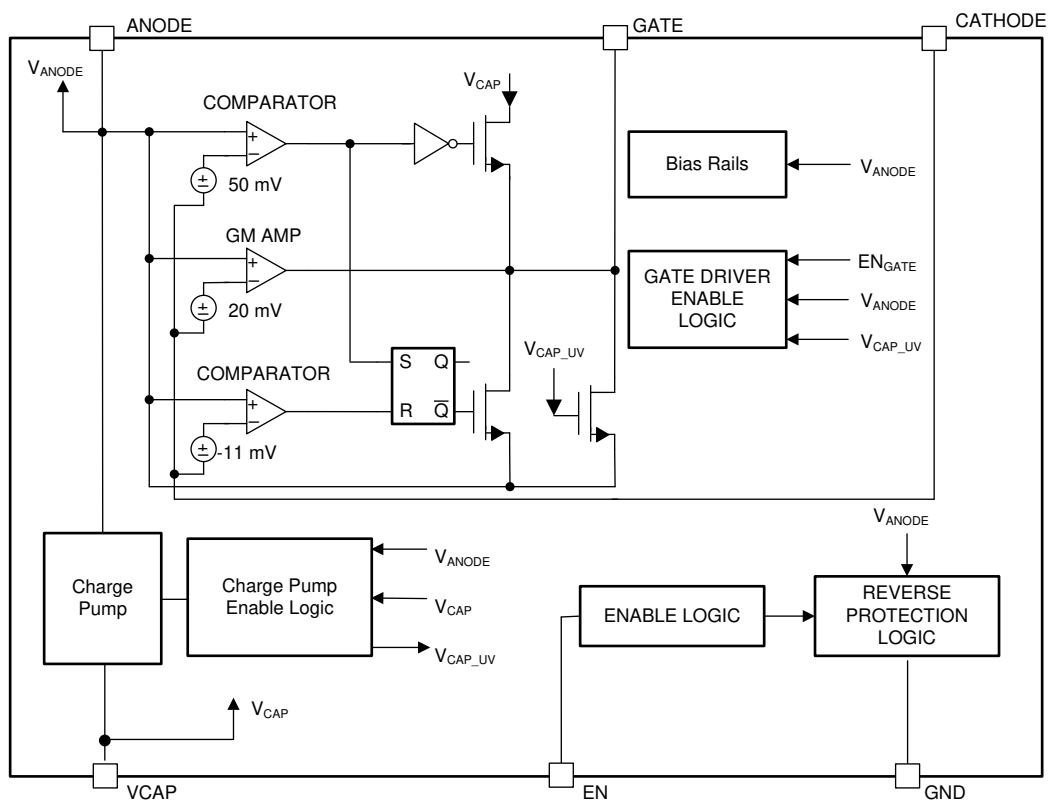
图 7-1. Timing Waveforms

## 8 Detailed Description

### 8.1 Overview

The LM74700-EP ideal diode controller has all the features necessary to implement an efficient and fast reverse polarity protection circuit or be used in an ORing configuration while minimizing the number of external components. This easy to use ideal diode controller is paired with an external N-channel MOSFET to replace other reverse polarity schemes, such as a P-channel MOSFET or a Schottky diode. An internal charge pump is used to drive the external N-Channel MOSFET to a maximum gate drive voltage of approximately 15 V. The voltage drop across the MOSFET is continuously monitored between the ANODE and GATE pins, and the GATE to ANODE voltage is adjusted as needed to regulate the forward voltage drop at 20 mV. This closed loop regulation scheme enables graceful turn off of the MOSFET during a reverse current event and ensures zero DC reverse current flow. A fast reverse current condition is detected when the voltage across ANODE and CATHODE pins reduces below  $-11$  mV, resulting in the GATE pin being internally connected to the ANODE pin turning off the external N-channel MOSFET, and using the body diode to block any of the reverse current. An enable pin, EN, is available to place the LM74700-EP in shutdown mode, disabling the N-Channel MOSFET and minimizing the quiescent current.

### 8.2 Functional Block Diagram



Copyright © 2017, Texas Instruments Incorporated

## 8.3 Feature Description

### 8.3.1 Input Voltage

The ANODE pin is used to power the LM74700-EP's internal circuitry, typically drawing 80  $\mu\text{A}$  when enabled and 1  $\mu\text{A}$  when disabled. If the ANODE pin voltage is greater than the POR Rising threshold, then LM74700-EP operates in either shutdown mode or conduction mode in accordance with the EN pin voltage. The voltage from ANODE to GND is designed to vary from 65 V to –65 V, allowing the LM74700-EP to withstand negative voltage transients.

### 8.3.2 Charge Pump

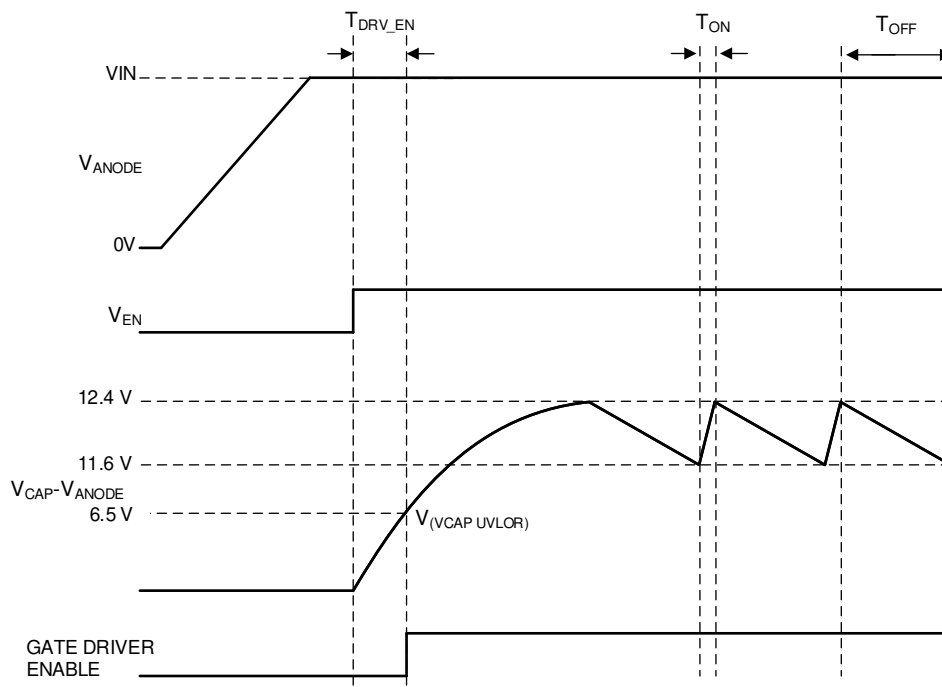
The charge pump supplies the voltage necessary to drive the external N-channel MOSFET. An external charge pump capacitor is placed between VCAP and ANODE pins to provide energy to turn on the external MOSFET. In order for the charge pump to supply current to the external capacitor the EN pin voltage must be above the specified input high threshold,  $V_{(EN\_IH)}$ . When enabled the charge pump sources a charging current of 300- $\mu\text{A}$  typical. If EN pins is pulled low, then the charge pump remains disabled. To ensure that the external MOSFET can be driven above its specified threshold voltage, the VCAP to ANODE voltage must be above the undervoltage lockout threshold, typically 6.5 V, before the internal gate driver is enabled. Use 式 1 to calculate the initial gate driver enable delay.

$$T_{(DRV\_EN)} = 75 \mu\text{s} + C_{(VCAP)} \times \frac{V_{(VCAP\_UVLOR)}}{300 \mu\text{A}} \quad (1)$$

where

- $C_{(VCAP)}$  is the charge pump capacitance connected across ANODE and VCAP pins
- $V_{(VCAP\_UVLOR)} = 6.5 \text{ V}$  (typical)

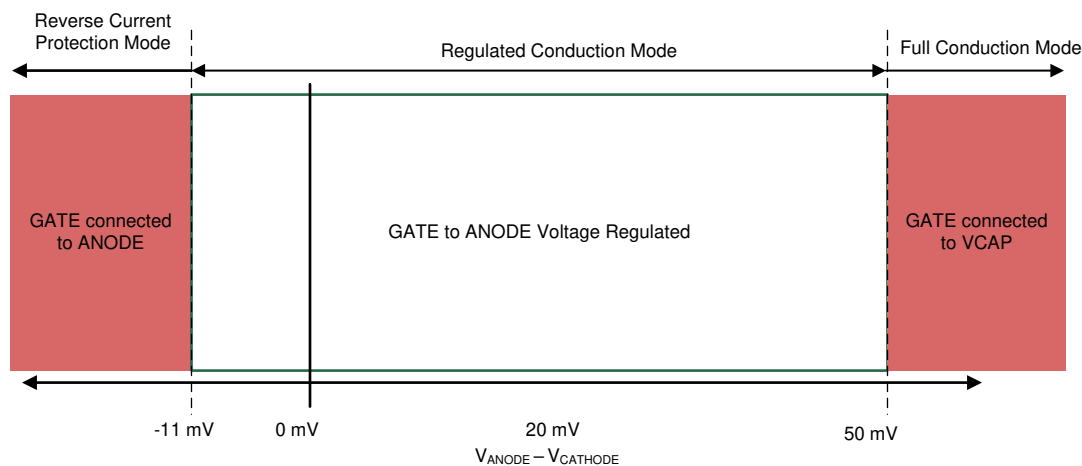
To remove any chatter on the gate drive, approximately 800 mV of hysteresis is added to the VCAP undervoltage lockout. The charge pump remains enabled until the VCAP to ANODE voltage reaches 12.4 V, typically, at which point the charge pump is disabled decreasing the current draw on the ANODE pin. The charge pump remains disabled until the VCAP to ANODE voltage is below to 11.6-V typically, at which point the charge pump is enabled. The voltage between VCAP and ANODE continue to charge and discharge between 11.6 V and 12.4 V as shown in 図 8-1. By enabling and disabling the charge pump, the operating quiescent current of the LM74700-EP is reduced. When the charge pump is disabled it sinks to 5- $\mu\text{A}$  typical.



8-1. Charge Pump Operation

### 8.3.3 Gate Driver

The gate driver is used to control the external N-Channel MOSFET by setting the GATE to ANODE voltage to the corresponding mode of operation. There are three defined modes of operation that the gate driver operates under forward regulation, full conduction mode and reverse current protection, according to the ANODE to CATHODE voltage. Forward regulation mode, full conduction mode and reverse current protection mode are described in more detail in the [Regulated Conduction Mode](#), [Full Conduction Mode](#) and [Reverse Current Production Mode](#) sections. 8-2 depicts how the modes of operation vary according to the ANODE to CATHODE voltage of the LM74700-EP. The threshold between forward regulation mode and conduction mode is when the ANODE to CATHODE voltage is 50 mV. The threshold between forward regulation mode and reverse current protection mode is when the ANODE to CATHODE voltage is -11 mV.



8-2. Gate Driver Mode Transitions

Before the gate driver is enabled, the following three conditions must be achieved:

- The EN pin voltage must be greater than the specified input high voltage.

- The VCAP to ANODE voltage must be greater than the undervoltage lockout voltage.
- The ANODE voltage must be greater than VANODE POR Rising threshold.

If the above conditions are not achieved, then the GATE pin is internally connected to the ANODE pin, assuring that the external MOSFET is disabled. Once these conditions are achieved, the gate driver operates in the correct mode depending on the ANODE to CATHODE voltage.

#### 8.3.4 Enable

The LM74700-EP has an enable pin, EN. The enable pin allows for the gate driver to be either enabled or disabled by an external signal. If the EN pin voltage is greater than the rising threshold, the gate driver and charge pump operates as described in [Gate Driver](#) and [Charge Pump](#) sections. If the enable pin voltage is less than the input low threshold, the charge pump and gate driver are disabled placing the LM74700-EP in shutdown mode. The EN pin can withstand a voltage as large as 65 V and as low as –65 V. This ability allows for the EN pin to connect directly to the ANODE pin if enable functionality is not needed. In conditions where EN is left floating, the internal sink current of 3 uA pulls EN pin low and disables the device.

### 8.4 Device Functional Modes

#### 8.4.1 Shutdown Mode

The LM74700-EP enters shutdown mode when the EN pin voltage is below the specified input low threshold  $V_{(EN\_IL)}$ . Both the gate driver and the charge pump are disabled in shutdown mode. During shutdown mode the LM74700-EP enters low  $I_Q$  operation with the ANODE pin only sinking 1  $\mu$ A. When the LM74700-EP is in shutdown mode, forward current flow through the external MOSFET is not interrupted but is conducted through the MOSFET's body diode.

#### 8.4.2 Conduction Mode

Conduction mode occurs when the gate driver is enabled. There are three regions of operating during conduction mode based on the ANODE to CATHODE voltage of the LM74700-EP. Each of the three modes is described in the [Regulated Conduction Mode](#), [Full Conduction Mode](#) and [Reverse Current Protection Mode](#) sections.

##### 8.4.2.1 Regulated Conduction Mode

For the LM74700-EP to operate in regulated conduction mode, the gate driver must be enabled as described in the [Gate Driver](#) section, and the current from source to drain of the external MOSFET must be within the range to result in an ANODE to CATHODE voltage drop of –11 mV to 50 mV. During forward regulation mode, the ANODE to CATHODE voltage is regulated to 20 mV by adjusting the GATE to ANODE voltage. This closed loop regulation scheme enables graceful turn off of the MOSFET at very light loads and ensures zero DC reverse current flow.

##### 8.4.2.2 Full Conduction Mode

For the LM74700-EP to operate in full conduction mode, the gate driver must be enabled as described in the [Gate Driver](#) section. The current from source to drain of the external MOSFET must be large enough to result in an ANODE to CATHODE voltage drop of greater than 50-mV typical. If these conditions are achieved, the GATE pin is internally connected to the VCAP pin resulting in the GATE to ANODE voltage being approximately the same as the VCAP to ANODE voltage. By connecting VCAP to GATE the external MOSFETs,  $R_{DS(ON)}$  is minimized, reducing the power loss of the external MOSFET when forward currents are large.

##### 8.4.2.3 Reverse Current Protection Mode

For the LM74700-EP to operate in reverse current protection mode, the gate driver must be enabled as described in the [Gate Driver](#) section, and the current of the external MOSFET must be flowing from the drain to the source. When the ANODE to CATHODE voltage is typically less than –11 mV, reverse current protection mode is entered and the GATE pin is internally connected to the ANODE pin. The connection of the GATE to ANODE pin disables the external MOSFET. The body diode of the MOSFET blocks any reverse current from flowing from the drain to source.

## 9 Application and Implementation

### Note

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

### 9.1 Application Information

The LM74700-EP is used with N-Channel MOSFET controller in a typical reverse polarity protection application. The schematic for the 12-V battery protection application is shown in 図 9-1, where the LM74700-EP is used in series with a battery to drive the MOSFET Q1. The TVS is not required for the LM74700-EP to operate, but they are used to clamp the positive and negative voltage surges. The output capacitor,  $C_{OUT}$ , is recommended to protect the immediate output voltage collapse as a result of line disturbance.

### 9.2 Typical Application

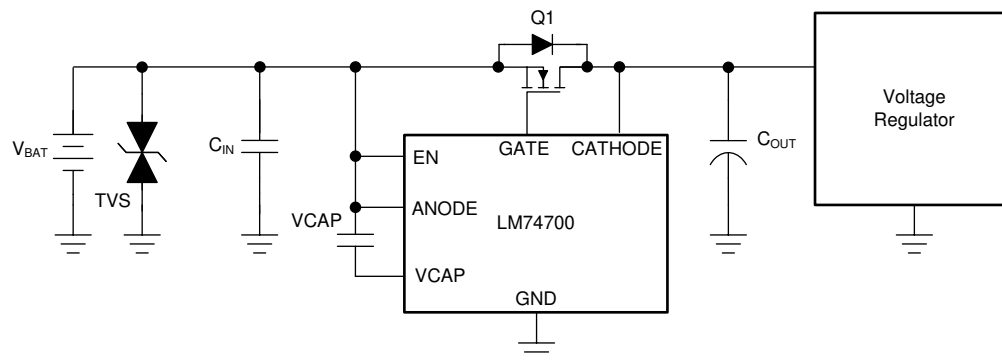


図 9-1. Typical Application Circuit

#### 9.2.1 Design Requirements

A design example, with system design parameters, is listed in 表 9-1.

表 9-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	12-V battery, 12-V nominal with 3.2-V cold crank and 35-V load dump
Output voltage	3.2 V during cold crank to 35-V load dump
Output current range	3-A nominal, 6-A maximum
Output capacitance	1-μF minimum, 220-μF typical hold up capacitance
Automotive EMC compliance	ISO 7637-2 and ISO 16750-2

#### 9.2.2 Detailed Design Procedure

##### 9.2.2.1 Design Considerations

- Input operating voltage range, including cold crank and load dump conditions
- Nominal load current and maximum load current

### 9.2.2.2 MOSFET Selection

The important MOSFET electrical parameters are the maximum continuous drain current,  $I_D$ , the maximum drain-to-source voltage,  $V_{DS(MAX)}$ , and the maximum source current through body diode and the drain-to-source On resistance  $R_{DS(ON)}$ .

The maximum continuous drain current,  $I_D$ , rating must exceed the maximum continuous load current. The maximum drain-to-source voltage,  $V_{DS(MAX)}$ , must be high enough to withstand the highest differential voltage seen in the application. This would include any anticipated fault conditions. TI recommends to use MOSFETs with voltage rating up to 60-V maximum with the LM74700-EP because anode-cathode maximum voltage is 65 V. The maximum  $V_{GS}$  LM74700-EP can drive is 13 V, so a MOSFET with 15-V minimum  $V_{GS}$  must be selected. If a MOSFET with < 15-V  $V_{GS}$  rating is selected, a zener diode can be used to clamp  $V_{GS}$  to safe level. During startup, inrush current flows through the body diode to charge the bulk hold-up capacitors at the output. The maximum source current through the body diode must be higher than the inrush current that can be seen in the application.

To reduce the MOSFET conduction losses, lowest possible  $R_{DS(ON)}$  is preferred, but selecting a MOSFET based on low  $R_{DS(ON)}$  can not always be beneficial. Higher  $R_{DS(ON)}$  will provide increased voltage information to LM74700-EP's reverse comparator at a lower reverse current. Reverse current detection is better with increased  $R_{DS(ON)}$ . TI recommends to operate the MOSFET in regulated conduction mode during nominal load conditions and select  $R_{DS(ON)}$ , such that at nominal operating current, forward voltage drop  $V_{DS}$  is close to 20-mV regulation point and not more than 50 mV.

As a guideline, TI suggests to choose  $(20 \text{ mV} / I_{Load(Nominal)}) \leq R_{DS(ON)} \leq (50 \text{ mV} / I_{Load(Nominal)})$ .

MOSFET manufacturers usually specify  $R_{DS(ON)}$  at 4.5-V  $V_{GS}$  and 10-V  $V_{GS}$ .  $R_{DS(ON)}$  increases drastically below 4.5-V  $V_{GS}$  and  $R_{DS(ON)}$  is highest when  $V_{GS}$  is close to MOSFET  $V_{th}$ . For stable regulation at light load conditions, TI recommends to operate the MOSFET close to 4.5-V  $V_{GS}$ , that is, much higher than MOSFET gate threshold voltage. TI recommends to choose MOSFET gate threshold voltage  $V_{th}$  of 2-V to 2.5-V maximum. Choosing a lower  $V_{th}$  MOSFET also reduces the turn ON time.

Based on the design requirements, preferred MOSFET ratings are:

- 60-V  $V_{DS(MAX)}$  and  $\pm 20$ -V  $V_{GS(MAX)}$
- $R_{DS(ON)}$  at 3-A nominal current:  $(20 \text{ mV} / 3 \text{ A}) \leq R_{DS(ON)} \leq (50 \text{ mV} / 3 \text{ A}) = 6.67 \text{ m}\Omega \leq R_{DS(ON)} \leq 16.67 \text{ m}\Omega$ .
- MOSFET gate threshold voltage  $V_{th}$ : 2-V maximum

DMT6007LFG MOSFET from Diodes Inc. is selected to meet this 12-V reverse battery protection design requirements and it is rated at:

- 60-V  $V_{DS(MAX)}$  and  $\pm 20$ -V  $V_{GS(MAX)}$
- $R_{DS(ON)}$  6.5-m $\Omega$  typical and 8.5-m $\Omega$  maximum rated at 4.5-V  $V_{GS}$
- MOSFET  $V_{th}$ : 2-V maximum

Thermal resistance of the MOSFET must be considered against the expected maximum power dissipation in the MOSFET to ensure that the junction temperature ( $T_J$ ) is well controlled.

### 9.2.2.3 Charge Pump VCAP, input and output capacitance

Minimum required capacitance for charge pump VCAP and input and output capacitance are:

- VCAP: Minimum 0.1  $\mu\text{F}$  is required; recommended value of VCAP ( $\mu\text{F}$ )  $\geq 10 \times C_{ISS(MOSFET)}(\mu\text{F})$
- $C_{IN}$ : minimum 22 nF of input capacitance
- $C_{OUT}$ : minimum 100 nF of output capacitance

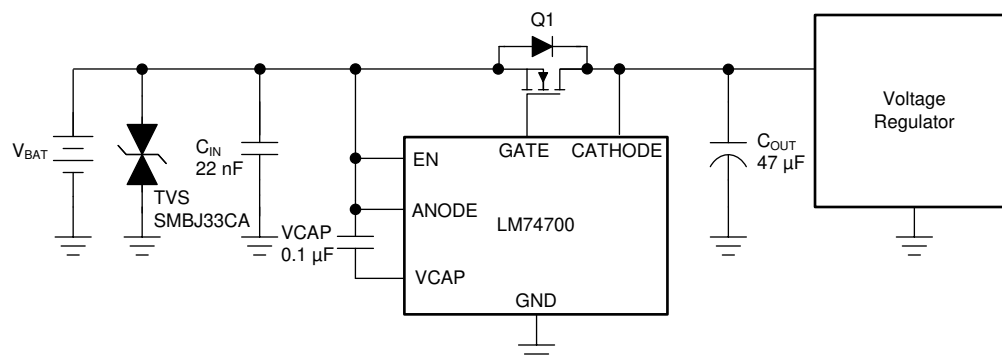
### 9.2.3 Selection of TVS Diodes for 12-V Battery Protection Applications

TVS diodes are used in automotive systems for protection against transients. In the 12-V battery protection application circuit shown in [Figure 9-2](#), a bi-directional TVS diode is used to protect from positive and negative transient voltages that occur during normal operation of the car and these transient voltage levels, and pulses are specified in ISO 7637-2 and ISO 16750-2 standards.



Two important specifications are breakdown voltage and clamping voltage of the TVS. Breakdown voltage is the voltage at which the TVS diode goes into avalanche similar to a zener diode and is specified at a low current value typical 1 mA and the breakdown voltage must be higher than worst case steady state voltages seen in the system. The breakdown voltage of the TVS+ must be higher than 24-V jump start voltage and 35-V suppressed load dump voltage and less than the maximum ratings of LM74700-EP (65 V). The breakdown voltage of TVS– must be beyond than maximum reverse battery voltage –16 V, so that the TVS– is not damaged due to long time exposure to reverse connected battery.

Clamping voltage is the voltage the TVS diode clamps in high current pulse situations and this voltage is much higher than the breakdown voltage. TVS diodes are meant to clamp transient pulses and must not interfere with steady state operation. In the case of an ISO 7637-2 pulse 1, the input voltage goes up to –150 V with a generator impedance of 10  $\Omega$ . This action translates to 15 A flowing through the TVS– and the voltage across the TVS would be close to its clamping voltage.



### 9-2. Typical 12-V Battery Protection With Single Bi-directional TVS

The next criterion is that the absolute maximum rating of Anode to Cathode reverse voltage of the LM74700-EP (–75 V) and the maximum  $V_{DS}$  rating MOSFET are not exceeded. In the design example, 60-V rated MOSFET is chosen and maximum limit on the cathode to anode voltage is 60 V.

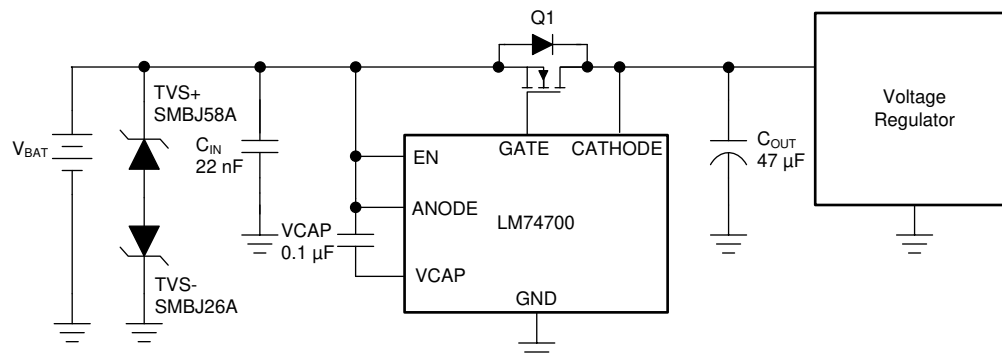
In case of ISO 7637-2 pulse 1, the anode of LM74700-EP is pulled down by the ISO pulse and clamped by TVS–. The MOSFET is turned off quickly to prevent reverse current from discharging the bulk output capacitors. When the MOSFET turns off, the cathode to anode voltage seen is equal to (TVS Clamping voltage + Output capacitor voltage). If the maximum voltage on output capacitor is 16-V (maximum battery voltage), then the clamping voltage of the TVS– must not exceed  $(60 \text{ V} - 16) \text{ V} = 44 \text{ V}$ .

The SMBJ33CA TVS diode can be used for 12-V battery protection application. The breakdown voltage of 36.7 V meets the jump start, load dump requirements on the positive side and 16-V reverse battery connection on the negative side. During ISO 7637-2 pulse 1 test, the SMBJ33CA clamps at –44 V with 15 A of peak surge current as shown in 9-5 and it meets the clamping voltage  $\leq 44 \text{ V}$ .

SMBJ series of TVS are rated up to 600-W peak pulse power levels. This rating is sufficient for ISO 7637-2 pulses and suppressed load dump (ISO-16750-2 pulse B).

#### 9.2.4 Selection of TVS Diodes and MOSFET for 24-V Battery Protection Applications

Typical 24-V battery protection application circuit shown in 9-3 uses two uni-directional TVS diodes to protect from positive and negative transient voltages.



**FIG 9-3. Typical 24-V Battery Protection With Two Uni-directional TVS**

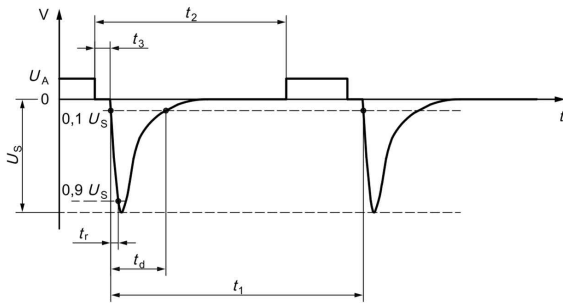
The breakdown voltage of the TVS+ must be higher than 48-V jump start voltage, less than the absolute maximum ratings of anode and enable pin of LM74700-EP (65 V) and must withstand 65-V suppressed load dump. The breakdown voltage of TVS- must be lower than maximum reverse battery voltage –32 V, so that the TVS- is not damaged due to long time exposure to reverse connected battery.

During ISO 7637-2 pulse 1, the input voltage goes up to –600 V with a generator impedance of 50 Ω. This action translates to 12 A flowing through the TVS-. The clamping voltage of the TVS- cannot be same as that of 12-V battery protection circuit. Because during the ISO 7637-2 pulse, the Anode to Cathode voltage seen is equal to (– TVS Clamping voltage + Output capacitor voltage). For 24-V battery application, the maximum battery voltage is 32 V, then the clamping voltage of the TVS- must not exceed 75 V – 32 V = 43 V.

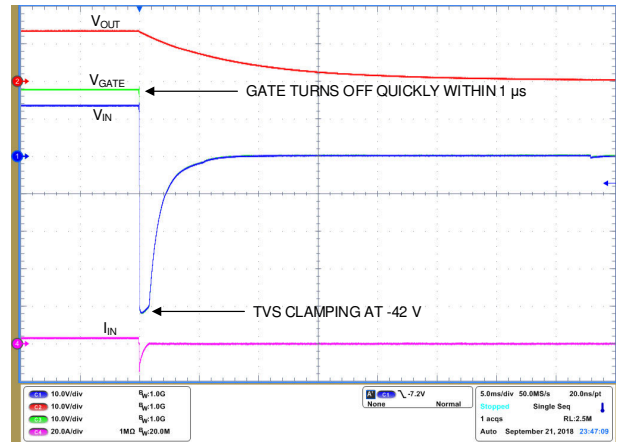
Single bi-directional TVS cannot be used for 24-V battery protection because breakdown voltage for TVS+ ≥ 65 V, maximum clamping voltage is ≤ 43 V and the clamping voltage cannot be less than the breakdown voltage. Two un-directional TVS connected back-to-back needs to be used at the input. For positive side TVS+, SMBJ58A with the breakdown voltage of 64.4 V (minimum), 67.8 (typical) is recommended. For the negative side TVS-, SMBJ26A with breakdown voltage close to 32-V (to withstand maximum reverse battery voltage –32 V) and maximum clamping voltage of 42.1 V is recommended.

For 24-V battery protection, a 75-V rated MOSFET is recommended to be used along with SMBJ26A and SMBJ58A connected back-to-back at the input.

## 9.2.5 Application Curves

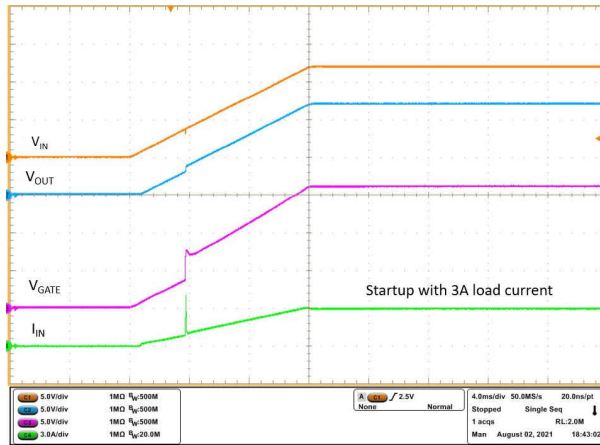


**9-4. ISO 7637-2 Pulse 1**



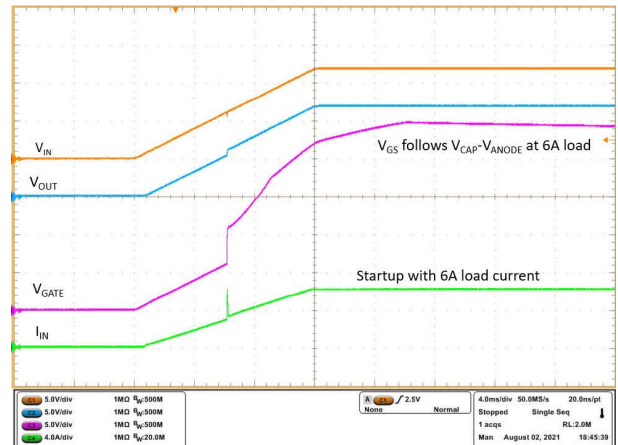
Time (5 ms/DIV)

**9-5. Response to ISO 7637-2 Pulse 1**



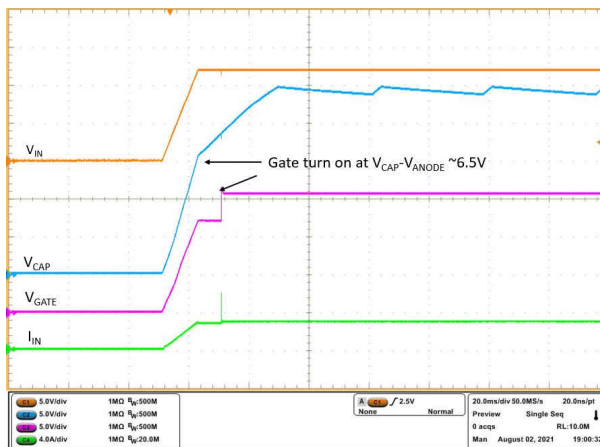
Time (4 ms/DIV)

**9-6. Startup With 3-A Load**



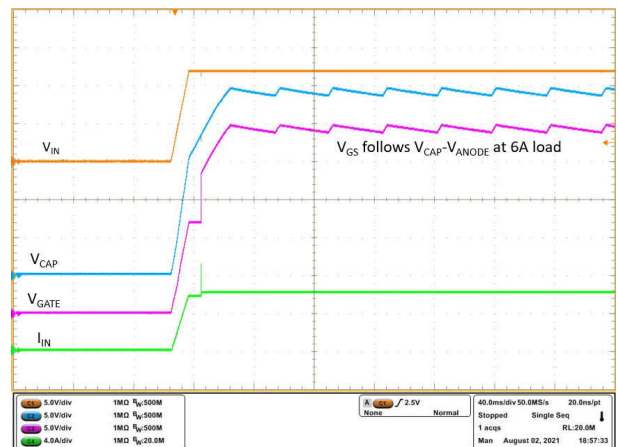
Time (4 ms/DIV)

**9-7. Startup With 6-A Load**



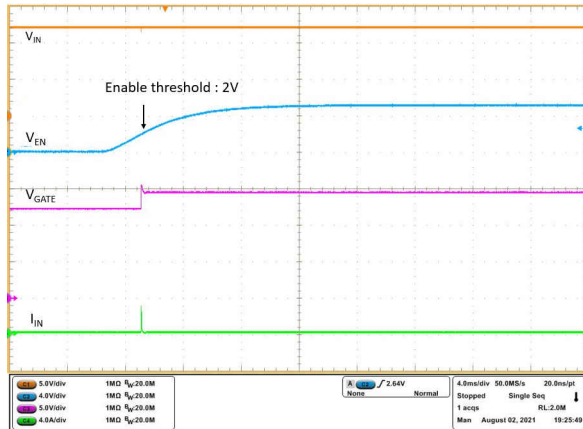
Time (20 ms/DIV)

**9-8. VCAP During Startup at 3-A Load**

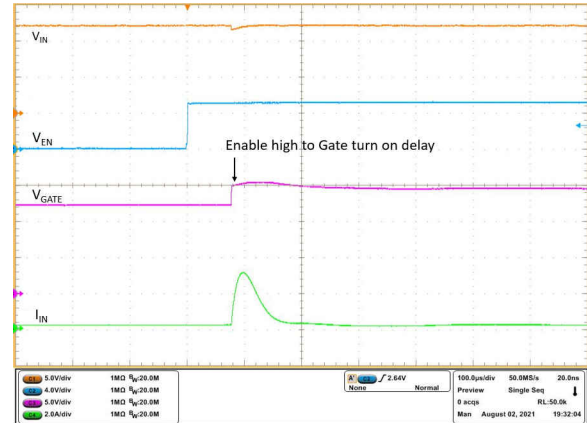


Time (40 ms/DIV)

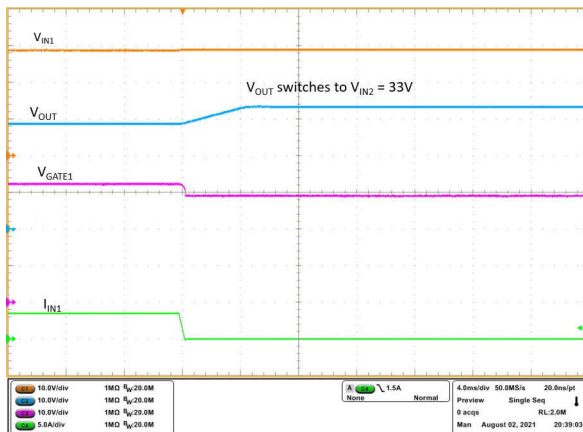
**9-9. VCAP During Startup at 6-A Load**




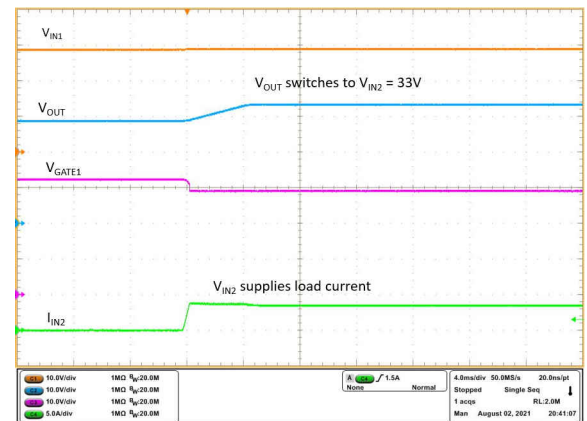
Time (4 ms/DIV)

 9-10. Enable Threshold


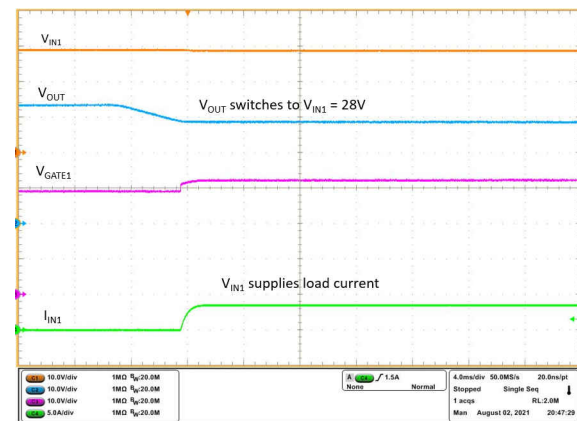
Time (100 μs/DIV)

 9-11. Enable Turn ON Delay


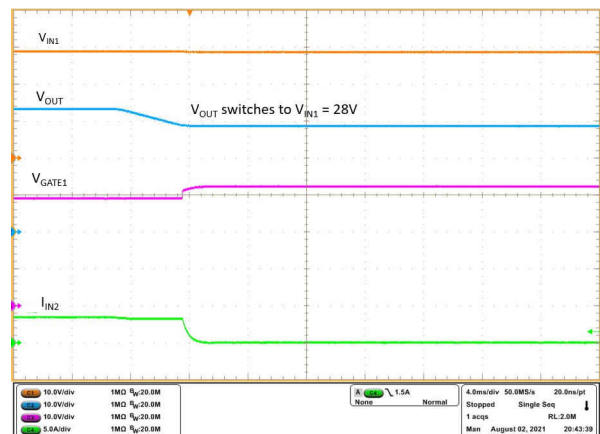
Time (4 ms/DIV)

 9-12. ORing  $V_{IN1}$  to  $V_{IN2}$  Switch Over


Time (4 ms/DIV)

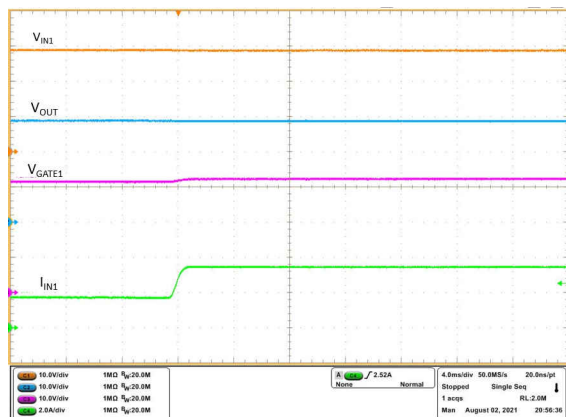
 9-13. ORing  $V_{IN1}$  to  $V_{IN2}$  Switch Over


Time (4 ms/DIV)

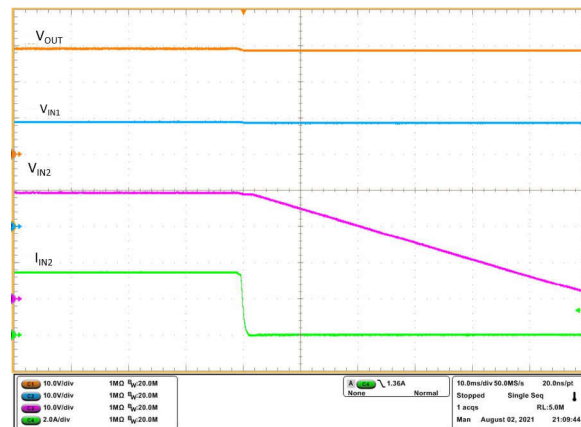
 9-14. ORing  $V_{IN2}$  to  $V_{IN1}$  Switch Over


Time (4 ms/DIV)

 9-15. ORing  $V_{IN2}$  to  $V_{IN1}$  Switch Over



**9-16. ORing –  $V_{IN2}$  Failure and Switch Over to  $V_{IN1}$**

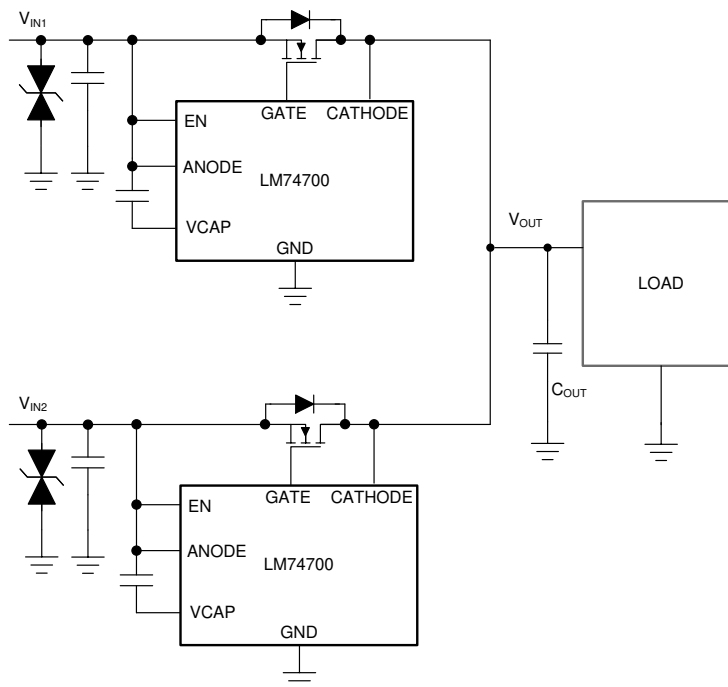


**9-17. ORing -  $V_{IN2}$  Failure and Switch Over to  $V_{IN1}$**

### 9.3 OR-ing Application Configuration

Basic redundant power architecture comprises of two or more voltage or power supply sources driving a single load. In its simplest form, the OR-ing solution for redundant power supplies consists of Schottky OR-ing diodes that protect the system against an input power supply fault condition. A diode OR-ing device provides effective and low cost solution with few components. However, the diodes forward voltage drops affects the efficiency of the system permanently, since each diode in an OR-ing application spends most of its time in forward conduction mode. These power losses increase the requirements for thermal management and allocated board space.

The LM74700-EP ICs combined with external N-Channel MOSFETs can be used in OR-ing Solution as shown in [9-18](#). The forward diode drop is reduced as the external N-Channel MOSFET is turned ON during normal operation. LM74700-EP quickly detects the reverse current, pulls down the MOSFET gate fast, leaving the body diode of the MOSFET to block the reverse current flow. An effective OR-ing solution needs to be extremely fast to limit the reverse current amount and duration. The LM74700-EP devices in OR-ing configuration constantly sense the voltage difference between Anode and Cathode pins, which are the voltage levels at the power sources ( $V_{IN1}$ ,  $V_{IN2}$ ) and the common load point respectively. The source to drain voltage  $V_{DS}$  for each MOSFET is monitored by the Anode and Cathode pins of the LM74700-EP. A fast comparator shuts down the Gate Drive through a fast pull-down within 0.45  $\mu$ s (typical) as soon as  $V_{(IN)} - V_{(OUT)}$  falls below -11 mV. The fast comparator turns on the Gate with 11-mA gate charge current once the differential forward voltage  $V_{(IN)} - V_{(OUT)}$  exceeds 50 mV.



**FIG 9-18. Typical OR-ing Application**

FIG 9-12 to FIG 9-15 show the smooth switch over between two power supply rails  $V_{IN1}$  at 28 V and  $V_{IN2}$  at 33 V. FIG 9-16 and FIG 9-17 illustrate the performance when  $V_{IN2}$  fails. LM74700-EP controlling  $V_{IN2}$  power rail turns off quickly, so that the output remains uninterrupted and  $V_{IN1}$  is protected from  $V_{IN2}$  failure.

## 10 Power Supply Recommendations

The LM74700-EP ideal diode controller is designed for the supply voltage range of  $3.2\text{ V} \leq V_{ANODE} \leq 65\text{ V}$ . If the input supply is located more than a few inches from the device, an input ceramic bypass capacitor higher than 22 nF is recommended. To prevent LM74700-EP and surrounding components from damage under the conditions of a direct output short circuit, it is necessary to use a power supply having over load and short circuit protection.

## 11 Layout

### 11.1 Layout Guidelines

- Connect ANODE, GATE and CATHODE pins of LM74700-EP close to the MOSFET's SOURCE, GATE and DRAIN pins.
- The high current path for this solution is through the MOSFET. Therefore, it is important to use thick traces for source and drain of the MOSFET to minimize resistive losses.
- The charge pump capacitor across VCAP and ANODE pins must be kept away from the MOSFET to lower the thermal effects on the capacitance value.
- The Gate pin of the LM74700-EP must be connected to the MOSFET gate with short trace. Avoid excessively thin and long trace to the Gate Drive.
- Keep the GATE pin close to the MOSFET to avoid increase in MOSFET turn-off delay due to trace resistance.
- Obtaining acceptable performance with alternate layout schemes is possible. However, the layout shown in [Figure 11-1](#) is intended as a guideline.

### 11.2 Layout Example

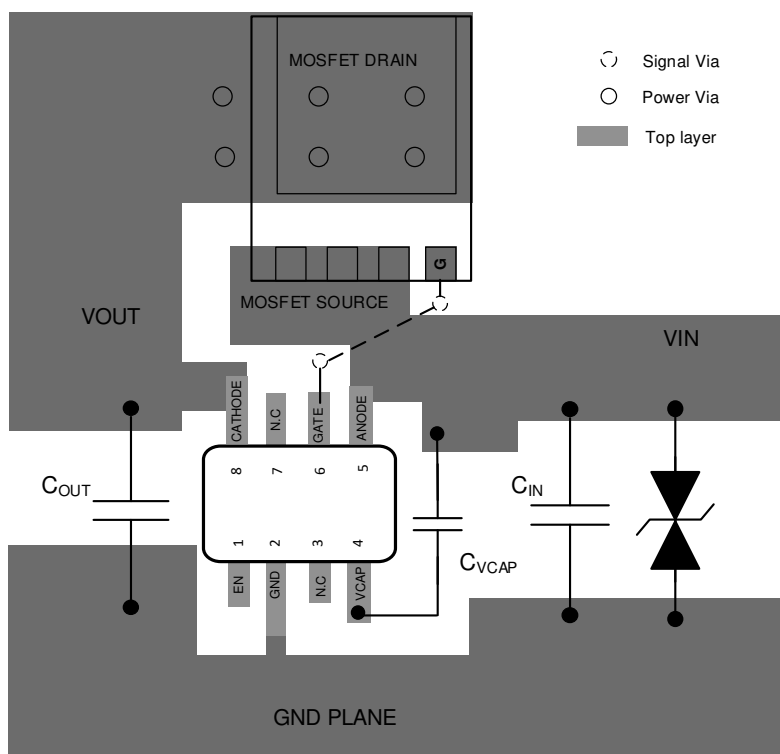


Figure 11-1. LM74700-EP DDF Package Layout Example



## 12 Device and Documentation Support

### 12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 12.2 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の[使用条件](#)を参照してください。

### 12.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

### 12.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 12.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM74700MDDFREP	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-50 to 125	EP747	<a href="#">Samples</a>
V62/21608	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-50 to 125	EP747	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

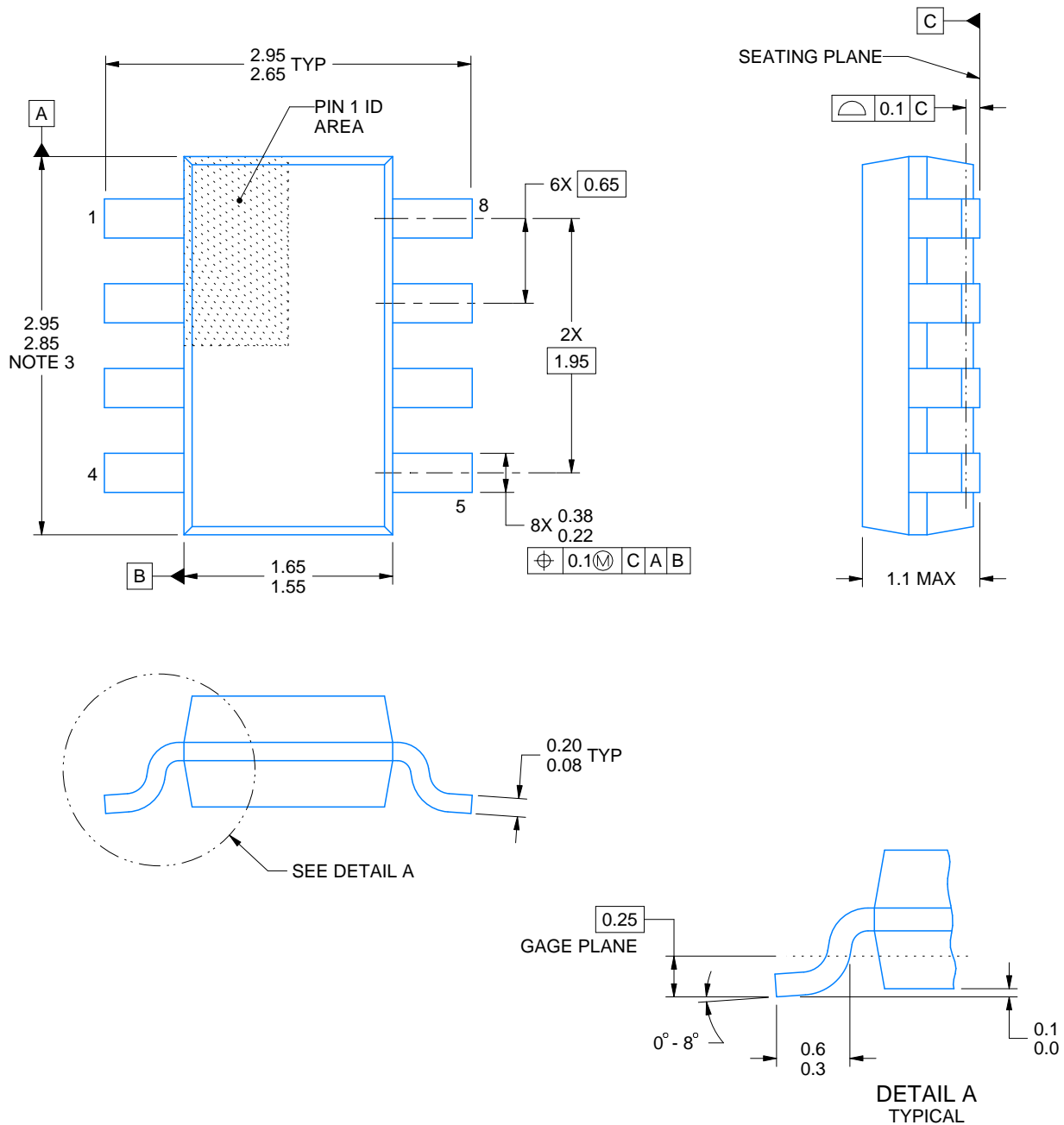
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF LM74700-EP :**

- Automotive : [LM74700-Q1](#)

**NOTE:** Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects



4222047/C 10/2022

## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

# EXAMPLE BOARD LAYOUT

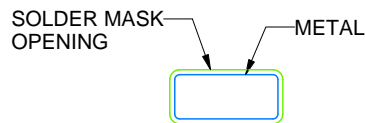
DDF0008A

SOT-23 - 1.1 mm max height

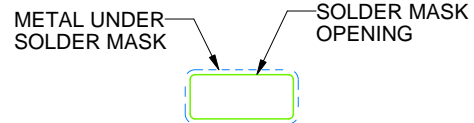
PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE  
SCALE:15X



NON SOLDER MASK  
DEFINED



SOLDER MASK  
DEFINED

SOLDER MASK DETAILS

4222047/C 10/2022

NOTES: (continued)

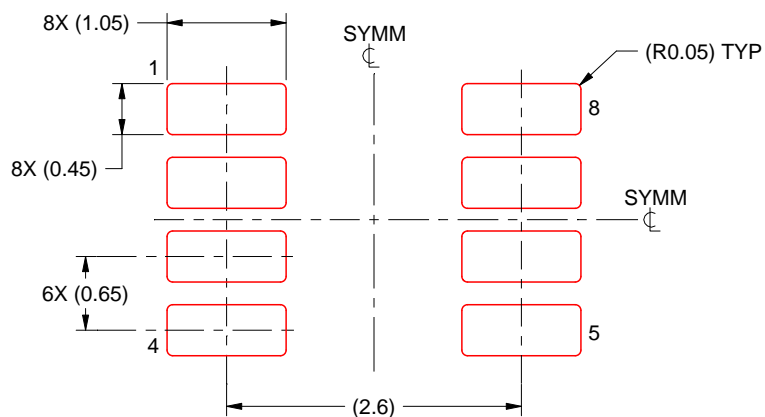
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DDF0008A

SOT-23 - 1.1 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4222047/C 10/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

## 重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス・デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとし、

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、[TI の販売条件](#)、または [ti.com](https://www.ti.com) やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、TI はそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2022, Texas Instruments Incorporated