TEXAS INSTRUMENTS
LMG3410R050, LMG3411R050
JAJSG97A – SEPTEMBER 2018 – REVISED MARCH 2019

LMG341xR050 過電流保護機能搭載、600V、50mΩ 統合型 GaN 出力段

1 特長

- TI の GaN プロセスは、加速信頼性アプリケーション内ハード・スイッチング・ミッション・プロファイルによる認定済み
- 高密度の電力変換設計が可能
  - カスコードまたはスタンドアロンの GaN FET で優れたシステム性能を実現
  - 低インダクタンスの 8mm×8mm QFN パッケージにより設計とレイアウトが容易
  - スイッチング性能と EMI 制御のため駆動強度を変更可能
  - デジタルのフォルト・ステータス出力信号
  - +12V の非レギュレート電源のみで動作可能
- 統合型ゲート・ドライバ
  - 共通ソース・インダクタンスが 0
  - 伝播遅延が 20ns で、MHz 動作が可能
  - ゲート・バイアス電圧をプロセスで調整することで高い信頼性を実現
  - スルー・レートを 25～100V/ns の範囲でユーザーが設定可能
- 堅牢な保護
  - 外付けの保護部品が不要
  - 応答時間 100ns 未満の過電流保護
  - 150V/ns を超えるスルー・レート耐性
  - 過渡過電圧耐性
  - 過熱保護
  - すべての電源レールの UVLO 保護
- 堅牢な保護
  - **LMG3410R050**:ラッチ付き過電流保護
  - **LMG3411R050**:サイクル単位の過電流保護

2 アプリケーション

- 高密度の産業用および民生用電源
- マルチレベル・コンバータ
- 太陽光インバータ
- 産業用モータ・ドライブ
- 無停電電源
- 高電圧バッテリ充電器

3 概要

ドライバおよび保護機能を内蔵した LMG341xR050 GaN 電力段を使うと、設計者はパワー・エレクトロニクス・システムにおいて、比類ない電力密度と効率を実現できます。シリコンMOSFETに対するLMG341xの本質的な利点には、入力および出力容量が非常に小さい、逆方向回復が0であるためスイッチング損失を約80%低減できる、スイッチ・ノードのリンギングが小さいためEMIが低減されるという事実が含まれます。これらの利点により、トーテムポールPFCのような高密度高効率のトポロジが可能になります。

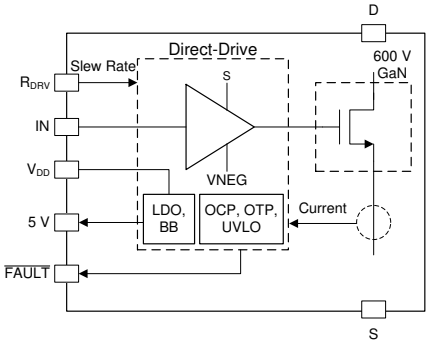
LMG341xR050 は、従来のカスコード GaN およびスタンドアロン GaN FET に代わる優れたデバイスで、組み込まれた一連の独自機能により、電源の設計を単純化し、信頼性を最大化し、性能を最適化できます。内蔵のゲート・ドライブにより、Vdsリンギングがほぼ0で100V/nsのスイッチングを行い、100ns未満の電流制限により意図しない貫通電流からデバイス自身を保護し、過熱シャットダウンにより熱暴走を防止し、システム・インターフェイス信号により自己監視を行えます。

製品情報(1)

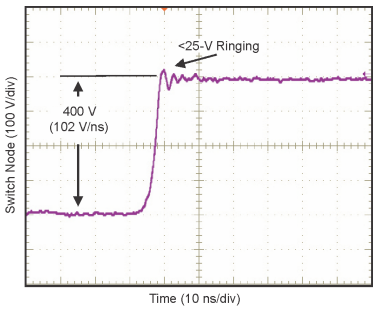
型番	パッケージ	本体サイズ(公称)
LMG341xR050	QFN (32)	8.00mm×8.00mm

(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

ブロック概略図



100V/nsを超えるスイッチング性能



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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

2018年9月発行のものから更新	**Page**
• LMG3411R050 デバイスを 追加	1

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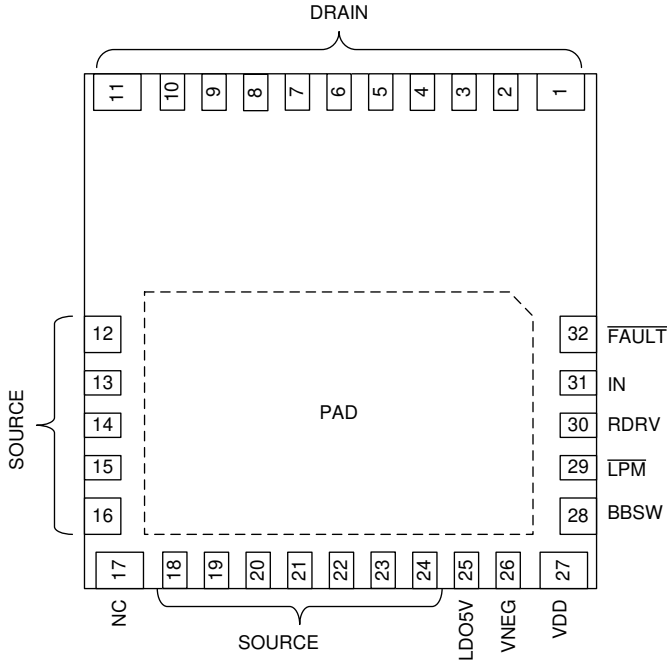
5 Pin Configuration and Functions

RWH (QFN) PACKAGE
32 PINS
(Top View)



Pin Functions

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
BBSW	28	P	Internal buck-boost converter switch pin. Connect an inductor from this point to source
DRAIN	1-11	P	Power transistor drain
$\overline{\text{FAULT}}$	32	O	Fault output, push-pull, active low
IN	31	I	CMOS-compatible non-inverting gate drive input
LDO5V	25	P	5-V LDO output for external digital isolator.
$\overline{\text{LPM}}$	29	I	Enables low-power-mode by connecting the pin to source
SOURCE	12-16, 18-24	P	Power transistor source, die-attach pad, thermal sink, signal ground reference
RDRV	30	I	Drive strength selection pin. Connect a resistor from this pin to ground to set the turn-on drive strength to control slew rate,
VDD	27	P	12-V power input, relative to source. Supplies 5-V rail and gate drive supply.
VNEG	26	P	Negative supply output, bypass to source with 2.2-µF capacitor
NC	17	—	Not connected, connect to source or leave floating.
PAD	—	P	Thermal Pad, tie to source with multiple vias.

(1) I = Input, O = Output, P = Power

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_{DS}	Drain-Source Voltage		600	V
$V_{DS(TR)}$ (2)	Transient Drain-Source Voltage		800	V
V_{DD}	Supply Voltage	–0.3	20	V
$I_{DS,pul}$ (3)	Drain-Source Current, Pulsed		130	A
V_{IN}	IN, $\overline{LPM}$ Pin Voltage	-0.3	5.5	V
V_{FAULT}	$\overline{FAULT}$ Pin Voltage	–0.3	5.5	V
T_{STG}	Storage Temperature	–55	150	°C
T_J	Operating Temperature	–40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) <1% duty cycle, <1us, for 1M pulses
(3) Pulse current <100ns

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±1000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DS}	Drain-Source Voltage			480	V
V_{DD}	Supply Voltage	9.5	12	18	V
I_{DS}	DC Drain-Source Current (T_j=125℃)			12	A
V_{IN}	IN, $\overline{LPM}$ Pin Voltage	3		5	V
I_{+5V}	LDO External Load Current			5	mA
R_{DRV}	Slew rate control resistor	15		150	kΩ
L_{DCDC}	DC-DC buck-boost converter output inductor		10		µH
C_{DCDC}	DC-DC buck/boost converter output capacitor		2.2		µF
T_J	Operating Temperature	-40		125	°C

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6.4 Thermal Information

THERMAL METRIC (1)		LMG341xR050 RWH (QFN) 32 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	26	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	5.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.5	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

6.5 Electrical Characteristics

over operating free-air temperature range, 9.5 V < V_{DD} < 18 V, LPM = 5 V, V_{NEG} = -14 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
GaN POWER TRANSISTOR						
$R_{DS,ON}$	On-state Resistance	T_J = 25°C		50		mΩ
		T_J = 125°C		78		
V_{SD}	Third-quadrant mode source-drain voltage	IN = 0 V, I_{SD} = 0.1 A		4.9		V
		IN = 0 V, I_{SD} = 10 A		6.8		
I_{dss}	Drain Leakage Current	V_{DS} =600V, T_J = 25°C		1		uA
		V_{DS} =600V, T_J = 125°C		10		
C_{oss}	GaN output capacitance	IN = 0 V, V_{DS} = 400 V, F_{SW} = 250 kHz		89		pF
$C_{oss,er}$	Effective output capacitance, energy related	IN = 0 V, V_{DS} =0-400 V		119		pF
$C_{oss,tr}$	Effective output capacitance, time related	I_D = 5 A, IN = 0 V, V_{DS} = 0-400 V		181		pF
Q_{rr}	Reverse recovery charge	V_R = 400 V, I_{SD} = 5 A, dI_{SD}/dt = 1 A/ns		0		nC
DRIVER SUPPLY						
$I_{VDD,LPM}$	Quiescent current, ultra-low-power mode	V_{LPM} = 0 V, V_{DD} = 12 V		80	95	µA
$I_{VDD,Q}$	Quiescent current (average)	Transistor held off, R_{DRV}=40 kΩ		0.5		mA
		Transistor held on, R_{DRV}=40 kΩ		0.5		
$I_{VDD,op}$	Operating current	V_{DD} = 12 V, F_{SW} = 500 KHz, R_{DRV}=40 kΩ, 50% duty cycle		27		mA
V_{+5V}	5V LDO output voltage	V_{DD} = 12 V	4.7		5.3	V
V_{NEG}	Negative Supply	30-mA load current		-13.9		V
BUCK BOOST CONVERTER						
$I_{DCDC,PK}$	Peak inductor current	I_{OUT} = 20 mA, V_{IN} = 12 V, V_{OUT} = -14 V		250	350	mA
ΔV_{NEG}	DC-DC output ripple voltage, pk-pk	C_{NEG} = 2.2 µF, I_{OUT} = 20 mA		50		mV
DRIVER INPUT						
V_{IH}	Input pin, $\overline{LPM}$ pin, logic high threshold				2.5	V
V_{IL}	Input pin, $\overline{LPM}$ pin, low threshold		0.8			V
V_{HYST}	Input pin, $\overline{LPM}$ pin, hysteresis			0.8		V
$R_{IN,L}$	Input pull-down resistance			150		kΩ
R_{LPM}	$\overline{LPM}$ pin pull-down resistance			150		kΩ

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Electrical Characteristics (continued)

over operating free-air temperature range, 9.5 V < V_{DD} < 18 V, LPM = 5 V, V_{NEG} = -14 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
UNDERVOLTAGE LOCKOUT						
$V_{DD,(ON)}$	V_{DD} turnon threshold	Turn-on voltage		9.1		V
$V_{DD,(OFF)}$	V_{DD} turnoff threshold	Turn-off voltage		8.5		V
$\Delta V_{DD,UVLO}$	UVLO Hysteresis			550		mV
FAULT						
I_{trip}	Current Fault Trip Point		40.4	60.8	77.6	A
T_{trip}	Temperature Trip Point	Trip point		165		°C
$T_{tripHys}$	Temperature Trip Hysteresis			20		°C

6.6 Switching Characteristics

over operating free-air temperature range, 9.5 V < V_{DD} < 18 V, V_{NEG} = -14 V, V_{BUS} = 400 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
GaN FET						
dv/dt	Turn-on Drain Slew Rate	R_{DRV} = 15 kΩ		100		V/ns
		R_{DRV} = 40 kΩ		50		
		R_{DRV} = 100 kΩ		25		
Δdv/dt	Slew Rate Variation	Turn on, I_L = 5 A, R_{DRV} = 40 kΩ		25		%
dv/dt	Edge Rate Immunity	Drain dv/dt, device remains off inductor-fed, max di/dt = 10 A/ns		150		V/ns
$f_{SW,GAN}$	FET switching frequency			0.5		MHz
STARTUP						
t_{START}	Startup Time, V_{IN} rising above UVLO	Time until gate responds to IN C_{NEG} = 2.2 µF, C_{LDO} = 1 µF		1		ms
DRIVER						
$t_{pd,on}$	Propagation delay, turn on	IN rising to I_{DS} > 1 A, V_{DS} = 400 V R_{DRV} = 15 kΩ, V_{NEG} = -14 V		18.5		ns
$t_{delay,on}$	Turn on delay time	I_{DS} > 1 A to V_{DS} < 320 V, I_D = 5 A, R_{DRV} = 15 kΩ		5.2		ns
$t_{VDS,ft}$	VDS fall time	V_{DS} = 320 V to V_{DS} = 80 V, I_D = 5 A, R_{DRV} = 15 kΩ		2.9		ns
$t_{pd,off}$	Propagation delay, turn off	IN falling to V_{DS} > 10 V,I_D = 5 A, R_{DRV} = 15 kΩ		25.3		ns
$t_{delay,off}$	Turn off delay time	V_{DS} = 10 V to V_{DS} = 80 V, I_D = 5 A, R_{DRV} = 15 kΩ		8.9		ns
$t_{VDS,rt}$	VDS rise time	V_{DS} = 80 V to V_{DS} = 320 V, I_D = 5 A, R_{DRV} = 15 kΩ		18		ns
FAULT						
t_{curr}	Current Fault Delay	I_{DS} > I_{TH} to $\overline{FAULT}$ low		50		ns
t_{blank}	Current Fault Blanking Time	V_{IN}>V_{IH} to end of blanking, RDRV=15kΩ		55		ns
t_{reset} (1)	Fault reset time	IN held low	250	350	500	µs

(1) Note: the reset time applies to the thermal-shut-down on both devices and the latched OCP on the LMG3410R050.

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7 Parameter Measurement Information

7.1 Switching Parameters

The circuit used to measure most switching parameters is shown in 図 1. The top LMG341xR050 in this circuit is used to re-circulate the inductor current and functions in third-quadrant mode only. The bottom device is the active device; it is turned on to increase the inductor current to the desired test current. The bottom device is then turned off and on to create switching waveforms at a specific inductor current. Both the drain current (at the source) and the drain-source voltage is measured. The specific timing measurement is shown in 図 2. It is recommended to use the half-bridge as double pulse tester. Excessive 3rd quadrant operation may over heat the top LMG341xR050.

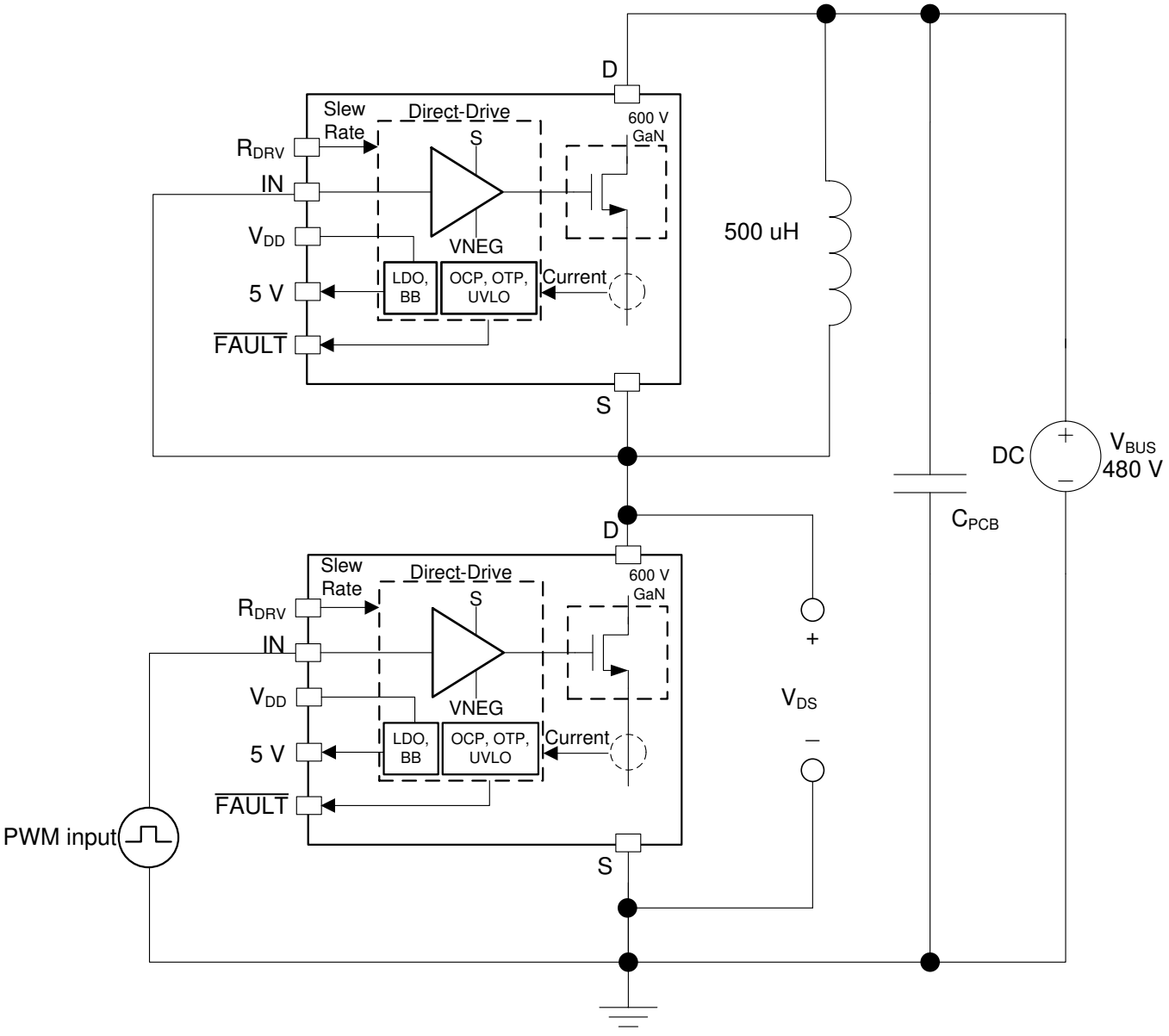

図 1. Circuit Used to Determine Switching Parameters

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Switching Parameters (continued)

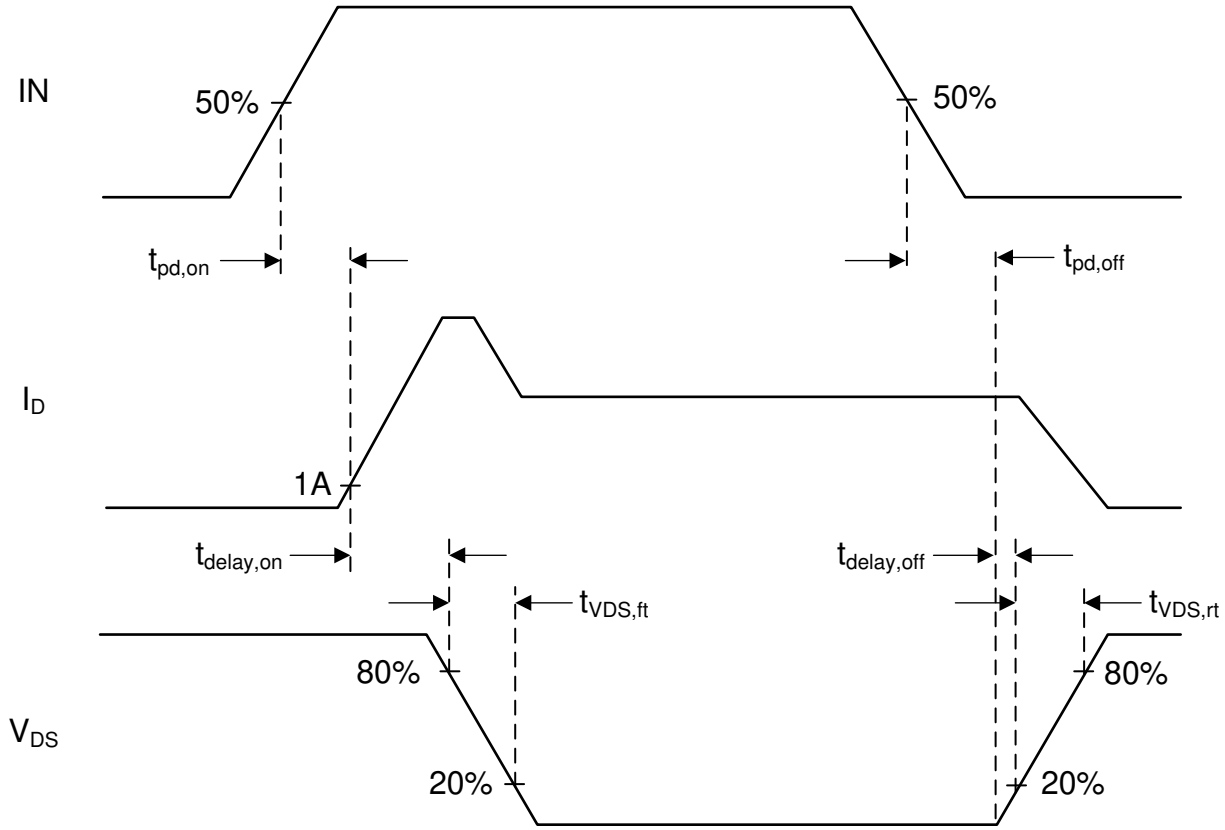

図 2. Measurement to Determine Propagation Delays and Slew Rates

7.1.1 Turn-on Delays

The timing of the turn-on transition has three components: propagation delay, turn-on delay and fall time. The first component is the propagation delay of the driver from when the input goes high to when the GaN FET starts turning on (represented by 1 A drain current). The turn-on delay is the delay from when the FET starts turning on to when the drain voltage swings down by 20 percent. Finally, the V_{DS} fall time is the time it takes the drain voltage to slew between 80 percent and 20 percent of the bus voltage. The drive-strength resistor value has a large effect on turn-on delay and V_{DS} fall time but does not affect the propagation delay significantly.

7.1.2 Turn-off Delays

The timing of the turn-off transition has three components: propagation delay, turn-off delay and rise time. The first component is the propagation delay of the driver from when the input goes low to when the GaN FET starts turning off. The turn-off delay is the delay from when the FET starts turning of (represented by the drain rising above 10 V) to when the drain voltage swings up by 20 percent. Finally, the V_{DS} rise time is the time it takes the drain voltage to slew between 20 percent and 80 percent of the bus voltage. The turn-off delays of the LMG341xR050 are independent of the drive-strength resistor but the turn-off delay and the V_{DS} rise time are heavily dependent on the load current.

7.1.3 Drain Slew Rate

The slew rate, measured in volts per nanosecond, is measured on the turn-on edge of the LMG341xR050. The slew rate is considered over the V_{DS} fall time, where the drain falls from 80 percent to 20 percent of the bus voltage. The drain slew rate is thus given by 60 percent of the bus voltage divided by the V_{DS} fall time. This drain slew rate is dependent on the RDRV value and is only slightly affected by drain current. Please refer to for the RDRV that is matched with the needed slew rate.

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8 Detailed Description

8.1 Overview

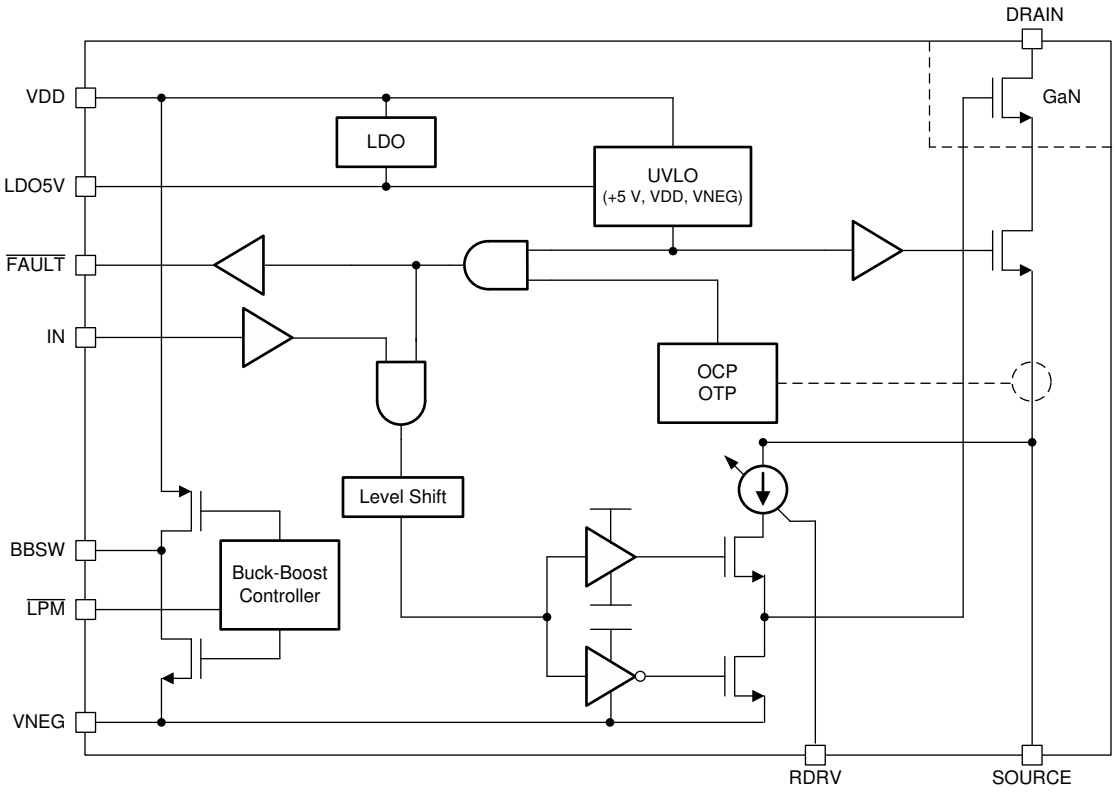
LMG341xR050 is a high-performance 600-V GaN transistor with integrated gate driver. The GaN transistor provides ultra-low input and output capacitance and zero reverse recovery. The lack of reverse recovery enables efficient operation in half-bridge and bridge-based topologies.

TI utilizes a Direct Drive architecture to control the GaN FET within the LMG341xR050. When the driver is powered up, the GaN FET is controlled directly with the integrated gate driver. This architecture provides superior switching performance compared with the traditional cascode approach.

The integrated driver solves a number of challenges using GaN devices. The LMG341xR050 contains a driver specifically tuned to the GaN device for fast driving without ringing on the gate. The driver ensures the device stays off for high drain slew rates up to 150 V/ns. In addition, the integrated driver protects against faults by providing overcurrent and overtemperature protection. This feature can protect the system in case of a device failure, or prevent a device failure in the case of a controller error or malfunction. LMG3410R050 and LMG3411R050 have the same design and features, except the handling of OCP events. LMG3410R050 adopts a latch-off strategy at OCP events, while LMG3411R050 can realize cycle-by-cycle current limit function. Please refer to Fault Detection for more details.

Unlike silicon MOSFETs, there is no p-n junction from source to drain in GaN devices. That is why GaN devices have no reverse recovery losses. However, the GaN device can still conduct from source to drain in 3rd quadrant of operation similar to a body diode but with higher voltage drop and higher conduction loss. 3rd quadrant operation can be defined as follows; when the GaN device is turned off and negative current pulls the drain node voltage to be lower than its source. The voltage drop across GaN device during 3rd quadrant operation is high; therefore, it is recommended to operate with synchronous switching and keep the duration of 3rd quadrant operation at minimum.

8.2 Functional Block Diagram



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8.3 Feature Description

The LMG341xR050 includes numerous features to provide increased switching performance and efficiency in customers' applications while providing an easy-to-use solution.

8.3.1 Direct-Drive GaN Architecture

The LMG341xR050 utilizes a series FET to ensure the GaN module stays off when V_{DD} is not applied. When this FET is off, the gate of the GaN transistor is held within a volt of the FET's source. As the silicon FET blocks the drain voltage, the V_{GS} of the GaN transistor decreases until it passes its threshold voltage. Then, the GaN transistor turns off and blocks the remaining drain voltage.

When the LMG341xR050 is powered up, the internal buck-boost converter generates a negative voltage (V_{NEG}) that is sufficient to directly turn off the GaN transistor. In this case, the silicon FET is held on and the GaN transistor is gated directly with the negative voltage. During operation, this removes the switching loss of silicon FET.

8.3.2 Internal Buck-Boost DC-DC Converter

An internal inverting buck-boost converter generates a regulated negative rail for the turn-off supply of the GaN device. The buck-boost converter is controlled by a peak current mode, hysteretic controller. In normal operation, the converter remains in discontinuous-conduction mode, but may enter continuous-conduction mode during startup and overload conditions. The converter is controlled internally and requires only a single surface-mount inductor and output bypass capacitor. For recommendations on the required passives, see *Buck-Boost Converter Design*.

8.3.3 Internal Auxiliary LDO

An internal low-dropout regulator is provided to supply external loads, such as digital isolators for the high-side drive signal. It is capable of delivering up to 5 mA to an external load. A bypass capacitor is recommended if using the rail externally, but is not required for LDO stability.

8.3.4 Fault Detection

The GaN driver includes built-in overcurrent protection (OCP), overtemperature protection (OTP) and under voltage lockout (UVLO).

8.3.4.1 Over-current Protection

The OCP circuit monitors the LMG341xR050's drain current and compares that current signal with an internally set limit. Upon detection of the over-current, the family of GaN FETs has two optional protection actions: 1) latched overcurrent protection; and 2) cycle-by-cycle overcurrent protection.

LMG3410R050 provides latched OCP option, by which the FET is shut off and held off until the fault is reset by either holding the IN pin low for more than 350 microseconds or removing power from VDD.

LMG3411R050 provides cycle-by-cycle OCP option. In this mode, the FET is also shut off when overcurrent happens, but the output fault signal will clear after the input PWM goes low. In the next cycle, the FET can turn on as normal. The cycle-by-cycle function can be used in cases where steady state operation current is below the OCP level but transient response can still reach high current, while the circuit operation cannot be paused. It also prevents the power stage from overheating by having overcurrent induced conduction loss.

During cycle-by-cycle operation, after the current reaches the upper limit but the PWM input is still high, the load current can flow through the third quadrant of the other FET of a half-bridge with no synchronous rectification. The extra high negative voltage drop (–6V to –8V) from drain to source could lead to high third quadrant loss, similar to dead time loss but with much longer time. An operation scheme of cycle-by-cycle current limitation is shown as 図 3. Therefore, it is critical to design the control scheme to make sure the number of switching cycles in cycle-by-cycle mode is limited, or to change PWM input based on the fault signal to shorten the time in third quadrant conduction mode of the power stage.

OCP circuit has a 20ns typical blanking time at slew rate of 100V/ns to prevent false triggering during switch node transitions. The blanking time increases with respect to lower slew rates accordingly since lower slew rates results in longer switching transition time. This fast response OCP circuit protects the GaN device even under a hard short-circuit condition.

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Feature Description (continued)

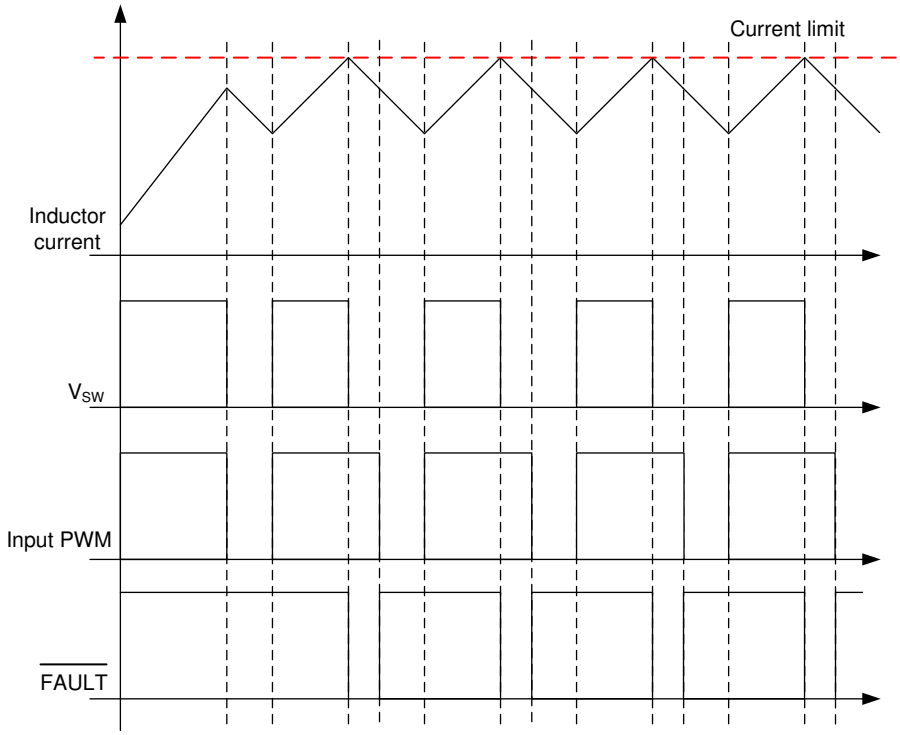

図 3. Cycle-by-cycle OCP Operation

8.3.4.2 Over-Temperature Protection and UVLO

The over-temperature protection circuit measures the temperature of the driver die and trips if the temperature exceeds the over-temperature threshold (typically 165 °C). Upon an over-temperature condition, the GaN device is held off and a fault is latched. To resume operation, the temperature must fall below the lower thermal shut down threshold and the input must be held low for typical 350 us to reset the latched fault.

The $\overline{FAULT}$ output is a push-pull output indicating the readiness and fault status of the driver. It is held low when starting up until the safety FET is turned on. In an OCP or OTP fault condition, it is held low until the fault latches are reset or fault is cleared. If the power supplies go below the UVLO thresholds, power transistor switching is disabled and $\overline{FAULT}$ is held low until the power supplies recover.

8.3.5 Drive Strength Adjustment

To allow for an adjustable slew rate to control stability and ringing in the circuit, as well as an adjustment to pass electro-magnetic compliance (EMC) standards, LMG341xR050 allows the user to adjust its drive strength. A resistor is connected the RDRV pin and ground. The value of the resistor determines the slew rate of the device during turn-on between 25V/ns and 100V/ns; The turn-off slew rate is dependent on the load current; therefore, it is not controlled.

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8.4 Device Functional Modes

8.4.1 Low-Power Mode

In some applications, it is important to reduce quiescent current during low power mode such as start up or burst. The LPM pin reduces the quiescent current to support low power modes. When LPM is pulled low, the supply current in the low-power mode is typically 80 µA. Once this pin is pulled high, the buck-boost converter will start up and LMG341xR050 will be ready to operate within 1 ms.

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The LMG341xR050 is a single-channel GaN power stage targeting high-voltage applications. It targets hard-switched and soft-switched applications running from a 350 V to 480 V bus such as power-factor correction (PFC) applications. As GaN devices such as the LMG341xR050 have zero reverse-recovery charge, they are well-suited for hard-switched half-bridge applications, such as the totem-pole bridgeless PFC circuit. It is also well-suited for resonant DC-DC converters, such as the LLC and phase-shifted full-bridge. As both of these converters utilize the half-bridge building block, this section will describe how to use the LMG341xR050 in a half-bridge configuration.

9.2 Typical Application

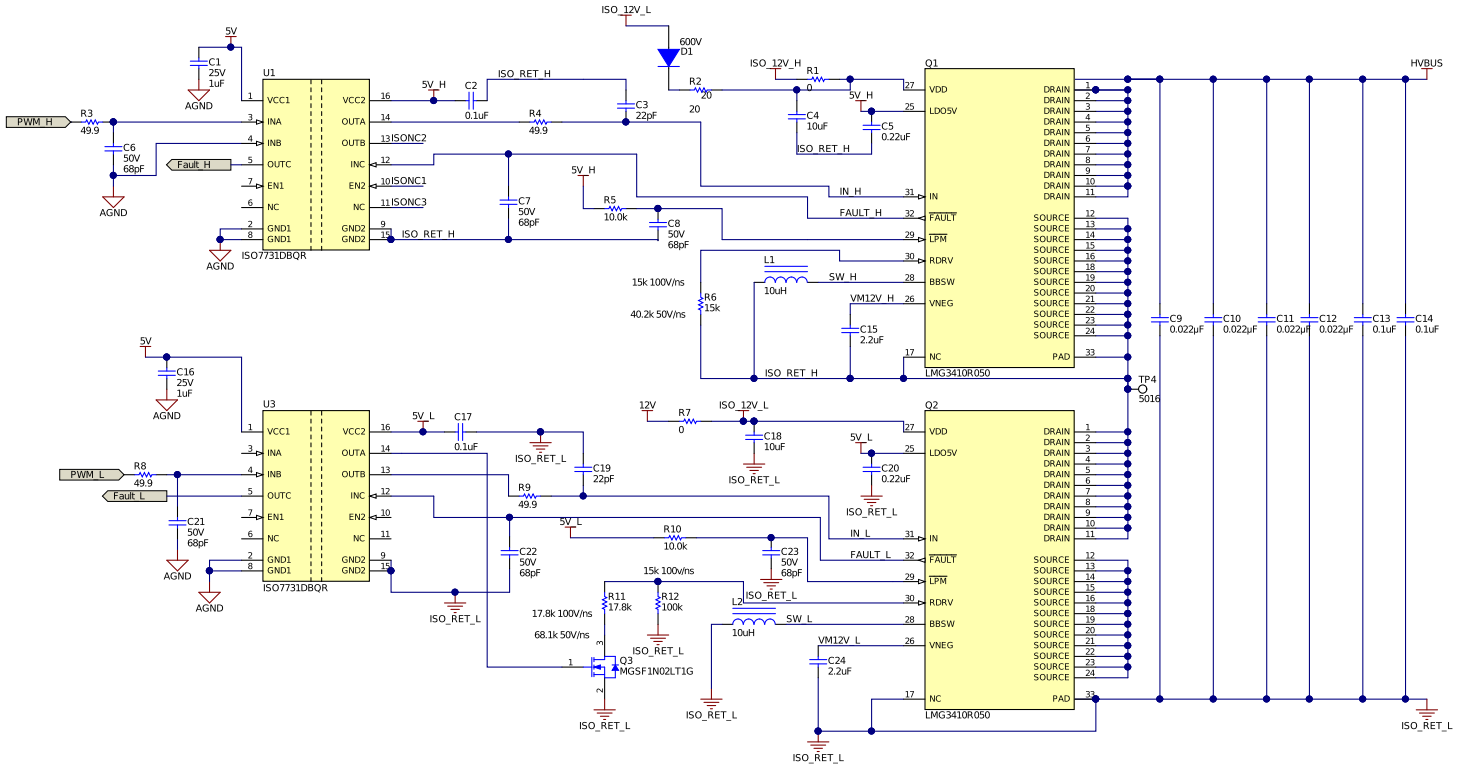

図 4. Typical Half-Bridge Application

9.2.1 Design Requirements

This design example is for a hard-switched boost converter which is representative of PFC applications. The system parameters considered are as follows.

表 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input Voltage	200 VDC
Output Voltage	400 VDC
Input (Inductor) Current	5 A
Switching Frequency	100 kHz

9.2.2 Detailed Design Procedure

In high-voltage power converters, correct circuit design and PCB layout is essential to obtaining a high-performance and even functional power converter. While the general procedure for designing a power converter is out of the scope of this document, this datasheet describes how to utilize the LMG341xR050 to build efficient, well-behaved power converters.

9.2.2.1 Slew Rate Selection

The LMG341xR050 supports slew rate adjustment through connecting a resistor from RDRV to source. The choice of RDRV will control the slew rate of the drain voltage of the device between approximately 25 V/ns and 100 V/ns. The slew rate adjustment is used to control the following aspects of the power stage:

- Switching loss in a hard-switched converter
- Radiated and conducted EMI generated by the switching stage
- Interference elsewhere in the circuit coupled from the switch node
- Voltage overshoot and ringing on the switch node due to power loop inductance and other parasitics

When increasing the slew rate, the switching power loss will decrease, as the portion of the switching period where the switch simultaneous conducts high current while blocking high voltage is decreased. However, by increasing the slew rate of the device, the other three aspects of the power stage get worse. Following the design recommendations in this datasheet will help mitigate the system-related challenges related to high slew rate. Ultimately, it is up to the power designer to ensure the chosen slew rate provides the best performance in his or her end application.

9.2.2.1.1 Startup and Slew Rate with Bootstrap High-Side Supply

Using a bootstrap supply for the high-side LMG341xR050 places additional constraints on the startup of the circuit. Before the high-side LMG341xR050 functions correctly, its VDD, LDO5V and VNEG power supplies must start up and be functional. Prior to the device powering up, the GaN device operates in cascode mode with reduced performance. In particular, under high drain slew rate (dv/dt), the transistor can conduct to a small extent and cause additional power dissipation. The correct startup procedure for a bootstrap-supplied half-bridge depends on the circuit used.

In a buck converter without pre-bias, where the initial output voltage is zero, the startup procedure is straightforward. In this case, before switching begins, turn on the low-side device to allow the high-side bootstrap transistor to charge up. When the $\overline{\text{FAULT}}$ signal goes high, the high-side device has powered up completely, and normal switching can begin.

In a boost converter or a buck converter with a pre-biased output, it is necessary to operate the circuit in switching PWM mode while the high-side LMG341xR050 is powering up. With a boost converter, if the low-side device is held on, the power inductor current will likely run away and the inductor will saturate. To start up a boost converter, the duty cycle has to be very low and gradually increase to charge the output to the desired value without the inductor current reaching saturation. This pulse sequence can be performed open-loop or using a current-mode controller. This startup mode is standard for boost-type converters.

However, with the LMG341xR050, during the boost converter startup, significant shoot-through current can occur for high drain slew rates while starting up. This shoot-through current is approximately 1.25 µC per switching event at 50 V/ns, and is comparable to a reverse-recovery event in a silicon MOSFET. If this shoot-through current is undesirable, the drain slew rate of the low-side device must be reduced during startup. In 図 4, the FAULT output from the high-side device is used to gate MOSFET Q1. When FAULT from the high-side is high, once the device is powered up, Q1 turns on and reduces the effective resistance connected to RDRV on the low-side LMG341xR050. With this circuit, the dv/dt of the low-side device can be held low to reduce power dissipation and reduce ringing during high-side startup, but then increase to reduce switching loss during normal operation.

9.2.2.2 Signal Level-Shifting

As the LMG341xR050 is a single-channel power stage, two devices are used to construct a half-bridge converter, such as the one shown in 図 4. A high-voltage level shifter or digital isolator must be used to provide signals to the high-side device. Using an isolator for the low-side device is optional but will equalize propagation delays between the high-side and low-side signal path, as well as providing the ability to use different grounds for the power stage and the controller. If an isolator is not used on the low-side device, the control ground and the power ground must be connected at the LMG341xR050, as described in *Layout Guidelines*, and nowhere else on the board. With the high current slew rate of the fast-switching GaN device, any ground-plane inductance common with the power path may cause oscillation or instability in the power stage without the use of an isolator.

Choosing a digital isolator for level-shifting is an important consideration for fault-free operation. Because GaN switches very quickly, exceeding 50 V/ns in hard-switching applications, isolators with high common-mode transient immunity (CMTI) are required. If an isolator suffers from a CMTI issue, it can output a false pulse or signal which can cause shoot-through. In addition, choosing an isolator that is not edge-triggered can improve circuit robustness. In an edge-triggered isolator, a high dv/dt event can cause the isolator to flip states and cause circuit malfunctioning.

On/off keyed isolators are preferred, such as the TI ISO78xxF series, as a high CMTI event would only cause a short (few nanosecond) false pulse, which can be filtered out. To allow for filtering of these false pulses, an R-C filter at the driver input is recommended to ensure these false pulses can be filtered. If issues are observed, values of 1 kΩ and 22 pF can be used to filter out any false pulses.

9.2.2.3 Buck-Boost Converter Design

The Buck-boost converter generates the negative voltage necessary to turn off the direct-drive GaN FET. While it is controlled internally, it requires an external power inductor and output capacitor. The converter is designed to use a 10 µH inductor and a 2.2 µF output capacitor. As the peak current of the buck-boost is limited to less than 350 mA, the inductor chosen must have a saturation current above 350 mA. A Wurth Elektronik 10 µH SMT inductor (74404020100) in a 0806 package is recommended. This inductor is connected between the BBSW pin and ground. A 2.2 µF, 25V 0805 bypass capacitor is required between V_{NEG} and ground. Due to the voltage coefficient of X7R capacitors, a 2.2 µF capacitor will provide the required minimum 1.0 µF capacitance when operating.

ADVANCE INFORMATION

9.2.3 Application Curves

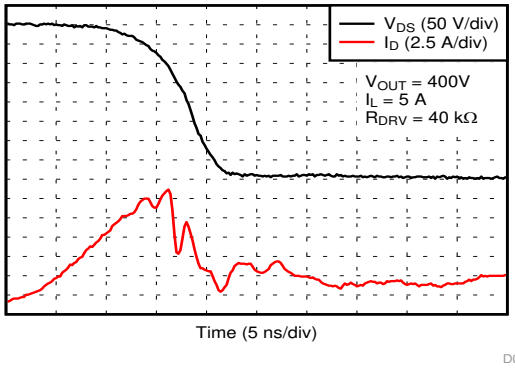

図 5. Turn-on Waveform in Application Example

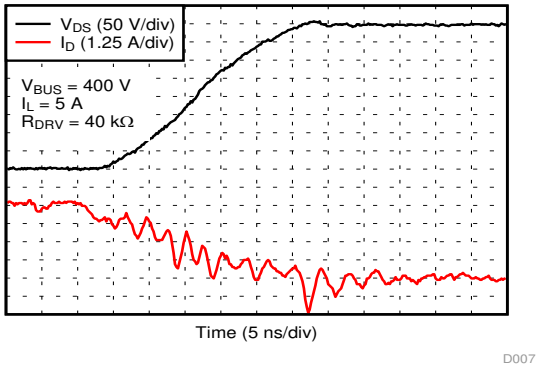

図 6. Turn-off Waveform in Application Example

9.3 Paralleling GaN Devices

LMG341xR050s can be paralleled directly in soft-switching applications. As for hard-switching applications, small decoupling inductors should be utilized to parallel the two half-bridge LMG341xR050s. This type of setup prevents current and thermal unbalances among the parallel devices due to any propagation delay and gate-source threshold voltage mismatches, and other factors.

9.4 Do's and Don'ts

The successful use of GaN devices in general and the LMG341xR050 in particular depends on proper use of the device. When using the LMG341xR050, **DO**:

- Read and fully understand the datasheet, including the application notes and layout recommendations
- Use a four-layer board and place the return power path on an inner layer to minimize power-loop inductance
- Use small, surface-mount bypass and bus capacitors to minimize parasitic inductance
- Use the proper size decoupling capacitors and locate them close to the IC as described in the *Layout Guidelines* section
- Use a signal isolator to supply the input signal for the low side device. If not, ensure the signal source is connected to the signal GND plane which is tied to the power source **only** at the LMG341xR050 IC
- Use the $\overline{\text{FAULT}}$ pin to determine power-up state and to detect overcurrent and overtemperature events and safely shut off the converter.

To avoid issues in your system when using the LMG341xR050, **DON'T**:

- Use a single-layer or two-layer PCB for the LMG341xR050 as the power-loop and bypass capacitor inductances will be excessive and prevent proper operation of the IC
- Reduce the bypass capacitor values below the recommended values
- Allow the device to experience drain transients above 600 V as they may damage the device
- Allow significant third-quadrant conduction when the device is OFF or unpowered, which may cause overheating. Self-protection feature cannot protect the device in this mode of operation
- Ignore the $\overline{\text{FAULT}}$ pin output.

ADVANCE INFORMATION

10 Power Supply Recommendations

The LMG341xR050 requires an unregulated 12-V supply to power its internal driver and fault protection circuitry. The low-side supply can be supplied from the local controller supply. The high-side device's supply must come from an isolated supply or bootstrap supply.

10.1 Using an Isolated Power Supply

Using an isolated power supply to power the high-side device has the advantage that it will work regardless of continued power-stage switching or duty cycle. It can also power the high-side device before power-stage switching begins, eliminating the power-loss concern of switching with an unpowered LMG341xR050 (see *Startup and Slew Rate with Bootstrap High-Side Supply* for details). Finally, a properly-selected isolated supply will contribute fewer parasitics to the switching power stage, increasing power-stage efficiency. However, the isolated power supply solution is larger and more expensive than the bootstrap solution.

The isolated supply can be constructed from an output of a flyback or FlyBuck™ converter, or using an isolated power module. When using an unregulated supply, ensure that the input to the LMG341xR050 does not exceed the maximum supply voltage. If necessary, a 18 V zener to clamp the VDD voltage supplied by the isolated power converter. Minimizing the inter-winding capacitance of the isolated power supply or transformer is necessary to reduce switching loss in hard-switched applications.

10.2 Using a Bootstrap Diode

When used in a half-bridge configuration, a floating supply is necessary for the top-side switch. Due to the switching performance of LMG341xR050, *a transformer-isolated power supply is recommended*. With caution, a bootstrap supply can be used with the recommendations in this section.

10.2.1 Diode Selection

LMG341xR050 has no reverse-recovery charge and little output charge. Hard-switched circuits using LMG341xR050 also exhibit high voltage slew rates. A compatible bootstrap diode must exhibit low output charge and, if used in a hard-switching circuit, very low reverse-recovery charge.

For soft-switching applications, the MCC UFM15PL ultra-fast silicon diode can be used. The output charge of 2.7 nC is small in comparison with the switching transistors, so it will have little influence on switching performance. In a hard-switching application, the reverse recovery charge of the silicon diode may contribute an additional loss to the circuit.

For hard-switched applications, a silicon carbide diode can be used to avoid reverse-recovery effects. The Cree C3D1P7060Q SiC diode has an output charge of 4.5 nC and a reverse recovery charge of about 5 nC. There will be some losses using this diode due to the output charge, but these will not dominate the switching stage's losses.

10.2.2 Managing the Bootstrap Voltage

In a synchronous buck, totem-pole PFC, or other converter where the low-side switch occasionally operates in third-quadrant mode, it is important to consider the bootstrap supply. During the dead time, the bootstrap supply charges through a path that includes the third-quadrant voltage drop of the low-side LMG341xR050. This third-quadrant drop can be large, which may over-charge the bootstrap supply in certain conditions. The V_{DD} supply of LMG341xR050 must not exceed 18 V in bootstrap operation.

Using a Bootstrap Diode (continued)

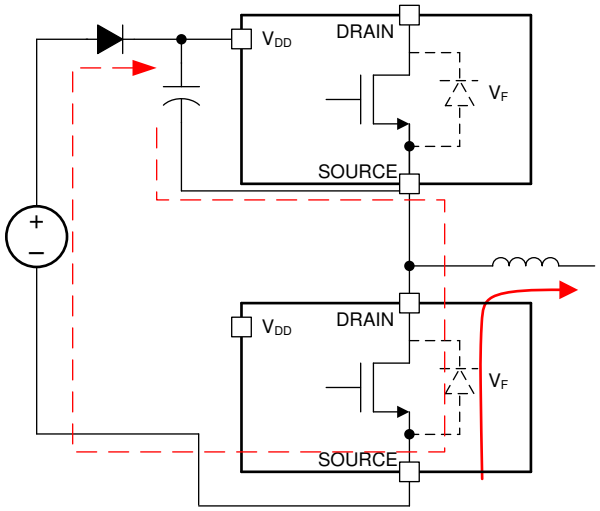

図 7. Charging Path for Bootstrap Diode

The recommended bootstrap supply connection includes a bootstrap diode and a series resistor with an optional zener as shown in 図 8. The series resistor limits the charging current at startup and when the low-side device is operating in third-quadrant mode. This resistor must be chosen to allow sufficient current to power the LMG341xR050 at the desired operating frequency. At 100 kHz operation, a value of approximately 5.1 ohms is recommended. At higher frequencies, this resistor value should be reduced or the resistor omitted entirely to ensure sufficient supply current.

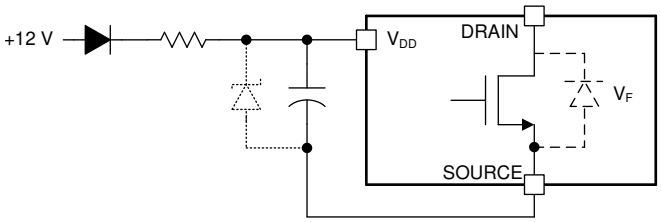

図 8. Suggested Bootstrap Regulation Circuit

Using a series resistor with the bootstrap supply will create a charging time constant in conjunction with the bypass capacitance on the order of a microsecond. When the dead time, or third-quadrant conduction time, is much lower than this time constant, the bootstrap voltage will be well-controlled and the optional zener clamp in 図 8 will not be necessary. If a large deadtime is needed, a 14-V zener diode can be used in parallel with the V_{DD} bypass capacitor to prevent damaging the high-side LMG341xR050.

10.2.3 Reliable Bootstrap Start-up

In some applications such as boost converter, the low side LMG341xR050 may need to start switching at high frequency while high side LMG341xR050 is not fully biased. If low side GaN device turn-on speed is adjusted to achieve high slew rate, the high side GaN device can turn-on unintentionally as high dv/dt can charge high side GaN device drain to source capacitance. For reliable operation, the slew rate should be slowed down to 30 V/ns by changing the resistance of RDRV pin of the low side LMG341xR050 until high side LMG341xR050's bias is fully settled. This can be monitored through the FAULT output of high side LMG341xR050 as given in 図 4.

11 Layout

11.1 Layout Guidelines

The layout of the LMG341xR050 is critical to its performance and functionality. Because the half-bridge configuration is typically used with these GaN devices, layout recommendations will be considered with this configuration. A four-layer or higher layer count board is required to reduce the parasitic inductances of the layout to achieve suitable performance.

11.1.1 Power Loop Inductance

The power loop, comprising the two devices in the half bridge and the high-voltage bus capacitance, undergoes large *di/dt* during switching events. By minimizing the inductance of this loop, ringing and electro-magnetic interference (EMI) can be reduced, as well as reducing voltage stress on the devices.

This loop inductance is minimized by locating the power devices as close together as possible. The bus capacitance is positioned in line with the two devices, either below the low-side device or above the high-side device, on the same side of the PCB. The return path (PGND in this case) is located on the second layer on the PCB in close proximity to the top layer. By using an inner layer and not the bottom layer, the vertical dimension of the loop is reduced, thus minimizing inductance. A large number of vias near both the device terminal and bus capacitance carries the high-frequency switching current to the inner layer while minimizing impedance.

11.1.2 Signal Ground Connection

The LMG341xR050's SOURCE pin is also signal ground reference. The signal GND plane should be connected to SOURCE with low impedance kelvin connection. In addition, the return path for the passives associated to the driver (e.g. bypass capacitance) must be connected to the GND plane. In 図 9, local signal GND planes are located on the second copper layer to act as the return for the local circuitry. The local signal GND planes are isolated from the high-current SOURCE plane except the kelvin connection at the source pin through enough low impedance vias.

11.1.3 Bypass Capacitors

The gate drive loop impedance must also be minimized to yield strong performance. Although the gate driver is integrated on package, the bypass capacitance for the driver is placed externally on the PCB board. As the GaN device is turned off to a negative voltage, the impedance of the negative source is included in the crucial turn-off path. As the critical hold-off path passes through this external bypass capacitor attached to V_{NEG}, this capacitor must be located close to the LMG341xR050. In the 図 9, V_{NEG} bypass capacitors C9 and C26 are located immediately adjacent to the pins on the IC with a direct connection to the SOURCE pin.

The bypass capacitors for the input supply (C8 and C23) and the 5V regulator (C5 and C7) must also be located immediately next to the IC with a close connection to the ground plane.

11.1.4 Switch-Node Capacitance

GaN devices have very low output capacitance and switch quickly with a high *dv/dt*, yielding very low switching loss. To preserve this low switching loss, additional capacitance added to the output node must be minimized. The PCB capacitance at the switch node can be minimized by following these guidelines:

- Minimize overlap between the switch-node plane and other power and ground planes
- Narrow the GND return path under the high-side device somewhat while still maintaining a low-inductance path
- Choose high-side isolator ICs and the isolated high-side supply or bootstrap diode with low capacitance
- Locate the power inductor as close to the power stage as possible
- Power inductors should be constructed with a single-layer winding to minimize intra-winding capacitance
- If a single-layer inductor is not possible, consider placing a small inductor between the primary inductor and the power stage to effectively shield the power stage from the additional capacitance
- If a back-side heat-sink is used, restrict the switch-node copper coverage on the bottom copper layer to the minimum area necessary to extract the needed heat

Layout Guidelines (continued)

11.1.5 Signal Integrity

The control signals to the LMG341xR050 must be protected from the high *dv/dt* that the GaN power stage produces. Coupling between the control signals and the drain may cause circuit instability and potential destruction. Route the control signals (IN, FAULT and LPM) over a ground plane located on an adjacent layer. For example, in the layout in 図 9, all the signals are routed on the top layer directly over the signal GND plane on the first inner copper layer.

The signals for the high-side device are often particularly vulnerable. Coupling between these signals and system ground planes could cause issues in the circuit. Keep the traces associated with the control signals away from drain copper. Shielding traces adjacent to the signal traces can be useful to minimize parasitic coupling. For the high-side level shifter, ensure no copper from either the input or output side extends beneath the isolator or the device's CMTI may be compromised.

11.1.6 High-Voltage Spacing

Circuits using the LMG341xR050 involve high voltage, potentially up to 600V. When laying out circuits using the LMG341xR050, understand the creepage and clearance requirements in your application and how they apply to the power stage. Functional (or working) isolation is required between the source and drain of each transistor, and between the high-voltage power supply and ground. Functional isolation or perhaps stronger isolation (such as reinforced isolation) may be required between the input circuitry to the LMG341xR050 and the power controller. Choose signal isolators and PCB spacing (creepage and clearance) distances which meet your isolation requirements.

If a heatsink is used to manage thermal dissipation of the LMG341xR050, ensure necessary electrical isolation and mechanical spacing is maintained between the heatsink and the PCB.

11.1.7 Thermal Recommendations

The LMG341xR050 is a lateral transistor grown on a Si substrate. The thermal pad is connected to the Source node. The LMG341xR050 may be used in applications with significant power dissipation, for example, hard-switched power converters. In these converters, cooling using just the PCB may not be sufficient to keep the part at a reasonable temperature. To improve the thermal dissipation of the part, TI recommends a heatsink is connected to the back of the PCB to extract additional heat. Using power planes and numerous thermal vias, the heat dissipated in the LMG341xR050(s) can be spread out in the PCB and effectively passed to the other side of the PCB. A heat sink can be applied to bare areas on the back of the PCB using an adhesive thermal interface material (TIM). The soldermask from the back of the board underneath the heatsink can be removed for more effective heat removal.

Please refer to the *High Voltage Half Bridge Design Guide for LMG3410 Smart GaN FET* and *Thermal Considerations for Designing a GaN Power Stage* application note for more recommendations and performance data on thermal layouts.

11.2 Layout Example

Correct layout of the LMG341xR050 and its surrounding components is essential for correct operation. The layout shown here reflects the power stage schematic in 図 4. It may be possible to obtain acceptable performance with alternate layout schemes, however this layout has been shown to produce good results and is intended as a guideline.

Layout Example (continued)

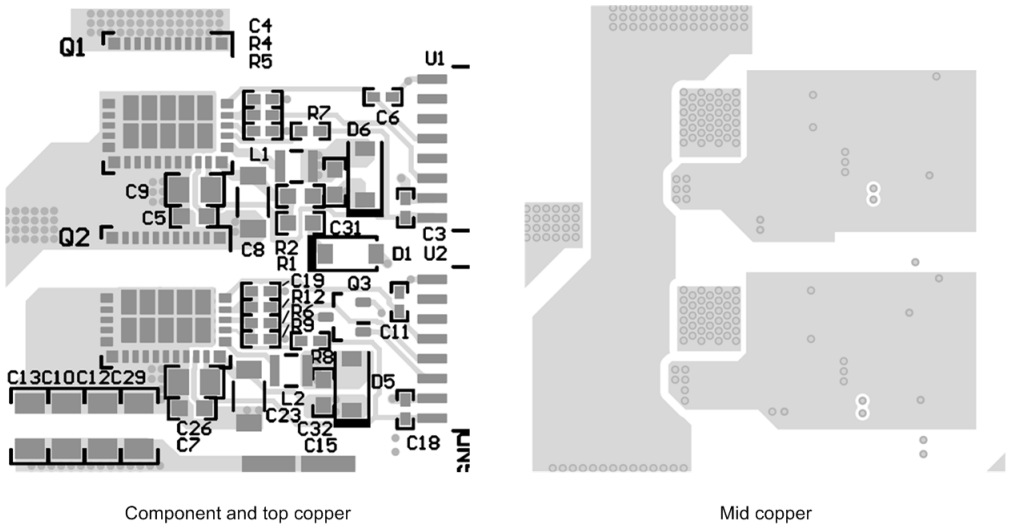

図 9. Example Half-Bridge Layout

ADVANCE INFORMATION

12 デバイスおよびドキュメントのサポート

12.1 デバイス・サポート

12.1.1 デベロッパー・ネットワークの製品に関する免責事項

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12.2 ドキュメントのサポート

12.2.1 関連資料

*『LMG3410xスマートGaN FETの高電圧ハーフブリッジ設計ガイド』*アプリケーション・レポート

12.3 ドキュメントの更新通知を受け取る方法

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12.4 コミュニティ・リソース

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMG3410R050RWHR	ACTIVE	VQFN	RWH	32	2000	RoHS-Exempt & Green	NIPDAU	Level-3-260C-168HRS	-40 to 150	LMG3410 R050	Samples
LMG3410R050RWHT	ACTIVE	VQFN	RWH	32	250	RoHS-Exempt & Green	NIPDAU	Level-3-260C-168HRS	-40 to 150	LMG3410 R050	Samples
LMG3411R050RWHR	ACTIVE	VQFN	RWH	32	2000	RoHS-Exempt & Green	NIPDAU	Level-3-260C-168HRS	-40 to 150	LMG3411 R050	Samples
LMG3411R050RWHT	ACTIVE	VQFN	RWH	32	250	RoHS-Exempt & Green	NIPDAU	Level-3-260C-168HRS	-40 to 150	LMG3411 R050	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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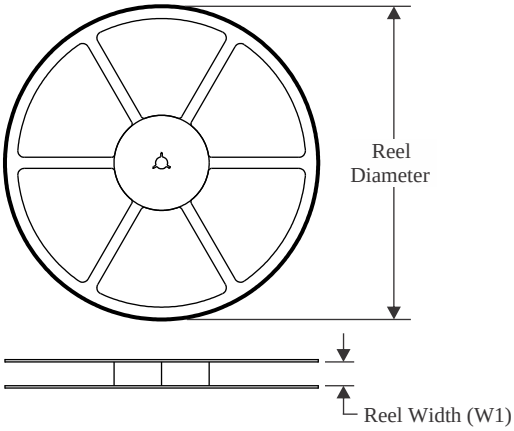
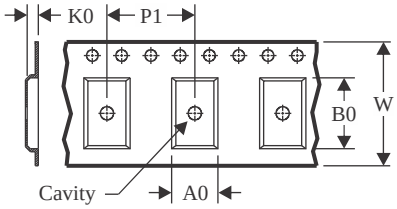
TAPE AND REEL INFORMATION

REEL DIMENSIONS

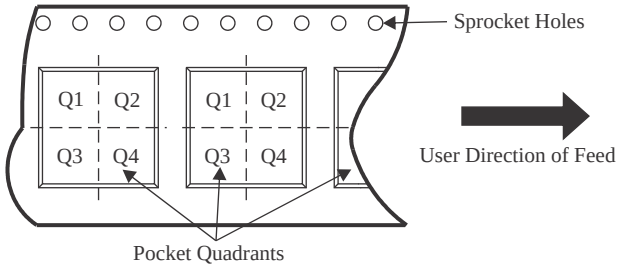


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

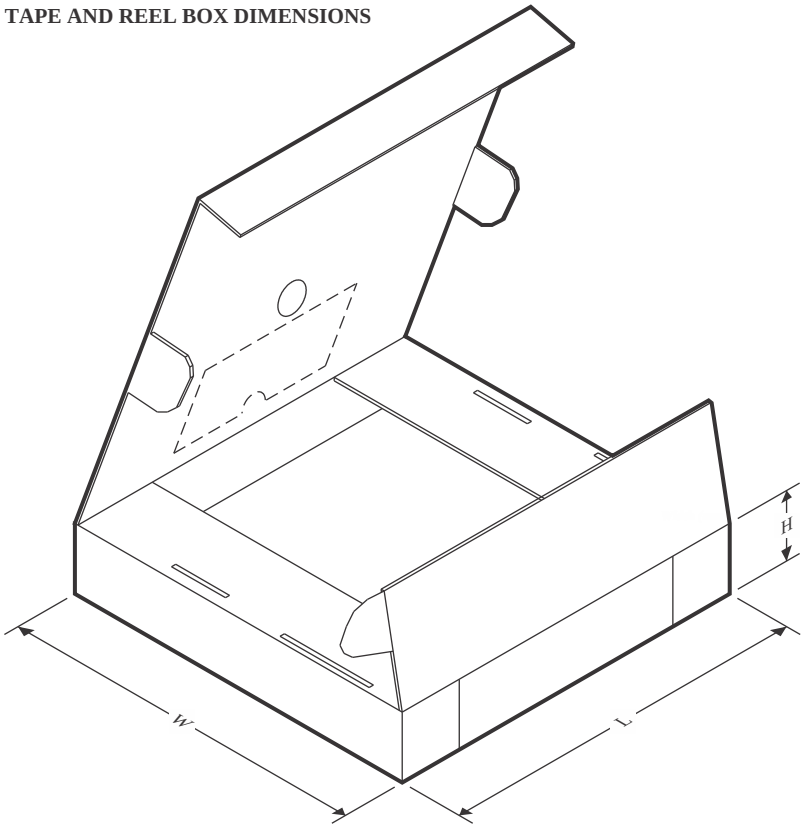
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMG3410R050RWHR	VQFN	RWH	32	2000	330.0	16.4	8.3	8.3	2.25	12.0	16.0	Q2
LMG3411R050RWHR	VQFN	RWH	32	2000	330.0	16.4	8.3	8.3	2.25	12.0	16.0	Q2

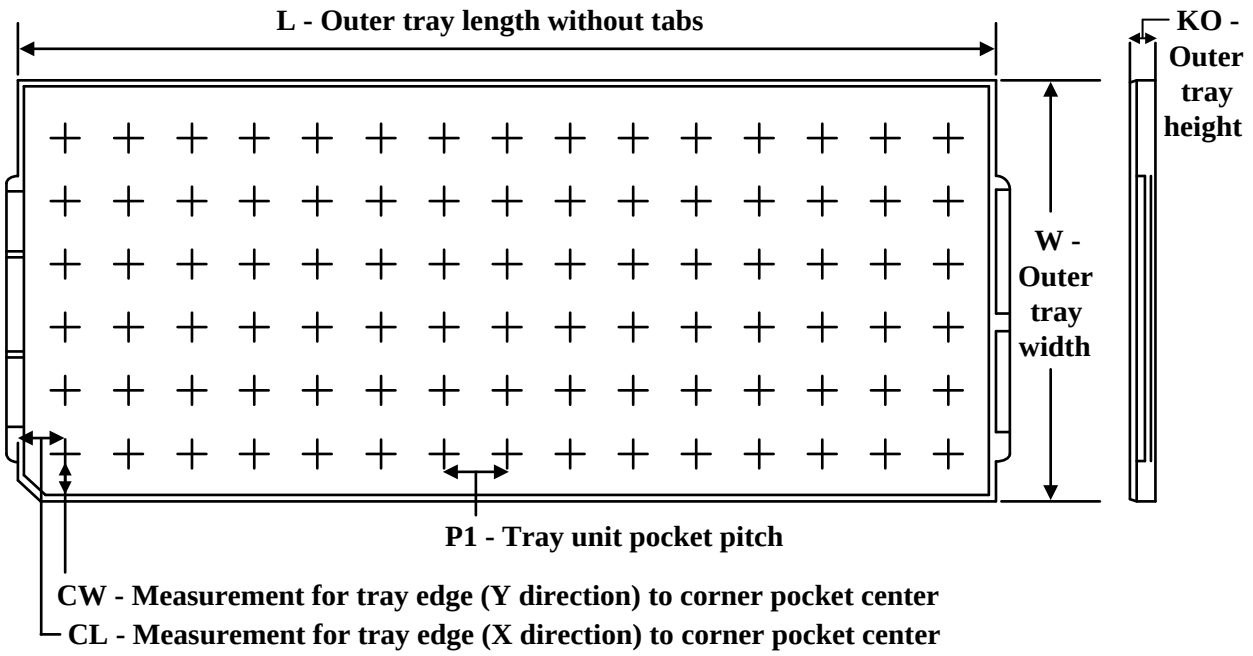
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMG3410R050RWHR	VQFN	RWH	32	2000	350.0	350.0	43.0
LMG3411R050RWHR	VQFN	RWH	32	2000	350.0	350.0	43.0

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

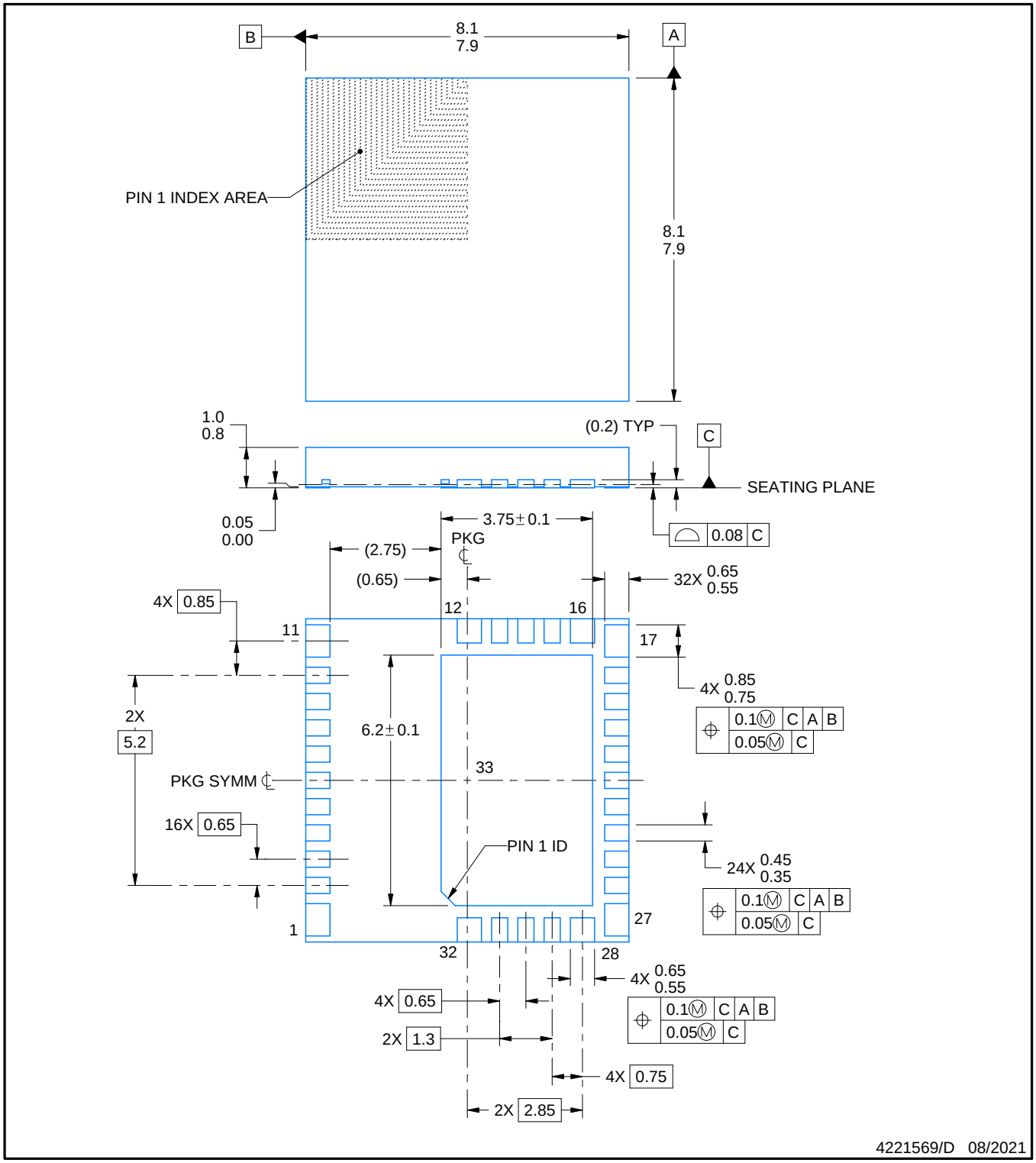
Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
LMG3410R050RWHR	RWH	VQFN	32	2000	10 x 26	150	315	135.9	7620	11.8	10	10.35
LMG3410R050RWHT	RWH	VQFN	32	250	10 x 26	150	315	135.9	7620	11.8	10	10.35
LMG3411R050RWHR	RWH	VQFN	32	2000	10 x 26	150	315	135.9	7620	11.8	10	10.35
LMG3411R050RWHT	RWH	VQFN	32	250	10 x 26	150	315	135.9	7620	11.8	10	10.35

PACKAGE OUTLINE

RWH0032A

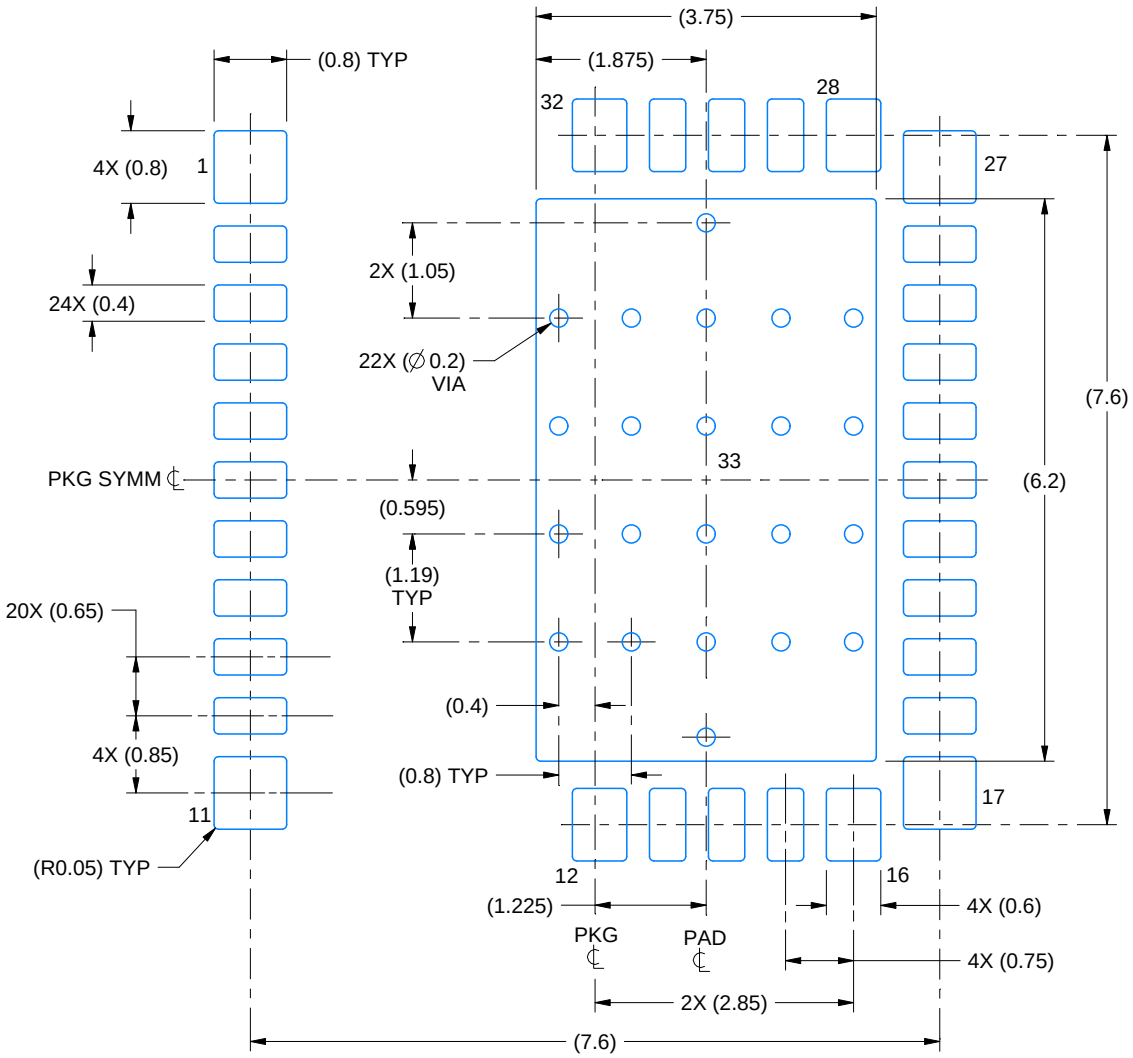
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X

NON SOLDER MASK DEFINED (PREFERRED)

SOLDER MASK DEFINED

SOLDER MASK DETAILS

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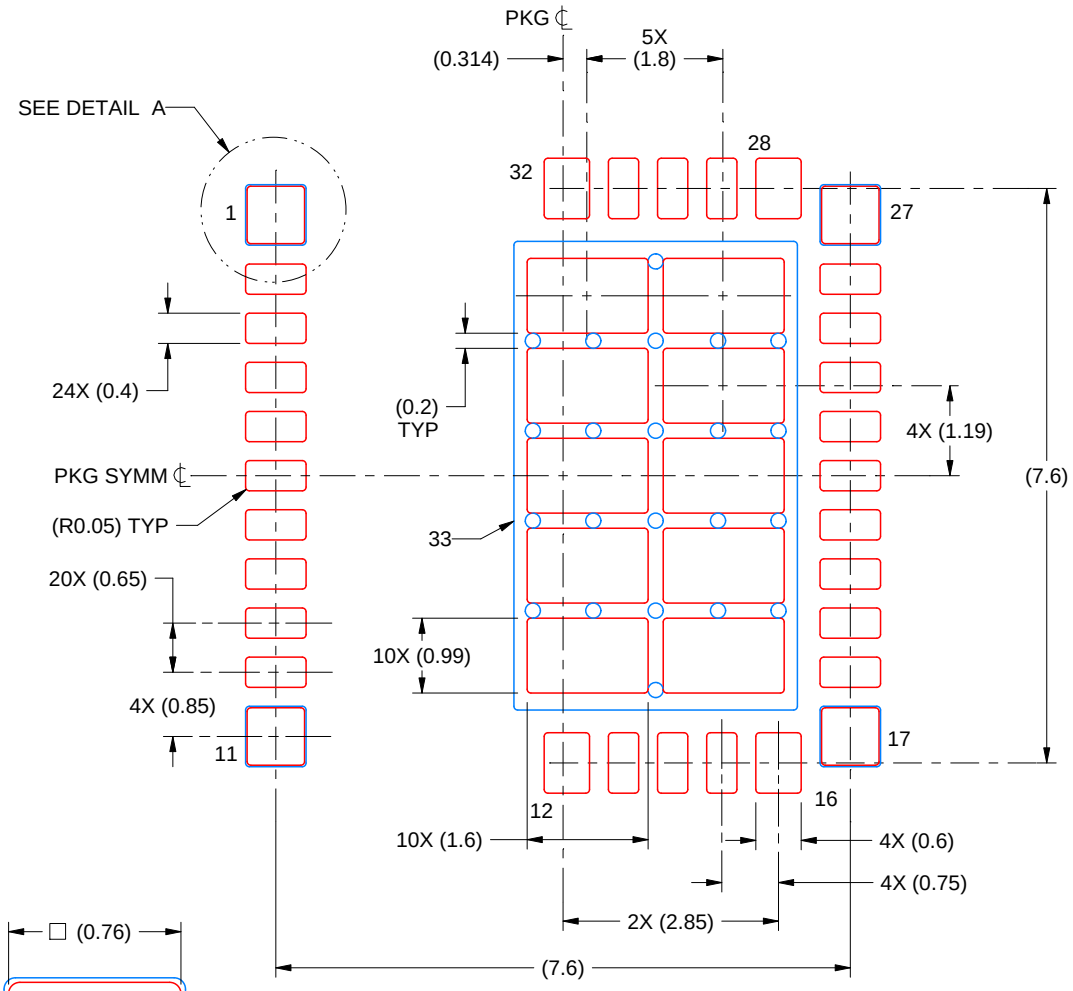
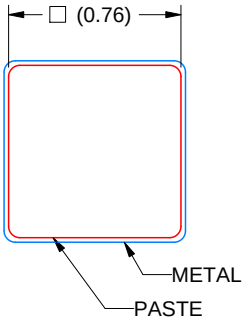
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
68% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:10X



DETAIL A
4X, SCALE: 30X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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