LMH0302 3Gbps HD/SD SDIケーブル・ドライバ

1 特長

- ST 424 (3G)、292 (HD)、259 (SD)をサポート
- 最大データレート2.97Gbps
- 270MbpsでDVB-ASIをサポート
- 100Ω差動入力
- 75Ωシングルエンド出力
- スルーレート選択可能
- 出力ドライバのパワーダウン制御
- 3.3V単電源動作
- 工業用温度範囲: −40℃～85℃
- 消費電力(標準値): SDモードで125mW、HDモードで165mW
- 16ピンWQFNパッケージ
- LMH0002SQとフットプリント互換
- Gennum社GS2978とピン互換

2 アプリケーション

- ST 424、ST 292、ST 344、ST 259シリアル・デジタル・インターフェイス
- デジタル・ビデオのルータおよびスイッチ
- 分配アンプ

3 概要

LMH0302 3Gbps HD/SD SDIケーブル・ドライバは、ST 424、ST 292、ST 344、ST 259シリアル・デジタル・ビデオ・アプリケーション用に設計されています。LMH0302は、75Ωの伝送ライン(Belden社1694A、Belden社8281、または同等のライン)を最大データレート2.97Gbpsで駆動します。

LMH0302は、ST 259、ST 424、ST 292に準拠するため、2種類のスルーレートが選択可能です。出力ドライバは、出力ドライバ・イネーブル・ピンによってパワーダウンすることができます。

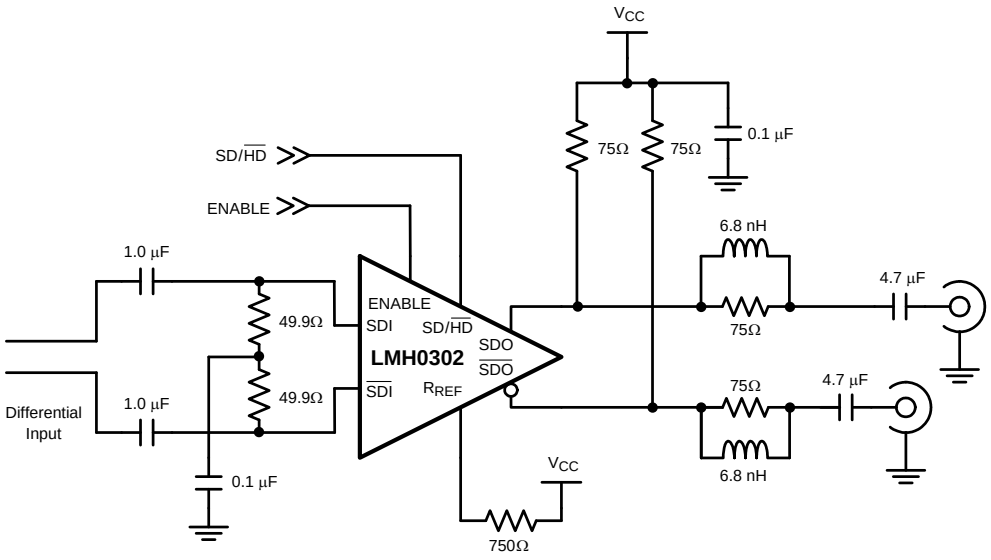
LMH0302は3.3V単電源で動作します。消費電力の標準値は、SDモードで125mW、HDモードで165mWです。LMH0302は、16ピンのWQFNパッケージで供給されます。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
LMH0302	WQFN (16)	4.00mm×4.00mm

(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

図 1. 代表的なアプリケーション



目次

4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision G (April 2013) から **Revision H** に変更 **Page**

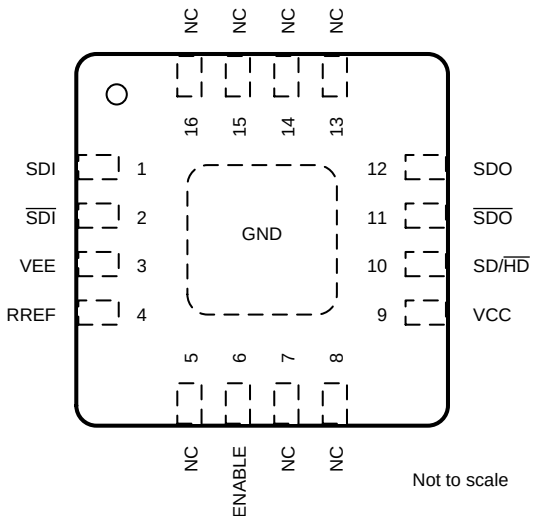
- 「*ESD定格*」の表、「*機能概要*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクションを追加 ... 1

Revision F (April 2013) から **Revision G** に変更 **Page**

- ナショナル セミコンダクターのデータシートのレイアウトをTIフォーマットへ 変更 ... 1

5 Pin Configuration and Functions

RUM Package
16-Pin WQFN
Top View



Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
ENABLE	6	I	Output driver enable. When low, the SDO/$\overline{\text{SDO}}$ output driver is powered off. ENABLE has an internal pullup. H = Normal operation. L = Output driver powered off.
EP	—	G	EP is the exposed pad at the bottom of the WQFN package. The exposed pad must be connected to the ground plane through a via array. See Figure 7 for details.
NC	5, 7, 8, 13, 14, 15, 16	—	No connect. Not bonded internally.
R_{REF}	4	I	Output driver level control. Connect a resistor to V_{CC} to set output voltage swing.
SD/$\overline{\text{HD}}$	10	I	Output slew rate control. Output rise/fall time complies with ST 424 or 292 when low and ST 259 when high.
SDI	1	I	Serial data true input.
$\overline{\text{SDI}}$	2	I	Serial data complement input.
SDO	12	O	Serial data true output.
$\overline{\text{SDO}}$	11	O	Serial data complement output.
V_{CC}	9	P	Positive power supply (3.3 V).
V_{EE}	3	G	Negative power supply (ground).

(1) G = Ground, I = Input, O = Output, and P = Power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply voltage	–0.5	3.6	V
Input voltage (all inputs)	–0.3	V_{CC} + 0.3	V
Output current		28	mA
Lead temperature, soldering (4 s)		260	°C
Junction temperature, T_J		125	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±2000	
		Machine model (MM)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage (V_{CC} – V_{EE})	3.13	3.3	3.46	V
Operating junction temperature			100	°C
Operating free air temperature, T_A	–40	25	85	°C

6.4 Thermal Information

THERMAL METRIC(1)		LMH0302 RUM (WQFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	47.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	47.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	25.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	25.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	14.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics – DC

Over supply voltage and operating free-air temperature range (unless otherwise noted) (1)(2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CMIN}	Input common mode voltage	SDI, $\overline{SDI}$	1.1 + V_{SDI}/2		V_{CC} – V_{SDI}/2	V
V_{SDI}	Input voltage swing	Differential, SDI, $\overline{SDI}$	100		2200	mV_{P-P}

(1) Current flow into device pins is defined as positive. Current flow out of device pins is defined as negative. All voltages are stated referenced to V_{EE} = 0 V.
(2) Typical values are stated for V_{CC} = 3.3 V and T_A = 25°C.

Electrical Characteristics – DC (continued)

Over supply voltage and operating free-air temperature range (unless otherwise noted) (1)(2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CMOUT}	Output common mode voltage	SDO, $\overline{SDO}$		$V_{CC} - V_{SDO}$		V
V_{SDO}	Output voltage swing	Single-ended, 75-Ω load, R_{REF} = 750 Ω 1%	720	800	880	mV_{P-P}
V_{IH}	Input voltage high level	SD/$\overline{HD}$, ENABLE	2			V
V_{IL}	Input voltage low level	SD/$\overline{HD}$, ENABLE			0.8	V
I_{CC}	Supply current	SD/$\overline{HD}$ = 0, SDO/$\overline{SDO}$ enabled		50	59	mA
		SD/$\overline{HD}$ = 0, SDO/$\overline{SDO}$ disabled		26	33	
		SD/$\overline{HD}$ = 1, SDO/$\overline{SDO}$ enabled		38	48	
		SD/$\overline{HD}$ = 1, SDO/$\overline{SDO}$ disabled		15	22	

6.6 Electrical Characteristics – AC

Over supply voltage and operating free-air temperature range (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DR_{SDI}	Input data rate	SDI, $\overline{SDI}$			2970	Mbps
T_{jit}	Additive jitter	2.97 Gbps, SDO, $\overline{SDO}$		20		ps_{P-P}
		1.485 Gbps, SDO, $\overline{SDO}$		18		
		270 Mbps, SDO, $\overline{SDO}$		15		
t_r,t_f	Output rise time, fall time	SD/$\overline{HD}$ = 0, 20% – 80%, SDO, $\overline{SDO}$		90	130	ps
		SD/$\overline{HD}$ = 1, 20% – 80%, SDO, $\overline{SDO}$	400		800	
T_{MATCH}	Mismatch in rise time, fall time	SD/$\overline{HD}$ = 0, SDO, $\overline{SDO}$			30	ps
		SD/$\overline{HD}$ = 1, SDO, $\overline{SDO}$			50	
T_{DCD}	Duty cycle distortion	SD/$\overline{HD}$ = 0, 2.97 Gbps, SDO, $\overline{SDO}$(2)			27	ps
		SD/$\overline{HD}$ = 0, 1.485 Gbps, SDO, $\overline{SDO}$(2)			30	
		SD/$\overline{HD}$ = 1, SDO, $\overline{SDO}$(2)			100	
T_{OS}	Output overshoot	SD/$\overline{HD}$ = 0, SDO, $\overline{SDO}$(2)			10%	
		SD/$\overline{HD}$ = 1, SDO, $\overline{SDO}$(2)			8%	
RL_{SDO}	Output return loss	5 MHz to 1.5 GHz, SDO, $\overline{SDO}$(3)	15			dB
		1.5 GHz to 3.0 GHz, SDO, $\overline{SDO}$(3)	10			

(1) Typical values are stated for V_{CC} = 3.3 V and T_A = 25°C.
(2) Specification is ensured by characterization.
(3) Output return loss is dependent on board design. The LMH0302 meets this specification on the SD302 evaluation board.

6.7 Typical Characteristics

Typical device characteristics at T_A = 25°C and V_{CC} = 3.3 V (unless otherwise noted)

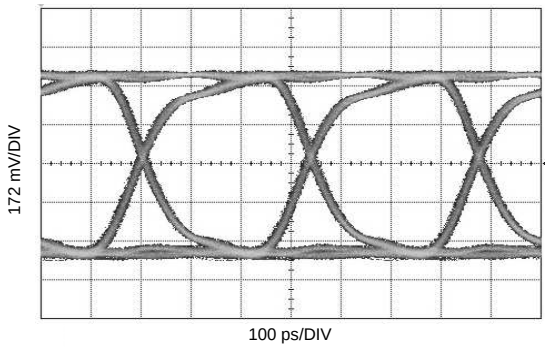


Figure 2. SDO PRBS10 at 2.97 Gbps

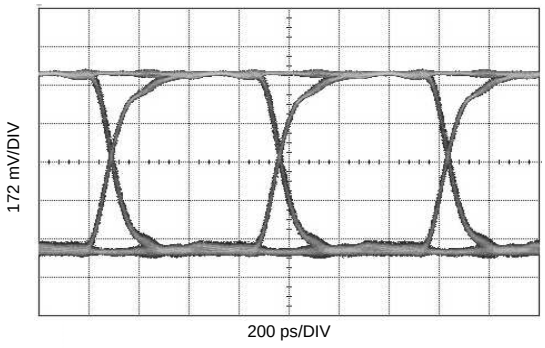


Figure 3. SDO PRBS10 at 1.485 Gbps

7 Detailed Description

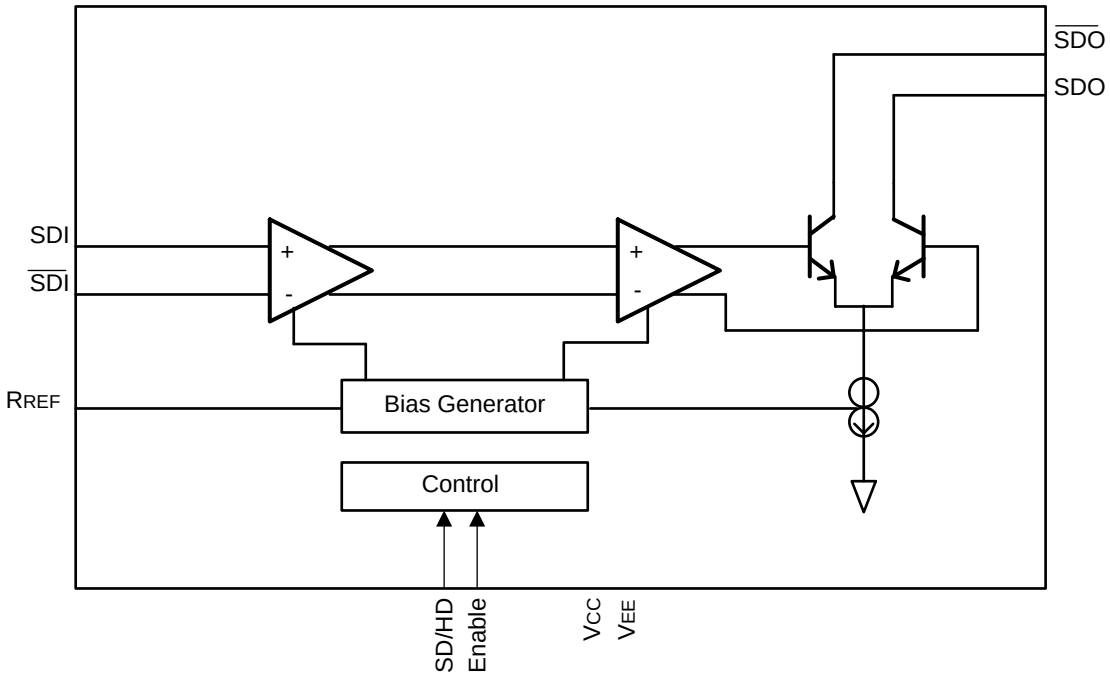
7.1 Overview

The LMH0302 ST 424, ST292, ST259 serial digital cable driver is a monolithic, high-speed cable driver designed for use in serial digital video data transmission applications. The LMH0302 drives 75-Ω transmission lines (Belden 8281, 1694A, Canare L-5CFB, or equivalent) at data rates up to 2.97 Gbps.

The LMH0302 provides two selectable slew rates for ST 259 and ST 292/424 compliance. The output voltage swing is adjustable through a single external resistor (R_{REF}).

The LMH0302 is powered from a single 3.3-V supply. Power consumption is typically 125 mW in SD mode and 165 mW in HD mode. The LMH0302 is available in a 16-pin WQFN package.

7.2 Functional Block Diagram



7.3 Feature Description

The LMH0302 data path consists of several key blocks:

- Input interfacing
- Output interfacing
- Output slew rate control
- Output enable

7.3.1 Input Interfacing

The LMH0302 accepts either differential or single-ended input. The inputs are self-biased, allowing for simple AC or DC coupling. DC-coupled inputs must be kept within the specified common-mode range.

7.3.2 Output Interfacing

The LMH0302 uses current mode outputs. Single-ended output levels are 800 mV_{P-P} into 75-Ω AC-coupled coaxial cable with an R_{REF} resistor of 750 Ω. The R_{REF} resistor is connected between the R_{REF} pin and V_{CC}.

Feature Description (continued)

The R_{REF} resistor must be placed as close as possible to the R_{REF} pin. In addition, the copper in the plane layers below the R_{REF} network must be removed to minimize parasitic capacitance.

7.3.3 Output Slew Rate Control

The LMH0302 output rise and fall times are selectable for either ST 259, ST 424, or 292 compliance through the SD/$\overline{HD}$ pin. For slower rise and fall times, or ST 259 compliance, SD/$\overline{HD}$ is set high. For faster rise and fall times, ST 424 and ST 292 compliance, SD/$\overline{HD}$ is set low.

7.3.4 Output Enable

The SDO/$\overline{SDO}$ output driver are enabled or disabled with the ENABLE pin. When set low, the output driver is powered off. ENABLE has an internal pullup.

7.4 Device Functional Modes

The LMH0302 features are programmed using pin mode only.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LMH0302 is a single-channel SDI cable driver that supports different application spaces. The following sections describe the typical use cases and common implementation practices.

8.1.1 General Guidance for All Applications

The SMPTE specifications define the use of AC-coupling capacitors for transporting uncompressed serial data streams with heavy low-frequency content. This specification requires the use of a 4.7-µF AC-coupling capacitor to avoid low frequency DC wander. The 75-Ω signal is also required to meet certain rise and fall timing to facilitate highest eye opening for the receiving device.

SMPTE specifies the requirements for the Serial Digital Interface to transport digital video at SD, HD, 3 Gbps, and higher data rates over coaxial cables. One of the requirements is meeting the required return loss. This requirement specifies how closely the port resembles 75-Ω impedance across a specified frequency band. Output return loss is dependent on board design. The LMH0302 supports these requirements.

8.2 Typical Application

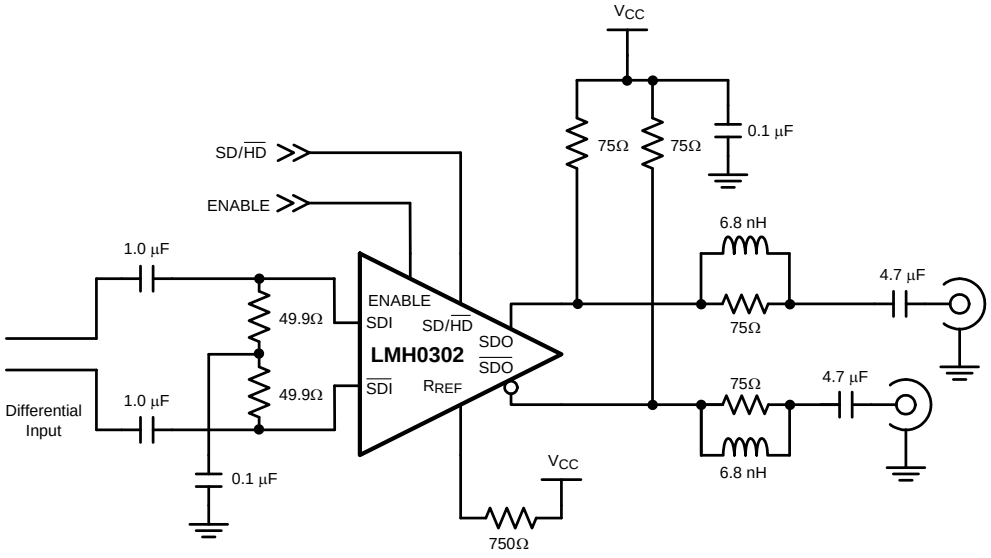


Figure 4. Application Circuit

Typical Application (continued)

8.2.1 Design Requirements

For the LMH0302 design example, Table 1 lists the design parameters.

Table 1. LMH0302 Design Parameters

PARAMETER	REQUIREMENT
Input termination	Required; 49.9 Ω are recommended (see *Figure 4*).
Output AC-coupling capacitors	Required; both SDO and $\overline{\text{SDO}}$ require AC-coupling capacitors. SDO AC-coupling capacitors are expected to be 4.7 µF to comply with SMPTE wander requirement.
DC power supply coupling capacitors	To minimize power supply noise, place 0.1-µF capacitor as close to the device V_{CC} pin as possible.
Distance from device to BNC	Keep this distance as short as possible.
High speed SDI and $\overline{\text{SDI}}$ trace impedance	Design differential trace impedance of SDI and $\overline{\text{SDI}}$ with 100 Ω.
High speed SDO and $\overline{\text{SDO}}$ trace impedance	Single-ended trace impedance for SDO and $\overline{\text{SDO}}$ with 75 Ω.

8.2.2 Detailed Design Procedure

The following design procedure is recommended:

1. Select a suitable power supply voltage for the LMH0302. It can be powered from a single 3.3-V supply.
2. Check that the power supply meets the DC requirements in *Electrical Characteristics – DC*.
3. Select the proper pull-high or pull-low for SD/$\overline{\text{HD}}$ to set the slew rate.
4. Select proper pull-high or pull-low for ENABLE to enable or disable the output driver.
5. Choose a high-quality 75-Ω BNC that is capable to support 2.97-Gbps applications. Consult a BNC supplier regarding insertion loss, impedance specifications, and recommended BNC footprint for meeting SMPTE return loss requirements.
6. Choose small 0402 surface-mount ceramic capacitors for the AC-coupling and bypass capacitors.
7. Use proper footprint for BNC and AC-coupling capacitors. Anti-pads are commonly used in power and ground planes under these landing pads to achieve optimum return loss.

8.2.3 Application Curves

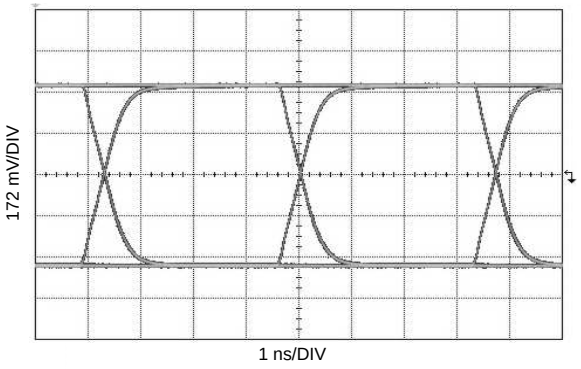


Figure 5. SDO PRBS10 at 270 Mbps

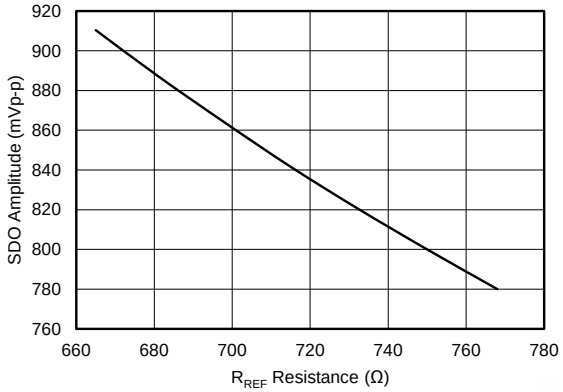


Figure 6. SDO Amplitude vs R_{REF} Resistance

9 Power Supply Recommendations

Follow these general guidelines when designing the power supply:

1. The power supply must be designed to provide the recommended operating conditions (see *Recommended Operating Conditions*).
2. The maximum current draw for the LMH0302 is provided in *Electrical Characteristics – DC*. This figure can be used to calculate the maximum current the supply must provide.
3. The LMH0302 does not require any special power supply filtering, provided the recommended operating conditions are met. Only standard supply coupling is required.

10 Layout

10.1 Layout Guidelines

TI recommends the following layout guidelines for the LMH0302:

1. The R_{REF} 1% tolerance resistor must be placed as close as possible to the R_{REF} pin. In addition, the copper in the plane layers below the R_{REF} network must be removed to minimize parasitic capacitance.
2. Choose a suitable board stackup that supports 75-Ω single-ended trace and 100-Ω differential trace routing on the top layer of the board. This is typically done with a Layer 2 ground plane reference for the 100-Ω differential traces and a second ground plane at Layer 3 reference for the 75-Ω single-ended traces.
3. Use single-ended uncoupled trace designed with 75-Ω impedance for signal routing to SDO and $\overline{\text{SDO}}$. The trace width is typically 8-10 mil reference to a ground plane at Layer 3.
4. Use coupled differential traces with 100-Ω impedance for signal routing to SDI and $\overline{\text{SDI}}$. They are usually 5-mil to 8-mil trace width reference to a ground plane at Layer 2.
5. Place anti-pad (ground relief) on the power and ground planes directly under the 4.7-µF AC-coupling capacitor, return loss network, and IC landing pads to minimize parasitic capacitance. The size of the anti-pad depends on the board stackup and can be determined by a 3-dimension electromagnetic simulation tool.
6. Use a well-designed BNC footprint to ensure the BNC's signal landing pad achieves 75-Ω characteristic impedance. BNC suppliers usually provide recommendations on BNC footprint for best results.
7. Keep trace length short between the BNC and SDO. The trace routing for SDO and $\overline{\text{SDO}}$ must be symmetrical, approximately equal lengths, and equal loading.
8. The exposed pad EP of the package must be connected to the ground plane through an array of vias. These vias are solder-masked to avoid solder flow into the plated-through holes during the board manufacturing process.
9. Connect each supply pin (V_{CC} and V_{EE}) to the power or ground planes with a short via. The via is usually placed tangent to the landing pads of the supply pins with the shortest trace possible.
10. Power-supply bypass capacitors must be placed close to the supply pins.

10.2 Layout Example

Figure 7 shows an example of proper layout requirements for the LMH0302.

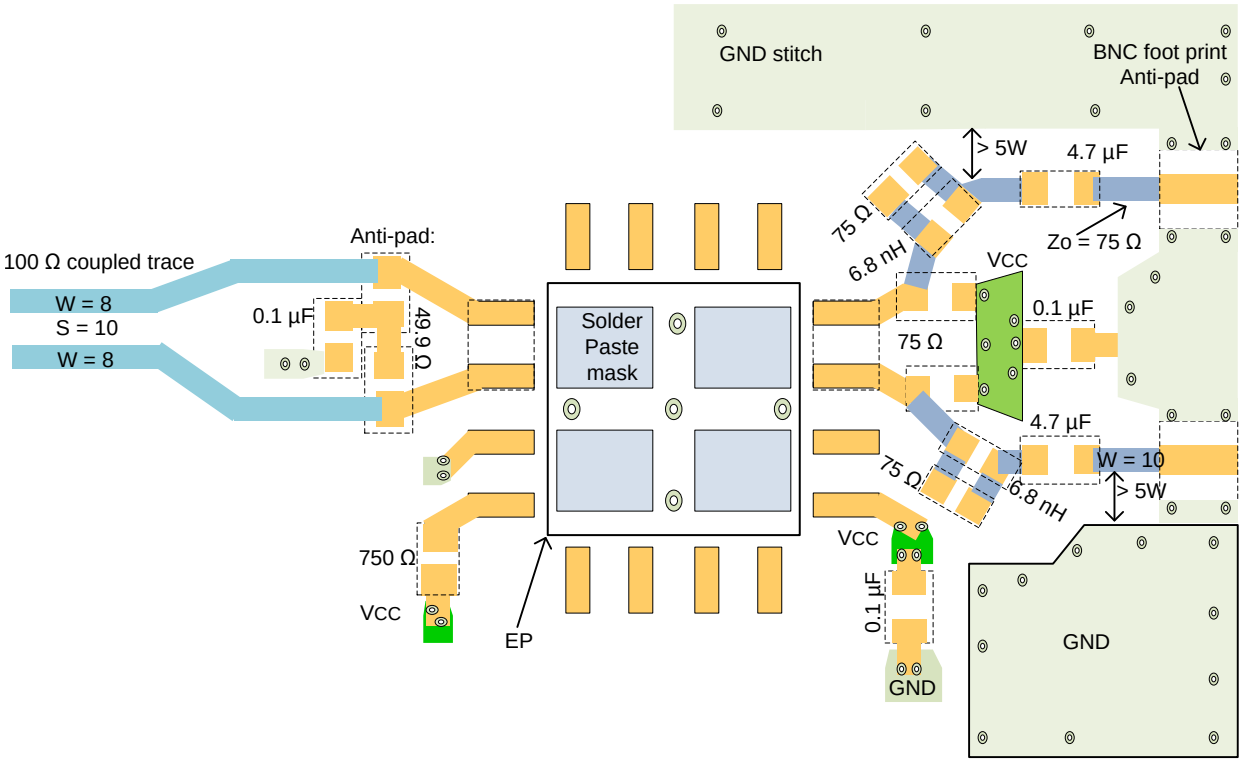


Figure 7. LMH0302 High-Speed Traces Layout Example

11 デバイスおよびドキュメントのサポート

11.1 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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All other trademarks are the property of their respective owners.

11.3 静電気放電に関する注意事項

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11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。これらの情報は、指定のデバイスに対して提供されている最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMH0302SQ/NOPB	ACTIVE	WQFN	RUM	16	1000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 85	L0302	Samples
LMH0302SQE/NOPB	ACTIVE	WQFN	RUM	16	250	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 85	L0302	Samples
LMH0302SQX/NOPB	ACTIVE	WQFN	RUM	16	4500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 85	L0302	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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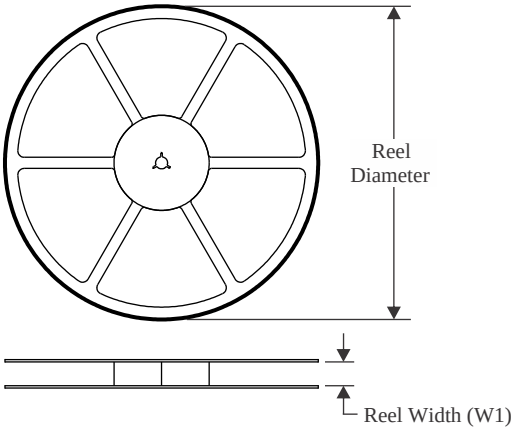
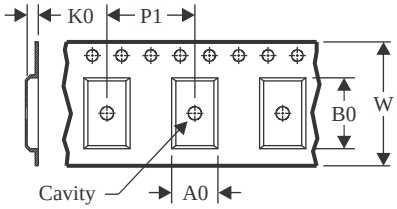
TAPE AND REEL INFORMATION

REEL DIMENSIONS

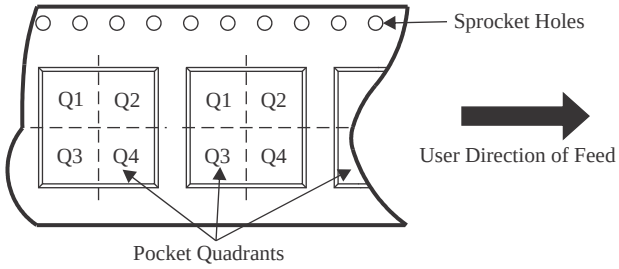


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

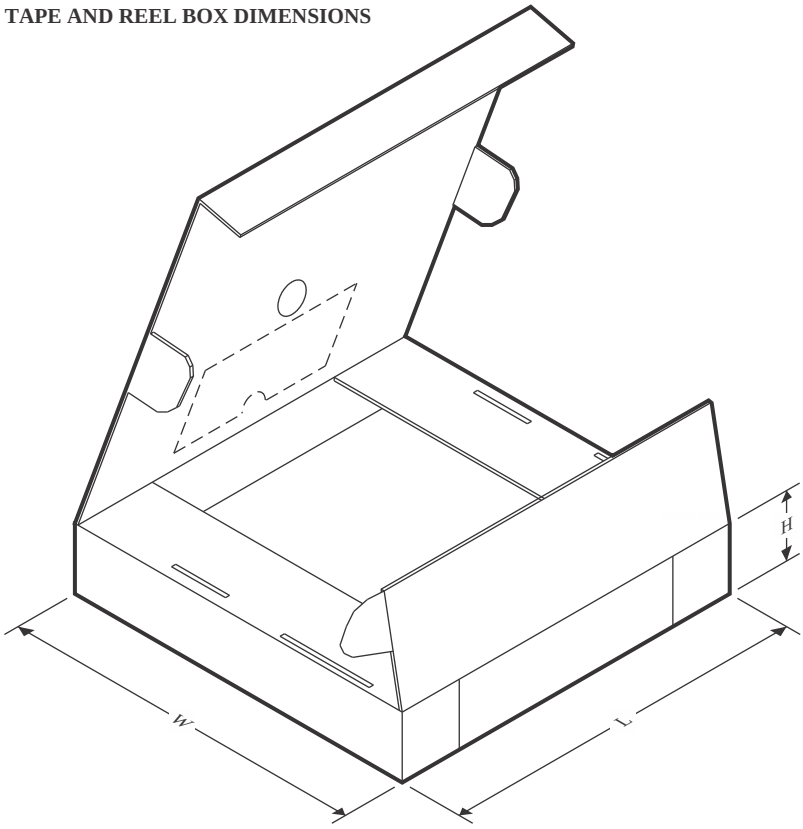
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH0302SQ/NOPB	WQFN	RUM	16	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LMH0302SQE/NOPB	WQFN	RUM	16	250	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LMH0302SQX/NOPB	WQFN	RUM	16	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

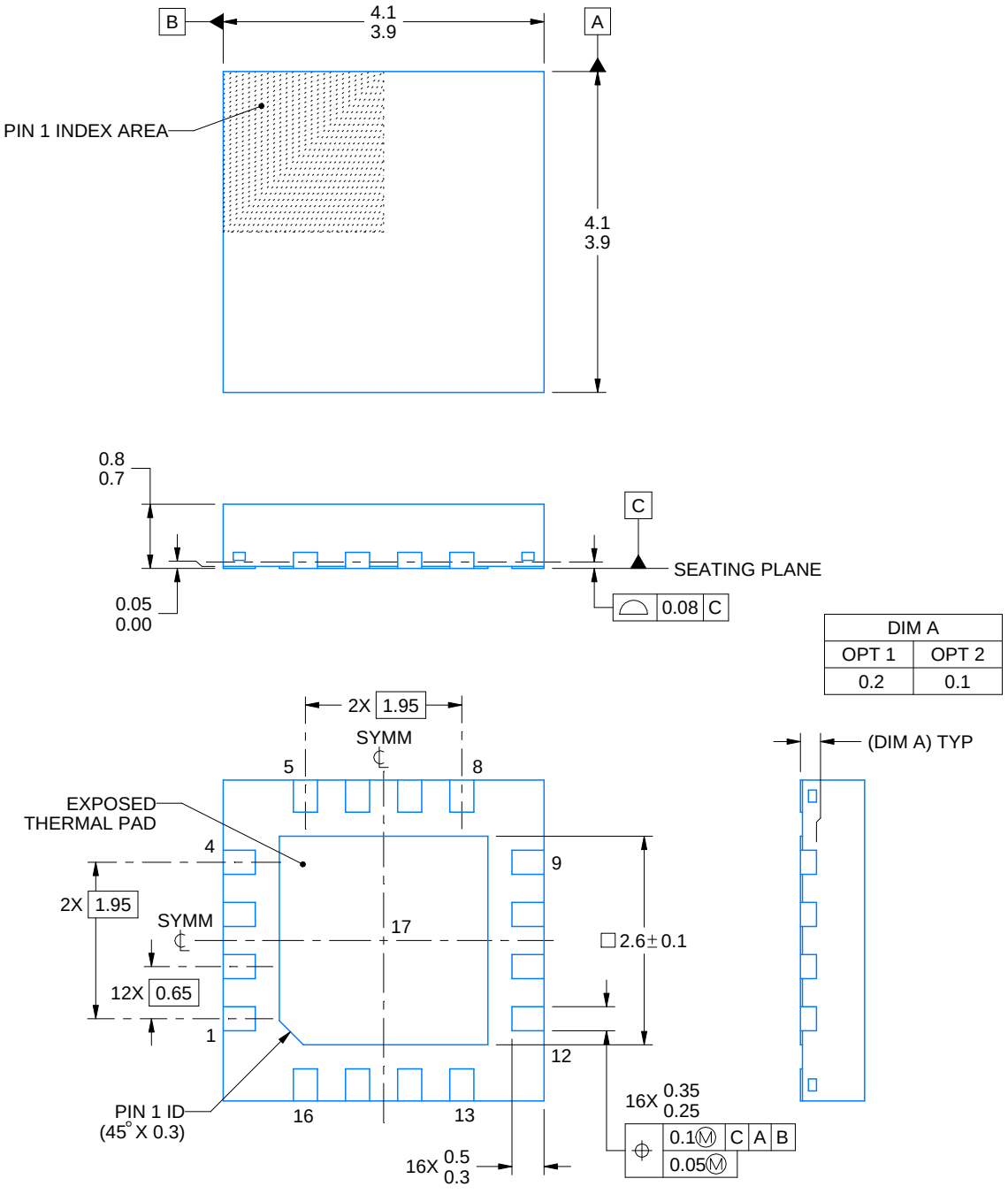
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH0302SQ/NOPB	WQFN	RUM	16	1000	208.0	191.0	35.0
LMH0302SQE/NOPB	WQFN	RUM	16	250	208.0	191.0	35.0
LMH0302SQX/NOPB	WQFN	RUM	16	4500	356.0	356.0	35.0

RUM0016A

PACKAGE OUTLINE

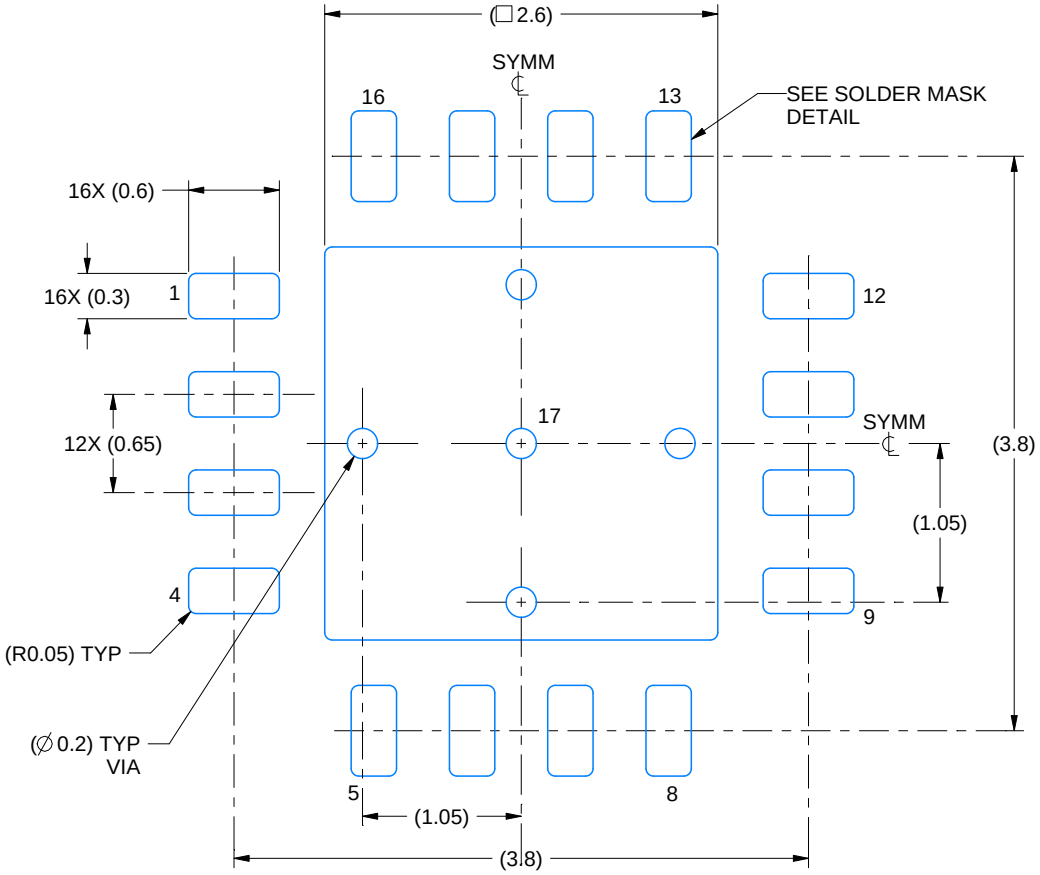
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

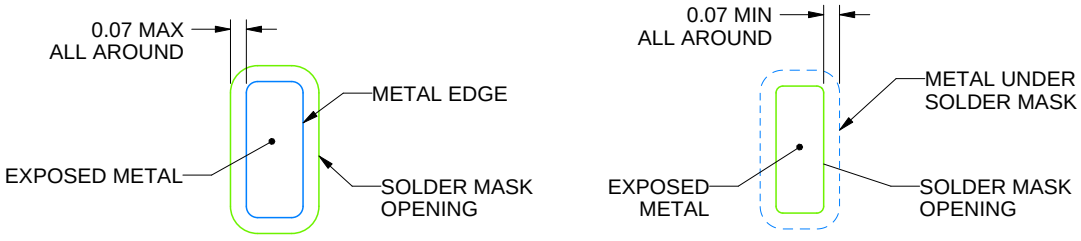


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



NON SOLDER MASK DEFINED (PREFERRED)

SOLDER MASK DEFINED

SOLDER MASK DETAILS

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NOTES: (continued)

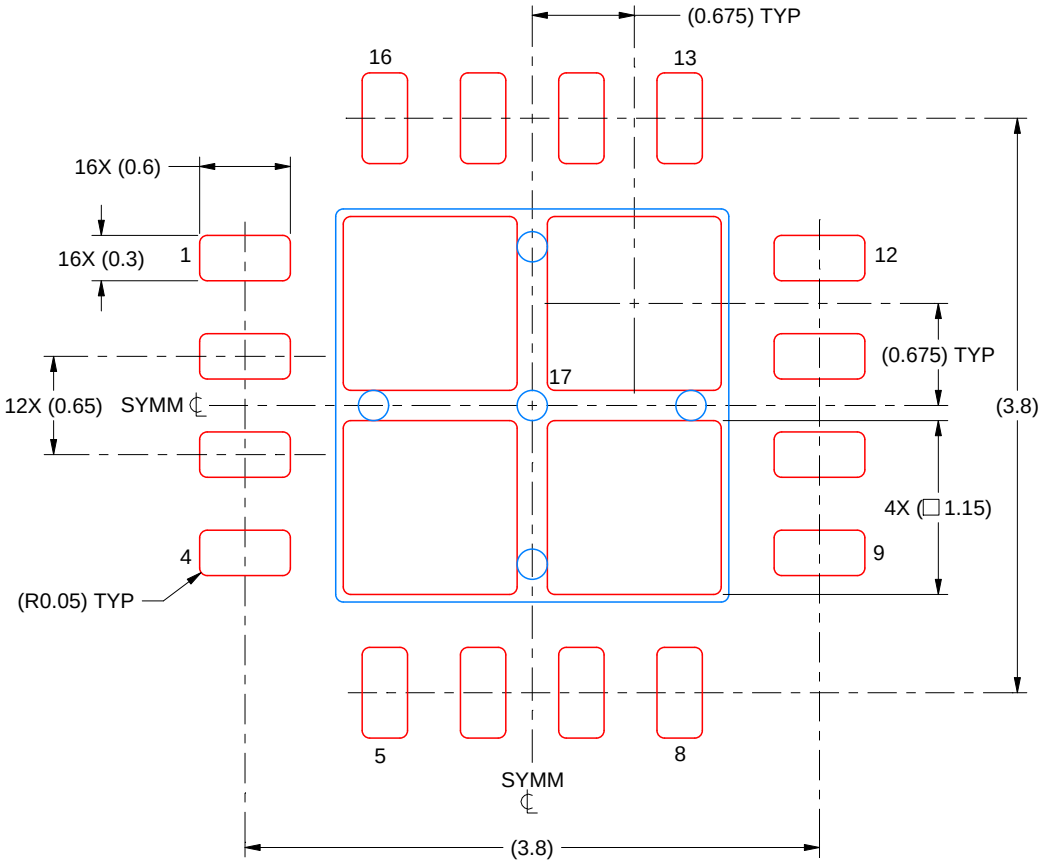
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RUM0016A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 17
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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