LMH1226 低消費電力、デュアル出力の12G UHDリクロッカ

1 特長

- ST-2082-1(12G)、ST-2081-1(6G)、ST-424(3G)、ST-292(HD)、ST-259(SD)をサポート
- SMPTE 2022-5/6のSFF8431 (SFP+)をサポート
- DVB-ASIおよびAES10 (MADI)と互換
- 基準クロックなしのリクロッカで、SMPTEおよび10GbEレートを11.88Gbps、5.94Gbps、2.97Gbps、1.485Gbps、またはDivide-by-1.001のサブレート、270Mbps、10.3125Gbpsにロック
- 基準クロックなしで高速なロック時間
- 入力1 (IN1)の適応型基板配線イコライザ
- 低消費電力: 214mW (標準値)
- パワーセーブ・モード: 16mW
- ディエンファシス付きの1:2のファンアウト出力を内蔵
- オンチップのループ・フィルタとアイ開口部モニタ
- 単一の2.5Vからオンチップの1.8Vレギュレータで電力を供給
- 制御ピン、SPI、またはSMBusインターフェイスにより構成可能
- 4mm×4mm、24ピンのQFNパッケージ
- 動作温度範囲: -40℃～+85℃

2 アプリケーション

- SMPTE互換のシリアル・デジタル・インターフェイス(SDI)
- UHDTV/4K/8K/HDTV/SDTVビデオ
- 放送用ビデオ・ルータ、スイッチャ、モニタ
- デジタル・ビデオ処理および編集
- 10 GbE - SDIのメディア・ゲートウェイ

3 概要

LMH1226は低消費電力、デュアル出力の12G UHDリクロッカです。最高11.88GbpsのSMPTEビデオとIP上の10GbEビデオをサポートし、4K/8Kアプリケーション用のUHDビデオに対応します。IN1の適応型基板配線イコライザはSFF-8431互換で、SMPTEと10GbEの両方のデータ速度をサポートします。

このリクロッカは高周波のジッタを減衰させ、最高の信号整合性を実現します。リクロッカの入力ジッタ許容範囲が高いため、タイミング・マージンが改善されます。このリクロッカにはループ・フィルタが組み込まれており、高精度の入力基準クロックを必要とせずに動作します。非破壊的なアイ・モニタによりシリアル・データをリアルタイムで計測できるため、システムのデバッグが簡素化し、基板の製品化を迅速に行えます。

内蔵の1:2ファンアウトにより、複数のビデオ信号を柔軟に使用できます。出力ドライバではディエンファシスをプログラム可能で、基板の配線損失を出力で補償できます。LMH1226の標準的な消費電力は214mWです。入力信号が存在しないとき、消費電力はさらに16mWに低下します。

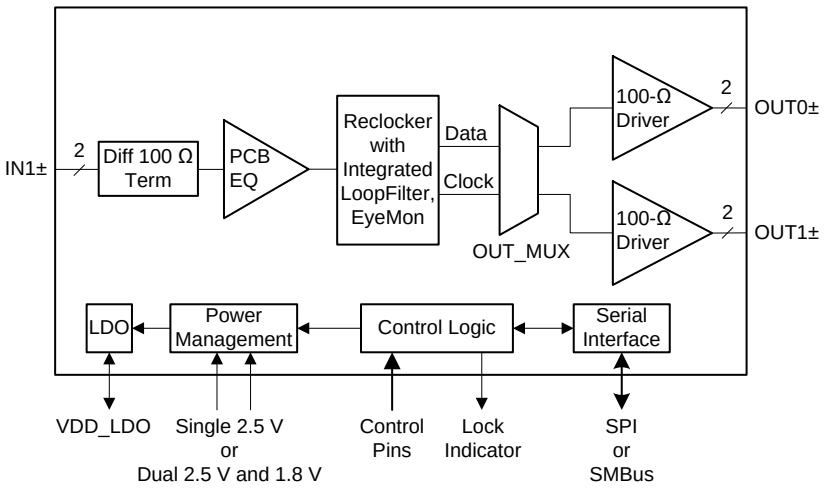
LMH1226は、LMH1219 (リクロッカを内蔵した12G-UHDのケーブル・イコライザ)とピン互換です。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
LMH1226	QFN (24)	4.00mm×4.00mm

(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

ブロック概略図



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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision C (October 2017) から Revision D に変更 **Page**

- 完全な量産データシートの最初の公開リリース ... 1

Revision B (February 2017) から Revision C に変更 **Page**

- 追加 パッケージ図 ... 43

Revision A (May 2016) から Revision B に変更 **Page**

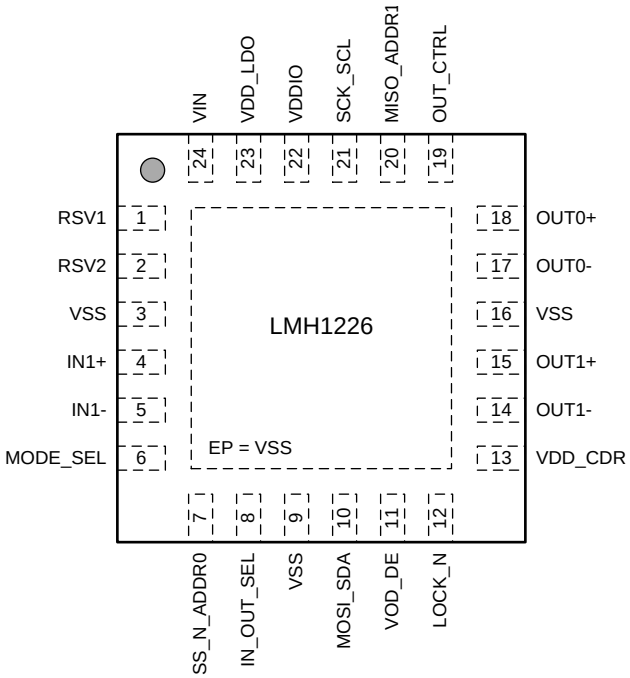
- Changed eq_en_bypass bit description from "Gain Stages 3 and 4" to "Gain Stages 2 and 3" ... 27
- Changed bit location of IN1 Carrier Detect Power Down Control from Reg 0x13[5] to Reg 0x15[6] ... 27

2016年4月発行のものから更新 **Page**

- Deleted min and max VOD_DE amplitude specification when VOD_DE = Level F ... 8
- Changed typical VOD_DE amplitude specifications for Levels F, R, and L ... 8
- Changed DEM value and DEM register settings in Table 5 to match correct VOD_DE pin logic levels ... 18
- 追加 new row for VOD = 5, DEM = 5 setting in 表 10 ... 39

5 Pin Configuration and Functions

RTW Package
24-Pin QFN
Top View



Pin Functions

PIN		I/O (1)	DESCRIPTION
NAME	NO.		
High-Speed Differential I/Os			
IN1+	4	I, Analog	Differential complementary inputs with internal 100-Ω termination. Requires external 4.7-µF AC coupling capacitors for SMPTE and 10 GbE.
IN1-	5	I, Analog	
OUT0+	18	O, Analog	Differential complementary outputs with 100-Ω internal termination. Requires external 4.7-µF AC coupling capacitors. Output driver OUT0± can be disabled under user control.
OUT0-	17	O, Analog	
OUT1+	15	O, Analog	Differential complementary outputs with 100 Ω internal termination. Requires external 4.7-µF AC coupling capacitors. Output driver OUT1± can be disabled under user control.
OUT1-	14	O, Analog	
RSV1	1		Reserved pins. Do not connect.
RSV2	2		
Control Pins			
LOCK_N	12	O, LVCMOS, OD	LOCK_N is the reclocker lock indicator for the selected input. LOCK_N is pulled LOW when the reclocker has acquired locking condition. LOCK_N is an open drain output, 3.3 V tolerant, and requires an external 2-kΩ to 5-kΩ pull-up resistor to logic supply. LOCK_N pin can be re-configured to indicate INT_N (Interrupt) through register programming.
IN_OUT_SEL	8	I, 4-LEVEL	IN_OUT_SEL selects the signal flow at input ports to output ports. See Table 2 for details. This pin setting can be overridden by register control.
OUT_CTRL	19	I, 4-LEVEL	OUT_CTRL selects the signal flow from IN1± to OUT1± and OUT0±. It selects reclocked data, reclocked data and clock, bypassed reclocker data (equalized data to output driver), or bypassed equalizer and reclocker data. See Table 4 for details. This pin setting can be overridden by register control.

(1) I = Input, O = Output, IO = Input or Output, OD = Open Drain, LVCMOS = 2-State Logic, 4-LEVEL = 4-State Logic

Pin Functions (continued)

PIN		I/O (1)	DESCRIPTION
NAME	NO.		
VOD_DE	11	I, 4-LEVEL	VOD_DE selects the driver output amplitude and de-emphasis level for both OUT0± and OUT1±. See Table 5 for details. This pin setting can be overridden by register control.
MODE_SEL	6	I, 4-LEVEL	MODE_SEL enables SPI or SMBus serial control interface. See Table 6 for details.
Serial Control Interface (SPI Mode), MODE_SEL = F (Float)			
SS_N	7	I, LVCMOS	SS_N is the Slave Select. When SS_N is at logic Low, it enables SPI access to the LMH1226 slave device. SS_N is a LVCMOS input reference to VDDIO.
MISO	20	O, LVCMOS	MISO is the SPI control serial data output from the LMH1226 slave device. MISO is a LVCMOS output reference to VDDIO.
MOSI	10	I, LVCMOS	MOSI is used as the SPI control serial data input to the LMH1226 slave device. MOSI is LVCMOS input reference to VDDIO.
SCK	21	I, LVCMOS	SCK is the SPI serial input clock to the LMH1226 slave device. SCK is LVCMOS reference to VDDIO.
Serial Control Interface (SMBus Mode) , MODE_SEL = L (1 kΩ to VSS)			
ADDR0	7	Strap, 4-LEVEL	ADDR[1:0] are SMBus address straps to select one of the 16 supported SMBus addresses. ADDR[1:0] are 4-level straps and are read into the device at power up.
ADDR1	20	Strap, 4-LEVEL	
SDA	10	IO, LVCMOS, OD	SDA is the SMBus bi-directional open drain SDA data line to or from the LMH1226 slave device. SDA is an open drain IO and tolerant to 3.3 V. SDA requires an external 2-kΩ to 5-kΩ pull-up resistor to the SMBus termination voltage.
SCL	21	I, LVCMOS, OD	SCL is the SMBus input clock to the LMH1226 slave device. It is driven by a LVCMOS open drain driver from the SMBus master. SCL is tolerant to 3.3 V and requires an external 2-kΩ to 5-kΩ pull up resistor to the SMBus termination voltage.
Power			
VSS	3, 9, 16	I, Ground	Ground reference.
VIN	24	I, Power	VIN is connected to an external power supply. It accepts either 2.5 V ± 5% or 1.8 V ± 5%. When VIN is powered from 2.5 V, VDD_LDO is the output of an on-chip LDO regulator. For lower power operation, both VIN and VDD_LDO should be connected to a 1.8 V supply.
VDDIO	22	I, Power	VDDIO powers the LVCMOS IO and 4-level input logic and connects to 2.5 V ± 5% supply.
VDD_LDO	23	IO, Power	VDD_LDO is the output of the internal 1.8 V LDO regulator when VIN is connected to a 2.5 V supply. VDD_LDO output requires external 1-μF and 0.1-μF bypass capacitors to VSS. The internal LDO is designed to power internal circuitry only. VDD_LDO is an input when VIN is powered from 1.8 V for lower power operation. When VIN is connected to a 1.8 V supply, both VIN and VDD_LDO should be connected to a 1.8 V supply.
VDD_CDR	13	I, Power	VDD_CDR powers the reclocker circuitry and connects to 2.5 V ± 5% supply.
EP		I, Ground	EP is the exposed pad at the bottom of the QFN package. The exposed pad must be connected to the ground plane through a via array. See 図 29 for details.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply Voltage for 2.5 V Mode (VDD_CDR, VIN, VDDIO)	–0.5	2.75	V
Supply Voltage for 1.8 V Mode (VIN, VDD_LDO)	–0.5	2.0	V
4-Level Input/Output Voltage (IN_OUT_SEL, OUT_CTRL, VOD_DE, MODE_SEL, ADDR0, ADDR1)	–0.5	2.75	V
SMBus Input/Output Voltage (SDA, SCL)	–0.5	4.0	V
SPI Input/Output Voltage (SS_N, MISO, MOSI, and SCK)	–0.5	2.75	V
Input Voltage (IN1±)	–0.5	2.75	V
Input Current (IN1±)	–30	30	mA
Operating Junction Temperature		125	°C
Storage temperature	-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4500	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500 V HBM is possible with the necessary precautions. Pins listed as ±4500 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250 V CDM is possible with the necessary precautions. Pins listed as ±1500 V may actually have higher performance.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
Single Supply Mode (1)	VIN, VDDIO, VDD_CDR to VSS		2.375	2.5	2.625	V
Dual Supply Mode (2)(3)	VIN, VDD_LDO to VSS		1.71	1.8	1.89	V
	VDD_CDR, VDDIO to VSS		2.375	2.5	2.625	V
VDD_{SMBUS}	SMBus: SDA, SCL Open Drain Termination Voltage		2.375		3.6	V
V_{IN1_LAUNCH}	Source Differential Launch Amplitude Before 5-Inch Board Trace		300		850	mVp-p
	Source Differential Launch Amplitude Before 20-Inch Board Trace		650		1000	mVp-p
$T_{JUNCTION}$	Operating Junction Temperature				100	°C
$T_{AMBIENT}$	Ambient Temperature		–40	25	85	°C
$NTps_{max}$ (4)	Maximum Supply Noise Tolerance	50 Hz to 1 MHz, Sinusoidal		<20		mVp-p
	Maximum Supply Noise Tolerance	1.1 MHz to 6 GHz, Sinusoidal		<10		mVp-p

(1) In Single Supply Mode, the VIN, VDDIO and VDD_CDR supplies are 2.5 V. The VDD_LDO is the 1.8 V LDO output of an internal LDO regulator, the VDD_LDO pin should not be connected to any external supply voltage.
(2) In Dual Supply Mode, the VIN and VDD_LDO are connected to a 1.8 V supply, while the VDD_CDR and VDDIO supplies are 2.5 V.
(3) In Dual Supply Mode, the VDDIO supply should be powered before or at the same time as VIN and VDD_LDO = 1.8 V.
(4) The sum of the DC supply voltage and AC supply noise should not exceed the recommended supply voltage range.

6.4 Thermal Information

THERMAL METRIC[1][2]		LMH1226 RTW (QFN) 24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	33.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	28.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	11.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	11.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) No heat sink is assumed for these estimations. Depending on the application, a heat sink, faster air flow, and/or reduced ambient temperature (< 85°C) may be required in order to maintain the maximum junction temperature specified in *Electrical Characteristics*.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER						
PD_{DUAL}	Power Dissipation, Dual Supply Mode	Measured with PRBS-10, Locked to 11.88 Gbps, only OUT1 enabled		214		mW
PD_{Z_DUAL}	Power Dissipation, Dual Supply Mode	Power Save Mode, no input signal		16		mW
PD_{SINGLE}	Power Dissipation, Single Supply Mode	Measured with PRBS-10, Locked to 11.88 Gbps, only OUT1 enabled		227		mW
PD_{Z_SINGLE}	Power Dissipation, Single Supply Mode	Power Save Mode, no input signal		27		mW
IDD_{DUAL}	Current Consumption, Dual Supply Mode	Measured at 2.5 V supply with PRBS-10, Locked to 11.88 Gbps, VOD = Default, only OUT1 enabled		73	80	mA
		Measured at 1.8 V supply with PRBS-10, Locked to 11.88 Gbps, VOD = Default, only OUT1 enabled		17	25	
IDD_{Z_DUAL}	Current Consumption, Dual Supply Mode	Forced Power Save Mode, MODE_SEL = LEVEL-H, measured at 2.5 V supply		4	5	mA
		Forced Power Save Mode, MODE_SEL = LEVEL-H, measured at 1.8 V supply		3	9	
IDD_{TRANS_DUAL}	Current Consumption, Dual Supply Mode, Acquiring Lock, HEO/VEO Lock Monitor Disabled	Measured at 2.5 V supply with PRBS-10, Acquiring Lock, VOD = Default, OUT0 and OUT1 enabled		90	101	mA
		Measured at 1.8 V supply with PRBS-10, Acquiring Lock, VOD = Default, OUT0 and OUT1 enabled		30	37	
VDD_{LDO}	LDO 1.8 V Output Voltage	VIN = 2.5 V, Single Supply Mode	1.71	1.8	1.89	V

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LVCMOS DC SPECIFICATIONS						
V_{IH}	High Level Input Voltage	2-Level Input (SS_N, SCK, MOSI), VDDIO = 2.5 V	0.7 x VDDIO		VDDIO + 0.3	V
		2-Level Input (SCL, SDA), VDDIO = 2.5 V	0.7 x VDDIO		3.6	
V_{IL}	Low Level Input Voltage	2-Level Input (SS_N, SCK, MOSI), VDDIO = 2.5 V	-0.3		0.3 x VDDIO	V
		2-Level Input (SCL, SDA), VDDIO = 2.5 V	0		0.3 x VDDIO	
V_{OH}	High Level Output Voltage	IOH = -2 mA, (MISO), VDDIO = 2.5 V	0.8 x VDDIO		VDDIO	V
V_{OL}	Low Level Output Voltage	IOL = 2 mA, (MISO), VDDIO = 2.5 V	0		0.2 x VDDIO	V
		IOL = 3 mA, (LOCK_N, SCL, SDA), VDDIO = 2.5 V	0		0.4	
I_{IH}	Input High Leakage Current	SPI Mode: LVCMOS (SS_N, SCK, MOSI), Vinput = VDDIO			15	µA
		SMBus Mode: LVCMOS (LOCK_N, SCL, SDA), Vinput = VDDIO			10	
I_{IL}	Input Low Leakage Current	SPI: LVCMOS (SS_N), Vinput = VSS	-40			µA
		SPI: LVCMOS (SCK, MOSI), Vinput = VSS	-15			
		SMBus: LVCMOS (CD_N, SCL, SDA), Vinput = VSS	-10			
4-LEVEL LOGIC DC SPECIFICATIONS (REFERENCE TO VDDIO, APPLY TO ALL 4-LEVEL INPUT CONTROL PINS)						
$V_{4\_LVL\_H}$	LEVEL-H Input Voltage	Pull-up 1 kΩ to VDDIO		VDDIO		V
$V_{4\_LVL\_F}$	LEVEL-F Default Voltage	Float, VDDIO = 2.5 V		2/3 x VDDIO		V
$V_{4\_LVL\_R}$	LEVEL-R Input Voltage	External Pull-down 20 kΩ to VSS, VDDIO = 2.5 V		1/3 x VDDIO		V
$V_{4\_LVL\_L}$	LEVEL-L Input Voltage	External Pull-down 1 kΩ to VSS		0		V
$I_{4\_LVL\_IH}$	Input High Leakage Current	4-Levels (IN_OUT_SEL, OUT_CTRL, VOD_DE, MODE_SEL); Vinput = VDDIO	20	45	80	µA
		SMBus Mode: 4-Levels (ADDR0, ADDR1), Vinput = VDDIO	20	45	80	
$I_{4\_LVL\_IL}$	Input Low Leakage Current	4-Levels (IN_OUT_SEL, OUT_CTRL, VOD_DE, MODE_SEL), Vinput = VSS	-160	-93	-40	µA
		SMBus Mode: 4-Levels (ADDR0, ADDR1), Vinput = VSS	-160	-93	-40	

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RECEIVER SPECIFICATIONS (IN1±)						
R_{IN1_TERM}	DC Input Differential Termination	Measured across IN1+ to IN1-	80	100	120	Ω
RL_{IN1_SDD11}	Input Differential Return Loss (1)	SDD11, 10 MHz - 2.8 GHz		-21		dB
		SDD11, 2.8 GHz - 6 GHz		-17		
		SDD11, 6 GHz - 11.1 GHz		-8		
RL_{IN1_SCD11}	Differential to common mode Conversion (1)	SCD11, 10 MHz to 11.1 GHz		-23		dB
$V_{IN1\_CM\_TOL}$	Input AC Common Mode Voltage Tolerance			15		mV (rms)
V_{IN1_CM}	DC Common Mode Voltage	Input common mode voltage at IN1+ or IN1- to VSS		2.06		V
CD_{ON_IN1}	CD_N = LOW, Signal Detect (default), Assert ON Threshold Level	10.3125 Gbps, 1010 Clock Pattern		39		mVp-p
		10.3125 Gbps, PRBS-31 Pattern		25		
		11.88 Gbps, EQ and PLL Pathological Pattern		20		
CD_{OFF_IN1}	CD_N = HIGH, Signal Detect (default), De-assert OFF Threshold Level for	10.3125 Gbps, 1010 Clock Pattern		15		mVp-p
		10.3125 Gbps, PRBS-31 Pattern		15		
		11.88 Gbps, EQ and PLL Pathological Pattern		18		
TRANSMITTER OUTPUT (OUT0± AND OUT1±)						
V_{OD}	Output Differential Voltage (2)	8T pattern, VOD_DE = LEVEL-H, see Figure 13 SD, HD, 3G, 6G, 12G, and 10 GbE		410		mVp-p
		8T pattern, VOD_DE = LEVEL-F, see Figure 13 SD, HD, 3G, 6G, 12G, and 10 GbE	485	560	620	
		8T pattern, VOD_DE = LEVEL-R, see Figure 13 SD, HD, 3G, 6G, 12G, and 10 GbE		635		
		8T pattern, VOD_DE = LEVEL-L, see Figure 13 SD, HD, 3G, 6G, 12G, and 10 GbE		810		
VOD_{DE}	De-emphasized Output Differential Voltage (2)	8T pattern, VOD_DE = LEVEL-H, see Figure 13 SD, HD, 3G, 6G, 12G, and 10 GbE		410		mVp-p
		8T pattern, VOD_DE = LEVEL-F, see Figure 13 SD, HD, 3G, 6G, 12G, and 10 GbE		500		
		8T pattern, VOD_DE = LEVEL-R, see Figure 13 SD, HD, 3G, 6G, 12G, and 10 GbE		480		
		8T pattern, VOD_DE = LEVEL-L, see Figure 13 SD, HD, 3G, 6G, 12G, and 10 GbE		480		

(1) This parameter was measured with an LMH1219EVM.
(2) ATE production tested with DC method.

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{OUT_TERM}	DC Output Differential Termination	Measured across OUTn+ and OUTn-	80	100	120	Ω
t_R/t_F	Output Rise/Fall Time (1)	20% - 80% using 8T Pattern SMPTE SD, HD, 3G, 6G, 12G, and 10 GbE, measured after 1 inch trace		45		ps
$RL_{TX-SDD22}$	Output Differential Return Loss, Measured with the device powered up and outputs a 10 MHz clock signal. (1)	SDD22, 10 MHz - 2.8 GHz		-17		dB
		SDD22, 2.8 GHz - 6 GHz		-15		
		SDD22, 6 GHz - 11.1 GHz		-15		
$RL_{TX-SCC22}$	Output Common Mode Return Loss, measured with the device powered up and outputs a 10 MHz clock signal. (3)	SCC22, 10 MHz - 4.75 GHz		-12		dB
		SCC22, 4.75 GHz - 11.1 GHz		-12		
V_{TX_CM}	AC Common Mode Voltage (3)	Default Setting, PRBS-31, 10.3125 Gbps		5		mV (rms)
OUTPUT JITTER						
T_J	Total Jitter (BER≤1e-12), Reclocked Output (4)	11.88 Gbps, PRBS-10, 500 mVp-p and 1000 mVp-p launch amplitude, 20 inch FR4 board trace at IN1±		0.11	0.15	UI
		5.94 Gbps, PRBS-10, 500 mVp-p and 1000 mVp-p launch amplitude, 20 inch FR4 board trace at IN1±		0.106		UI
		2.97 Gbps, PRBS-10, 500 mVp-p and 1000 mVp-p launch amplitude, 20 inch FR4 board trace at IN1±		0.075		UI
		1.485 Gbps, PRBS-10, 500 mVp-p and 1000 mVp-p launch amplitude, 20 inch FR4 board trace at IN1±		0.07		UI
		270 Mbps, PRBS-10, 500 mVp-p and 1000 mVp-p launch amplitude, 20 inch FR4 board trace at IN1±		0.07		UI
		10.3125 Gbps, PRBS-10, 500 mVp-p and 1000 mVp-p launch amplitude, 20 inch FR4 board trace at IN1±		0.09	0.15	UI
R_J	Random Jitter, Reclocked Output	11.88 Gbps, PRBS-10, 500 mVp-p and 1000 mVp-p launch amplitude, 20 inch FR4 board trace at IN1±		5		mUI (rms)
		10.3125 Gbps, PRBS-10, 500 mVp-p and 1000 mVp-p launch amplitude, 20 inch FR4 board trace at IN1±		4.1		mUI (rms)
D_J	Deterministic Jitter, Reclocked Output	11.88 Gbps, PRBS-10, 500 mVp-p and 1000 mVp-p launch amplitude, 20 inch FR4 board trace at IN1±		40		mUI
		10.3125 Gbps, PRBS-10, 500 mVp-p and 1000 mVp-p launch amplitude, 20 inch FR4 board trace at IN1±		34		mUI

(3) This parameter was measured with an LMH1219EVM.
(4) These limits are ensured by bench characterization and are not production tested.

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TJ_{RAW}	Total Jitter (BER≤1e-12), RAW (Reclocker Bypassed)	125 Mbps, PRBS-10, 500 mVp-p and 1000 mVp-p launch amplitude, 20 inch FR4 board trace at IN1±		0.17		UI
		1.25 Gbps, PRBS-10, 500 mVp-p and 1000 mVp-p launch amplitude, 20 inch FR4 board trace at IN1±		0.17		
CLOCK AND DATA RECOVERY						
$LOCK_{RATE}$	Reclocker Lock Data Rates	SMPTE 12G, /1		11.88		Gbps
		SMPTE 12G, /1.001		11.868		Gbps
		SMPTE 6G, /1		5.94		Gbps
		SMPTE 6G, /1.001		5.934		Gbps
		SMPTE 3G, /1		2.97		Gbps
		SMPTE 3G, /1.001		2.967		Gbps
		SMPTE HD, /1		1.485		Gbps
		SMPTE HD, /1.001		1.4835		Gbps
		SMPTE SD, /1		270		Mbps
		10 GbE		10.3125		Gbps
$BYPASS_{RATE}$	Bypass reclocker data rate	MADI		125		Mbps
		1 GbE		1.25		Gbps
BW_{PLL}	PLL Bandwidth	Measured with 0.2 UI SJ at -3 dB, 10.3125 Gbps		8		MHz
		Measured with 0.2 UI SJ at -3 dB, 11.88 Gbps		13		
		Measured with 0.2 UI SJ at -3 dB, 5.94 Gbps		7		
		Measured with 0.2 UI SJ at -3 dB, 2.97 Gbps		5		
		Measured with 0.2 UI SJ at -3 dB, 1.485 Gbps		3		
		Measured with 0.2 UI SJ at -3 dB, 270 Mbps		1		
$J_{PEAKING}$	PLL Jitter Peaking	SD, HD, 3G, 6G, 12G, and 10 GbE		0.3		dB
J_{TOL_IN1}	IN1 Input Jitter Tolerance per SFF-8431 Appendix D.11	Total jitter tolerance combination of Dj, Pj, and Rj at 10 GbE, with RX stress eye mask Y1, Y2 limits		>0.7		UI
J_{TOL}	IN1 Input Jitter Tolerance with SJ	Sinusoidal jitter, tested at 3G, 6G and 12G; SJ amplitude low to high sweep, tested at BER ≤ 1e-12		0.65		UI
T_{LOCK}	Reclocker lock time	All supported data rates, disable HEO/VEO monitor		5		ms
$TEMP_{LOCK}$	VCO Lock with Temp Ramp	Lock Temperature Range (5 °C per min, ramp up and down), -40°C to 85°C operating range		125		°C
$T_{LATENCY}$	Reclocker Latency(5)	IN1, all supported data rates		1.5 UI + 190		ps
T_{PD-RAW}	Propagation Delay	Raw Data (reclocker bypassed), IN1± EQ = default		190		ps

(5) This parameter is data rate dependent. For example, at 11.88 Gbps, 1.5 UI = 1.5 x 84.17 ps = 126.25 ps. Therefore, $T_{Latency}$ = (126.25 + 190) ps = 316.25 ps.

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$FCLK_{OUT}$	Output Clock Frequency OUT1 Programmed to Output Recovered Clock	Operating at 11.88 Gbps		297		MHz
		Operating at 5.94 Gbps		297		MHz
		Operating at 2.97 Gbps		2.97		GHz
		Operating at 1.485 Gbps		1.485		GHz
		Operating at 270 Mbps		270		MHz

6.6 Recommended SMBus Interface AC Timing Specifications (1)(2)(3)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
F_{SCL}	SMBus SCL Frequency		10		400	kHz
T_{BUF}	Bus Free Time Between Stop and Start Condition		1.3			µs
$T_{HD:STA}$	Hold time after (Repeated) Start Condition. After this period, the first clock is generated.		0.6			µs
$T_{SU:STA}$	Repeated Start Condition Setup Time		0.6			µs
$T_{SU:STO}$	Stop Condition Setup Time		0.6			µs
$T_{HD:DAT}$	Data Hold Time		0			ns
$T_{SU:DAT}$	Data Setup Time		100			ns
T_{LOW}	Clock Low Period		1.3			µs
T_{HIGH}	Clock High Period		0.6			µs
T_R	Clock/Data Rise Time				300	ns
T_F	Clock/Data Fall Time				300	ns

(1) These parameters support SMBus 2.0 specifications.
(2) These parameters are not production tested.
(3) See Figure 1 for timing diagrams.

6.7 Serial Parallel Interface (SPI) AC Timing Specifications (1)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
F_{SCK}	SPI SCK Frequency			10	20	MHz
T_{SCK}	SCK Period		50			ns
T_{PH}	SCK Pulse Width High		0.40 x T_{SCK}			ns
T_{PL}	SCK Pulse Width Low		0.40 x T_{SCK}			ns
T_{SU}	MOSI Setup Time		4			ns
T_H	MOSI Hold Time		4			ns
T_{SSSU}	SS_N Setup Time		14			ns
T_{SSH}	SS_N Hold Time		4			ns
T_{SSOF}	SS_N Off Time		1			µs
T_{ODZ}	MISO Driven-to-Tristate Time			20		ns
T_{OZD}	MISO Tristate-to-Driven Time			10		ns
T_{OD}	MISO Output Delay Time			15		ns

(1) See Figure 2 for timing diagrams.

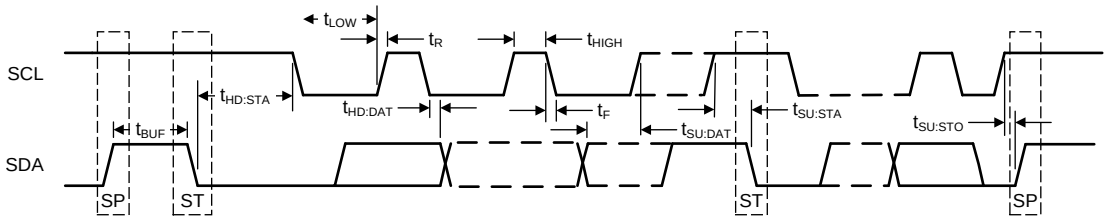


Figure 1. SMBUS Timing Parameters

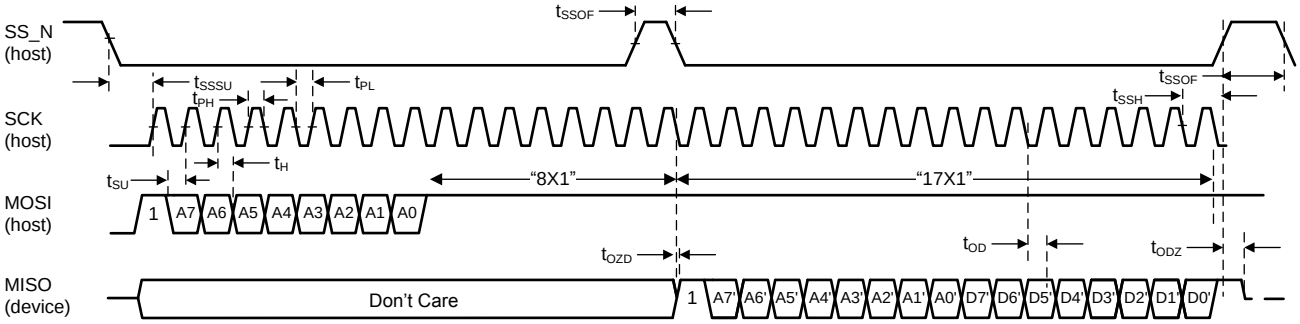


Figure 2. SPI Timing Parameters

6.8 Typical Characteristics

T_A = 25°C and VDD = 2.5 V (unless otherwise noted)

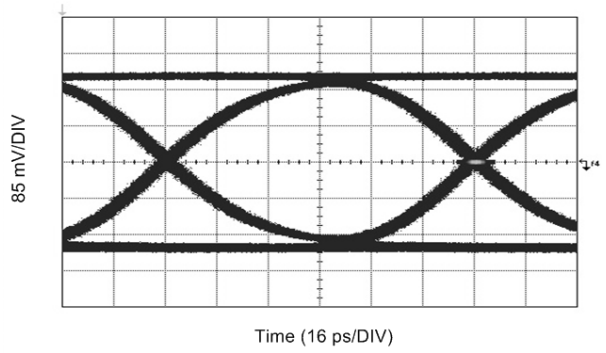


Figure 3. 10.3125 Gbps, Input: 20 in. FR4 Trace

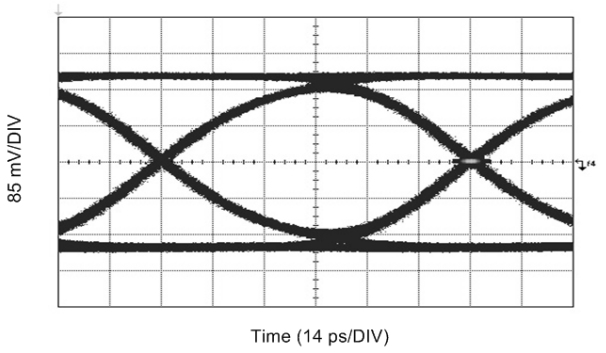


Figure 4. 11.88 Gbps, Input: 20 in. FR4 Trace

Typical Characteristics (continued)

T_A = 25°C and VDD = 2.5 V (unless otherwise noted)

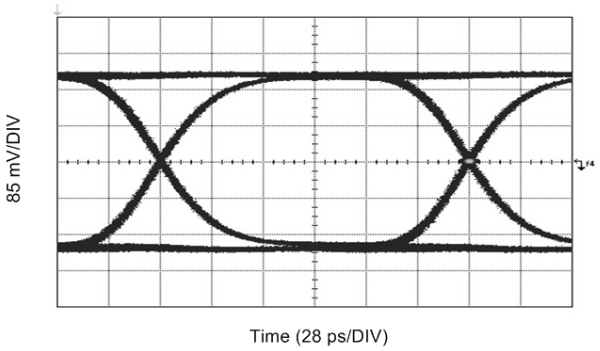


Figure 5. 5.94 Gbps, Input: 20 in. FR4 Trace

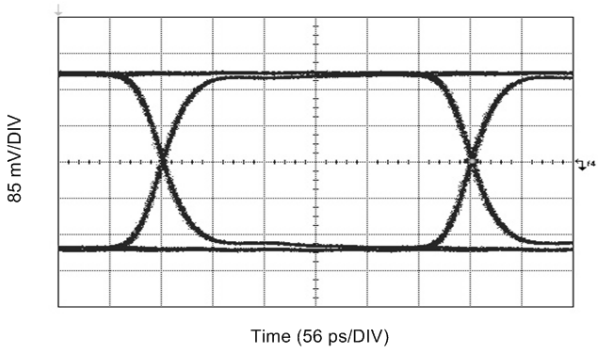


Figure 6. 2.97 Gbps, Input: 20 in. FR4 Trace

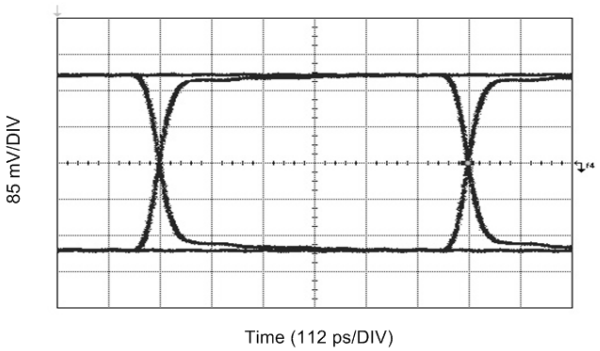


Figure 7. 1.485 Gbps, Input: 20 in. FR4 Trace

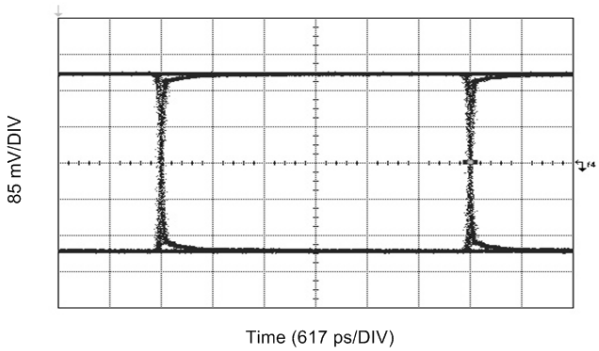


Figure 8. 270 Mbps, Input: 20 in. FR4 Trace

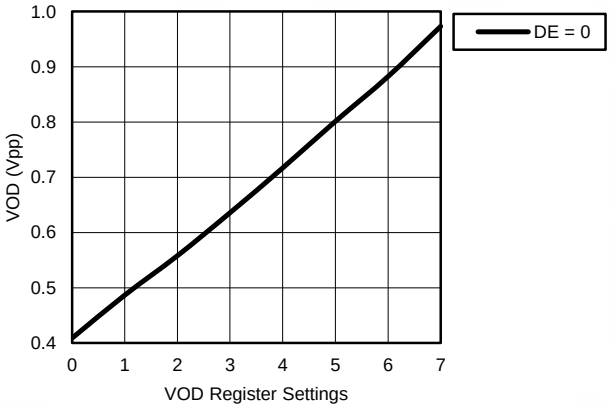


Figure 9. VOD vs. VOD and DEM Register Settings

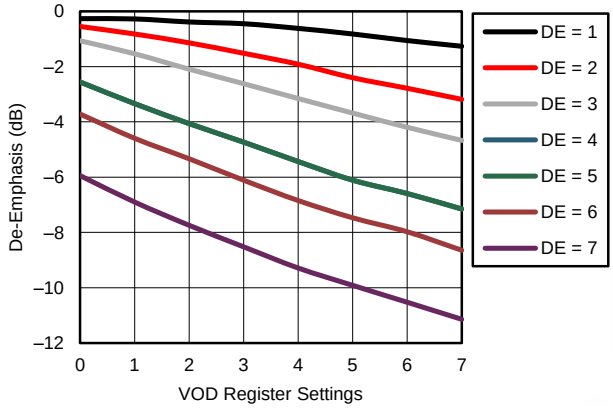


Figure 10. De-Emphasis vs. VOD and DEM Register Settings

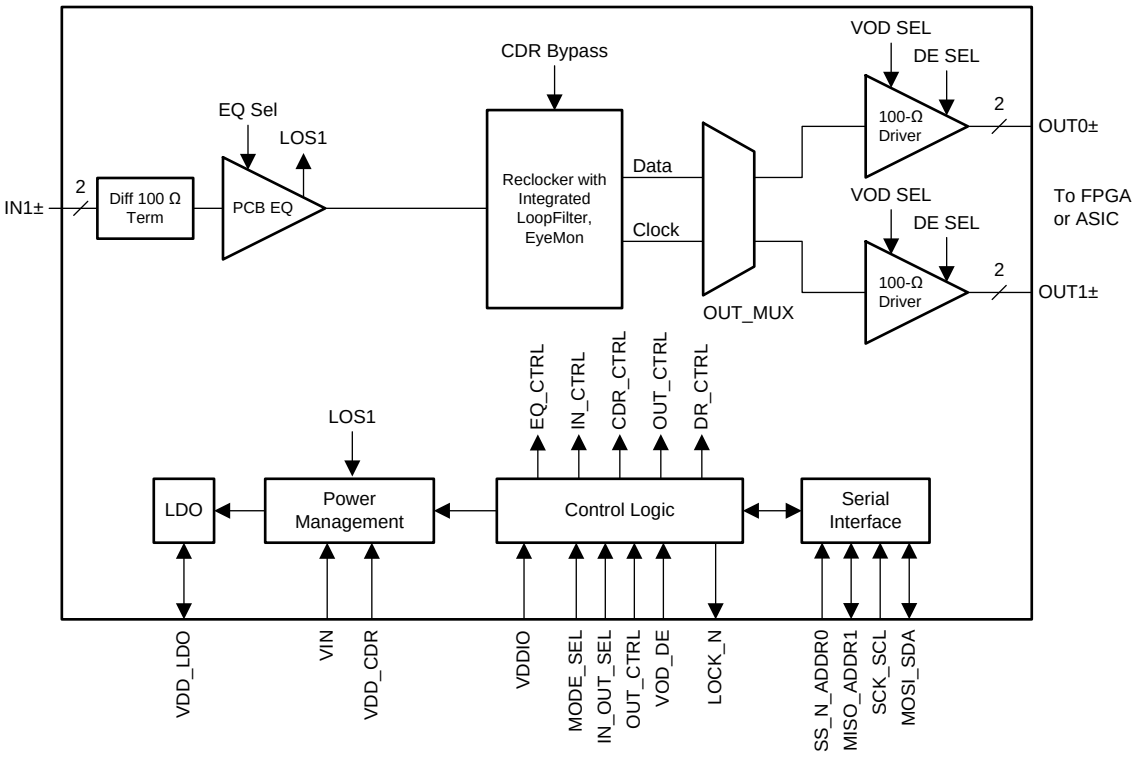
7 Detailed Description

7.1 Overview

The LMH1226 is a SMPTE and 10 GbE compatible multi-rate serial digital video reclocker for SMPTE ST-2081/2, ST-424, ST-292, ST-259, and 10 GbE SFF-8431 requirements. The LMH1226 has a 100-Ω PCB (printed circuit board) equalizer at IN1. The 100-Ω PCB equalizer input supports high speed signals across differential PCB traces that connect to an external SFF-8431 optical module or on-board FPGA. The input then passes through a multi-rate reclocker with a built-in loop-filter. The multi-rate reclocker is compatible with SMPTE data rates (11.88, 5.94, 2.97, 1.485 Gbps, 270 Mbps) and their divide-by-1.001 sub-rates. It is also compatible with the 10 GbE data rate (10.3125 Gbps). After the reclocker, an internal 1:2 fan-out mux allows users to select the data or clock content for each output. At both outputs, the LMH1226 has 100-Ω drivers with de-emphasis. The de-emphasis feature of the drivers is designed to compensate for insertion loss caused by output PCB traces.

The operating mode of the LMH1226 can be set by 4-level control pins, SPI, or SMBus serial control interface. The LMH1226 can be powered from a single 2.5 V supply or dual 2.5 V/1.8 V supplies for lower power consumption. The LMH1226 is offered in a small 4 mm x 4 mm 24-lead QFN package.

7.2 Functional Block Diagram



7.3 Feature Description

The LMH1226 consists of several key blocks:

- 4-Level Input Configuration Pins
- Input Carrier Detect
- Continuous Time Linear Equalizer (CTLE)
- Input-Output Mux Selection
- Clock and Data Recovery (CDR) Reclocker
- Internal Eye Opening Monitor (EOM)
- Output Function Control
- Output Driver Amplitude and De-Emphasis Control
- Status Indicators and Interrupts

7.3.1 4-Level Input Configuration Pins

The 4-level input configuration pins use a resistor divider to provide four logic states for each control pin. There is an internal 30-kΩ pull-up and a 60-kΩ pull-down connected to the control pin that sets the default voltage at 2/3 x VDDIO. These resistors, together with the external resistor, combine to achieve the desired voltage level. By using the 1-kΩ pull-down, 20-kΩ pull-down, no connect, and 1-kΩ pull-up, the optimal voltage levels for each of the four input states are achieved as shown in Table 1.

Table 1. 4-Level Control Pin Settings

LEVEL	SETTING	RESULTING PIN VOLTAGE
H	Tie 1 kΩ to VDDIO	VDDIO
F	Float (leave pin open)	2/3 × VDDIO
R	Tie 20 kΩ to VSS	1/3 × VDDIO
L	Tie 1 kΩ to VSS	0

Typical 4-Level Input Thresholds:

- Internal Threshold between L and R = 0.2 × VDDIO
- Internal Threshold between R and F = 0.5 × VDDIO
- Internal Threshold between F and H = 0.8 × VDDIO

7.3.2 Input Carrier Detect

The LMH1226 has a Carrier Detect circuit to monitor the presence or absence of the input signal. When the input signal amplitude surpasses the Carrier Detect assert threshold, the LMH1226 operates in normal mode.

In the absence of an input signal, the LMH1226 automatically goes into Power Save Mode to conserve power consumption. When a valid signal is detected, the LMH1226 automatically exits Power Save Mode and returns to the normal operating mode.

7.3.3 Continuous Time Linear Equalizer (CTLE)

The LMH1226 has a Continuous Time Linear Equalizer (CTLE) block for IN1. The CTLE compensates for frequency-dependent loss due to the transmission media prior to the device input. The CTLE accomplishes this by applying variable gain to the input signal, thereby boosting higher frequencies more than lower frequencies. The CTLE can be bypassed either by using the OUT_CTRL pin or via register control.

7.3.3.1 Adaptive PCB Trace Equalizer (IN1±)

The IN1 PCB equalizer has an on-chip 100-Ω termination and is designed for AC coupling, requiring a 4.7-µF AC coupling capacitor for minimizing base-line wander due to the rare-occurring pathological bit pattern. The PCB equalizer can compensate up to 20 inches of board trace at data rates up to 11.88 Gbps. There are two adapt modes for IN1: AM0 manual mode and AM1 adaptive mode. In AM0 manual mode, fixed EQ boost settings are applied through user-programmable register control, whereas in AM1 adaptive mode, state machines automatically find the optimal equalization setting from a set of 16 pre-determined settings defined in Registers 0x40-0x4F.

By default, AM1 adaptive mode is enabled at the data rate determined by the IN_OUT_SEL pin. The PCB equalizer is able to adapt at 10.3125 Gbps (10 GbE) and 2.97 Gbps, 5.94 Gbps, and 11.88 Gbps (SMPTE) data rates. At 1.485 Gbps and 270 Mbps data rates, the equalization is fixed at 0x00 (minimum EQ boost). This fixed EQ value can be changed via register control. For more details, refer to the LMH1226 Register Map.

7.3.4 Input-Output Mux Selection

By default, the LMH1226 input-to-output signal flow and data rate selection are configured by the IN_OUT_SEL pin logic settings shown in Table 2. These settings can be overridden via register control by applying the appropriate override bit values. For more information, refer to the LMH1226 Register Map.

Table 2. IN_OUT_SEL Pin Settings

LEVEL	DEFINITION
H	SMPTE Data Rates: IN1 to OUT0 and OUT1
F	SMPTE Data Rates: IN1 to OUT1 (OUT0 disabled)
R	10 GbE Data Rate: IN1 to OUT1 (OUT0 disabled)
L	10 GbE Data Rate: IN1 to OUT0 and OUT1

7.3.5 Clock and Data Recovery (CDR) Reclocker

After the input signal passes through the CTLE, the equalized data is fed into the clock and data recovery (CDR) block. Using an internal PLL, the CDR locks to the incoming equalized data and recovers a clean internal clock to re-sample the equalized data. The LMH1226 CDR is able to tolerate high input jitter, tracking low frequency input jitter below the PLL bandwidth while reducing high frequency input jitter above the PLL bandwidth.

The supported data rates are listed in Table 3. IN1 locks to either SMPTE or 10 GbE data rates according to the IN_OUT_SEL pin logic shown previously in Table 2. When locked to SMPTE data rates according to IN_OUT_SEL pin logic, IN1 can be programmed to lock to the 10 GbE data rate, and vice versa, via register control by applying the appropriate override bit values. For more information, refer to the LMH1226 Register Map.

Table 3. Supported Data Rates

IN_OUT_SEL LEVEL	DATA RATE	RECLOCKER MODE
H, F	11.88 Gbps, 5.94 Gbps, 2.97 Gbps, 1.485 Gbps, 270 Mbps(1)	Reclocker Enabled
	125 Mbps	Reclocker Disabled (CDR Bypassed)
R, L	10.3125 Gbps	Reclocker Enabled
	1.25 Gbps	Reclocker Disabled (CDR Bypassed)

(1) Divide-by-1.001 lock rates available only for 11.88 Gbps, 5.94 Gbps, 2.97 Gbps, and 1.485 Gbps.

NOTE

If the selected data rate (SMPTE or 10 GbE) is changed while the device is operating with active data, a CDR reset and release is required for the CDR to re-acquire lock. If the input data signal is toggled off and on after the selected data rate is changed, the Carrier Detect circuit will reset the CDR. In this case, no register write is needed for the CDR to re-acquire lock.

7.3.6 Internal Eye Opening Monitor (EOM)

The LMH1226 has an on-chip eye opening monitor (EOM) that can be used to analyze, monitor, and diagnose the post-equalized waveform, just prior to the CDR reclocker. The EOM is operational for 2.97 Gbps and higher data rates.

The EOM monitors the post-equalized waveform in a time window that spans one unit interval and a configurable voltage range that spans up to ±400 mV differential. The time window and voltage range are divided into 64 steps, so the result of the eye capture is a 64 × 64 matrix of *hits*, where each point represents a specific voltage and phase offset relative to the main data sampler. The number of *hits* registered at each point needs to be taken in context with the total number of bits observed at that voltage and phase offset in order to determine the corresponding probability for that point. The number of bits observed at each point is configurable.

The resulting 64 × 64 matrix produced by the EOM can be processed by software and visualized in a number of ways. Two common ways to visualize this data are shown in Figure 11 and Figure 12. These diagrams depict examples of eye monitor plots implemented by software. The first plot is an example using the EOM data to plot a basic eye using ASCII characters, which can be useful for simple diagnostic software. The second plot shows the first derivative of the EOM data, revealing the density of hits and the actual waveforms and crossings that comprise the eye.

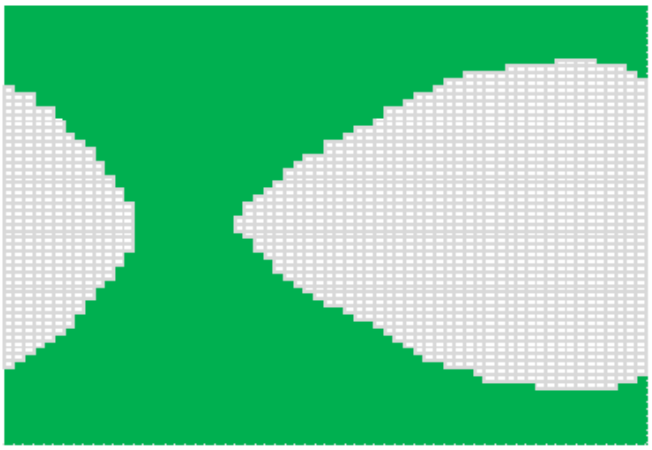


Figure 11. Internal Input Eye Monitor Plot

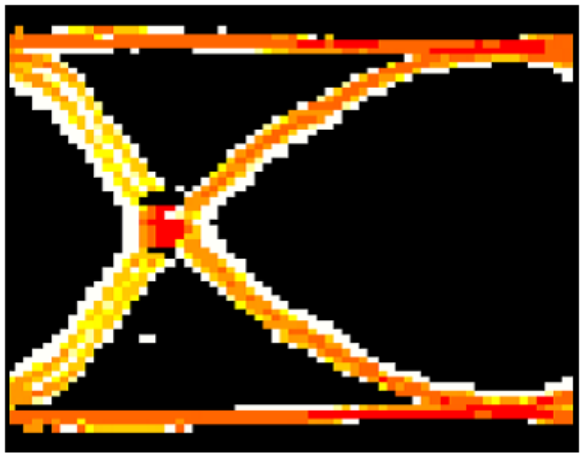


Figure 12. Internal Eye Monitor Hit Density Plot

A common measurement performed by the EOM is the horizontal and vertical eye opening. The horizontal eye opening (HEO) represents the width of the post-equalized eye at 0-V differential amplitude, measured in unit intervals or picoseconds (ps). The vertical eye opening (VEO) represents the height of the post-equalized eye, measured midway between the mean zero crossing of the eye. This position in time approximates the CDR sampling phase.

7.3.7 Output Function Control

By default, the LMH1226 output function control for OUT0 and OUT1 is configured by the OUT_CTRL pin logic settings shown in Table 4. These settings can be overridden via register control by applying the appropriate override bit values. For more information, refer to the LMH1226 Register Map.

Table 4. OUT_CTRL Pin Settings

LEVEL	DEFINITION
H	OUT0 and OUT1: Raw Data, Both EQ and Reclocker Bypassed
F	OUT0 and OUT1: Recovered Data, Both EQ and Reclocker Enabled
R	OUT0: Recovered Data, EQ and Reclocker Enabled OUT1: Full-Rate Recovered Clock if Data Rate ≤ 3 Gbps. 297 MHz Recovered Clock if Data Rate > 3 Gbps(1)
L	OUT0 and OUT1: Equalized Data, EQ Enabled, Reclocker Bypassed

(1) This setting is only valid for SMPTE data rates. It is not supported for the 10 GbE data rate.

7.3.8 Output Driver Amplitude and De-Emphasis Control

The VOD_DE control pin selects the output amplitude and de-emphasis settings for both OUT0 and OUT1. It offers users the capability to select higher output amplitude and de-emphasis levels for longer board trace that connects the drivers to their downstream receivers. Driver de-emphasis provides transmitter equalization to reduce the ISI caused by the board trace.

By default, the output driver VOD and de-emphasis settings are configured by the VOD_DE pin logic settings shown in Table 5. These settings can be overridden via register control by applying the appropriate override bit values. When these parameters are controlled by registers, the VOD and de-emphasis levels for each channel can be programmed independently. For more information, refer to the LMH1226 Register Map.

Table 5. Recommended VOD_DE Pin and Register Settings for Different FR4 Trace Lengths (1)

VOD_DE LEVEL	VOD REG SETTING OUT0±: 0x30[5]=1, 0x30[2:0] OUT1±: 0x32[5]=1, 0x32[2:0]	DEM REG SETTING OUT0±: 0x31[6]=1, 0x31[2:0] OUT1±: 0x33[6]=1, 0x33[2:0]	VOD (mVpp) (2)	VOD_{DE} (mVpp) (2)	DEM (dB)	FR4 TRACE LENGTH (inches)
H	0	0	410	410	0	0 – 1
F	2	2	560	500	-0.9	2 – 4
R	3	3	635	480	-2.4	5 – 6
L	5	5	810	480	-6.1	7 – 8

(1) The output drivers are capable of providing higher VOD and DEM levels (max settings are 7). For more VOD and de-emphasis levels, refer to 表 10.
(2) See Figure 13.

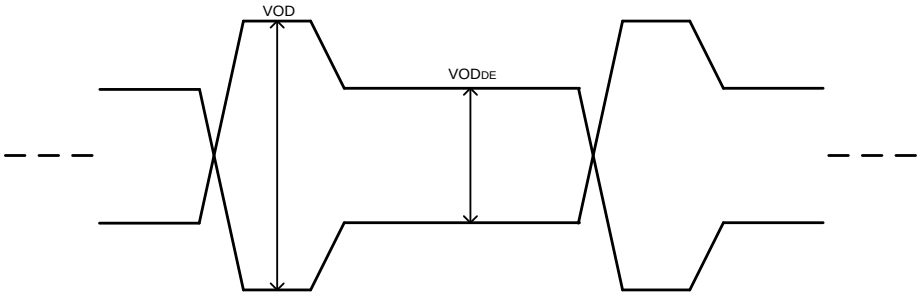


Figure 13. VOD and VOD_{DE} Levels

7.3.9 Status Indicators and Interrupts

7.3.9.1 LOCK_N (Lock Indicator)

The LOCK_N pin is a 3.3 V tolerant, active-low open drain output. An external resistor to the logic supply is required. By default, LOCK_N is the reclocker lock indicator, and this pin asserts low when the LMH1226 achieves lock to a valid SMPTE or 10 GbE data rate. The LOCK_N pin functionality can also be configured via register control to indicate CD_N (Carrier Detect) or INT_N (Interrupt) events. For more information about how to reconfigure the LOCK_N pin functionality, refer to the LMH1226 Register Map.

7.3.9.2 CD_N (Carrier Detect)

The LOCK_N pin can be reconfigured via register control to indicate a CD_N (Carrier Detect) event. When configured as a CD_N output, the pin asserts low at the end of adaptation after a valid signal is detected by the Carrier Detect circuit. Under register control, this pin can be reconfigured to indicate CD_N. For more information about how to configure the LOCK_N pin for CD_N functionality, refer to the LMH1226 Register Map.

7.3.9.3 INT_N (Interrupt)

The LOCK_N pin can be configured to indicate an INT_N (Interrupt) event. When configured as an INT_N output, the pin asserts low when an interrupt occurs, according to the programmed interrupt masks. Five separate masks can be programmed via register control as interrupt sources:

- If there is a Loss of Signal (LOS) event on IN1 (2 separate masks).
- If HEO or VEO falls below a certain threshold after CDR is locked (1 mask).

- If a CDR Lock event has occurred (2 separate masks).

INT_N is a sticky bit, meaning that it will flag after an interrupt event occurs and will not clear until read back. Once the Interrupt Status Register is read, the INT_N pin will assert high again. For more information about how to configure the LOCK_N pin for INT_N functionality, refer to the LMH1226 Register Map.

7.4 Device Functional Modes

The LMH1226 operates in one of two modes: System Management Bus (SMBus) or Serial Peripheral Interface (SPI) mode. In order to determine the mode of operation, the proper setting must be applied to the MODE_SEL pin at power-up, as detailed in Table 6.

Table 6. MODE_SEL Pin Settings

LEVEL	DEFINITION
H	Forced Power Save Mode, only SPI is enabled (all other circuitry powered down)
F	Select SPI Interface for register access
R	Reserved for factory testing – do not use
L	Select SMBus Interface for register access

NOTE

Changing logic states between LEVEL-L and LEVEL-H after power up is not allowed.

7.4.1 System Management Bus (SMBus) Mode

If MODE_SEL = L, the LMH1226 is in SMBus mode. In SMBus mode, Pins 10 and 21 are configured as SDA and SCL. Pins 7 and 20 act as 4-level address straps for ADDR0 and ADDR1 at power up to determine the 7-bit slave address of the LMH1226, as shown in Table 7.

Table 7. SMBus Device Slave Addresses(1)

ADDR0 (LEVEL)	ADDR1 (LEVEL)	7-BIT SLAVE ADDRESS [HEX]	8-BIT WRITE COMMAND [HEX]
L	L	1D	3A
L	R	1E	3C
L	F	1F	3E
L	H	20	40
R	L	21	42
R	R	22	44
R	F	23	46
R	H	24	48
F	L	25	4A
F	R	26	4C
F	F	27	4E
F	H	28	50
H	L	29	52
H	R	2A	54
H	F	2B	56
H	H	2C	58

(1) The 8-bit write command consists of the 7-bit slave address (Bits 7:1) with 0 appended to the LSB to indicate an SMBus write. For example, if the 7-bit slave address is 0x1D (001 1101'b), the 8-bit write command is 0x3A (0011 1010'b).

7.4.1.1 SMBus Read and Write Transactions

SMBus is a two-wire serial interface through which various system component chips can communicate with the master. Slave devices are identified by having a unique device address. The two-wire serial interface consists of SCL and SDA signals. SCL is a clock output from the master to all of the slave devices on the bus. SDA is a bidirectional data signal between the master and slave devices. The LMH1226 SMBus SCL and SDA signals are open drain and require external pull-up resistors.

Start and Stop:

The master generates start and stop patterns at the beginning and end of each transaction.

- Start: High to low transition (falling edge) of SDA while SCL is high.
- Stop: Low to high transition (rising edge) of SDA while SCL is high.

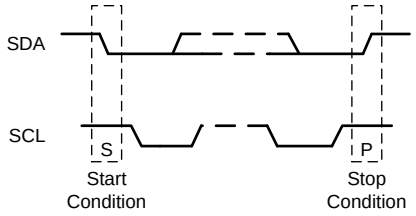


Figure 14. Start and Stop Conditions

The master generates nine clock pulses for each byte transfer. The 9th clock pulse constitutes the ACK cycle. The transmitter releases SDA to allow the receiver to send the ACK signal. An ACK is recorded when the device pulls SDA low, while a NACK is recorded if the line remains high.

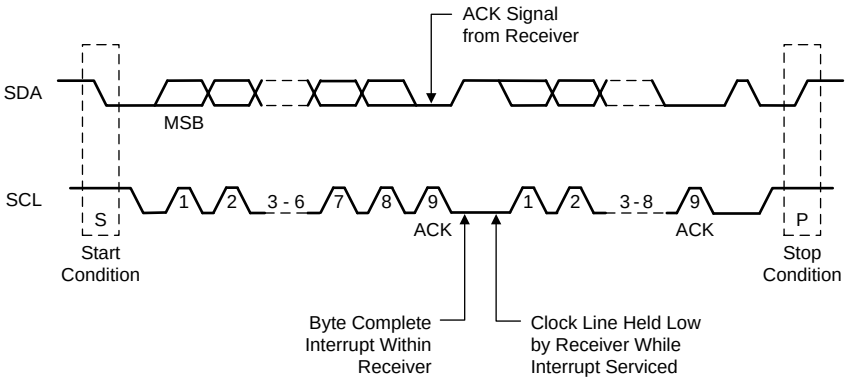


Figure 15. Acknowledge (ACK)

7.4.1.1.1 SMBus Write Operation Format

Writing data to a slave device consists of three parts, as illustrated in Figure 16:

1. The master begins with a start condition, followed by the slave device address with the R/$\overline{W}$ bit set to 0'b.
2. After an ACK from the slave device, the 8-bit register word address is written.
3. After an ACK from the slave device, the 8-bit data is written, followed by a stop condition.

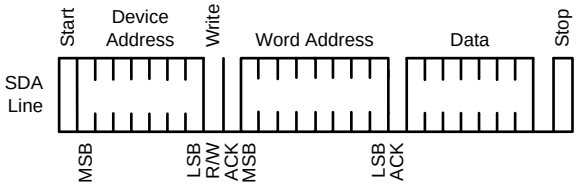


Figure 16. SMBus Write Operation

7.4.1.1.2 SMBus Read Operation Format

Reading data from a slave device consists of four parts, as illustrated in Figure 17:

1. The master begins with a start condition, followed by the slave device address with the R/$\overline{W}$ bit set to 0'b.
2. After an ACK from the slave device, the 8-bit register word address is written.
3. After an ACK from the slave device, the master initiates a re-start condition, followed by the slave address with the R/$\overline{W}$ bit set to 1'b.
4. After an ACK from the slave device, the 8-bit data is read back. The last ACK is high if there are no more bytes to read, and the last read is followed by a stop condition.

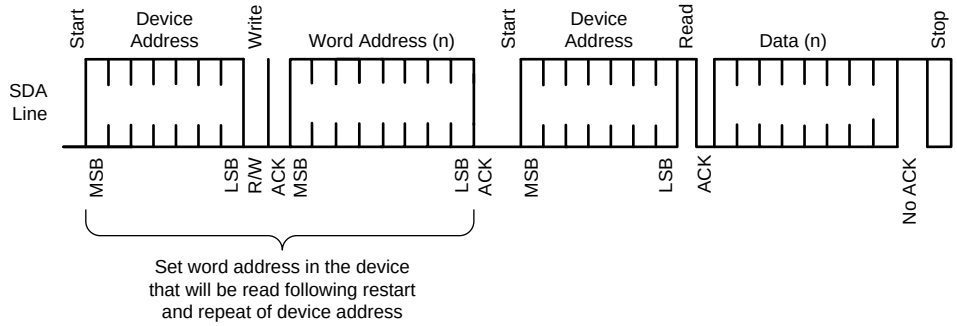


Figure 17. SMBus Read Operation

7.4.2 Serial Peripheral Interface (SPI) Mode

If MODE_SEL = F or H, the LMH1226 is in SPI mode. In SPI mode, the following pins are used for SPI bus communication:

- MOSI (pin 10): Master Output Slave Input
- MISO (pin 20): Master Input Slave Output
- SS_N (pin 7): Slave Select (active low)
- SCK (pin 21): Serial clock (input to the LMH1226 slave device)

7.4.2.1 SPI Read and Write Transactions

Each SPI transaction to a single device is 17 bits long and is framed by SS_N when asserted low. The MOSI input is ignored, and the MISO output is floated whenever SS_N is de-asserted (high).

The bits are shifted in left-to-right. The first bit is R/$\overline{W}$, which is 1'b for "read" and 0'b for "write." Bits A7-A0 are the 8-bit register address, and bits D7-D0 are the 8-bit read or write data. The previous SPI command, address, and data are shifted out on MISO as the current command, address, and data are shifted in on MOSI. In all SPI transactions, the MISO output signal is enabled asynchronously when SS_N asserts low. The contents of a single MOSI or MISO transaction frame are shown in Table 8.

Table 8. 17-Bit Single SPI Transaction Frame

R/$\overline{W}$	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0

7.4.2.1.1 SPI Write Transaction Format

For SPI writes, the R/$\overline{W}$ bit is 0'b. SPI write transactions are 17 bits per device, and the command is executed on the rising edge of SS_N. The SPI transaction always starts on the rising edge of the clock.

The signal timing for a SPI Write transaction is shown in Figure 18. The "prime" values on MISO (for example, A7') reflect the contents of the shift register from the previous SPI transaction and are *don't-care* for the current transaction.

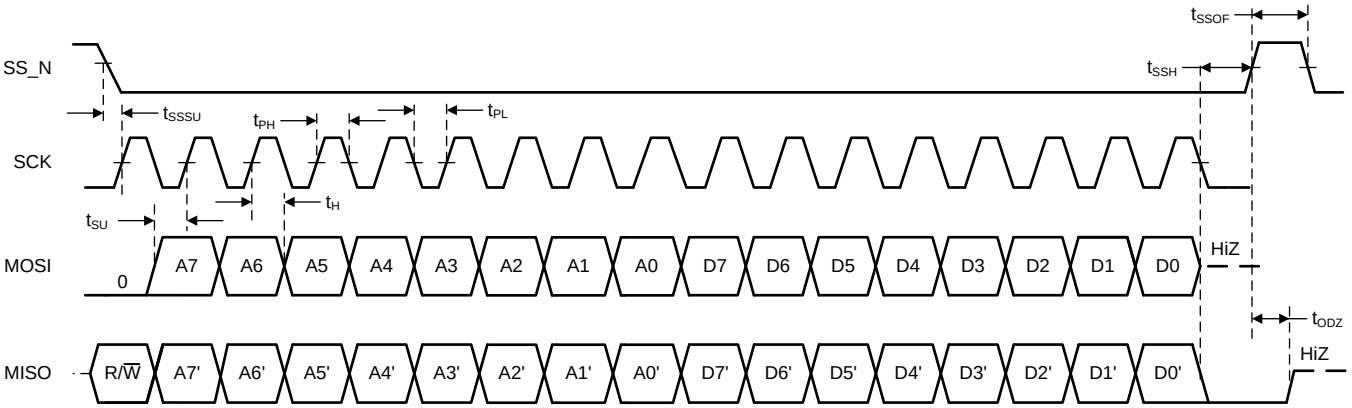


Figure 18. Signal Timing for a SPI Write Transaction

7.4.2.1.2 SPI Read Transaction Format

A SPI read transaction is 34 bits per device and consists of two 17-bit frames. The first 17-bit read transaction frame shifts in the address to be read, followed by a dummy transaction second frame to shift out 17-bit read data. The R/$\overline{W}$ bit is 1'b for the read transaction, as shown in Figure 19.

The first 17 bits from the read transaction specifies 1-bit of R/$\overline{W}$ and 8-bits of address A7-A0 in the first 8 bits. The eight 1's following the address are ignored. The second dummy transaction acts like a read operation on address 0xFF and needs to be ignored. However, the transaction is necessary in order to shift out the read data D7-D0 in the last 8 bits of the MISO output. As with the SPI Write, the "prime" values on MISO during the first 16 clocks are *don't-care* for this portion of the transaction. The values shifted out on MISO during the last 17 clocks reflect the read address and 8-bit read data for the current transaction.

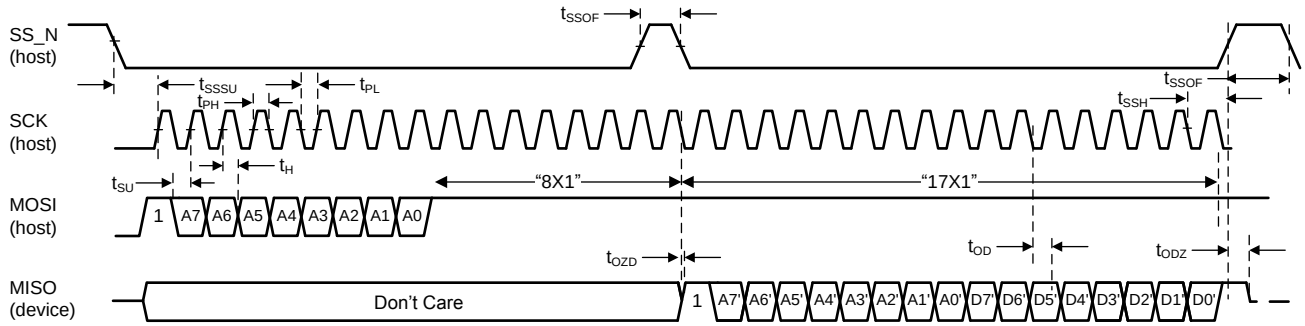


Figure 19. Signal Timing for a SPI Read Transaction

7.4.2.2 SPI Daisy Chain

The LMH1226 supports SPI daisy-chaining among multiple devices, as shown in Figure 20.

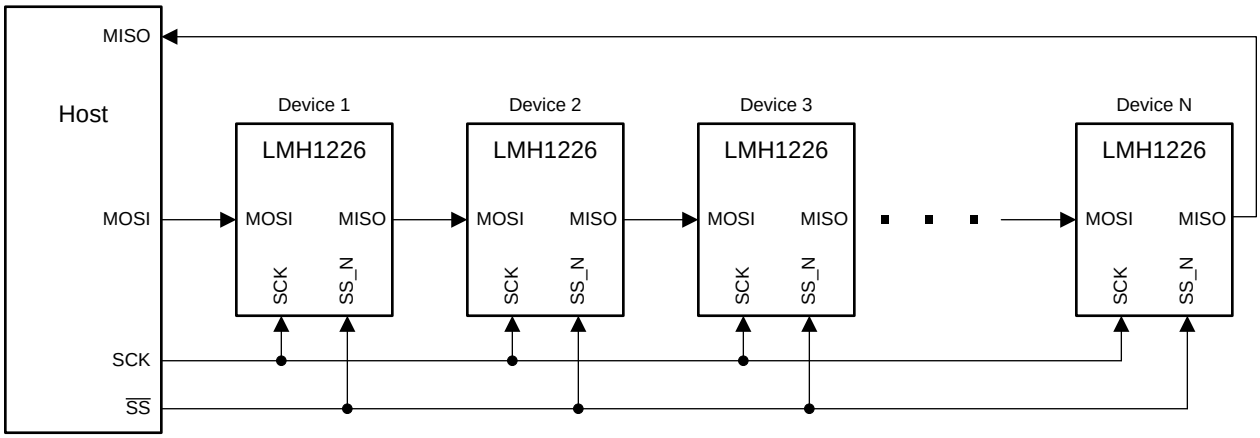


Figure 20. Daisy-Chain Configuration

Each LMH1226 device is directly connected to the SCK and SS_N pins of the host. The first LMH1226 device in the chain is connected to the host's MOSI pin, and the last device in the chain is connected to the host's MISO pin. The MOSI pin of each intermediate LMH1226 device in the chain is connected to the MISO pin of the previous LMH1226 device, thereby creating a serial shift register. In a daisy-chain configuration of N x LMH1226 devices, the host conceptually sees a shift register of length 17 x N for a basic SPI transaction, during which SS_N is asserted low for 17 x N clock cycles.

7.5 LMH1226 Register Map

The LMH1226 register map is divided into three register pages. These register pages are used to control different aspects of the LMH1226 functionality. A brief summary of the pages is shown below:

1. **Share Register Page**: This page corresponds to global parameters, such as LMH1226 device ID and LOCK_N status configuration. This is the default page at start-up.
2. **CTLE/CDR Register Page**: This page corresponds to IN1 PCB CTLE, input and output mux settings, internal CDR settings, and output interrupt overrides. Access this page by setting Reg 0xFF[2:0] = 100'b.
3. **Drivers Register Page**: This page corresponds to both OUT0 and OUT1 driver output settings. Access this page by setting Reg 0xFF[2:0] = 101'b.

Please note the following about the LMH1226 default register values in the register map:

- Default register values were read after power-up with no active inputs applied to IN1.
- Default register values for Reserved "Read-Only" bits may vary dynamically from part to part.

7.5.1 Share Register Page

Address	Register Name	Bit	Field	Default	Type	Description
0x00	Reserved	7:0	Reserved	0x00	R	Reserved
0x01	Reserved	7:0	Reserved	0x40	R	Reserved
0x02	Reserved	7:0	Reserved	0x02	RW	Reserved
0x03	Reserved	7:0	Reserved	0x00	RW	Reserved
0x04	Reserved	7:0	Reserved	0x01	RW	Reserved
0x05	Reserved	7:0	Reserved	0x00	RW	Reserved
0x06	Reserved	7:0	Reserved	0x00	RW	Reserved
0x07	Reserved	7:0	Reserved	0x04	RW	Reserved
0x08	Reserved	7:0	Reserved	0x11	RW	Reserved
0x09	Reserved	7:0	Reserved	0x00	R	Reserved
0xE2	Reset Share/Channel Regs	7:5	Reserved	0x10	R	Reserved
		4	reset_done		R	0 = Internal state machine register initialization not done. 1 = Internal state machine register initialization done.
		3:1	Reserved		RW	Reserved
		0	reset_init		RW	1 = Initialize internal state machine register settings. Refer to the LMH1219 Programming Guide for details.
0xF0	Device Revision	7:0	Version	0x02	R	Device Revision
0xF1	Device ID	7:0	Device_ID	0x86	R	For LMH1226, Device ID = 0x86
0xFF	Register Communication Control	7:6	Reserved	0x00	RW	Reserved
		5:4	los_int_bus_sel		RW	Controls the output on LOCK_N pin 00 = Default behavior (LOCK_N outputs lock status from reclocker) 01 = Reserved 10 = LOS of IN1 11 = Interrupts are output on LOCK_N pin, as determined by CTLE/CDR Page Reg 0x56[6:0]
		3	Reserved		RW	Reserved
		2	page_select_enable		RW	0 = The shared registers are enabled. 1 = Enables communication access to the Register Page specified in Reg 0xFF[1:0].
		1:0	page_select		RW	Enable communication access to a specific Register Page 00 = CTLE/CDR Register Page 01 = Drivers Register Page Other settings are invalid.

7.5.2 CTLE/CDR Register Page

Address	Register Name	Bit	Field	Default	Type	Description
0x00	Reset CTLE/CDR Registers	7:3	Reserved	0x00	RW	Reserved
		2	rst_CTLE/CDR_regs		RW	Reset registers (self-clearing) 0 = Normal Operation 1 = Reset CTLE/CDR Registers. Register re-initialization procedure required after resetting the CTLE/CDR Registers.
		1:0	Reserved		RW	Reserved
0x01	LOS Status	7:2	Reserved	0x03	RW	Reserved
		1	LOS1		R	0 = Signal Present on IN1 1 = Loss of Signal on IN1
		0	Reserved		R	Reserved
0x02	CDR_Status	7:0	CDR_Status	0x41	R	CDR status indicator. See "Lock Data Rate Indication" subsection in the LMH1219 Programming Guide for more information.
0x03	IN1 Manual EQ Boost	7:6	eq_BST0	0x80	RW	Used for setting manual EQ value for IN1 when Reg 0x2D[3] = 1. EQ boost value can be read back on CTLE/CDR Page Reg 0x52. [7:6]: 2-bit control for Stage 0 of the CTLE. [5:4]: 2-bit control for Stage 1 of the CTLE. [3:2]: 2-bit control for Stage 2 of the CTLE. [1:0]: 2-bit control for Stage 3 of the CTLE.
		5:4	eq_BST1		RW	
		3:2	eq_BST2		RW	
		1:0	eq_BST3		RW	
0x04	Reserved	7:0	Reserved	0x00	RW	Reserved
0x05	Reserved	7:0	Reserved	0x00	RW	Reserved
0x06	Reserved	7:0	Reserved	0x00	RW	Reserved
0x07	Reserved	7:0	Reserved	0x00	RW	Reserved
0x08	Reserved	7:0	Reserved	0x00	RW	Reserved
0x09	Output Mux Override Control	7:6	Reserved	0x00	RW	Reserved
		5	reg_out_control_ov		RW	Output Mux Override Control 0 = Reg 0x1C[3:2] determines the output selection for both OUT0 and OUT1 1 = Enable individual output mux control based on values from Reg 0x1C[7:5] and Reg 0x1E[7:5]
		4:3	Reserved		RW	Reserved
		2:0	Reserved		RW	Reserved
0x0A	CDR Reset Control	7:4	Reserved	0x50	RW	Reserved
		3	reg_cdr_reset_ov		RW	0 = Disables CDR Reset (Normal Operating Mode) 1 = Enables Reg 0x0A[2] to control CDR Reset
		2	reg_cdr_reset		RW	0 = No CDR Reset if Reg 0x0A[3] = 1 1 = CDR Reset if Reg 0x0A[3] = 1
		1:0	Reserved		RW	Reserved
0x0B	Reserved	7:0	Reserved	0x1F	RW	Reserved
0x0C	CDR Output Status Control	7:4	reg_sh_status_control	0x08	RW	Value determines what CDR status outputs are displayed in CTLE/CDR Page Reg 0x02. See "Lock Data Rate Indication" subsection in the LMH1219 Programming Guide for more information.
		3:0	Reserved		RW	Reserved
0x0D	Reserved	7:0	Reserved	0x00	RW	Reserved
0x0E	Reserved	7:0	Reserved	0x93	RW	Reserved
0x0F	Reserved	7:0	Reserved	0x69	RW	Reserved
0x10	Reserved	7:0	Reserved	0x27	RW	Reserved

Address	Register Name	Bit	Field	Default	Type	Description
0x11	EOM Voltage Range Control	7:6	eom_sel_vrange	0xE0	RW	Sets the expected incoming eye diagram vertical eye opening interval if Reg 0x2C[6] = 0 00 = 3.125 mV (3.125 mV x 64 = 200 mV; ±100 mV range) 01 = 6.25 mV (6.25 mV x 64 = 400 mV; ±200 mV range) 10 = 9.375 mV (9.375 mV x 64 = 600 mV; ±300 mV range) 11 = 12.5 mV (12.5 mV x 64 = 800 mV; ±400 mV range)
		5	eom_PD		RW	0 = EOM is always powered up 1 = Power down EOM when not in use
		4:0	Reserved		RW	Reserved
0x12	Reserved	7:0	Reserved	0xA0	RW	Reserved
0x13	IN1 Carrier Detect and CTLE Control	7:4	Reserved	0x90	RW	Reserved
		3	eq_PD_EQ		RW	IN1 CTLE Power-Down Control 0 = Powers up EQ of IN1 1 = Powers down EQ of IN1 Note: The un-selected channel is always powered-down.
		2	Reserved		RW	Reserved
		1	eq_en_bypass		RW	0 = Enable Gain Stages 2 and 3 of IN1 CTLE 1 = Bypass Gain Stages 2 and 3 of IN1 CTLE
		0	Reserved		RW	Reserved
0x14	Reserved	7:0	Reserved	0x00	RW	Reserved
0x15	IN1 Carrier Detect Threshold Setting	7	Reserved	0x00	RW	Reserved
		6	cd_1_PD		RW	IN1 Carrier Detect Power Down Control 0 = Power Up IN1 Carrier Detect 1 = Power Down IN1 Carrier Detect
		5:4	cd_1_refa_sel		RW	Controls IN1 Carrier Detect Assert and De-Assert Thresholds 0000 = Default levels (nominal) 0101 = Nominal - 2 mV 1010 = Nominal + 5 mV 1111 = Nominal + 3 mV
		3:2	cd_1_refd_sel		RW	
		1:0	Reserved		RW	Reserved
0x16	Reserved	7:0	Reserved	0x25	RW	Reserved
0x17	Reserved	7:0	Reserved	0x25	RW	Reserved
0x18	Reserved	7:0	Reserved	0x40	RW	Reserved
0x19	Reserved	7:0	Reserved	0x00	RW	Reserved
0x1A	Reserved	7:0	Reserved	0xA0	RW	Reserved
0x1B	Reserved	7:0	Reserved	0x03	RW	Reserved

Address	Register Name	Bit	Field	Default	Type	Description
0x1C	OUT Mux Select_0	7:5	out_sel0_data_mux	0x58	RW	In normal operating mode, Reg 0x1C[7:5] returns the mux select value applied at OUT0. When Reg 0x09[5] = 1, OUT0 mux selection is controlled by Reg 0x1C[7:5] as follows: 000 = Mute 001 = 10 MHz Clock 010 = Raw Data (EQ Only) 100 = Retimed Data Other Settings are invalid.
		4	VCO_Div40		RW	When Reg 0x09[5] = 1 and Reg 0x1E[7:5] = 101'b, OUT1 clock selection can be controlled by Reg 0x1C[4] as follows: 0 = OUT1 outputs 10 MHz clock 1 = OUT1 outputs VCO divide-by-40
		3:2	drv_out_ctrl		RW	Controls output mux selection for both OUT0 and OUT1 if Reg 0x3F[3] = 1 to override the OUT_CTRL pin 00 = Mute both OUT0 and OUT1 01 = When CDR is locked, output reclocked data on OUT0 and output clock on OUT1. If locked data rate is ≤ 3G, OUT1 = VCO. If locked data rate is > 3G, OUT1 = VCO/40. When unlocked, output raw data on OUT0 and mute OUT1. 10 = When locked, output retimed data on both OUT0 and OUT1. When unlocked, output raw data on both OUT0 and OUT1. This is the default setting. 11 = Output raw data on both OUT0 and OUT1.
		1:0	Reserved		RW	Reserved
0x1D	Reserved	7:0	Reserved	0x00	RW	Reserved
0x1E	OUT Mux Select_1	7:5	out_sel1_data_mux	0x09	RW	In normal operating mode, Reg 0x1E[7:5] returns the mux select value applied at OUT1. When Reg 0x09[5] = 1, OUT1 mux selection is controlled by Reg 0x1E[7:5] as follows: 000 = Raw Data (EQ Only) 001 = Retimed Data 010 = Full Rate VCO clock 101 = 10 MHz Clock if Reg 0x1C[4] = 0 and VCO/40 clock if Reg 0x1C[4] = 1 111 = Mute Other Settings are invalid
		4:0	Reserved		RW	Reserved
0x1F	OUT1 Polarity	7	sel_inv_out1	0x10	RW	0 = OUT1 normal polarity 1 = Inverts OUT1 driver polarity Note: No polarity inversion for OUT0
		6:0	Reserved		RW	Reserved
0x20	Reserved	7:0	Reserved	0x00	RW	Reserved
0x21	Reserved	7:0	Reserved	0x00	RW	Reserved
0x22	Reserved	7:0	Reserved	0x00	RW	Reserved
0x23	HEO_VEO_OV	7	eom_get_heo_ veo_ov	0x40	RW	0 = Disable HEO/VEO Acquisition override. 1 = Enable HEO/VEO Acquisition override. Value determined by Reg 0x24[1].
		6:0	Reserved			Reserved
0x24	EOM Control	7	fast_eom	0x40	RW	0 = Disable Fast EOM mode 1 = Enable Fast EOM mode
		6	Reserved		R	Reserved
		5	get_heo_veo_error_ no_hits		R	Zero Crossing Error Detector Status 0 = Zero crossing errors in the eye diagram observed 1 = No zero crossing errors in the eye diagram observed
		4	get_heo_veo_error_ no_opening		R	Vertical Eye Closure Detector Status 0 = Open eye diagram detected 1 = Eye diagram completely closed
		3:2	Reserved		R	Reserved
		1	eom_get_heo_veo		RW	1 = Acquire HEO and VEO (self-clearing) if Reg 0x23[7] = 1
		0	eom_start		RW	1 = Start EOM counter (self-clearing)

Address	Register Name	Bit	Field	Default	Type	Description
0x25	EOM_MSB	7:0	eom_count_msb	0x00	R	MSBs of EOM counter
0x26	EOM_LSB	7:0	eom_count_lsb	0x00	R	LSBs of EOM counter
0x27	HEO	7:0	heo	0x00	R	HEO value. This is measured in 0-63 phase settings. To get HEO in UI, read HEO, convert hex to dec, then divide by 64.
0x28	VEO	7:0	veo	0x00	R	VEO value. This is measured in 0-63 vertical steps. To get VEO in mV, convert hex to dec, then multiply by the EOM Voltage Range defined in Reg 0x29[6:5].
0x29	Auto EOM Voltage Range	7	Reserved	0x00	RW	Reserved
		6:5	eom_vrange_setting		R	Readback of automatic EOM Voltage Range granularity. 00 = 3.125 mV 01 = 6.25 mV 10 = 9.375 mV 11 = 12.5 mV
		4:0	Reserved		RW	Reserved
0x2A	EOM_timer_thr	7:0	eom_timer_thr	0x30	RW	EOM timer for how long to check each phase/voltage setting.
0x2B	Reserved	7:0	Reserved	0x00	RW	Reserved
0x2C	VEO Scale	7	Reserved	0x72	RW	Reserved
		6	veo_scale		RW	0 = VEO scaling based on manual Voltage Range settings (see Reg 0x11[7:6]) 1 = Enable Auto VEO scaling
		5:0	Reserved		RW	Reserved
0x2D	CTLE Boost Override	7:4	Reserved	0x00	RW	Reserved
		3	reg_eq_bst_ov		RW	IN1 EQ Boost Override Control 0 = Disable IN1 EQ boost override 1 = Override the internal IN1 EQ boost settings with values in Reg 0x03[7:0]
		2:0	Reserved		RW	Reserved
0x2E	Reserved	7:0	Reserved	0x24	RW	Reserved
0x2F	Rate Overrides	7:6	refn_rate	0x06	RW	Reference Rate Selection for CDR Lock if Reg 0x3F[2] = 1 00 = Select SMPTE rates 01 = Select 10G Ethernet rate Other settings are Invalid
		5:0	Reserved		R	Reserved
0x30	Reserved	7:0	Reserved	0x00	RW	Reserved
0x31	IN1 Adaptation Mode and Input Mux Select	7	Reserved	0x00	RW	Reserved
		6:5	adapt_mode		RW	Adapt Mode Override Value if Reg 0x3F[5] = 1 00 = Manual CTLE for IN1. Set CTLE/CDR Page Reg 0x2D[3] = 1 to enable IN1 EQ boost settings with values in Reg 0x03[7:0]. 01 = Automatic CTLE Adaptation for IN1.
		4:2	Reserved		RW	Reserved
		1:0	input_mux_ch_sel		RW	Input Mux Selection if Reg 0x3F[4] = 1 to override IN_OUT_SEL pin 10 = IN1 to OUT1 only 11 = IN1 to OUT0 and OUT1 Other settings are Invalid
0x32	HEO/VEO Interrupt Threshold	7:4	heo_int_thresh	0x11	RW	Compares HEO value, Reg 0x27[7:0] vs. threshold from Reg 0x32[7:4] x 4.
		3:0	veo_int_thresh		RW	Compares VEO value. Reg 0x28[7:0] vs. threshold from Reg 0x32[3:0] x 4.
0x33	Reserved	7:0	Reserved	0x88	RW	Reserved
0x34	Reserved	7:0	Reserved	0x3F	RW	Reserved
0x35	Reserved	7:0	Reserved	0x1F	RW	Reserved
0x36	Reserved	7:0	Reserved	0x11	RW	Reserved
0x37	Reserved	7:0	Reserved	0x00	R	Reserved
0x38	Reserved	7:0	Reserved	0x00	R	Reserved

Address	Register Name	Bit	Field	Default	Type	Description
0x39	Reserved	7:0	Reserved	0x00	R	Reserved
0x3A	Low Data Rate IN1 EQ Boost	7:6	fixed_eq_BST0	0x00	RW	Fixed IN1 CTLE setting for 270M and 1.5G SMPTE rates. If Reg 0x3F[0] = 0, Reg 0x3A fixed IN1 CTLE setting is also used for 3G rate. [7:6]: 2-bit control for Stage 0 of the CTLE [5:4]: 2-bit control for Stage 1 of the CTLE. [3:2]: 2-bit control for Stage 2 of the CTLE. [1:0]: 2-bit control for Stage 3 of the CTLE.
		5:4	fixed_eq_BST1		RW	
		3:2	fixed_eq_BST2		RW	
		1:0	fixed_eq_BST3		RW	
0x3B	Reserved	7:0	Reserved	0x96	R	Reserved
0x3C	Reserved	7:0	Reserved	0x90	R	Reserved
0x3D	Reserved	7:0	Reserved	0x00	RW	Reserved
0x3E	HEO_VEO Lock Monitor Enable	7	heo_veo_lockmon_en	0x80	RW	Enable HEO/VEO lock monitoring. Once the lock and adaptation processes are complete, HEO/VEO monitoring is performed once per the interval determined by Reg 0x69[3:0].
		6:0	Reserved		RW	Reserved
0x3F	Pin Override Register Control	7:6	Reserved	0x01	RW	Reserved
		5	mr_adapt_mode_ov		RW	0 = Normal Behavior (Automatic Adaptation when IN1 is selected) 1 = Override Automatic Adaptation for IN1. Adaptation behavior is controlled by Reg 0x31[6:5].
		4	mr_in_out_sel_ov		RW	0 = Input channel selection determined by IN_OUT_SEL pin 1 = Override input channel selection pin settings. Input selection is controlled by Reg 0x31[1:0].
		3	mr_out_ctrl_ov		RW	0 = Output mux settings determined by OUT_CTRL pin 1 = Override output mux pin settings. Output mux is controlled by Reg 0x1C[3:2].
		2	mr_refn_rate_ov		RW	0 = SMPTE or 10 GbE reference rates determined by IN_OUT_SEL pin 1 = Override reference rate pin settings. Reference rates for CDR lock are controlled by Reg 0x2F[7:6].
		1	mr_eqbst_pin_ov		RW	0 = IN1 EQ boost Bypass is controlled by OUT_CTRL pin behavior 1 = Override IN1 EQ boost pin control. IN1 EQ boost bypass characteristics are controlled by settings in Reg 0x2D[3] and Reg 0x03[7:0].
		0	mr_en_3G_divsel_eq		RW	0 = Disables IN1 EQ Adaptation for 3G data rate 1 = Enables IN1 EQ Adaptation for 3G data rate
0x40	IN1 Index 0 Boost for Adaptation	7:6	EQ_index_0_BST0	0x00	RW	Index 0 Boost [7:6]: 2-bit control for Stage 0 of the CTLE [5:4]: 2-bit control for Stage 1 of the CTLE. [3:2]: 2-bit control for Stage 2 of the CTLE. [1:0]: 2-bit control for Stage 3 of the CTLE.
		5:4	EQ_index_0_BST1		RW	
		3:2	EQ_index_0_BST2		RW	
		1:0	EQ_index_0_BST3		RW	
0x41	IN1 Index 1 Boost for Adaptation	7:6	EQ_index_1_BST0	0x40	RW	Index 1 Boost [7:6]: 2-bit control for Stage 0 of the CTLE [5:4]: 2-bit control for Stage 1 of the CTLE. [3:2]: 2-bit control for Stage 2 of the CTLE. [1:0]: 2-bit control for Stage 3 of the CTLE.
		5:4	EQ_index_1_BST1		RW	
		3:2	EQ_index_1_BST2		RW	
		1:0	EQ_index_1_BST3		RW	
0x42	IN1 Index 2 Boost for Adaptation	7:6	EQ_index_2_BST0	0x80	RW	Index 2 Boost [7:6]: 2-bit control for Stage 0 of the CTLE [5:4]: 2-bit control for Stage 1 of the CTLE. [3:2]: 2-bit control for Stage 2 of the CTLE. [1:0]: 2-bit control for Stage 3 of the CTLE.
		5:4	EQ_index_2_BST1		RW	
		3:2	EQ_index_2_BST2		RW	
		1:0	EQ_index_2_BST3		RW	
0x43	IN1 Index 3 Boost for Adaptation	7:6	EQ_index_3_BST0	0x50	RW	Index 3 Boost [7:6]: 2-bit control for Stage 0 of the CTLE [5:4]: 2-bit control for Stage 1 of the CTLE. [3:2]: 2-bit control for Stage 2 of the CTLE. [1:0]: 2-bit control for Stage 3 of the CTLE.
		5:4	EQ_index_3_BST1		RW	
		3:2	EQ_index_3_BST2		RW	
		1:0	EQ_index_3_BST3		RW	

Address	Register Name	Bit	Field	Default	Type	Description
0x44	IN1 Index 4 Boost for Adaptation	7:6	EQ_index_4_BST0	0xC0	RW	Index 4 Boost [7:6]: 2-bit control for Stage 0 of the CTLE [5:4]: 2-bit control for Stage 1 of the CTLE. [3:2]: 2-bit control for Stage 2 of the CTLE. [1:0]: 2-bit control for Stage 3 of the CTLE.
		5:4	EQ_index_4_BST1		RW	
		3:2	EQ_index_4_BST2		RW	
		1:0	EQ_index_4_BST3		RW	
0x45	IN1 Index 5 Boost for Adaptation	7:6	EQ_index_5_BST0	0x90	RW	Index 5 Boost [7:6]: 2-bit control for Stage 0 of the CTLE [5:4]: 2-bit control for Stage 1 of the CTLE. [3:2]: 2-bit control for Stage 2 of the CTLE. [1:0]: 2-bit control for Stage 3 of the CTLE.
		5:4	EQ_index_5_BST1		RW	
		3:2	EQ_index_5_BST2		RW	
		1:0	EQ_index_5_BST3		RW	
0x46	IN1 Index 6 Boost for Adaptation	7:6	EQ_index_6_BST0	0x54	RW	Index 6 Boost [7:6]: 2-bit control for Stage 0 of the CTLE [5:4]: 2-bit control for Stage 1 of the CTLE. [3:2]: 2-bit control for Stage 2 of the CTLE. [1:0]: 2-bit control for Stage 3 of the CTLE.
		5:4	EQ_index_6_BST1		RW	
		3:2	EQ_index_6_BST2		RW	
		1:0	EQ_index_6_BST3		RW	
0x47	IN1 Index 7 Boost for Adaptation	7:6	EQ_index_7_BST0	0xA0	RW	Index 7 Boost [7:6]: 2-bit control for Stage 0 of the CTLE [5:4]: 2-bit control for Stage 1 of the CTLE. [3:2]: 2-bit control for Stage 2 of the CTLE. [1:0]: 2-bit control for Stage 3 of the CTLE.
		5:4	EQ_index_7_BST1		RW	
		3:2	EQ_index_7_BST2		RW	
		1:0	EQ_index_7_BST3		RW	
0x48	IN1 Index 8 Boost for Adaptation	7:6	EQ_index_8_BST0	0xB0	RW	Index 8 Boost [7:6]: 2-bit control for Stage 0 of the CTLE [5:4]: 2-bit control for Stage 1 of the CTLE. [3:2]: 2-bit control for Stage 2 of the CTLE. [1:0]: 2-bit control for Stage 3 of the CTLE.
		5:4	EQ_index_8_BST1		RW	
		3:2	EQ_index_8_BST2		RW	
		1:0	EQ_index_8_BST3		RW	
0x49	IN1 Index 9 Boost for Adaptation	7:6	EQ_index_9_BST0	0x95	RW	Index 9 Boost [7:6]: 2-bit control for Stage 0 of the CTLE [5:4]: 2-bit control for Stage 1 of the CTLE. [3:2]: 2-bit control for Stage 2 of the CTLE. [1:0]: 2-bit control for Stage 3 of the CTLE.
		5:4	EQ_index_9_BST1		RW	
		3:2	EQ_index_9_BST2		RW	
		1:0	EQ_index_9_BST3		RW	
0x4A	IN1 Index 10 Boost for Adaptation	7:6	EQ_index_10_BST0	0x69	RW	Index 10 Boost [7:6]: 2-bit control for Stage 0 of the CTLE [5:4]: 2-bit control for Stage 1 of the CTLE. [3:2]: 2-bit control for Stage 2 of the CTLE. [1:0]: 2-bit control for Stage 3 of the CTLE.
		5:4	EQ_index_10_BST1		RW	
		3:2	EQ_index_10_BST2		RW	
		1:0	EQ_index_10_BST3		RW	
0x4B	IN1 Index 11 Boost for Adaptation	7:6	EQ_index_11_BST0	0xD5	RW	Index 11 Boost [7:6]: 2-bit control for Stage 0 of the CTLE [5:4]: 2-bit control for Stage 1 of the CTLE. [3:2]: 2-bit control for Stage 2 of the CTLE. [1:0]: 2-bit control for Stage 3 of the CTLE.
		5:4	EQ_index_11_BST1		RW	
		3:2	EQ_index_11_BST2		RW	
		1:0	EQ_index_11_BST3		RW	
0x4C	IN1 Index 12 Boost for Adaptation	7:6	EQ_index_12_BST0	0x99	RW	Index 12 Boost [7:6]: 2-bit control for Stage 0 of the CTLE [5:4]: 2-bit control for Stage 1 of the CTLE. [3:2]: 2-bit control for Stage 2 of the CTLE. [1:0]: 2-bit control for Stage 3 of the CTLE.
		5:4	EQ_index_12_BST1		RW	
		3:2	EQ_index_12_BST2		RW	
		1:0	EQ_index_12_BST3		RW	
0x4D	IN1 Index 13 Boost for Adaptation	7:6	EQ_index_13_BST0	0xA5	RW	Index 13 Boost [7:6]: 2-bit control for Stage 0 of the CTLE [5:4]: 2-bit control for Stage 1 of the CTLE. [3:2]: 2-bit control for Stage 2 of the CTLE. [1:0]: 2-bit control for Stage 3 of the CTLE.
		5:4	EQ_index_13_BST1		RW	
		3:2	EQ_index_13_BST2		RW	
		1:0	EQ_index_13_BST3		RW	
0x4E	IN1 Index 14 Boost for Adaptation	7:6	EQ_index_14_BST0	0xE6	RW	Index 14 Boost [7:6]: 2-bit control for Stage 0 of the CTLE [5:4]: 2-bit control for Stage 1 of the CTLE. [3:2]: 2-bit control for Stage 2 of the CTLE. [1:0]: 2-bit control for Stage 3 of the CTLE.
		5:4	EQ_index_14_BST1		RW	
		3:2	EQ_index_14_BST2		RW	
		1:0	EQ_index_14_BST3		RW	
0x4F	IN1 Index 15 Boost for Adaptation	7:6	EQ_index_15_BST0	0xF9	RW	Index 15 Boost [7:6]: 2-bit control for Stage 0 of the CTLE [5:4]: 2-bit control for Stage 1 of the CTLE. [3:2]: 2-bit control for Stage 2 of the CTLE. [1:0]: 2-bit control for Stage 3 of the CTLE.
		5:4	EQ_index_15_BST1		RW	
		3:2	EQ_index_15_BST2		RW	
		1:0	EQ_index_15_BST3		RW	
0x50	Reserved	7:0	Reserved	0x00	RW	Reserved

Address	Register Name	Bit	Field	Default	Type	Description
0x51	Reserved	7:0	Reserved	0x00	RW	Reserved
0x52	IN1 Active EQ Readback	7:0	eq_bst_to_ana	0x00	R	IN1 CTLE boost setting readback from Active CTLE Adaptation.
0x53	Reserved	7:0	Reserved	0x00	R	Reserved
0x54	Interrupt Status Register	7	cardet	0x00	R	0 = Carrier Detect from the selected input de-asserted 1 = Carrier Detect from the selected input asserted Note: Clears when Reg 0x54 is read-back.
		6	cdr_lock_int		R	0 = No interrupt from CDR Lock 1 = CDR Lock Interrupt Note: Clears when Reg 0x54 is read-back.
		5	carrier_det1_int		R	0 = No interrupt from IN1 Carrier Detect 1 = IN1 Carrier Detect Interrupt Note: Clears when Reg 0x54 is read-back.
		4	Reserved		R	Reserved
		3	heo_veo_int		R	0 = No interrupt from HEO/VEO 1 = HEO/VEO Threshold Reached Interrupt Note: Clears when Reg 0x54 is read-back.
		2	cdr_lock_loss_int		R	0 = No interrupt from CDR Lock 1 = CDR Loss of Lock Interrupt Note: Clears when Reg 0x54 is read-back.
		1	carrier_det1_loss_int		R	0 = No interrupt from IN1 Carrier Detect 1 = IN1 Carrier Detect Loss Interrupt Note: Clears when Reg 0x54 is read-back.
		0	Reserved		R	Reserved
0x55	Reserved	7:0	Reserved	0x02	R	Reserved
0x56	Interrupt Control Register	7	Reserved	0x00	RW	Reserved
		6	cdr_lock_int_en		RW	0 = Disable interrupt if CDR lock is achieved 1 = Enable interrupt if CDR lock is achieved
		5	carrier_det1_int_en		RW	0 = Disable interrupt if IN1 Carrier Detect is asserted 1 = Enable interrupt if IN1 Carrier Detect is asserted
		4	Reserved		RW	Reserved
		3	heo_veo_int_en		RW	0 = Disable interrupt if HEO/VEO threshold is reached 1 = Enable interrupt if HEO/VEO threshold is reached
		2	cdr_lock_loss_int_en		RW	0 = Disable interrupt if CDR loses lock 1 = Enable interrupt if CDR loses lock
		1	carrier_det1_loss_int_en		RW	0 = Disable interrupt if there is loss of signal (LOS) on IN1 1 = Enable interrupt if there is loss of signal (LOS) on IN1
		0	Reserved		RW	Reserved
0x60	Reserved	7:0	Reserved	0x26	RW	Reserved
0x61	Reserved	7:0	Reserved	0x31	RW	Reserved
0x62	Reserved	7:0	Reserved	0x70	RW	Reserved
0x63	Reserved	7:0	Reserved	0x3D	RW	Reserved
0x64	Reserved	7:0	Reserved	0xFF	RW	Reserved
0x65	Reserved	7:0	Reserved	0x00	RW	Reserved
0x66	Reserved	7:0	Reserved	0x00	RW	Reserved
0x67	Reserved	7:0	Reserved	0x00	RW	Reserved
0x68	Reserved	7:0	Reserved	0x00	RW	Reserved
0x69	HEO_VEO Lock Monitor	7:4	Reserved	0x0A	RW	Reserved
		3:0	hv_lckmon_cnt_ms		RW	While monitoring lock, these bits set the amount of interval times to monitor HEO or VEO lock. Each interval is 6.5 ms. Therefore, by default, Reg 0x69[3:0] = 1010'b causes HEO_VEO lock monitor to occur once every 65 ms.
0x6A	HEO and VEO Lock Threshold	7:4	veo_lck_thrsh	0x44	RW	HEO/VEO lock thresholds. Lock will not be declared until HEO ≥ (heo_lck_thrsh x 4) and VEO ≥ (veo_lck_thrsh x 4).
		3:0	heo_lck_thrsh		RW	
0x6B	Reserved	7:0	Reserved	0x40	RW	Reserved

Address	Register Name	Bit	Field	Default	Type	Description
0x6C	Reserved	7:0	Reserved	0x00	RW	Reserved
0x6D	Reserved	7:0	Reserved	0x00	RW	Reserved
0x6E	Reserved	7:0	Reserved	0x00	RW	Reserved
0x6F	Reserved	7:0	Reserved	0x00	RW	Reserved
0x70	Reserved	7:0	Reserved	0x03	RW	Reserved
0x71	Reserved	7:0	Reserved	0x20	R	Reserved
0x72	Reserved	7:0	Reserved	0x00	RW	Reserved
0x73	Reserved	7:0	Reserved	0x00	RW	Reserved
0x74	Reserved	7:0	Reserved	0x00	RW	Reserved
0x75	Reserved	7:0	Reserved	0x00	RW	Reserved
0x77	Reserved	7:0	Reserved	0x00	RW	Reserved
0x80	Reserved	7:0	Reserved	0x50	RW	Reserved
0x81	Reserved	7:0	Reserved	0x00	RW	Reserved
0x82	Reserved	7:0	Reserved	0x80	RW	Reserved
0x83	Reserved	7:0	Reserved	0x70	RW	Reserved
0x84	Reserved	7:0	Reserved	0x04	RW	Reserved
0x85	Reserved	7:0	Reserved	0x00	RW	Reserved
0x87	Reserved	7:0	Reserved	0x00	RW	Reserved
0x90	Reserved	7:0	Reserved	0xA5	RW	Reserved
0x91	Reserved	7:0	Reserved	0x23	RW	Reserved
0x92	Reserved	7:0	Reserved	0x2C	RW	Reserved
0x93	Reserved	7:0	Reserved	0x32	RW	Reserved
0x94	Reserved	7:0	Reserved	0x37	RW	Reserved
0x95	Reserved	7:0	Reserved	0x3E	RW	Reserved
0x98	Reserved	7:0	Reserved	0x3F	RW	Reserved
0x99	Reserved	7:0	Reserved	0x04	RW	Reserved
0x9A	Reserved	7:0	Reserved	0x04	RW	Reserved
0x9B	Reserved	7:0	Reserved	0x04	RW	Reserved
0x9C	Reserved	7:0	Reserved	0x06	RW	Reserved
0x9D	Reserved	7:0	Reserved	0x04	RW	Reserved
0x9E	Reserved	7:0	Reserved	0x04	RW	Reserved
0xA0	SMPTE Data Rate Lock Enable	7:5	Reserved	0x1F	RW	Reserved
		4	dvb_enable		RW	0 = Disable CDR Lock to 270 Mbps 1 = Enable CDR Lock to 270 Mbps
		3	hd_enable		RW	0 = Disable CDR Lock to 1.485/1.4835 Gbps 1 = Enable CDR Lock to 1.485/1.4835 Gbps
		2	3G_enable		RW	0 = Disable CDR Lock to 2.97/2.967 Gbps 1 = Enable CDR Lock to 2.97/2.967 Gbps
		1	6G_enable		RW	0 = Disable CDR Lock to 5.94/5.934 Gbps 1 = Enable CDR Lock to 5.94/5.934 Gbps
		0	12G_enable		RW	0 = Disable CDR Lock to 11.88/11.868 Gbps 1 = Enable CDR Lock to 11.88/11.868 Gbps

7.5.3 Drivers Register Page

Address	Register Name	Bit	Field	Default	Type	Description
0x00	Reserved	7:0	Reserved	0x08	RW	Reserved
0x01	Reserved	7:0	Reserved	0x80	RW	Reserved
0x02	Reserved	7:0	Reserved	0x07	RW	Reserved
0x03	Reserved	7:0	Reserved	0x3F	RW	Reserved
0x04	Reserved	7:0	Reserved	0x00	RW	Reserved
0x05	Reserved	7:0	Reserved	0x00	RW	Reserved
0x06	Reserved	7:0	Reserved	0xA0	RW	Reserved
0x07	Reserved	7:0	Reserved	0x24	RW	Reserved
0x08	Reserved	7:0	Reserved	0x27	RW	Reserved
0x09	Reserved	7:0	Reserved	0x01	RW	Reserved
0x0A	Reserved	7:0	Reserved	0x05	RW	Reserved
0x0B	Reserved	7:0	Reserved	0x37	RW	Reserved
0x0C	Reserved	7:0	Reserved	0x01	RW	Reserved
0x0D	Reserved	7:0	Reserved	0x25	RW	Reserved
0x0E	Reserved	7:0	Reserved	0x37	RW	Reserved
0x0F	Reserved	7:0	Reserved	0x02	RW	Reserved
0x10	Reserved	7:0	Reserved	0x0A	RW	Reserved
0x11	Reserved	7:0	Reserved	0x02	RW	Reserved
0x12	Reserved	7:0	Reserved	0x08	RW	Reserved
0x13	Reserved	7:0	Reserved	0x04	RW	Reserved
0x14	Reserved	7:0	Reserved	0x3C	RW	Reserved
0x15	Reserved	7:0	Reserved	0x00	RW	Reserved
0x16	Reserved	7:0	Reserved	0x00	RW	Reserved
0x17	Reserved	7:0	Reserved	0x08	RW	Reserved
0x18	Reserved	7:0	Reserved	0x01	RW	Reserved
0x19	Reserved	7:0	Reserved	0x08	RW	Reserved
0x1A	Reserved	7:0	Reserved	0x01	RW	Reserved
0x1B	Reserved	7:0	Reserved	0xA7	RW	Reserved
0x1C	Reserved	7:0	Reserved	0x00	RW	Reserved
0x1D	Reserved	7:0	Reserved	0x00	RW	Reserved
0x1E	Reserved	7:0	Reserved	0x00	RW	Reserved
0x1F	Reserved	7:0	Reserved	0x00	RW	Reserved
0x20	Reserved	7:0	Reserved	0x00	RW	Reserved
0x21	Reserved	7:0	Reserved	0xC0	RW	Reserved
0x22	Reserved	7:0	Reserved	0x00	RW	Reserved
0x23	Reserved	7:0	Reserved	0x00	RW	Reserved
0x24	Reserved	7:0	Reserved	0x00	RW	Reserved
0x25	Reserved	7:6	Reserved	0x00	R	Reserved
0x26	Reserved	7:0	Reserved	0x05	R	Reserved
0x27	Reserved	7:0	Reserved	0x00	RW	Reserved
0x28	Reserved	7:0	Reserved	0x00	RW	Reserved
0x29	Reserved	7:0	Reserved	0x20	R	Reserved
0x2A	Reserved	7:0	Reserved	0x40	RW	Reserved
0x2B	Reserved	7:0	Reserved	0x89	RW	Reserved
0x2C	Reserved	7:0	Reserved	0x0B	RW	Reserved
0x2D	Reserved	7:0	Reserved	0x20	RW	Reserved
0x2E	Reserved	7:0	Reserved	0x00	R	Reserved

Address	Register Name	Bit	Field	Default	Type	Description
0x2F	Reserved	7:0	Reserved	0x00	RW	Reserved
0x30	OUT0 Output Control	7	tx0_mute_ov	0x0A	RW	OUT0 Mute Override Control 0 = Disable OUT0 Mute Override Control 1 = Enable OUT0 Mute Override Control by value in Reg 0x30[6].
		6	tx0_mute_val		RW	0 = Normal Operation 1 = Mute OUT0 if Reg 0x30[7] = 1
		5	tx0_vod_ov		RW	OUT0 VOD Override Control 0 = VOD settings for OUT0 determined by VOD_DE pin 1 = Override VOD pin settings for OUT0. VOD settings for OUT0 are controlled by Reg 0x30[2:0]
		4:3	Reserved		RW	Reserved
		2:0	tx0_vod		RW	VOD settings with DE = 0 for OUT0 if Reg 0x30[5] = 1. See Figure 9.
0x31	OUT0 De-Emphasis Control	7	Reserved	0x01	RW	Reserved
		6	tx0_dem_ov		RW	OUT0 De-Emphasis Override Control 0 = De-emphasis for OUT0 determined by VOD_DE pin 1 = Override De-emphasis settings for OUT0. De-emphasis settings for OUT0 are controlled by Reg 0x31[2:0]
		5	tx0_PD_ov		RW	OUT0 Power Down Override Control 0 = Disable OUT0 Power Down Override Control 1 = Enable OUT0 Power Down Override Control by value in Reg 0x31[4].
		4	tx0_PD		RW	0 = Normal Operation 1 = Power Down OUT0 if Reg 0x31[5] = 1
		3	Reserved		RW	Reserved
		2:0	tx0_dem		RW	De-emphasis settings for OUT0 if Reg 0x31[6] = 1. See Figure 10.
0x32	OUT1 Output Control	7	tx1_mute_ov	0x0A	RW	OUT1 Mute Override Control 0 = Disable OUT1 Mute Override Control 1 = Enable OUT1 Mute Override Control by value in Reg 0x32[6].
		6	tx1_mute_val		RW	0 = Normal Operation 1 = Mute OUT1 if Reg 0x32[7] = 1
		5	tx1_vod_ov		RW	OUT1 VOD Override Control 0 = VOD settings for OUT1 determined by VOD_DE pin 1 = Override VOD pin settings for OUT1. VOD settings for OUT1 are controlled by Reg 0x32[2:0]
		4:3	Reserved		RW	Reserved
		2:0	tx1_vod		RW	VOD settings with DE = 0 for OUT1 if Reg 0x32[5] = 1. See Figure 9.
0x33	OUT1 De-Emphasis Control	7	Reserved	0x11	RW	Reserved
		6	tx1_dem_ov		RW	OUT1 De-Emphasis Override Control 0 = De-emphasis for OUT1 determined by VOD_DE pin 1 = Override De-emphasis settings for OUT1. De-emphasis settings for OUT1 are controlled by Reg 0x33[2:0]
		5	tx1_PD_ov		RW	OUT1 Power Down Override Control 0 = Disable OUT1 Power Down Override Control 1 = Enable OUT1 Power Down Override Control by value in Reg 0x33[4].
		4	tx1_PD		RW	0 = Normal Operation 1 = Power Down OUT1 if Reg 0x33[5] = 1
		3	Reserved		RW	Reserved
		2:0	tx1_dem		RW	De-emphasis settings for OUT1 if Reg 0x33[6] = 1. See Figure 10.
0x34	Reserved	7:0	Reserved	0x17	RW	Reserved
0x35	Reserved	7:0	Reserved	0x61	RW	Reserved
0x36	Reserved	7:0	Reserved	0x02	RW	Reserved
0x37	Reserved	7:0	Reserved	0x00	RW	Reserved

Address	Register Name	Bit	Field	Default	Type	Description
0x38	Reserved	7:0	Reserved	0x00	RW	Reserved
0x39	Reserved	7:0	Reserved	0x00	RW	Reserved
0x3A	Reserved	7:0	Reserved	0x00	RW	Reserved
0x3B	Reserved	7:0	Reserved	0x00	RW	Reserved
0x3C	Reserved	7:0	Reserved	0x00	RW	Reserved
0x3D	Reserved	7:0	Reserved	0x7F	RW	Reserved
0x3E	Reserved	7:0	Reserved	0x00	RW	Reserved
0x3F	Reserved	7:0	Reserved	0x00	RW	Reserved
0x40	Reserved	7:0	Reserved	0x00	R	Reserved
0x41	Reserved	7:0	Reserved	0x00	R	Reserved
0x42	Reserved	7:0	Reserved	0x00	R	Reserved
0x43	Reserved	7:0	Reserved	0x00	R	Reserved
0x44	Reserved	7:0	Reserved	0x00	R	Reserved
0x45	Reserved	7:0	Reserved	0x00	R	Reserved
0x46	Reserved	7:0	Reserved	0x00	R	Reserved
0x47	Reserved	7:0	Reserved	0x00	R	Reserved
0x48	Reserved	7:0	Reserved	0x00	R	Reserved
0x49	Reserved	7:0	Reserved	0x01	R	Reserved
0x4A	Reserved	7:0	Reserved	0x00	R	Reserved
0x4B	Reserved	7:0	Reserved	0x00	R	Reserved
0x4C	Reserved	7:0	Reserved	0x00	R	Reserved
0x4D	Reserved	7:0	Reserved	0x00	RW	Reserved
0x4E	Reserved	7:0	Reserved	0x00	RW	Reserved
0x4F	Reserved	7:0	Reserved	0x00	RW	Reserved
0x50	Reserved	7:0	Reserved	0x00	RW	Reserved
0x51	Reserved	7:0	Reserved	0x00	RW	Reserved
0x52	Reserved	7:0	Reserved	0x00	RW	Reserved
0x53	Reserved	7:0	Reserved	0x00	RW	Reserved
0x54	Reserved	7:0	Reserved	0x0F	R	Reserved

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 General Guidance for SMPTE and 10 GbE Applications

SMPTE specifications define the use of AC coupling capacitors for transporting uncompressed serial data streams with heavy low frequency content. The use of 4.7-µF AC coupling capacitors is recommended to avoid low frequency DC wander. SFF-8431 (SFP+) requires the 100-Ω signal to meet the electrical, return loss, jitter, and eye mask specifications. It is recommended to place the LMH1226 as close as possible to the 100-Ω SFP+ optical module in order to meet the specifications for SFF-8431. Refer to 表 9 for design guidelines.

8.1.2 LMH1219 and LMH1226 Compatibility

The LMH1226 is pin compatible with LMH1219 (12G UHD cable equalizer with integrated reclocker). Both LMH1219 and LMH1226 devices support Single Supply Mode and Dual Supply Mode as shown in 図 27 and 図 28, respectively.

8.2 Typical Application

The LMH1226 is a multi-rate reclocker that supports SDI data rates up to 11.88 Gbps and 10 GbE. 図 21 shows a typical implementation of the LMH1226 as a SDI reclocker. Signal from a FPGA or optical module is connected to the input port at IN1±. Equalized and reclocked data is output at OUT0± and OUT1± to a downstream video processor.

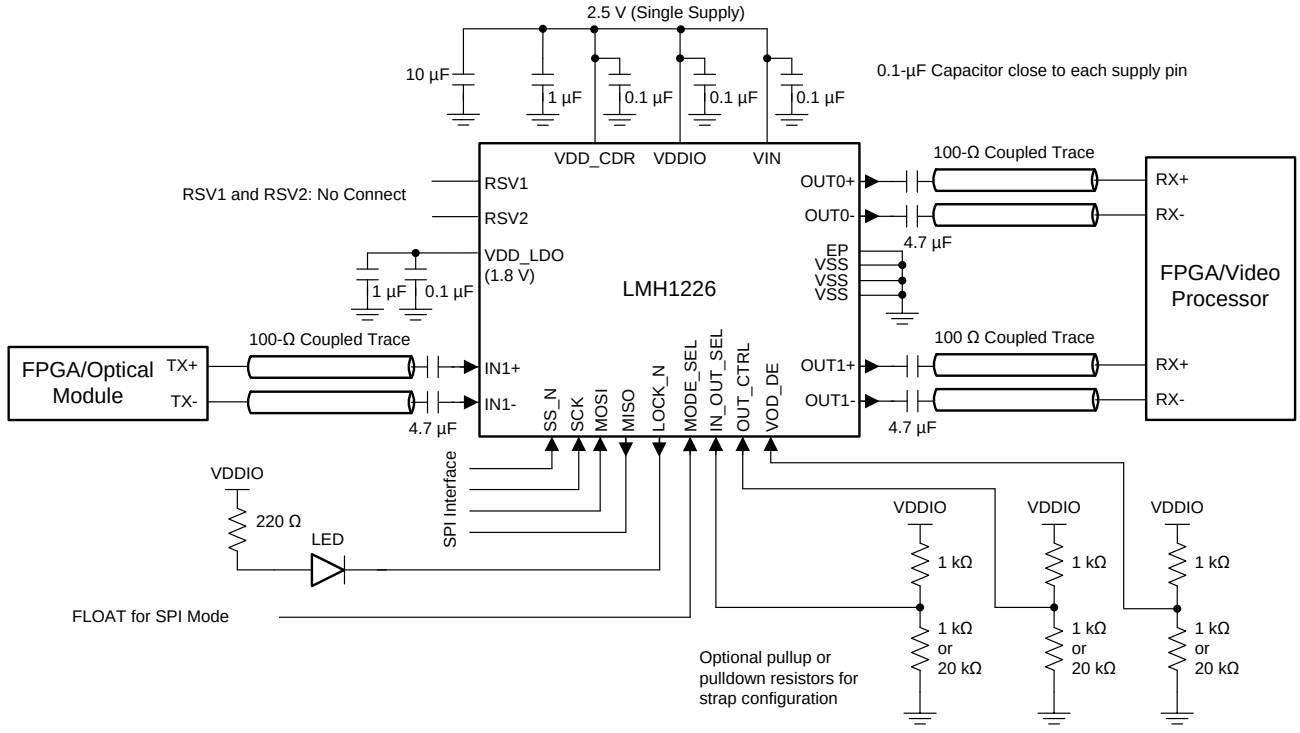


図 21. LMH1226 SPI Mode Connection Diagram

Typical Application (continued)

8.2.1 Design Requirements

表 9. LMH1226 Design Requirements

DESIGN PARAMETER	REQUIREMENTS
IN1± Input AC coupling capacitors	AC Coupling capacitors at IN1± should be 4.7-µF capacitors. Choose small 0402 surface mount ceramic capacitors. This allows both SMPTE and 10 GbE data traffic.
Output AC coupling Capacitors	Both OUT0± and OUT1± require AC coupling capacitors. Choose small 0402 surface mount ceramic capacitors. 4.7-µF AC coupling capacitors are recommended.
DC power supply decoupling capacitors	Decoupling capacitors are required to minimize power supply noise. Place 10-µF and 1-µF bulk capacitors close to each device. Place a 0.1-µF capacitor close to each supply pin.
VDD_LDO decoupling capacitors	Place 1-µF and 0.1-µF surface mount ceramic capacitors as close as possible to the device VDD_LDO pin.
High Speed IN1, OUT0, and OUT1 trace impedance	IN1±, OUT0± and OUT1± should be routed with coupled board traces with 100-Ω differential impedance.
SFP+ (SFF-8431) return loss	Place SFP module within 1-2 inches of the LMH1226 to minimize insertion and return loss.
Use of SPI or SMBus interface	Set MODE_SEL to Level-F (pin unconnected) for SPI. Set MODE_SEL to Level-L (connect 1 kΩ to VSS) for SMBus. SMBus is 3.3 V tolerant.

8.2.2 Detailed Design Procedure

The following general design procedure is recommended:

1. Select a suitable power supply voltage for the LMH1226. See Power Supply Recommendations for details.
2. Check that the power supply meets the DC and AC requirements in *Recommended Operating Conditions*.
3. Select the proper pull-high or pull-low resistors for IN_OUT_SEL and OUT_CTRL for setting the signal path.
4. Depending on the length and insertion loss of the output traces for OUT0± and OUT1±, select the proper pull-high or pull-low resistors for VOD_DE to set the output amplitude and de-emphasis settings. Refer to Table 5 for details.
5. Follow all design requirements detailed in 表 9 to optimize LMH1226 performance.
6. For additional layout recommendations, refer to PCB Layout Guidelines.

8.2.3 Recommended VOD and DEM Register Settings

表 10 shows recommended output amplitude and de-emphasis register settings for most applications.

表 10. VOD and DEM Register Settings

VOD REG SETTING OUT0±: 0x30[5]=1, 0x30[2:0] OUT1±: 0x32[5]=1, 0x32[2:0]	DEM REG SETTING OUT0±: 0x31[6]=1, 0x31[2:0] OUT1±: 0x33[6]=1, 0x33[2:0]	VOD (mVpp)	DEM (dB)
0	0	410	0
1	1	486	-0.1
2	1	560	-0.1
2	2	560	-0.9
3	1	635	-0.3
3	2	635	-1.3
3	3	635	-2.4
4	1	716	-0.5
4	2	716	-1.8
4	3	716	-3.0
4	4	716	-4.0
5	1	810	-0.8
5	2	810	-2.4
5	3	810	-3.6
5	4	810	-4.6

表 10. VOD and DEM Register Settings (continued)

VOD REG SETTING OUT0±: 0x30[5]=1, 0x30[2:0] OUT1±: 0x32[5]=1, 0x32[2:0]	DEM REG SETTING OUT0±: 0x31[6]=1, 0x31[2:0] OUT1±: 0x33[6]=1, 0x33[2:0]	VOD (mVpp)	DEM (dB)
5	5	810	-6.1
6	1	880	-1.0
6	2	880	-2.7
6	3	880	-4.0
6	4	880	-5.0
6	5	880	-6.5
7	1	973	-1.2
7	2	973	-3.1
7	3	973	-4.6
7	4	973	-5.7
7	5	973	-7.1

8.2.4 Application Performance Plots

The LMH1226 performance was measured with the test setup shown in 図 22.

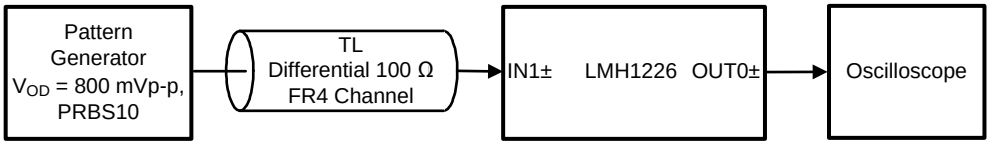
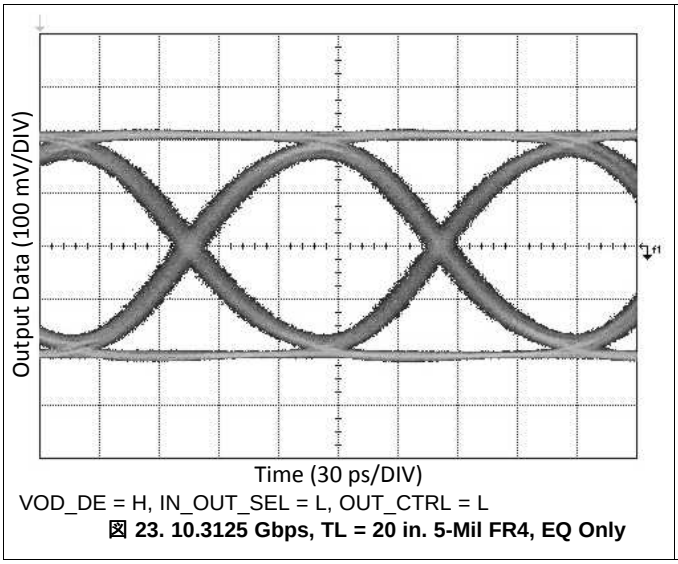


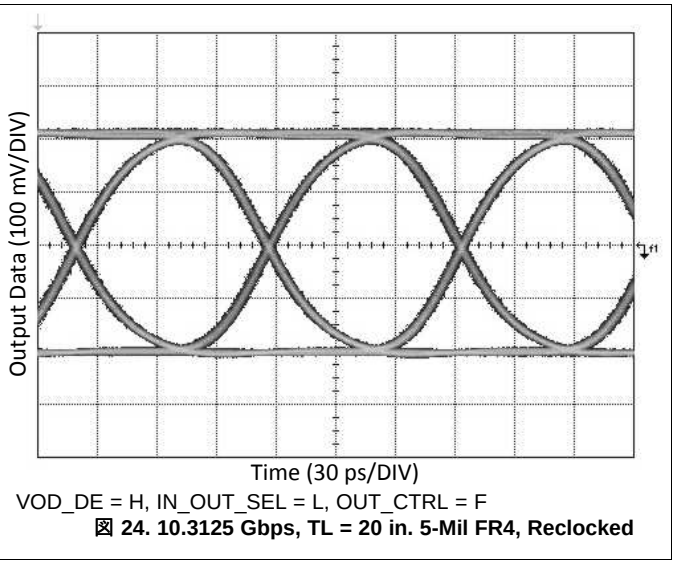
図 22. Test Setup for LMH1226 PCB Equalizer (IN1±)

The eye diagrams in this subsection show how the LMH1226 improves overall signal integrity in the data path for 100-Ω differential FR4 PCB trace at IN1.



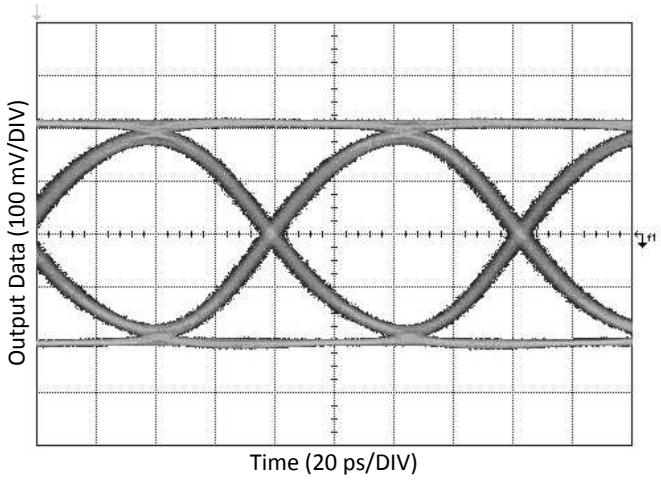
VOD_DE = H, IN_OUT_SEL = L, OUT_CTRL = L

図 23. 10.3125 Gbps, TL = 20 in. 5-Mil FR4, EQ Only



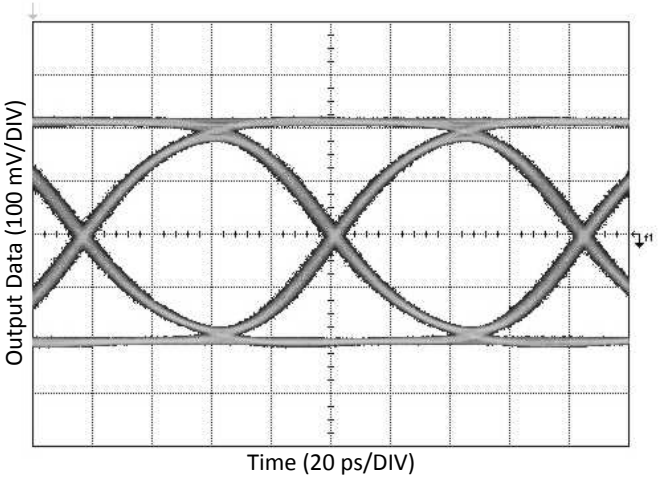
VOD_DE = H, IN_OUT_SEL = L, OUT_CTRL = F

図 24. 10.3125 Gbps, TL = 20 in. 5-Mil FR4, Reclocked



VOD_DE = H, IN_OUT_SEL = H, OUT_CTRL = L

図 25. 11.88 Gbps, TL = 20 in. 5-Mil FR4, EQ Only



VOD_DE = H, IN_OUT_SEL = H, OUT_CTRL = F

図 26. 11.88 Gbps, TL = 20 in. 5-Mil FR4, Reclocked

9 Power Supply Recommendations

The LMH1226 is designed to provide flexibility in supply rails. There are two ways to power the LMH1226:

- **Single Supply Mode (2.5 V):** This mode offers ease of use, with the internal circuitry receiving power from the on-chip 1.8 V regulator. In this mode, 2.5 V is applied to VDD_CDR, VIN, and VDDIO. See 図 27 for more details.
- **Dual Supply Mode (2.5 V and 1.8 V):** This mode provides lower power consumption. In this mode, 1.8 V is connected to both VIN and VDD_LDO. VDD_CDR, and VDDIO are powered from a 2.5 V supply. See 図 28 for more details.
- When Dual Supply Mode is used, the 2.5 V supply for VDD_CDR and VDDIO should be powered *before or at the same time as* the 1.8 V supply that powers VIN and VDD_LDO.

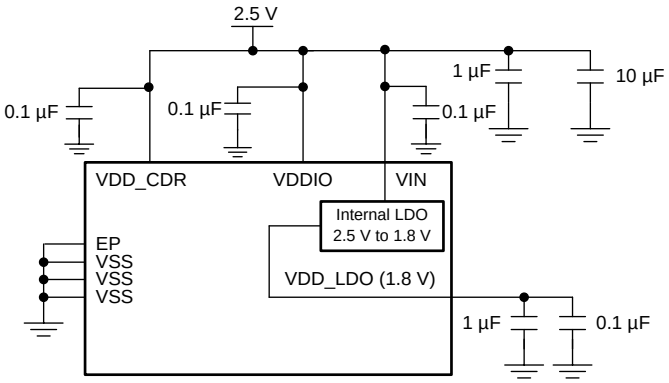


図 27. Typical Connection for Single 2.5 V Supply

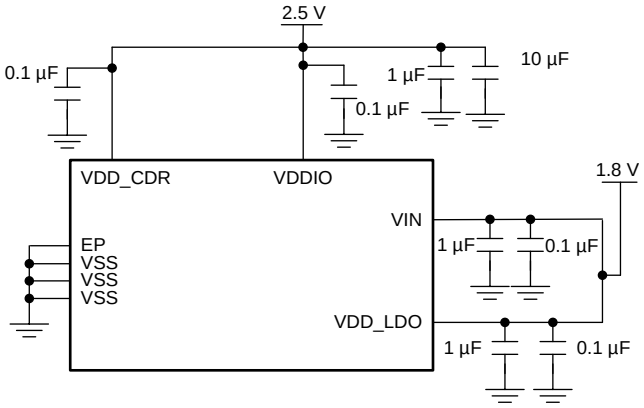


図 28. Typical Connection for Dual 2.5 V and 1.8 V Supply

For power supply de-coupling, 0.1-µF surface-mount ceramic capacitors are recommended to be placed close to each VDD_CDR, VIN, VDD_LDO, and VDDIO supply pin to VSS. Larger bulk capacitors (for example, 10 µF and 1 µF) are recommended for VDD_CDR and VIN. Good supply bypassing requires low inductance capacitors. This can be achieved through an array of multiple small body size surface-mount bypass capacitors in order to keep low supply impedance. Better results can be achieved through the use of a buried capacitor formed by a VDD and VSS plane separated by 2-4 mil dielectric in a printed circuit board.

10 Layout

10.1 PCB Layout Guidelines

The following guidelines are recommended for designing the board layout for the LMH1226:

1. Choose a suitable board stack-up that supports 100-Ω differential trace routing on the board's top layer. This is typically done with a Layer 2 ground plane reference for the 100-Ω differential traces.

PCB Layout Guidelines (continued)

2. Place anti-pad (ground relief) on the power and ground planes directly under the 4.7-µF AC coupling capacitor and IC landing pads to minimize parasitic capacitance. The size of the anti-pad depends on the board stack-up and can be determined by a 3-dimension electromagnetic simulation tool.
3. Keep trace length within 1-2 inches between the SFP module and IN1±. This minimizes insertion loss and return loss.
4. Use coupled differential traces with 100-Ω impedance for signal routing to IN1±, OUT0± and OUT1±. They are usually 5-8 mil trace width reference to a ground plane at Layer 2.
5. The exposed pad EP of the package should be connected to the ground plane through an array of vias. These vias are solder-masked to avoid solder flowing into the plated-through holes during the board manufacturing process.
6. Connect each supply pin (VDD_CDR, VIN, VDDIO, VDD_LDO) to the power or ground planes with a short via. The via is usually placed tangent to the supply pins' landing pads with the shortest trace possible.
7. Power supply bypass capacitors should be placed close to the supply pins. They are commonly placed at the bottom layer and share the ground of the EP.

10.2 Layout Example

The following example demonstrates the high speed signal trace routing to the LMH1226.

1. Anti-pad under passive components.
2. 100-Ω coupled trace.
3. Vias with solder mask.

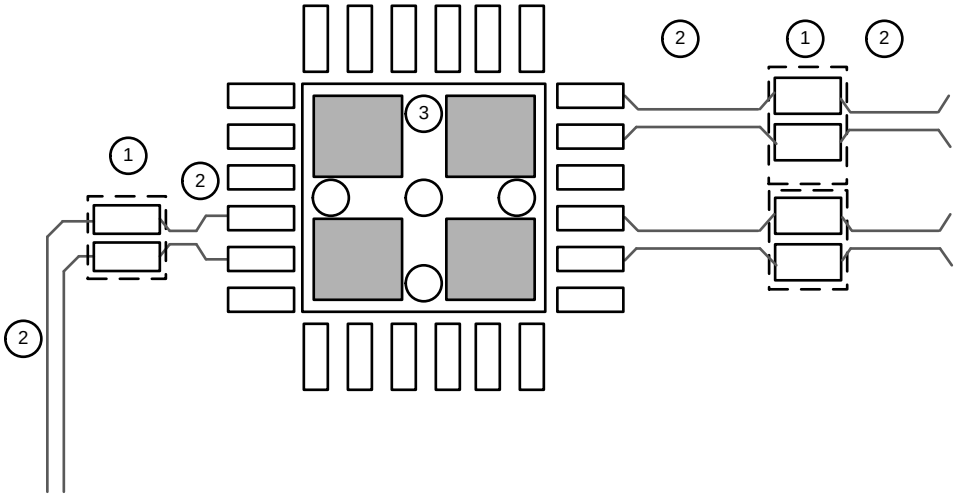


図 29. LMH1226 PCB Layout Example

11 デバイスおよびドキュメントのサポート

11.1 ドキュメントの更新通知を受け取る方法

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11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMH1226RTWR	ACTIVE	WQFN	RTW	24	3000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 85	L1226A2	Samples
LMH1226RTWT	ACTIVE	WQFN	RTW	24	250	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 85	L1226A2	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

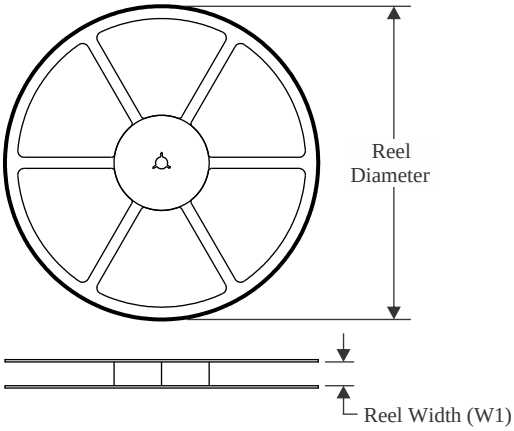
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

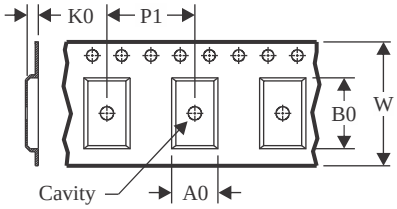
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

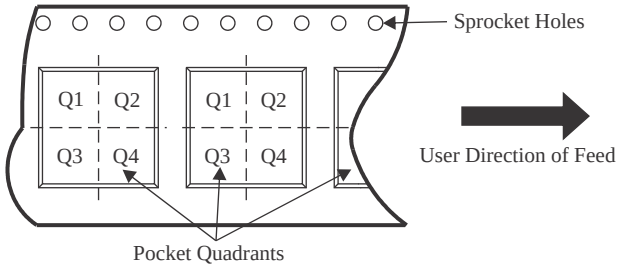


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

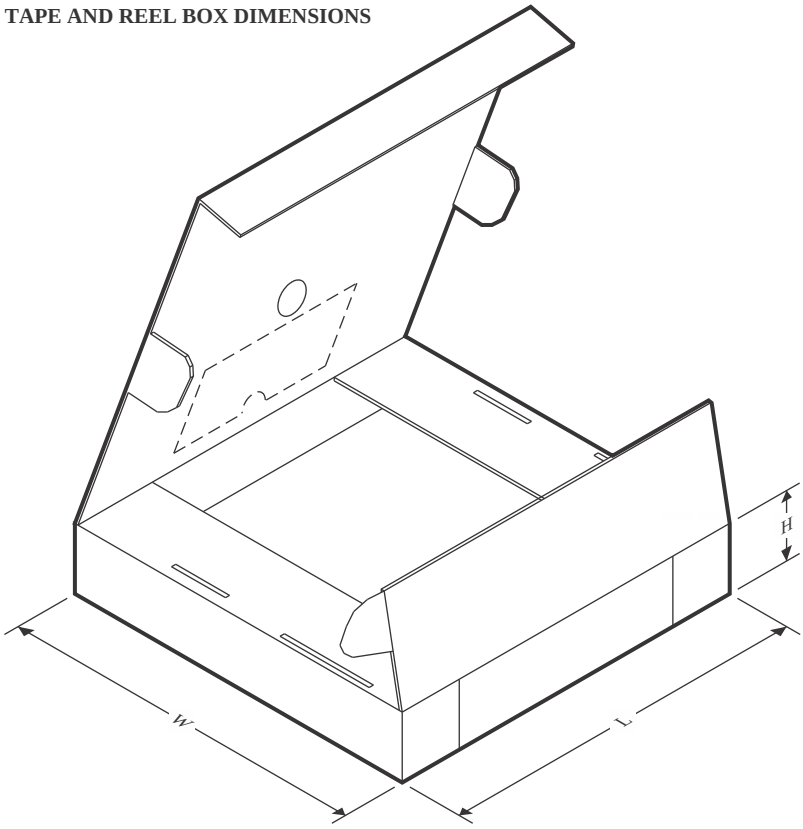
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH1226RTWR	WQFN	RTW	24	3000	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LMH1226RTWT	WQFN	RTW	24	250	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

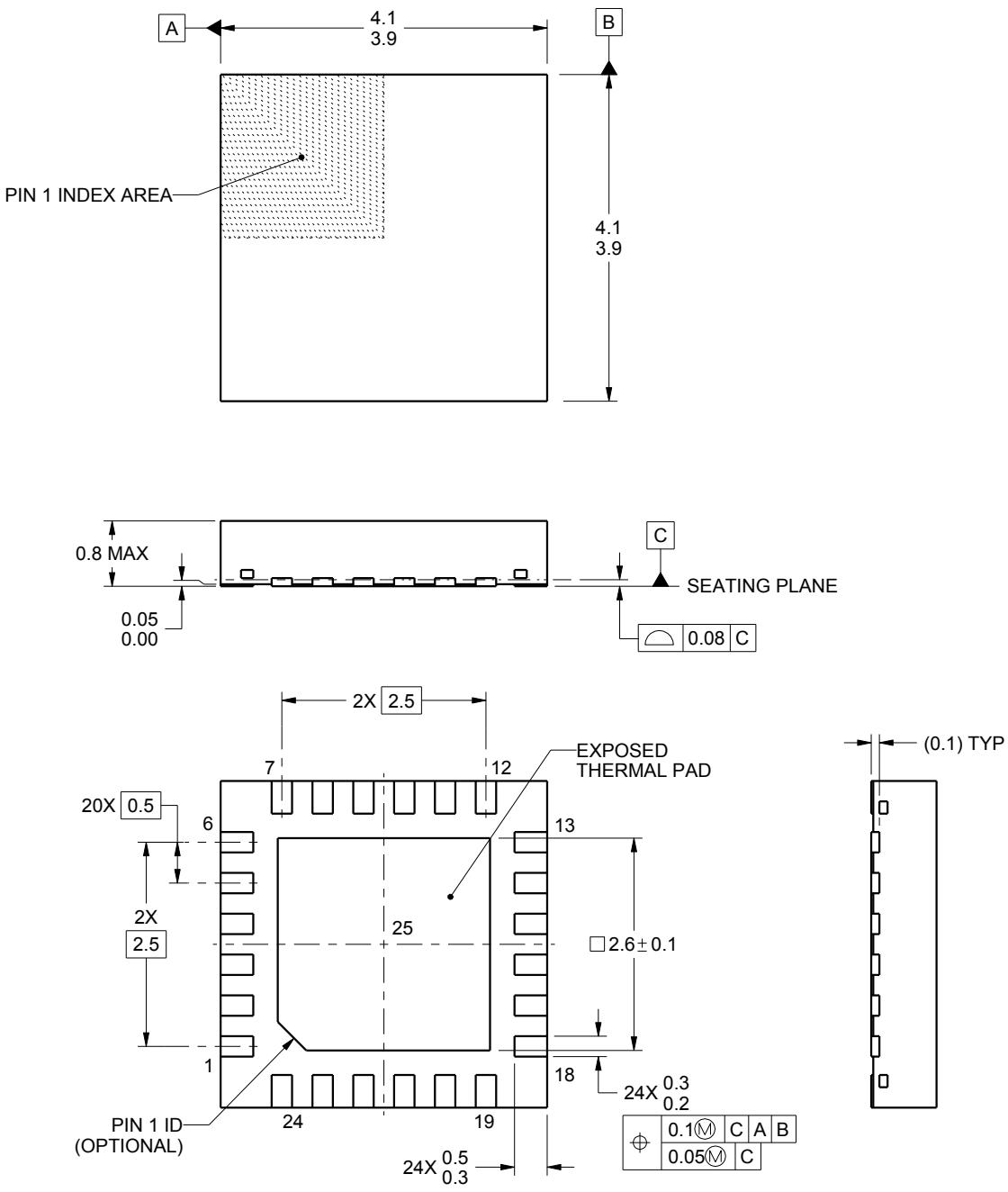
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH1226RTWR	WQFN	RTW	24	3000	356.0	356.0	35.0
LMH1226RTWT	WQFN	RTW	24	250	208.0	191.0	35.0

PACKAGE OUTLINE

RTW0024A

WQFN - 0.8 mm max height

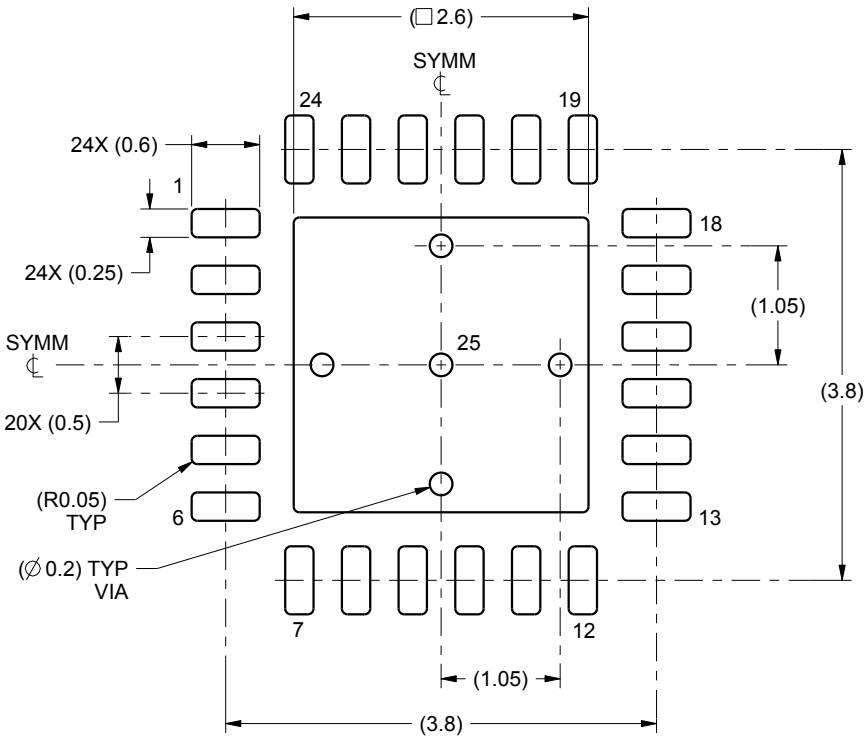
PLASTIC QUAD FLATPACK - NO LEAD



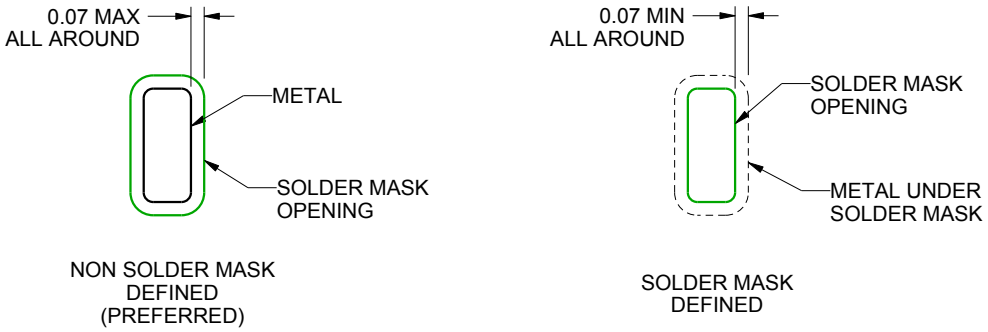
4222815/A 03/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:15X

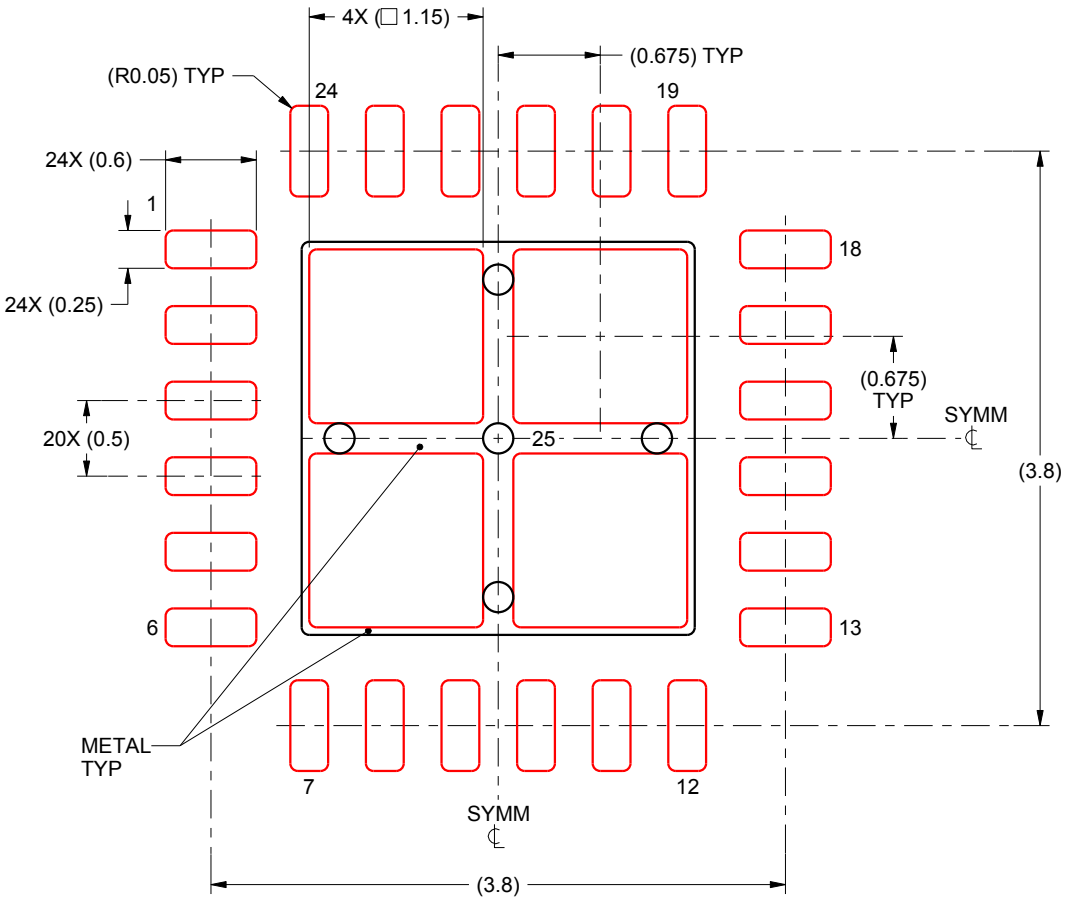


SOLDER MASK DETAILS

4222815/A 03/2016

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25:
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4222815/A 03/2016

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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