LMV831シングル/LMV832デュアル/LMV834クワッド 3.3MHz低消費電力CMOS、EMI強化オペアンプ

1 特長

- 特に記述のない限り、
  T_A = 25℃、V^+ = 3.3Vでの標準値
- 電源電圧: 2.7V～5.5V
- 消費電流(チャネルごとに): 240µA
- 入力オフセット電圧: 1mV (最大値)
- 入力バイアス電流: 0.1pA
- GBW: 3.3MHz
- 1.8GHz時のEMIRR: 120dB
- 1kHz時の入力ノイズ電圧: 12 nV/√Hz
- スルーレート: 2V/µs
- レール・ツー・レールの出力電圧スイング
- 出力電流ドライブ: 30mA
- 動作時周囲温度範囲: -40℃～+125℃

2 アプリケーション

- フォトダイオードのプリアンプ
- 圧電性センサ
- 携帯用およびバッテリ駆動の電子機器
- フィルタおよびバッファ
- PDAおよびスマートフォン用アクセサリ

3 概要

LMV83xデバイスはCMOS入力、低消費電力のオペアンプICで、入力バイアス電流が低く、-40℃～125℃の広い範囲の温度で動作し、性能が優れているため、堅牢な汎用部品として使用できます。さらに、LMV83xはEMI強化されており、干渉が最小限で、EMIに敏感なアプリケーションで理想的です。

LMV83xはユニティ・ゲイン安定で3.3MHzの帯域幅を備え、チャネルごとの消費電流はわずか0.24mAです。これらのデバイスは、最大200pFの容量性負荷で安定性を維持できます。LMV83xは優れた性能を実現するとともに、電力と占有面積の点で経済的に優れています。

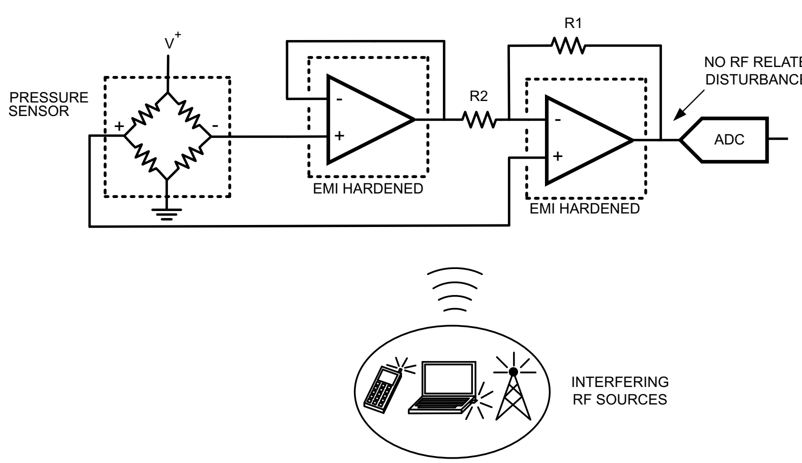
このファミリの部品は最大入力オフセット電圧が1mVで、レール・ツール・レールの出力段をもち、入力同相電圧範囲にグランドが含まれます。LMV83xは2.7V～5.5Vの動作範囲にわたってPSRRが93dB、CMRRが91dBです。LMV831は省スペースの5ピンSC70パッケージ、LMV832は8ピンVSSOP、LMV834は14ピンTSSOPパッケージで供給されます。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
LMV831	SC70 (5)	1.25mm×2.00mm
LMV832	VSSOP (8)	3.00mm×3.00mm
LMV834	TSSOP (14)	4.40mm×5.00mm

(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

代表的なアプリケーション



目次

4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision B (March 2013) から **Revision C** に変更 — **Page**

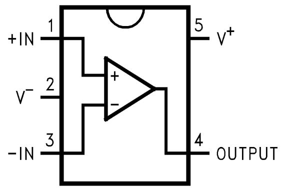
- 「*ESD定格*」の表、「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクションを追加。 1

Revision A (March 2013) から **Revision B** に変更 — **Page**

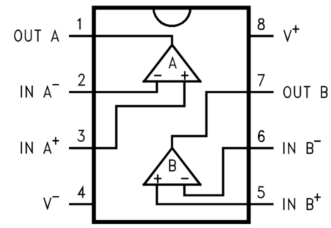
- Changed layout of National Semiconductor Data Sheet to TI format 24

5 Pin Configuration and Functions

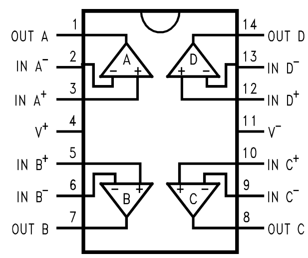
DCK Package
5-Pin SC70
Top View



DGK Package
8-Pin VSSOP
Top View



PW Package
14-Pin TSSOP
Top View



Pin Functions

PIN				TYPE	DESCRIPTION
NAME	SC70	VSSOP	TSSOP		
IN+	1	—	—	I	Noninverting Input
IN–	3	—	—	I	Inverting Input
IN A^+	—	3	3	I	Noninverting Input, Channel A
IN $A^–$	—	2	2	I	Inverting Input, Channel A
IN B^+	—	5	5	I	Noninverting Input, Channel B
IN $B^–$	—	6	6	I	Inverting Input, Channel B
IN C^+	—	—	10	I	Noninverting Input, Channel C
IN $C^–$	—	—	9	I	Inverting Input, Channel C
IN D^+	—	—	12	I	Noninverting Input, Channel D
IN $D^–$	—	—	13	I	Inverting Input, Channel D
OUT A	—	1	1	O	Output, Channel A
OUT B	—	7	7	O	Output, Channel B
OUT C	—	—	8	O	Output, Channel C
OUT D	—	—	14	O	Output, Channel D
OUTPUT	4	—	—	O	Output
V^+	5	8	4	P	Positive (highest) Power Supply
$V^–$	2	4	11	P	Negative (lowest) Power Supply

6 Specifications

6.1 Absolute Maximum Ratings

See [1][2]

		MIN	MAX	UNIT
V_{IN} differential		±Supply Voltage		V
Supply voltage ($V_S = V^+ – V^-$)			6	V
Voltage at input/output pins		$V^- − 0.4$	$V^+ + 0.4$	V
Junction temperature[3]			150	°C
Soldering information	Infrared or Convection (20 sec)		260	°C
Storage temperature, T_{stg}		−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} – T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge[1]	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101	±1000	
		Machine Model (MM)	±200	

(1) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC) Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).

6.3 Recommended Operating Conditions

	MIN	MAX	UNIT
Temperature range[1]	−40	125	°C
Supply voltage ($V_S = V^+ – V^-$)	2.7	5.5	V

(1) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} – T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PCB.

6.4 Thermal Information

THERMAL METRIC[1]		LMV831	LMV832	LMV834	UNIT
		DCK (SC70)	DGK (VSSOP)	PW (TSSOP)	
		5 PINS	8 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance [2]	267.7	177.1	118.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	96.6	67.1	44.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	48.8	97.5	60.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.5	9.9	4.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	47.9	96.1	59.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} – T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.

6.5 Electrical Characteristics, 3.3 V

Unless otherwise specified, all limits are specified for at T_A = 25°C, V^+ = 3.3 V, V^- = 0 V, V_{CM} = V^+/2, and R_L = 10 kΩ to V^+/2.(1)

PARAMETER		TEST CONDITIONS		MIN(2)	TYP(3)	MAX(2)	UNIT
V_{OS}	Input offset voltage(4)	T_A = 25°C			±0.25	±1	mV
		–40°C ≤ T_A ≤ +125°C				±1.23	
TCV_{OS}	Input offset voltage temperature drift(4)(5)	LMV831, LMV832			±0.5	±1.5	μV/°C
		LMV834			±0.5	±1.7	
I_B	Input bias current(5)	T_A = 25°C			0.1	10	pA
		–40°C ≤ T_A ≤ +125°C				500	
I_{OS}	Input offset current				1		pA
CMRR	Common-mode rejection ratio(4)	0.2 V ≤ V_{CM} ≤ V^+ – 1.2 V	T_A = 25°C	76	91		dB
			–40°C ≤ T_A ≤ +125°C	75			
PSRR	Power supply rejection ratio(4)	2.7 V ≤ V^+ ≤ 5.5 V, V_{OUT} = 1 V	T_A = 25°C	76	93		dB
			–40°C ≤ T_A ≤ +125°C	75			
EMIRR	EMI rejection ratio, IN+ and IN–(6)	V_{RF_PEAK} = 100 mV_P (−20 dB_P), f = 400 MHz			80		dB
		V_{RF_PEAK} = 100 mV_P (−20 dB_P), f = 900 MHz			90		
		V_{RF_PEAK} = 100 mV_P (−20 dB_P), f = 1800 MHz			110		
		V_{RF_PEAK} = 100 mV_P (−20 dB_P), f = 2400 MHz			120		
CMVR	Input common-mode voltage range	CMRR ≥ 65 dB		−0.1		2.1	V
A_{VOL}	Large signal voltage gain(7)	R_L = 2 kΩ, V_{OUT} = 0.15 V to 1.65 V, V_{OUT} = 3.15 V to 1.65 V	LMV831, LMV832	102	121		dB
			LMV831, LMV832, –40°C ≤ T_A ≤ +125°C	102			
			LMV834	102	121		
			LMV834 –40°C ≤ T_A ≤ +125°C	102			
		R_L = 10 kΩ, V_{OUT} = 0.1 V to 1.65 V, V_{OUT} = 3.2 V to 1.65 V	LMV831, LMV832	104	126		
			LMV831, LMV832, –40°C ≤ T_A ≤ +125°C	104			
			LMV834	104	123		
			LMV834 –40°C ≤ T_A ≤ +125°C	103			

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T_J > T_A.
(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlations using statistical quality control (SQC) method.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(4) The typical value is calculated by applying absolute value transform to the distribution, then taking the statistical average of the resulting distribution.
(5) This parameter is specified by design and/or characterization and is not tested in production.
(6) The EMI Rejection Ratio is defined as EMIRR = 20log ($V_{RF\_PEAK}/\Delta V_{OS}$).
(7) The specified limits represent the lower of the measured values for each output range condition.

Electrical Characteristics, 3.3 V (continued)

Unless otherwise specified, all limits are specified for at T_A = 25°C, V^+ = 3.3 V, V^- = 0 V, V_{CM} = V^+/2, and R_L = 10 kΩ to V^+/2.(1)

PARAMETER		TEST CONDITIONS		MIN(2)	TYP(3)	MAX(2)	UNIT
V_{OUT}	Output voltage swing high	R_L = 2 kΩ to V^+/2	LMV831, LMV832		29	36	mV from either rail
			LMV831, LMV832, –40°C ≤ T_A ≤ +125°C			43	
			LMV834		31	38	
			LMV834 –40°C ≤ T_A ≤ +125°C			44	
		R_L = 10 kΩ to V^+/2	LMV831, LMV832		6	8	
			LMV831, LMV832, –40°C ≤ T_A ≤ +125°C			9	
			LMV834		7	9	
			LMV834 –40°C ≤ T_A ≤ +125°C			10	
	Output voltage swing low	R = 2 kΩ to V^+/2	T_A = 25°C		25	34	
			–40°C ≤ T_A ≤ +125°C			43	
		R_L = 10 kΩ to V^+/2	T_A = 25°C		5	8	
			–40°C ≤ T_A ≤ +125°C			10	
I_{OUT}	Output short circuit current	Sourcing, V_{OUT} = V_{CM}, V_{IN} = 100 mV	LMV831, LMV832	27	28		mA
			LMV831, LMV832, –40°C ≤ T_A ≤ +125°C	22			
			LMV834	24	28		
			LMV834 –40°C ≤ T_A ≤ +125°C	19			
		Sinking, V_{OUT} = V_{CM}, V_{IN} = −100 mV	T_A = 25°C	27	32		
			–40°C ≤ T_A ≤ +125°C	21			
I_S	Supply current	LMV831			0.24	0.27	mA
		LMV831, –40°C ≤ T_A ≤ +125°C				0.3	
		LMV832			0.46	0.51	
		LMV832, –40°C ≤ T_A ≤ +125°C				0.58	
		LMV834			0.9	1	
		LMV834, –40°C ≤ T_A ≤ +125°C				1.16	
SR	Slew rate(8)	A_V = +1, V_{OUT} = 1 V_{PP}, 10% to 90%			2		V/μs
GBW	Gain bandwidth product				3.3		MHz
Φ_m	Phase margin				65		deg
e_n	Input referred voltage noise	f = 1 kHz			12		nV/√Hz
		f = 10 kHz			10		
i_n	Input referred current noise	f = 1 kHz			0.005		pA/√Hz
R_{OUT}	Closed-loop output impedance	f = 2 MHz			500		Ω

(8) Number specified is the slower of positive and negative slew rates.

Electrical Characteristics, 3.3 V (continued)

Unless otherwise specified, all limits are specified for at T_A = 25°C, V^+ = 3.3 V, V^- = 0 V, V_{CM} = $V^+/2$, and R_L = 10 kΩ to $V^+/2$.(1)

PARAMETER		TEST CONDITIONS	MIN(2)	TYP(3)	MAX(2)	UNIT
C_{IN}	Common-mode input capacitance			15		pF
	Differential-mode input capacitance			20		
THD+N	Total harmonic distortion + noise	f = 1 kHz, A_V = 1, BW ≥ 500 kHz		0.02%		

6.6 Electrical Characteristics, 5 V

Unless otherwise specified, all limits are specified for at T_A = 25°C, V^+ = 5 V, V^- = 0 V, V_{CM} = $V^+/2$, and R_L = 10 kΩ to $V^+/2$. (1)

PARAMETER		TEST CONDITIONS		MIN(2)	TYP(3)	MAX(2)	UNIT
V_{OS}	Input offset voltage(4)	T_A = 25°C			±0.25	±1	mV
		–40°C ≤ T_A ≤ +125°C				±1.23	
TCV_{OS}	Input offset voltage temperature drift(4)(5)	LMV831, LMV832			±0.5	±1.5	µV/°C
		LMV834			±0.5	±1.7	
I_B	Input bias current(5)	T_A = 25°C			0.1	10	pA
		–40°C ≤ T_A ≤ +125°C				500	
I_{OS}	Input offset current				1		pA
CMRR	Common-mode rejection ratio(4)	0 V ≤ V_{CM} ≤ V^+ −1.2 V	T_A = 25°C	77	93		dB
			–40°C ≤ T_A ≤ +125°C	77			
PSRR	Power supply rejection ratio(4)	2.7 V ≤ V^+ ≤ 5.5 V, V_{OUT} = 1 V	T_A = 25°C	76	93		dB
			–40°C ≤ T_A ≤ +125°C	75			
EMIRR	EMI rejection ratio, IN+ and IN–(6)	V_{RF_PEAK} = 100 mV_P (−20 dB_P), f = 400 MHz			80		dB
		V_{RF_PEAK} = 100 mV_P (−20 dB_P), f = 900 MHz			90		
		V_{RF_PEAK} = 100 mV_P (−20 dB_P), f = 1800 MHz			110		
		V_{RF_PEAK}=100 mV_P (−20 dB_P), f = 2400 MHz			120		
CMVR	Input common-mode voltage range	CMRR ≥ 65 dB		–0.1		3.8	V

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T_J > T_A.
(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlations using statistical quality control (SQC) method.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(4) The typical value is calculated by applying absolute value transform to the distribution, then taking the statistical average of the resulting distribution.
(5) This parameter is specified by design and/or characterization and is not tested in production.
(6) The EMI Rejection Ratio is defined as EMIRR = 20log ($V_{RF\_PEAK}/\Delta V_{OS}$).

Electrical Characteristics, 5 V (continued)

Unless otherwise specified, all limits are specified for at T_A = 25°C, V^+ = 5 V, V^- = 0 V, V_{CM} = V^+/2, and R_L = 10 kΩ to V^+/2. (1)

PARAMETER		TEST CONDITIONS		MIN (2)	TYP (3)	MAX (2)	UNIT
A_{VOL}	Large signal voltage gain (7)	R_L = 2 kΩ, V_{OUT} = 0.15 V to 2.5 V, V_{OUT} = 4.85 V to 2.5 V	LMV831, LMV832	107	127		dB
			LMV831, LMV832, –40°C ≤ T_A ≤ +125°C	106			
			LMV834	104	127		
			LMV834, –40°C ≤ T_A ≤ +125°C	104			
		R_L = 10 kΩ, V_{OUT} = 0.1 V to 2.5 V, V_{OUT} = 4.9 V to 2.5 V	LMV831, LMV832	107	130		
			LMV831, LMV832, –40°C ≤ T_A ≤ +125°C	107			
			LMV834	105	127		
			LMV834, –40°C ≤ T_A ≤ +125°C	104			
V_{OUT}	Output voltage swing high	R_L = 2 kΩ to V^+/2	LMV831, LMV832		32	42	mV from either rail
			LMV831, LMV832, –40°C ≤ T_A ≤ +125°C			49	
			LMV834		35	45	
			LMV834, –40°C ≤ T_A ≤ +125°C			52	
		R_L = 10 kΩ to V^+/2	LMV831, LMV832		6	9	
			LMV831, LMV832, –40°C ≤ T_A ≤ +125°C			10	
			LMV834		7	10	
			LMV834, –40°C ≤ T_A ≤ +125°C			11	
	Output voltage swing low	R_L = 2 kΩ to V^+/2	T_A = 25°C		27	43	
			–40°C ≤ T_A ≤ +125°C			52	
		R_L = 10 kΩ to V^+/2	T_A = 25°C		6	10	
			–40°C ≤ T_A ≤ +125°C			12	
I_{OUT}	Output short circuit current	Sourcing V_{OUT} = V_{CM} V_{IN} = 100 mV	LMV831, LMV832	59	66		mA
			LMV831, LMV832, –40°C ≤ T_A ≤ +125°C	49			
			LMV834	57	63		
			LMV834, –40°C ≤ T_A ≤ +125°C	45			
		Sinking V_{OUT} = V_{CM} V_{IN} = −100 mV	LMV831, LMV832	50	64		
			LMV831, LMV832, –40°C ≤ T_A ≤ +125°C	41			
			LMV834	53	63		
			LMV834, –40°C ≤ T_A ≤ +125°C	41			

(7) The specified limits represent the lower of the measured values for each output range condition.

Electrical Characteristics, 5 V (continued)

Unless otherwise specified, all limits are specified for at T_A = 25°C, V^+ = 5 V, V^- = 0 V, V_{CM} = V^+/2, and R_L = 10 kΩ to V^+/2. [1]

PARAMETER		TEST CONDITIONS	MIN[2]	TYP[3]	MAX[2]	UNIT
I_S	Supply current	LMV831		0.25	0.27	mA
		LMV831, –40°C ≤ T_A ≤ +125°C			0.31	
		LMV832		0.47	0.52	
		LMV832, –40°C ≤ T_A ≤ +125°C			0.6	
		LMV834		0.92	1.02	
		LMV834, –40°C ≤ T_A ≤ +125°C			1.18	
SR	Slew rate[8]	A_V = +1, V_{OUT} = 2 V_{PP}, 10% to 90%		2		V/µs
GBW	Gain bandwidth product			3.3		MHz
Φ_m	Phase margin			65		deg
e_n	Input referred voltage noise	f = 1 kHz		12		nV/√Hz
		f = 10 kHz		10		
i_n	Input referred current noise	f = 1 kHz		0.005		pA/√Hz
R_{OUT}	Closed-loop output impedance	f = 2 MHz		500		Ω
C_{IN}	Common-mode input capacitance			14		pF
	Differential-mode input capacitance			20		
THD+N	Total harmonic distortion + noise	f = 1 kHz, A_V = 1, BW ≥ 500 kHz		0.02%		

(8) Number specified is the slower of positive and negative slew rates.

6.7 Typical Characteristics

At T_A = 25°C, R_L = 10 kΩ, V^+ = 3.3 V, V^- = 0 V, Unless otherwise specified.

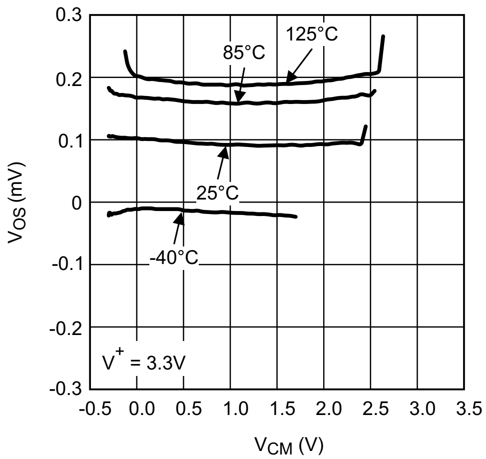


Figure 1. V_{OS} vs V_{CM} at V^+ = 3.3 V

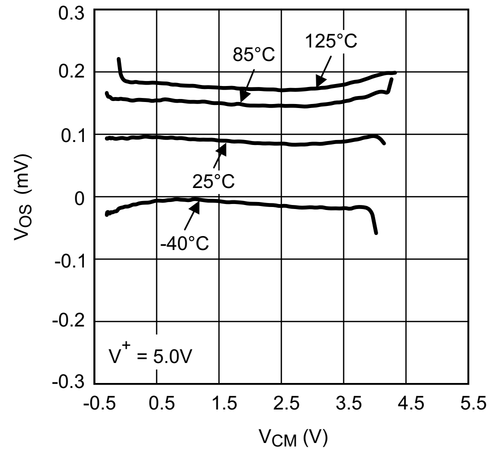


Figure 2. V_{OS} vs V_{CM} at V^+ = 5 V

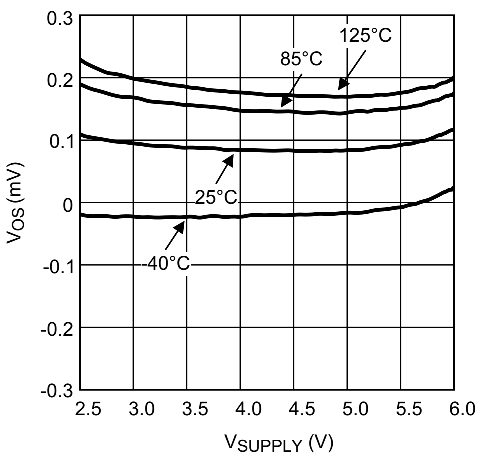


Figure 3. V_{OS} vs Supply Voltage

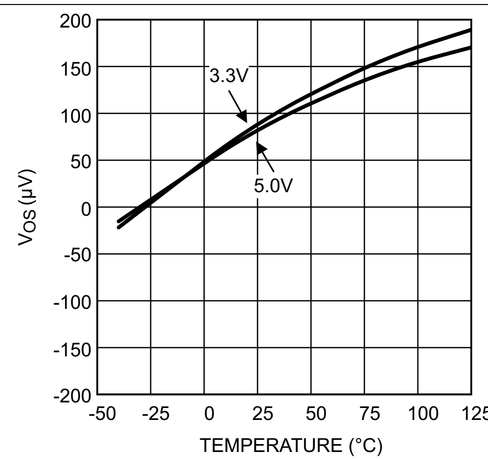


Figure 4. V_{OS} vs Temperature

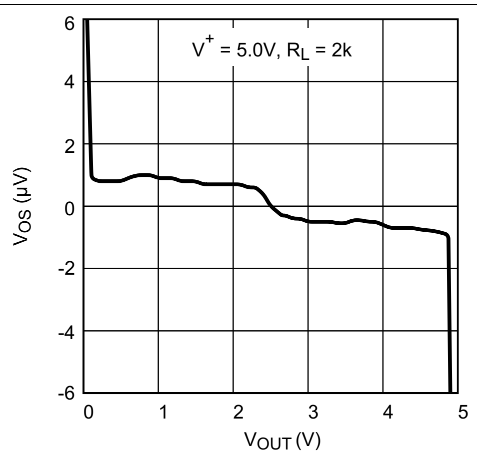


Figure 5. V_{OS} vs V_{OUT}

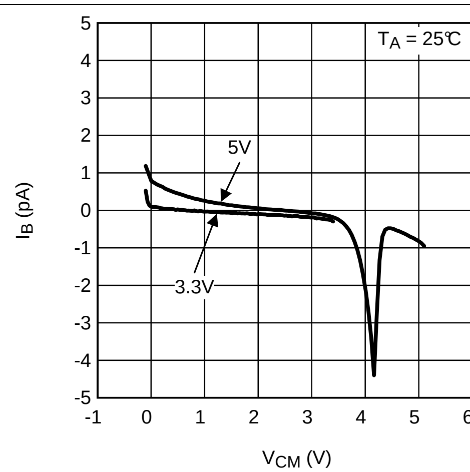


Figure 6. Input Bias Current vs V_{CM} at 25°C

Typical Characteristics (continued)

At T_A = 25°C, R_L = 10 kΩ, V^+ = 3.3 V, V^- = 0 V, Unless otherwise specified.

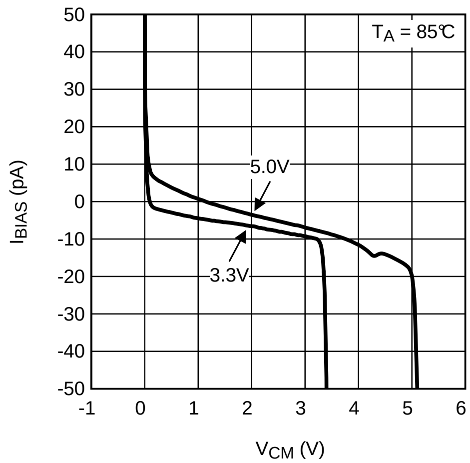


Figure 7. Input Bias Current vs V_{CM} at 85°C

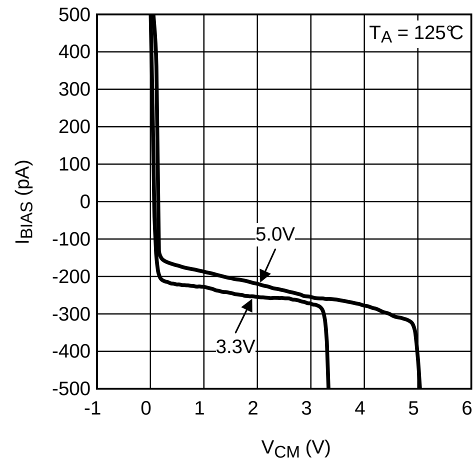


Figure 8. Input Bias Current vs V_{CM} at 125°C

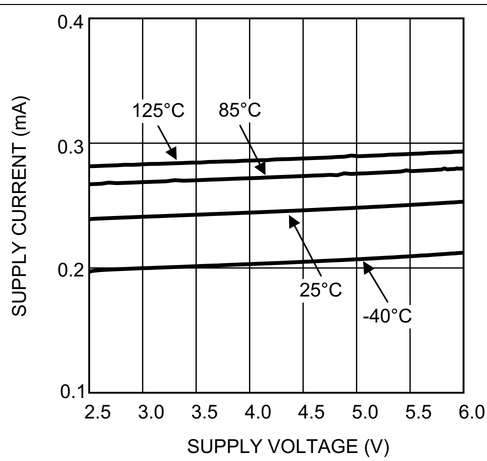


Figure 9. Supply Current vs Supply Voltage Single LMV831

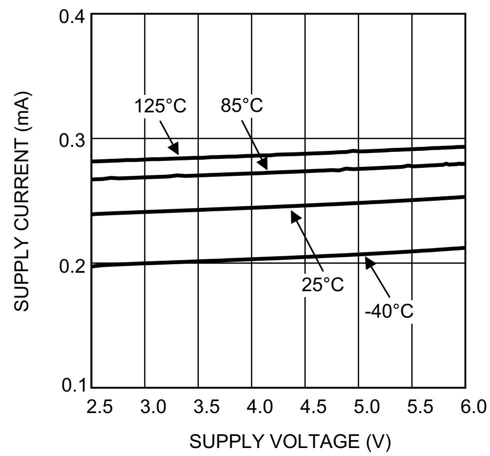


Figure 10. Supply Current vs Supply Voltage Dual LMV832

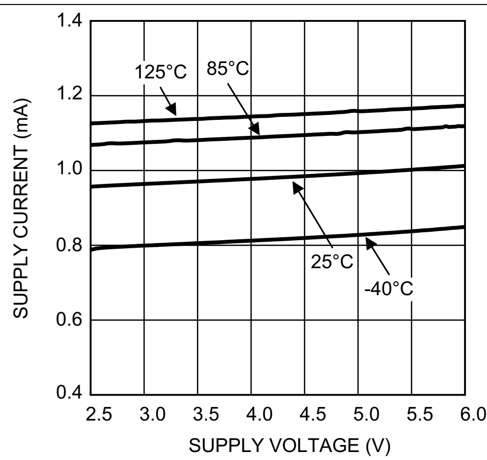


Figure 11. Supply Current vs Supply Voltage Quad LMV834

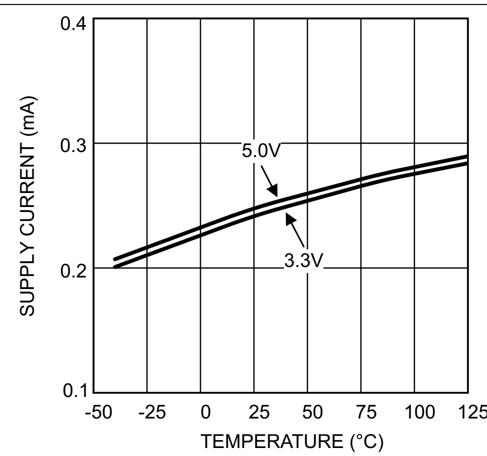


Figure 12. Supply Current vs Temperature Single LMV831

Typical Characteristics (continued)

At T_A = 25°C, R_L = 10 kΩ, V^+ = 3.3 V, V^- = 0 V, Unless otherwise specified.

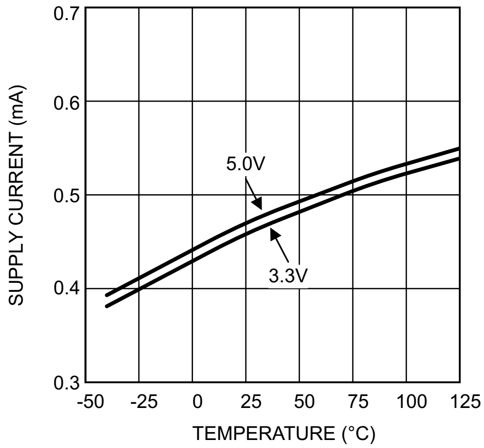


Figure 13. Supply Current vs Temperature Dual LMV832

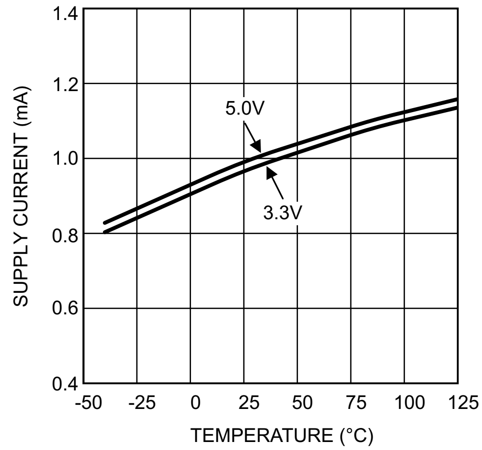


Figure 14. Supply Current vs Temperature Quad LMV834

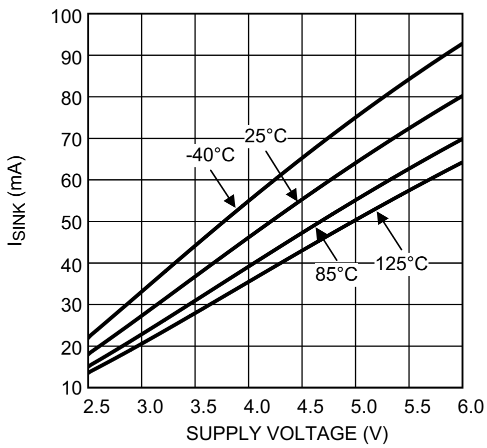


Figure 15. Sinking Current vs Supply Voltage

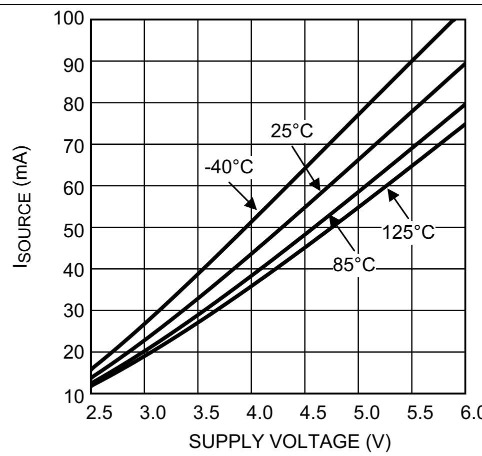
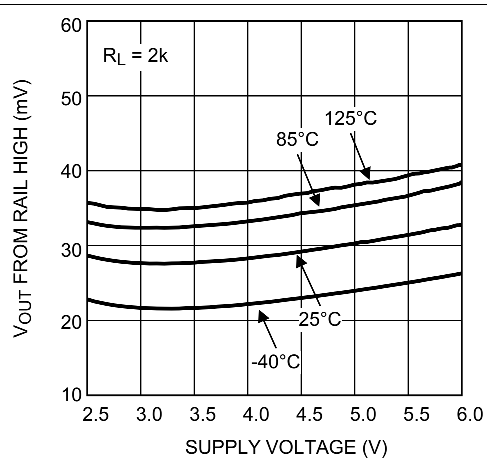
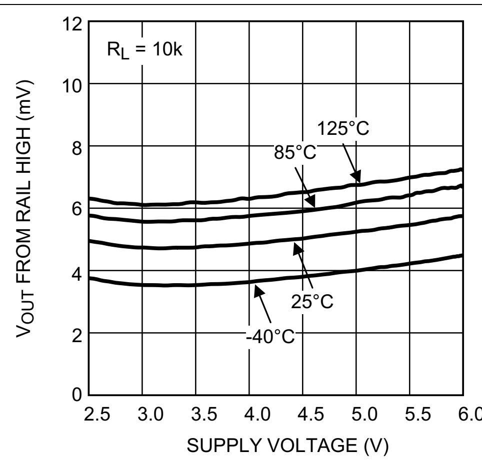


Figure 16. Sourcing Current vs Supply Voltage



R_L = 2 kΩ

Figure 17. Output Swing High vs Supply Voltage

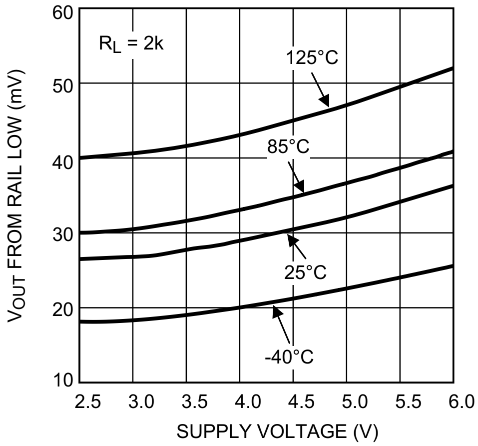


R_L = 10 kΩ

Figure 18. Output Swing High vs Supply Voltage

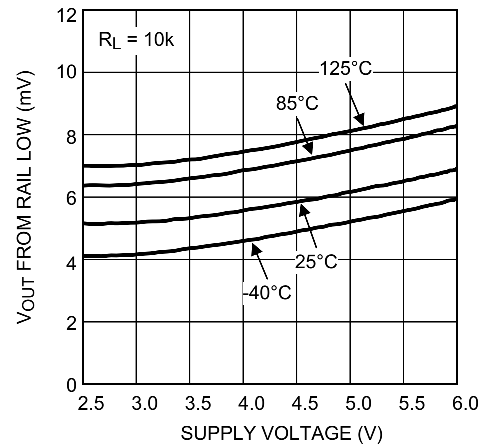
Typical Characteristics (continued)

At T_A = 25°C, R_L = 10 kΩ, V^+ = 3.3 V, V^- = 0 V, Unless otherwise specified.



R_L = 2 kΩ

Figure 19. Output Swing Low vs Supply Voltage



R_L = 10 kΩ

Figure 20. Output Swing Low vs Supply Voltage

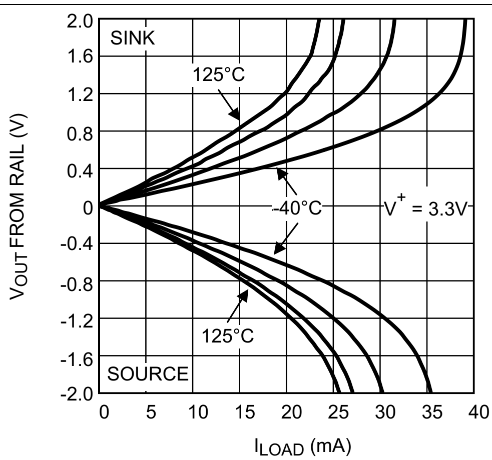


Figure 21. Output Voltage Swing vs Load Current at V^+ = 3.3 V

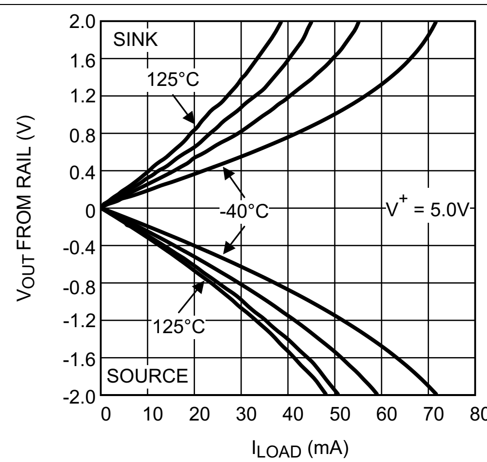


Figure 22. Output Voltage Swing vs Load Current at V^+ = 5 V

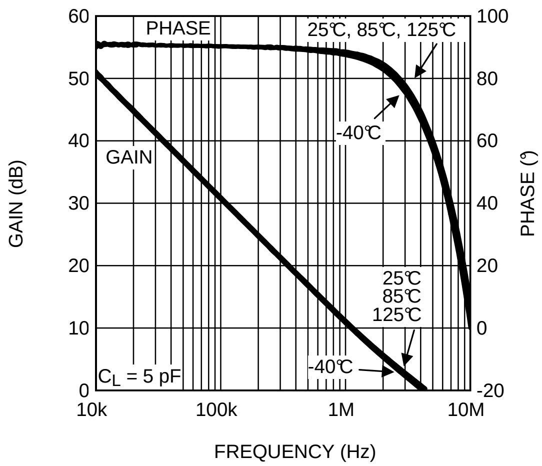


Figure 23. Open-Loop Frequency Response vs Temperature

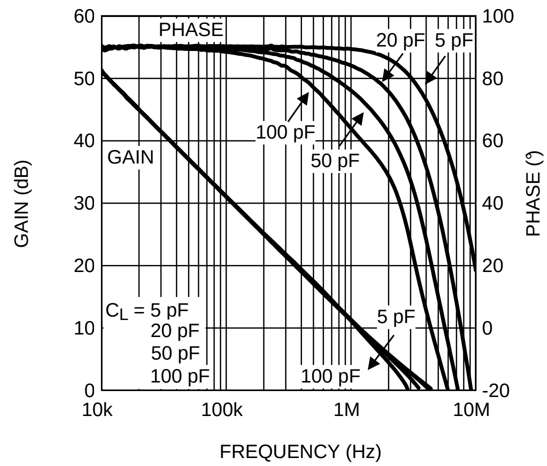


Figure 24. Open-Loop Frequency Response vs Load Conditions

Typical Characteristics (continued)

At T_A = 25°C, R_L = 10 kΩ, V^+ = 3.3 V, V^- = 0 V, Unless otherwise specified.

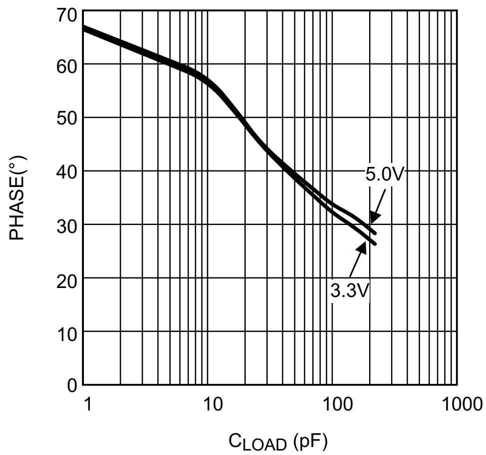


Figure 25. Phase Margin vs Capacitive Load

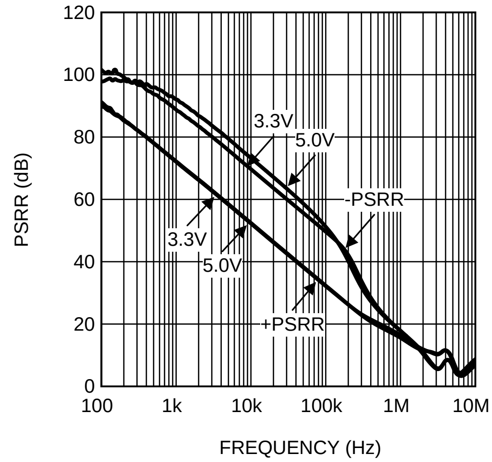


Figure 26. PSRR vs Frequency

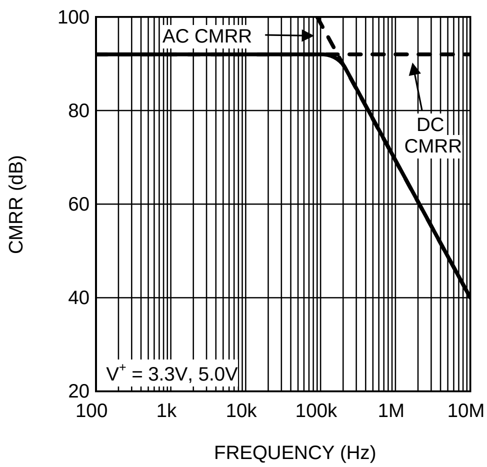


Figure 27. CMRR vs Frequency

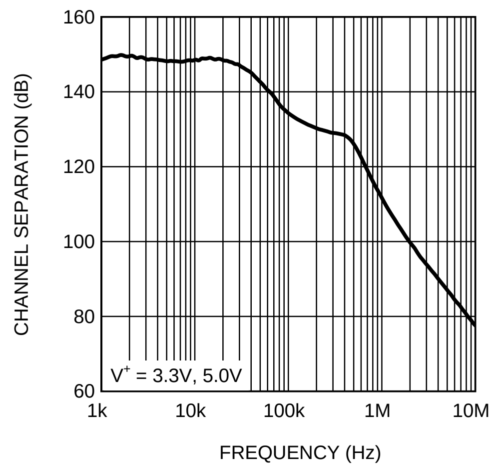


Figure 28. Channel Separation vs Frequency

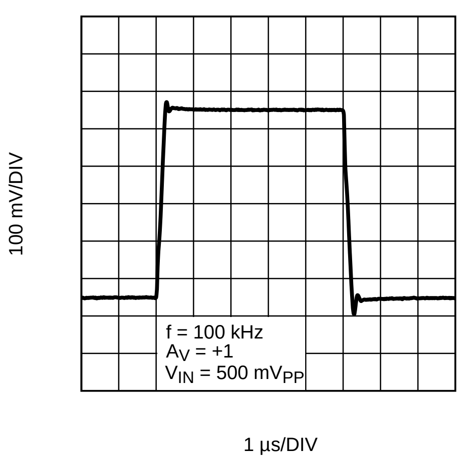


Figure 29. Large Signal Step Response With Gain = 1

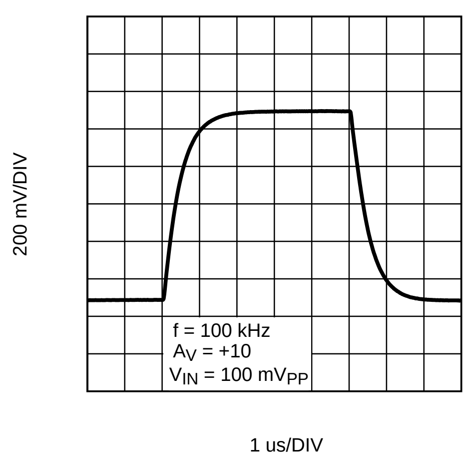


Figure 30. Large Signal Step Response With Gain = 10

Typical Characteristics (continued)

At T_A = 25°C, R_L = 10 kΩ, V^+ = 3.3 V, V^- = 0 V, Unless otherwise specified.

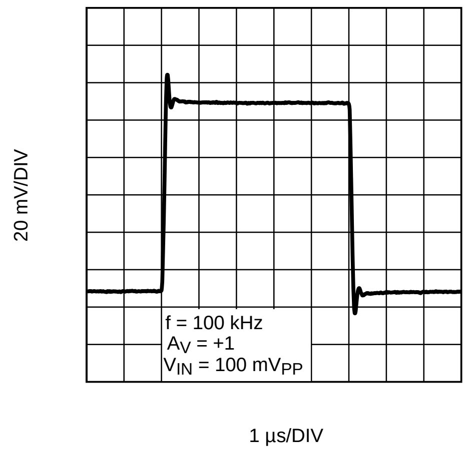


Figure 31. Small Signal Step Response With Gain = 1

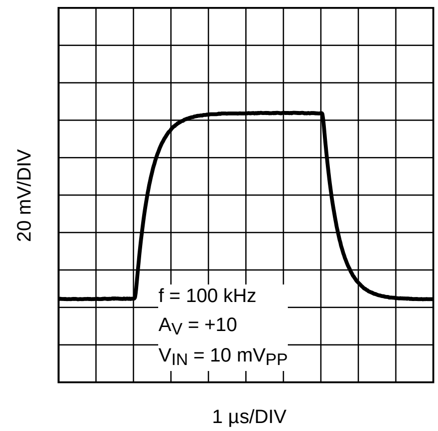


Figure 32. Small Signal Step Response With Gain = 10

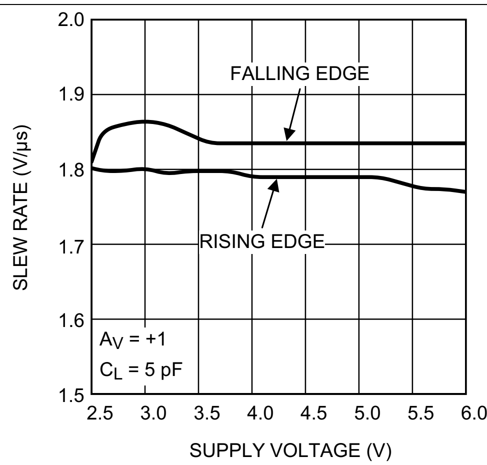


Figure 33. Slew Rate vs Supply Voltage

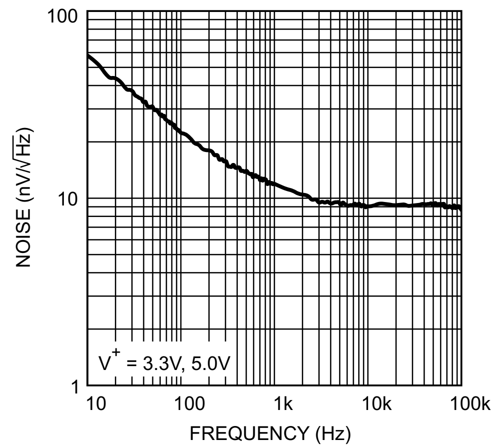


Figure 34. Input Voltage Noise vs Frequency

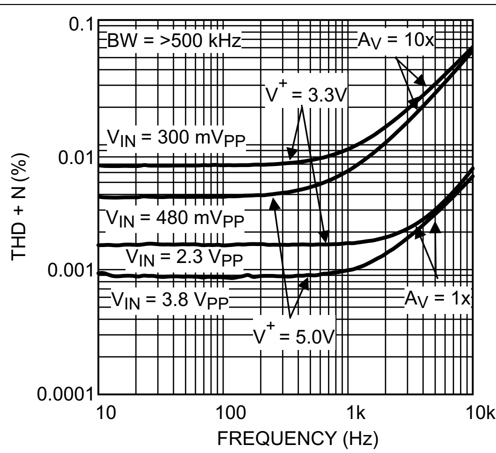


Figure 35. THD+N vs Frequency

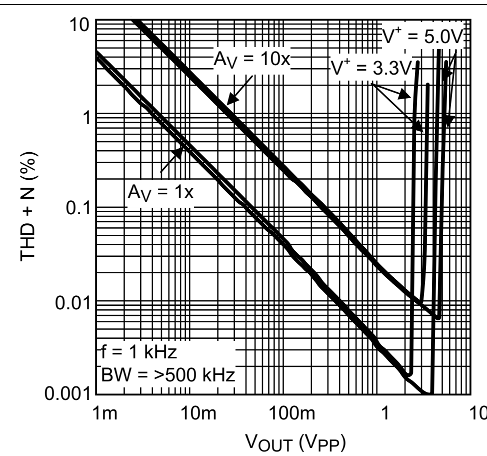


Figure 36. THD+N vs Amplitude

Typical Characteristics (continued)

At T_A = 25°C, R_L = 10 kΩ, V^+ = 3.3 V, V^- = 0 V, Unless otherwise specified.

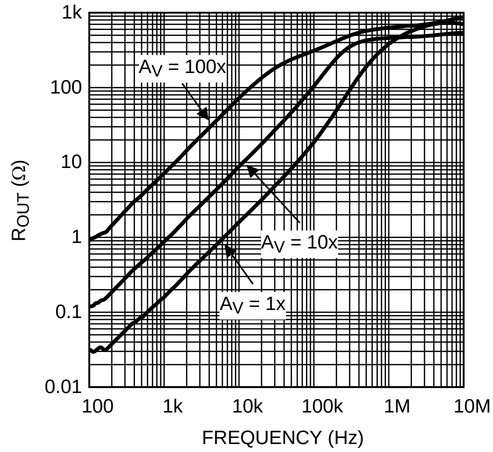


Figure 37. R_{OUT} vs Frequency

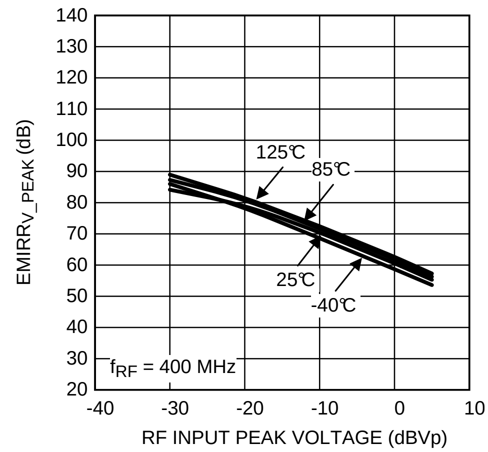


Figure 38. EMIRR IN+ vs Power at 400 MHz

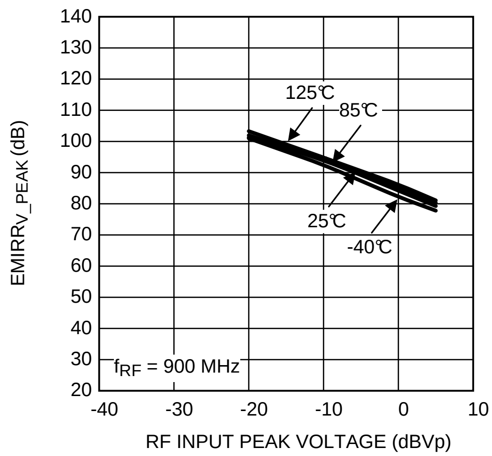


Figure 39. EMIRR IN+ vs Power at 900 MHz

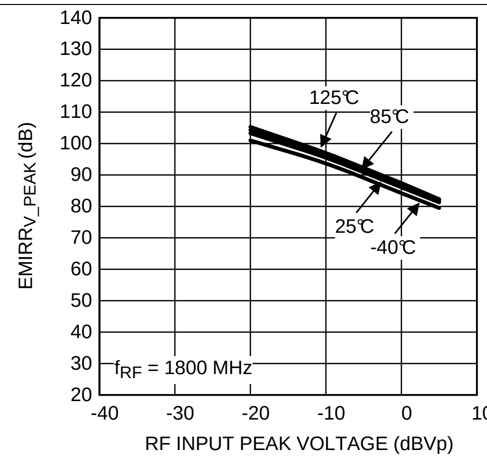


Figure 40. EMIRR IN+ vs Power at 1800 MHz

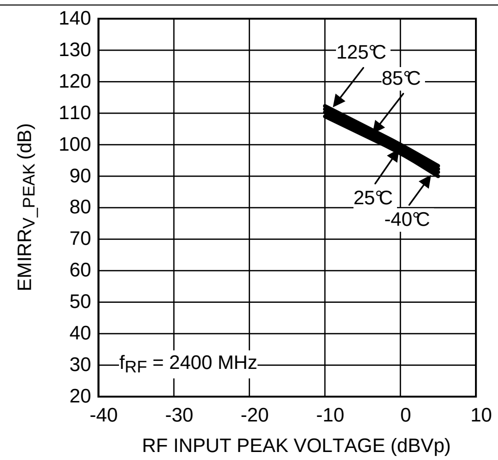


Figure 41. EMIRR IN+ vs Power at 2400 MHz

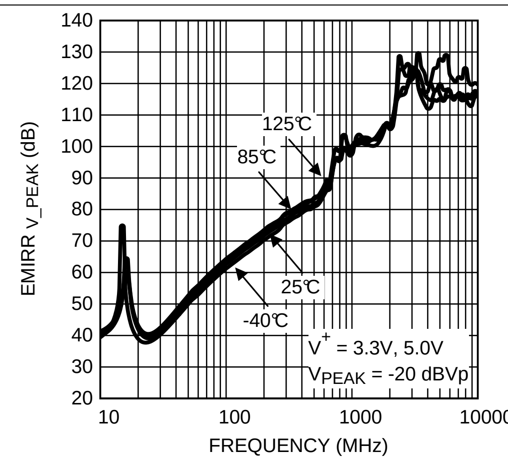


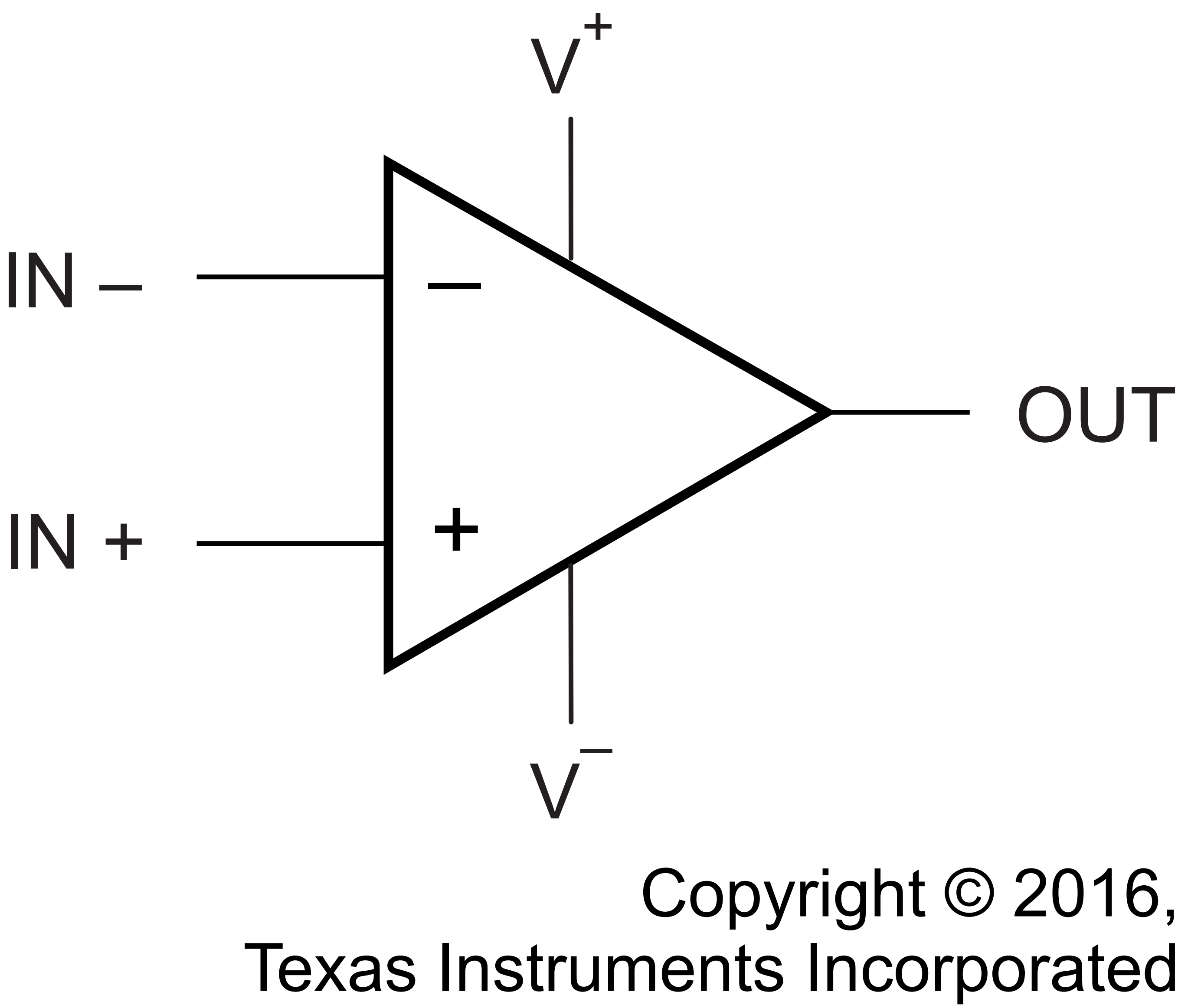
Figure 42. EMIRR IN+ vs Frequency

7 Detailed Description

7.1 Overview

The LMV831, LMV832, and LMV834 are operational amplifiers with excellent specifications, such as low offset, low noise and a rail-to-rail output. The EMI hardening makes the LMV831, LMV832 or LMV834 a must for almost all operational amplifier applications that are exposed to Radio Frequency (RF) signals such as the signals transmitted by mobile phones or wireless computer peripherals. The LMV831, LMV832, and LMV834 will effectively reduce disturbances caused by RF signals to a level that will be hardly noticeable. This again reduces the need for additional filtering and shielding. Using this EMI resistant series of operational amplifiers will thus reduce the number of components and space needed for applications that are affected by EMI, and will help applications, not yet identified as possible EMI sensitive, to be more robust for EMI.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Input Characteristics

The input common-mode voltage range of the LMV831, LMV832, and LMV834 includes ground, and can even sense well below ground. The CMRR level does not degrade for input levels up to 1.2 V below the supply voltage. For a supply voltage of 5 V, the maximum voltage that should be applied to the input for best CMRR performance is thus 3.8 V.

When not configured as unity gain, this input limitation will usually not degrade the effective signal range. The output is rail-to-rail and therefore will introduce no limitations to the signal range.

The typical offset is only 0.25 mV, and the TCV_{OS} is 0.5 μV/°C, specifications close to precision operational amplifiers.

7.3.2 EMIRR

With the increase of RF transmitting devices in the world, the electromagnetic interference (EMI) between those devices and other equipment becomes a bigger challenge. The LMV831, LMV832, and LMV834 are EMI-hardened operational amplifiers which are specifically designed to overcome electromagnetic interference. Along with EMI-hardened operational amplifiers, the EMIRR parameter is introduced to unambiguously specify the EMI performance of an operational amplifier. This section presents an overview of EMIRR. A detailed description on this specification for EMI-hardened operational amplifiers can be found in AN-1698 (SNOA497).

The dimensions of an operational amplifier IC are relatively small compared to the wavelength of the disturbing RF signals. As a result the operational amplifier itself will hardly receive any disturbances. The RF signals interfering with the operational amplifier are dominantly received by the PCB and wiring connected to the operational amplifier. As a result the RF signals on the pins of the operational amplifier can be represented by voltages and currents. This representation significantly simplifies the unambiguous measurement and specification of the EMI performance of an operational amplifier.

RF signals interfere with operational amplifiers through the non-linearity of the operational amplifier circuitry. This non-linearity results in the detection of the so called out-of-band signals. The obtained effect is that the amplitude modulation of the out-of-band signal is downconverted into the base band. This base band can easily overlap with the band of the operational amplifier circuit. As an example Figure 43 depicts a typical output signal of a unity-gain connected operational amplifier in the presence of an interfering RF signal. Clearly the output voltage varies in the rhythm of the on-off keying of the RF carrier.

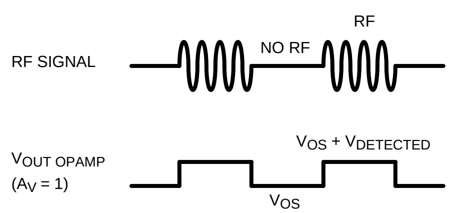


Figure 43. Offset Voltage Variation Due to an Interfering RF Signal

7.3.3 EMIRR Definition

To identify EMI-hardened operational amplifiers, a parameter is needed that quantitatively describes the EMI performance of operational amplifiers. A quantitative measure enables the comparison and the ranking of operational amplifiers on their EMI robustness. Therefore the EMI Rejection Ratio (EMIRR) is introduced. This parameter describes the resulting input-referred offset voltage shift of an operational amplifier as a result of an applied RF carrier (interference) with a certain frequency and level. The definition of EMIRR is given by Equation 1:

$$EMIRR_{V_{RF\_PEAK}} = 20 \log \left(\frac{V_{RF\_PEAK}}{\Delta V_{OS}} \right)$$

In which

- V_{RF_PEAK} is the amplitude of the applied un-modulated RF signal (V)

Feature Description (continued)

- ΔV_{OS} is the resulting input-referred offset voltage shift (V) (1)

The offset voltage depends quadratically on the applied RF level, and therefore, the RF level at which the EMIRR is determined should be specified. The standard level for the RF signal is 100 mV_P. AN-1698 (SNOA497) addresses the conversion of an EMIRR measured for an other signal level than 100 mV_P. The interpretation of the EMIRR parameter is straightforward. When two operational amplifiers have an EMIRR which differ by 20 dB, the resulting error signals when used in identical configurations, differ by 20 dB as well. So, the higher the EMIRR, the more robust the operational amplifier.

7.3.3.1 Coupling an RF Signal to the IN+ Pin

Each of the operational amplifier pins can be tested separately on EMIRR. In this section, the measurements on the IN+ pin (which, based on symmetry considerations, also apply to the IN– pin) are discussed. In AN-1698 (SNOA497) the other pins of the operational amplifier are treated as well. For testing the IN+ pin the operational amplifier is connected in the unity gain configuration. Applying the RF signal is straightforward as it can be connected directly to the IN+ pin. As a result the RF signal path has a minimum of components that might affect the RF signal level at the pin. The circuit diagram is shown in Figure 44. The PCB trace from RF_{IN} to the IN+ pin should be a 50-Ω stripline in order to match the RF impedance of the cabling and the RF generator. On the PCB a 50-Ω termination is used. This 50-Ω resistor is also used to set the bias level of the IN+ pin to ground level. For determining the EMIRR, two measurements are needed: one is measuring the DC output level when the RF signal is off; and the other is measuring the DC output level when the RF signal is switched on. The difference of the two DC levels is the output voltage shift as a result of the RF signal. As the operational amplifier is in the unity-gain configuration, the input referred offset voltage shift corresponds one-to-one to the measured output voltage shift.

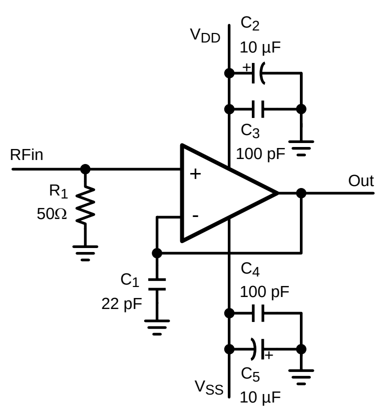


Figure 44. Circuit for Coupling the RF Signal to IN+

7.3.3.2 Cell Phone Call

The effect of electromagnetic interference is demonstrated in a set-up where a cell phone interferes with a pressure sensor application. The application is shown in Figure 49.

This application needs two operational amplifiers and therefore a dual operational amplifier is used. The operational amplifier configured as a buffer and connected at the negative output of the pressure sensor prevents the loading of the bridge by resistor R2. The buffer also prevents the resistors of the sensor from affecting the gain of the following gain stage. The operational amplifiers are placed in a single-supply configuration.

The experiment is performed on two different dual operational amplifiers: a typical standard operational amplifier and the LMV832, EMI-hardened dual operational amplifier. A cell phone is placed on a fixed position a couple of centimeters from the operational amplifiers in the sensor circuit.

Feature Description (continued)

When the cell phone is called, the PCB and wiring connected to the operational amplifiers receive the RF signal. Subsequently, the operational amplifiers detect the RF voltages and currents that end up at their pins. The resulting effect on the output of the second operational amplifier is shown in Figure 45.

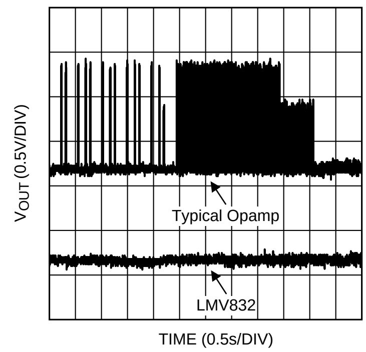


Figure 45. Comparing EMI Robustness

The difference between the two types of dual operational amplifiers is clearly visible. The typical standard dual operational amplifier has an output shift (disturbed signal) larger than 1 V as a result of the RF signal transmitted by the cell phone. The LMV832, EMI-hardened operational amplifier does not show any significant disturbances. This means that the RF signal will not disturb the signal entering the ADC when using the LMV832.

7.4 Device Functional Modes

7.4.1 Output Characteristics

As already mentioned the output is rail-to-rail. When loading the output with a 10-kΩ resistor the maximum swing of the output is typically 6 mV from the positive and negative rail.

The output of the LMV83x can drive currents up to 30 mA at 3.3 V and even up to 65 mA at 5 V.

The LMV83x can be connected as noninverting unity-gain amplifiers. This configuration is the most sensitive to capacitive loading. The combination of a capacitive load placed at the output of an amplifier along with the output impedance of the amplifier creates a phase lag, which reduces the phase margin of the amplifier. If the phase margin is significantly reduced, the response will be under damped which causes peaking in the transfer and, when there is too much peaking, the operational amplifier might start oscillating. The LMV83x can directly drive capacitive loads up to 200 pF without any stability issues. In order to drive heavier capacitive loads, an isolation resistor, R_{ISO}, should be used, as shown in Figure 46. By using this isolation resistor, the capacitive load is isolated from the output of the amplifier, and hence, the pole caused by C_L is no longer in the feedback loop. The larger the value of R_{ISO}, the more stable the amplifier will be. If the value of R_{ISO} is sufficiently large, the feedback loop will be stable, independent of the value of C_L. However, larger values of R_{ISO} result in reduced output swing and reduced output current drive.

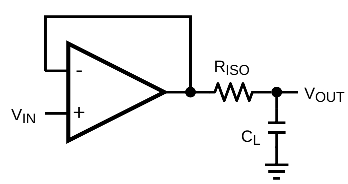


Figure 46. Isolating Capacitive Load

A resistor value of around 150 Ω would be sufficient. As an example some values are given in Table 1, for 5 V.

Device Functional Modes (continued)

Table 1. Resistor Values

C_{LOAD}	R_{ISO}
300 pF	165 Ω
400 pF	175 Ω
500 pF	185 Ω

7.4.2 CMRR Measurement

The CMRR measurement results may need some clarification. This is because different set-ups are used to measure the AC CMRR and the DC CMRR.

The DC CMRR is derived from ΔV_{OS} versus ΔV_{CM}. This value is stated in the tables, and is tested during production testing. The AC CMRR is measured with the test circuit shown in Figure 47.

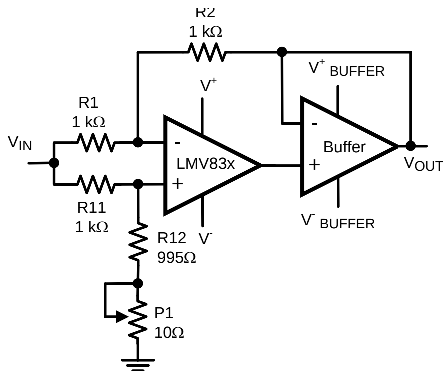


Figure 47. AC CMRR Measurement Set-Up

The configuration is largely the usually applied balanced configuration. With potentiometer P1, the balance can be tuned to compensate for the DC offset in the DUT. The main difference is the addition of the buffer. This buffer prevents the open-loop output impedance of the DUT from affecting the balance of the feedback network. Now the closed-loop output impedance of the buffer is a part of the balance. As the closed-loop output impedance is much lower, and by careful selection of the buffer also has a larger bandwidth, the total effect is that the CMRR of the DUT can be measured much more accurately. The differences are apparent in the larger measured bandwidth of the AC CMRR.

One artifact from this test circuit is that the low frequency CMRR results appear higher than expected. This is because in the AC CMRR test circuit the potentiometer is used to compensate for the DC mismatches. So, mainly AC mismatch is all that remains. Therefore, the obtained DC CMRR from this AC CMRR test circuit tends to be higher than the actual DC CMRR based on DC measurements.

The CMRR curve in Figure 48 shows a combination of the AC CMRR and the DC CMRR.

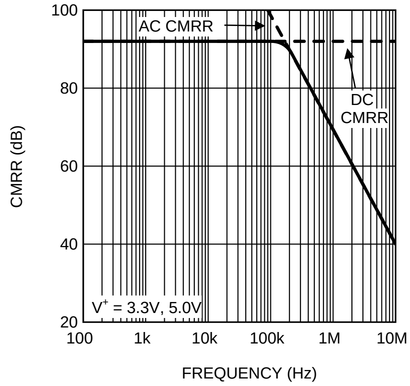


Figure 48. CMRR Curve

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LMV83x family of amplifiers is specified for operation from 2.7 V to 5.5 V (±1.35 V to ±2.25 V). Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics*.

8.2 Typical Application

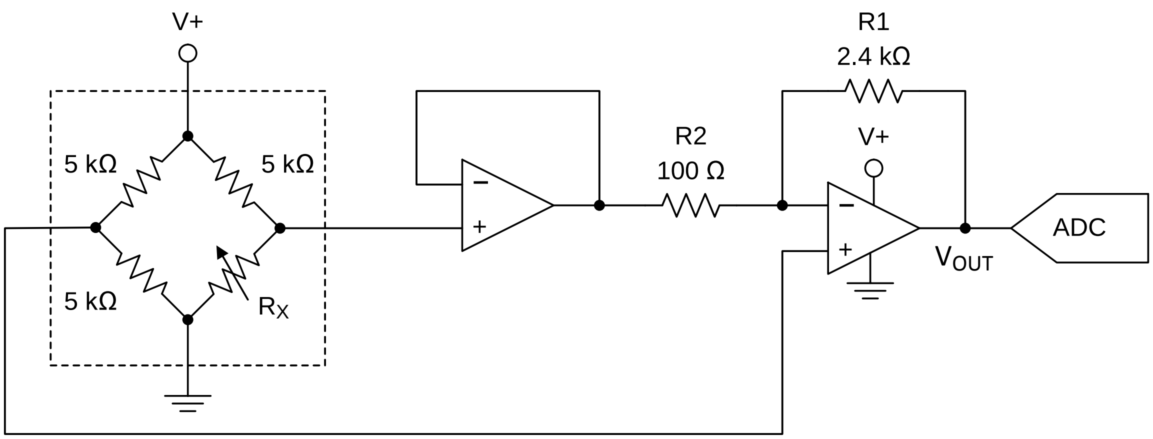


Figure 49. Pressure Sensor Application

8.2.1 Design Requirements

The LMV83x can be used for pressure sensor applications. Because of their low power the LMV83x are ideal for portable applications, such as blood pressure measurement devices, or portable barometers. This example describes a universal pressure sensor that can be used as a starting point for different types of sensors and applications.

The pressure sensor used in this example functions as a Wheatstone bridge. The value of the resistors in the bridge change when pressure is applied to the sensor. This change of the resistor values will result in a differential output voltage, depending on the sensitivity of the sensor and the applied pressure.

8.2.2 Detailed Design Procedure

The difference between the output at full-scale pressure and the output at zero pressure is defined as the span of the pressure sensor. A typical value for the span is 100 mV. A typical value for the resistors in the bridge is 5 kΩ. Loading of the resistor bridge could result in incorrect output voltages of the sensor. Therefore the selection of the circuit configuration, which connects to the sensor, should take into account a minimum loading of the sensor.

The configuration shown in Figure 49 is simple, and is very useful for the read out of pressure sensors. With two operational amplifiers in this application, the dual LMV832 fits very well. The operational amplifier configured as a buffer and connected at the negative output of the pressure sensor prevents the loading of the bridge by resistor R2. The buffer also prevents the resistors of the sensor from affecting the gain of the following gain stage. Given the differential output voltage V_S of the pressure sensor, the output signal of this operational amplifier configuration, V_{OUT}, equals Equation 2:

Typical Application (continued)

$$V_{OUT} = \frac{V_{DD}}{2} - \frac{V_S}{2}\left(1+2\times\frac{R1}{R2}\right) \quad (2)$$

To align the pressure range with the full range of an ADC, the power supply voltage and the span of the pressure sensor are needed. For this example a power supply of 5 V is used and the span of the sensor is 100 mV. When a 100-Ω resistor is used for R2, and a 2.4-kΩ resistor is used for R1, the maximum voltage at the output is 4.95 V and the minimum voltage is 0.05 V. This signal is covering almost the full input range of the ADC. Further processing can take place in the microprocessor following the ADC.

8.2.3 Application Curve

Figure 50 shows the resulting output voltage as R_X is varied between 4.5 kΩ and 5.5 kΩ.

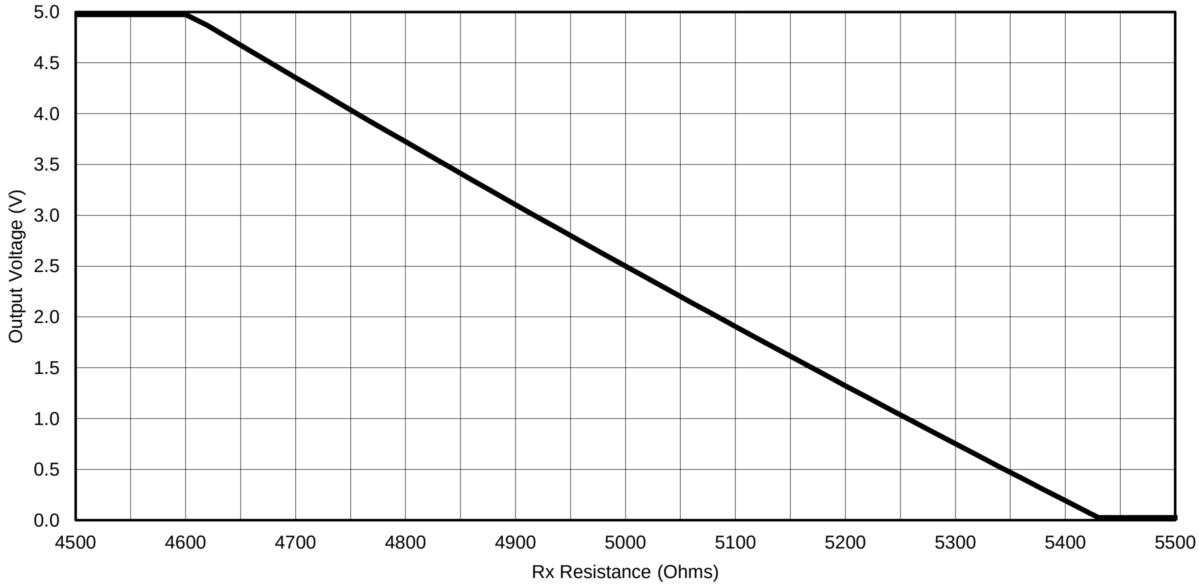


Figure 50. Output Voltage vs R_X

9 Power Supply Recommendations

For proper operation, the power supplies must be properly decoupled. For decoupling the supply lines, TI recommends that 10-nF capacitors be placed as close as possible to the operational amplifier power supply pins. For single-supply, place a capacitor between V+ and V− supply leads. For dual supplies, place one capacitor between V+ and ground, and one capacitor between V– and ground.

CAUTION

Supply voltages larger than 6 V can permanently damage the device.

The internal RFI filters shunt the received EMI energy to the supply pins. To maximize the effectiveness of the built-in EMI filters, the power supply pin bypassing should have a low impedance, low inductance path to RF ground.

The normally suggested 0.1-µF and larger capacitors tend to be inductive over the effective frequency range of the EMI filters and are not effective at filtering high frequencies (> 50 MHz). Capacitors with high self-resonance frequencies near the GHz range should be placed at the supply pins. This can be accomplished with small (0805 or less) 10 pF to 100 pF SMT ceramic capacitors placed directly at the supply pins to a solid RF ground. These capacitors will provide a direct AC path for the high-frequency EMI to ground. These capacitors are in addition to, and not a replacement for, the recommended low-frequency supply bypassing capacitors.

10 Layout

10.1 Layout Guidelines

- Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- For single-supply, place a capacitor between V^+ and V^-.
- For dual supplies, place one capacitor between V^+ and the board ground, and a second capacitor between ground and V^-.
- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and operational amplifier itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pick-up. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current. For more detailed information refer to *Circuit Board Layout Techniques*, SLOA089.
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.

Even with the LMV83x inherent hardening against EMI, TI still recommends to keep the input traces short and as far as possible from RF sources. Then the RF signals entering the chip are as low as possible, and the remaining EMI can be, almost, completely eliminated in the chip by the EMI reducing features of the LMV83x.

10.2 Layout Example

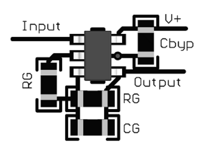


Figure 51. SOT-23 Noninverting Layout Example

11 デバイスおよびドキュメントのサポート

11.1 デバイス・サポート

11.1.1 開発サポート

LMV831 PSPICEモデル、SNOM049

LMV832 PSPICEモデル、SNOM050

LMV834 PSPICEモデル、SNOM038

TINA-TI SPICEベースのアナログ・シミュレーション・プログラム、http://www.ti.com/tool/tina-ti

TI Filterproソフトウェア、http://www.ti.com/tool/filterpro

DIPアダプタ評価モジュール、http://www.ti.com/tool/dip-adapter-evm

TIユニバーサル・オペアンプ評価モジュール、http://www.ti.com/tool/opampevm

11.2 ドキュメントのサポート

11.2.1 関連資料

関連資料については、以下を参照してください。

- *『AN-028 フィードバック・プロットによるオペアンプAC性能の定義』*、SBOA015
- *『基板のレイアウト技法』*、SLOA089
- *『絶縁抵抗を使用した容量性負荷駆動ソリューション』*、TIPD128
- *『オペアンプ・アプリケーション・ハンドブック』*、SBOA092
- *『堅牢な回路設計用のEMI強化されたオペアンプ』*、SNOA817
- *『AN-1698 EMI強化されたオペアンプの仕様』*、SNOA497
- *『AN-1867 LMV831/LMV832/LMV834用のEMIRR評価基板』*(これらの基板は既に供給されておらず、このドキュメントは参考のみのものです)、SNOA530

11.3 関連リンク

次の表に、クイック・アクセス・リンクを示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびサンプル注文またはご購入へのクイック・アクセスが含まれます。

表 2. 関連リンク

製品	プロダクト・フォルダ	サンプルとご購入	技術資料	ツールとソフトウェア	サポートとコミュニティ
LMV831	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
LMV832	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
LMV834	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

11.4 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™オンライン・コミュニティ ***TIのE2E（Engineer-to-Engineer）***コミュニティ。エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイディアを検討して、問題解決に役立てることができます。

設計サポート ***TIの設計サポート*** 役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

11.5 商標

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 静電気放電に関する注意事項

これらのデバイスは、限定的なESD（静電破壊）保護機能を内 蔵しています。保存時または取り扱い時は、MOSゲートに対す る静電破壊を防止するために、リード線同士をショートさせて おくか、デバイスを導電フォームに入れる必要があります。

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMV831MG/NOPB	ACTIVE	SC70	DCK	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	AFA	Samples
LMV831MGE/NOPB	ACTIVE	SC70	DCK	5	250	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	AFA	Samples
LMV831MGX/NOPB	ACTIVE	SC70	DCK	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	AFA	Samples
LMV832MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	AU5A	Samples
LMV832MME/NOPB	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	AU5A	Samples
LMV832MMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	AU5A	Samples
LMV834MT/NOPB	ACTIVE	TSSOP	PW	14	94	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LMV834 MT	Samples
LMV834MTX/NOPB	ACTIVE	TSSOP	PW	14	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LMV834 MT	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

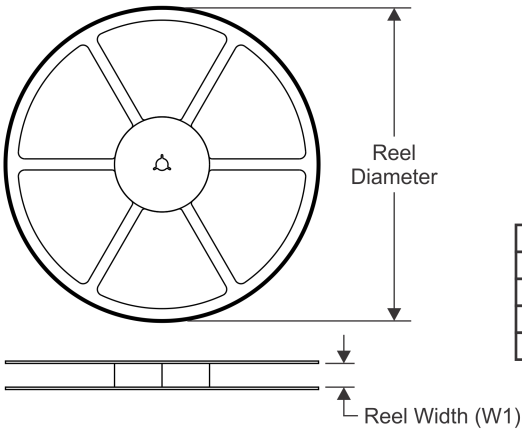
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

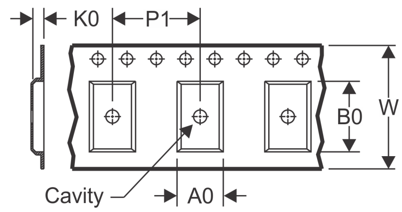
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

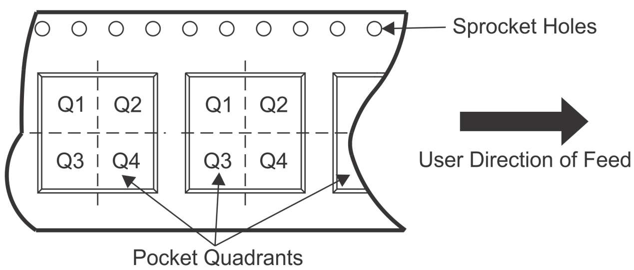


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

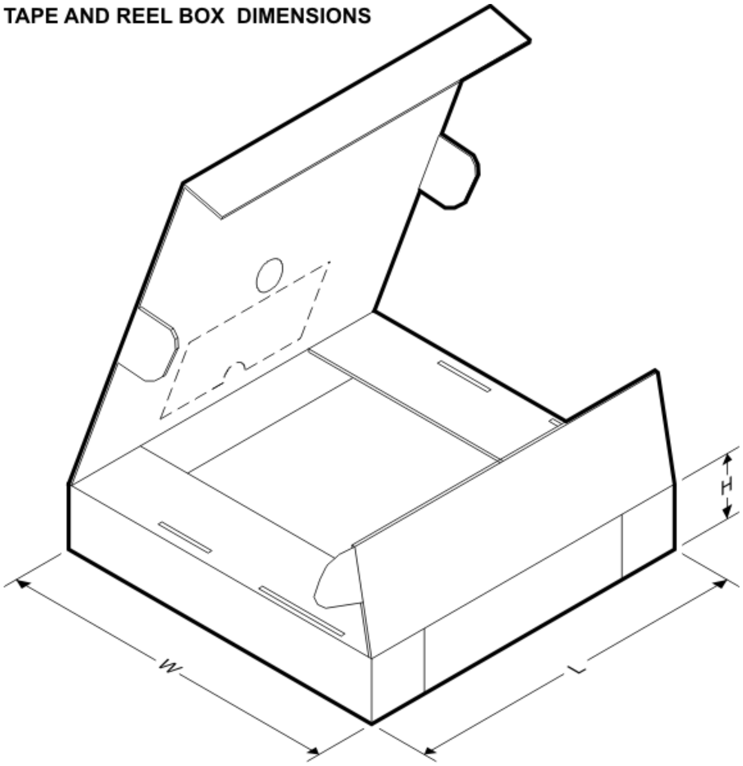
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV831MG/NOPB	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV831MGE/NOPB	SC70	DCK	5	250	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV831MGX/NOPB	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV832MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV832MME/NOPB	VSSOP	DGK	8	250	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV832MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV834MTX/NOPB	TSSOP	PW	14	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1

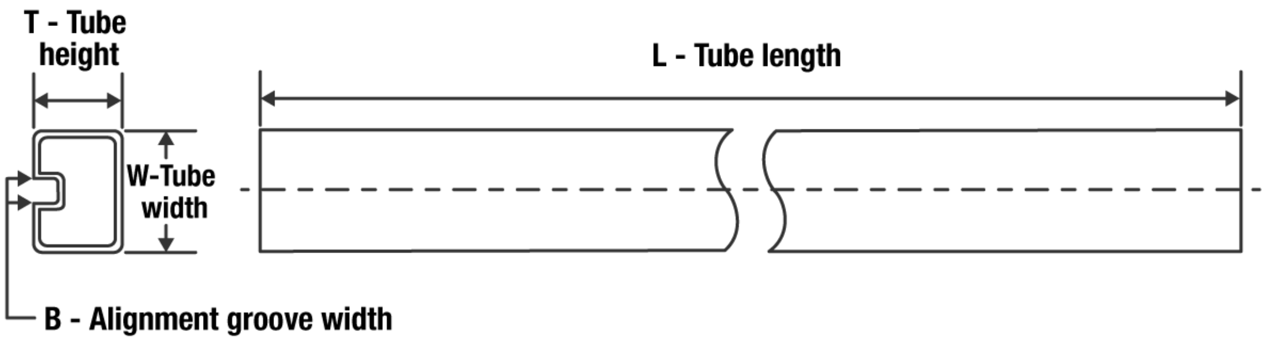
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

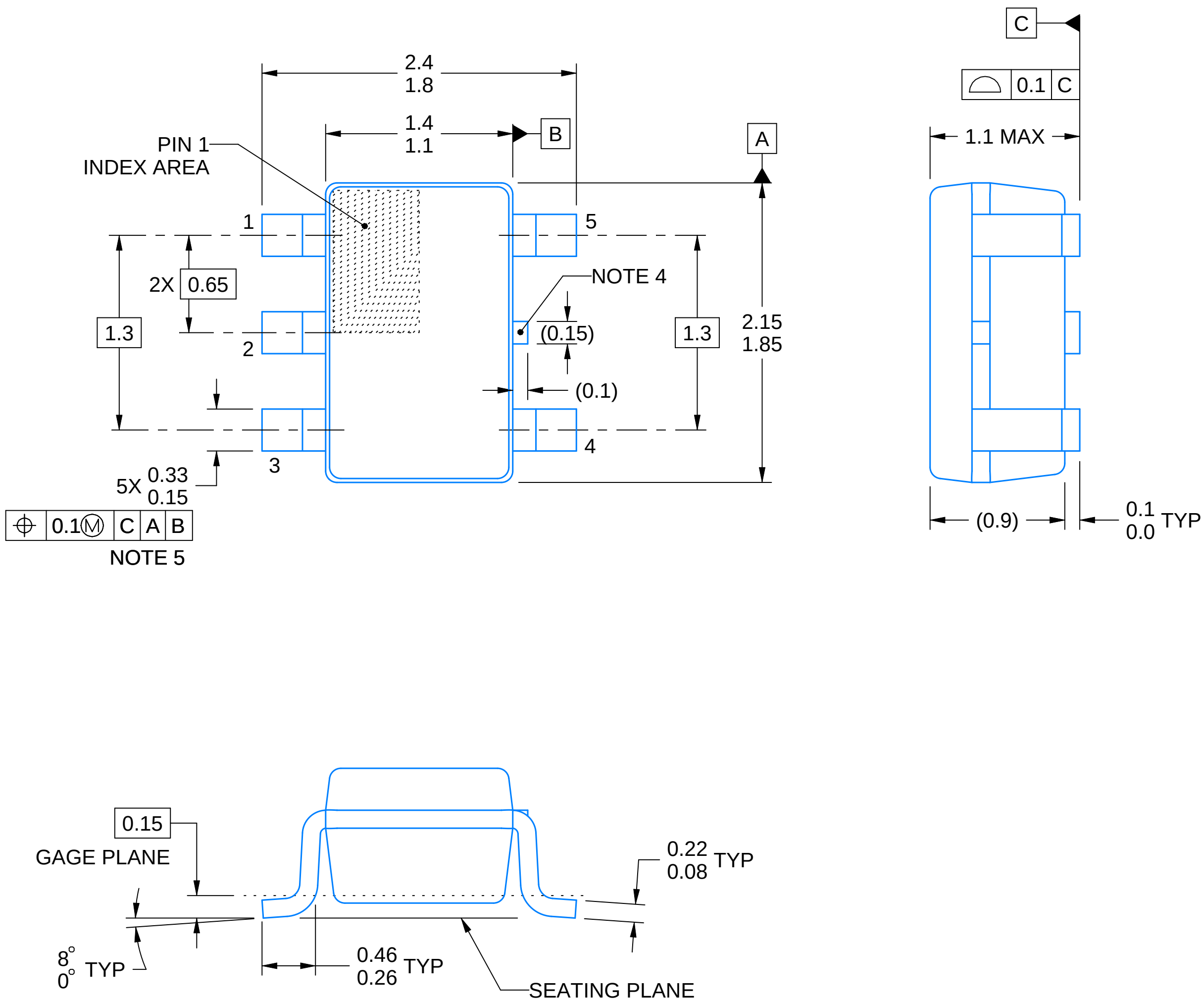
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV831MG/NOPB	SC70	DCK	5	1000	208.0	191.0	35.0
LMV831MGE/NOPB	SC70	DCK	5	250	208.0	191.0	35.0
LMV831MGX/NOPB	SC70	DCK	5	3000	208.0	191.0	35.0
LMV832MM/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LMV832MME/NOPB	VSSOP	DGK	8	250	208.0	191.0	35.0
LMV832MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LMV834MTX/NOPB	TSSOP	PW	14	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

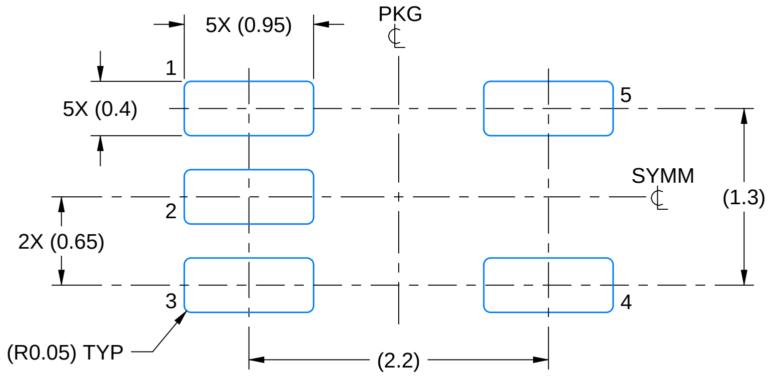
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LMV834MT/NOPB	PW	TSSOP	14	94	495	8	2514.6	4.06



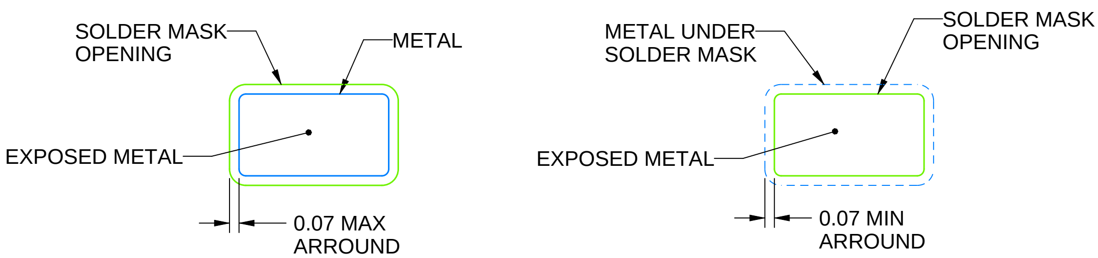
4214834/D 07/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



NON SOLDER MASK
DEFINED
(PREFERRED)

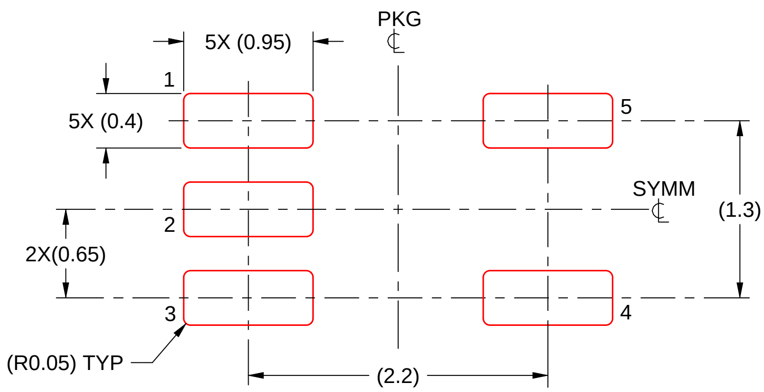
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214834/D 07/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



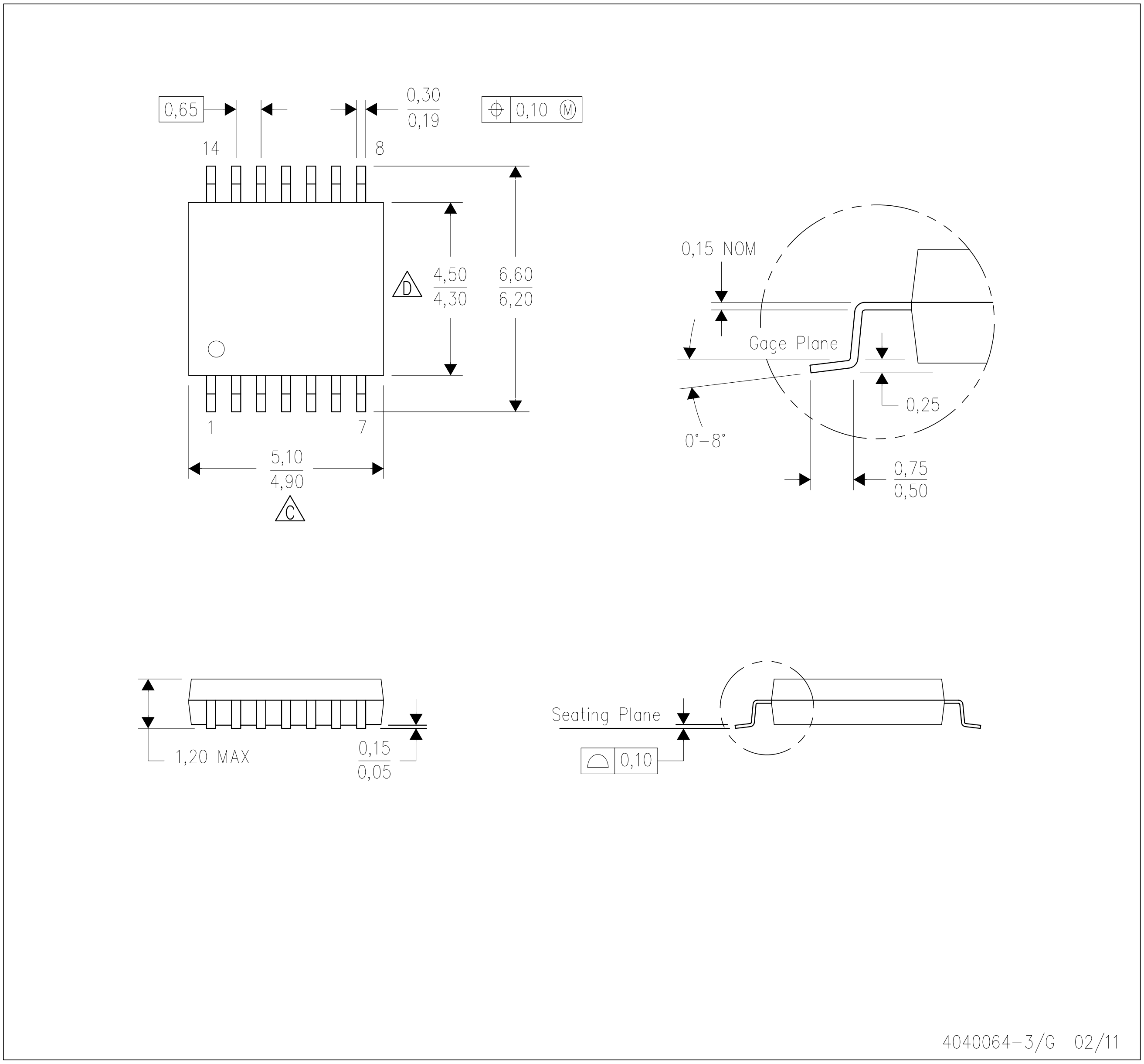
SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/D 07/2023

NOTES: (continued)

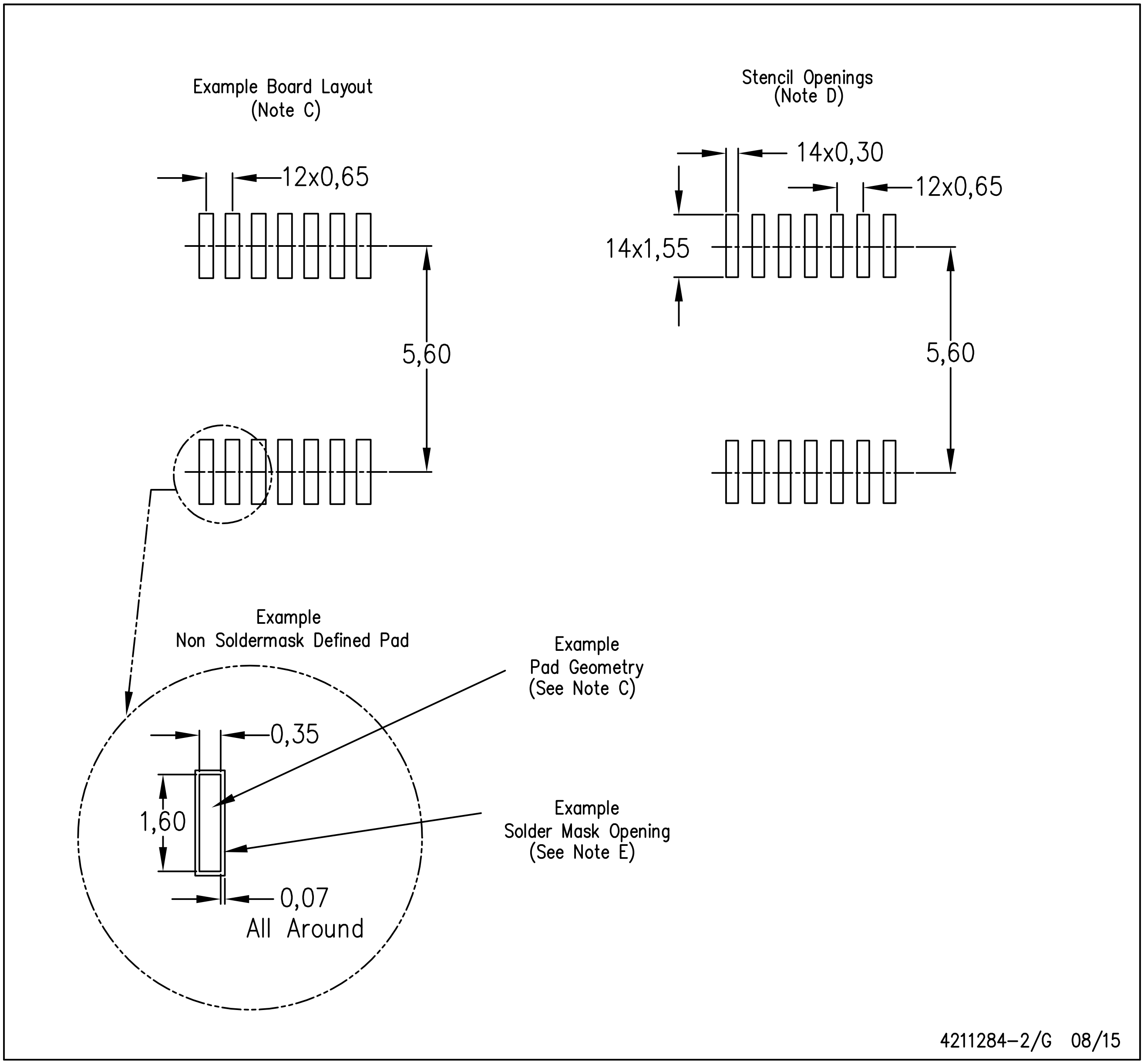
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE

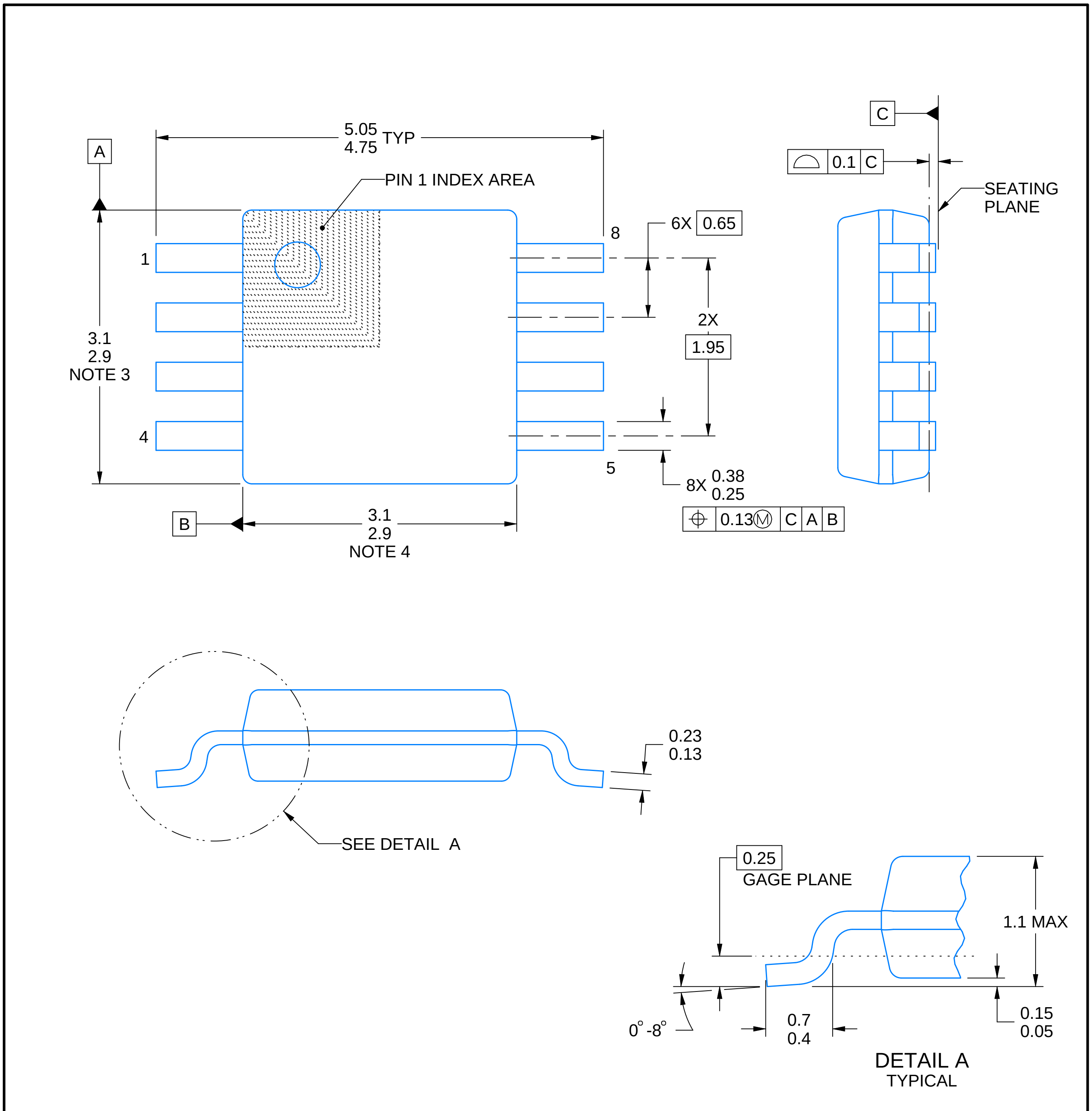


NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO–153

PW (R-PDSO-G14) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

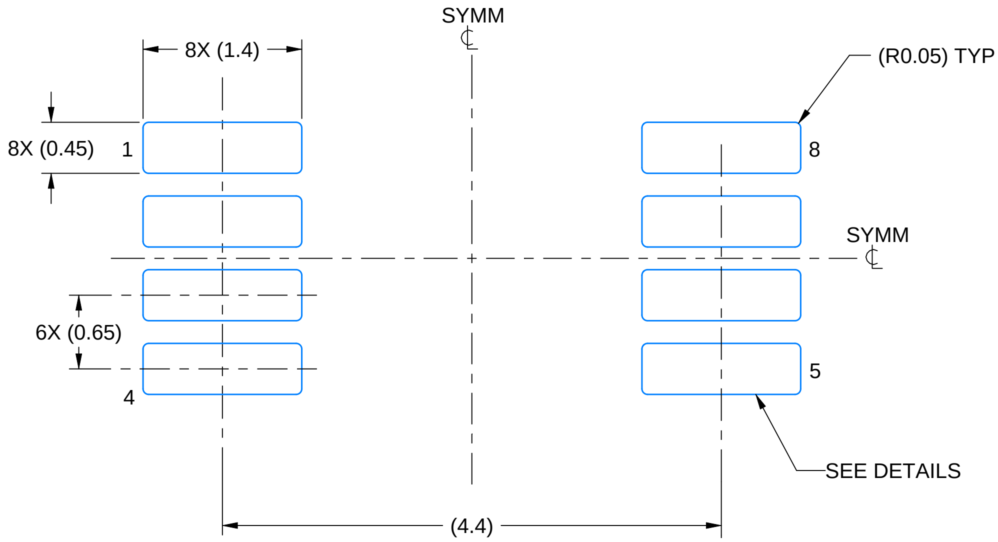


4214862/A 04/2023

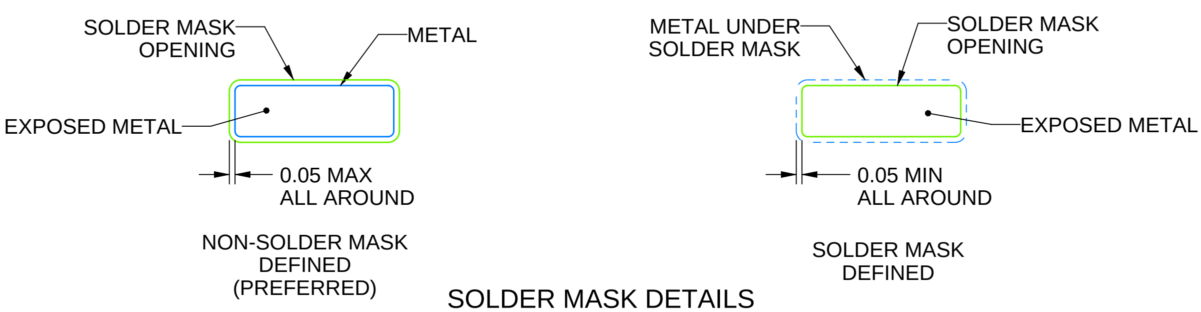
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

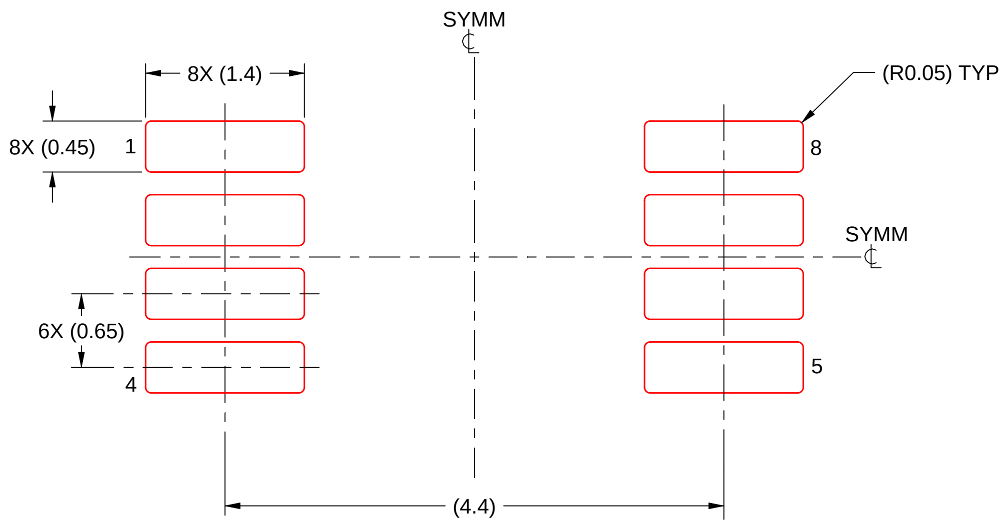


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス・デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、TI の販売条件、または ti.com やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、TI はそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265