LMV98x-N 小型、低消費電力、1.8V RRIOオペアンプ、シャットダウン機能付き

1 特長

- 1.8V、2.7V、5Vでの仕様を保証
- 出力スイング
  - 600Ω負荷: レールから80mV
  - 2kΩ負荷: レールから30mV
- レールを200mV超えるV_{CM}
- 消費電流(チャネルごとに): 100μA
- ゲイン帯域幅積: 1.4MHz
- 最大V_{OS}: 4mV
- 600Ω負荷でのゲイン: 101dB
- 超小型のパッケージ: DSBGA 1.0mm×1.5mm
- シャットダウンからのターンオン時間: 19μs
- デュアルでの独立したシャットダウン
- 温度範囲: -40℃～125℃

2 アプリケーション

- 産業用および車載用
- 消費者向け通信機器
- フィットネス用トラッカー
- ウェアラブル
- 携帯電話/スマートフォン
- ポータブル・オーディオ
- 携帯用およびバッテリ駆動の電子機器
- 消費電流の監視
- バッテリ監視

3 概要

LMV98x-Nは低電圧、低消費電力のオペアンプです。LMV98x-Nは1.8V～5Vの電源電圧で動作し、入力と出力がレール・ツー・レールです。LMV98x-Nの入力同相モード電圧範囲は電源を200mV超えるため、電源電圧の範囲を超えるユーザー拡張機能が可能になります。出力は無負荷でレール・ツー・レールのスイングが可能であり、1.8V電源で600Ω負荷のとき、レールから105mV以内です。LMV98x-Nは1.8Vでの動作に最適化されているため、2つのボタン電池や単一セルのリチウムイオン・バッテリを使用するバッテリ駆動システムに理想的です。

LMV98x-Nにはシャットダウン・ピンがあり、デバイスをディセーブルして消費電流を減らすために使用できます。$\overline{SHDN}$ピンがLOWのとき、デバイスはシャットダウン中です。シャットダウン時は出力が高インピーダンスになります。

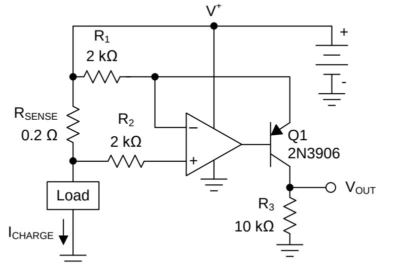
LMV98x-Nは速度/電力比が非常に優れており、1.8Vの電源電圧と小さな消費電流で、1.4MHzのゲイン帯域幅積を実現しています。LMV98x-Nは、600Ωの負荷と1000pFまでの容量性負荷を、最小のリンギングで駆動できます。LMV98x-NはDCゲインが101dBと高いため、低周波数のアプリケーションに適しています。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
LMV981-N	DSBGA (6)	1.50mm×1.30mm
	SC70 (6)	2.00mm×1.25mm
	SOT-23 (6)	2.90mm×1.60mm
LMV982-N	VSSOP (10)	3.00mm×3.00mm

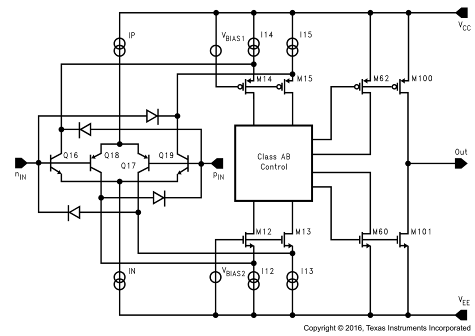
(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

代表的なアプリケーション



$$V_{OUT} = \frac{R_{SENSE} \times R_3}{R_1} \times I_{CHARGE} = 1\Omega \times I_{CHARGE}$$

概略回路図



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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision L (March 2013) から **Revision M** に変更 — **Page**

- 「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクション 追加 ... 1
- Changed $R_{\theta JA}$ values for LMV981-N: YZR (DSBGA) From: 286 To: 138.2 ... 5
- Changed $R_{\theta JA}$ values for LMV981-N: DCK (SC70) From: 286 To: 229.1 ... 5
- Changed $R_{\theta JA}$ values for LMV981-N: DBV (SOT-23) From: 286 To: 209.9 ... 5
- Changed $R_{\theta JA}$ values for LMV982-N: DGS (VSSOP) From: 286 To: 182.8 ... 5

Revision K (March 2013) から **Revision L** に変更 — **Page**

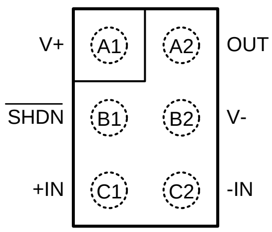
- ナショナル・セミコンダクターのデータシートのレイアウトをTIフォーマットへ 変更 ... 1

5 Description (continued)

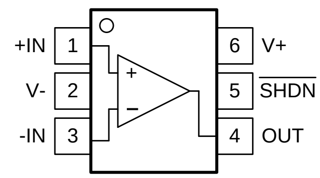
LMV981-N is offered in space-saving, 6-pin DSBGA, SC70, and SOT-23 packages. The 6-pin DSBGA package has only a 1.006 mm × 1.514 mm × 0.945 mm footprint. LMV982-N is offered in a space-saving, 10-pin VSSOP package. These small packages are ideal solutions for area constrained PCBs and portable electronics such as cellular phones and PDAs.

6 Pin Configuration and Functions

YZR Package
6-Pin DSBGA
Top View



DCK or DBV Package
6-Pin SC70 or SOT-23
Top View

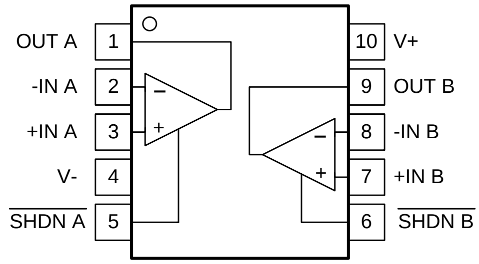


Pin Functions: LMV981-N

PIN			TYPE[1]	DESCRIPTION
NAME	DSBGA	SC70, SOT-23		
+IN	C1	1	I	Noninverting input
–IN	C2	3	I	Inverting input
OUT	A2	4	O	Output
SHDN	B1	5	I	Shutdown input
V+	A1	6	P	Positive (highest) power supply
V–	B2	2	P	Negative (lowest) power supply

(1) I = Input, O = Output, P = Power

DGS Package
10-Pin VSSOP
Top View



Pin Functions: LMV982-N

PIN		TYPE[1]	DESCRIPTION
NAME	VSSOP		
+IN A	3	I	Noninverting input, channel A
+IN B	7	I	Noninverting input, channel B
–IN A	2	I	Inverting input, channel A
–IN B	8	I	Inverting input, channel B
OUT A	1	O	Output, channel A
OUT B	9	O	Output, channel B
$\overline{\text{SHDN A}}$	5	I	Shutdown input, channel A
$\overline{\text{SHDN B}}$	6	I	Shutdown input, channel B
V+	10	P	Positive (highest) power supply
V–	4	P	Negative (lowest) power supply

(1) I = Input, O = Output, P = Power

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

	MIN	MAX	UNIT
Supply voltage ($V^+ – V^-$)		5.5	V
Differential input voltage	±Supply voltage		
Voltage at input/output pins	V^++ 0.3	V^- - 0.3	V
Junction temperature(3)		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) For soldering specifications, see TI application report, *Absolute Maximum Ratings for Soldering* (SNOA549).
(3) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)}–T_A)/R_{\theta JA}$. All numbers apply for packages soldered directly into a PCB.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Machine model(2)	±200	

(1) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC)

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply voltage	1.8	5	V
Temperature	–40	125	°C

7.4 Thermal Information

THERMAL METRIC(1)		LMV981-N			LMV982-N	UNIT
		YZR (DSBGA)	DCK (SC70)	DBV (SOT-23)	DGS (VSSOP)	
		6 PINS	6 PINS	6 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	138.2	229.1	209.9	182.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	1.2	116.1	181.2	73.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	23.4	53.3	53.2	103.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	5	8.8	55.5	12.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	23.2	52.7	52.6	101.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics – DC, 1.8 V

T_J = 25°C, V^+ = 1.8 V, V^- = 0 V, V_{CM} = V^+/2, V_O = V^+/2, R_L > 1 MΩ, and $\overline{SHDN}$ tied to V^+ (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS			MIN(2)	TYP(3)	MAX(2)	UNIT
V_{OS}	Input offset voltage	LMV981-N (single)		T_J = 25°C		1	4	mV
				T_J = –40°C to 125°C			6	
		LMV982-N (dual)		T_J = 25°C		1	5.5	
				T_J = –40°C to 125°C			7.5	
TCV_{OS}	Input offset voltage average drift					5.5		µV/°C
I_B	Input bias current	T_J = 25°C				15	35	nA
		T_J = –40°C to 125°C					50	
I_{OS}	Input offset current	T_J = 25°C				13	25	nA
		T_J = –40°C to 125°C					40	
I_S	Supply current (per channel)	T_J = 25°C				103	185	µA
		T_J = –40°C to 125°C					205	
		In shutdown	LMV981-N (single)	T_J = 25°C		0.156	1	
				T_J = –40°C to 125°C			2	
			LMV982-N (dual)	T_J = 25°C		0.178	3.5	
				T_J = –40°C to 125°C			5	
CMRR	Common mode rejection ratio	LMV981-N, 0 V ≤ V_{CM} ≤ 0.6 V, 1.4 V ≤ V_{CM} ≤ 1.8 V(4)		T_J = 25°C	60	78		dB
				T_J = –40°C to 125°C	55			
		LMV982, 0 V ≤ V_{CM} ≤ 0.6 V, 1.4 V ≤ V_{CM} ≤ 1.8 V(4)		T_J = 25°C	55	76		
				T_J = –40°C to 125°C	50			
		–0.2 V ≤ V_{CM} ≤ 0 V, 1.8 V ≤ V_{CM} ≤ 2 V			50	72		
PSRR	Power supply rejection ratio	1.8 V ≤ V^+ ≤ 5 V		T_J = 25°C	75	100		dB
				T_J = –40°C to 125°C	70			
CMVR	Input common-mode voltage	For CMRR range ≥ 50 dB		T_A = 25°C	V^- − 0.2	–0.2		V
						2.1	V^+ + 0.2	
				T_A = –40°C to 85°C	V^-		V^+	
				T_A = 125°C	V^- + 0.2		V^+ − 0.2	
A_V	Large signal voltage gain LMV981-N (single)	R_L = 600 Ω to 0.9 V, V_O = 0.2 V to 1.6 V, V_{CM} = 0.5 V		T_J = 25°C	77	101		dB
				T_J = –40°C to 125°C	73			
		R_L = 2 kΩ to 0.9 V, V_O = 0.2 V to 1.6 V, V_{CM} = 0.5 V		T_J = 25°C	80	105		
				T_J = –40°C to 125°C	75			
	Large signal voltage gain LMV982-N (dual)	R_L = 600 Ω to 0.9 V, V_O = 0.2 V to 1.6 V, V_{CM} = 0.5 V		T_J = 25°C	75	90		dB
				T_J = –40°C to 125°C	72			
		R_L = 2 kΩ to 0.9 V, V_O = 0.2 V to 1.6 V, V_{CM} = 0.5 V		T_J = 25°C	78	100		
				T_J = –40°C to 125°C	75			

(1) Electrical characteristics table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in limited self-heating of the device such that T_J = T_A. No ensured specification of parametric performance is indicated in the electrical tables under conditions of internal self heating where T_J > T_A. *Absolute Maximum Ratings* indicated junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.
(2) All limits are specified by testing or statistical analysis.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(4) For ensured temperature ranges, see input common-mode voltage range specifications.

Electrical Characteristics – DC, 1.8 V (continued)

T_J = 25°C, V^+ = 1.8 V, V^- = 0 V, V_{CM} = V^+/2, V_O = V^+/2, R_L > 1 MΩ, and $\overline{SHDN}$ tied to V^+ (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		MIN(2)	TYP(3)	MAX(2)	UNIT
V_O	Output swing	R_L = 600 Ω to 0.9 V, V_{IN} = ±100 mV	T_J = 25°C	1.65	1.72		V
					0.077	0.105	
			T_J = –40°C to 125°C	1.63		0.12	
		R_L = 2 kΩ to 0.9 V, V_{IN} = ±100 mV	T_J = 25°C	1.75	1.77		
					0.024	0.035	
			T_J = –40°C to 125°C	1.74		0.04	
I_O	Output short circuit current(5)	Sourcing, V_O = 0 V, V_{IN} = 100 mV	T_J = 25°C	4	8		mA
			T_J = –40°C to 125°C	3.3			
		Sinking, V_O = 1.8 V, V_{IN} = –100 mV	T_J = 25°C	7	9		
			T_J = –40°C to 125°C	5			
Ton	Turnon time from shutdown				19		µs
V_{SHDN}	Turnon voltage to enable part				1		V
	Turnoff voltage				0.55		

(5) Applies to both single-supply and split-supply operation. Continuous short-circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of 45 mA over long term may adversely affect reliability.

7.6 Electrical Characteristics – AC, 1.8 V

T_J = 25°C, V^+ = 1.8 V, V^- = 0 V, V_{CM} = V^+/2, V_O = V^+/2, R_L > 1 MΩ, and $\overline{SHDN}$ tied to V^+ (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN(2)	TYP(3)	MAX(2)	UNIT
SR	Slew rate(4)			0.35		V/µs
GBW	Gain-bandwidth product			1.4		MHz
Φ_m	Phase margin			67		°
G_m	Gain margin			7		dB
e_n	Input-referred voltage noise	f = 10 kHz, V_{CM} = 0.5 V		60		nV/√Hz
i_n	Input-referred current noise	f = 10 kHz		0.08		pA/√Hz
THD	Total harmonic distortion	f = 1 kHz, A_V = +1, R_L = 600 Ω, V_{IN} = 1 V_{PP}		0.023%		
	Amp-to-amp isolation(5)			123		dB

(1) Electrical characteristics table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in limited self-heating of the device such that T_J = T_A. No ensured specification of parametric performance is indicated in the electrical tables under conditions of internal self heating where T_J > T_A. *Absolute Maximum Ratings* indicated junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.
(2) All limits are specified by testing or statistical analysis.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(4) Connected as voltage follower with input step from V^- to V^+. Number specified is the slower of the positive and negative slew rates.
(5) Input referred, R_L = 100 kΩ connected to V^+/ 2. Each amp excited in turn with 1 kHz to produce V_O = 3 V_{PP} (for supply voltages < 3 V, V_O = V^+).

7.7 Electrical Characteristics – DC, 2.7 V

T_J = 25°C, V^+ = 2.7 V, V^- = 0 V, V_{CM} = V^+/2, V_O = V^+/2, R_L > 1 MΩ, and $\overline{SHDN}$ tied to V^+ (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS			MIN[2]	TYP[3]	MAX[2]	UNIT
V_{OS}	Input offset voltage	LMV981-N (single)		T_J = 25°C		1	4	mV
				T_J = –40°C to 125°C			6	
		LMV982-N (dual)		T_J = 25°C		1	6	mV
				T_J = –40°C to 125°C			7.5	
TCV_{OS}	Input offset voltage average drift					5.5		μV/°C
I_B	Input bias current	T_J = 25°C				15	35	nA
		T_J = –40°C to 125°C					50	
I_{OS}	Input offset current	T_J = 25°C				8	25	nA
		T_J = –40°C to 125°C					40	
I_S	Supply current (per channel)	T_J = 25°C				105	190	μA
		T_J = –40°C to 125°C					210	
		In shutdown	LMV981-N (single)	T_J = 25°C		0.061	1	
				T_J = –40°C to 125°C			2	
			LMV982-N (dual)	T_J = 25°C		0.101	3.5	
				T_J = –40°C to 125°C			5	
CMRR	Common mode rejection ratio	LMV981-N, 0 V ≤ V_{CM} ≤ 1.5 V, 2.3 V ≤ V_{CM} ≤ 2.7 V[4]		T_J = 25°C	60	81		dB
				T_J = –40°C to 125°C	55			
		LMV982, 0 V ≤ V_{CM} ≤ 1.5 V, 2.3 V ≤ V_{CM} ≤ 2.7 V[4]		T_J = 25°C	55	80		
				T_J = –40°C to 125°C	50			
		−0.2 V ≤ V_{CM} ≤ 0 V, 2.7 V ≤ V_{CM} ≤ 2.9 V			50	74		
PSRR	Power supply rejection ratio	1.8 V ≤ V^+ ≤ 5 V, V_{CM} = 0.5 V		T_J = 25°C	75	100		dB
				T_J = –40°C to 125°C	70			
CMVR	Input common mode voltage	For CMRR Range ≥ 50 dB		T_A = 25°C	V^- − 0.2	–0.2		V
						3	V^+ + 0.2	
				T_A = −40°C to 85°C	V^-		V^+	
				T_A = 125°C	V^- + 0.2		V^+ − 0.2	
A_V	Large signal voltage gain LMV981-N (single)	R_L = 600 Ω to 1.35 V, V_O = 0.2 V to 2.5 V		T_J = 25°C	87	104		dB
				T_J = –40°C to 125°C	86			
		R_L = 2 kΩ to 1.35 V, V_O = 0.2 V to 2.5 V		T_J = 25°C	92	110		
				T_J = –40°C to 125°C	91			
	Large signal voltage gain LMV982-N (dual)	R_L = 600 Ω to 1.35 V, V_O = 0.2 V to 2.5 V		T_J = 25°C	78	90		
				T_J = –40°C to 125°C	75			
		R_L = 2 kΩ to 1.35 V, V_O = 0.2 V to 2.5 V		T_J = 25°C	81	100		
				T_J = –40°C to 125°C	78			

(1) Electrical characteristics table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in limited self-heating of the device such that T_J = T_A. No ensured specification of parametric performance is indicated in the electrical tables under conditions of internal self heating where T_J > T_A. *Absolute Maximum Ratings* indicated junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.
(2) All limits are specified by testing or statistical analysis.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(4) For ensured temperature ranges, see input common mode voltage range specifications.

Electrical Characteristics – DC, 2.7 V (continued)

T_J = 25°C, V^+ = 2.7 V, V^- = 0 V, V_{CM} = V^+/2, V_O = V^+/2, R_L > 1 MΩ, and $\overline{SHDN}$ tied to V^+ (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		MIN(2)	TYP(3)	MAX(2)	UNIT
V_O	Output swing	R_L = 600 Ω to 1.35 V, V_{IN} = ±100 mV	T_J = 25°C	2.55	2.62		V
					0.083	0.11	
			T_J = –40°C to 125°C	2.53		0.13	
		R_L = 2 kΩ to 1.35 V, V_{IN} = ±100 mV	T_J = 25°C	2.65	2.675		
					0.025	0.04	
			T_J = –40°C to 125°C	2.64		0.045	
I_O	Output short circuit current(5)	Sourcing, V_O = 0 V, V_{IN} = 100 mV	T_J = 25°C	20	30		mA
			T_J = –40°C to 125°C	15			
		Sinking, V_O = 0 V, V_{IN} = –100 mV	T_J = 25°C	18	25		
			T_J = –40°C to 125°C	12			
Ton	Turnon time from shutdown				12.5		µs
V_{SHDN}	Turnon voltage to enable part				1.9		V
	Turnoff voltage				0.8		

(5) Applies to both single-supply and split-supply operation. Continuous short-circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of 45 mA over long term may adversely affect reliability.

7.8 Electrical Characteristics – AC, 2.7 V

T_J = 25°C, V^+ = 2.7 V, V^- = 0 V, V_{CM} = 1 V, V_O = 1.35 V, R_L > 1 MΩ, and $\overline{SHDN}$ tied to V^+ (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN(2)	TYP(3)	MAX(2)	UNIT
SR	Slew rate(4)			0.4		V/µs
GBW	Gain-bandwidth product			1.4		MHz
Φ_m	Phase margin			70		°
G_m	Gain margin			7.5		dB
e_n	Input-referred voltage noise	f = 10 kHz, V_{CM} = 0.5 V		57		nV/√Hz
i_n	Input-referred current noise	f = 10 kHz		0.08		pA/√Hz
THD	Total harmonic distortion	f = 1 kHz, A_V = +1, R_L = 600 Ω, V_{IN} = 1 V_{PP}		0.022%		
	Amp-to-amp isolation(5)			123		dB

(1) Electrical characteristics table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in limited self-heating of the device such that T_J = T_A. No ensured specification of parametric performance is indicated in the electrical tables under conditions of internal self heating where T_J > T_A. *Absolute Maximum Ratings* indicated junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.
(2) All limits are specified by testing or statistical analysis.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(4) Connected as voltage follower with input step from V^- to V^+. Number specified is the slower of the positive and negative slew rates.
(5) Input referred, R_L = 100 kΩ connected to V^+/2. Each amp excited in turn with 1 kHz to produce V_O = 3 V_{PP} (for supply voltages < 3 V, V_O = V^+).

7.9 Electrical Characteristics – DC, 5 V

T_J = 25°C, V^+ = 5 V, V^- = 0 V, V_{CM} = V^+/2, V_O = V^+/2, R_L > 1 MΩ, and $\overline{SHDN}$ tied to V^+ (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS		MIN[2]	TYP[3]	MAX[2]	UNIT
V_{OS}	Input offset voltage	LMV981-N (single)	T_J = 25°C		1	4	mV
			T_J = –40°C to 125°C			6	
		LMV982-N (dual)	T_J = 25°C		1	5.5	
			T_J = –40°C to 125°C			7.5	
TCV_{OS}	Input offset voltage average drift				5.5		µV/°C
I_B	Input bias current	T_J = 25°C			14	35	nA
		T_J = –40°C to 125°C				50	
I_{OS}	Input offset current	T_J = 25°C			9	25	nA
		T_J = –40°C to 125°C				40	
I_S	Supply current (per channel)	T_J = 25°C			116	210	µA
		T_J = –40°C to 125°C				230	
		In shutdown, LMV981-N (single)	T_J = 25°C		0.201	1	µA
			T_J = –40°C to 125°C			2	
		In shutdown, LMV982-N (dual)	T_J = 25°C		0.302	3.5	
			T_J = –40°C to 125°C			5	
CMRR	Common mode rejection ratio[4]	0 V ≤ V_{CM} ≤ 3.8 V, 4.6 V ≤ V_{CM} ≤ 5 V	T_J = 25°C	60	86		dB
			T_J = –40°C to 125°C	55			
		−0.2 V ≤ V_{CM} ≤ 0 V, 5 V ≤ V_{CM} ≤ 5.2 V		50	78		
PSRR	Power supply rejection ratio	1.8 V ≤ V^+ ≤ 5 V, V_{CM} = 0.5 V	T_J = 25°C	75	100		dB
			T_J = –40°C to 125°C	70			
CMVR	Input common mode voltage	For CMRR range ≥ 50 dB	T_A = 25°C	V^- − 0.2	–0.2		V
					5.3	V^+ + 0.2	
			T_A = −40°C to 85°C	V^-		V^+	
			T_A = 125°C	V^- + 0.3		V^+ − 0.3	
A_V	Large signal voltage gain LMV981-N (single)	R_L = 600 Ω to 2.5 V, V_O = 0.2 V to 4.8 V	T_J = 25°C	88	102		dB
			T_J = –40°C to 125°C	87			
		R_L = 2 kΩ to 2.5 V, V_O = 0.2 V to 4.8 V	T_J = 25°C	94	113		
			T_J = –40°C to 125°C	93			
	Large signal voltage gain LMV982-N (dual)	R_L = 600 Ω to 2.5 V, V_O = 0.2 V to 4.8 V	T_J = 25°C	81	90		dB
			T_J = –40°C to 125°C	78			
		R_L = 2 kΩ to 2.5 V, V_O = 0.2 V to 4.8 V	T_J = 25°C	85	100		
			T_J = –40°C to 125°C	82			
V_O	Output swing	R_L = 600 Ω to 2.5 V, V_{IN} = ±100 mV	T_J = 25°C	4.855	4.89		V
					0.12	0.16	
			T_J = –40°C to 125°C	4.835		0.18	
		R_L = 2 kΩ to 2.5 V, V_{IN} = ±100 mV	T_J = 25°C	4.945	4.967		
					0.037	0.065	
			T_J = –40°C to 125°C	4.935		0.075	

(1) Electrical characteristics table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in limited self-heating of the device such that T_J = T_A. No ensured specification of parametric performance is indicated in the electrical tables under conditions of internal self heating where T_J > T_A. *Absolute Maximum Ratings* indicated junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.
(2) All limits are specified by testing or statistical analysis.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(4) For ensured temperature ranges, see input common mode voltage range specifications.

Electrical Characteristics – DC, 5 V (continued)

T_J = 25°C, V^+ = 5 V, V^- = 0 V, V_{CM} = V^+/2, V_O = V^+/2, R_L > 1 MΩ, and $\overline{SHDN}$ tied to V^+ (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		MIN (2)	TYP (3)	MAX (2)	UNIT
I_O	Output short-circuit current (5)	LMV981-N, sourcing, V_O = 0 V, V_{IN} = 100 mV	T_J = 25°C	80	100		mA
			T_J = –40°C to 125°C	68			
		Sinking, V_O = 5 V, V_{IN} = −100 mV	T_J = 25°C	58	65		
			T_J = –40°C to 125°C	45			
Ton	Turnon time from shutdown				8.4		µs
V_{SHDN}	Turnon voltage to enable part				4.2		V
	Turnoff voltage				0.8		

(5) Applies to both single-supply and split-supply operation. Continuous short-circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of 45 mA over long term may adversely affect reliability.

7.10 Electrical Characteristics – AC, 5 V

T_J = 25°C, V^+ = 5 V, V^- = 0 V, V_{CM} = V^+/2, V_O = 2.5 V, R_L > 1 MΩ, and $\overline{SHDN}$ tied to V^+ (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN (2)	TYP (3)	MAX (2)	UNIT
SR	Slew rate (4)			0.42		V/µs
GBW	Gain-bandwidth product			1.5		MHz
Φ_m	Phase margin			71		°
G_m	Gain margin			8		dB
e_n	Input-referred voltage noise	f = 10 kHz, V_{CM} = 1 V		50		nV/√Hz
i_n	Input-referred current noise	f = 10 kHz		0.08		pA/√Hz
THD	Total harmonic distortion	f = 1 kHz, A_V = +1, R_L = 600 Ω, V_O = 1 V_{PP}		0.022%		
	Amp-to-amp isolation (5)			123		dB

(1) Electrical characteristics table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in limited self-heating of the device such that T_J = T_A. No ensured specification of parametric performance is indicated in the electrical tables under conditions of internal self heating where T_J > T_A. *Absolute Maximum Ratings* indicated junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.
(2) All limits are specified by testing or statistical analysis.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(4) Connected as voltage follower with input step from V^- to V^+. Number specified is the slower of the positive and negative slew rates.
(5) Input referred, R_L = 100 kΩ connected to V^+/2. Each amp excited in turn with 1 kHz to produce V_O = 3 V_{PP} (for supply voltages < 3 V, V_O = V^+).

7.11 Typical Characteristics

V_S = 5 V, single supply, and T_A = 25°C (unless otherwise noted)

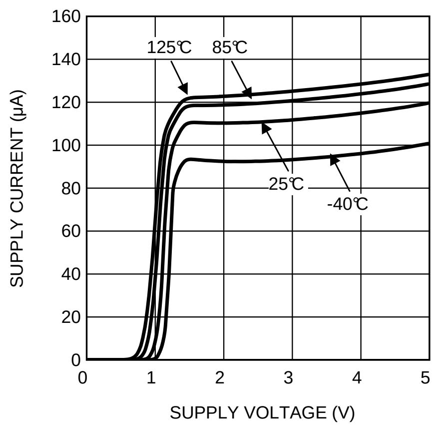


Figure 1. Supply Current vs Supply Voltage (LMV981-N)

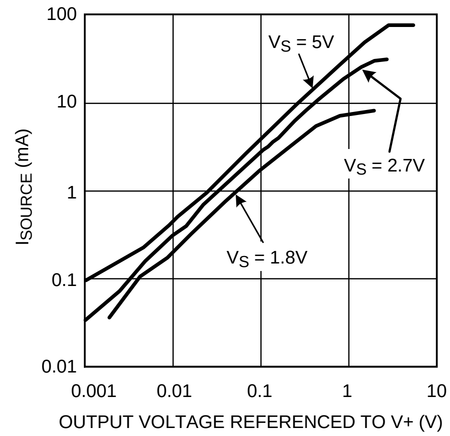


Figure 2. Sourcing Current vs Output Voltage

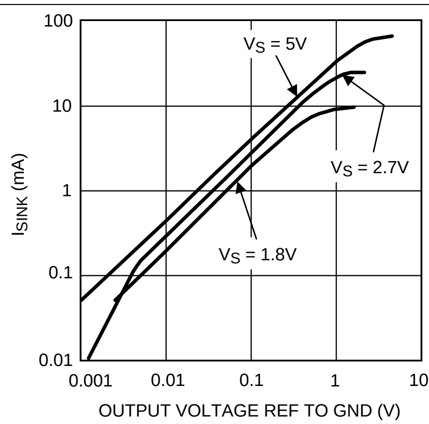


Figure 3. Sinking Current vs Output Voltage

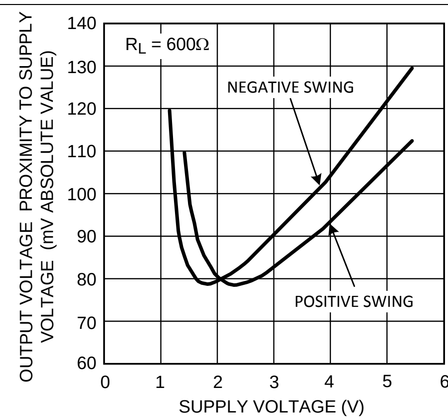


Figure 4. Output Voltage Swing vs Supply Voltage

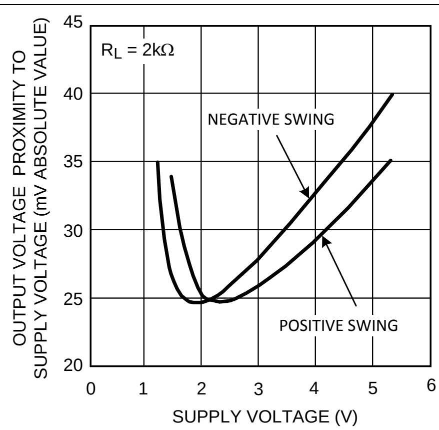


Figure 5. Output Voltage Swing vs Supply Voltage

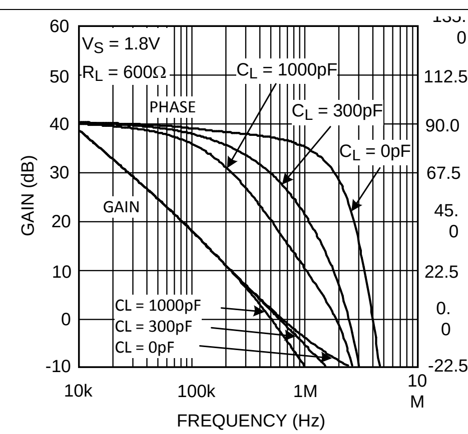


Figure 6. Gain and Phase vs Frequency

Typical Characteristics (continued)

V_S = 5 V, single supply, and T_A = 25°C (unless otherwise noted)

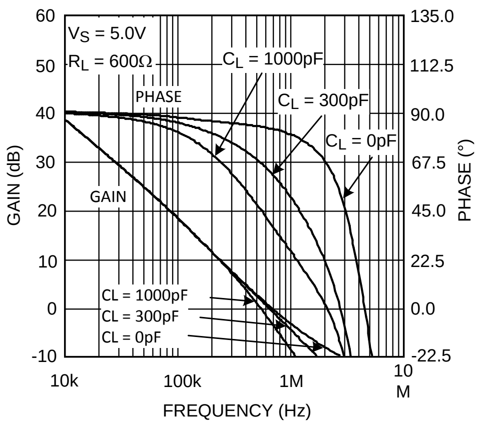


Figure 7. Gain and Phase vs Frequency

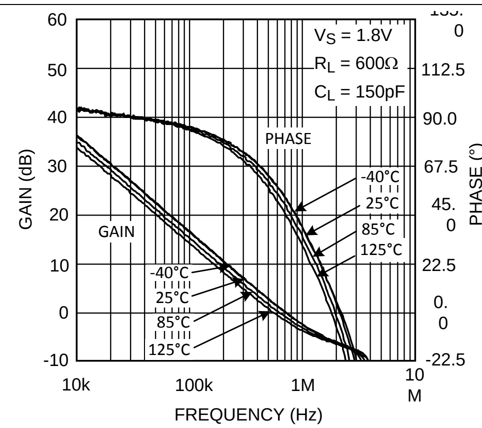


Figure 8. Gain and Phase vs Frequency

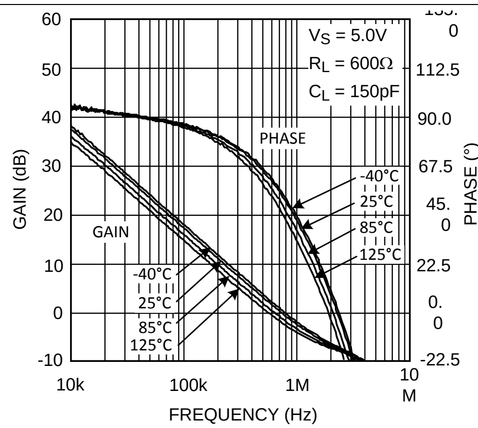


Figure 9. Gain and Phase vs Frequency

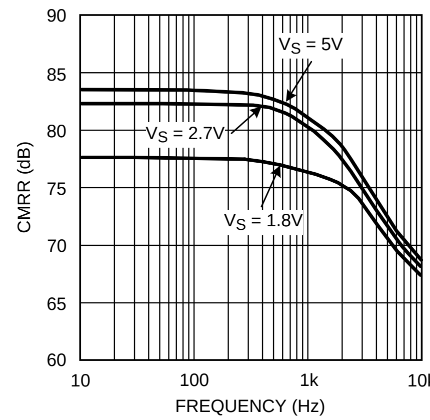


Figure 10. CMRR vs Frequency

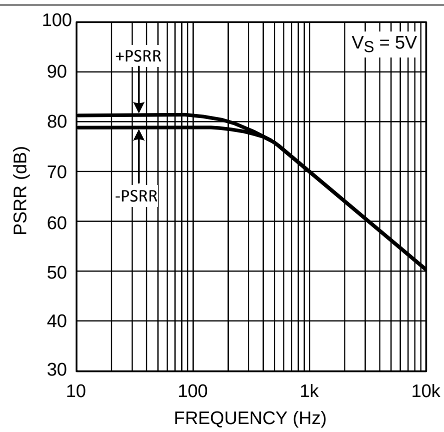


Figure 11. PSRR vs Frequency

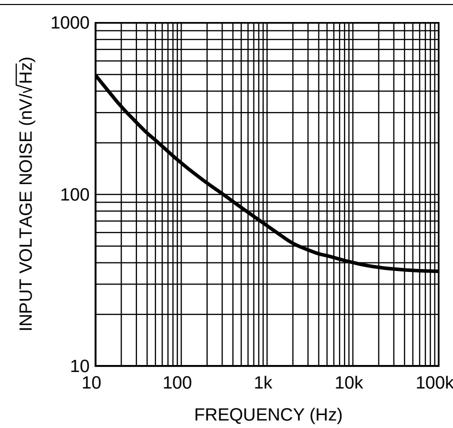


Figure 12. Input Voltage Noise vs Frequency

Typical Characteristics (continued)

V_S = 5 V, single supply, and T_A = 25°C (unless otherwise noted)

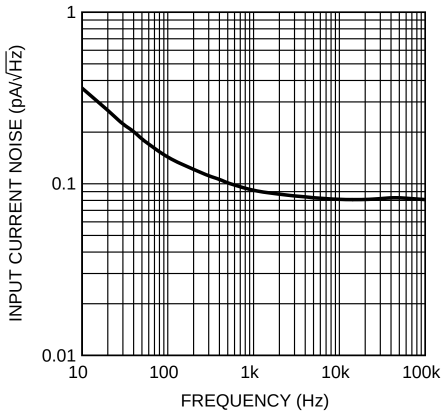


Figure 13. Input Current Noise vs Frequency

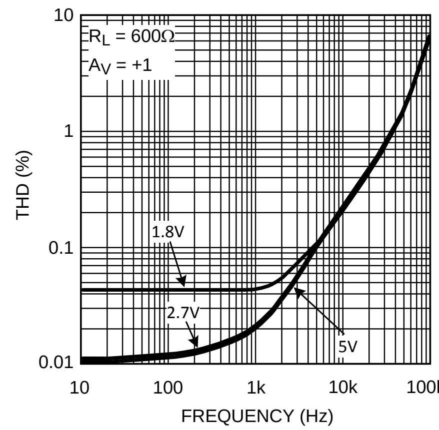


Figure 14. THD vs Frequency

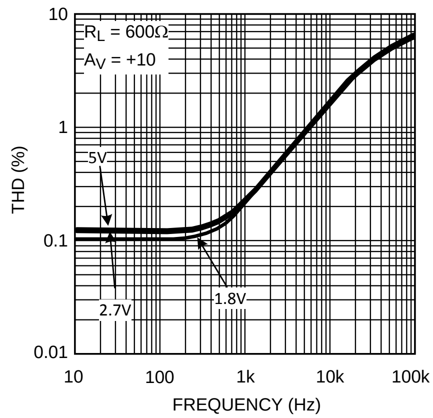


Figure 15. THD vs Frequency

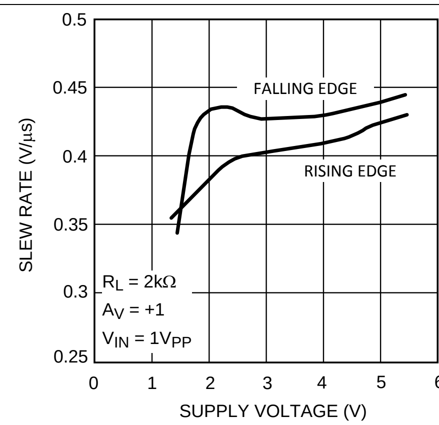


Figure 16. Slew Rate vs Supply Voltage

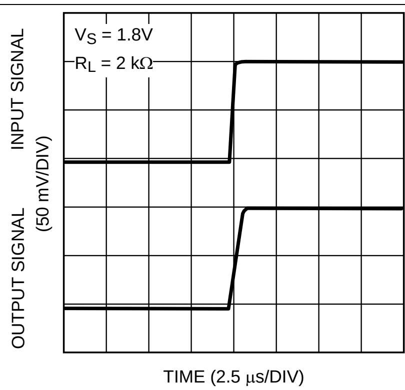


Figure 17. Small-Signal Noninverting Response

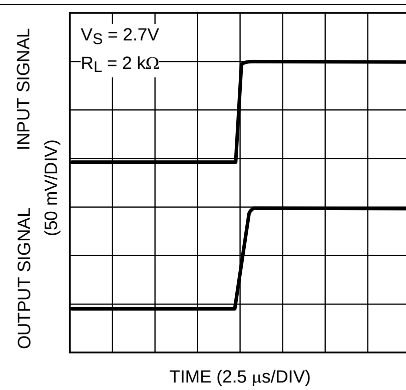


Figure 18. Small-Signal Noninverting Response

Typical Characteristics (continued)

V_S = 5 V, single supply, and T_A = 25°C (unless otherwise noted)

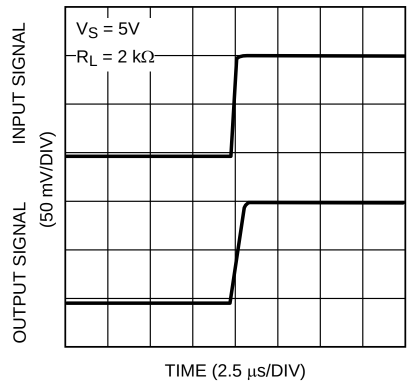


Figure 19. Small-Signal Noninverting Response

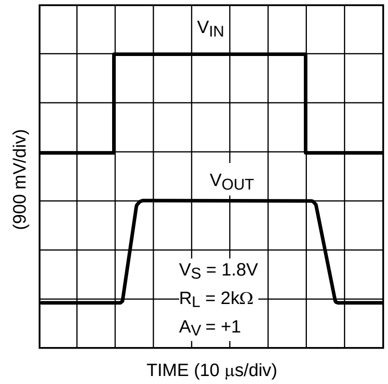


Figure 20. Large-Signal Noninverting Response

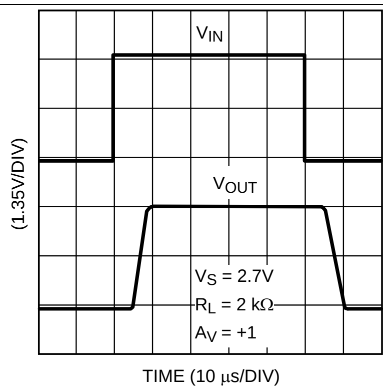


Figure 21. Large-Signal Noninverting Response

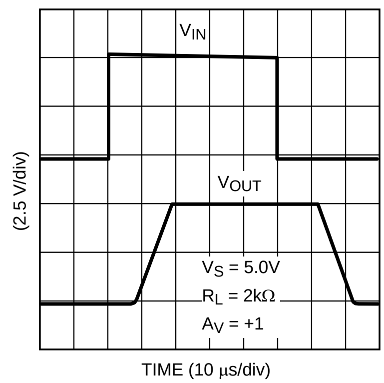


Figure 22. Large-Signal Noninverting Response

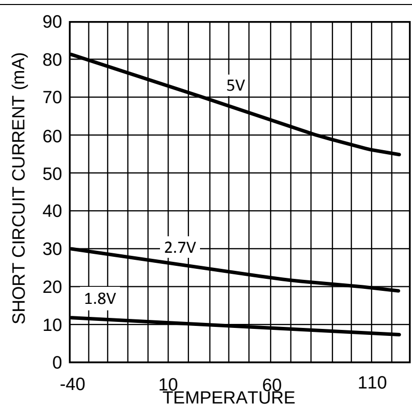


Figure 23. Short-Circuit Current vs Temperature (Sinking)

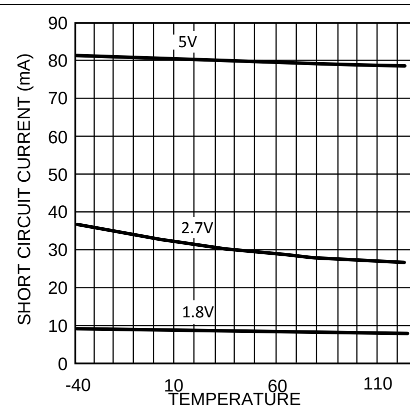


Figure 24. Short-Circuit Current vs Temperature (Sourcing)

Typical Characteristics (continued)

V_S = 5 V, single supply, and T_A = 25°C (unless otherwise noted)

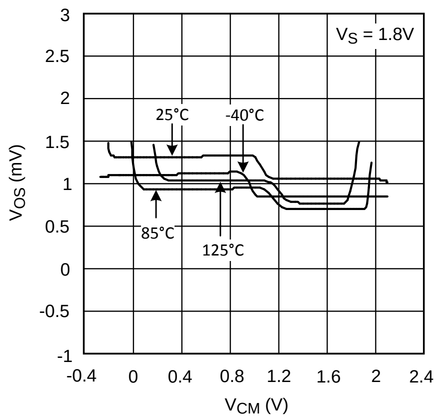


Figure 25. Offset Voltage vs Common Mode Range

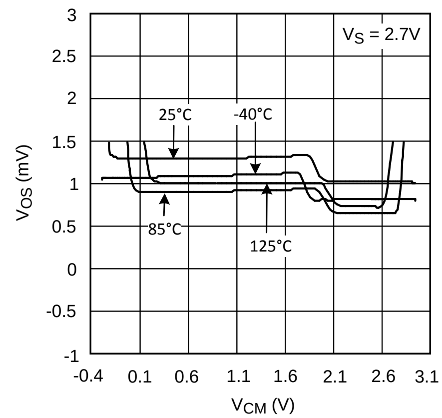


Figure 26. Offset Voltage vs Common Mode Range

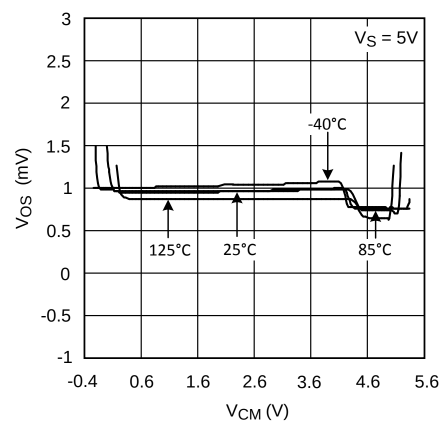


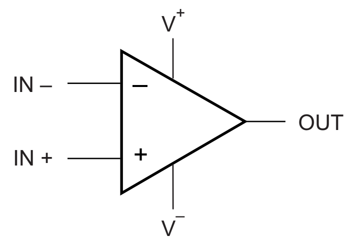
Figure 27. Offset Voltage vs Common Mode Range

8 Detailed Description

8.1 Overview

The LMV98x-N are low-voltage, low-power operational amplifiers (op-amp) operating from 1.8-V to 5.5-V supply voltages and have rail-to-rail input and output with shutdown. LMV98x-N input common-mode voltage extends 200 mV beyond the supplies which enables user enhanced functionality beyond the supply voltage range.

8.2 Functional Block Diagram



(each amplifier)

8.3 Feature Description

The differential inputs of the amplifier consist of a noninverting input (+IN) and an inverting input (–IN). The amplifer amplifies only the difference in voltage between the two inputs, which is called the differential input voltage. The output voltage of the op-amp V_{OUT} is given by Equation 1:

$$V_{OUT} = A_{OL} (IN^+ - IN^-)$$

where

- A_{OL} is the open-loop gain of the amplifier, typically around 100 dB (100,000x, or 10 µV per volt). (1)

8.4 Device Functional Modes

8.4.1 Input and Output Stage

The rail-to-rail input stage of this family provides more flexibility for the designer. The LMV98x-N use a complimentary PNP and NPN input stage in which the PNP stage senses common-mode voltage near V^- and the NPN stage senses common-mode voltage near V^+. The transition from the PNP stage to NPN stage occurs 1 V below V^+. Because both input stages have their own offset voltage, the offset of the amplifier becomes a function of the input common-mode voltage and has a crossover point at 1 V below V^+.

Device Functional Modes (continued)

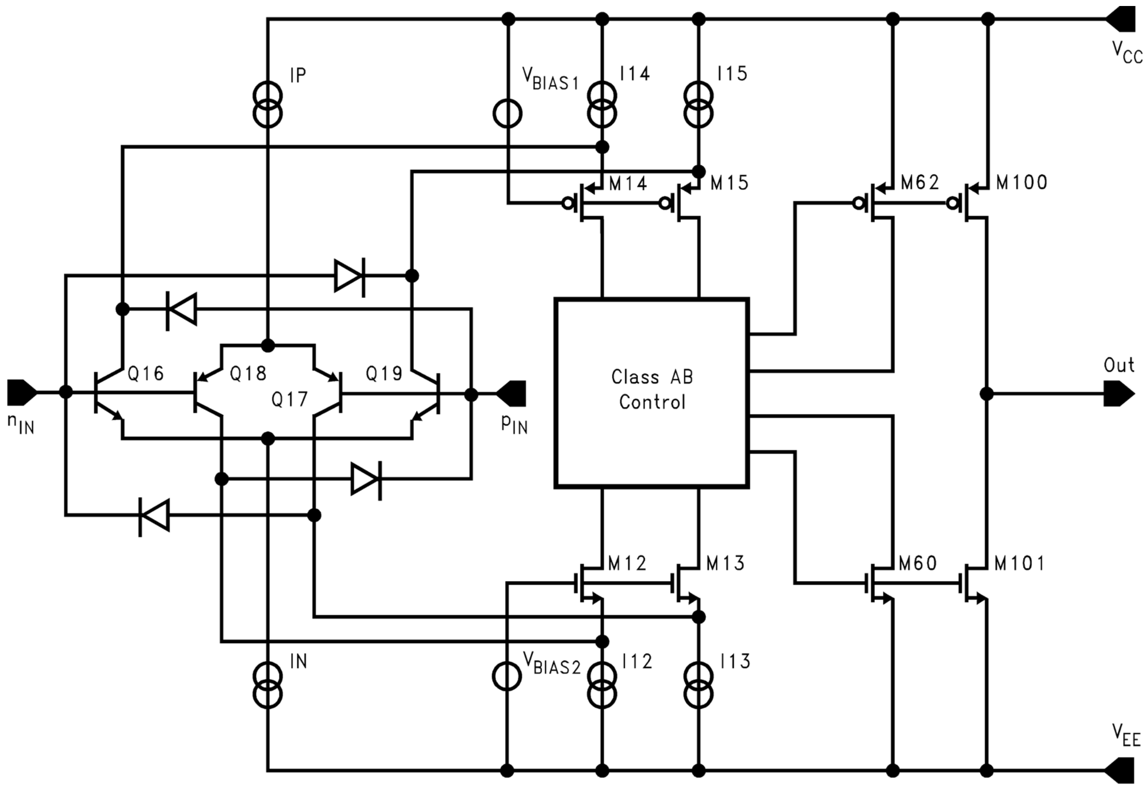


Figure 28. Simplified Schematic Diagram

This V_{OS} crossover point can create problems for both DC− and AC-coupled signals if proper care is not taken. Large input signals that include the V_{OS} crossover point causes distortion in the output signal. One way to avoid such distortion is to keep the signal away from the crossover. For example, in a unity gain buffer configuration with V_S = 5 V, a 5-V peak-to-peak signal contains input-crossover distortion while a 3-V peak-to-peak signal centered at 1.5 V does not contain input-crossover distortion as it avoids the crossover point. Another way to avoid large signal distortion is to use a gain of −1 circuit which avoids any voltage excursions at the input terminals of the amplifier. In that circuit, the common-mode DC voltage can be set at a level away from the V_{OS} cross-over point. For small signals, this transition in V_{OS} shows up as a V_{CM} dependent spurious signal in series with the input signal and can effectively degrade small-signal parameters such as gain and common-mode rejection ratio. To resolve this problem, the small signal must be placed such that it avoids the V_{OS} crossover point. In addition to the rail-to-rail performance, the output stage can provide enough output current to drive 600-Ω loads. Because of the high-current capability, take care not to exceed the 150°C maximum junction temperature specification.

8.4.2 Shutdown Mode

The LMV98x-N family has a shutdown pin. To conserve battery life in portable applications, the LMV98x-N can be disabled when the shutdown pin voltage is pulled low. When in shutdown, the output stage is in a high-impedance state and the input bias current drops to less than 1 nA.

The shutdown pin cannot be left unconnected. In case shut-down operation is not required, the shutdown pin must be connected to V+ when the LMV98x-N are used. Leaving the shutdown pin floating results in an undefined operation mode, either shutdown or active, or even oscillating between the two modes.

Device Functional Modes (continued)

8.4.3 Input Bias Current Consideration

The LMV98x-N family has a complementary bipolar input stage. The typical input bias current (I_B) is 15 nA. The input bias current can develop a significant offset voltage. This offset is primarily due to I_B flowing through the negative feedback resistor, R_F. For example, if I_B is 50 nA and R_F is 100 kΩ, then an offset voltage of 5 mV develops ($V_{OS} = I_B \times R_F$). Using a compensation resistor (R_C), as shown in Figure 29, cancels this effect. But the input offset current (I_{OS}) still contributes to an offset voltage in the same manner.

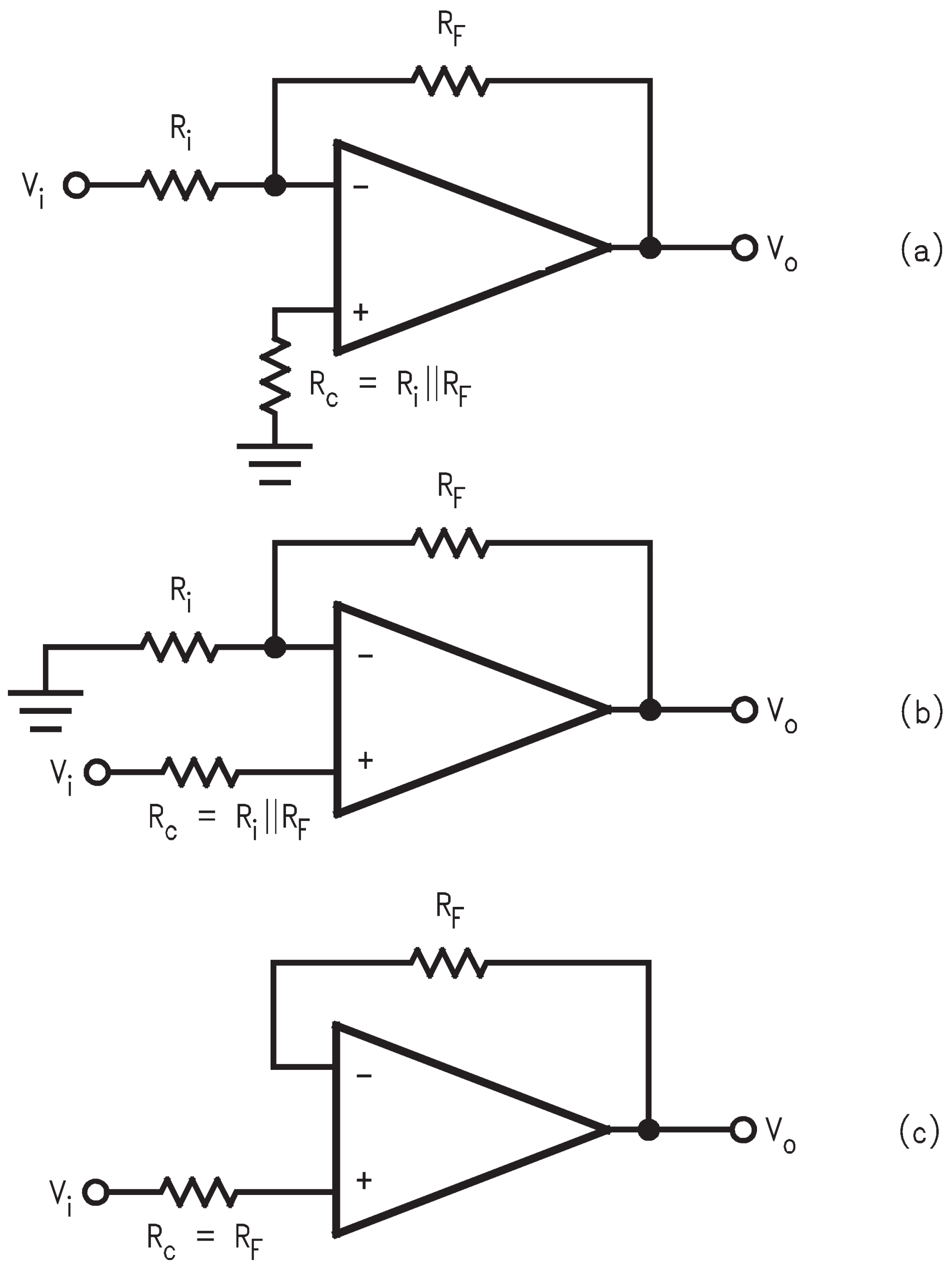


Figure 29. Canceling the Offset Voltage due to Input Bias Current

9 Application and Implementation

NOTE

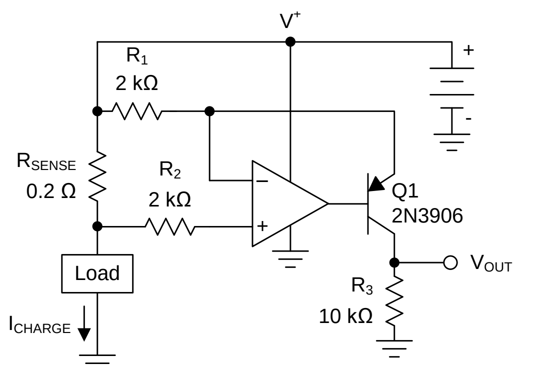
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The LMV98x-N devices bring performance, economy, and ease-of-use to low-voltage, low-power systems. They provide rail-to-rail input and rail-to-rail output swings into heavy loads.

9.2 Typical Applications

9.2.1 High-Side Current-Sensing Application



$$V_{OUT} = \frac{R_{SENSE} \times R_3}{R_1} \times I_{CHARGE} = 1\Omega \times I_{CHARGE}$$

Figure 30. High-Side Current Sensing

9.2.1.1 Design Requirements

The high-side current-sensing circuit (Figure 30) is commonly used in a battery charger to monitor charging current to prevent overcharging. A sense resistor R_{SENSE} is connected to the battery directly. This system requires an op amp with rail-to-rail input. The LMV98x-N are ideal for this application because its common-mode input range extends up to the positive supply.

9.2.1.2 Detailed Design Procedure

As seen in Figure 30, the I_{CHARGE} current flowing through sense resistor R_{SENSE} develops a voltage drop equal to V_{SENSE}. The voltage at the negative sense point is now less than the positive sense point by an amount proportional to the V_{SENSE} voltage.

The low-bias currents of the LMV98x cause little voltage drop through R_2, so the negative input of the LMV98x amplifier is at essentially the same potential as the negative sense input.

The LMV98x detects this voltage error between its inputs and servo the transistor base to conduct more current through Q1, increasing the voltage drop across R_1 until the LMV98x inverting input matches the noninverting input. At this point, the voltage drop across R_1 now matches V_{SENSE}.

I_G, a current proportional to I_{CHARGE}, flows according to Equation 2.

$$I_G = V_{RSENSE} / R_1 = (R_{SENSE} \times I_{CHARGE}) / R_1 \quad (2)$$

Typical Applications (continued)

I_G also flows through the gain resistor R_3 developing a voltage drop equal to Equation 3 and Equation 4.

$$V_3 = I_G \times R_3 = (V_{RSENSE} / R_1) \times R_3 = ((R_{SENSE} \times I_{CHARGE}) / R_2) \times R_3 \quad (3)$$

$$V_{OUT} = (R_{SENSE} \times I_{CHARGE}) \times G$$

where

- $G = R_3 / R_1$ (4)

The other channel of the LMV98x may be used to buffer the voltage across R3 to drive the following stages.

9.2.1.3 Application Curve

Figure 31 shows the results of the example current sense circuit. After 4 V, there is an error where transistor Q1 runs out of headroom and saturates, limiting the upper output swing.

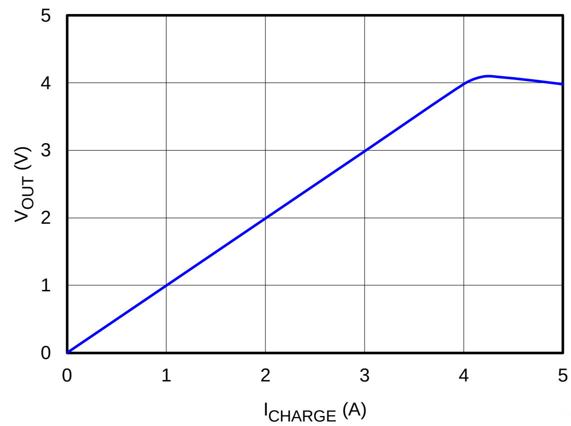


Figure 31. Current Sense Amplifier Results

9.2.2 Half-Wave Rectifier Applications

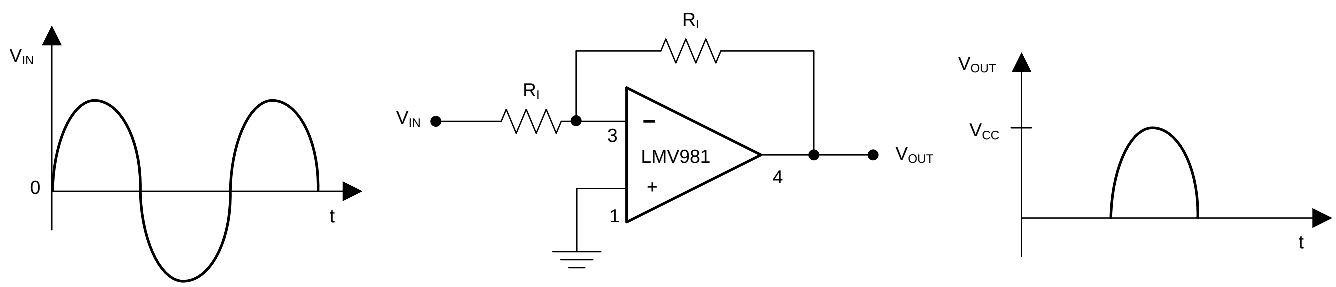


Figure 32. Half-Wave Rectifier With Rail-To-Ground Output Swing Referenced to Ground

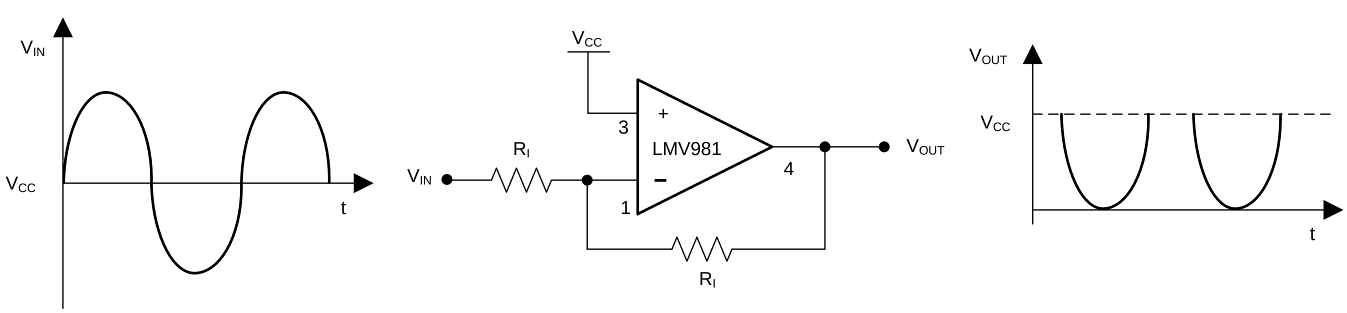


Figure 33. Half-Wave Rectifier With Negative-Going Output Referenced to V_{CC}

Typical Applications (continued)

9.2.2.1 Design Requirements

Because the LMV98x-N input common-mode range includes both positive and negative supply rails and the output can also swing to either supply, achieving half-wave rectifier functions in either direction is an easy task. All that is required are two external resistors; there is no requirement for diodes or matched resistors. The half-wave rectifier can have either positive or negative going outputs, depending on the way the circuit is arranged.

9.2.2.2 Detailed Design Procedure

In Figure 32 the circuit is referenced to ground, while in Figure 33 the circuit is biased to the positive supply. These configurations implement the half-wave rectifier because the LMV98x-N can not respond to one-half of the incoming waveform. It can not respond to one-half of the incoming because the amplifier cannot swing the output beyond either rail; therefore, the output disengages during this half cycle. During the other half cycle, however, the amplifier achieves a half wave that can have a peak equal to the total supply voltage. R_l must be large enough not to load the LMV98x-N.

9.2.2.3 Application Curves

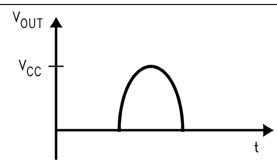


Figure 34. Output of Ground-to-Rail Circuit

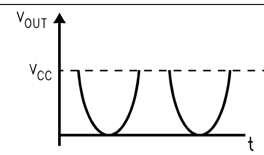


Figure 35. Output of Rail-to-Ground Circuit

9.2.3 Instrumentation Amplifier With Rail-to-Rail Input and Output Application

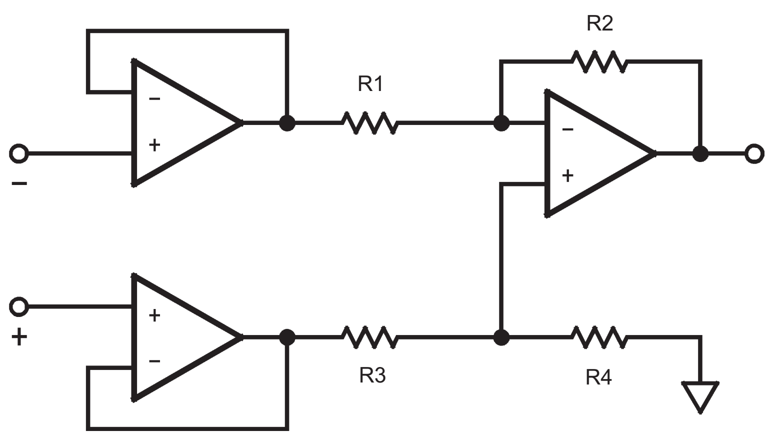


Figure 36. Rail-to-Rail Instrumentation Amplifier

9.2.3.1 Design Requirements

Using three of the LMV98x-N amplifiers, an instrumentation amplifier with rail-to-rail inputs and outputs can be made as shown in Figure 36.

9.2.3.2 Detailed Design Procedure

In this example, amplifiers on the left side act as buffers to the differential stage. These buffers assure that the input impedance is high. They also assure that the difference amp is driven from a voltage source. This is necessary to maintain the CMRR set by the matching R_1 to R_2 with R_3 to R_4. The gain is set by the ratio of R_2/R_1 and R_3 must equal R_1 and R_4 equal R_2. With both rail-to-rail input and output ranges, the input and output are only limited by the supply voltages. Remember that even with rail-to-rail outputs, the output can not swing past the supplies so the combined common-mode voltages plus the signal must not be greater that the supplies or limiting occurs.

Typical Applications (continued)

9.2.3.3 Application Curve

Figure 37 shows the results of the instrumentation amplifier with R_1 and R_3 = 1 K, and R_2 and R_4 = 100 kΩ, for a gain of 100, running on a single 5-V supply with a input of V_{CM} = V_S/2. The combined effects of the individual offset voltages can be seen as a shift in the offset of the curve.

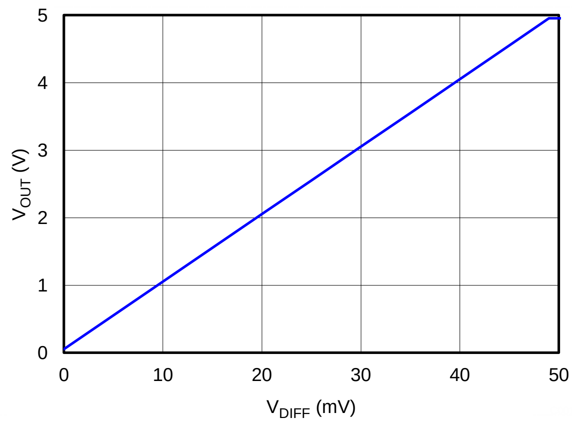


Figure 37. Instrumentation Amplifier Output Results

9.3 Do's and Don'ts

Do properly bypass the power supplies.

Do add series resistence to the output when driving capacitive loads, particularly cables, Muxes and ADC inputs.

Do add series current limiting resistors and external schottky clamp diodes if input voltage is expected to exceed the supplies. Limit the current to 1 mA or less (1 kΩ per volt).

10 Power Supply Recommendations

The LMV98x-N is specified for operation from 1.8 V to 5 V; many specifications apply from –40°C to 125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in *Typical Characteristics*.

CAUTION

Supply voltages larger than 5.5 V can permanently damage the device; see *Absolute Maximum Ratings*.

For proper operation, the power supplies must be properly decoupled. For decoupling the supply lines, TI recommends that 10-nF capacitors be placed as close as possible to the op amp power supply pins. For single-supply, place a capacitor between V^+ and V^- supply leads. For dual supplies, place one capacitor between V^+ and ground, and one capacitor between V^- and ground.

11 Layout

11.1 Layout Guidelines

The V^+ pin must be bypassed to ground with a low-ESR capacitor.

The optimum placement is closest to the V^+ and ground pins.

Take care to minimize the loop area formed by the bypass capacitor connection between V^+ and ground.

The ground pin must be connected to the PCB ground plane at the pin of the device.

The feedback components must be placed as close to the device as possible minimizing strays.

11.2 Layout Example

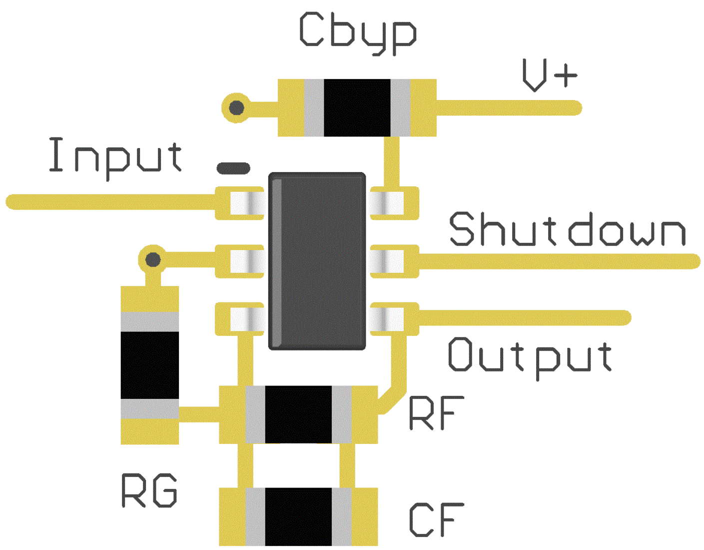


Figure 38. SOT-23 Layout Example

12 デバイスおよびドキュメントのサポート

12.1 ドキュメントのサポート

12.1.1 関連資料

関連資料については、以下を参照してください。

『ハンダ付けの絶対最大定格』(SNOA549)

12.2 関連リンク

次の表に、クイック・アクセス・リンクを示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびサンプル注文またはご購入へのクイック・アクセスが含まれます。

表 1. 関連リンク

製品	プロダクト・フォルダ	サンプルとご購入	技術資料	ツールとソフトウェア	サポートとコミュニティ
LMV981-N	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
LMV982-N	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

12.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

12.4 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 商標

E2E is a trademark of Texas Instruments.
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12.6 静電気放電に関する注意事項

これらのデバイスは、限定的なESD(静電破壊)保護機能を内 蔵しています。保存時または取り扱い時は、MOSゲートに対す る静電破壊を防止するために、リード線同士をショートさせて おくか、デバイスを導電フォームに入れる必要があります。

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMV981MF	LIFEBUY	SOT-23	DBV	6	1000	Non-RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 125	A78A	
LMV981MF/NOPB	ACTIVE	SOT-23	DBV	6	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	A78A	Samples
LMV981MFX/NOPB	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	A78A	Samples
LMV981MG/NOPB	ACTIVE	SC70	DCK	6	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	A77	Samples
LMV981MGX/NOPB	ACTIVE	SC70	DCK	6	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	A77	Samples
LMV981TL/NOPB	ACTIVE	DSBGA	YZR	6	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	A H	Samples
LMV981TLX/NOPB	ACTIVE	DSBGA	YZR	6	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	A H	Samples
LMV982MM/NOPB	ACTIVE	VSSOP	DGS	10	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	A87A	Samples
LMV982MMX/NOPB	ACTIVE	VSSOP	DGS	10	3500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	A87A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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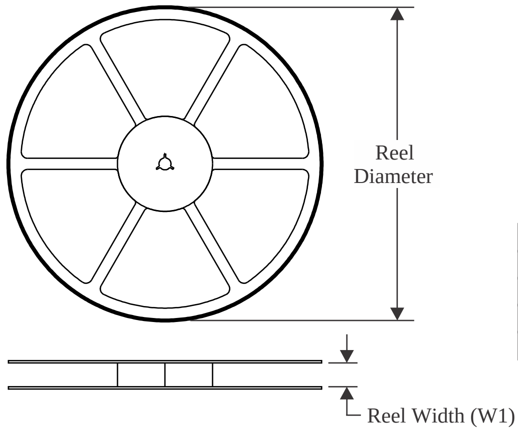
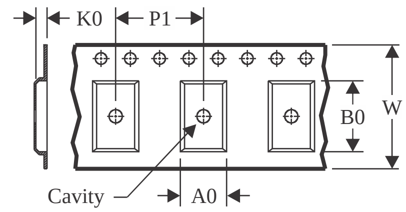
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

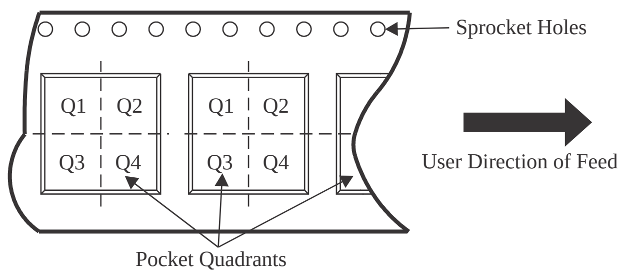


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

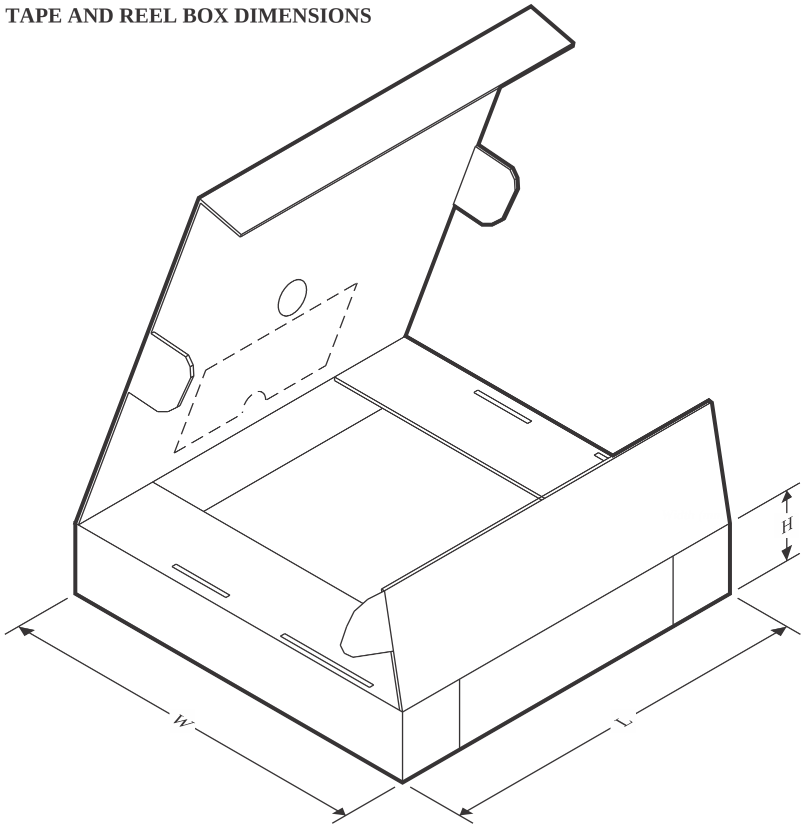
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

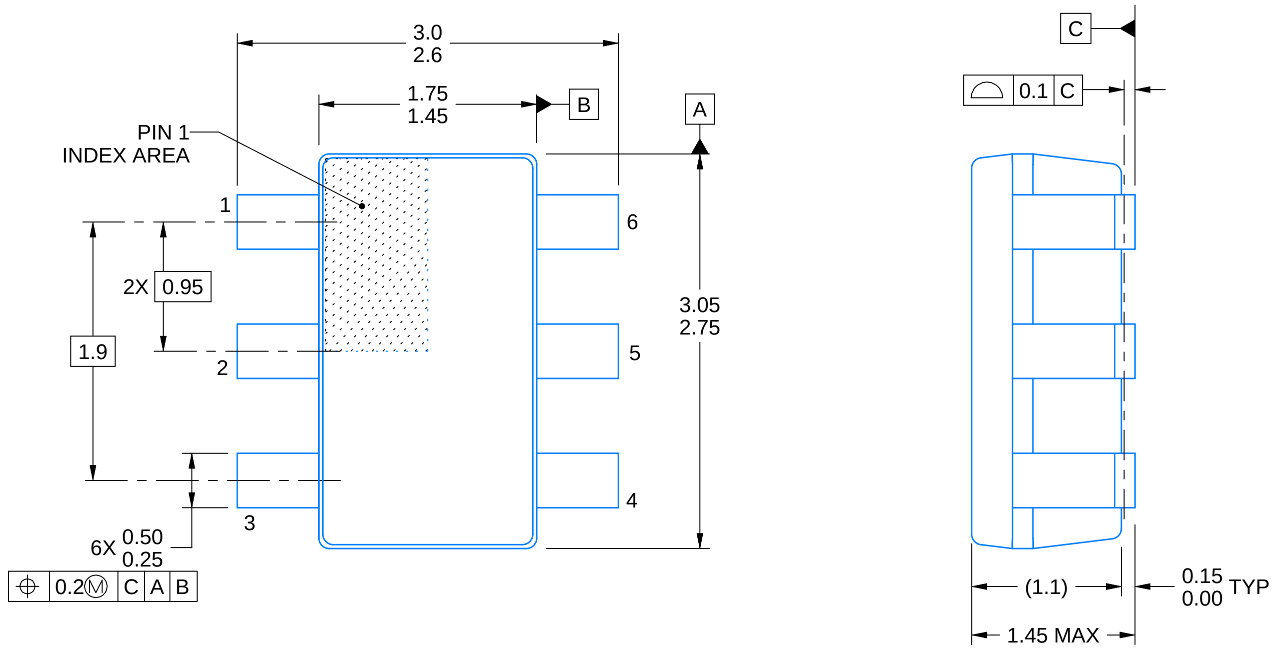
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV981MF	SOT-23	DBV	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV981MF/NOPB	SOT-23	DBV	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV981MFX/NOPB	SOT-23	DBV	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV981MG/NOPB	SC70	DCK	6	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV981MGX/NOPB	SC70	DCK	6	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV981TL/NOPB	DSBGA	YZR	6	250	178.0	8.4	1.12	1.63	0.76	4.0	8.0	Q1
LMV981TLX/NOPB	DSBGA	YZR	6	3000	178.0	8.4	1.12	1.63	0.76	4.0	8.0	Q1
LMV982MM/NOPB	VSSOP	DGS	10	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV982MMX/NOPB	VSSOP	DGS	10	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

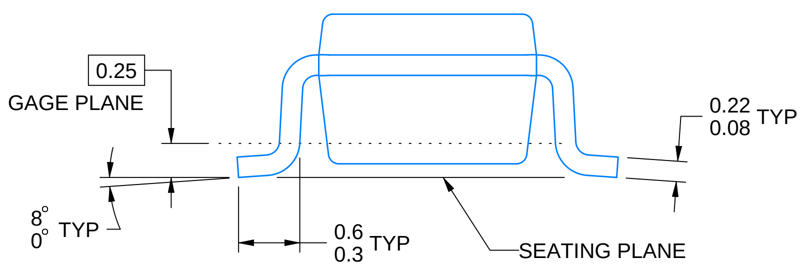
TAPE AND REEL BOX DIMENSIONS

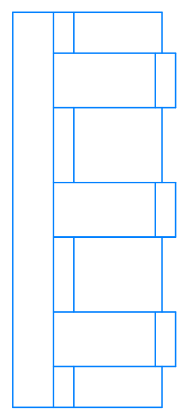


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV981MF	SOT-23	DBV	6	1000	208.0	191.0	35.0
LMV981MF/NOPB	SOT-23	DBV	6	1000	208.0	191.0	35.0
LMV981MFX/NOPB	SOT-23	DBV	6	3000	208.0	191.0	35.0
LMV981MG/NOPB	SC70	DCK	6	1000	208.0	191.0	35.0
LMV981MGX/NOPB	SC70	DCK	6	3000	208.0	191.0	35.0
LMV981TL/NOPB	DSBGA	YZR	6	250	208.0	191.0	35.0
LMV981TLX/NOPB	DSBGA	YZR	6	3000	208.0	191.0	35.0
LMV982MM/NOPB	VSSOP	DGS	10	1000	208.0	191.0	35.0
LMV982MMX/NOPB	VSSOP	DGS	10	3500	367.0	367.0	35.0





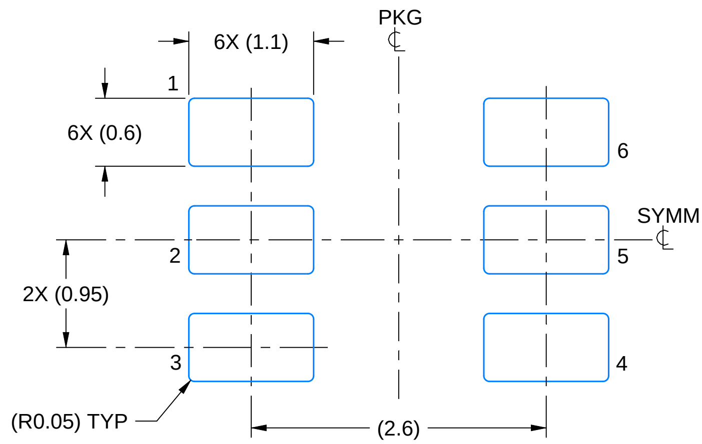


ALTERNATIVE PACKAGE SINGULATION VIEW

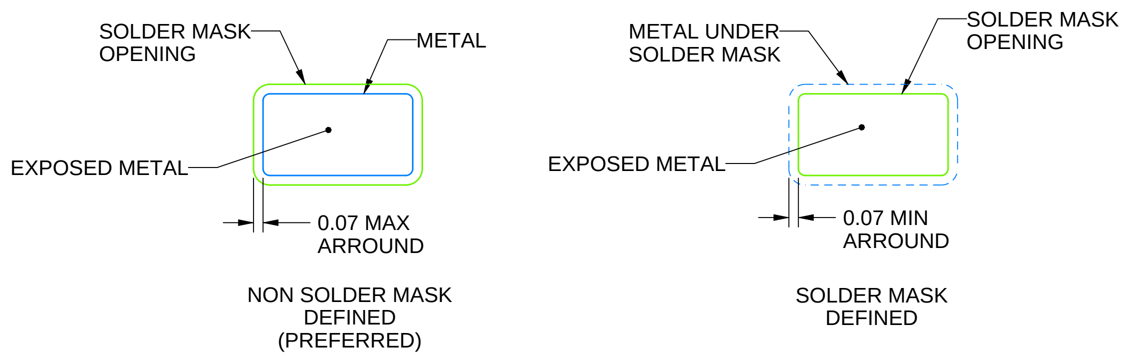
4214840/E 02/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

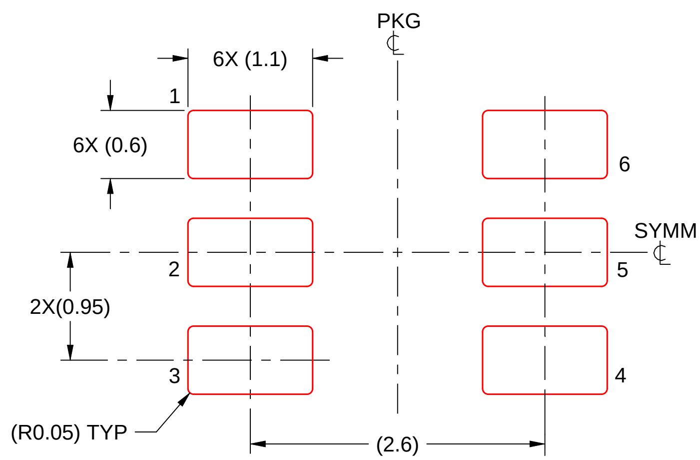


SOLDER MASK DETAILS

4214840/E 02/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

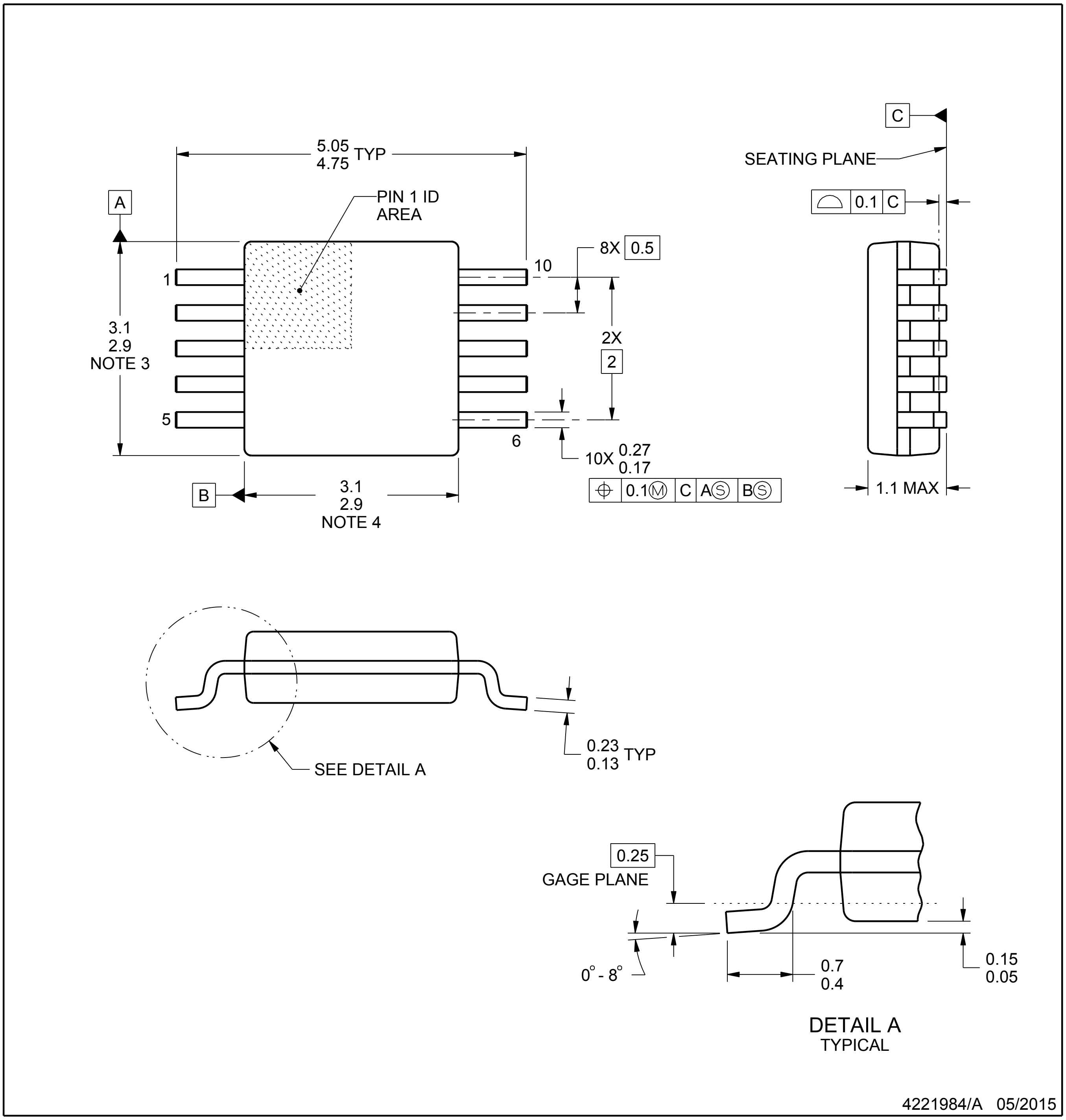


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/E 02/2024

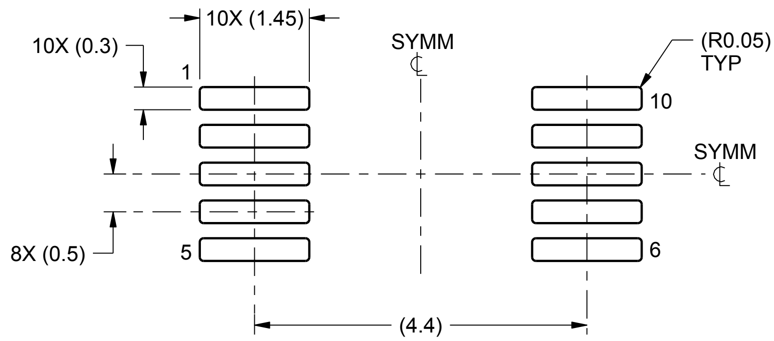
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

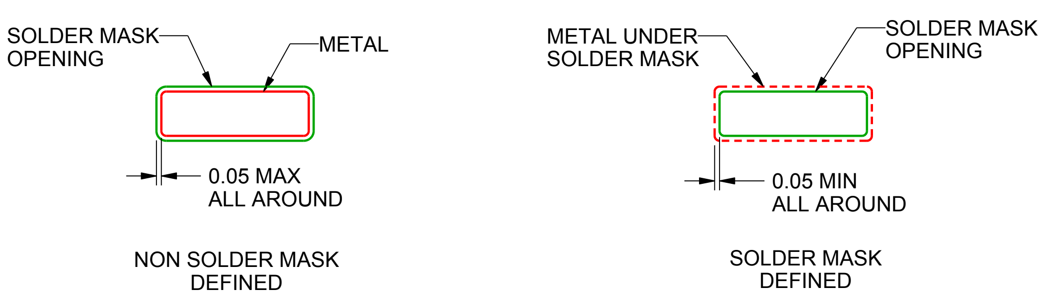


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

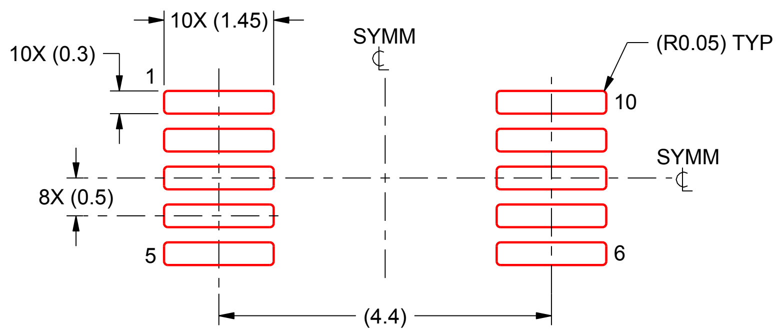


SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



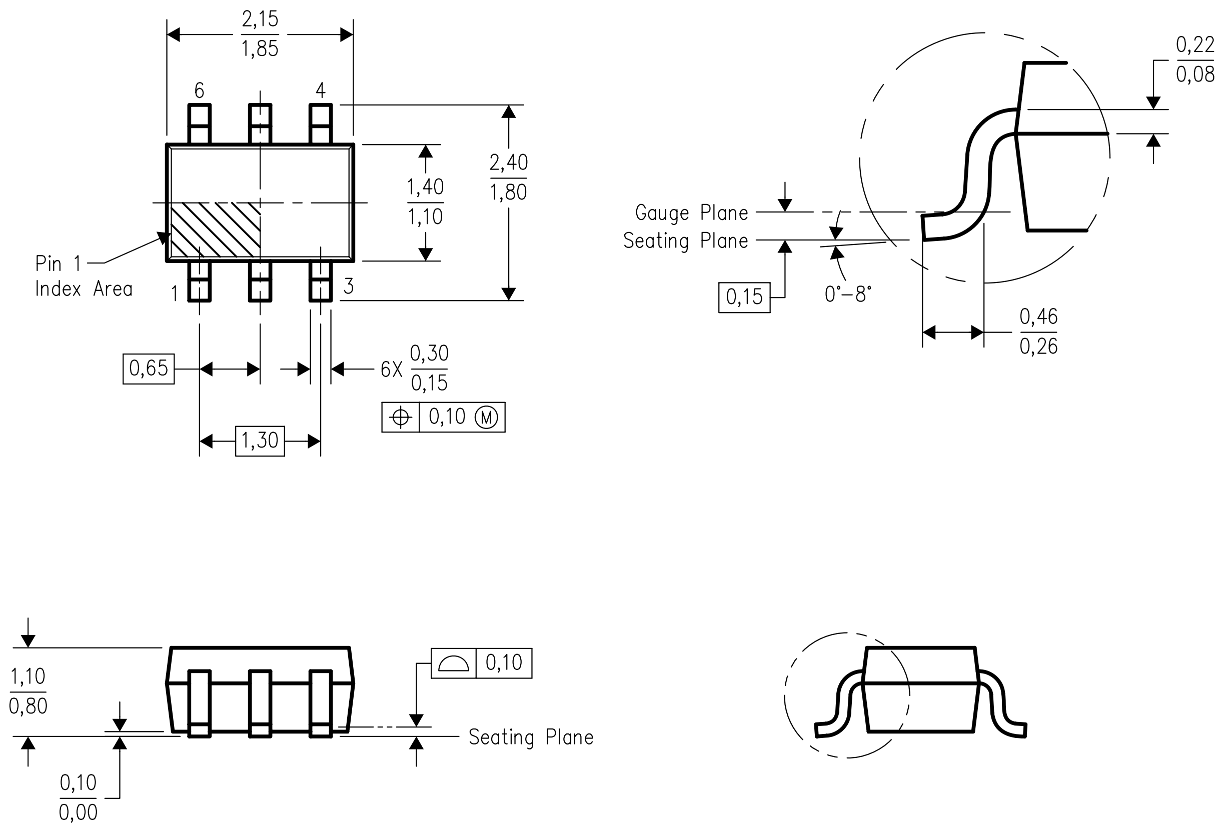
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

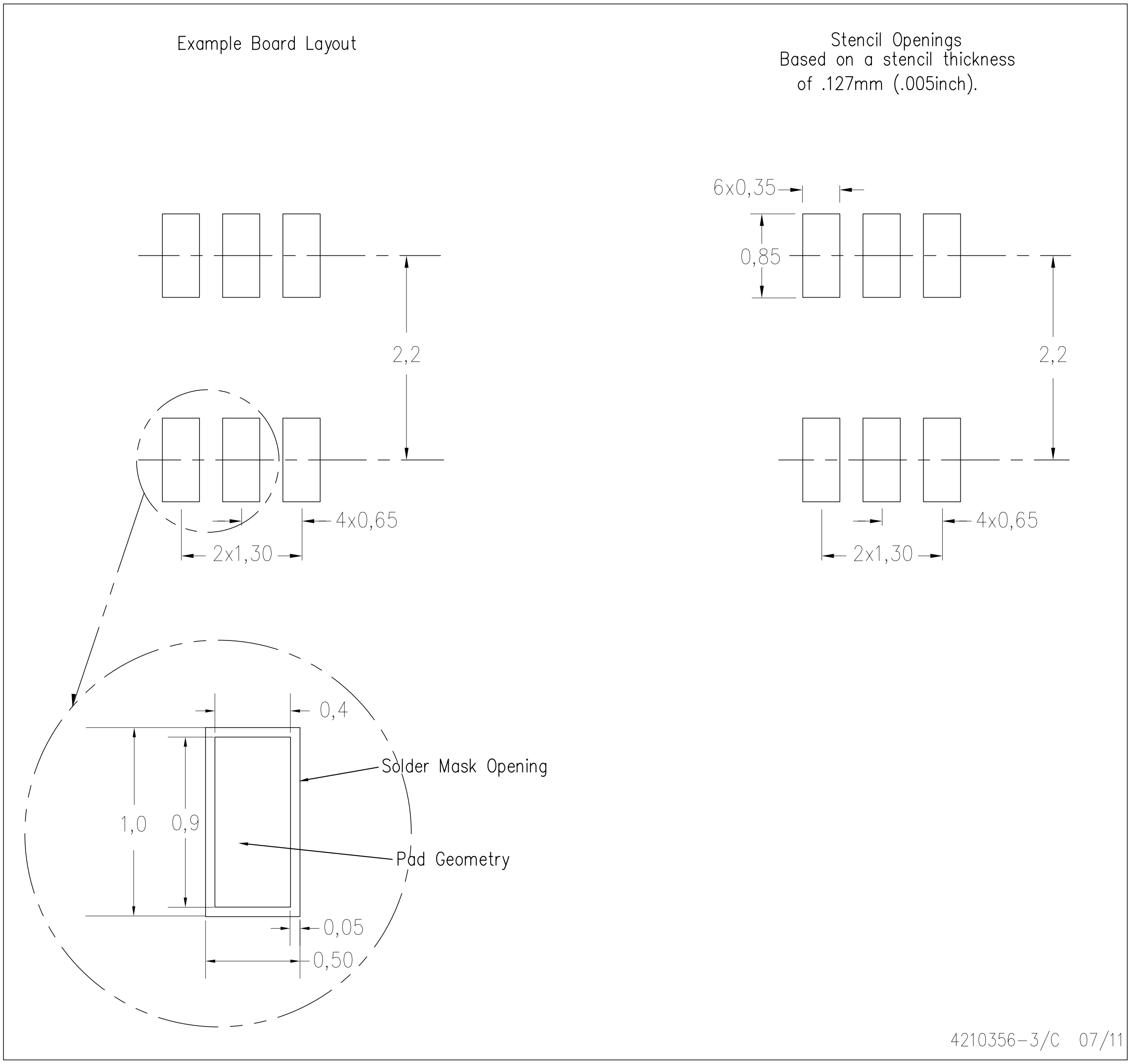
DCK (R-PDSO-G6) PLASTIC SMALL-OUTLINE PACKAGE



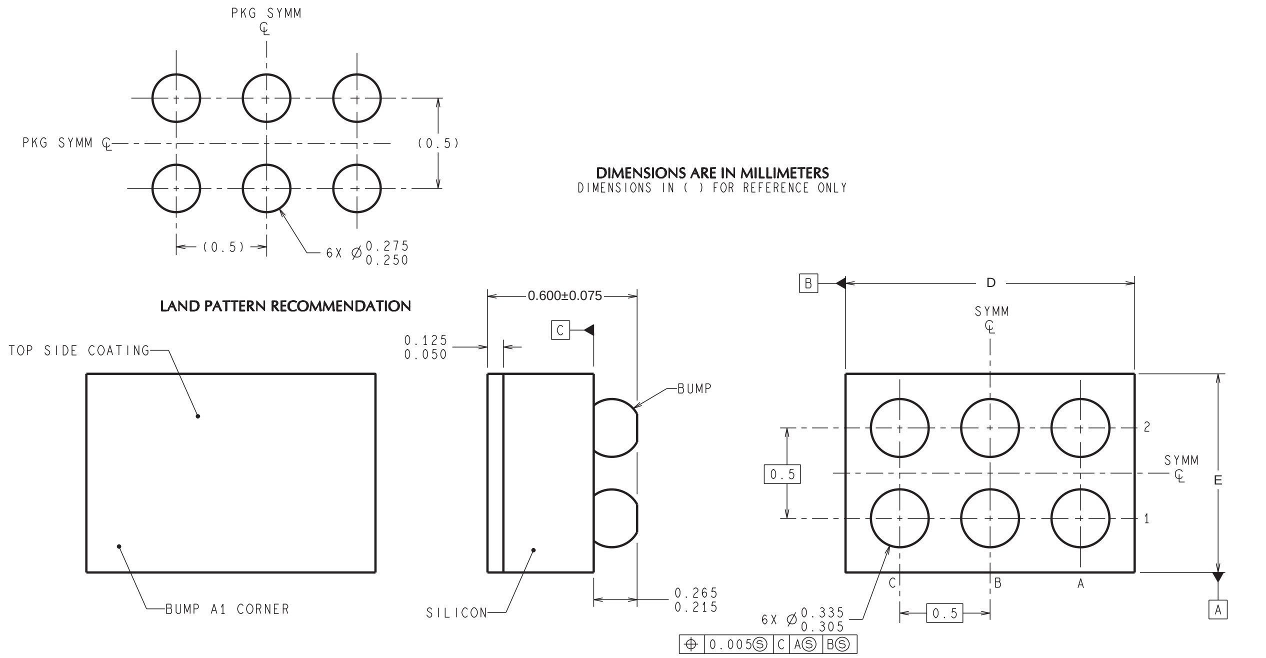
4093553-4/G 01/2007

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO-203 variation AB.

DCK (R–PDSO–G6) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC–7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.



TLA06XXX (Rev C)

D: Max = 1.565 mm, Min =1.504 mm

E: Max = 1.057 mm, Min =0.996 mm

4215044/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.