

## LPV811/LPV812 高精度425nA Nanopowerオペアンプ

### 1 特長

- ナノパワー消費電流: チャンネルごとに425nA
- オフセット電圧: 300 $\mu$ V (最大値)
- $T_cV_{os}$ : 1 $\mu$ V/ $^{\circ}$ C
- ゲイン帯域幅: 8kHz
- ユニティ・ゲインで安定
- 低い入力バイアス電流: 100fA
- 広い電源電圧範囲: 1.6V~5.5V
- レール・ツー・レール出力
- 出力反転なし
- EMI保護
- 温度範囲: -40 $^{\circ}$ C~+125 $^{\circ}$ C
- 業界標準パッケージ:
  - シングル: 5ピンSOT-23
  - デュアル: 8ピンVSSOP

### 2 アプリケーション

- COおよびO<sub>2</sub>ガスの検出器(TIDA-0756)
- PIR動作検出器
- 電流検出
- サーモスタット
- IoTリモート・センサ
- アクティブRFIDリーダーおよびタグ
- 携帯型医療機器

### 3 概要

LPV811 (シングル)およびLPV812 (デュアル)は、バッテリー駆動のワイヤレスおよび低消費電力の有線機器における「常時オン」センシング・アプリケーションを対象とした、超低消費電力の高精度オペアンプ・ファミリです。425nAの静止電流からの8kHz帯域幅、および300 $\mu$ V未満にトリムされたオフセット電圧により、LPV81xアンプはガス検出器や携帯用電子機器など、バッテリー動作時間が重要な機器において、要求される精度を実現しながら、消費電力を最小化できます。

超低消費電力に加えて、LPV81xアンプにはCMOS入力段があり、インピーダンス源のアプリケーションについてバイアス電流がフェムトアンペア単位です。またLPV81xアンプには、負のレール・センシング入力段とレール・ツー・レール出力段が搭載されており、レールから数mVの範囲内までスイング可能で、可能な限り最も広いダイナミック・レンジを維持できます。LPV81xの設計には、携帯電話、WiFi、ラジオ送信機、タグ・リーダーからの不要なRF信号に対するシステムの感受性を低下させるため、EMI保護が組み込まれています。

#### 製品情報<sup>(1)</sup>

型番	パッケージ	本体サイズ
LPV811	SOT-23 (5)	2.90mmx1.60mm
LPV812	VSSOP (8)	3.00mmx3.00mm

#### LPV8xxファミリのNanopowerアンプ

型番	チャンネル	消費電流 (標準値 /チャンネル)	オフセット 電圧 (最大値)
LPV801	1	500nA	3.5mV
LPV802	2	320nA	3.5mV
LPV811	1	450nA	370 $\mu$ V
LPV812	2	425nA	300 $\mu$ V

(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

図 1. NanoPower COセンサ

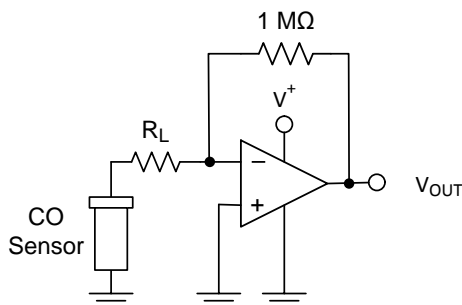
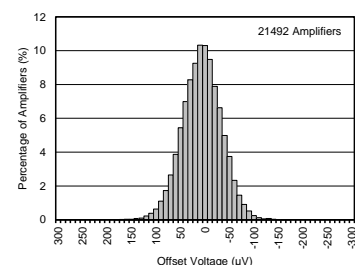


図 2. LPV812のオフセット電圧分布



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## 4 改訂履歴

### Revision A (October 2016) から Revision B に変更

**Page**

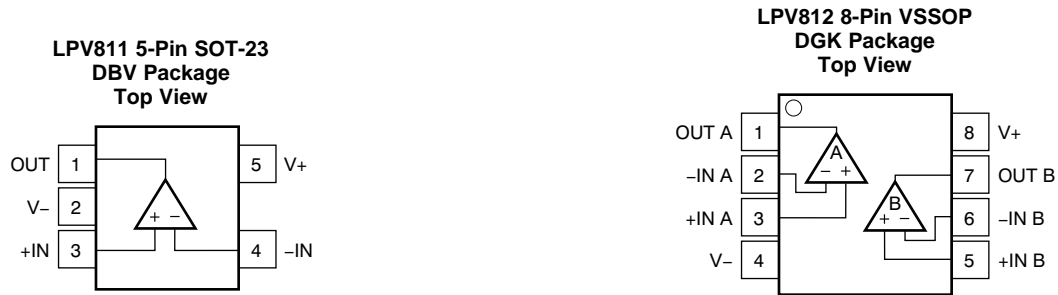
•	表紙にファミリのアップセル表を 追加.....	<b>1</b>
•	表紙のO2センシング回路をオフセット電圧分布のグラフに 変更 .....	<b>1</b>
•	大きなファミリのアップセル表を 削除.....	<b>2</b>
•	Deleted LPV811 preview "preliminary spec" table note. ....	<b>5</b>
•	Added separate LPV811 CMRR Specification. ....	<b>5</b>
•	Added offset distribution graphs .....	<b>6</b>

### 2016年8月発行のものから更新

**Page**

•	製品プレビューから量産データへ 変更 .....	<b>1</b>
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## 5 Pin Configuration and Functions



**Pin Functions: LPV811 DBV**

PIN		TYPE	DESCRIPTION
NAME	NUMBER		
OUT	1	O	Output
-IN	4	I	Inverting Input
+IN	3	I	Non-Inverting Input
V-	2	P	Negative (lowest) power supply
V+	5	P	Positive (highest) power supply

**Pin Functions: LPV812 DGK**

PIN		TYPE	DESCRIPTION
NAME	NUMBER		
OUT A	1	O	Channel A Output
-IN A	2	I	Channel A Inverting Input
+IN A	3	I	Channel A Non-Inverting Input
V-	4	P	Negative (lowest) power supply
+IN B	5	I	Channel B Non-Inverting Input
-IN B	6	I	Channel B Inverting Input
OUT B	7	O	Channel B Output
V+	8	P	Positive (highest) power supply

## 6 Specifications

### 6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

		MIN	MAX	UNIT
Supply voltage, $V_s = (V+) - (V-)$		-0.3	6	V
Input pins	Voltage <sup>(2) (3)</sup>	Common mode		(V-) - 0.3 (V+) + 0.3
		Differential		(V-) - 0.3 (V+) + 0.3
Input pins	Current	-10	10	mA
Output short current <sup>(4)</sup>		Continuous	Continuous	
Storage temperature, $T_{stg}$		-65	150	°C
Junction temperature			150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Not to exceed -0.3V or +6.0V on ANY pin, referred to V-
- (3) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3 V beyond the supply rails should be current-limited to 10 mA or less.
- (4) Short-circuit to  $V_s/2$ , one amplifier per package. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.

### 6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±1000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±250	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±2000 V may actually have higher performance.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions. Pins listed as ±750 V may actually have higher performance.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply voltage (V+ – V-)	1.6	5.5	V
Specified temperature	-40	125	°C

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		LPV811 DBV (SOT-23) 5 PINS	LPV812 DGK (VSSOP) 8 PINS	UNIT
$\theta_{JA}$	Junction-to-ambient thermal resistance	177.4	177.6	°C/W
$\theta_{JcTop}$	Junction-to-case (top) thermal resistance	133.9	68.8	
$\theta_{JB}$	Junction-to-board thermal resistance	36.3	98.2	
$\Psi_{JT}$	Junction-to-top characterization parameter	23.6	12.3	
$\Psi_{JB}$	Junction-to-board characterization parameter	35.7	96.7	

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.5 Electrical Characteristics

$T_A = 25^\circ\text{C}$ ,  $V_S = 1.8\text{ V to } 5\text{ V}$ ,  $V_{CM} = V_{OUT} = V_S/2$ , and  $R_L \geq 10\text{ M}\Omega$  to  $V_S/2$ , unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>OFFSET VOLTAGE</b>						
$V_{OS}$	Input offset voltage, LPV811	$V_S = 1.8\text{ V and } 3.3\text{ V}$ , $V_{CM} = V_-$		$\pm 60$	$\pm 370$	$\mu\text{V}$
	Input offset voltage, LPV812	$V_S = 1.8\text{ V and } 3.3\text{ V}$ , $V_{CM} = V_-$		$\pm 55$	$\pm 300$	$\mu\text{V}$
$\Delta V_{OS}/\Delta T$	Input offset drift	$V_{CM} = V_-$		$\pm 1$		$\mu\text{V}/^\circ\text{C}$
PSRR	Power-supply rejection ratio	$V_S = 1.8\text{ V to } 3.3\text{ V}$ , $V_{CM} = V_-$		$\pm 1.6$	$\pm 60$	$\mu\text{V}/\text{V}$
<b>INPUT VOLTAGE RANGE</b>						
$V_{CM}$	Common-mode voltage range	$V_S = 3.3\text{ V}$	0		2.4	V
CMRR	Common-mode rejection ratio, LPV811	$(V_-) \leq V_{CM} \leq (V_+) - 0.9\text{ V}$ , $V_S = 3.3\text{ V}$	77	95		dB
	Common-mode rejection ratio, LPV812	$(V_-) \leq V_{CM} \leq (V_+) - 0.9\text{ V}$ , $V_S = 3.3\text{ V}$	80	98		dB
<b>INPUT BIAS CURRENT</b>						
$I_B$	Input bias current	$V_S = 1.8\text{ V}$		$\pm 100$		fA
$I_{OS}$	Input offset current	$V_S = 1.8\text{ V}$		$\pm 100$		fA
<b>INPUT IMPEDANCE</b>						
	Differential			7		pF
	Common mode			3		pF
<b>NOISE</b>						
$E_n$	Input voltage noise	$f = 0.1\text{ Hz to } 10\text{ Hz}$		6.5		$\mu\text{Vp-p}$
$e_n$	Input voltage noise density	$f = 100\text{ Hz}$		340		$\text{nV}/\sqrt{\text{Hz}}$
		$f = 1\text{ kHz}$		420		
<b>OPEN-LOOP GAIN</b>						
$A_{OL}$	Open-loop voltage gain	$(V_-) + 0.3\text{ V} \leq V_O \leq (V_+) - 0.3\text{ V}$ , $R_L = 100\text{ k}\Omega$		120		dB
<b>OUTPUT</b>						
$V_{OH}$	Voltage output swing from positive rail	$V_S = 1.8\text{ V}$ , $R_L = 100\text{ k}\Omega$ to $V^+/2$	10	3.5		mV
$V_{OL}$	Voltage output swing from negative rail	$V_S = 1.8\text{ V}$ , $R_L = 100\text{ k}\Omega$ to $V^+/2$		2.5	10	
$I_{SC}$	Short-circuit current	$V_S = 3.3\text{ V}$ , Short to $V_S/2$		4.7		mA
$Z_O$	Open loop output impedance	$f = 1\text{ KHz}$ , $I_O = 0\text{ A}$		90		k $\Omega$
<b>FREQUENCY RESPONSE</b>						
GBP	Gain-bandwidth product	$C_L = 20\text{ pF}$ , $R_L = 10\text{ M}\Omega$ , $V_S = 5\text{ V}$		8		kHz
SR	Slew rate (10% to 90%)	$G = 1$ , Rising Edge, $C_L = 20\text{ pF}$ , $V_S = 5\text{ V}$		2		V/ms
		$G = 1$ , Falling Edge, $C_L = 20\text{ pF}$ , $V_S = 5\text{ V}$		2.1		
<b>POWER SUPPLY</b>						
$I_Q$	Quiescent Current, LPV811	$V_{CM} = V_-$ , $I_O = 0$ , $V_S = 3.3\text{ V}$		450	540	nA
	Quiescent Current, Per Channel, LPV812	$V_{CM} = V_-$ , $I_O = 0$ , $V_S = 3.3\text{ V}$		425	495	

### 6.6 Typical Characteristics

at  $T_A = 25^\circ\text{C}$ ,  $R_L = 10\text{M}\Omega$  to  $V_S/2$ ,  $C_L = 20\text{pF}$ ,  $V_{CM} = V_S / 2\text{V}$  unless otherwise specified.

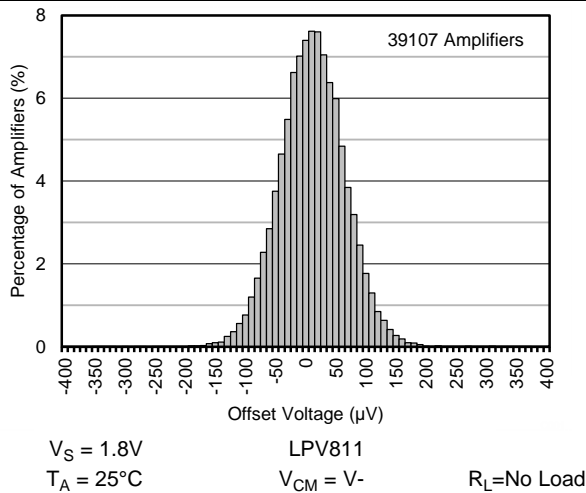


Figure 3. Offset Distribution of LPV811

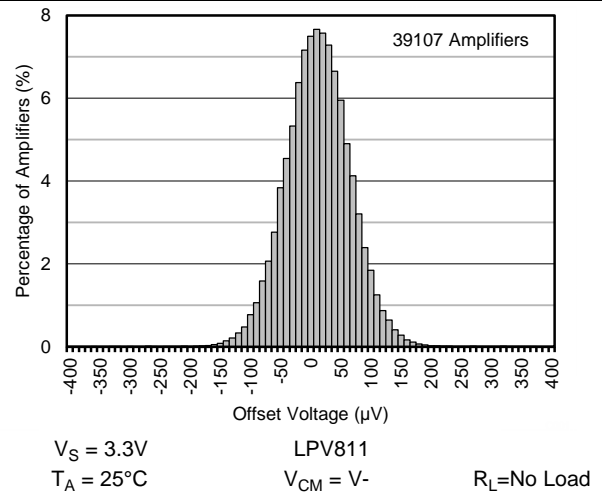


Figure 4. Offset Distribution of LPV811

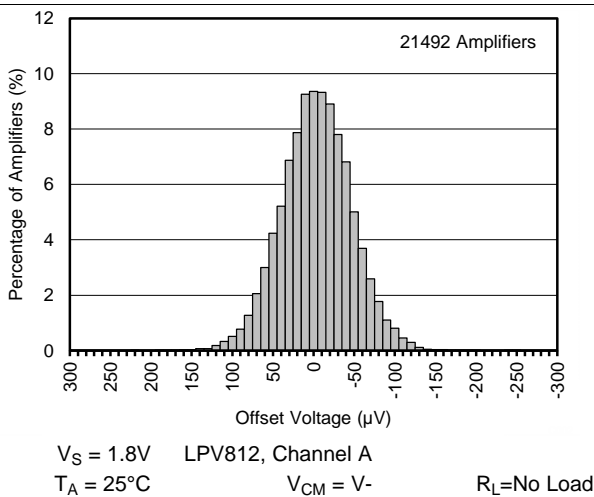


Figure 5. Offset Distribution of LPV812, CH A

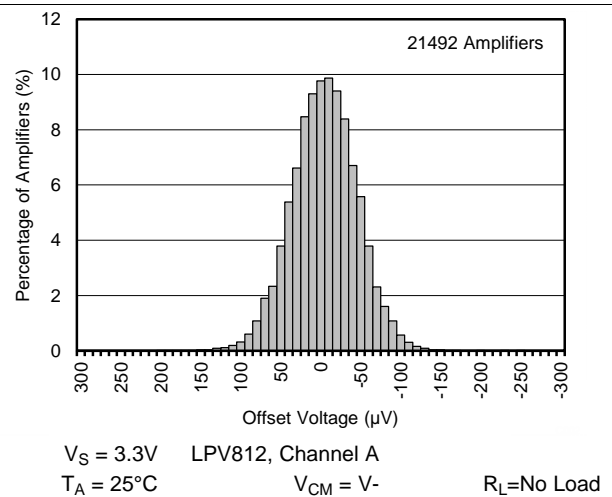


Figure 6. Offset Distribution of LPV812, CH A

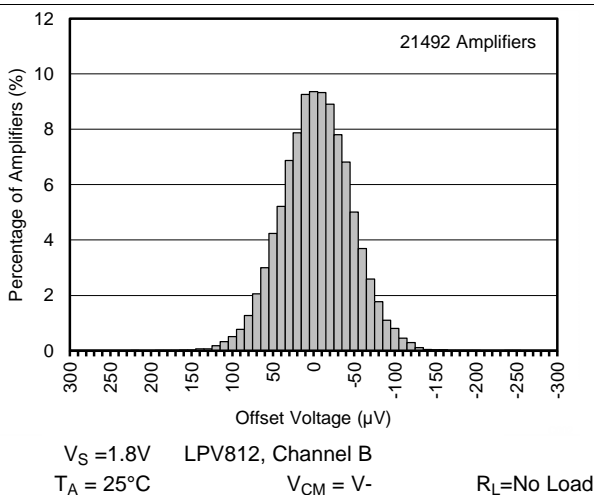


Figure 7. Offset Distribution of LPV812, CH B

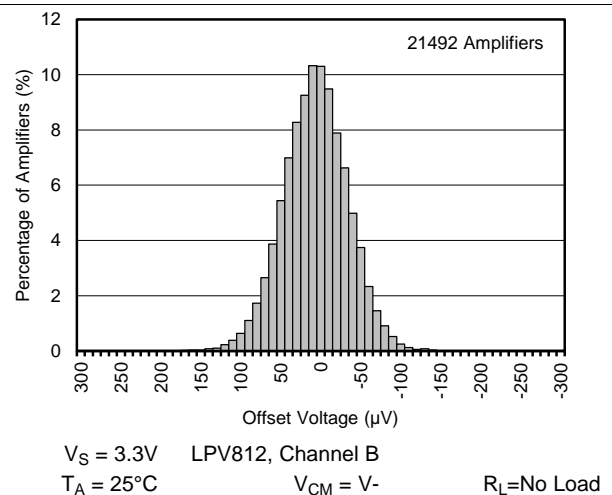


Figure 8. Offset Distribution of LPV812, CH B

Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $R_L = 10\text{M}\Omega$  to  $V_S/2$ ,  $C_L = 20\text{pF}$ ,  $V_{CM} = V_S / 2\text{V}$  unless otherwise specified.

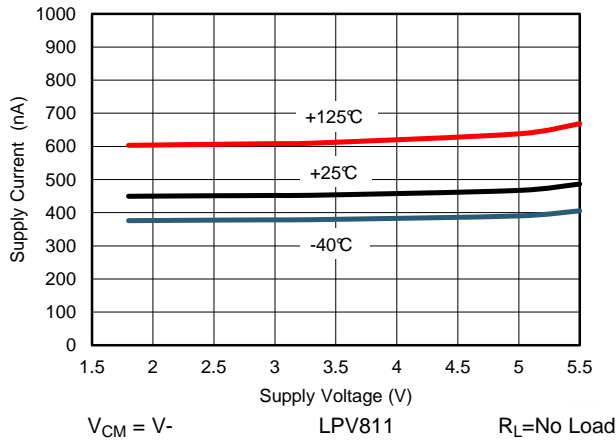


Figure 9. Supply Current vs. Supply Voltage, LPV811

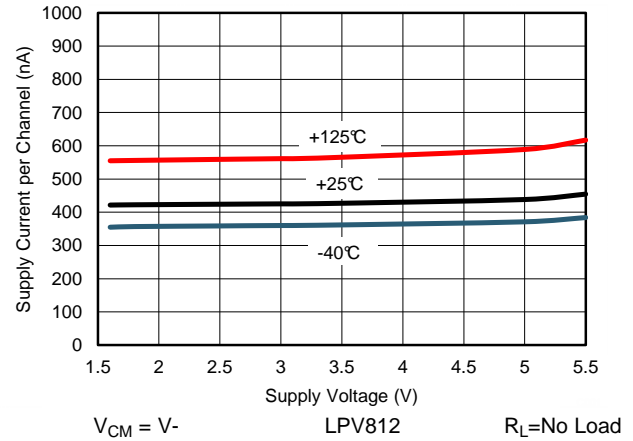


Figure 10. Supply Current vs. Supply Voltage, LPV812

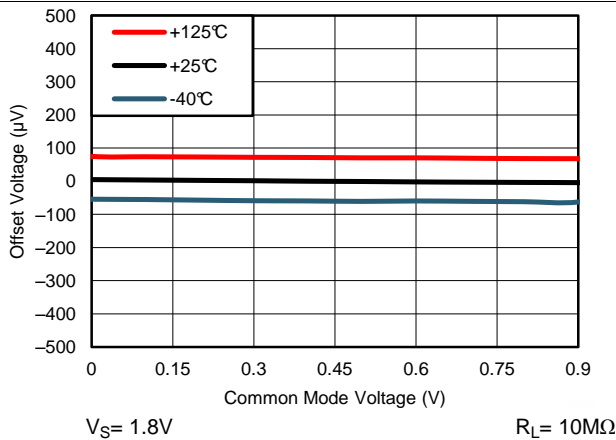


Figure 11. Typical Offset Voltage vs. Common Mode Voltage

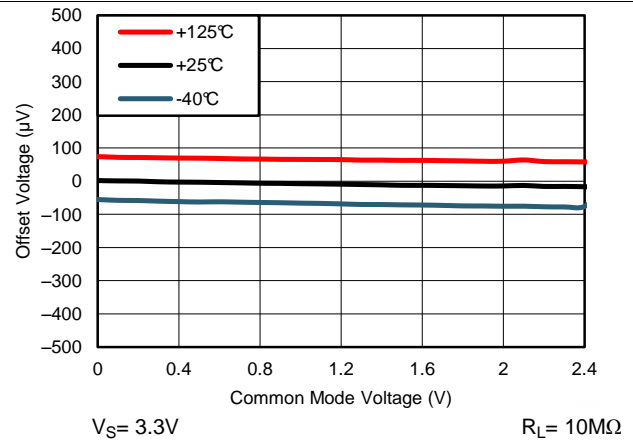


Figure 12. Typical Offset Voltage vs. Common Mode Voltage

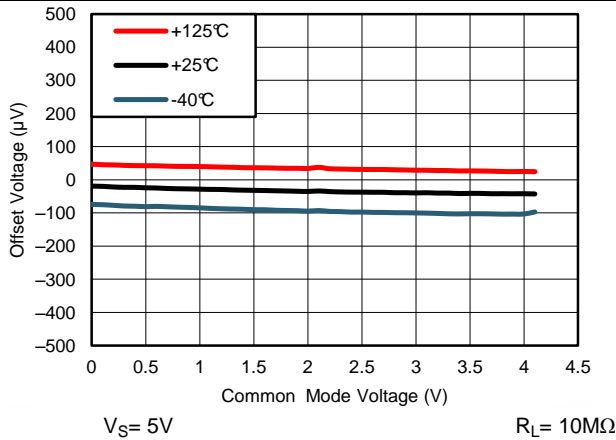


Figure 13. Typical Offset Voltage vs. Common Mode Voltage

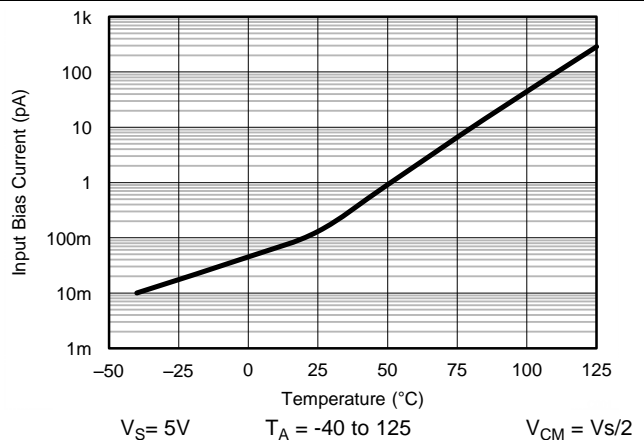
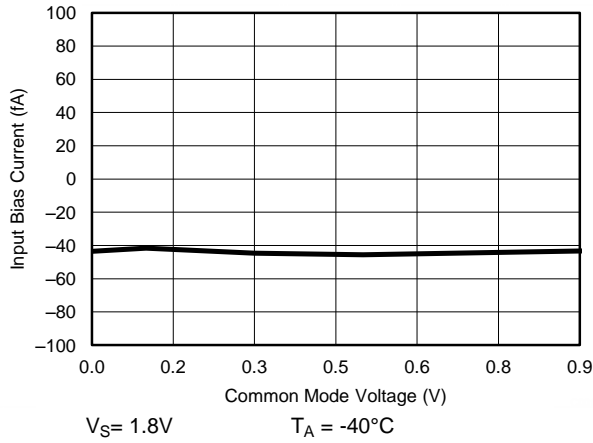


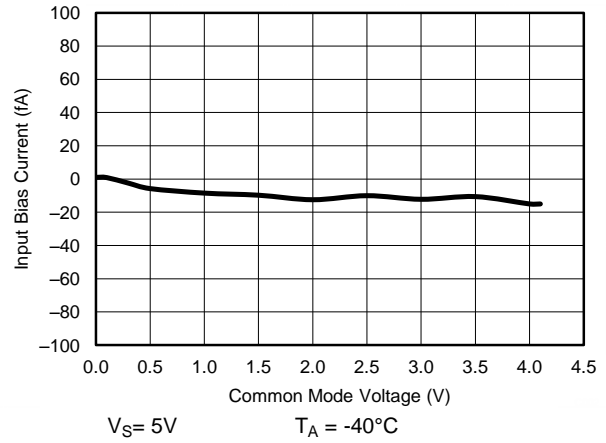
Figure 14. Input Bias Current vs. Temperature

**Typical Characteristics (continued)**

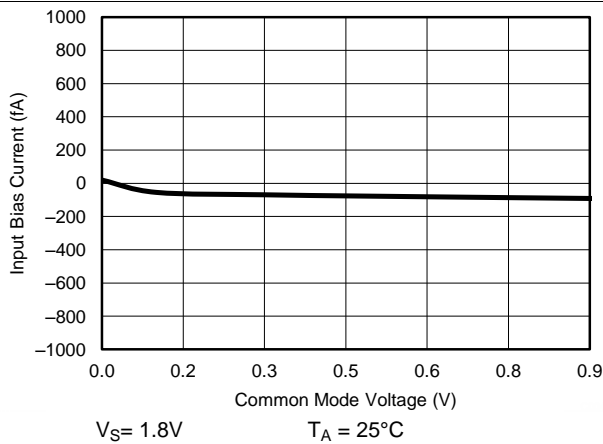
at  $T_A = 25^\circ\text{C}$ ,  $R_L = 10\text{M}\Omega$  to  $V_S/2$ ,  $C_L = 20\text{pF}$ ,  $V_{CM} = V_S / 2\text{V}$  unless otherwise specified.



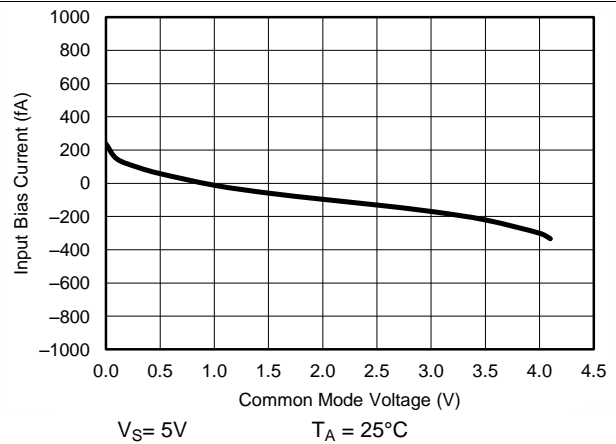
**Figure 15. Input Bias Current vs. Common Mode Voltage**



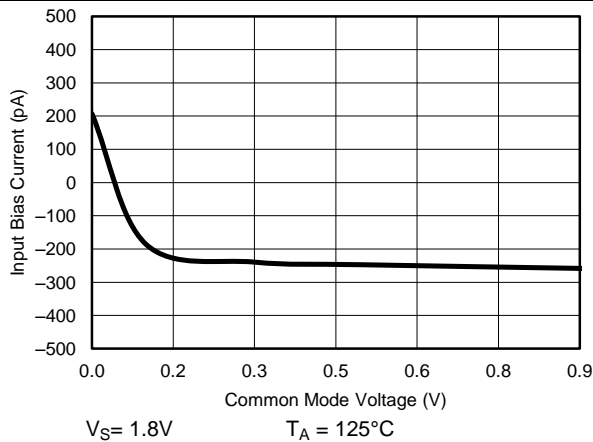
**Figure 16. Input Bias Current vs. Common Mode Voltage**



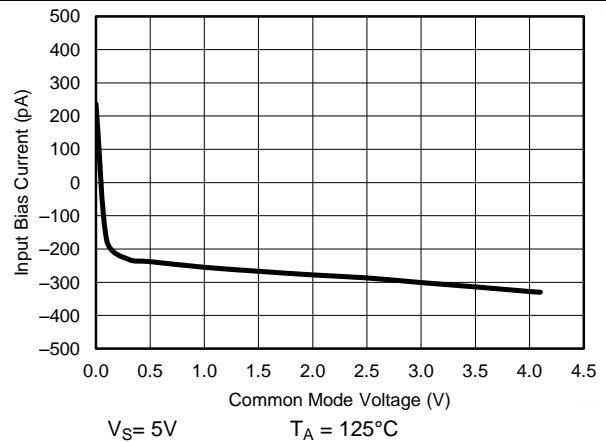
**Figure 17. Input Bias Current vs. Common Mode Voltage**



**Figure 18. Input Bias Current vs. Common Mode Voltage**



**Figure 19. Input Bias Current vs. Common Mode Voltage**

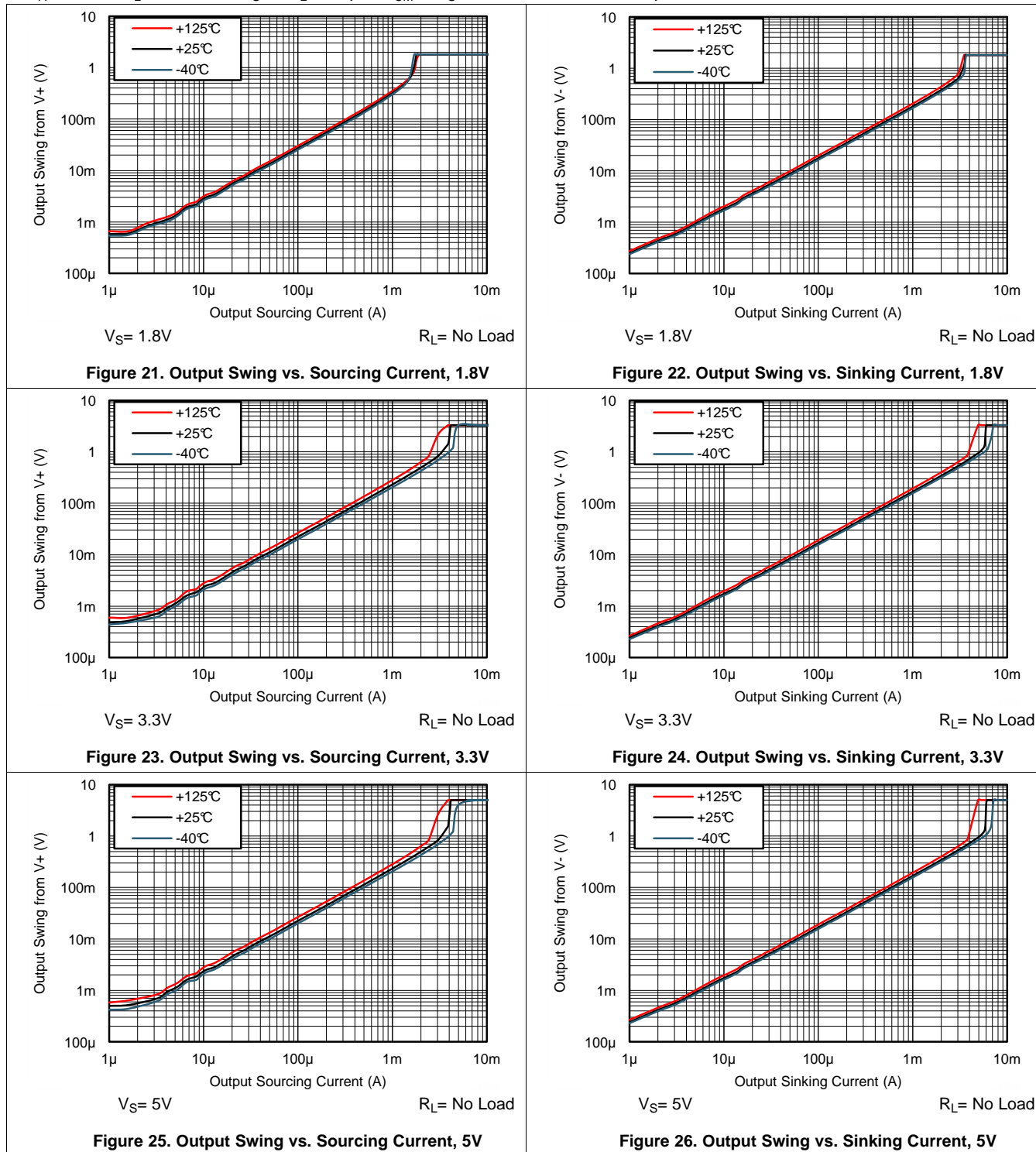


**Figure 20. Input Bias Current vs. Common Mode Voltage**



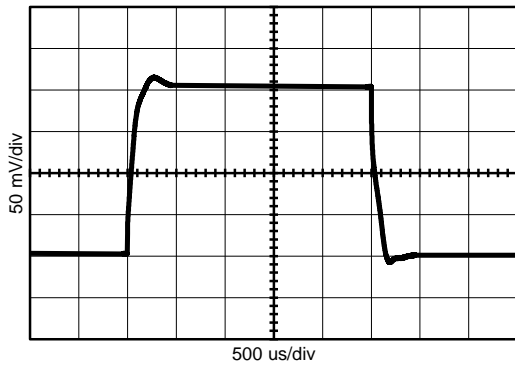
Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $R_L = 10\text{M}\Omega$  to  $V_S/2$ ,  $C_L = 20\text{pF}$ ,  $V_{CM} = V_S / 2\text{V}$  unless otherwise specified.



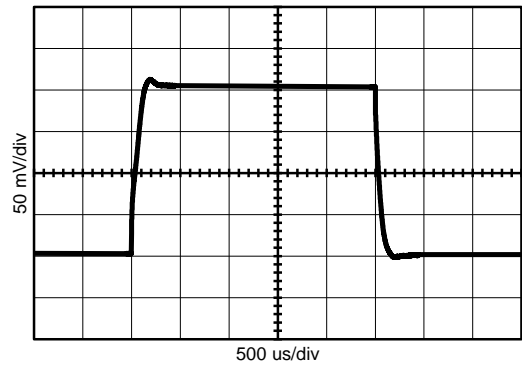
Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $R_L = 10\text{M}\Omega$  to  $V_S/2$ ,  $C_L = 20\text{pF}$ ,  $V_{CM} = V_S / 2\text{V}$  unless otherwise specified.



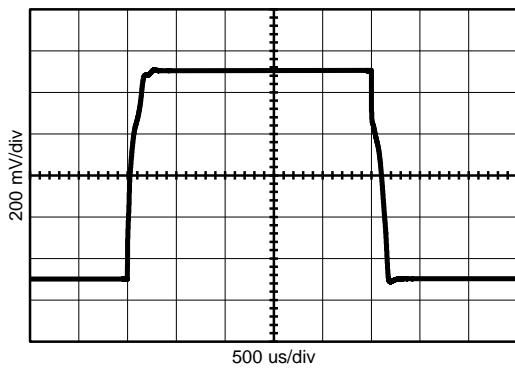
$T_A = 25$        $R_L = 10\text{M}\Omega$        $V_{out} = 200\text{mVpp}$   
 $V_S = \pm 0.9\text{V}$        $C_L = 20\text{pF}$        $A_V = +1$

Figure 27. Small Signal Pulse Response, 1.8V



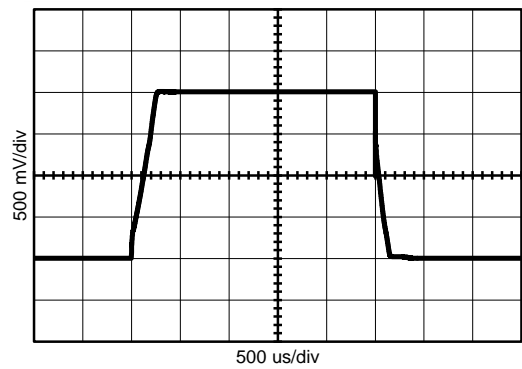
$T_A = 25$        $R_L = 10\text{M}\Omega$        $V_{out} = 200\text{mVpp}$   
 $V_S = \pm 2.5\text{V}$        $C_L = 20\text{pF}$        $A_V = +1$

Figure 28. Small Signal Pulse Response, 5V



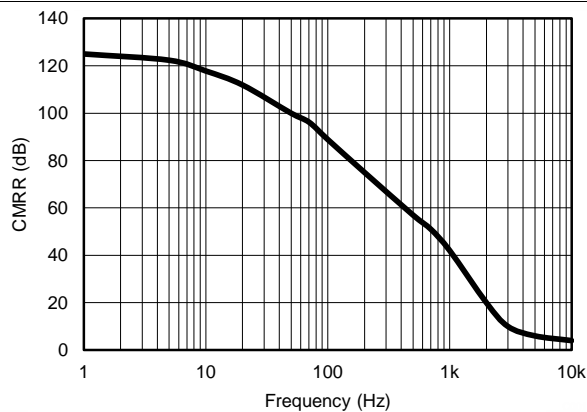
$T_A = 25$        $R_L = 10\text{M}\Omega$        $V_{out} = 1\text{Vpp}$   
 $V_S = \pm 0.9\text{V}$        $C_L = 20\text{pF}$        $A_V = +1$

Figure 29. Large Signal Pulse Response, 1.8V



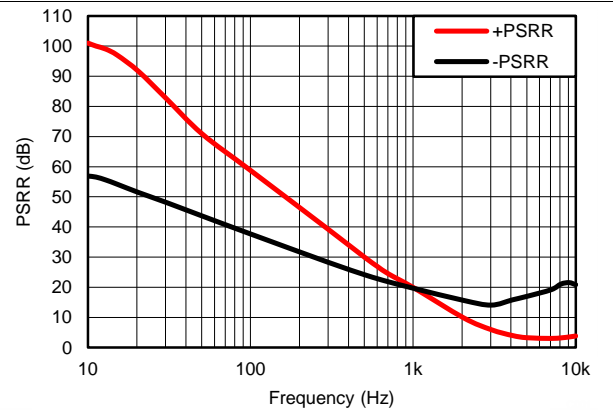
$T_A = 25$        $R_L = 10\text{M}\Omega$        $V_{out} = 2\text{Vpp}$   
 $V_S = \pm 2.5\text{V}$        $C_L = 20\text{pF}$        $A_V = +1$

Figure 30. Large Signal Pulse Response, 5V



$T_A = 25$        $R_L = 10\text{M}\Omega$        $\Delta V_{CM} = 0.5\text{Vpp}$   
 $V_S = 5\text{V}$        $C_L = 20\text{p}$   
 $V_{CM} = V_S/2$        $A_V = +1$

Figure 31. CMRR vs Frequency



$T_A = 25$        $R_L = 10\text{M}\Omega$        $\Delta V_S = 0.5\text{Vpp}$   
 $V_S = 3.3\text{V}$        $C_L = 20\text{p}$   
 $V_{CM} = V_S/2$        $A_V = +1$

Figure 32.  $\pm$ PSRR vs Frequency

Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $R_L = 10\text{M}\Omega$  to  $V_S/2$ ,  $C_L = 20\text{pF}$ ,  $V_{CM} = V_S / 2\text{V}$  unless otherwise specified.

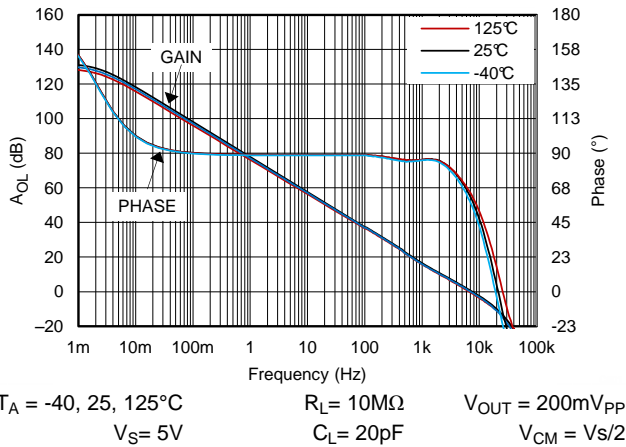


Figure 33. Open Loop Gain and Phase, 5V, 10 MΩ Load

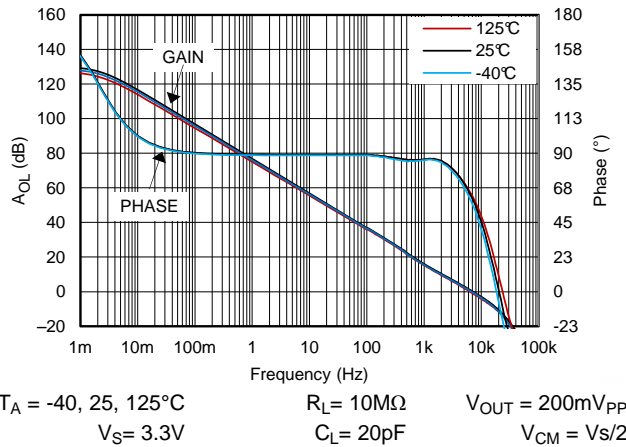


Figure 34. Open Loop Gain and Phase, 3.3V, 10 MΩ Load

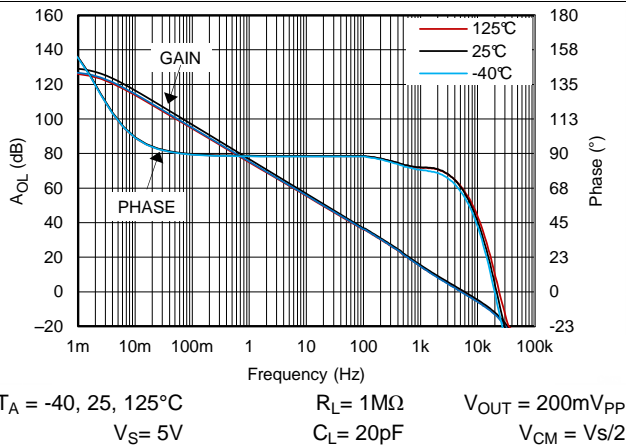


Figure 35. Open Loop Gain and Phase, 5V, 1 MΩ Load

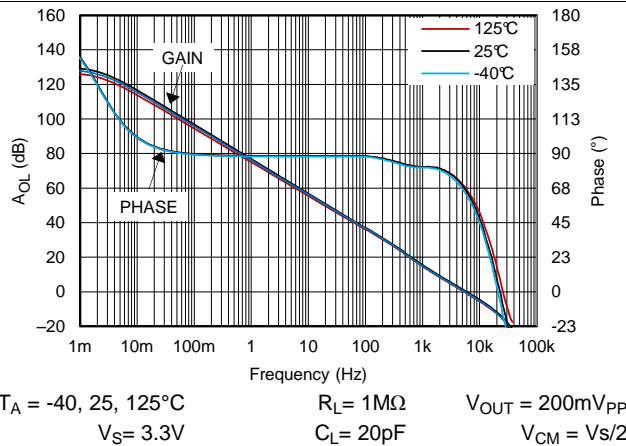


Figure 36. Open Loop Gain and Phase, 3.3V, 1 MΩ Load

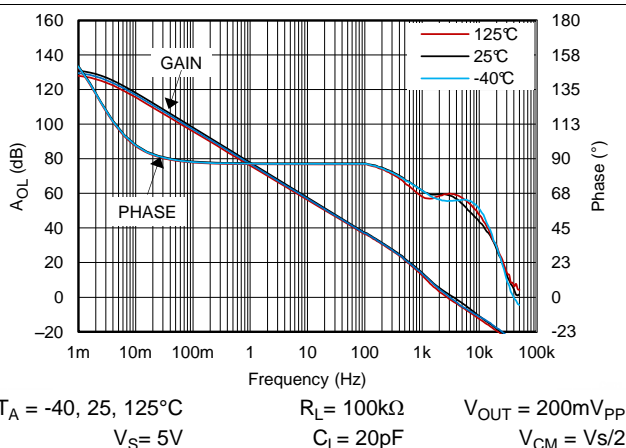


Figure 37. Open Loop Gain and Phase, 5V, 100kΩ Load

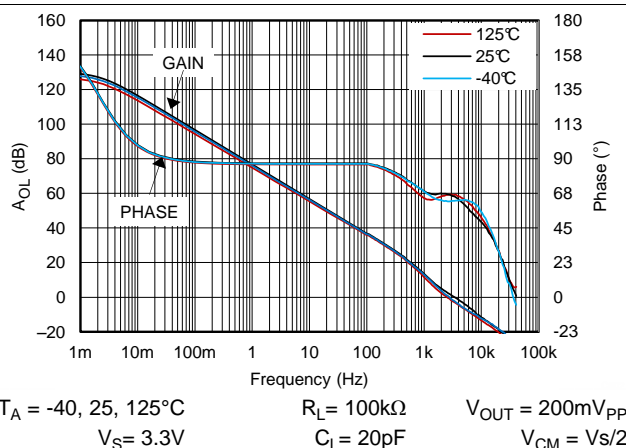
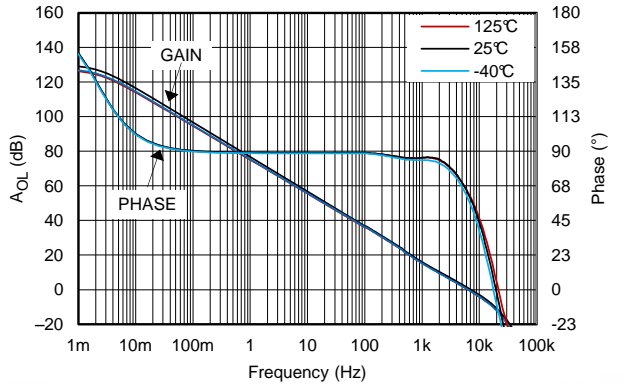


Figure 38. Open Loop Gain and Phase, 3.3V, 100kΩ Load

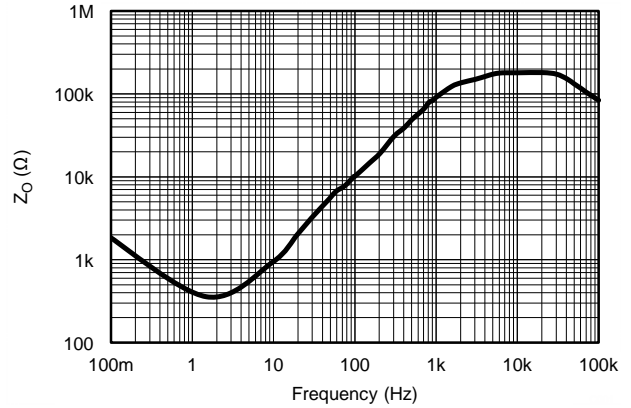
Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $R_L = 10\text{M}\Omega$  to  $V_S/2$ ,  $C_L = 20\text{pF}$ ,  $V_{CM} = V_S / 2\text{V}$  unless otherwise specified.



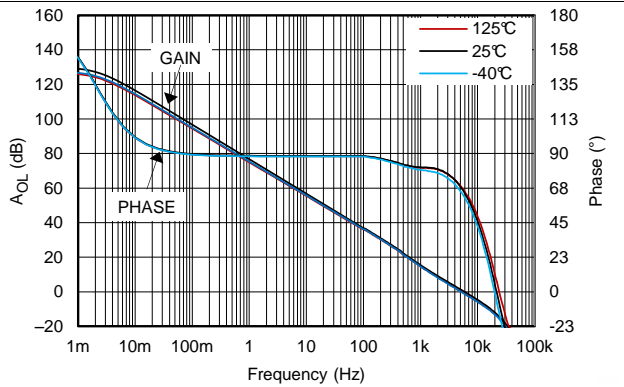
$T_A = -40, 25, 125^\circ\text{C}$   $R_L = 10\text{M}\Omega$   $V_{OUT} = 200\text{mV}_{PP}$   
 $V_S = 1.8\text{V}$   $C_L = 20\text{pF}$   $V_{CM} = V_S/2$

Figure 39. Open Loop Gain and Phase, 1.8V, 10 MΩ Load



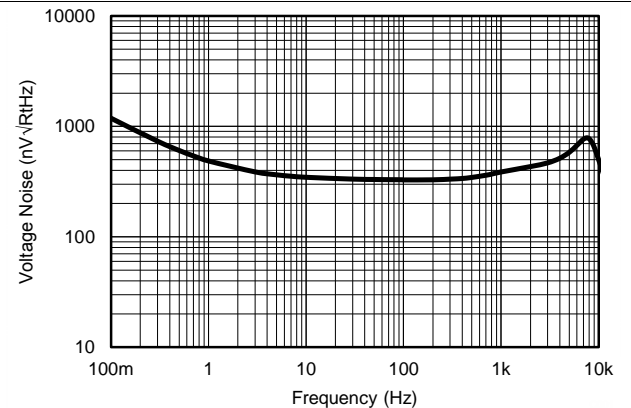
$T_A = 25^\circ\text{C}$   $V_S = 5\text{V}$   $R_L = 10\text{M}\Omega$

Figure 40. Open Loop Output Impedance



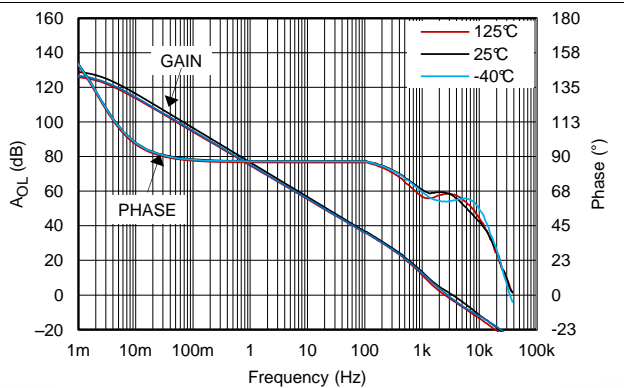
$T_A = -40, 25, 125^\circ\text{C}$   $R_L = 1\text{M}\Omega$   $V_{OUT} = 200\text{mV}_{PP}$   
 $V_S = 1.8\text{V}$   $C_L = 20\text{pF}$   $V_{CM} = V_S/2$

Figure 41. Open Loop Gain and Phase, 1.8V, 1 MΩ Load



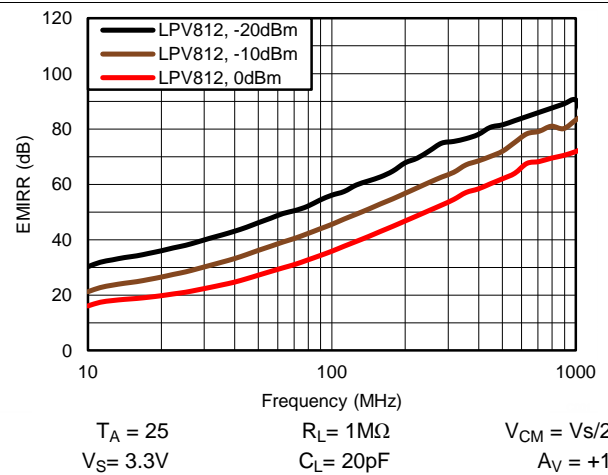
$T_A = 25$   $R_L = 1\text{M}\Omega$   $V_{CM} = V_S/2$   
 $V_S = 5\text{V}$   $C_L = 20\text{pF}$   $A_V = +1$

Figure 42. Input Voltage Noise vs Frequency



$T_A = -40, 25, 125^\circ\text{C}$   $R_L = 100\text{k}\Omega$   $V_{OUT} = 200\text{mV}_{PP}$   
 $V_S = 1.8\text{V}$   $C_L = 20\text{pF}$   $V_{CM} = V_S/2$

Figure 43. Open Loop Gain and Phase, 1.8V, 100kΩ Load



$T_A = 25$   $R_L = 1\text{M}\Omega$   $V_{CM} = V_S/2$   
 $V_S = 3.3\text{V}$   $C_L = 20\text{pF}$   $A_V = +1$

Figure 44. EMIRR Performance

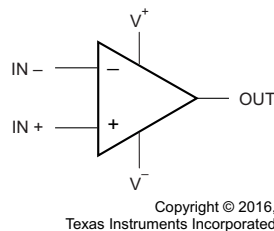
## 7 Detailed Description

### 7.1 Overview

The LPV811 (single) and LPV812 (dual) series of nanoPower CMOS operational amplifiers are designed for long-life battery-powered and energy harvested applications. They operate on a single supply with operation as low as 1.6V. The Input Offset is trimmed to less than 300uV and the output is rail-to-rail and swings to within 3.5mV of the supplies with a 100kΩ load. The common-mode range extends to the negative supply making it ideal for single-supply applications. EMI protection has been employed internally to reduce the effects of EMI.

Parameters that vary significantly with operating voltages or temperature are shown in the [Typical Characteristics](#) curves.

### 7.2 Functional Block Diagram



### 7.3 Feature Description

The amplifier's differential inputs consist of a non-inverting input (+IN) and an inverting input (–IN). The amplifier amplifies only the difference in voltage between the two inputs, which is called the differential input voltage. The output voltage of the op-amp  $V_{OUT}$  is given by [Equation 1](#):

$$V_{OUT} = A_{OL} (IN^+ - IN^-)$$

where

- $A_{OL}$  is the open-loop gain of the amplifier, typically around 120 dB (1,000,000x, or 1,000,000 Volts per microvolt).

(1)

### 7.4 Device Functional Modes

#### 7.4.1 Negative-Rail Sensing Input

The input common-mode voltage range of the LPV81x extends from (V-) to (V+) – 0.9 V. In this range, low offset can be expected with a minimum of 77dB CMRR. The LPV81x is protected from output "inversions" or "reversals".

#### 7.4.2 Rail to Rail Output Stage

The LPV81x output voltage swings 3.5 mV from rails at 1.8 V supply, which provides the maximum possible dynamic range at the output. This is particularly important when operating on low supply voltages.

The LPV81x Maximum Output Voltage Swing graph defines the maximum swing possible under a particular output load.

#### 7.4.3 Design Optimization for Nanopower Operation

When designing for ultra-low power, choose system feedback components carefully. To minimize quiescent current consumption, select large-value feedback resistors. Any large resistors will react with stray capacitance in the circuit and the input capacitance of the operational amplifier. These parasitic RC combinations can affect the stability of the overall system. A feedback capacitor may be required to assure stability and limit overshoot or gain peaking.

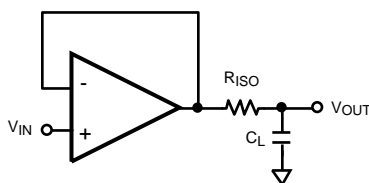
When possible, use AC coupling and AC feedback to reduce static current draw through the feedback elements. Use film or ceramic capacitors since large electrolytics may have large static leakage currents in the nanoamps.

## Device Functional Modes (continued)

### 7.4.4 Driving Capacitive Load

The LPV81x is internally compensated for stable unity gain operation, with a 8 kHz typical gain bandwidth. However, the unity gain follower is the most sensitive configuration to capacitive load. The combination of a capacitive load placed directly on the output of an amplifier along with the amplifier's output impedance creates a phase lag, which reduces the phase margin of the amplifier. If the phase margin is significantly reduced, the response will be under damped which causes peaking in the transfer and, when there is too much peaking, the op amp might start oscillating.

In order to drive heavy (>50pF) capacitive loads, an isolation resistor,  $R_{ISO}$ , should be used, as shown in Figure 45. By using this isolation resistor, the capacitive load is isolated from the amplifier's output. The larger the value of  $R_{ISO}$ , the more stable the amplifier will be. If the value of  $R_{ISO}$  is sufficiently large, the feedback loop will be stable, independent of the value of  $C_L$ . However, larger values of  $R_{ISO}$  result in reduced output swing and reduced output current drive. The recommended value for  $R_{ISO}$  is 30-50k $\Omega$ .



**Figure 45. Resistive Isolation Of Capacitive Load**

## 8 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

The LPV81x is a ultra-low power operational amplifier that provides 8 kHz bandwidth with only 425nA typical quiescent current, trimmed input offset voltage and precision drift specifications. These rail-to-rail output amplifiers are specifically designed for battery-powered applications. The input common-mode voltage range extends to the negative supply rail and the output swings to within millivolts of the rails, maintaining a wide dynamic range.

### 8.2 Typical Application: Three Terminal CO Gas Sensor Amplifier

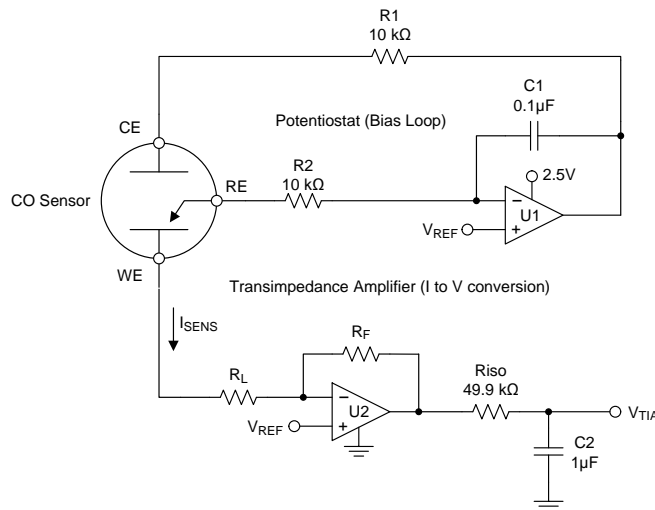


Figure 46. Three Terminal Gas Sensor Amplifier Schematic

#### 8.2.1 Design Requirements

Figure 46 shows a simple micropower potentiostat circuit for use with three terminal unbiased CO sensors, though it is applicable to many other type of three terminal gas sensors or electrochemical cells.

The basic sensor has three electrodes; The Sense or Working Electrode ("WE"), Counter Electrode ("CE") and Reference Electrode ("RE"). A current flows between the CE and WE proportional to the detected concentration.

The RE monitors the potential of the internal reference point. For an unbiased sensor, the WE and RE electrodes must be maintained at the same potential by adjusting the bias on CE. Through the Potentiostat circuit formed by U1, the servo feedback action will maintain the RE pin at a potential set by  $V_{REF}$ .

R1 is to maintain stability due to the large capacitance of the sensor. C1 and R2 form the Potentiostat integrator and set the feedback time constant.

U2 forms a transimpedance amplifier ("TIA") to convert the resulting sensor current into a proportional voltage. The transimpedance gain, and resulting sensitivity, is set by  $R_F$  according to Equation 2.

$$V_{TIA} = (-I * R_F) + V_{REF} \quad (2)$$

$R_L$  is a load resistor of which the value is normally specified by the sensor manufacturer (typically 10 ohms). The potential at WE is set by the applied  $V_{REF}$ . Riso provides capacitive isolation and, combined with C2, form the output filter and ADC reservoir capacitor to drive the ADC.

## Typical Application: Three Terminal CO Gas Sensor Amplifier (continued)

### 8.2.2 Detailed Design Procedure

For this example, we will be using a CO sensor with a sensitivity of 69nA/ppm. The supply voltage and maximum ADC input voltage is 2.5V, and the maximum concentration is 300ppm.

First the  $V_{REF}$  voltage must be determined. This voltage is a compromise between maximum headroom and resolution, as well as allowance for "footroom" for the minimum swing on the CE terminal, since the CE terminal generally goes negative in relation to the RE potential as the concentration (sensor current) increases. Bench measurements found the difference between CE and RE to be 180mV at 300ppm for this particular sensor.

To allow for negative CE swing "footroom" and voltage drop across the 10k resistor, 300mV was chosen for  $V_{REF}$ .

Therefore +300mV will be used as the minimum  $V_{ZERO}$  to add some headroom.

$$V_{ZERO} = V_{REF} = +300\text{mV}$$

where

- $V_{ZERO}$  is the zero concentration voltage
  - $V_{REF}$  is the reference voltage (300mV)
- (3)

Next we calculate the maximum sensor current at highest expected concentration:

$$I_{SENSMAX} = I_{PERPPM} * \text{ppmMAX} = 69\text{nA} * 300\text{ppm} = 20.7\mu\text{A}$$

where

- $I_{SENSMAX}$  is the maximum expected sensor current
  - $I_{PERPPM}$  is the manufacturer specified sensor current in Amps per ppm
  - ppmMAX is the maximum required ppm reading
- (4)

Now find the available output swing range above the reference voltage available for the measurement:

$$V_{SWING} = V_{OUTMAX} - V_{ZERO} = 2.5\text{V} - 0.3\text{V} = 2.2\text{V}$$

where

- $V_{SWING}$  is the expected change in output voltage
  - $V_{OUTMAX}$  is the maximum amplifier output swing (usually near V+)
- (5)

Now we calculate the transimpedance resistor ( $R_F$ ) value using the maximum swing and the maximum sensor current:

$$R_F = V_{SWING} / I_{SENSMAX} = 2.2\text{V} / 20.7\mu\text{A} = 106.28 \text{ k}\Omega \text{ (we will use } 110 \text{ k}\Omega \text{ for a common value)}$$
(6)



Typical Application: Three Terminal CO Gas Sensor Amplifier (continued)

8.2.3 Application Curve

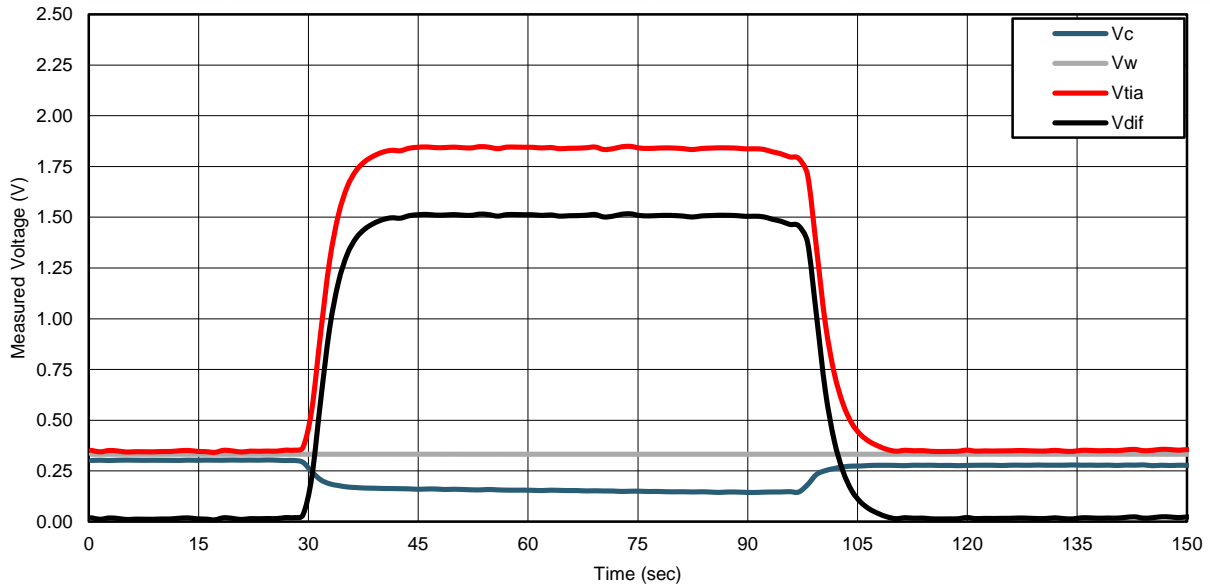


Figure 47. Monitored Voltages when exposed to 200ppm CO

Figure 47 shows the resulting circuit voltages when the sensor was exposed to 200ppm step of carbon monoxide gas.  $V_C$  is the monitored CE pin voltage and clearly shows the expected CE voltage dropping below the WE voltage,  $V_W$ , as the concentration increases.

$V_{TIA}$  is the output of the transimpedance amplifier U2.  $V_{DIFF}$  is the calculated difference between  $V_{REF}$  and  $V_{TIA}$ , which will be used for the ppm calculation.

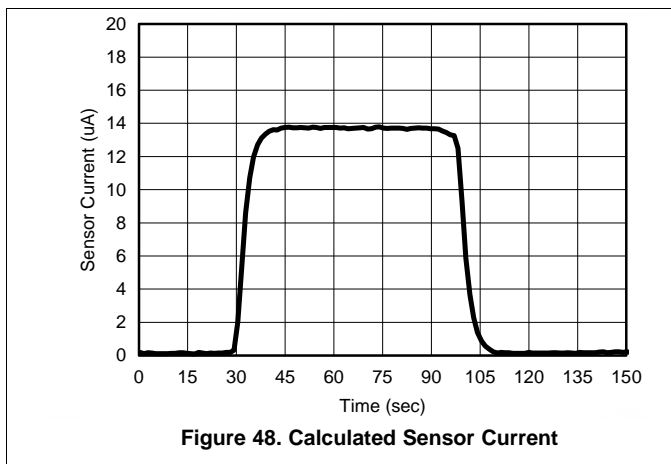


Figure 48. Calculated Sensor Current

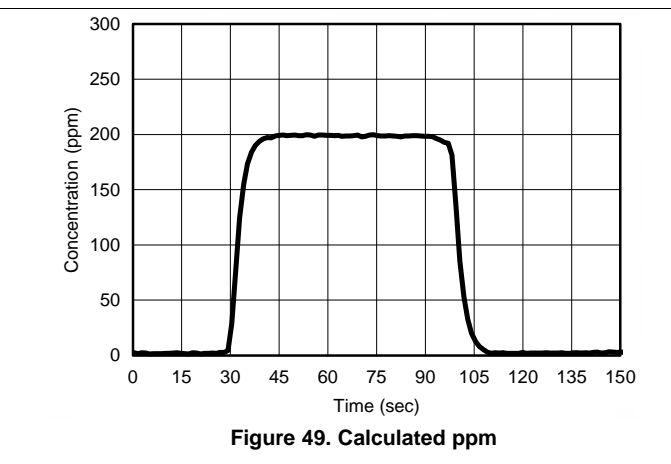


Figure 49. Calculated ppm

Figure 48 shows the calculated sensor current using the formula in Equation 7 :

$$I_{SENSOR} = V_{DIFF} / R_F = 1.52V / 110 \text{ k}\Omega = 13.8\mu A \tag{7}$$

Equation 8 shows the resulting conversion of the sensor current into ppm.

$$\text{ppm} = I_{SENSOR} / I_{PERPPM} = 13.8\mu A / 69nA = 200 \tag{8}$$

Total supply current for the amplifier section is less than 700 nA, minus sensor current. Note that the sensor current is sourced from the amplifier output, which in turn comes from the amplifier supply voltage. Therefore, any continuous sensor current must also be included in supply current budget calculations.

### 8.3 Do's and Don'ts

Do properly bypass the power supplies.

Do add series resistance to the output when driving capacitive loads, particularly cables, Muxes and ADC inputs.

Do add series current limiting resistors and external schottky clamp diodes if input voltage is expected to exceed the supplies. Limit the current to 1mA or less (1K $\Omega$  per volt).

## 9 Power Supply Recommendations

The LPV81x is specified for operation from 1.6 V to 5.5 V ( $\pm 0.8$  V to  $\pm 2.75$  V) over a  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  temperature range. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the [Typical Characteristics](#).

### CAUTION

Supply voltages larger than 6 V can permanently damage the device.

For proper operation, the power supplies must be properly decoupled. For decoupling the supply lines it is suggested that 100 nF capacitors be placed as close as possible to the operational amplifier power supply pins. For single supply, place a capacitor between  $V^+$  and  $V^-$  supply leads. For dual supplies, place one capacitor between  $V^+$  and ground, and one capacitor between  $V^-$  and ground.

Low bandwidth nanopower devices do not have good high frequency ( $> 1$  kHz) AC PSRR rejection against high-frequency switching supplies and other 1 kHz and above noise sources, so extra supply filtering is recommended if kilohertz or above noise is expected on the power supply lines.

## 10 Layout

### 10.1 Layout Guidelines

The  $V^+$  pin should be bypassed to ground with a low ESR capacitor.

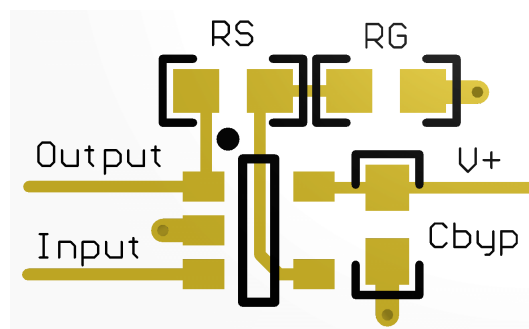
The optimum placement is closest to the  $V^+$  and ground pins.

Care should be taken to minimize the loop area formed by the bypass capacitor connection between  $V^+$  and ground.

The ground pin should be connected to the PCB ground plane at the pin of the device.

The feedback components should be placed as close to the device as possible to minimize strays.

### 10.2 Layout Example



**Figure 50. SOT-23 Layout Example (Top View)**

## 11 デバイスおよびドキュメントのサポート

### 11.1 デバイス・サポート

#### 11.1.1 開発サポート

[TINA-TI SPICEベースのアナログ・シミュレーション・プログラム](#)

[DIP アダプタ評価モジュール](#)

[TIユニバーサル・オペアンプ評価モジュール](#)

[TI FilterProフィルタ設計ソフトウェア](#)

### 11.2 ドキュメントのサポート

#### 11.2.1 関連資料

関連資料については、以下を参照してください。

- 『AN-1798 電気化学的センサを使用した設計』
- 『AN-1803 トランスインピーダンス・アンプ設計の考慮事項』
- 『AN-1852 pH電極を使用した設計』
- 『トランスインピーダンス・アンプの直感的な補正』
- 『高速オペアンプのトランスインピーダンスの考慮事項』
- 『FETトランスインピーダンス・アンプのノイズ解析』
- 『基板のレイアウト技法』
- 『オペアンプ・アプリケーション・ハンドブック』

### 11.3 関連リンク

次の表に、クイック・アクセス・リンクを示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびサンプル注文またはご購入へのクイック・アクセスが含まれます。

表 1. 関連リンク

製品	プロダクト・フォルダ	サンプルとご購入	技術資料	ツールとソフトウェア	サポートとコミュニティ
LPV811	<a href="#">ここをクリック</a>	<a href="#">ここをクリック</a>	<a href="#">ここをクリック</a>	<a href="#">ここをクリック</a>	<a href="#">ここをクリック</a>
LPV812	<a href="#">ここをクリック</a>	<a href="#">ここをクリック</a>	<a href="#">ここをクリック</a>	<a href="#">ここをクリック</a>	<a href="#">ここをクリック</a>

### 11.4 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[ti.com](http://ti.com)のデバイス製品フォルダを開いてください。右上の隅にある「通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

### 11.5 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 11.6 商標

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

## 11.7 静電気放電に関する注意事項



これらのデバイスは、限定的なESD(静電破壊)保護機能を内蔵しています。保存時または取り扱い時は、MOSゲートに対する静電破壊を防止するために、リード線同士をショートさせておくか、デバイスを導電フォームに入れる必要があります。

## 11.8 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LPV811DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	15TM	<a href="#">Samples</a>
LPV811DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	15TM	<a href="#">Samples</a>
LPV812DGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG   SN	Level-1-260C-UNLIM	-40 to 125	LPV 812	<a href="#">Samples</a>
LPV812DGKT	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	NIPDAUAG   SN	Level-1-260C-UNLIM	-40 to 125	LPV 812	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LPV811DBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LPV811DBVT	SOT-23	DBV	5	250	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LPV812DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LPV812DGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LPV811DBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
LPV811DBVT	SOT-23	DBV	5	250	208.0	191.0	35.0
LPV812DGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
LPV812DGKT	VSSOP	DGK	8	250	366.0	364.0	50.0





# EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# DGK0008A



# PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4214862/A 04/2023

**NOTES:**

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

# EXAMPLE BOARD LAYOUT

DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 15X



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

# EXAMPLE STENCIL DESIGN

DGK0008A

<sup>TM</sup> VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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