TEXAS INSTRUMENTS
OPA835, OPA2835
JAJSLI5J – JANUARY 2011 – REVISED MARCH 2021

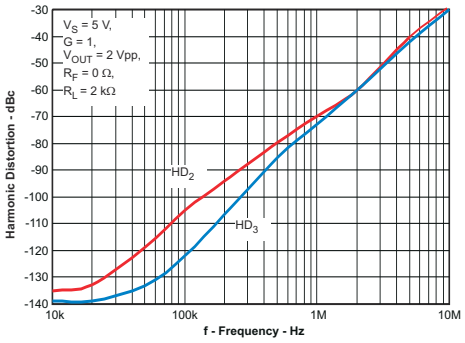
OPAx835 超低消費電力、レール・ツー・レール出力、負電源入力、VFB オペアンプ

1 特長

- 超低消費電力
  - 電源電圧:2.5V～5.5V
  - 静止電流:250µA/チャネル (標準値)
  - パワーダウン・モード:0.5µA (標準値)
- 帯域幅:56MHz (A_V = 1V/V)
- スルーレート:160V/µs
- 立ち上がり時間:10ns ($2V_{STEP}$)
- セトリング・タイム(0.1%):55ns ($2V_{STEP}$)
- オーバードライブ復帰時間:200ns
- SNR:0.00015% (-116.4dBc) (1kHz、$1V_{RMS}$ 時)
- THD:0.00003% (-130dBc) (1kHz、$1V_{RMS}$ 時)
- HD_2/HD_3:-70dBc/-73dBc (1MHz、$2V_{PP}$ 時)
- 入力電圧ノイズ:9.3nV/√Hz (f = 100kHz)
- 入力オフセット電圧:100µV (最大 ±500µV)
- CMRR:113dB
- 出力電流駆動能力:40mA
- RRO:レール・ツー・レール出力
- 入力電圧範囲:-0.2V～3.9V
  (5V 電源)
- 動作温度範囲:
  –40°C～+125°C

2 アプリケーション

- 低消費電力のシグナル・コンディショニング
- オーディオ用 A/D コンバータの入力バッファ
- 低消費電力の SAR および ΔΣ ADC ドライバ
- ポータブル・システム
- 低消費電力システム
- 高密度システム
- 超音波流量計



高調波歪みと周波数との関係

3 概要

OPA835 および OPA2835 デバイス (OPAx835) は、シングルおよびデュアルの超低消費電力、レール・ツー・レール出力、負レール入力、電圧帰還 (VFB) オペアンプで、単一電源で 2.5V～5.5V、デュアル電源で ±1.25V～±2.75V の電源電圧範囲で動作するよう設計されています。チャネルあたり 250µA の消費電力と 56MHz のユニティ・ゲイン帯域幅により、これらのアンプは、レール・ツー・レール・アンプに関して業界最高レベルの電力性能比を実現します。

消費電力が重視されるバッテリ駆動式の携帯機器において、消費電力が小さく高周波性能に優れた OPA835 および OPA2835 デバイスは、他のデバイスでは達成できない電力性能比を実現します。電流を 1.5µA 未満に低減する省電力モードも備えているため、バッテリ駆動機器の高周波アンプに最適です。

OPA835 RUN パッケージ・オプションはゲイン設定抵抗を内蔵しているため、プリント基板の占有面積を最小限 (約 2.00mm × 2.00mm) に抑えることができます。PCB に回路トレースを追加することにより、+1、–1、–1.33、+2、+2.33、–3、+4、–4、+5、–5.33、+6.33、–7、+8 のゲインと –0.1429、–0.1875、–0.25、–0.33、–0.75 の反転減衰を実現できます。詳細は、表 9-1 および 表 9-2 をご覧ください。

OPA835 および OPA2835 デバイスは、–40°C～+125°C の拡張産業用温度範囲全体にわたって動作が規定されています。

製品情報 (1)

部品番号	パッケージ	本体サイズ (公称)
OPA835	SOT-23 (6)	2.90mm × 1.60mm
	QFN (10)	2.00mm × 2.00mm
OPA2835	SOIC (8)	4.90mm × 3.91mm
	VSSOP (10)	3.00mm × 3.00mm
	UQFN (10)	2.00mm × 2.00mm
	QFN (10)	2.00mm × 2.00mm

(1) 利用可能なすべてのパッケージについて、このデータシートの末尾にあるパッケージ・オプションについての付録を参照してください。

Table of Contents

4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision I (August 2016) to Revision J (March 2021) — **Page**

- 文書全体にわたって表、図、相互参照の採番方法を更新 ... 1
- Changed the input impedance common-mode typical test condition from 200 || 1.2 kΩ || pF to 250 || 1.2 MΩ || pF ... 7
- Changed the input impedance common-mode typical test condition from 200 || 1.2 kΩ || pF to 250 || 1.2 MΩ || pF ... 10

Changes from Revision H (November 2015) to Revision I (August 2016) — **Page**

- Reformatted table note on *Thermal Information: OPA835* and *Thermal Information: OPA2835* tables ... 6
- Deleted the word "linear" from output voltage low, output voltage high, and output current drive parameters in *Electrical Characteristics: V_S = 2.7 V* table ... 7
- Changed Current noise 1/f corner frequency parameter units from Hz to kHz in *Electrical Characteristics: V_S = 5 V* table ... 10
- Deleted the word "linear" from output voltage low, output voltage high, and output current drive parameters in *Electrical Characteristics: V_S = 5 V* table ... 10
- Reformatted *Development Support* section ... 42
- Reformatted *Related Documentation* section ... 42

Changes from Revision G (June 2015) to Revision H (November 2015) — **Page**

- Changed package designator from DMC to RMC (typo) ... 4
- Changed text in first paragraph of *Power-Down Operation* section ... 24

Changes from Revision F (June 2015) to Revision G (June 2015) — **Page**

- Moved all switching parameters from the *Switching Characteristics: V_S = 2.7 V* back into the *Electrical Characteristics: V_S = 2.7 V* table ... 7
- Moved all switching parameters from the *Switching Characteristics: V_S = 5 V* table back into the *Electrical Characteristics: V_S = 5 V* table ... 10

Changes from Revision E (July 2013) to Revision F (June 2015) **Page**

- 「*ピン構成および機能*」セクション、「*ESD*」表、「*スイッチング特性*」表、「*機能説明*」セクション、「*デバイスの機能モード*」、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクションを追加。 1
- Moved the switching parameters from the *Electrical Characteristics* tables into *Switching Characteristics* tables 10

Changes from Revision D (October 2011) to Revision E (July 2013) **Page**

- ドキュメントに RMC パッケージを追加 1
- Added RMC to *Thermal Information* table 6

Changes from Revision C (September 2011) to Revision D (September 2011) **Page**

- Removed Product Preview from OPA835IRUNT and OPA835IRUNR 4
- Changed Resistor temperature coefficient typical value from TBD to < 10 7
- "Changed Quiescent operating current" parameter to "Quiescent operating current per amplifier" 7
- Changed Resistor temperature coefficient parameter units from TBD to < 10 10
- Changed Quiescent operating current parameter to Quiescent operating current per amplifer 10

Changes from Revision B (May 2011) to Revision C (August 2011) **Page**

- Removed Product Preview from all devices except OPA835IRUNT and OPA835IRUNR 4
- Changed - Channel to channel crosstalk (OPA2835) typical value from TBD to –120 dB 7
- Changed the Common-mode rejection ratio minimum value from 91 dB to 88 dB 7
- Added GAIN-SETTING RESISTORS (OPA835IRUN ONLY) parameter 7
- Changed the Quiescent operating current per amplifier(T_A = 25°C) parameter minimum value from190 µA to 175 µA 7
- Changed the Power supply rejection (±PSRR) minimum value from 91 dB to 88 dB 7
- Changed the Power-down pin bias current test conditions from $\overline{PD}$ = 0.7 V to $\overline{PD}$ = 0.5 V 7
- Changed the Power-down quiescent current test conditions from $\overline{PD}$ = 0.7 V to $\overline{PD}$ = 0.5 V 7
- Changed Channel to channel crosstalk (OPA2835) typical value from TBD to -120 dB 10
- Changed the common-mode rejection ratio minimum value from 94 dB to 91 dB 10
- Added GAIN-SETTING RESISTORS (OPA835IRUN ONLY) parameter 10
- Changed the Quiescent operating current (T_A = 25°C) Min value From: 215 µA To: 200 µA 10
- Changed the Power supply rejection (±PSRR) minimum value from 93 dB to 90 dB 10
- Changed the Power-down quiescent current test conditions from $\overline{PD}$ = 0.7 V to $\overline{PD}$ = 0.5 V 10
- Changed the Power-down quiescent current test conditions from $\overline{PD}$ = 0.7 V to $\overline{PD}$ = 0.5 V 10
- Added Figure Crosstalk vs Frequency 13
- Added Figure Crosstalk vs Frequency 18
- Added *Single-Ended to Differential Amplifier* section 30

Changes from Revision A (March 2011) to Revision B (May 2011) **Page**

- OPA835 を製品プレビューから生産データに変更 1

5 Device Comparision Table

PART NUMBER	BW (A_V = 1) MHz	SLEW RATE V/µsec	Iq (+5 V) mA	INPUT NOISE nV/√Hz	RAIL-TO-RAIL IN/OUT	DUALS
OPA835	30	110	0.25	9.3	–VS/Out	OPA2835
OPA365	50	25	5	4.5	In/Out	OPA2365
THS4281	95	35	0.75	12.5	In/Out	
LMH6618	140	45	1.25	10	In/Out	LMH6619
OPA836	205	560	1	4.6	–VS/Out	OPA2836
OPA830	310	600	3.9	9.5	–VS/Out	OPA2830

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6 Pin Configuration and Functions

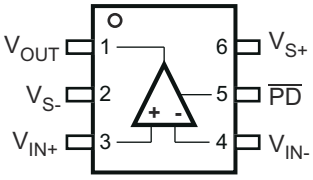


図 6-1. OPA835: DBV Package 6-Pin SOT-23 Top View

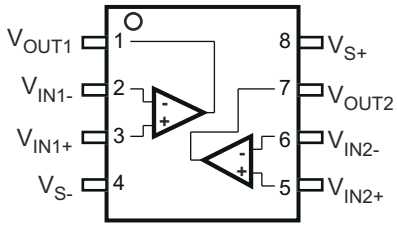


図 6-2. OPA2835: D Package 8-Pin SOIC Top View

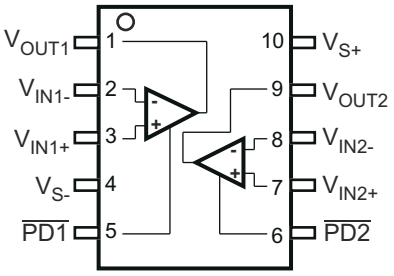


図 6-3. OPA2835: DGS Package 10-Pin VSSOP Top View

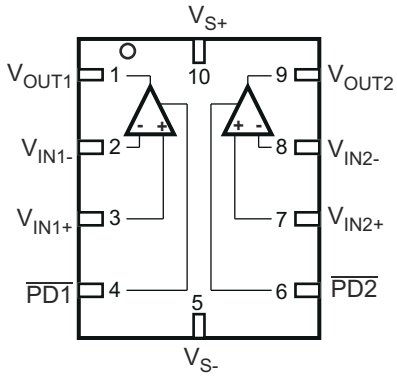


図 6-4. OPA2835: RMC and RUN Packages 10-Pin UQFN and 10-Pin QFN Top View

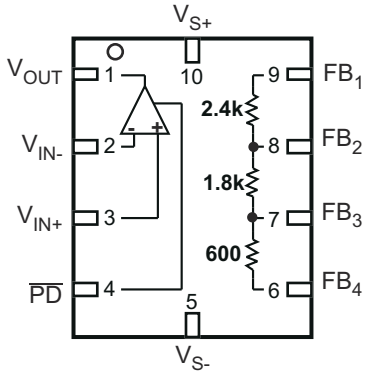


図 6-5. OPA835: RUN Package 10-Pin QFN Top View

表 6-1. Pin Functions

PIN						I/O	DESCRIPTION
NAME	OPA835		OPA2835				
	SOT-23	QFN	SOIC	VSSOP	QFN, UQFN		
FB_1	—	9	—	—	—	I/O	Connection to top of 2.4-kΩ internal gain-setting resistors
FB_2		8				I/O	Connection to junction of 1.8-kΩ and 2.4-kΩ internal gain-setting resistors
FB_3		7				I/O	Connection to junction of 600-Ω and 1.8-kΩ internal gain-setting resistors
FB_4		6				I/O	Connection to bottom of 600-Ω internal gain-setting resistors
$\overline{PD}$	5	4				I	Amplifier Power Down, low = low-power mode, high = normal operation **(PIN MUST BE DRIVEN)**
$\overline{PD1}$	—	—		5	4	I	Amplifier 1 Power Down, low = low-power mode, high = normal operation **(PIN MUST BE DRIVEN)**
$\overline{PD2}$				6	6	I	Amplifier 2 Power Down, low = low-power mode, high = normal operation **(PIN MUST BE DRIVEN)**
V_{IN+}	3	3		—	—	I	Amplifier noninverting input
$V_{IN–}$	4	2				I	Amplifier inverting input
V_{IN1+}	—	—	3	3	3	I	Amplifier 1 noninverting input
$V_{IN1–}$			2	2	2	I	Amplifier 1 inverting input
V_{IN2+}			5	7	7	I	Amplifier 2 noninverting input
$V_{IN2–}$			6	8	8	I	Amplifier 2 inverting input
V_{OUT}	1	1	—	—	—	O	Amplifier output
V_{OUT1}	—	—	1	1	1	O	Amplifier 1 output
V_{OUT2}			7	9	9	O	Amplifier 2 output
V_{S+}	6	10	8	10	10	POW	Positive power supply input
$V_{S–}$	2	5	4	4	5	POW	Negative power supply input

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
$V_{S–}$ to V_{S+}	Supply voltage		5.5	V
V_I	Input voltage	$V_{S–}$ – 0.7	V_{S+} + 0.7	V
V_{ID}	Differential input voltage		1	V
I_I	Continuous input current		0.85	mA
I_O	Continuous output current		60	mA
	Continuous power dissipation	See セクション 7.4 and セクション 7.5		
T_J	Maximum junction temperature		150	°C
T_A	Operating free-air temperature	–40	125	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±6000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	
		Machine model	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{S+}	Single supply voltage	2.5	5	5.5	V
T_A	Ambient temperature	–40	25	125	°C

7.4 Thermal Information: OPA835

THERMAL METRIC(1)		OPA835		UNIT
		DBV (SOT23-6)	RUN (QFN)	
		6 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	194	145.8	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	129.2	75.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	39.4	38.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	25.6	13.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	38.9	104.5	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics* (SPRA953).

7.5 Thermal Information: OPA2835

THERMAL METRIC[1]		OPA2835				UNIT
		D (SOIC)	DGS (VSSOP)	RUN (QFN)	RMC (UQFN)	
		8 PINS	10 PINS	10 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	150.1	206	145.8	143.2	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	83.8	75.3	75.1	49.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	68.4	96.2	38.9	61.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	33.0	12.9	13.5	3.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	67.9	94.6	104.5	61.9	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics* (SPRA953).

7.6 Electrical Characteristics: V_S = 2.7 V

at V_{S+} = +2.7 V, $V_{S–}$ = 0 V, V_{OUT} = 1 V_{PP}, R_F = 0 Ω, R_L = 2 kΩ, G = 1 V/V, input and output referenced to mid-supply, V_{IN_CM} = mid-supply – 0.5 V. T_A = 25°C, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL[1]
AC PERFORMANCE						
Small-signal bandwidth	V_{OUT} = 100 mV_{PP}, G = 1		51		MHz	C
	V_{OUT} = 100 mV_{PP}, G = 2		22.5			
	V_{OUT} = 100 mV_{PP}, G = 5		7.2			
	V_{OUT} = 100 mV_{PP}, G = 10		3			
Gain-bandwidth product	V_{OUT} = 100 mV_{PP}, G = 10		30		MHz	C
Large-signal bandwidth	V_{OUT} = 1 V_{PP}, G = 1		24		MHz	C
Bandwidth for 0.1-dB flatness	V_{OUT} = 1 V_{PP}, G = 2		4		MHz	C
Slew rate, rise	V_{OUT} = 1 V_{STEP}, G = 2		110		V/µs	C
Slew rate, fall	V_{OUT} = 1 V_{STEP}, G = 2		130		V/µs	C
Rise time	V_{OUT} = 1 V_{STEP}, G = 2		9.5		ns	C
Fall time	V_{OUT} = 1 V_{STEP}, G = 2		9		ns	C
Settling time to 1%, rise	V_{OUT} = 1 V_{STEP}, G = 2		35		ns	C
Settling time to 1%, fall	V_{OUT} = 1 V_{STEP}, G = 2		30		ns	C
Settling time to 0.1%, rise	V_{OUT} = 1 V_{STEP}, G = 2		60		ns	C
Settling time to 0.1%, fall	V_{OUT} = 1 V_{STEP}, G = 2		65		ns	C
Settling time to 0.01%, rise	V_{OUT} = 1 V_{STEP}, G = 2		120		ns	C
Settling time to 0.01%, rise	V_{OUT} = 1 V_{STEP}, G = 2		90		ns	C
Overshoot/Undershoot	V_{OUT} = 1 V_{STEP}, G = 2		0.5%/0.2%			C
Second-order harmonic distortion	f = 10 kHz, V_{IN_CM} = mid-supply – 0.5 V		–133		dBc	C
	f = 100 kHz, V_{IN_CM} = mid-supply – 0.5 V		–110			
	f = 1 MHz, V_{IN_CM} = mid-supply – 0.5 V		–73			
Third-order harmonic distortion	f = 10 kHz, V_{IN_CM} = mid-supply – 0.5 V		–137		dBc	C
	f = 100 kHz, V_{IN_CM} = mid-supply – 0.5 V		–125			
	f = 1 MHz, V_{IN_CM} = mid-supply – 0.5 V		–78			
Second-order intermodulation distortion	f = 1 MHz, 200-kHz Tone Spacing, V_{OUT} Envelope = 1 V_{PP}, V_{IN_CM} = mid-supply – 0.5 V		–75		dBc	C
Third-order intermodulation distortion	f = 1 MHz, 200-kHz Tone Spacing, V_{OUT} Envelope = 1 V_{PP}, V_{IN_CM} = mid-supply – 0.5 V		–81		dBc	C
Input voltage noise	f = 100 kHz		9.3		nV/√Hz	C
Voltage noise 1/f corner frequency			147		Hz	C

7.6 Electrical Characteristics: V_S = 2.7 V (continued)

at V_{S+} = +2.7 V, $V_{S–}$ = 0 V, V_{OUT} = 1 V_{PP}, R_F = 0 Ω, R_L = 2 kΩ, G = 1 V/V, input and output referenced to mid-supply, V_{IN_CM} = mid-supply – 0.5 V. T_A = 25°C, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL(1)
AC PERFORMANCE (continued)						
Input current noise	f = 1 MHz		0.45		pA/√Hz	C
Current noise 1/f corner frequency			14.7		kHz	C
Overdrive recovery time, over/under	Overdrive = 0.5 V		140/125		ns	C
Closed-loop output impedance	f = 100 kHz		0.028		Ω	C
Channel-to-channel crosstalk (OPA2835)	f = 10 kHz		–120		dB	C
DC PERFORMANCE						
Open-loop voltage gain (A_{OL})		100	120		dB	A
Input referred offset voltage	T_A = 25°C	–500	±100	500	μV	A
	T_A = 0°C to 70°C	–880		880		B
	T_A = –40°C to 85°C	–1040		1040		
	T_A = –40°C to 125°C	–1850		1850		
Input offset voltage drift(3)	T_A = 0°C to 70°C	–8.5	±1.4	8.5	μV/°C	B
	T_A = –40°C to 85°C	–9	±1.5	9		
	T_A = –40°C to 125°C	–13.5	±2.25	13.5		
Input bias current(2)	T_A = 25°C	50	200	400	nA	A
	T_A = 0°C to 70°C	47		410		B
	T_A = –40°C to 85°C	45		425		
	T_A = –40°C to 125°C	45		530		
Input bias current drift(3)	T_A = 0°C to 70°C	–1.4	±0.25	1.4	nA/°C	B
	T_A = –40°C to 85°C	–1.05	±0.175	1.05		
	T_A = –40°C to 125°C	–1.1	±0.185	1.1		
Input offset current	T_A = 25°C	–100	±13	100	nA	A
	T_A = 0°C to 70°C	–100	±13	100		B
	T_A = –40°C to 85°C	–100	±13	100		
	T_A = –40°C to 125°C	–100	±13	100		
Input offset current drift(3)	T_A = 0°C to 70°C	–1.230	±0.205	1.230	nA/°C	B
	T_A = –40°C to 85°C	–0.940	±0.155	0.940		
	T_A = –40°C to 125°C	–0.940	±0.155	0.940		
INPUT						
Common-mode input range low	T_A = 25°C, < 3 dB degradation in CMRR limit		–0.2	0	V	A
	T_A = –40°C to 125°C, < 3-dB degradation in CMRR limit		–0.2	0	V	B
Common-mode input range high	T_A = 25°C, < 3-dB degradation in CMRR limit	1.5	1.6		V	A
	T_A = –40°C to 125°C, < 3-dB degradation in CMRR limit	1.5	1.6		V	B
Common-mode rejection ratio		88	110		dB	A
Input impedance common-mode			250 || 1.2		MΩ || pF	C
Input impedance differential mode			200 || 1		kΩ || pF	C
OUTPUT						
Output voltage low	T_A = 25°C, G = 5		0.15	0.2	V	A
	T_A = –40°C to 125°C, G = 5		0.15	0.2	V	B
Output voltage high	T_A = 25°C, G = 5	2.45	2.5		V	A
	T_A = –40°C to 125°C, G = 5	2.45	2.5		V	B
Output saturation voltage, high/low	T_A = 25°C, G = 5		45/13		mV	C
Output current drive	T_A = 25°C	±25	±35		mA	A
	T_A = –40°C to 125°C	±20			mA	B

7.6 Electrical Characteristics: V_S = 2.7 V (continued)

at V_{S+} = +2.7 V, $V_{S–}$ = 0 V, V_{OUT} = 1 V_{PP}, R_F = 0 Ω, R_L = 2 kΩ, G = 1 V/V, input and output referenced to mid-supply, V_{IN_CM} = mid-supply – 0.5 V. T_A = 25°C, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL(1)
GAIN-SETTING RESISTORS (OPA835IRUN ONLY)						
Resistor FB1 to FB2	DC resistance	2376	2400	2424	Ω	A
Resistor FB2 to FB3	DC resistance	1782	1800	1818	Ω	A
Resistor FB3 to FB4	DC resistance	594	600	606	Ω	A
Resistor tolerance	DC resistance	–1%		1%		A
Resistor temperature coefficient	DC resistance		< 10		PPM	C
POWER SUPPLY						
Specified operating voltage		2.5		5.5	V	B
Quiescent operating current per amplifier	T_A = 25°C	175	245	340	µA	A
	T_A = –40°C to 125°C	135		345	µA	B
Power supply rejection (±PSRR)		88	105		dB	A
POWER DOWN (PIN MUST BE DRIVEN)						
Enable voltage threshold	Specified on above $V_{S–}$ + 2.1 V		1.4	2.1	V	A
Disable voltage threshold	Specified off below $V_{S–}$ + 0.7 V	0.7	1.4		V	A
Power-down pin bias current	$\overline{PD}$ = 0.5 V		20	500	nA	A
Power-down quiescent current	$\overline{PD}$ = 0.5 V		0.5	1.5	µA	A
Turnon time delay	Time from $\overline{PD}$ = high to V_{OUT} = 90% of final value		250		ns	C
Turnoff time delay	Time from $\overline{PD}$ = low to V_{OUT} = 10% of original value		50		ns	C

(1) Test levels (all values set by characterization and simulation): **(A)** 100% tested at 25°C; over temperature limits by characterization and simulation. **(B)** Not tested in production; limits set by characterization and simulation. **(C)** Typical value only for information.
(2) Current is considered positive out of the pin.
(3) Input Offset Voltage Drift, Input Bias Current Drift, and Input Offset Current Drift are average values calculated by taking data at the end points, computing the difference, and dividing by the temperature range.

7.7 Electrical Characteristics: V_S = 5 V

at V_{S+} = +5 V, V_{S-} = 0 V, V_{OUT} = 2 V_{PP}, R_F = 0 Ω, R_L = 2 kΩ, G = 1 V/V, input and output referenced to mid-supply. T_A = 25°C, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL(1)
AC PERFORMANCE						
Small-signal bandwidth	V_{OUT} = 100 mV_{PP}, G = 1		56		MHz	C
	V_{OUT} = 100 mV_{PP}, G = 2		22.5			
	V_{OUT} = 100 mV_{PP}, G = 5		7.4			
	V_{OUT} = 100 mV_{PP}, G = 10		3.1			
Gain-bandwidth product	V_{OUT} = 100 mV_{PP}, G = 10		31		MHz	C
Large-signal bandwidth	V_{OUT} = 2 V_{PP}, G = 1		31		MHz	C
Bandwidth for 0.1-dB flatness	V_{OUT} = 2 V_{PP}, G = 2		14.5		MHz	C
Slew rate, rise	V_{OUT} = 2-V Step, G = 2		160		V/µs	C
Slew rate, fall	V_{OUT} = 2-V Step, G = 2		260		V/µs	C
Rise time	V_{OUT} = 2-V Step, G = 2		10		ns	C
Fall time	V_{OUT} = 2-V Step, G = 2		7		ns	C
Settling time to 1%, rise	V_{OUT} = 2-V Step, G = 2		45		ns	C
Settling time to 1%, fall	V_{OUT} = 2-V Step, G = 2		45		ns	C
Settling time to 0.1%, rise	V_{OUT} = 2-V Step, G = 2		50		ns	C
Settling time to 0.1%, fall	V_{OUT} = 2-V Step, G = 2		55		ns	C
Settling time to 0.01%, rise	V_{OUT} = 2-V Step, G = 2		82		ns	C
Settling time to 0.01%, fall	V_{OUT} = 2-V Step, G = 2		85		ns	C
Overshoot/Undershoot	V_{OUT} = 2-V Step, G = 2		2.5%/1.5%			C
Second-order harmonic distortion	f = 10 kHz		–135		dBc	C
	f = 100 kHz		–105			
	f = 1 MHz		–70			
AC PERFORMANCE (continued)						
Third-order harmonic distortion	f = 10 kHz		–139		dBc	C
	f = 100 kHz		–122			
	f = 1 MHz		-73			
Second-order intermodulation distortion	f = 1 MHz, 200-kHz Tone Spacing, V_{OUT} Envelope = 2 V_{PP}		–70		dBc	C
Third-order intermodulation distortion	f = 1 MHz, 200-kHz Tone Spacing, V_{OUT} Envelope = 2 V_{PP}		–83		dBc	C
Signal-to-noise ratio, SNR	f = 1 kHz, V_{OUT} = 1 V_{RMS}, 22-kHz bandwidth		0.00015%			C
			–116.4		dBc	
Total harmonic distortion, THD	f = 1 kHz, V_{OUT} = 1 V_{RMS}		0.00003%			C
			–130		dBc	C
Input voltage noise	f = 100 kHz		9.3		nV/√Hz	C
Voltage noise 1/f corner frequency			147		Hz	C
Input current noise	f = 1 MHz		0.45		pA/√Hz	C
Current noise 1/f corner frequency			14.7		kHz	C
Overdrive recovery time, over/under	Overdrive = 0.5 V		195/135		ns	C
Closed-loop output impedance	f = 100 kHz		0.028		Ω	C
Channel to channel crosstalk (OPA2835)	f = 10 kHz		–120		dB	C
DC PERFORMANCE						
Open-loop voltage gain (A_{OL})		100	120		dB	A

7.7 Electrical Characteristics: V_S = 5 V (continued)

at V_{S+} = +5 V, $V_{S–}$ = 0 V, V_{OUT} = 2 V_{PP}, R_F = 0 Ω, R_L = 2 kΩ, G = 1 V/V, input and output referenced to mid-supply. T_A = 25°C, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL(1)
Input referred offset voltage	T_A = 25°C	–500	±100	500	μV	A
	T_A = 0°C to 70°C	–880		880		B
	T_A = –40°C to 85°C	–1040		1040		
	T_A = –40°C to 125°C	–1850		1850		
Input offset voltage drift(3)	T_A = 0°C to 70°C	–8.5	±1.4	8.5	μV/°C	B
	T_A = –40°C to 85°C	–9	±1.5	9		
	T_A = –40°C to 125°C	–13.5	±2.25	13.5		
Input bias current(2)	T_A = 25°C	50	200	400	nA	A
	T_A = 0°C to 70°C	47		410		B
	T_A = –40°C to 85°C	45		425		
	T_A = –40°C to 125°C	45		530		
Input bias current drift(3)	T_A = 0°C to 70°C	–1.4	±0.25	1.4	nA/°C	B
	T_A = –40°C to 85°C	–1.05	±0.175	1.05		
	T_A = –40°C to 125°C	–1.1	±0.185	1.1		
Input offset current	T_A = 25°C	–100	±13	100	nA	A
	T_A = 0°C to 70°C	–100	±13	100		B
	T_A = –40°C to 85°C	–100	±13	100		
	T_A = –40°C to 125°C	–100	±13	100		
Input offset current drift(3)	T_A = 0°C to 70°C	–1.23	±0.205	1.23	nA/°C	B
	T_A = –40°C to 85°C	–0.94	±0.155	0.94		
	T_A = –40°C to 125°C	–0.94	±0.155	0.94		
INPUT						
Common-mode input range low	T_A = 25°C, < 3-dB degradation in CMRR limit		–0.2	0	V	A
	T_A = –40°C to 125°C, < 3-dB degradation in CMRR limit		–0.2	0	V	B
Common-mode input range high	T_A = 25°C, < 3-dB degradation in CMRR limit	3.8	3.9		V	A
	T_A = –40°C to 125°C, < 3-dB degradation in CMRR limit	3.8	3.9		V	B
Common-mode rejection ratio		91	113		dB	A
Input impedance common-mode			250 || 1.2		MΩ || pF	C
Input impedance differential mode			200 || 1		kΩ || pF	C
OUTPUT						
Output voltage low	T_A = 25°C, G = 5		0.15	0.2	V	A
	T_A = –40°C to 125°C, G = 5		0.15	0.2	V	B
Output voltage high	T_A = 25°C, G = 5	4.75	4.8		V	A
	T_A = –40°C to 125°C, G = 5	4.75	4.8		V	B
Output saturation voltage, high/low	T_A = 25°C, G = 5		70/25		mV	C
Output current drive	T_A = 25°C	±30	±40		mA	A
	T_A = –40°C to 125°C	±25			mA	B
GAIN-SETTING RESISTORS (OPA835IRUN ONLY)						
Resistor FB1 to FB2	DC resistance	2376	2400	2424	Ω	A
Resistor FB2 to FB3	DC resistance	1782	1800	1818	Ω	A
Resistor FB3 to FB4	DC resistance	594	600	606	Ω	A
Resistor tolerance	DC resistance	–1%		1%		A
Resistor temperature coefficient	DC resistance		<10		PPM	C
POWER SUPPLY						
Specified operating voltage		2.5		5.5	V	B
Quiescent operating current per amplifier	T_A = 25°C	200	250	350	μA	A
	T_A = –40°C to 125°C	150		365	μA	B

7.7 Electrical Characteristics: V_S = 5 V (continued)

at V_{S+} = +5 V, $V_{S–}$ = 0 V, V_{OUT} = 2 V_{PP}, R_F = 0 Ω, R_L = 2 kΩ, G = 1 V/V, input and output referenced to mid-supply. T_A = 25°C, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL(1)
Power supply rejection (±PSRR)		90	110		dB	A
POWER DOWN (PIN MUST BE DRIVEN)						
Enable voltage threshold	Specified "on" above $V_{S–}$+ 2.1 V		1.4	2.1	V	A
Disable voltage threshold	Specified "off" below $V_{S–}$+ 0.7 V	0.7	1.4		V	A
Power-down pin bias current	$\overline{PD}$ = 0.5 V		20	500	nA	A
Power-down quiescent current	$\overline{PD}$ = 0.5 V		0.5	1.5	µA	A
Turnon time delay	Time from $\overline{PD}$ = high to V_{OUT} = 90% of final value		200		ns	C
Turnoff time delay	Time from $\overline{PD}$ = low to V_{OUT} = 10% of original value		60		ns	C

(1) Test levels (all values set by characterization and simulation): **(A)** 100% tested at 25°C; over temperature limits by characterization and simulation. **(B)** Not tested in production; limits set by characterization and simulation. **(C)** Typical value only for information.
(2) Current is considered positive out of the pin.
(3) Input Offset Voltage Drift, Input Bias Current Drift, and Input Offset Current Drift are average values calculated by taking data at the end points, computing the difference, and dividing by the temperature range.

7.8 Typical Characteristics: V_S = 2.7 V

Test conditions unless otherwise noted: V_{S+} = +2.7 V, $V_{S–}$ = 0 V, V_{OUT} = 1 Vpp, R_F = 0 Ω, R_L = 2 kΩ, G = 1 V/V, input and output referenced to mid-supply, V_{IN_CM} = mid-supply – 0.5 V. T_A = 25°C

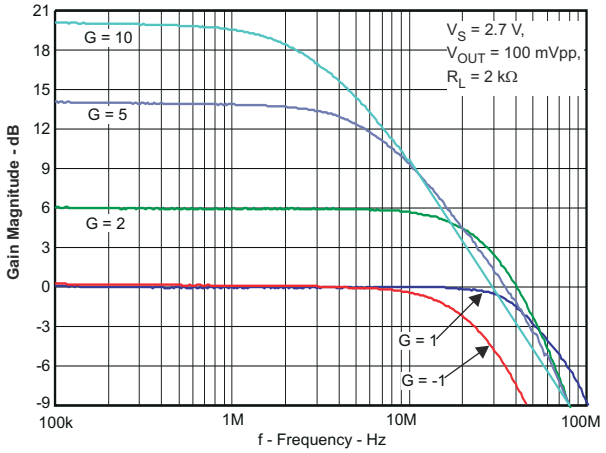


図 7-1. Small-Signal Frequency Response

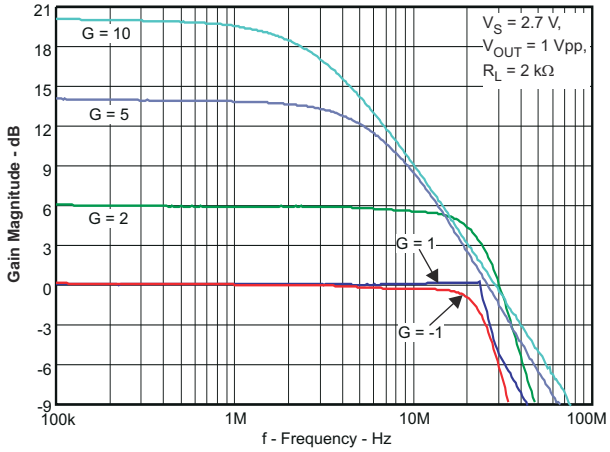


図 7-2. Large-Signal Frequency Response

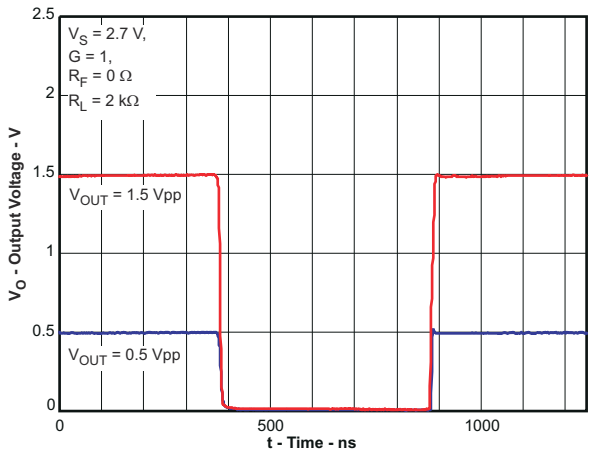


図 7-3. Noninverting Pulse Response

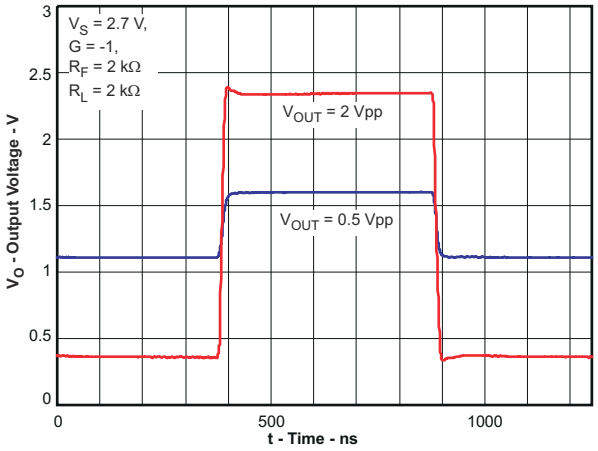


図 7-4. Inverting Pulse Response

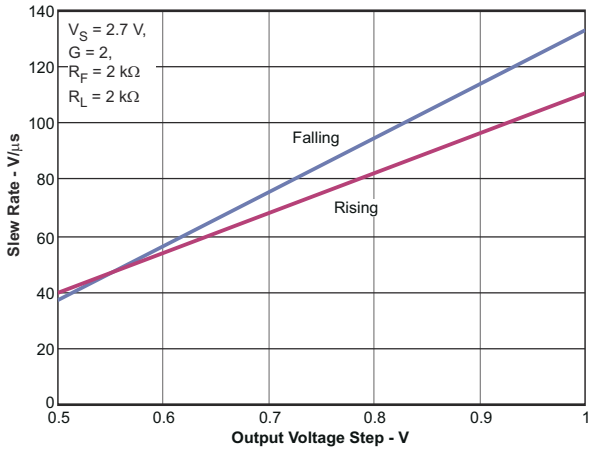


図 7-5. Slew Rate vs Output Voltage Step

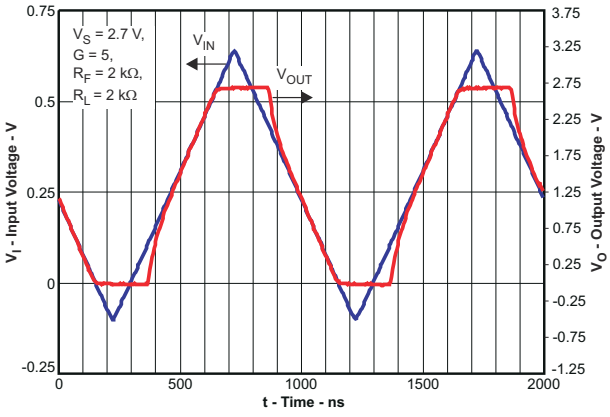


図 7-6. Output Overdrive Recovery

7.8 Typical Characteristics: V_S = 2.7 V (continued)

Test conditions unless otherwise noted: V_{S+} = +2.7 V, $V_{S–}$ = 0 V, V_{OUT} = 1 Vpp, R_F = 0 Ω, R_L = 2 kΩ, G = 1 V/V, input and output referenced to mid-supply, V_{IN_CM} = mid-supply – 0.5 V. T_A = 25°C

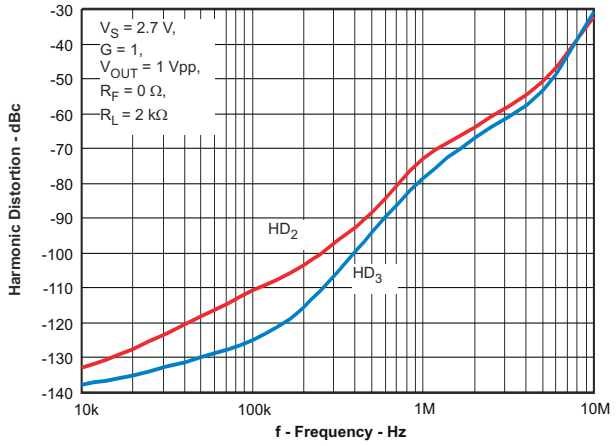


図 7-7. Harmonic Distortion vs Frequency

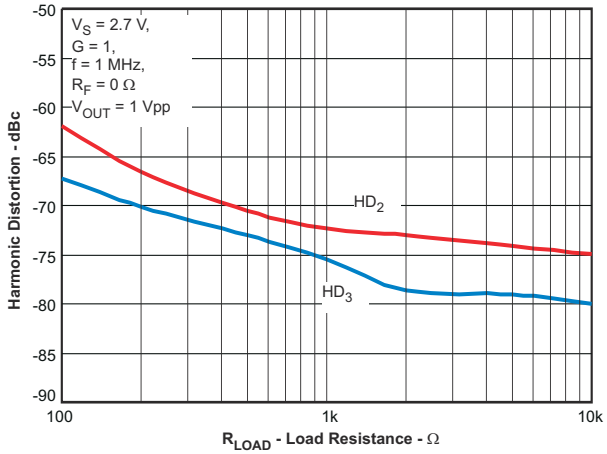


図 7-8. Harmonic Distortion vs Load Resistance

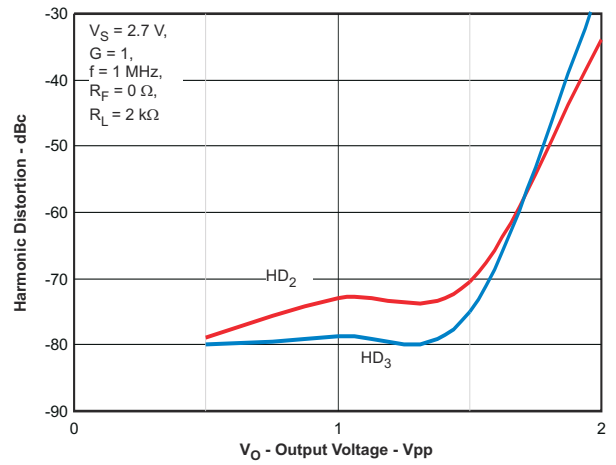


図 7-9. Harmonic Distortion vs Output Voltage

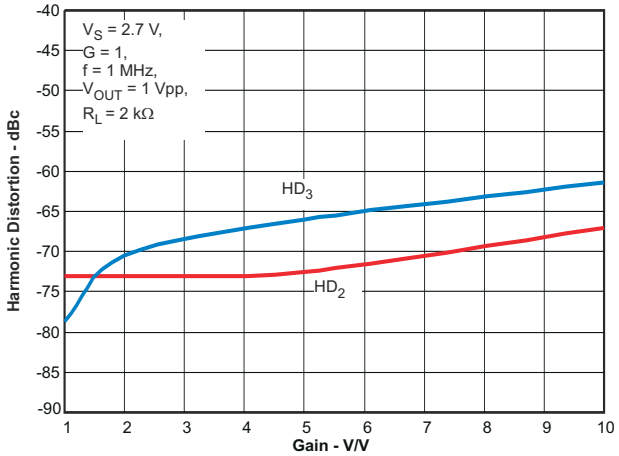


図 7-10. Harmonic Distortion vs Gain

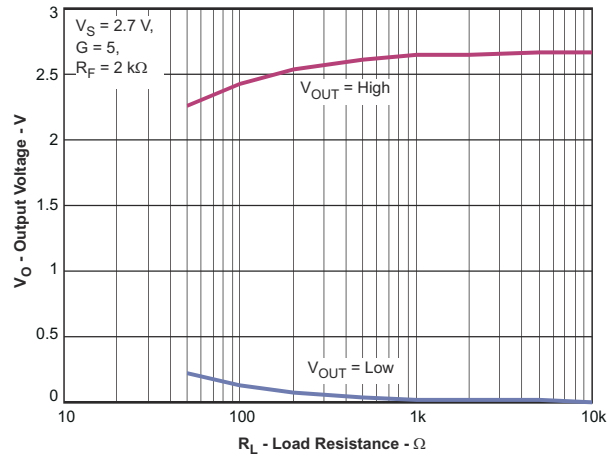


図 7-11. Output Voltage Swing vs Load Resistance

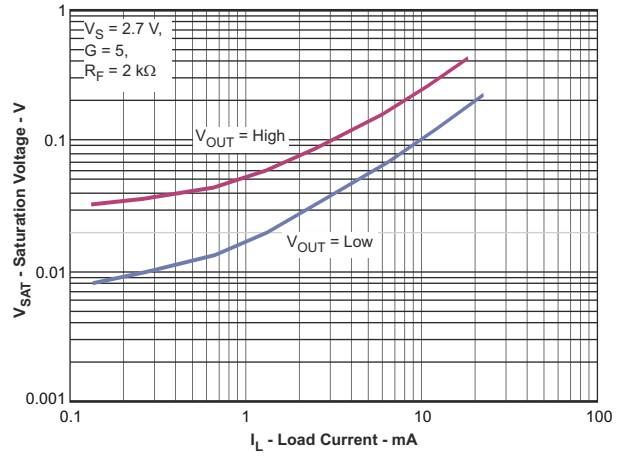


図 7-12. Output Saturation Voltage vs Load Current

7.8 Typical Characteristics: V_S = 2.7 V (continued)

Test conditions unless otherwise noted: V_{S+} = +2.7 V, $V_{S–}$ = 0 V, V_{OUT} = 1 Vpp, R_F = 0 Ω, R_L = 2 kΩ, G = 1 V/V, input and output referenced to mid-supply, V_{IN_CM} = mid-supply – 0.5 V. T_A = 25°C

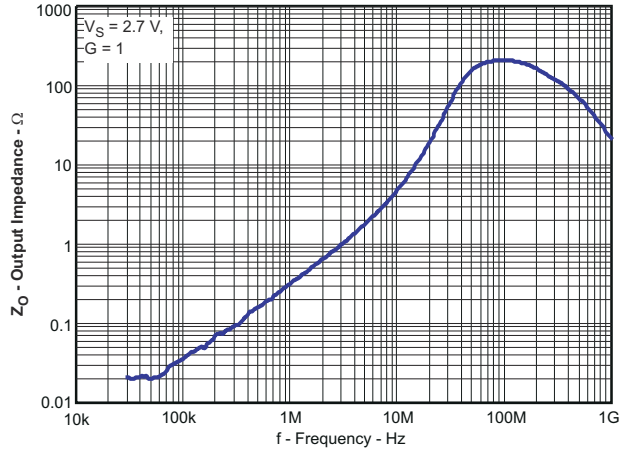


図 7-13. Output Impedance vs Frequency

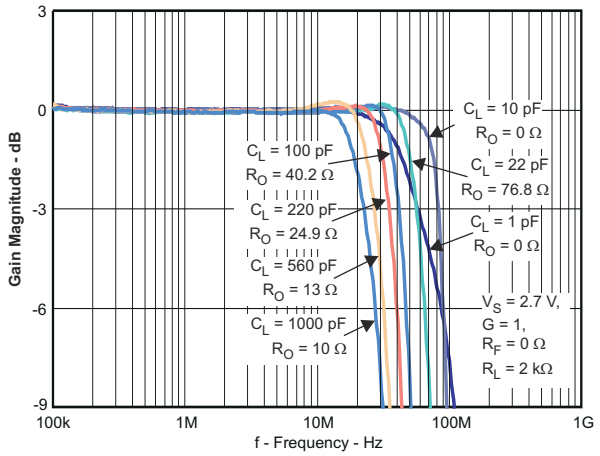


図 7-14. Frequency Response With Capacitive Load

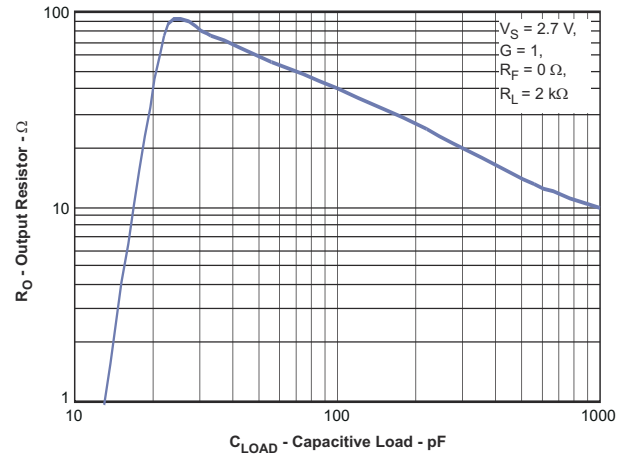


図 7-15. Series Output Resistor vs Capacitive Load

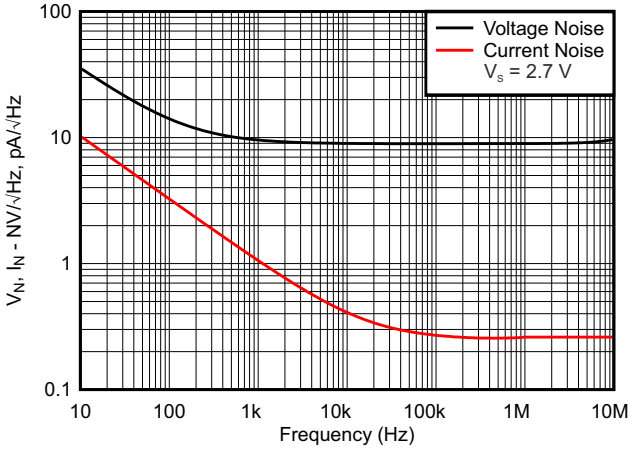


図 7-16. Input Referred Noise vs Frequency

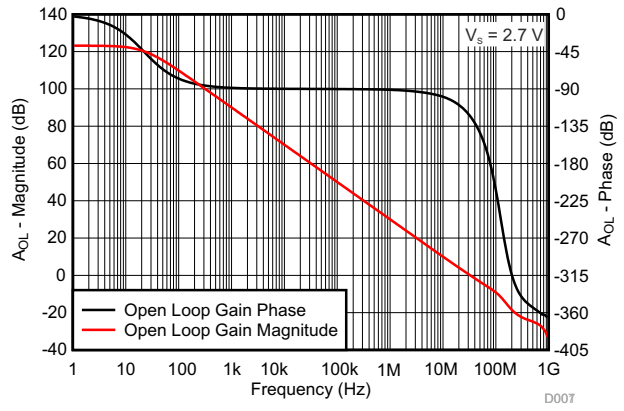


図 7-17. Open Loop Gain vs Frequency

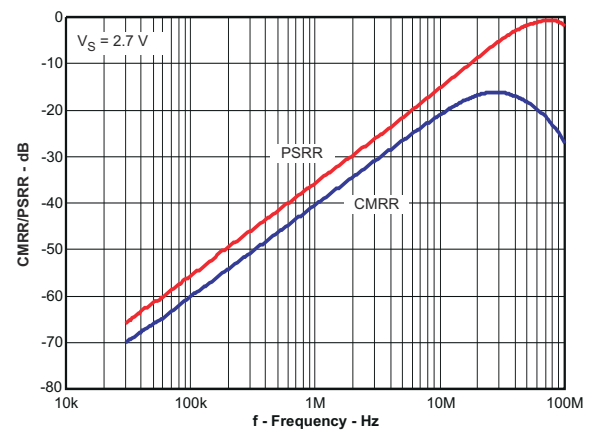


図 7-18. Common-Mode/Power Supply Rejection Ratios vs Frequency

7.8 Typical Characteristics: V_S = 2.7 V (continued)

Test conditions unless otherwise noted: V_{S+} = +2.7 V, V_{S-} = 0 V, V_{OUT} = 1 Vpp, R_F = 0 Ω, R_L = 2 kΩ, G = 1 V/V, input and output referenced to mid-supply, V_{IN_CM} = mid-supply – 0.5 V. T_A = 25°C

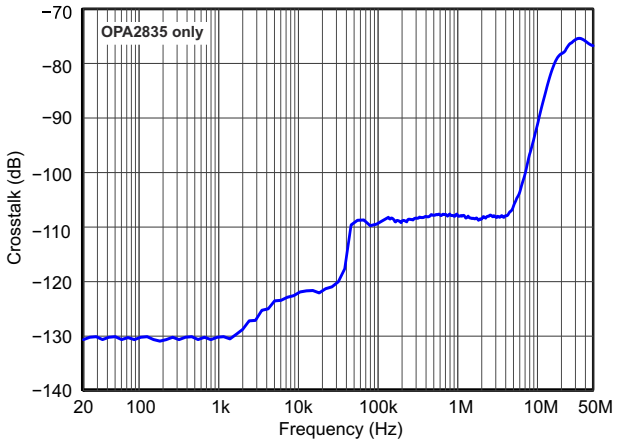


図 7-19. Crosstalk vs Frequency

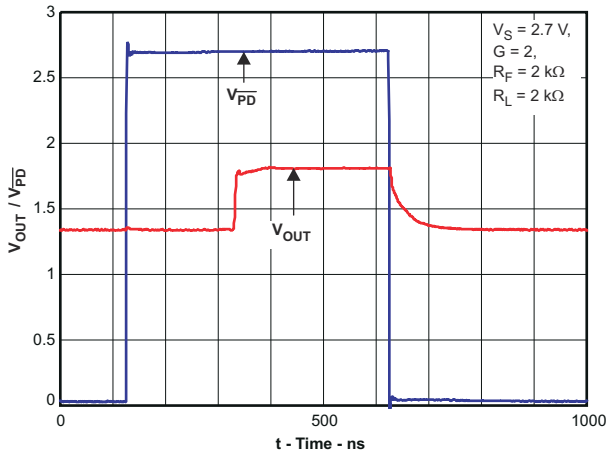


図 7-20. Power Down Response

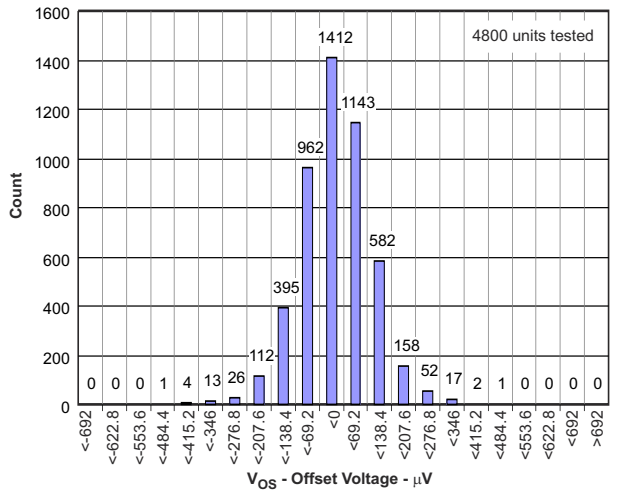


図 7-21. Input Offset Voltage

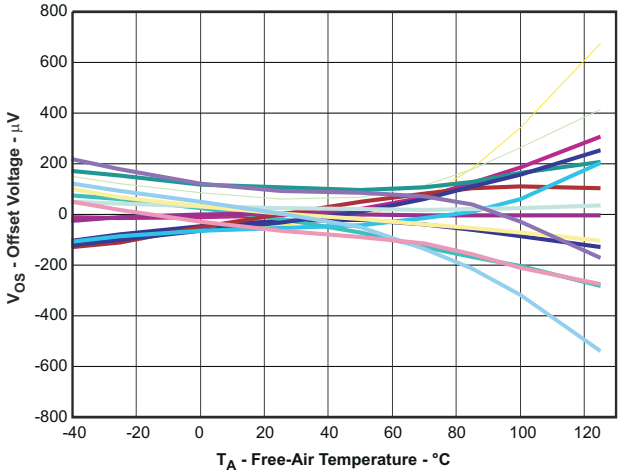


図 7-22. Input Offset Voltage vs Free-Air Temperature

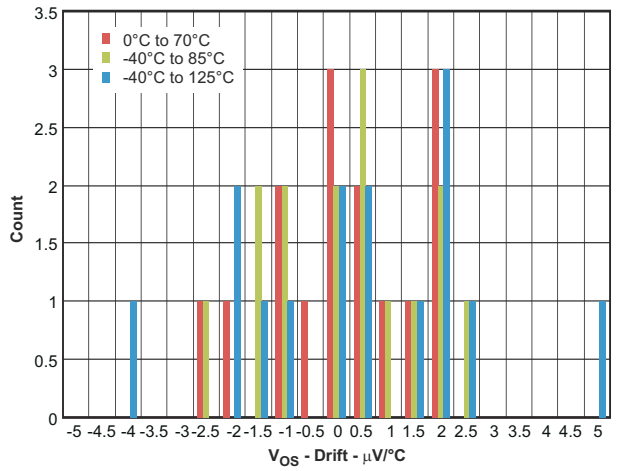


図 7-23. Input Offset Voltage Drift

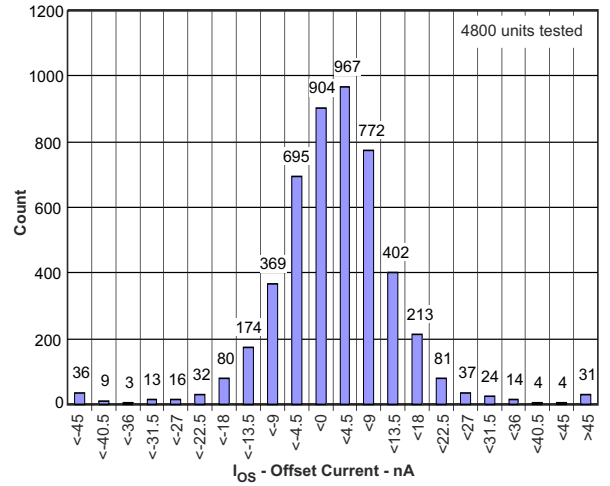


図 7-24. Input Offset Current

7.8 Typical Characteristics: V_S = 2.7 V (continued)

Test conditions unless otherwise noted: V_{S+} = +2.7 V, $V_{S–}$ = 0 V, V_{OUT} = 1 Vpp, R_F = 0 Ω, R_L = 2 kΩ, G = 1 V/V, input and output referenced to mid-supply, V_{IN_CM} = mid-supply – 0.5 V. T_A = 25°C

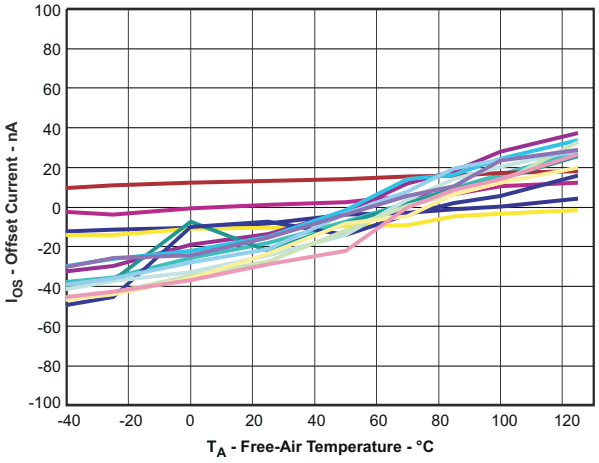


図 7-25. Input Offset Current vs Free-Air Temperature

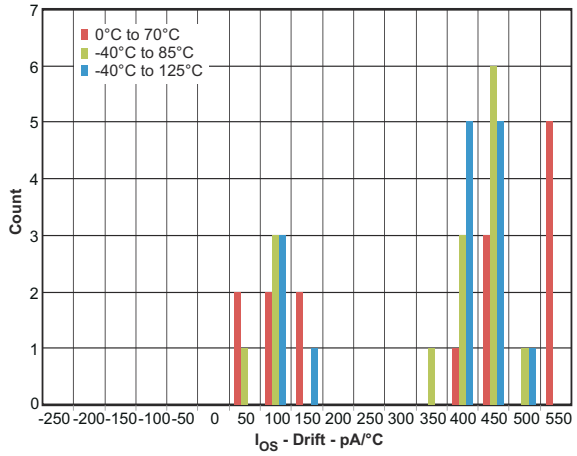


図 7-26. Input Offset Current Drift

7.9 Typical Characteristics: V_S = 5 V

Test conditions unless otherwise noted: V_{S+} = +5 V, $V_{S–}$ = 0 V, V_{OUT} = 2 Vpp, R_F = 0 Ω, R_L = 2 kΩ, G = 1 V/V, input and output referenced to mid-supply. T_A = 25°C

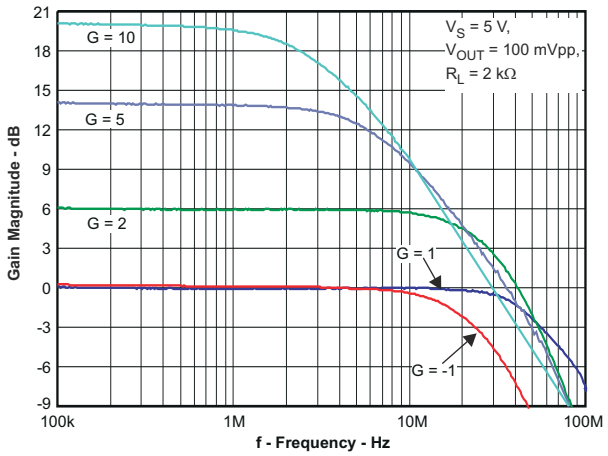


図 7-27. Small-Signal Frequency Response

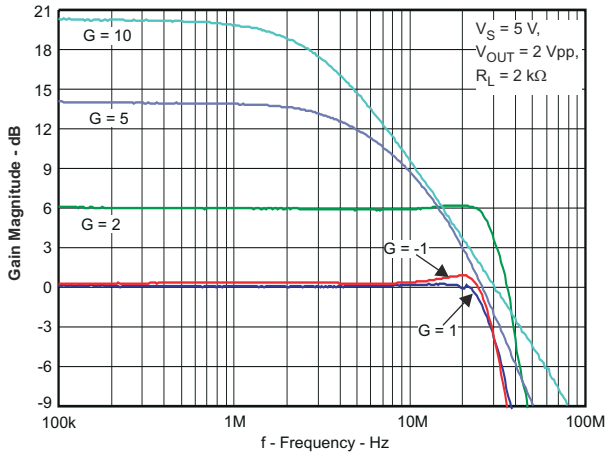


図 7-28. Large-Signal Frequency Response

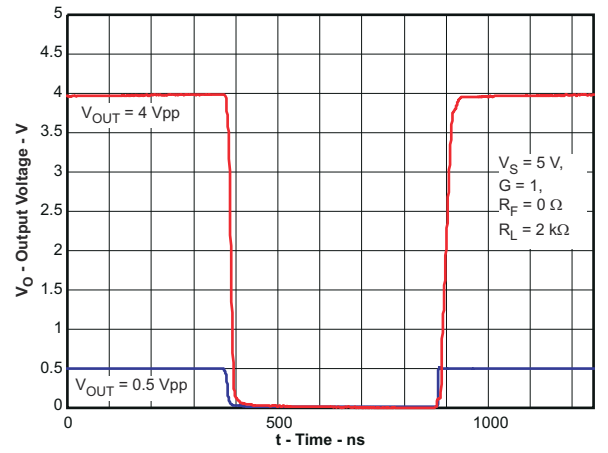


図 7-29. Noninverting Pulse Response

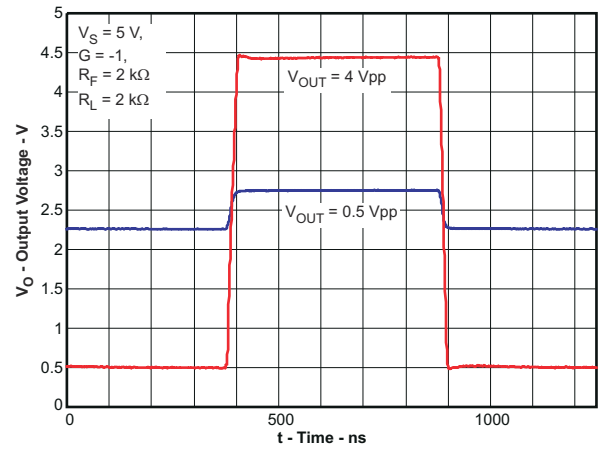


図 7-30. Inverting Pulse Response

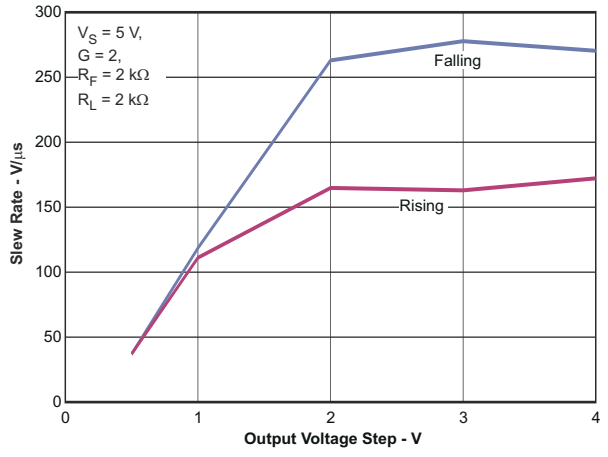


図 7-31. Slew Rate vs Output Voltage Step

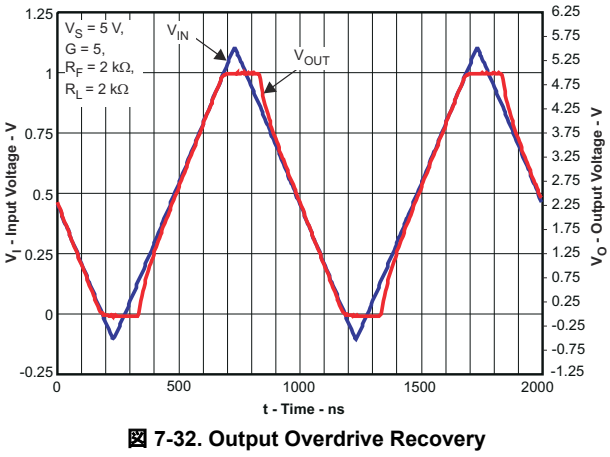


図 7-32. Output Overdrive Recovery

7.9 Typical Characteristics: V_S = 5 V (continued)

Test conditions unless otherwise noted: V_{S+} = +5 V, $V_{S–}$ = 0 V, V_{OUT} = 2 Vpp, R_F = 0 Ω, R_L = 2 kΩ, G = 1 V/V, input and output referenced to mid-supply. T_A = 25°C

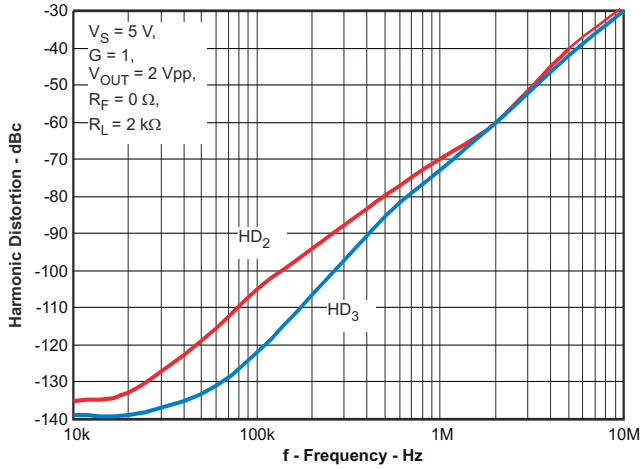


図 7-33. Harmonic Distortion vs Frequency

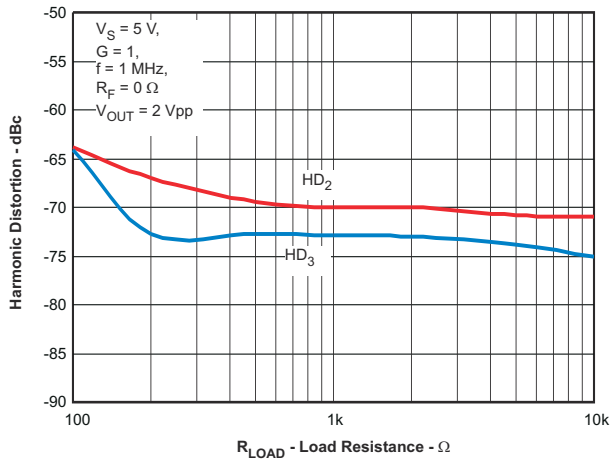


図 7-34. Harmonic Distortion vs Load Resistance

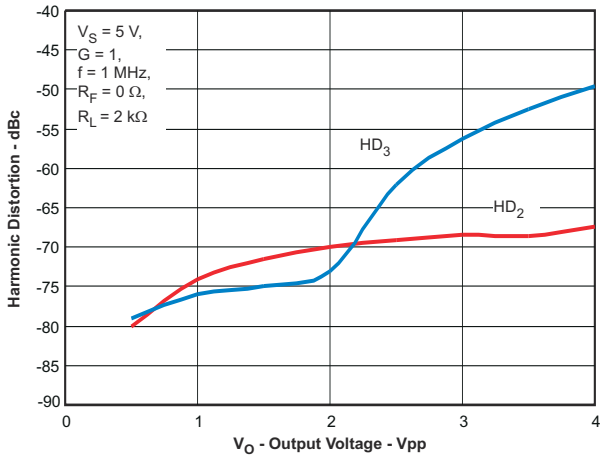


図 7-35. Harmonic Distortion vs Output Voltage

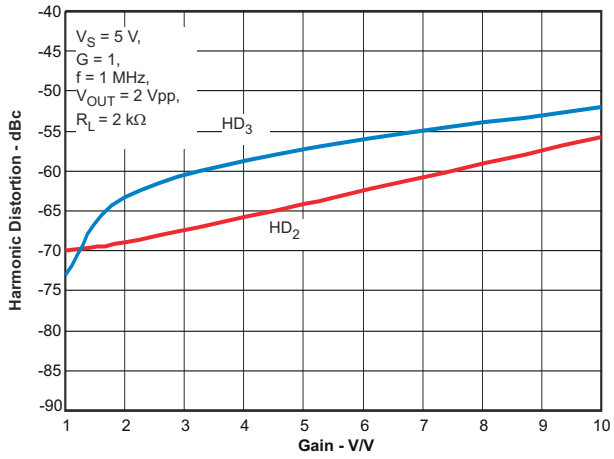


図 7-36. Harmonic Distortion vs Gain

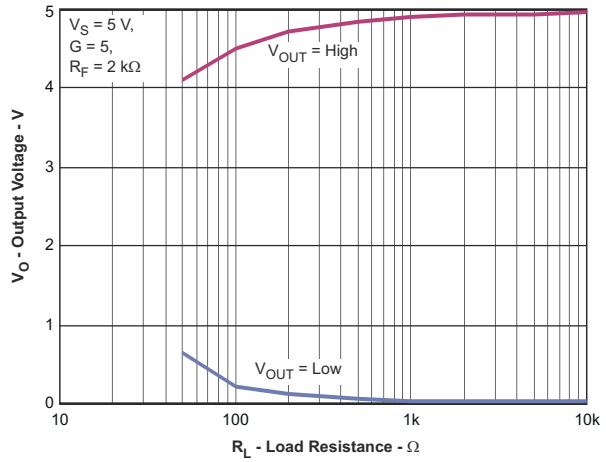


図 7-37. Output Voltage Swing vs Load Resistance

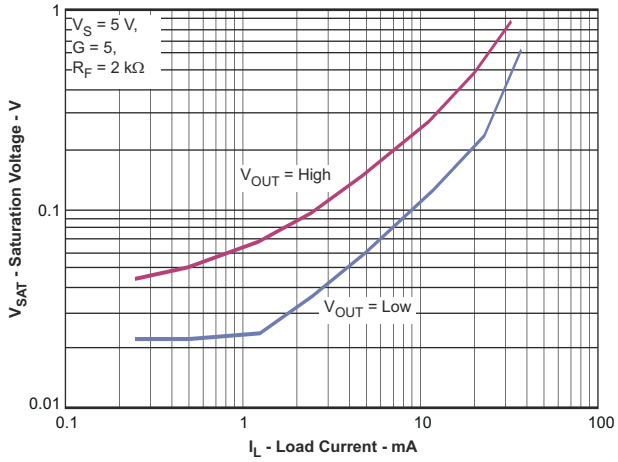


図 7-38. Output Saturation Voltage vs Load Current

7.9 Typical Characteristics: V_S = 5 V (continued)

Test conditions unless otherwise noted: V_{S+} = +5 V, $V_{S–}$ = 0 V, V_{OUT} = 2 Vpp, R_F = 0 Ω, R_L = 2 kΩ, G = 1 V/V, input and output referenced to mid-supply. T_A = 25°C

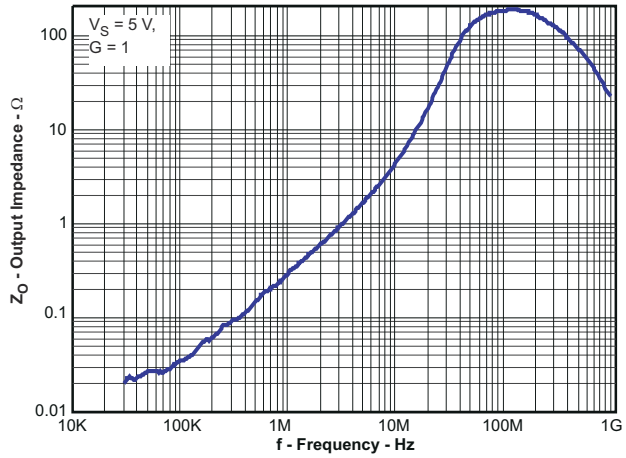


図 7-39. Output Impedance vs Frequency

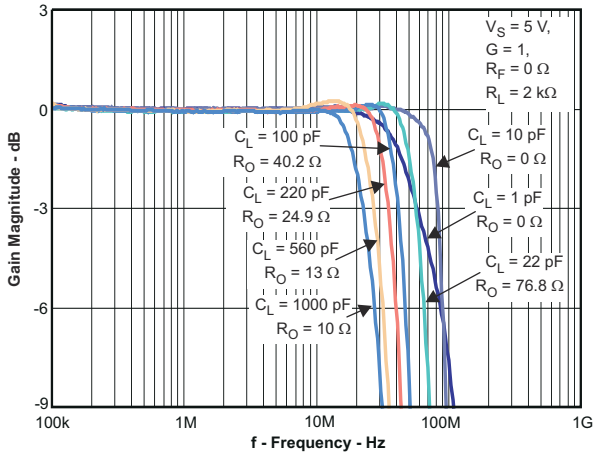


図 7-40. Frequency Response With Capacitive Load

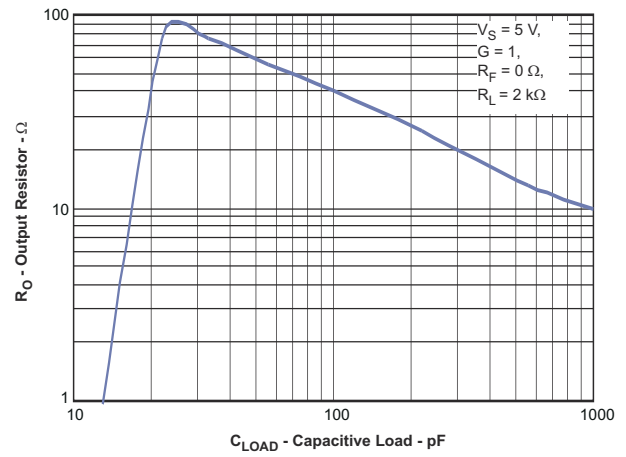


図 7-41. Series Output Resistor vs Capacitive Load

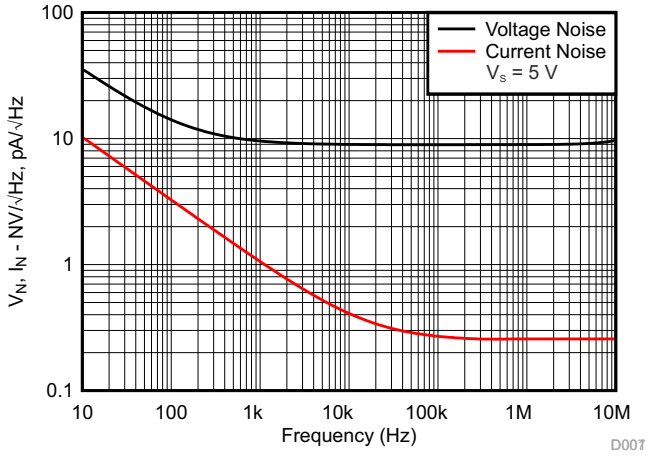


図 7-42. Input Referred Noise vs Frequency

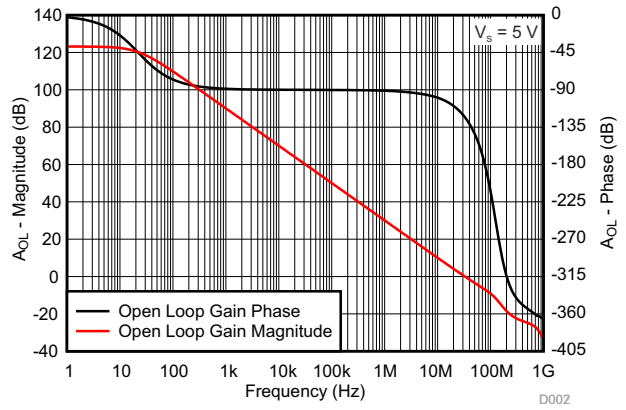


図 7-43. Open-Loop Gain vs Frequency

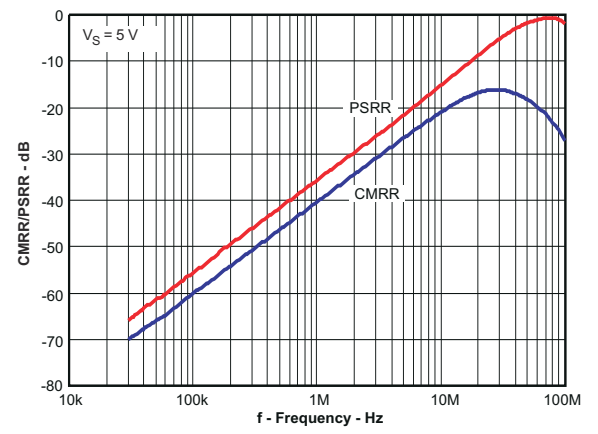


図 7-44. Common-Mode/Power Supply Rejection Ratios vs Frequency

7.9 Typical Characteristics: V_S = 5 V (continued)

Test conditions unless otherwise noted: V_{S+} = +5 V, V_{S-} = 0 V, V_{OUT} = 2 Vpp, R_F = 0 Ω, R_L = 2 kΩ, G = 1 V/V, input and output referenced to mid-supply. T_A = 25°C

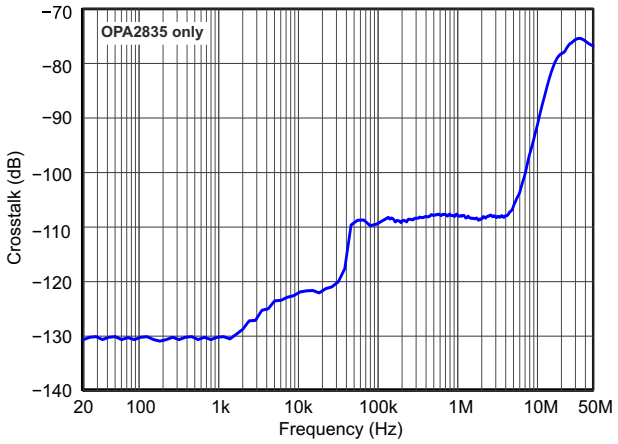


図 7-45. Crosstalk vs Frequency

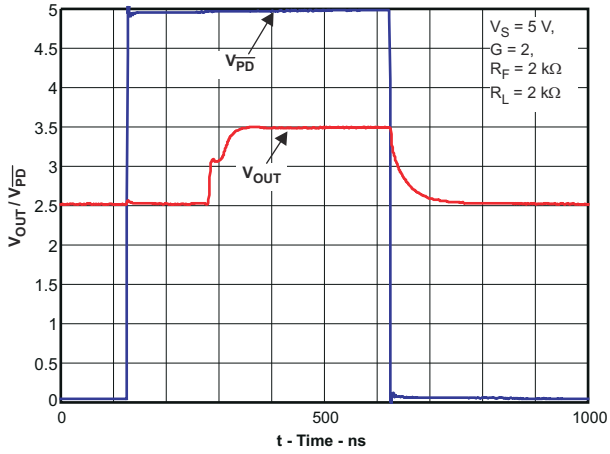


図 7-46. Power Down Response

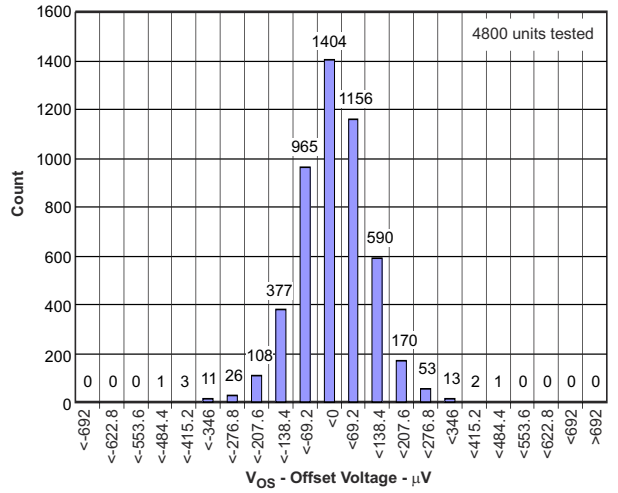


図 7-47. Input Offset Voltage

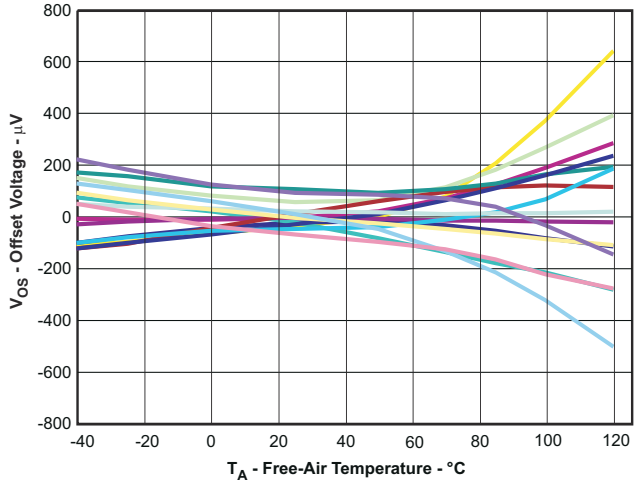


図 7-48. Input Offset Voltage vs Free-Air Temperature

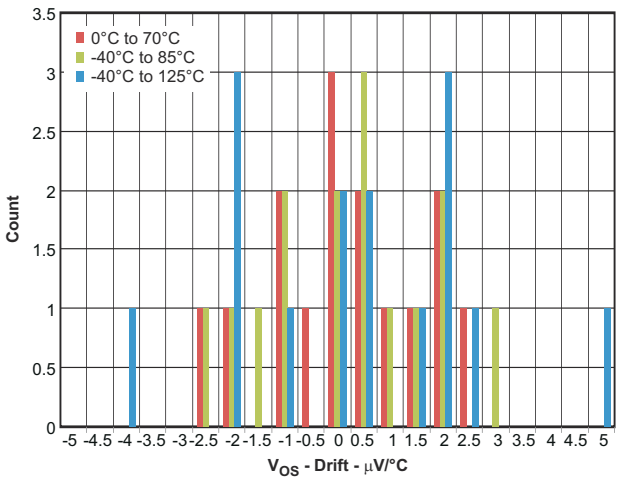


図 7-49. Input Offset Voltage Drift

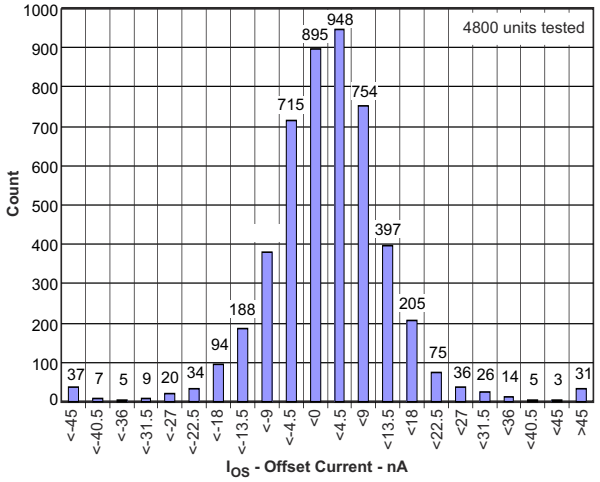


図 7-50. Input Offset Current

7.9 Typical Characteristics: V_S = 5 V (continued)

Test conditions unless otherwise noted: V_{S+} = +5 V, $V_{S–}$ = 0 V, V_{OUT} = 2 Vpp, R_F = 0 Ω, R_L = 2 kΩ, G = 1 V/V, input and output referenced to mid-supply. T_A = 25°C

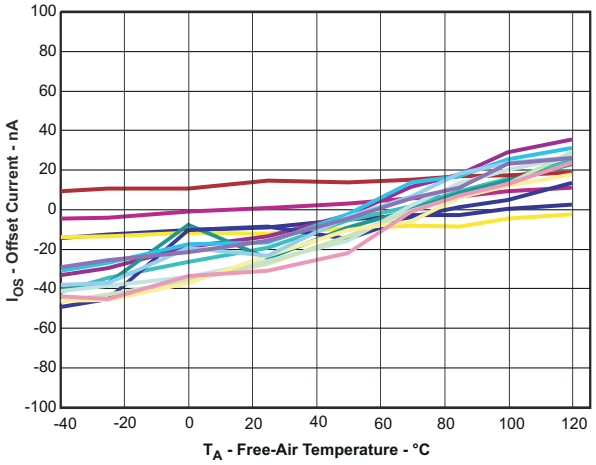


図 7-51. Input Offset Current vs Free-Air Temperature

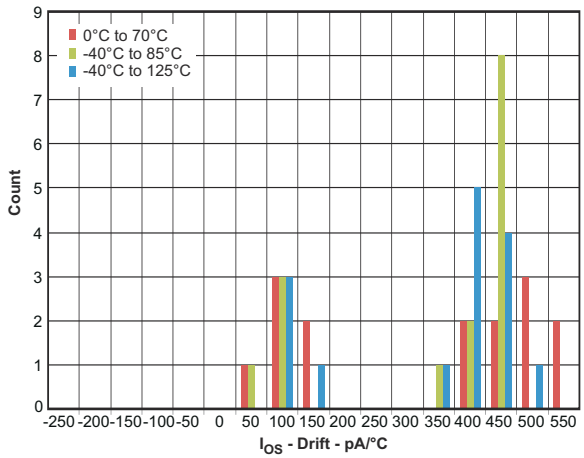


図 7-52. Input Offset Current Drift

8 Detailed Description

8.1 Overview

The OPAx835 family of bipolar-input operational amplifiers offers excellent bandwidth of 56 MHz with ultra-low THD of 0.00003% at 1 kHz. The device can swing to within 200 mV of the supply rails while driving a 2-kΩ load. The input common-mode of the amplifier can swing to 200 mV below the negative supply rail. This level of performance is achieved at 250 µA of quiescent current per amplifier channel.

8.2 Functional Block Diagram

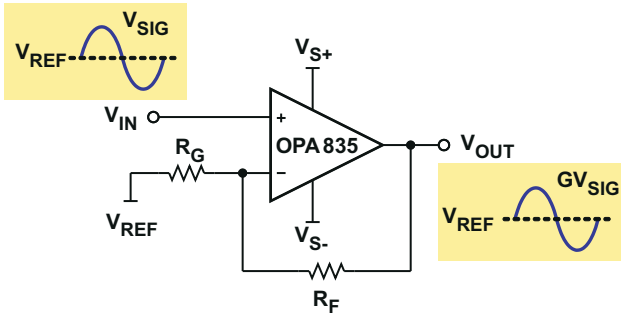


図 8-1. Noninverting Amplifier

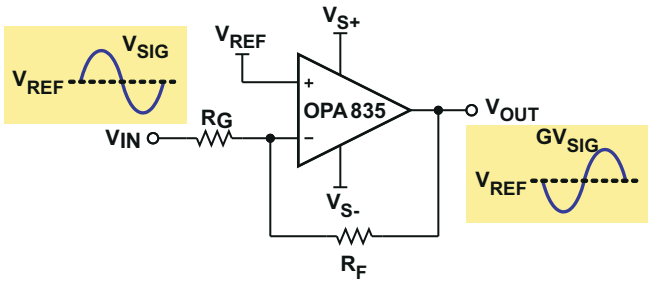


図 8-2. Inverting Amplifier

8.3 Feature Description

8.3.1 Input Common-Mode Voltage Range

When the primary design goal is a linear amplifier, with high CMRR, it is important to not violate the input common-mode voltage range (V_{ICR}) of an op amp.

The common-mode input range specifications in the table data use CMRR to set the limit. The limits are selected to ensure CMRR will not degrade more than 3 dB below the CMRR limit if the input voltage is kept within the specified range. The limits cover all process variations, and most parts will be better than specified. The typical specifications are 0.2 V below the negative rail and 1.1 V below the positive rail.

Assuming the op amp is in linear operation, the voltage difference between the input pins is small (ideally 0 V); and the input common-mode voltage is analyzed at either input pin with the other input pin assumed to be at the same potential. The voltage at V_{IN+} is simple to evaluate. In noninverting configuration, 図 8-1, the input signal, V_{IN}, must not violate the V_{ICR}. In inverting configuration, as shown in 図 8-2, the reference voltage, V_{REF}, must be within the V_{ICR}.

The input voltage limits have fixed headroom to the power rails and track the power supply voltages. For one 5-V supply, the linear input voltage ranges from –0.2 V to 3.9 V and –0.2 V to 1.6 V for a 2.7-V supply. The delta headroom from each power supply rail is the same in either case: –0.2 V and 1.1 V.

8.3.2 Output Voltage Range

The OPA835 and OPA2835 devices are rail-to-rail output (RRO) op amps. Rail-to-rail output typically means that the output voltage swings within a couple hundred millivolts of the supply rails. There are different ways to specify this: one is with the output still in linear operation and another is with the output saturated. Saturated output voltages are closer to the power supply rails than linear outputs, but the signal is not a linear representation of the input. Linear output is a better representation of how well a device performs when used as a linear amplifier. Saturation and linear operation limits are affected by the output current, where higher currents lead to more loss in the output transistors.

The specification tables list linear and saturated output voltage specifications with 2-kΩ load. 図 7-11 and 図 7-37 show saturated voltage-swing limits versus output load resistance, and 図 7-12 and 図 7-38 show the output saturation voltage versus load current. Given a light load, the output voltage limits have nearly constant headroom to the power rails and track the power supply voltages. For example, with a 2-kΩ load and a single 5-V supply, the linear output voltage ranges from 0.15 V to 4.8 V and ranges from 0.15 V to 2.5 V for a 2.7-V supply. The delta from each power supply rail is the same in either case: 0.15 V and 0.2 V.

With devices like the OPA835 and OPA2835 where the input range is lower than the output range, typically the input will limit the available signal swing only in noninverting gain of 1. Signal swing in noninverting configurations in gains > +1 and inverting configurations in any gain is typically limited by the output voltage limits of the op amp.

8.3.3 Power-Down Operation

The OPA835 and OPA2835 devices include a power-down mode. Under logic control, the amplifiers can switch from normal operation to a standby current of < 1.5 µA. When the $\overline{PD}$ pin is connected high, the amplifier is active. Connecting $\overline{PD}$ pin low disables the amplifier and places the output in a high-impedance state. When the amplifier is configured as a unity-gain buffer, the output stage is in a high dc-impedance state. To protect the input stage of the amplifier, the devices use internal, back-to-back ESD diodes between the inverting and noninverting input pins. This configuration creates a parallel low-impedance path from the amplifier output to the noninverting pin when the differential voltage between the pins exceeds a diode voltage drop. When the op amp is configured in other gains, the feedback (RF) and gain (RG) resistor network forms a parallel load.

The $\overline{PD}$ pin must be actively driven high or low and must not be left floating. If the power-down mode is not used, $\overline{PD}$ must be tied to the positive supply rail.

$\overline{PD}$ logic states are TTL with reference to the negative supply rail, V_{S-}. When the op amp is powered from a single-supply and ground, driven from logic devices with similar V_{DD} voltages to the op amp do not require any special consideration. When the op amp is powered from a split supply, with V_{S-} below ground, an open-collector type of interface with a pullup resistor is more appropriate. Pullup resistor values must be lower than 100 kΩ. Additionally, the drive logic must be negated due to the inverting action of an open-collector gate.

8.3.4 Low-Power Applications and the Effects of Resistor Values on Bandwidth

The OPA835 and OPA2835 devices are designed for the nominal value of R_F to be 2 kΩ in gains other than +1. This gives excellent distortion performance, maximum bandwidth, best flatness, and best pulse response. It also loads the amplifier. For example; in gain of 2 with $R_F = R_G = 2$ kΩ, R_G to ground, and $V_{OUT} = 4$ V, 1 mA of current will flow through the feedback path to ground. In gain of +1, R_G is open and no current will flow to ground. In low-power applications, it is desirable to reduce the current in the feedback path by increasing the gain-setting resistors values. Using larger value gain resistors has two primary side effects (other than lower power) due to their interaction with parasitic circuit capacitance.

- Lowers the bandwidth
- Lowers the phase margin
  - This causes peaking in the frequency response
  - This causes overshoot and ringing in the pulse response

図 8-3 shows the small-signal frequency response on OPA835EVM for noninverting gain of 2 with R_F and R_G equal to 2 kΩ, 10 kΩ, and 100 kΩ. The test was done with $R_L = 2$ kΩ. Due to loading effects of R_L, lower R_L values may reduce the peaking, but higher values will not have a significant effect.

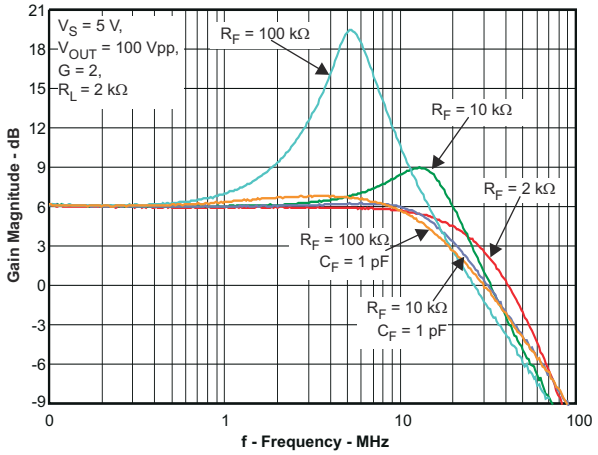


図 8-3. Frequency Response With Various Gain-Setting Resistor Values

As expected, larger value gain resistors cause lower bandwidth and peaking in the response (peaking in frequency response is synonymous with overshoot and ringing in pulse response). Adding 1-pF capacitors in parallel with R_F helps compensate the phase margin and restores flat frequency response. 図 8-4 shows the test circuit.

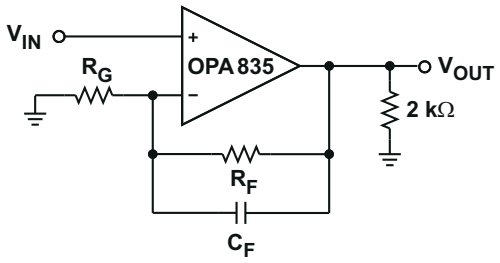


図 8-4. G = 2 Test Circuit for Various Gain-Setting Resistor Values

8.3.5 Driving Capacitive Loads

The OPA835 and OPA2835 devices drive up to a nominal capacitive load of 10 pF on the output with no special consideration. When driving capacitive loads greater than 10 pF, TI recommends using a small resistor (R_O) in series with the output as close to the device as possible. Without R_O, output capacitance interacts with the output impedance of the amplifier causing phase shift in the loop gain of the amplifier that will reduce the phase margin. This will cause peaking in the frequency response and overshoot and ringing in the pulse response. Interaction with other parasitic elements may lead to instability or oscillation. Inserting R_O will isolate the phase shift from the loop gain path and restore the phase margin; however R_O can limit the bandwidth slightly.

図 8-5 shows the test circuit and 図 7-41 shows the recommended values of R_O versus capacitive loads, C_L. See 図 7-40 for the frequency responses with various values.

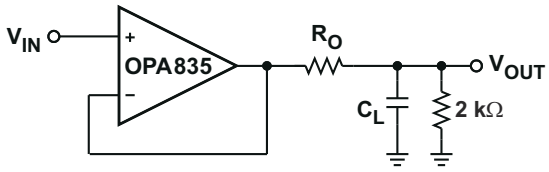


図 8-5. R_O versus C_L Test Circuit

8.4 Device Functional Modes

8.4.1 Split-Supply Operation (±1.25 V to ±2.75 V)

To facilitate testing with common lab equipment, the OPA835 EVM (see *OPA835DBV and OPA836DBV EVM User's Guide* (SLOU314)) is built to allow split-supply operation. This configuration eases lab testing because the mid-point between the power rails is ground, and most signal generators, network analyzers, oscilloscopes, spectrum analyzers and other lab equipment have inputs and outputs with a ground reference.

図 8-6 shows a simple noninverting configuration analogous to 図 8-1 with ±2.5-V supply and V_{REF} equal to ground. The input and output will swing symmetrically around ground. For ease of use, split supplies are preferred in systems where signals swing around ground.

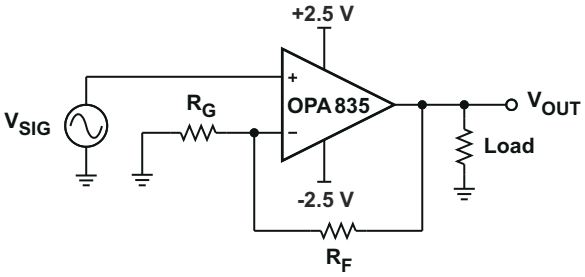


図 8-6. Split-Supply Operation

8.4.2 Single-Supply Operation (2.5 V to 5.5 V)

Often, newer systems use a single power supply to improve efficiency and reduce the cost of the power supply. OPA835 and OPA2835 devices are designed for use with single-supply power operation and can be used with single-supply power with no change in performance from split supply, as long as the input and output are biased within the linear operation of the device.

To change the circuit from split supply to single-supply, level shift all voltages by ½ the difference between the power supply rails. For example, changing from ± 2.5-V split supply to 5-V single-supply is shown in 図 8-7.

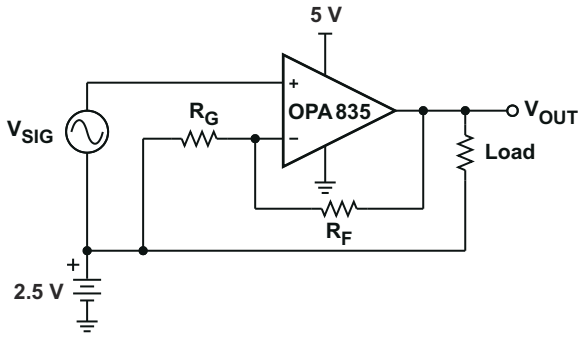


図 8-7. Single-Supply Concept

A practical circuit will have an amplifier or other circuit providing the bias voltage for the input, and the output of this amplifier stage provides the bias for the next stage.

図 8-8 shows a typical noninverting amplifier circuit. With 5-V single-supply, a mid-supply reference generator is needed to bias the negative side through R_G. To cancel the voltage offset that would otherwise be caused by the input bias currents, R_1 is selected to be equal to R_F in parallel with R_G. For example if gain of 2 is required and R_F = 2 kΩ, select R_G = 2 kΩ to set the gain, and R_1 = 1 kΩ for bias current cancellation. The value for C is dependent on the reference, and TI recommends a value of at least 0.1 µF to limit noise.

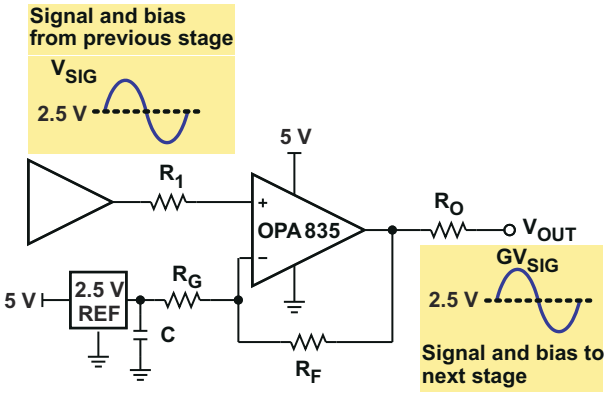


図 8-8. Noninverting Single Supply With Reference

図 8-9 shows a similar noninverting single-supply scenario with the reference generator replaced by the Thevenin equivalent using resistors and the positive supply. R_G' and R_G" form a resistor divider from the 5-V supply and are used to bias the negative side with the parallel sum equal to the equivalent R_G to set the gain. To cancel the voltage offset that would otherwise be caused by the input bias currents, R_1 is selected to be equal to R_F in parallel with R_G' in parallel with R_G" (R_1= R_F || R_G' || R_G"). For example, if a gain of 2 is required and R_F = 2 kΩ, selecting R_G' = R_G" = 4 kΩ gives equivalent parallel sum of 2 kΩ, sets the gain to 2, and references the input to mid supply (2.5 V). R_1 is set to 1 kΩ for bias current cancellation. The resistor divider costs less than the 2.5V reference in 図 8-8 but may increase the current from the 5-V supply.

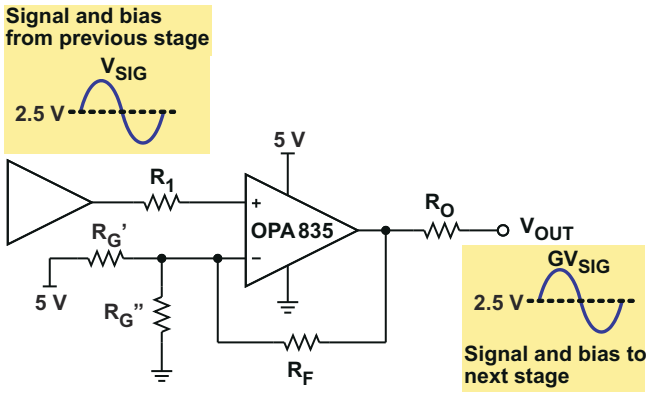


図 8-9. Noninverting Single Supply With Resistors

図 8-10 shows a typical inverting-amplifier circuit. With a 5-V single-supply, a mid-supply reference generator is needed to bias the positive side through R_1. To cancel the voltage offset that would otherwise be caused by the input bias currents, R_1 is selected to be equal to R_F in parallel with R_G. For example, if a gain of –2 is required and R_F = 2 kΩ, select R_G = 1 kΩ to set the gain and R_1 = 667 Ω for bias current cancellation. The value for C is dependent on the reference, but TI recommends a value of at least 0.1 µF to limit noise into the op amp.

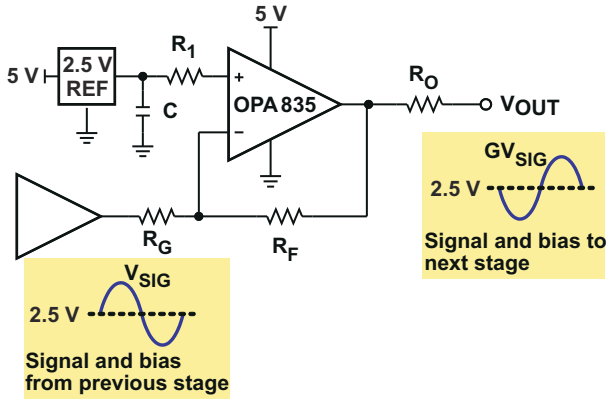


図 8-10. Inverting Single Supply With Reference

図 8-11 shows a similar inverting single-supply scenario with the reference generator replaced by the Thevenin equivalent using resistors and the positive supply. R_1 and R_2 form a resistor divider from the 5-V supply and are used to bias the positive side. To cancel the voltage offset that would otherwise be caused by the input bias currents, set the parallel sum of R_1 and R_2 equal to the parallel sum of R_F and R_G. C must be added to limit coupling of noise into the positive input. For example, if gain of –2 is required and R_F = 2 kΩ, select R_G = 1 kΩ to set the gain. $R_1 = R_2$ = 667 Ω for mid-supply voltage bias and for op-amp input-bias current cancellation. A good value for C is 0.1 µF. The resistor divider costs less than the 2.5-V reference in 図 8-10 but may increase the current from the 5-V supply.

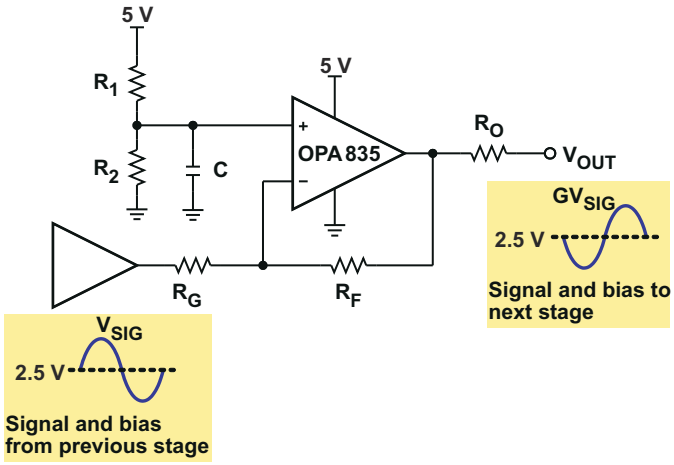


図 8-11. Inverting Single Supply With Resistors

9 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

9.1 Application Information

9.1.1 Noninverting Amplifier

The OPA835 and OPA2835 devices can be used as noninverting amplifiers with signal input to the noninverting input, V_{IN+}. A basic block diagram of the circuit is shown in 図 8-1.

If $V_{IN} = V_{REF} + V_{SIG}$, the amplifier output may be calculated according to 式 1.

$$V_{OUT} = V_{SIG}\left(1 + \frac{R_F}{R_G}\right) + V_{REF} \quad (1)$$

The signal gain of the circuit is set by $G = 1 + \frac{R_F}{R_G}$, and V_{REF} provides a reference around which the input and output signals swing. Output signals are in-phase with the input signals.

The OPA835 and OPA2835 devices are designed for the nominal value of R_F to be 2 kΩ in gains other than +1. This gives excellent distortion performance, maximum bandwidth, best flatness, and best pulse response. R_F = 2 kΩ must be used as a default unless other design goals require changing to other values. All test circuits used to collect data for this data sheet had R_F = 2 kΩ for all gains other than +1. A gain of +1 is a special case where R_F is shorted and R_G is left open.

9.1.2 Inverting Amplifier

The OPA835 and OPA2835 devices can be used as inverting amplifiers with signal input to the inverting input, $V_{IN–}$, through the gain-setting resistor R_G. A basic block diagram of the circuit is shown in 図 8-2.

If $V_{IN} = V_{REF} + V_{SIG}$, the output of the amplifier may be calculated according to 式 2.

$$V_{OUT} = V_{SIG}\left(\frac{-R_F}{R_G}\right) + V_{REF} \quad (2)$$

The signal gain of the circuit $G = \frac{-R_F}{R_G}$ and V_{REF} provides a reference point around which the input and output signals swing. Output signals are 180° out-of-phase with the input signals. The nominal value of R_F must be 2 kΩ for inverting gains.

9.1.3 Instrumentation Amplifier

図 9-1 is an instrumentation amplifier that combines the high input impedance of the differential-to-differential amplifier circuit and the common-mode rejection of the differential-to-single-ended amplifier circuit. This circuit is often used in applications where high input impedance is required (such as taps from a differential line) or in cases where the signal source is a high impedance.

If $V_{IN+} = V_{CM} + V_{SIG+}$ and $V_{IN–} = V_{CM} + V_{SIG–}$, the output of the amplifier may be calculated according to 式 3.

$$V_{OUT} = (V_{IN+} - V_{IN–}) \times \left(1 + \frac{2R_{F1}}{R_{G1}}\right)\left(\frac{R_{F2}}{R_{G2}}\right) + V_{REF} \quad (3)$$

The signal gain of the circuit is $G = \left(1 + \frac{2R_{F1}}{R_{G1}}\right)\left(\frac{R_{F2}}{R_{G2}}\right)$. V_{CM} is rejected, and V_{REF} provides a level shift around which the output signal swings. The single-ended output signal is in-phase with the differential input signal.

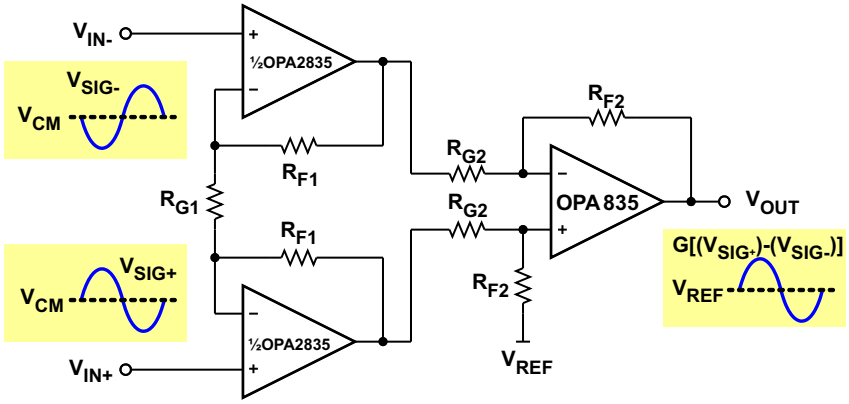


図 9-1. Instrumentation Amplifier

Integrated solutions are available, but the OPA835 device provides a much lower-power, high-frequency solution. For best CMRR performance, resistors must be matched. A good rule of thumb is CMRR ≈ the resistor tolerance; so 0.1% tolerance will provide approximately 60-dB CMRR.

9.1.4 Attenuators

The noninverting circuit shown in 図 8-1 has a minimum gain of 1. To implement attenuation, a resistor divider can be placed in series with the positive input, and the amplifier set for a gain of 1 by shorting V_{OUT} to $V_{IN–}$ and removing R_G. Because the op amp input is high impedance, the resistor divider sets the attenuation.

The inverting circuit of 図 8-2 is used as an attenuator by making R_G larger than R_F. The attenuation is the resistor ratio. For example, a 10:1 attenuator can be implemented with R_F = 2 kΩ and R_G = 20 kΩ.

9.1.5 Single-Ended to Differential Amplifier

図 9-2 shows an amplifier circuit that converts single-ended signals to differential signals and provides gain and level shifting. This circuit can convert signals to differential in applications such as driving Cat5 cabling or driving differential-input SAR and ΔΣ ADCs.

By setting $V_{IN} = V_{REF} + V_{SIG}$, then the output of the amplifier may be calculated according to 式 4.

$$V_{OUT+} = G \times V_{IN} + V_{REF} \quad \text{and} \quad V_{OUT-} = -G \times V_{IN} + V_{REF} \quad \text{Where: } G = 1 + \frac{R_F}{R_G} \tag{4}$$

The differential-signal gain of the circuit is 2 × G, and V_{REF} provides a reference around which the output signal swings. The differential output signal is in-phase with the single-ended input signal.

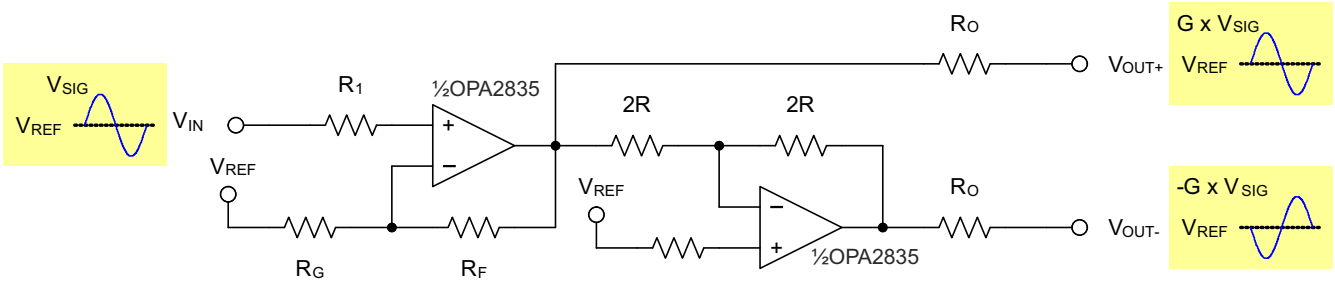


図 9-2. Single-Ended to Differential Amplifier

Line termination on the output can be accomplished with resistors R_O. The differential impedance seen from the line will be 2 × R_O. For example, if 100-Ω Cat5 cable is used with double termination, the amplifier is typically set for a differential gain of 2 V/V (6 dB) with R_F = 0 Ω (short) R_G = ∞Ω (open), 2R = 2 kΩ, R1 = 0 Ω, R = 1 kΩ to balance the input bias currents, and R_O = 49.9 Ω for output line termination. This configuration is shown in 図 9-3.

For driving a differential-input ADC the situation is similar, but the output resistors, R_O, are selected with a capacitor across the ADC input for optimum filtering and settling-time performance.

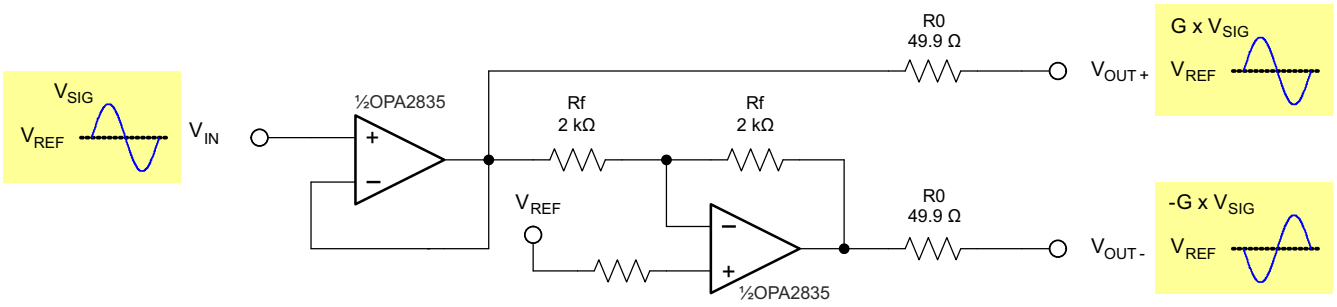


図 9-3. Cat5 Line Driver With Gain = 2 V/V (6 dB)

9.1.6 Differential to Single-Ended Amplifier

図 9-4 shows a differential amplifier that converts differential signals to single-ended and provides gain (or attenuation) and level shifting. This circuit can be used in applications like a line receiver for converting a differential signal from a Cat5 cable to a single-ended signal.

If $V_{IN+} = V_{CM} + V_{SIG+}$ and $V_{IN-} = V_{CM} + V_{SIG-}$, then the output of the amplifier may be calculated according to 式 5.

$$V_{OUT} = \left(V_{IN+} - V_{IN-}\right) \times \left(\frac{R_F}{R_G}\right) + V_{REF} \tag{5}$$

The signal gain of the circuit is $G = \frac{R_F}{R_G}$, V_{CM} is rejected, and V_{REF} provides a level shift around which the output signal swings. The single-ended output signal is in-phase with the differential input signal.

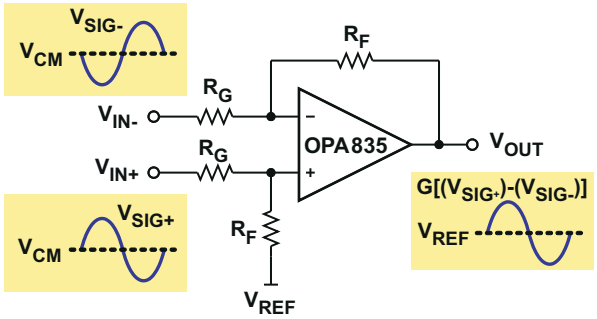


図 9-4. Differential to Single-Ended Amplifier

Line termination can be accomplished by adding a shunt resistor across the VIN+ and VIN- inputs. The differential impedance is the shunt resistance in parallel with the input impedance of the amplifier circuit, which is usually much higher. For low gain and low line impedance, the resistor value to add is approximately the impedance of the line. For example, if a 100-Ω Cat5 cable is used with a gain of 1 amplifier and R_F = R_G = 2 kΩ, adding a 100-Ω shunt across the input will give a differential impedance of 99 Ω, which is adequate for most applications.

For best CMRR performance, resistors must be matched. Assuming CMRR ≈ the resistor tolerance, a 0.1% tolerance will provide about 60-dB CMRR.

9.1.7 Differential-to-Differential Amplifier

図 9-5 shows a differential amplifier that is used to amplify differential signals. This circuit has high input impedance and is used in differential line driver applications where the signal source is a high-impedance driver (for example, a differential DAC) that must drive a line.

If the user sets $V_{IN\pm} = V_{CM} + V_{SIG\pm}$, then the output of the amplifier may be calculated according to 式 6.

$$V_{OUT\pm} = V_{IN\pm} \times \left(1 + \frac{2R_F}{R_G}\right) + V_{CM} \tag{6}$$

The signal gain of the circuit is $G = 1 + \frac{2R_F}{R_G}$, and V_{CM} passes with unity gain. The amplifier combines two noninverting amplifiers into one differential amplifier that shares the R_G resistor, which makes R_G effectively ½ its value when calculating the gain. The output signals are in-phase with the input signals.

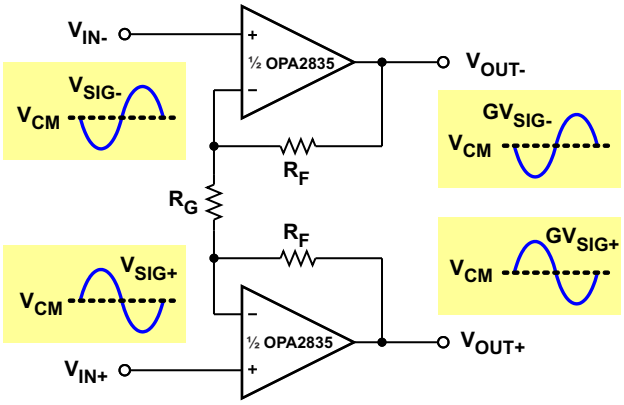


図 9-5. Differential-to-Differential Amplifier

9.1.8 Gain Setting With OPA835 RUN Integrated Resistors

The OPA835 RUN package option includes integrated gain-setting resistors for the smallest possible footprint on a printed circuit board (≈ 2.00 mm x 2.00 mm). By adding circuit traces on the PCB, gains of +1, –1, –1.33, +2, +2.33, -3, +4, –4, +5, –5.33, +6.33, –7, +8 and inverting attenuations of –0.1429, –0.1875, –0.25, –0.33, –0.75 can be achieved.

図 9-6 shows a simplified view of how the OPA835IRUN integrated gain-setting network is implemented. 表 9-1 lists the required pin connections for various noninverting and inverting gains (reference 図 8-1 and 図 8-2). 表 9-2 lists the required pin connections for various attenuations using the inverting-amplifier architecture (reference 図 8-2). Due to ESD protection devices being used on all pins, the absolute maximum and minimum input voltage range, $V_{S–}$ – 0.7 V to V_{S+} + 0.7 V, applies to the gain-setting resistors, and so attenuation of large input voltages will require external resistors to implement.

The gain-setting resistors are laser trimmed to 1% tolerance with nominal values of 2.4 kΩ, 1.8 kΩ, and 600 Ω. The gain-setting resistors have excellent temperature coefficient, and gain tracking is superior to using external gain-setting resistors. The 800-Ω resistor and 1.25-pF capacitor in parallel with the 2.4-kΩ gain-setting resistor provide compensation for best stability and pulse response.

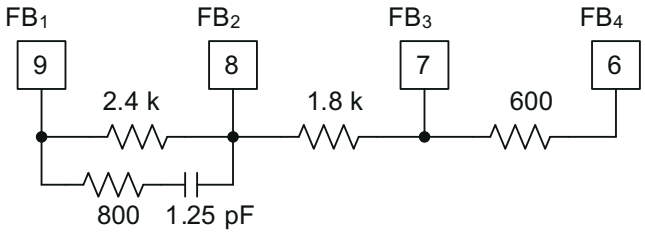


図 9-6. OPA835IRUN Gain-Setting Network

表 9-1. Gain Settings

NONINVERTING GAIN (図 8-1)	INVERTING GAIN (図 8-2)	SHORT PINS	SHORT PINS	SHORT PINS	SHORT PINS
1 V/V (0 dB)	—	1 to 9			—
2 V/V (6.02 dB)	–1 V/V (0 dB)	1 to 9	2 to 8	6 to GND	—
2.33 V/V (7.36 dB)	–1.33 V/V (2.5 dB)	1 to 9	2 to 8	7 to GND	—
4 V/V (12.04 dB)	–3 V/V (9.54 dB)	1 to 8	2 to 7	6 to GND	—
5 V/V (13.98 dB)	–4 V/V (12.04 dB)	1 to 9	2 to 7 or 8	7 to 8	6 to GND
6.33 V/V (16.03 dB)	–5.33 V/V (14.54 dB)	1 to 9	2 to 6 or 8	6 to 8	7 to GND
8 V/V (18.06 dB)	–7 V/V (16.90 dB)	1 to 9	2 to 7	6 to GND	—

表 9-2. Attenuator Settings

INVERTING GAIN (図 8-2)	SHORT PINS	SHORT PINS	SHORT PINS	SHORT PINS
–0.75 V/V (–2.5 dB)	1 to 7	2 to 8	9 to GND	—
–0.333 V/V (–9.54 dB)	1 to 6	2 to 7	8 to GND	—
–0.25 V/V (–12.04 dB)	1 to 6	2 to 7 or 8	7 to 8	9 to GND
–0.1875 V/V (–14.54 dB)	1 to 7	2 to 6 or 8	6 to 8	9 to GND
–0.1429 V/V (–16.90 dB)	1 to 6	2 to 7	9 to GND	—

9.1.9 Pulse Application With Single-Supply

For pulsed applications where the signal is at ground and pulses to a positive or negative voltage, the circuit bias-voltage considerations differ from those in an application with a signal that swings symmetrically about a reference point. 図 9-7 shows a circuit where the signal is at ground (0 V) and pulses to a positive value.

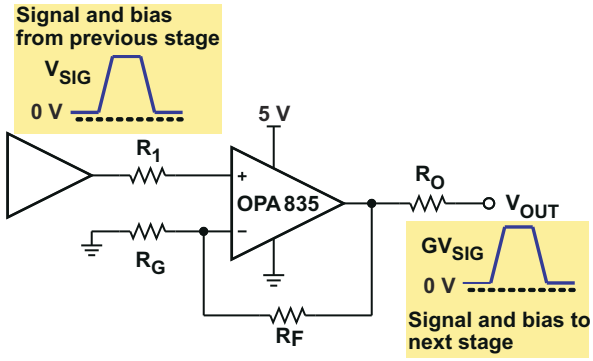


図 9-7. Noninverting Single Supply With Pulse

If the input signal pulses negative from ground, an inverting amplifier is more appropriate, as shown in 図 9-8. A key consideration in noninverting and inverting cases is that the input and output voltages are kept within the limits of the amplifier. Because the V_{ICR} of the OPA835 device includes the negative supply rail, the OPA835 op amp is well-suited for this application.

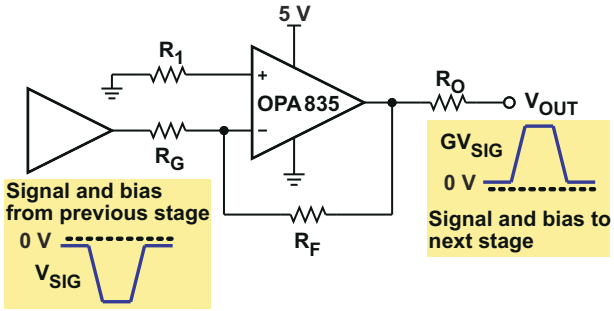


図 9-8. Inverting Single Supply With Pulse

9.1.10 ADC Driver Performance

The OPA835 device provides excellent performance when driving high-performance delta-sigma (ΔΣ) and successive-approximation-register (SAR) ADCs in low-power audio and industrial applications.

To show achievable performance, the OPA835 device is tested as the drive amplifier for the ADS8326 device. The ADS8326 device is a 16-bit, micro power, SAR ADC with pseudodifferential inputs and sample rates up to 250 kSPS. The device offers excellent noise and distortion performance in a small 8-pin SOIC or VSSOP (MSOP) package. Low power and small size make the ADS8326 and OPA835 devices an ideal solution for portable and battery-operated systems, remote data-acquisition modules, simultaneous multichannel systems, and isolated data acquisition.

With the circuit shown in 図 9-9 to test the performance, 図 9-10 shows the spectral performance with a 10-kHz input frequency. The tabulated AC results are in 表 9-3.

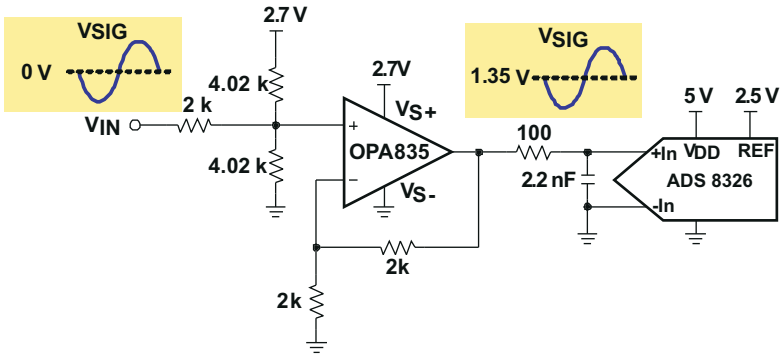


図 9-9. OPA835 and ADS8326 Test Circuit

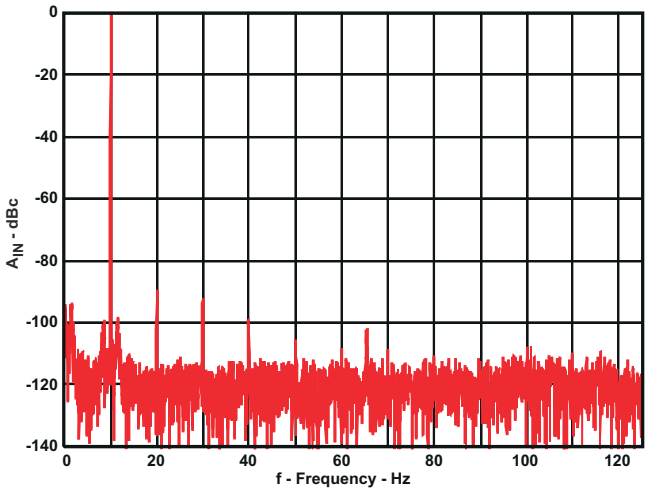


図 9-10. ADS8326 and OPA835 10-kHz FFT

表 9-3. AC Analysis

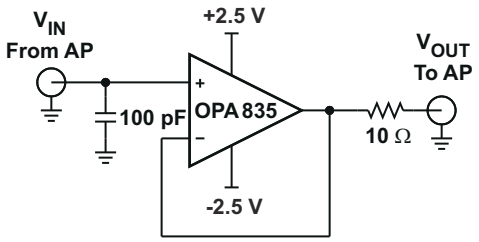
TONE (Hz)	SIGNAL (dBFS)	SNR (dBc)	THD (dBc)	SINAD (dBc)	SFDR (dBc)
10k	–0.85	81.9	–87.5	80.8	89.9

9.2 Typical Application

9.2.1 Audio Frequency Performance

The OPA835 and OPA2835 devices provide excellent audio performance with low quiescent power. To show performance in the audio band, an audio analyzer from Audio Precision (2700 series) tests THD+N and FFT at 1 V_{RMS} output voltage.

図 9-11 shows the test circuit used for the audio-frequency performance application.



The 100-pF capacitor to ground on the input helped to decouple noise pick up in the lab and improved noise performance.

図 9-11. OPA835 Audio Precision Analyzer Test Circuit

9.2.1.1 Design Requirements

Design a low distortion, single-ended input to single-ended output audio amplifier using the OPA835 device. The 2700 series audio analyzer from Audio Precision is the signal source and the measurement system.

表 9-4. Design Requirements

CONFIGURATION	INPUT EXCITATION	PERFORMANCE TARGET	R_{LOAD}
OPA835 Unity Gain Config.	1 KHz Tone Frequency	> 110 dBc SFDR	300 Ω and 100 KΩ

9.2.1.2 Detailed Design Procedure

The OPA835 device is tested in this application in a unity-gain buffer configuration. A buffer configuration is selected as the configuration maximizes the loop gain of the amplifier configuration. At higher closed-loop gains, the loop gain of the circuit reduces, which results in degraded harmonic distortion. The relationship between distortion and closed loop gain at a fixed input frequency can be seen in 図 7-36 in *セクション 7.9*. The test was performed under varying output-load conditions using a resistive load of 300 Ω and 100 KΩ. 図 7-34 shows the distortion performance of the amplifier versus the output resistive load. Output loading, output swing, and closed-loop gain play a key role in determining the distortion performance of the amplifier.

注

The 100-pF capacitor to ground on the input helped to decouple noise pickup in the lab and improved noise performance.

The Audio Precision was configured as a single-ended output in this application circuit. In applications where a differential output is available, the OPA835 device can be configured as a differential to single-ended amplifier as shown in 図 9-4. Power supply bypassing is critical to reject noise from the power supplies. A 2.2-µF power-supply decoupling capacitor must be placed within two inches of the device and can be shared with other op amps on the same board. A 0.1-µF decoupling capacitor must be placed as close to the power supply pins as possible, preferably within 0.1 inch. For split supply, a capacitor is required for both supplies. A 0.1-µF capacitor placed directly between the supplies is also beneficial for improving system noise performance. If the output load is heavy, from 16 Ω to 32 Ω, amplifier performance could begin to degrade. To drive such heavy loads, both channels of the OPA2835 device can be paralleled with the outputs isolated with 1-Ω resistors to reduce the loading effects.

9.2.1.3 Application Curves

A 10-Ω series resistor can be inserted between the capacitor and the noninverting pin to isolate the capacitance.

図 9-12 shows the THD+N performance with 100-kΩ and 300-Ω loads, and with no weighting and A-weighting. With no weighting, the THD+N performance is dominated by the noise for both loads. A-weighting provides filtering that improves the noise so a larger difference can be seen between the loads due to more distortion with R_L = 300 Ω.

図 9-13 and 図 9-14 show FFT output with a 1-kHz tone and 100-kΩ and 300-Ω loads. To show relative performance of the device versus the test set, one channel has the OPA835 device in-line between generator output and analyzer input, and the other channel is in “Gen Mon” loopback mode, which internally connects the signal generator to the analyzer input. With 100-kΩ load (see 図 9-13), the curves are indistinguishable from each other except for noise, which means the OPA835 device cannot be directly measured. With a 300-Ω load as shown in 図 9-14, the main difference between the curves is the OPA835 device due to the higher even-order harmonics. The test-set performance masks the odd-order harmonics.

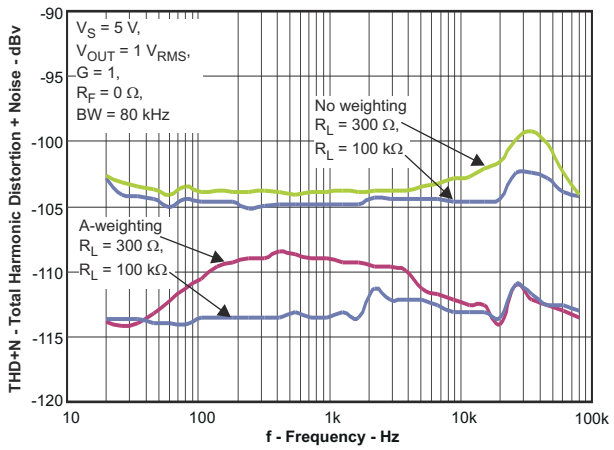


図 9-12. OPA835 1 V_{RMS} 20 Hz to 80 kHz THD+N

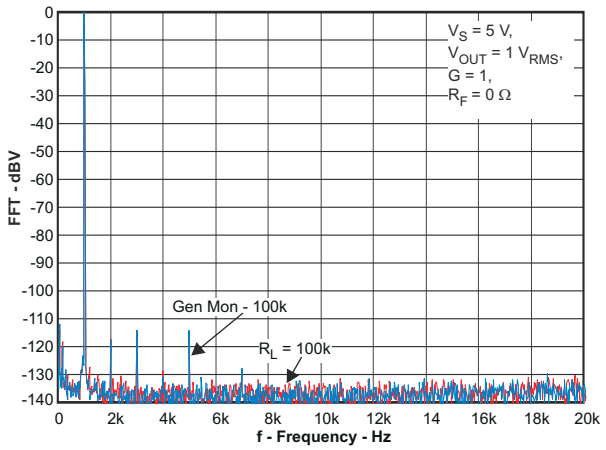


図 9-13. OPA835 and AP Gen Mon 1-kHz FFT Plot; V_{OUT} = 1 V_{RMS}, R_L = 100 kΩ

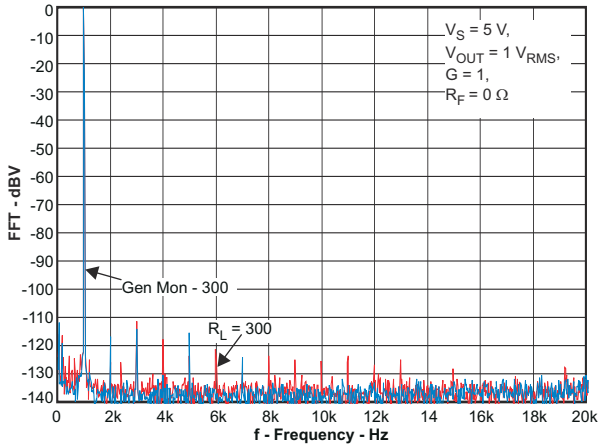


図 9-14. OPA835 and AP Gen Mon 1kHz FFT Plot; V_{OUT} = 1 V_{RMS}, R_L = 300 Ω

9.2.2 Active Filters

The OPA835 and OPA2835 devices are good choices for active filters. 図 9-16 and 図 9-15 show MFB and Sallen-Key circuits designed using the *WEBENCH® Filter Designer* to implement second-order low-pass Butterworth filter circuits. 図 9-17 shows the frequency response.

Other MFB and Sallen-Key filter circuits display similar performance. The main difference is the MFB is an inverting amplifier in the pass band and the Sallen-Key is noninverting. The primary advantage for each is the Sallen-Key in unity gain has no resistor gain error term, and thus no sensitivity to gain error, while the MFB has better attenuation properties beyond the bandwidth of the op amp.

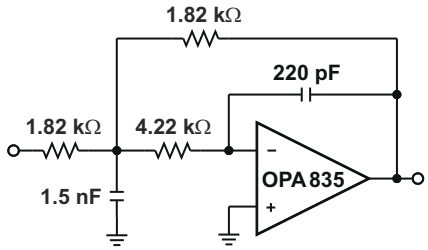


図 9-15. MFB 100-kHz Second-Order Low-Pass Butterworth Filter Circuit

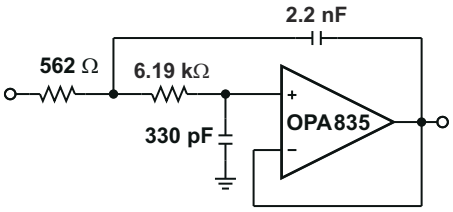


図 9-16. Sallen-Key 100-kHz Second-Order Low-Pass Butterworth Filter Circuit

9.2.2.1 Application Curve

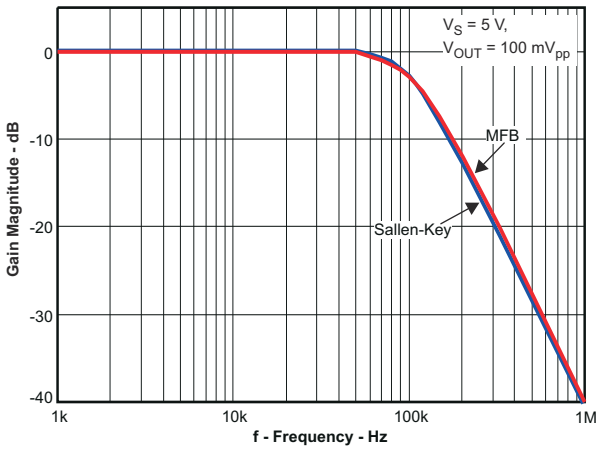


図 9-17. MFB and Sallen-Key Second-Order Low-Pass Butterworth Filter Response

10 Power Supply Recommendations

The OPAx835 devices are intended to work in a supply range of 2.7 V to 5 V. Supply-voltage tolerances are supported with the specified operating range of 2.5 V (7% on a 2.7-V supply) and 5.5 V (10% on a 5-V supply). Good power-supply bypassing is required. Minimize the distance (< 0.1 inch) from the power-supply pins to high frequency, 0.1-µF decoupling capacitors. A larger capacitor (2.2 µF is typical) is used along with a high frequency, 0.1-µF supply-decoupling capacitor at the device supply pins. For single-supply operation, only the positive supply has these capacitors. When a split supply is used, use these capacitors for each supply to ground. If necessary, place the larger capacitors further from the device and share these capacitors among several devices in the same area of the PCB. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. An optional supply decoupling capacitor across the two power supplies (for bipolar operation) reduces second harmonic distortion.

11 Layout

11.1 Layout Guidelines

The *OPA835 EVM* (SLOU314) can be used as a reference when designing the circuit board. TI recommends following the EVM layout of the external components near to the amplifier, ground plane construction, and power routing as closely as possible. General guidelines are listed below:

1. Signal routing must be direct and as short as possible into an out of the op amp.
2. The feedback path must be short and direct avoiding vias if possible, especially with G = +1.
3. Ground or power planes must be removed from directly under the negative input and output pins of the amplifier.
4. TI recommends placing a series output resistor as close to the output pin as possible. See 図 7-41 for recommended values for the expected capacitive load.
5. A 2.2-µF power-supply decoupling capacitor must be placed within two inches of the device and can be shared with other op amps. For split supply, a capacitor is required for both supplies.
6. A 0.1-µF power-supply decoupling capacitor must be placed as close to the supply pins as possible, preferably within 0.1 inch. For split supply, a capacitor is required for both supplies.
7. The $\overline{PD}$ pin uses TTL logic levels. If the pin is not used, it must tied to the positive supply to enable the amplifier. If the pin is used, it must be actively driven. A bypass capacitor is not necessary, but is used for robustness in noisy environments.

11.2 Layout Example

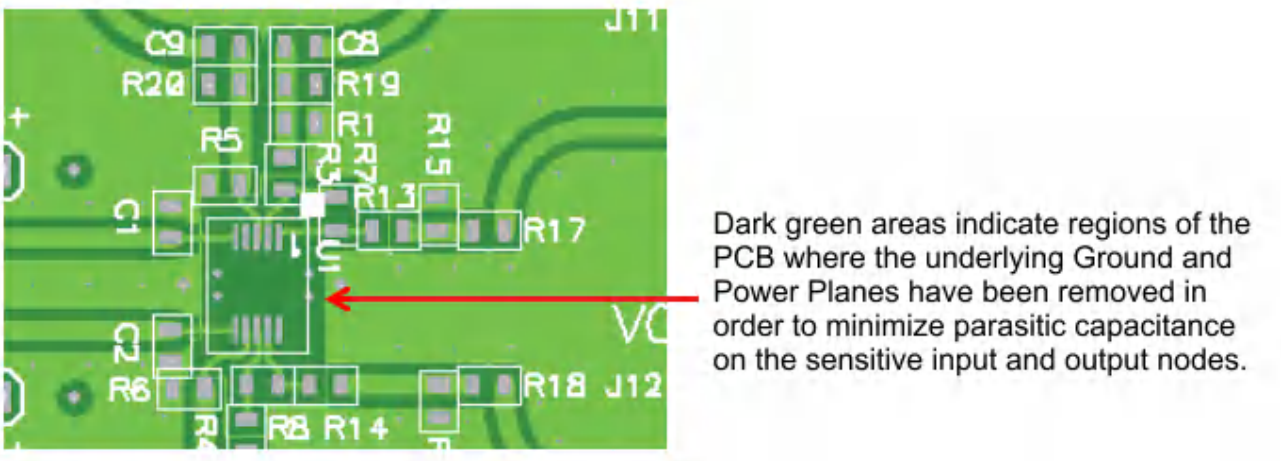


図 11-1. Top Layer

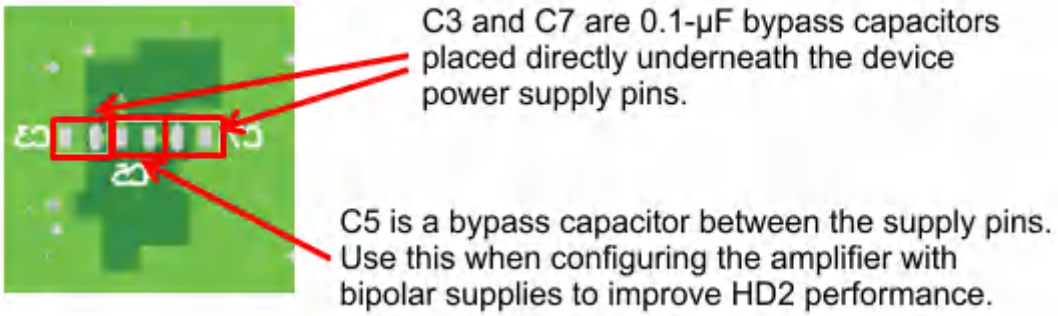


図 11-2. Bottom Layer

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

WEBENCH® Filter Designer

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *OPA835DBV, OPA836DBV EVM* user's guide

12.3 Related Links

表 12-1 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 12-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
OPA835	Click here	Click here	Click here	Click here	Click here
OPA2835	Click here	Click here	Click here	Click here	Click here

12.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.5 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の使用条件を参照してください。

12.6 Trademarks

TI E2E™ is a trademark of Texas Instruments.
WEBENCH® is a registered trademark of TI.
すべての商標は、それぞれの所有者に帰属します。

12.7 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.8 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2835ID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2835	Samples
OPA2835IDGS	ACTIVE	VSSOP	DGS	10	80	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2835	Samples
OPA2835IDGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2835	Samples
OPA2835IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2835	Samples
OPA2835IRMCR	ACTIVE	UQFN	RMC	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2835	Samples
OPA2835IRMCT	ACTIVE	UQFN	RMC	10	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2835	Samples
OPA2835IRUNR	ACTIVE	QFN	RUN	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2835	Samples
OPA2835IRUNT	ACTIVE	QFN	RUN	10	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2835	Samples
OPA835IDBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	QUM	Samples
OPA835IDBVT	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	QUM	Samples
OPA835IRUNR	ACTIVE	QFN	RUN	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	835	Samples
OPA835IRUNT	ACTIVE	QFN	RUN	10	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	835	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

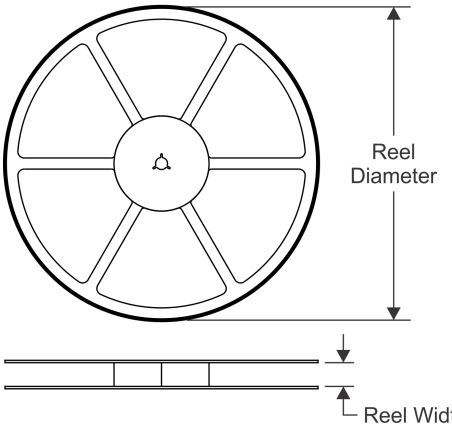
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

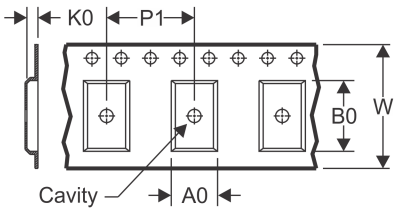
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

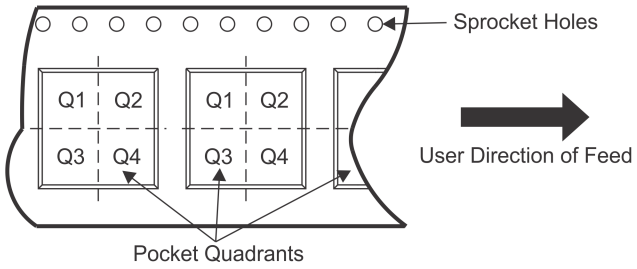


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

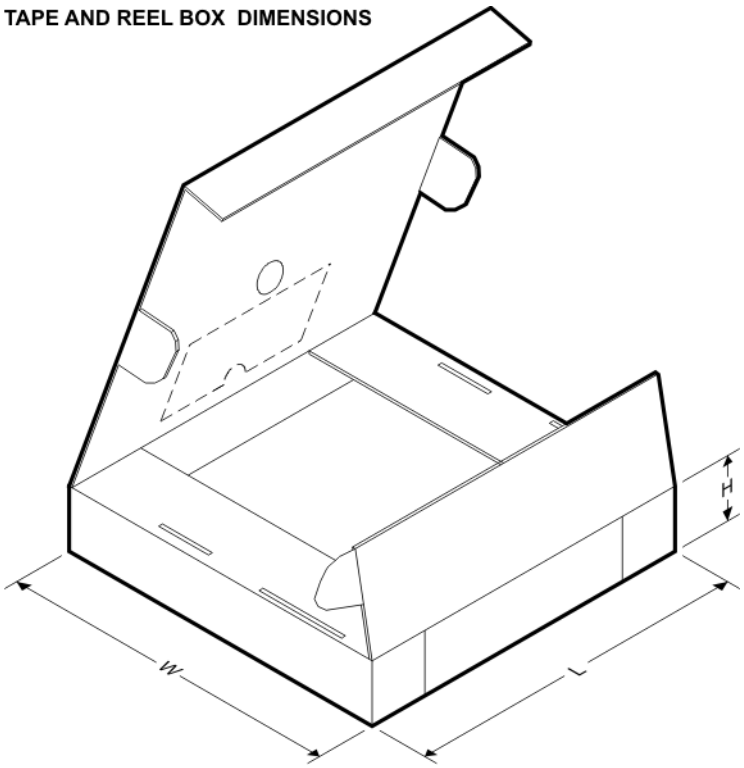
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2835IDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2835IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2835IRMCR	UQFN	RMC	10	3000	180.0	9.5	2.3	2.3	1.1	2.0	8.0	Q2
OPA2835IRMCT	UQFN	RMC	10	250	180.0	9.5	2.3	2.3	1.1	2.0	8.0	Q2
OPA2835IRUNR	QFN	RUN	10	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
OPA2835IRUNT	QFN	RUN	10	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
OPA835IDBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
OPA835IDBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
OPA835IRUNR	QFN	RUN	10	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
OPA835IRUNT	QFN	RUN	10	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

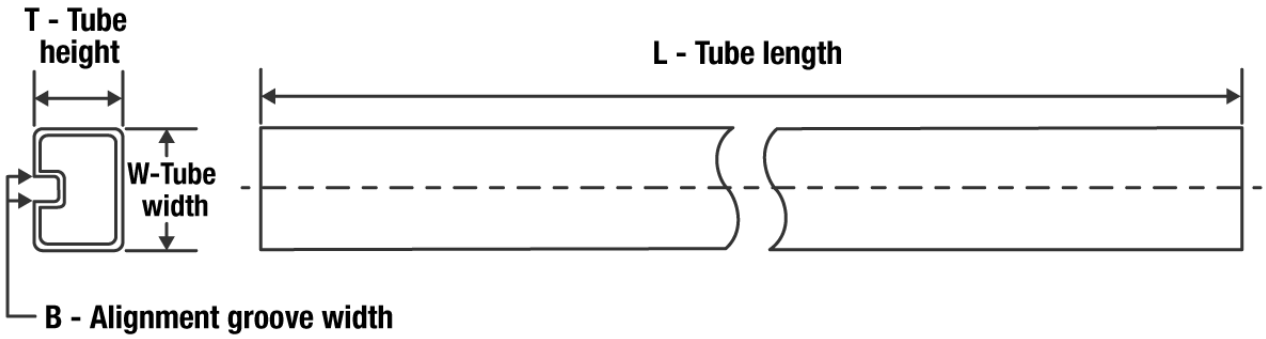
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2835IDGSR	VSSOP	DGS	10	2500	366.0	364.0	50.0
OPA2835IDR	SOIC	D	8	2500	340.5	336.1	25.0
OPA2835IRMCR	UQFN	RMC	10	3000	205.0	200.0	30.0
OPA2835IRMCT	UQFN	RMC	10	250	205.0	200.0	30.0
OPA2835IRUNR	QFN	RUN	10	3000	210.0	185.0	35.0
OPA2835IRUNT	QFN	RUN	10	250	210.0	185.0	35.0
OPA835IDBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
OPA835IDBVT	SOT-23	DBV	6	250	180.0	180.0	18.0
OPA835IRUNR	QFN	RUN	10	3000	210.0	185.0	35.0
OPA835IRUNT	QFN	RUN	10	250	210.0	185.0	35.0

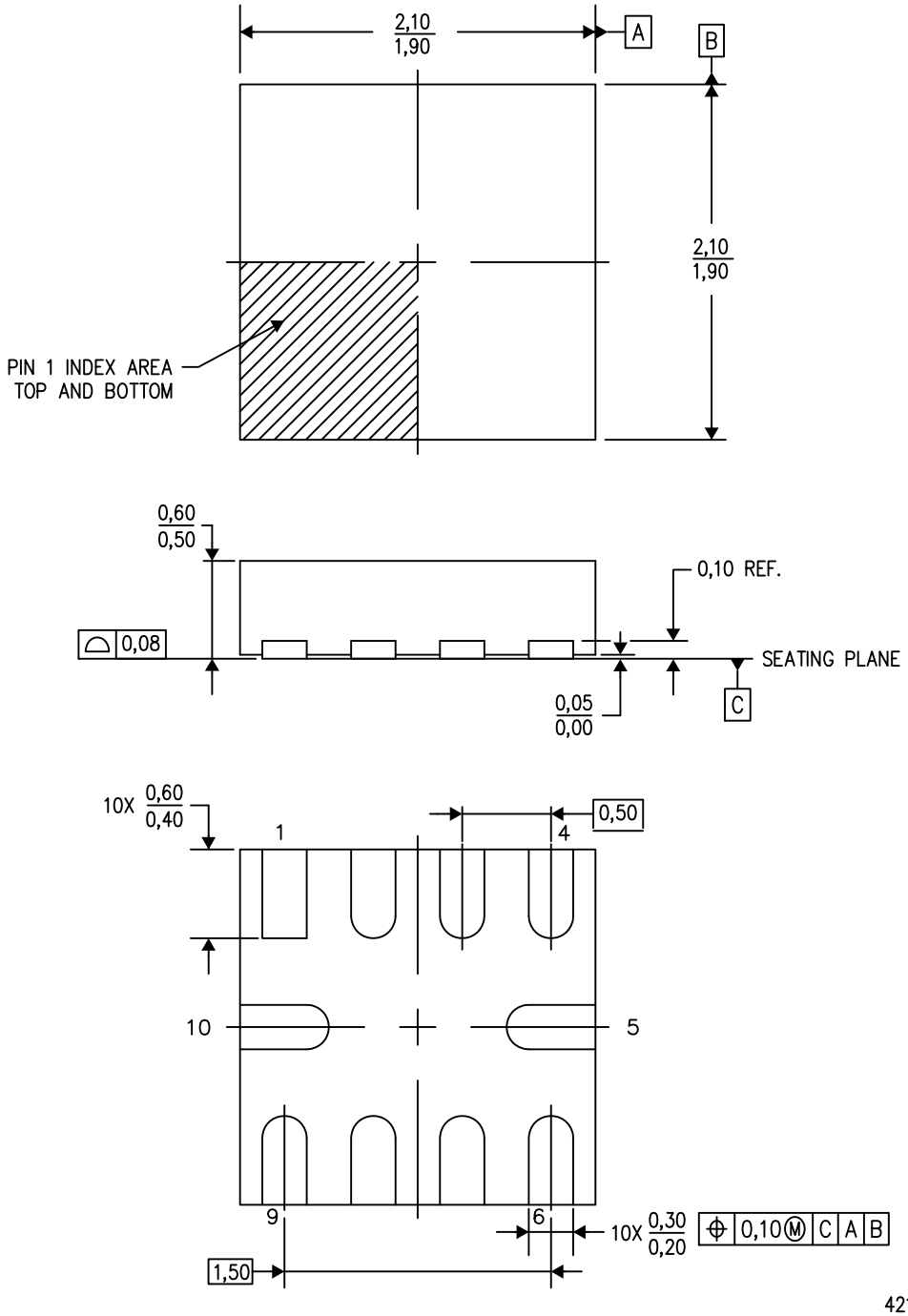
TUBE



*All dimensions are nominal

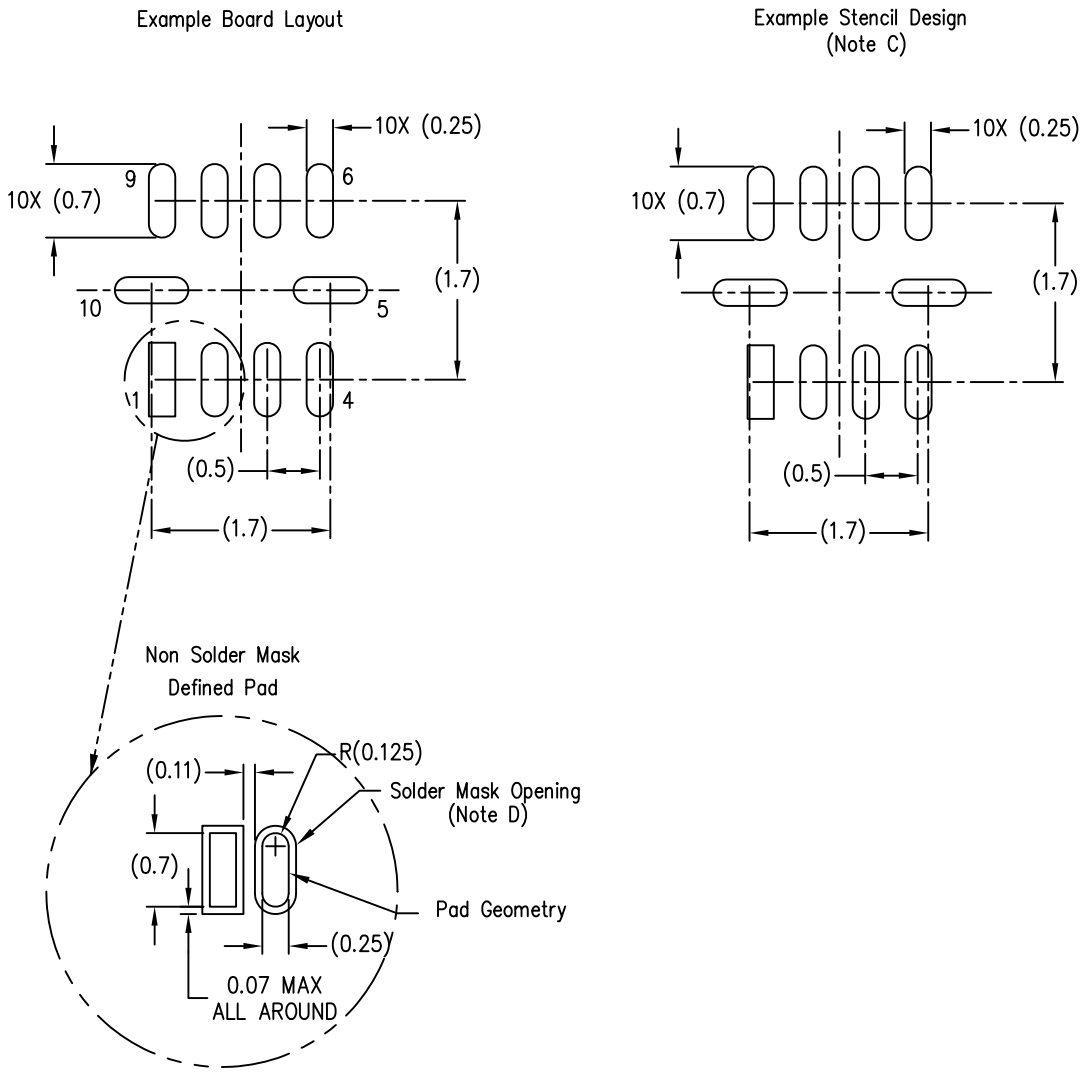
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA2835ID	D	SOIC	8	75	507	8	3940	4.32
OPA2835IDGS	DGS	VSSOP	10	80	330	6.55	500	2.88

RMC (S–PUQFN–N10) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.

RMC (S–PUQFN–N10) PLASTIC QUAD FLATPACK NO–LEAD



4221693/A 10/2014

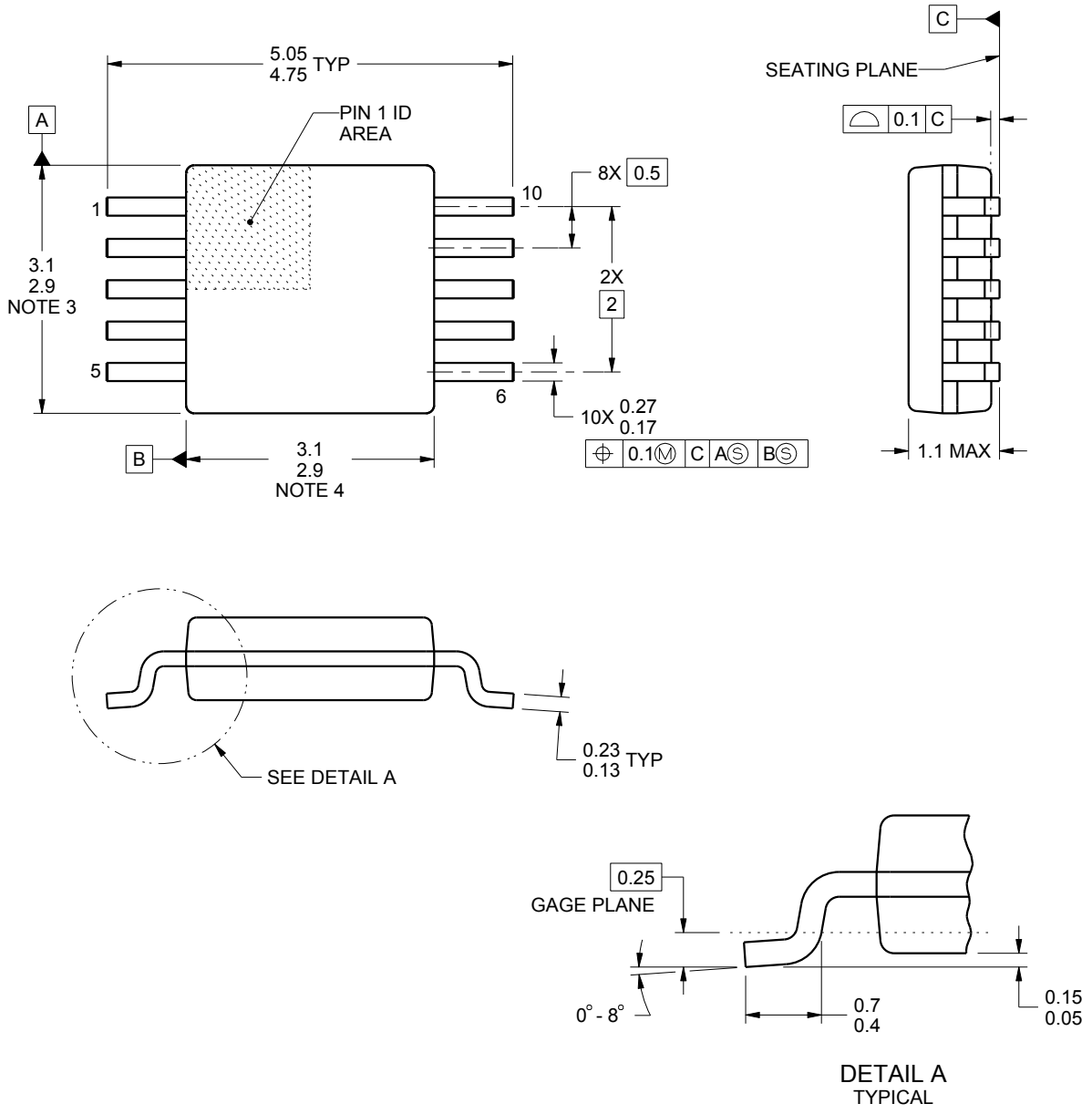
NOTES:
A. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only.
B. This drawing is subject to change without notice.
C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

PACKAGE OUTLINE

DGS0010A

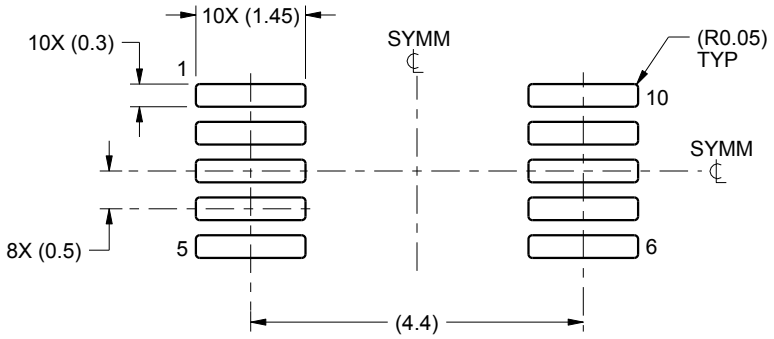
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

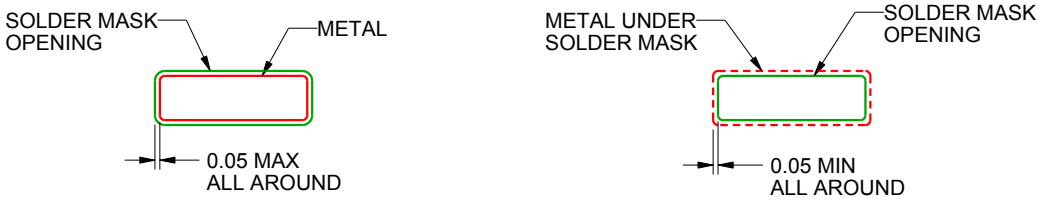


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

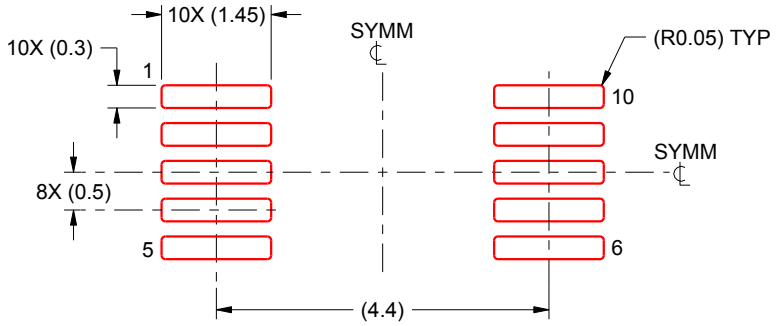


SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

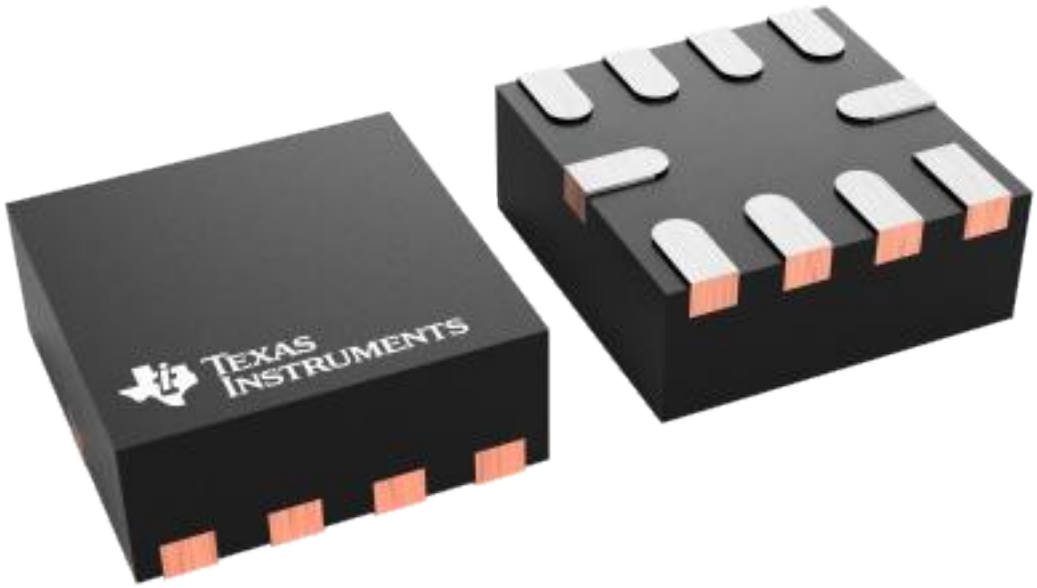
RUN 10

WQFN - 0.8 mm max height

2 X 2, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



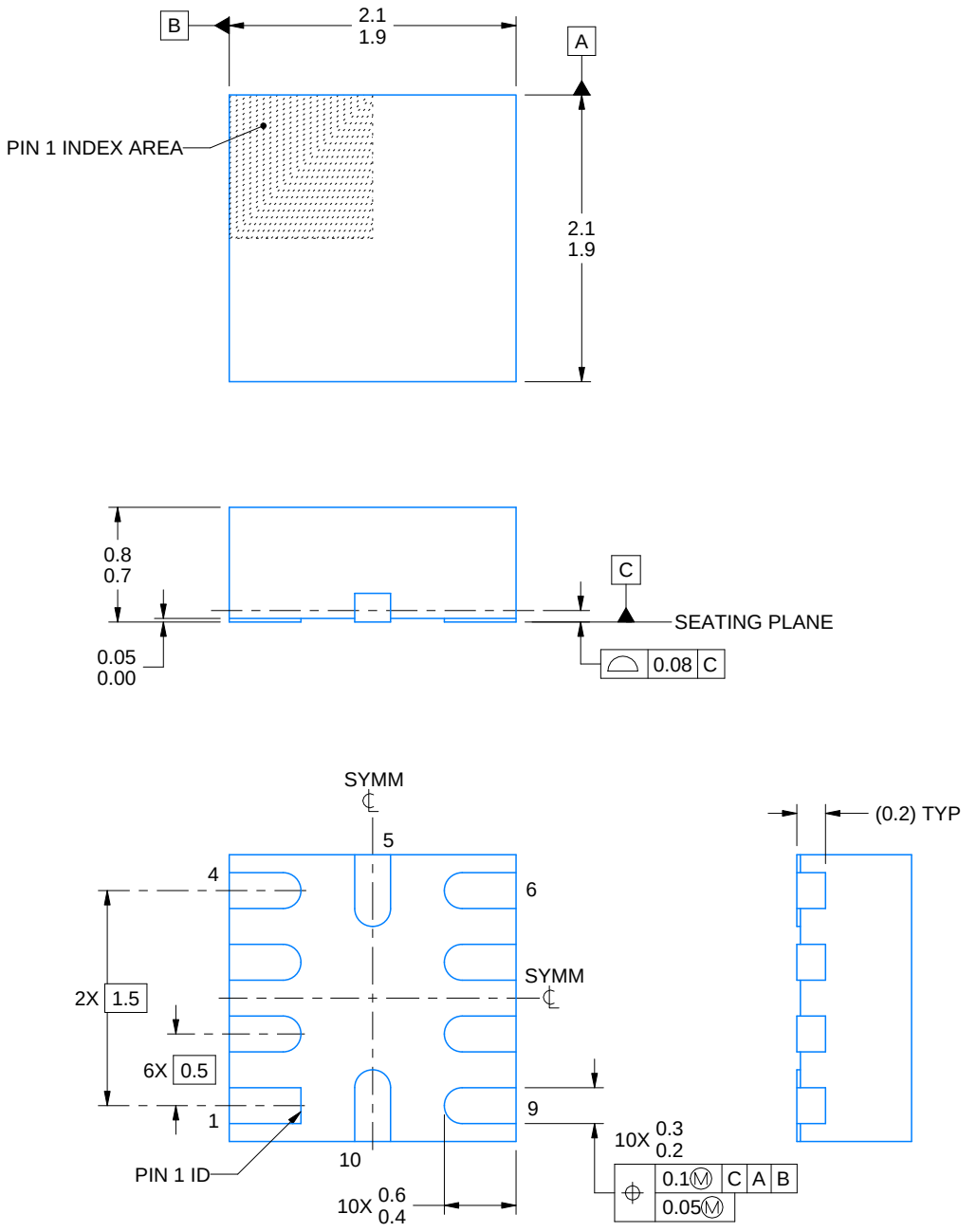
4228249/A

RUN0010A

PACKAGE OUTLINE

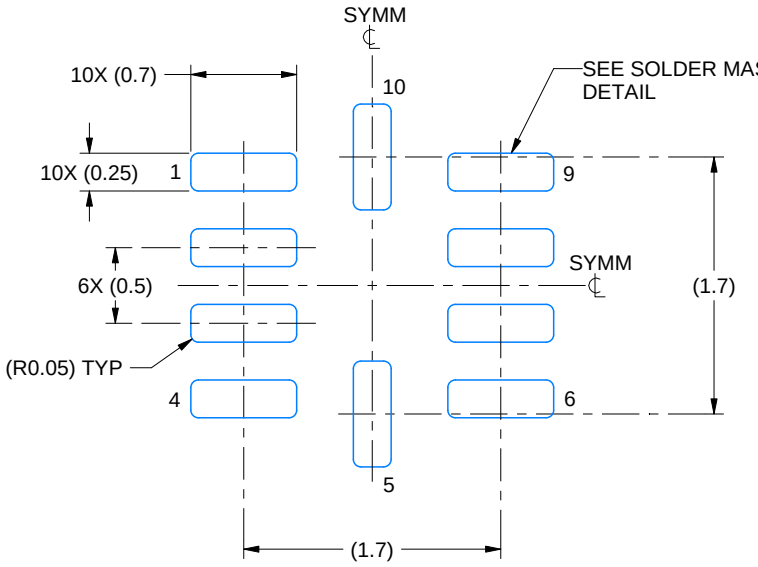
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

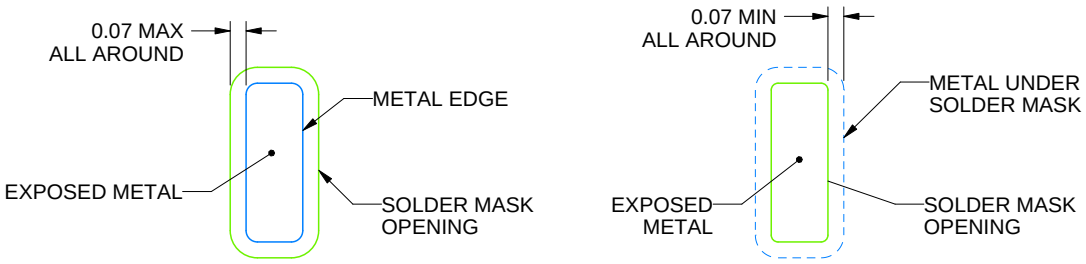


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

4220470/A 05/2020

NOTES: (continued)

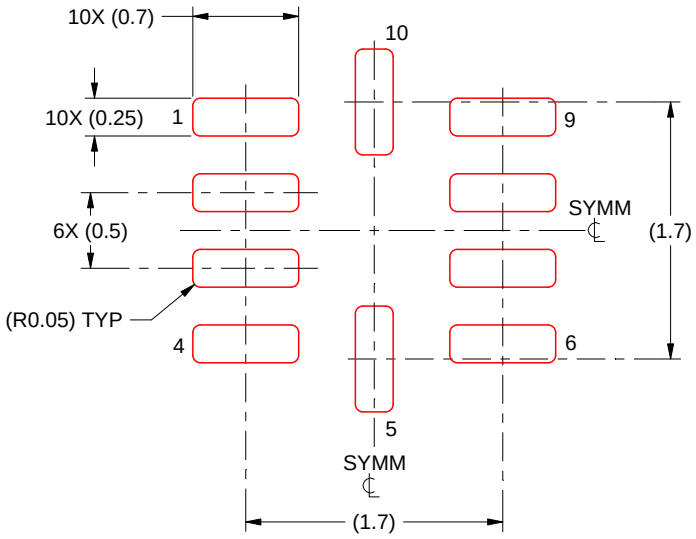
3. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

RUN0010A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

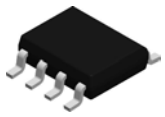


SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

4220470/A 05/2020

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

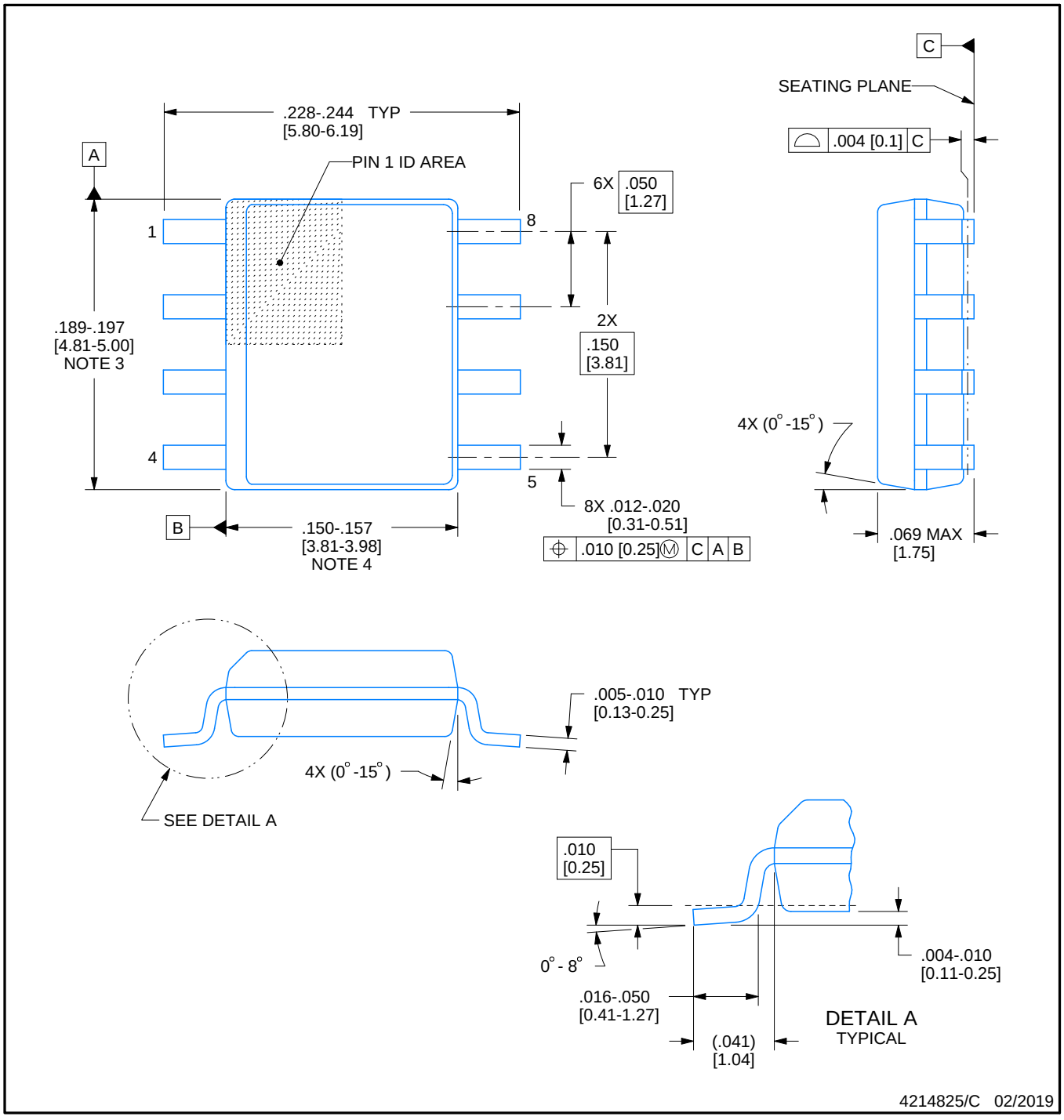


PACKAGE OUTLINE

D0008A

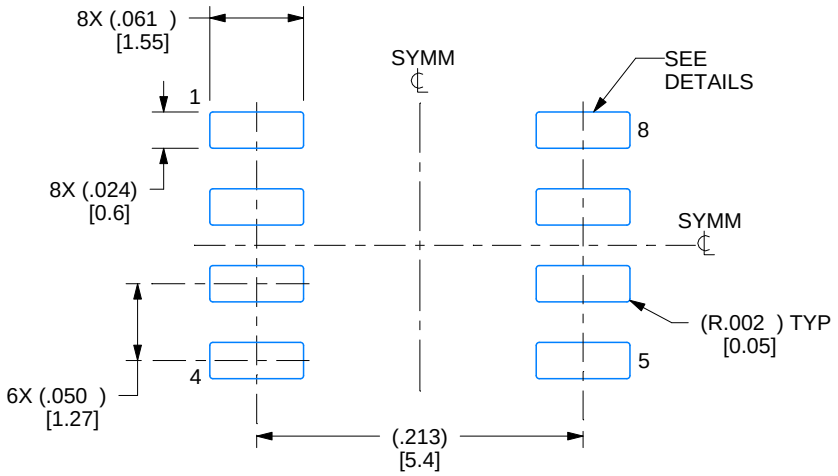
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

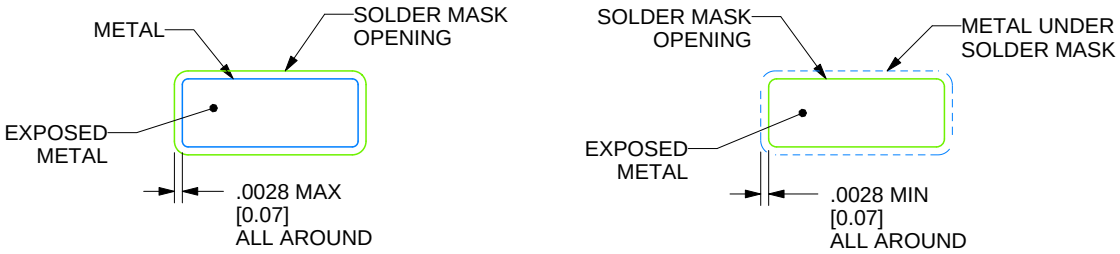


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

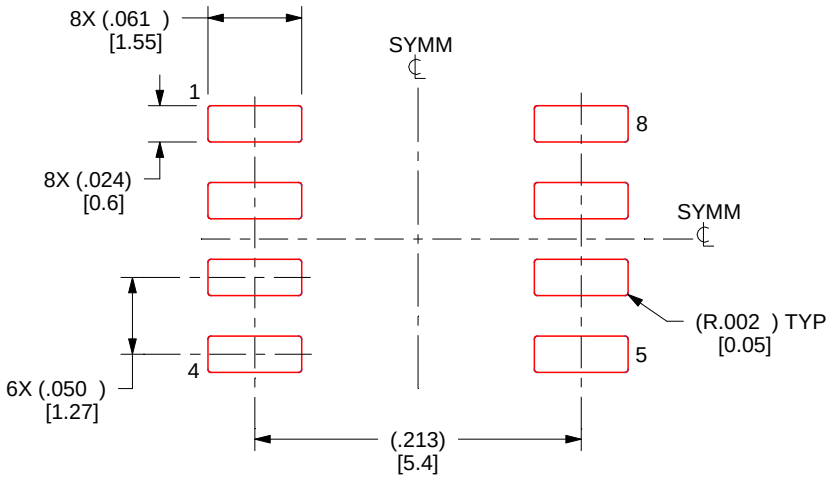
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

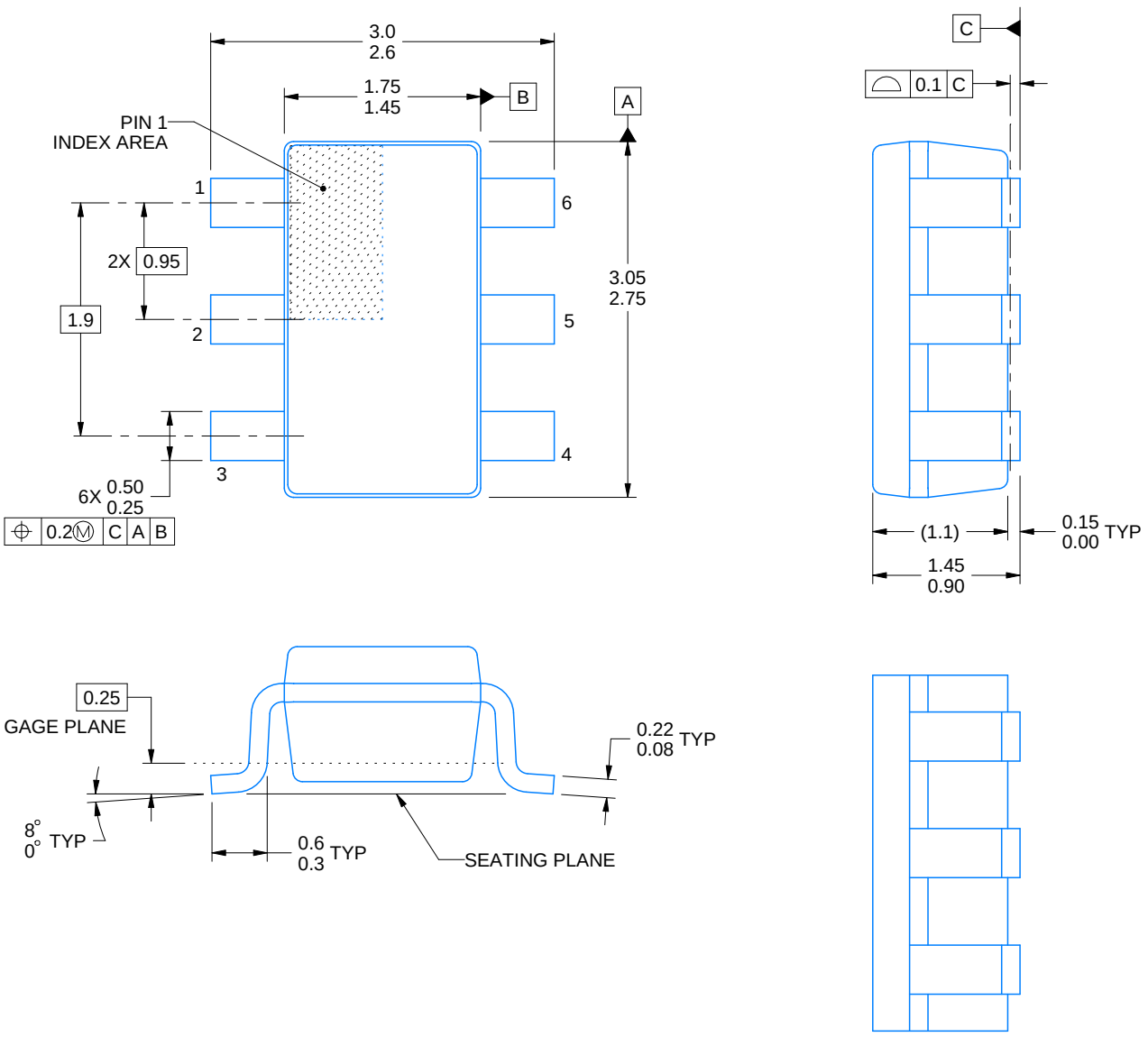
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

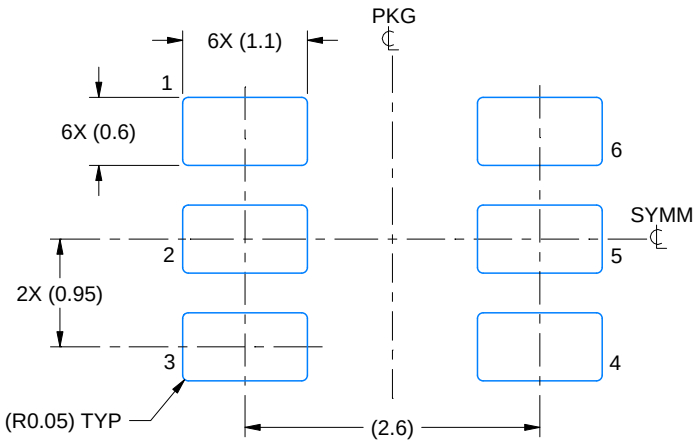


ALTERNATIVE PACKAGE SINGULATION VIEW

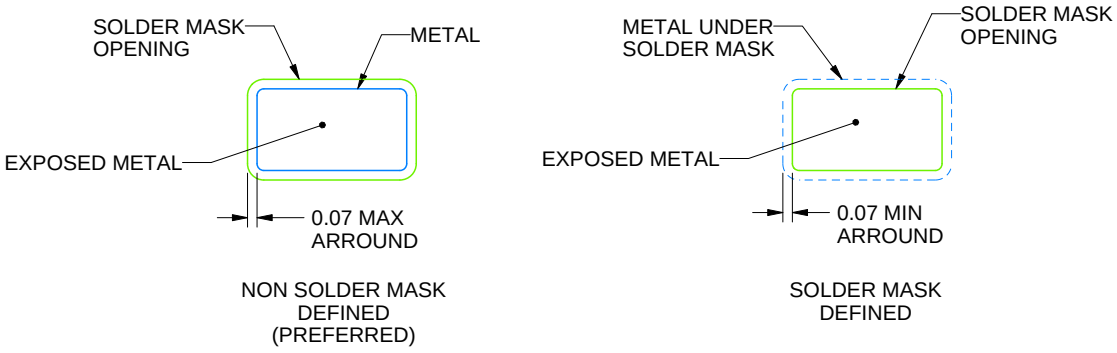
4214840/F 05/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

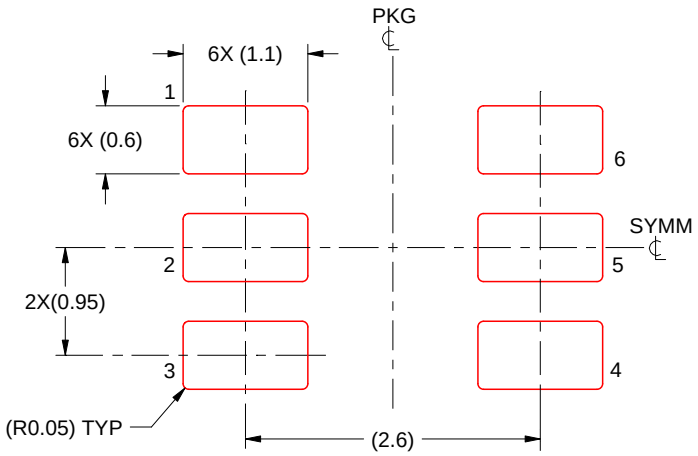


SOLDER MASK DETAILS

4214840/F 05/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/F 05/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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