SN74AHCT1G32 シングル 2 入力、正論理 OR ゲート

1 特長

- 動作範囲:4.5V～5.5V
- 最大 t_{pd} 8ns (5V 時)
- 低消費電力、最大 I_{CC}:10µA
- 5V で ±8mA の出力駆動能力
- 入力は TTL 電圧互換
- JESD 17 準拠
  250mA 超のラッチアップ性能

2 アプリケーション

- I/O モジュール:アナログ PLC/DCS 入力
- サーバー マザーボード
- オートモーティブ クラスタ
- モータ駆動および制御
- DLP フロント プロジェクション システム
- テレビ
- セットトップ ボックス
- オーディオ

3 概要

SN74AHCT1G32 はシングル 2 入力正論理 OR ゲートです。このデバイスはブール関数 Y = A + B or Y = $\overline{A \cdot B}$ を正論理で実行します。

表 3-1. パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)	本体サイズ (3)
SN74AHCT1G32	DBV (SOT-23、5)	2.90mm × 2.8mm	2.90mm × 1.60mm
	DCK (SC-70、5)	2.00mm × 2.1mm	2.00mm × 1.30mm
	DRL (SOT-553、5)	1.65mm × 1.6mm	1.65mm × 1.20mm

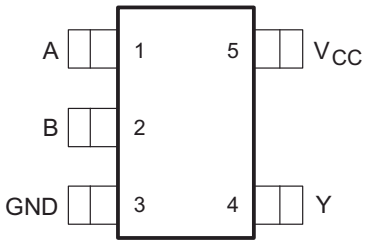
(1) 詳細については、セクション 11 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。
(3) 本体サイズ (長さ×幅) は公称値であり、ピンは含まれません。

概略回路図

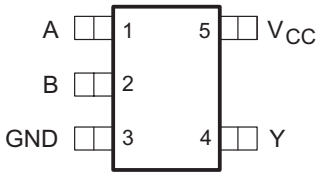
Table of Contents

4 Pin Configuration and Functions

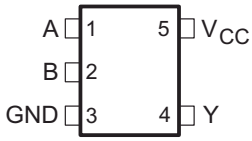
DBV PACKAGE
(TOP VIEW)



DCK PACKAGE
(TOP VIEW)



DRL PACKAGE
(TOP VIEW)



See mechanical drawings for dimensions.

表 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NO.	NAME		
1	A	I	Input A
2	B	I	Input B
3	GND	—	Ground Pin
4	Y	O	Output Y
5	V_{CC}	—	Power Pin

(1) Signal Types: I = Input, O = Output, I/O = Input or Output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	7	V
V_I	Input voltage range(2)		–0.5	7	V
V_O	Output voltage range(2)		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		–20	mA
I_{OK}	Output clamp current	V_O < 0 or V_O > V_{CC}		±20	mA
I_O	Continuous output current	V_O = 0 to V_{CC}		±25	mA
	Continuous current through V_{CC} or GND			±50	mA
T_{stg}	Storage temperature range		–65	150	°C
T_J	Junction Temperature			150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *セクション 5.3* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	5.5	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current		–8	mA
I_{OL}	Low-level output current		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20	ns/V
T_A	Operating free-air temperature	–40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

5.4 Thermal Information

THERMAL METRIC(1)		SN74AHCT1G32			UNIT
		DBV	DCK	DRL	
		5 PINS			
$R_{\theta JA}$	Junction-to-ambient thermal resistance	278	287.6	328.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	180.5	97.7	105.1	
$R_{\theta JB}$	Junction-to-board thermal resistance	184.4	65.	150.3	
ψ_{JT}	Junction-to-top characterization parameter	115.4	2.0	6.9	
ψ_{JB}	Junction-to-board characterization parameter	183.4	64.2	148.4	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			–40°C to 85°C		–40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High level output voltage	I_{OH} = –50 µA	4.5 V	4.4	4.5		4.4		4.4		V
		I_{OH} = –8 mA		3.94			3.8		3.8		
V_{OL}	Low level output voltage	I_{OL} = 50 µA	4.5 V			0.1		0.1		0.1	V
		I_{OL} = 8 mA				0.36		0.44		0.44	
I_I	Input leakage current	V_I = 5.5 V or GND	0 V to 5.5 V			±0.1		±1		±1	µA
I_{CC}	Supply current	V_I = V_{CC} or GND, I_O = 0	5.5 V			1		10		10	µA
ΔI_{CC} (1)	Supply-current change	One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			1.35		1.5		1.5	mA
C_i	Input Capacitance	V_I = V_{CC} or GND	5 V		2	10		10		10	pF

(1) This is the increase in supply current for each input at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.

5.6 Switching Characteristics

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see 図 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			–40°C to 85°C		–40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	C_L = 15 pF		5	6.9	1	8	1	9	ns
t_{PHL}					5	6.9	1	8	1	9	
t_{PLH}	A or B	Y	C_L = 50 pF		5.5	7.9	1	9	1	10	ns
t_{PHL}					5.5	7.9	1	9	1	10	

5.7 Operating Characteristics

V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	No load,	f = 1 MHz	11.5	pF

5.8 Typical Characteristics

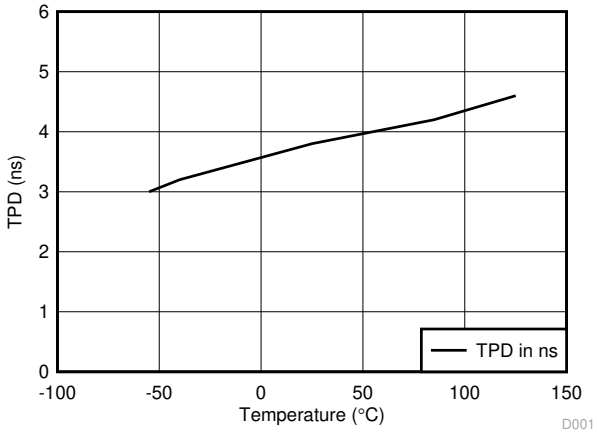
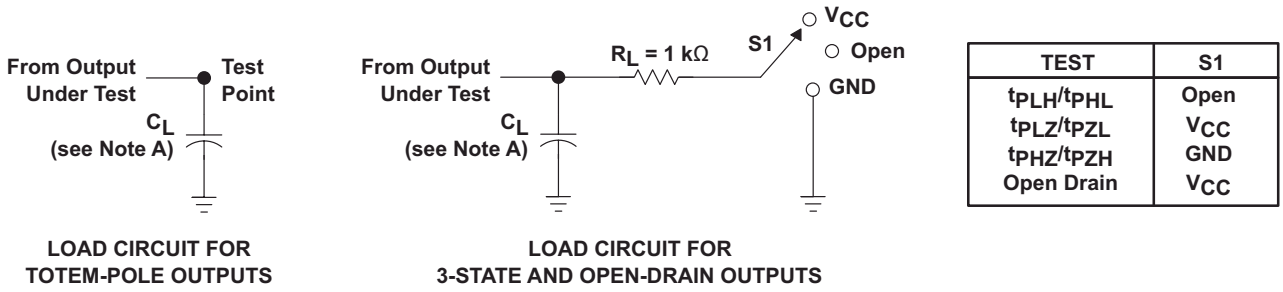


図 5-1. TPD vs Temperature

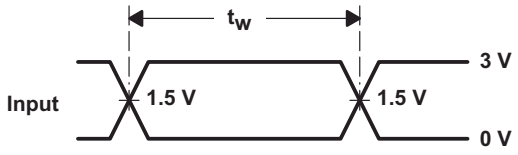
6 Parameter Measurement Information

6.1

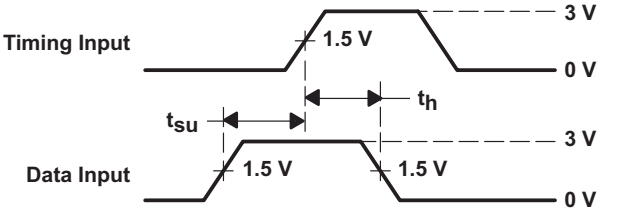


LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS

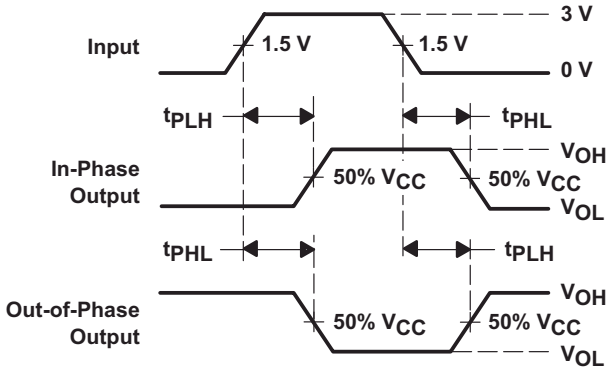
LOAD CIRCUIT FOR 3-STATE AND OPEN-DRAIN OUTPUTS



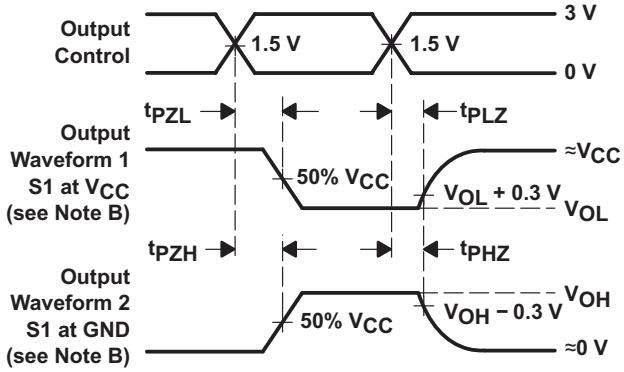
VOLTAGE WAVEFORMS PULSE DURATION



VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
D. The outputs are measured one at a time, with one input transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

図 6-1. Load Circuit and Voltage Waveforms

7 Detailed Description

7.1 Overview

The SN74AHCT1G32 device is a single 2-input positive-OR gate. The device performs the Boolean function $Y = A + B$ or $Y = \overline{\overline{A} \bullet \overline{B}}$ in positive logic.

The device has TTL inputs that allow up translation from 3.3 V to 5 V. The inputs are high impedance when V_{CC} = 0 V.

7.2 Functional Block Diagram

図 7-1. Logic Diagram (Positive Logic)

7.3 Feature Description

- Slow rise and fall time on outputs allow for low noise outputs.
- TTL inputs
  - Allows up translation from 3.3 V to 5 V

7.4 Device Functional Modes

表 7-1. Function Table

INPUTS(1)		OUTPUT(2)
A	B	Y
H	X	H
X	H	H
L	L	L

(1) H = High Voltage Level, L = Low Voltage Level, X = Don't Care
(2) H = Driving High, L = Driving Low, Z = High Impedance State

8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

SN74AHCT1G32 is a low-drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The TTL inputs can accept voltages down to 3.3 V and translate up to 5 V.

8.2 Typical Application

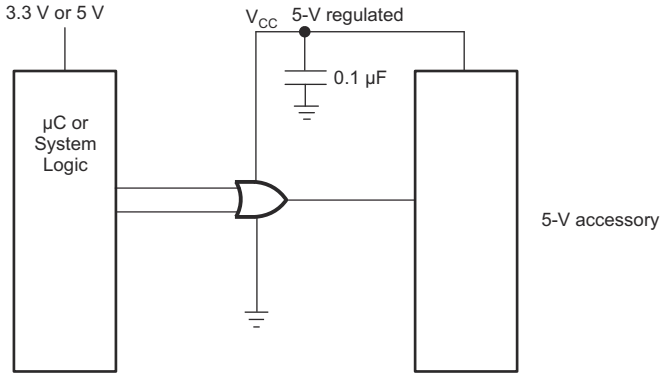


図 8-1. Typical Application Schematic

8.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

8.2.2 Detailed Design Procedure

1. Recommended Input Conditions
   - For rise time and fall time specifications, see Δt/ΔV in the *セクション 5.3* table.
   - For specified High and low levels, see V_{IH} and V_{IL} in the *セクション 5.3* table.
2. Recommend Output Conditions
   - Load currents should not exceed 25 mA per output and 50 mA total for the part.
   - Outputs should not be pulled above V_{CC}.

8.2.3 Application Curves

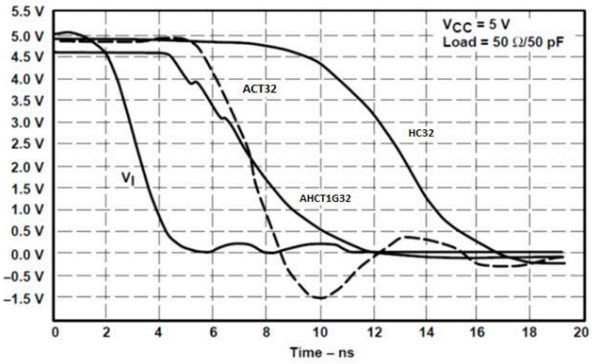


図 8-2. Switching Characteristics Comparison

8.3 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the *セクション 5.3* table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 µF is recommended. If there are multiple V_{CC} pins, 0.01 µF or 0.022 µF is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 µF and 1 µF are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

8.4 Layout

8.4.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in 図 8-3 are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC}, whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the I/Os so they also cannot float when disabled.

8.4.2 Layout Example

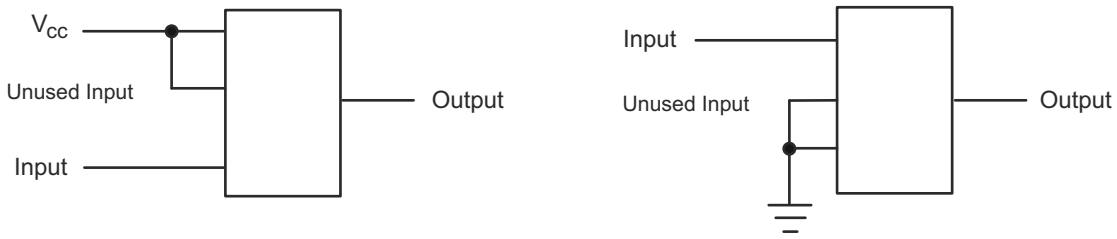


図 8-3. Layout Diagram

9 Device and Documentation Support

9.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

9.2 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の使用条件を参照してください。

9.3 Trademarks

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9.4 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.5 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

Changes from Revision O (December 2014) to Revision P (March 2024)	Page
• ドキュメント全体にわたって表、図、相互参照の採番方法を更新	1
• Updated thermal values for DBV package from RθJA = 231.3 to 278, RθJC(top) = 119.9 to 180.5, RθJB =60.6 to 184.4, ΨJT = 17.8 to 115.4, ΨJB = 60.1 to 183.4, RθJC(bot) = N/A, all values in °C/W	5

Changes from Revision N (June 2005) to Revision O (December 2014)	Page
• 「アプリケーション」、「製品情報」表、「ピンの機能」表、「ESD 定格」表、「熱に関する情報」表、「代表的特性」、「機能説明」セクション、「デバイスの機能モード」、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、および「メカニカル、パッケージ、および注文情報」セクションを追加。	1
• 「注文情報」表を削除。	1
• Changed MAX operating temperature to 125°C in *Recommended Operating Conditions* table.	4

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74AHCT1G32DBVRG4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	B32G	Samples
74AHCT1G32DCKRG4	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BG3	Samples
SN74AHCT1G32DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(B323, B32G, B32J, B32L, B32S)	Samples
SN74AHCT1G32DCK3	ACTIVE	SC70	DCK	5	3000	RoHS & Non-Green	SNBI	Level-1-260C-UNLIM	-40 to 85	BGY	Samples
SN74AHCT1G32DCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(1QU, BG3, BGG, BGJ, BGL, BGS)	Samples
SN74AHCT1G32DRLR	ACTIVE	SOT-5X3	DRL	5	4000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	BGS	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF SN74AHCT1G32 :

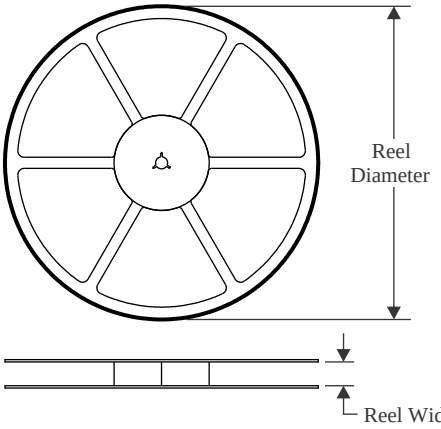
- Automotive : SN74AHCT1G32-Q1

NOTE: Qualified Version Definitions:

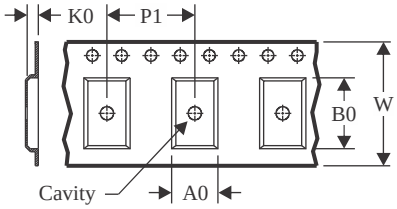
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

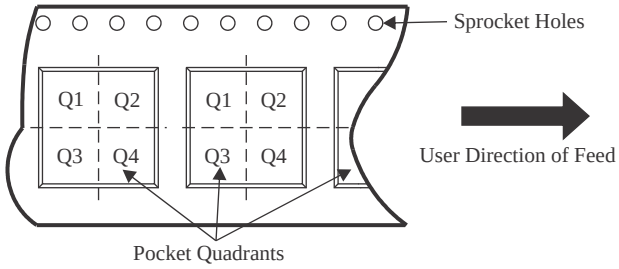


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

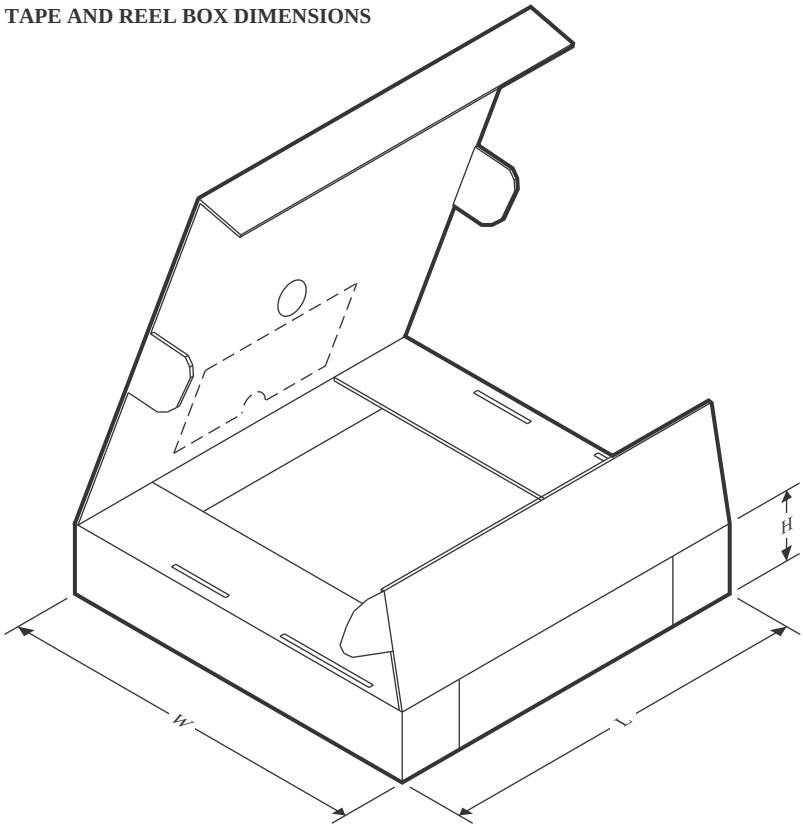
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74AHCT1G32DBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
74AHCT1G32DCKRG4	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AHCT1G32DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AHCT1G32DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
SN74AHCT1G32DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74AHCT1G32DRLR	SOT-5X3	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

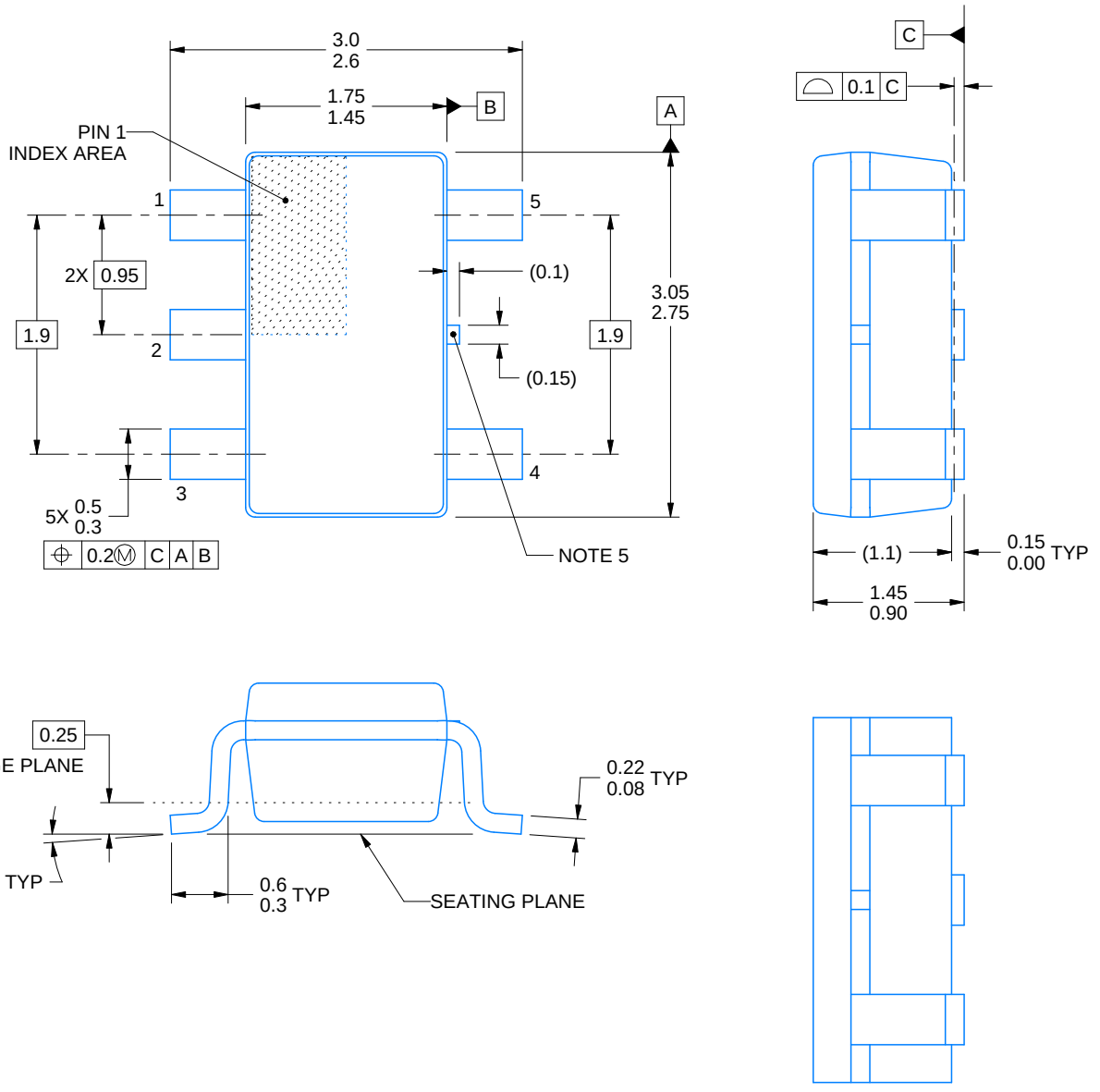
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74AHCT1G32DBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
74AHCT1G32DCKRG4	SC70	DCK	5	3000	180.0	180.0	18.0
SN74AHCT1G32DBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
SN74AHCT1G32DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74AHCT1G32DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74AHCT1G32DRLR	SOT-5X3	DRL	5	4000	202.0	201.0	28.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

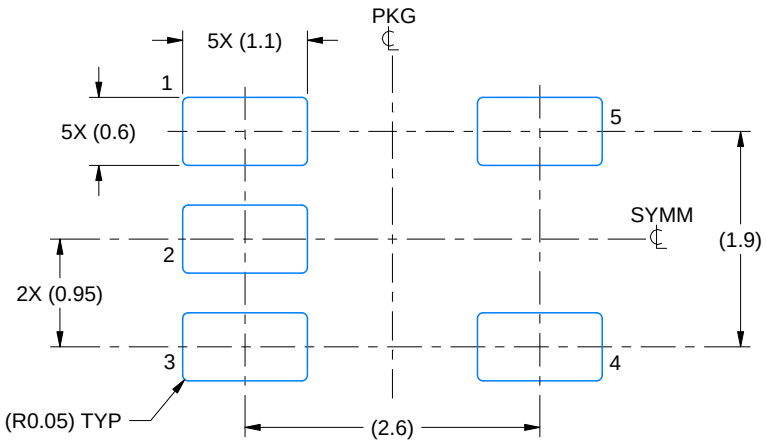


ALTERNATIVE PACKAGE SINGULATION VIEW

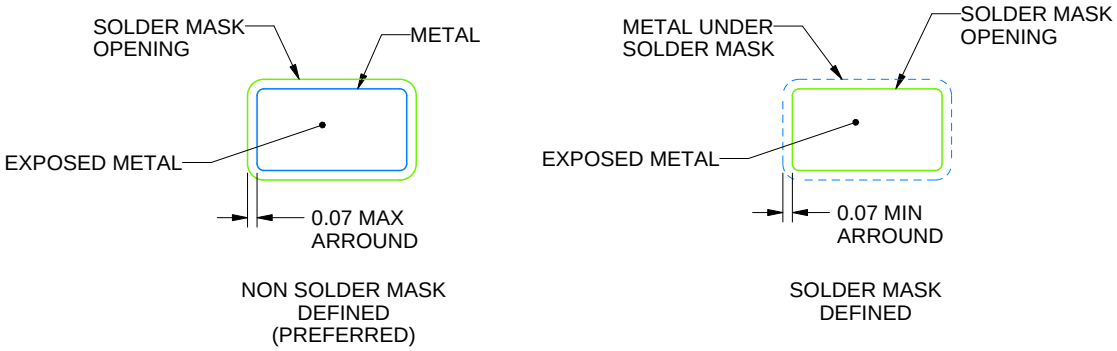
4214839/J 02/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

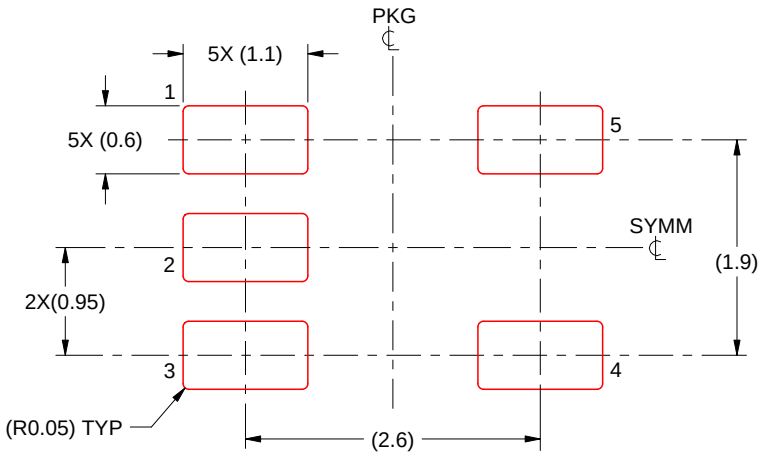


SOLDER MASK DETAILS

4214839/J 02/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/J 02/2024

NOTES: (continued)

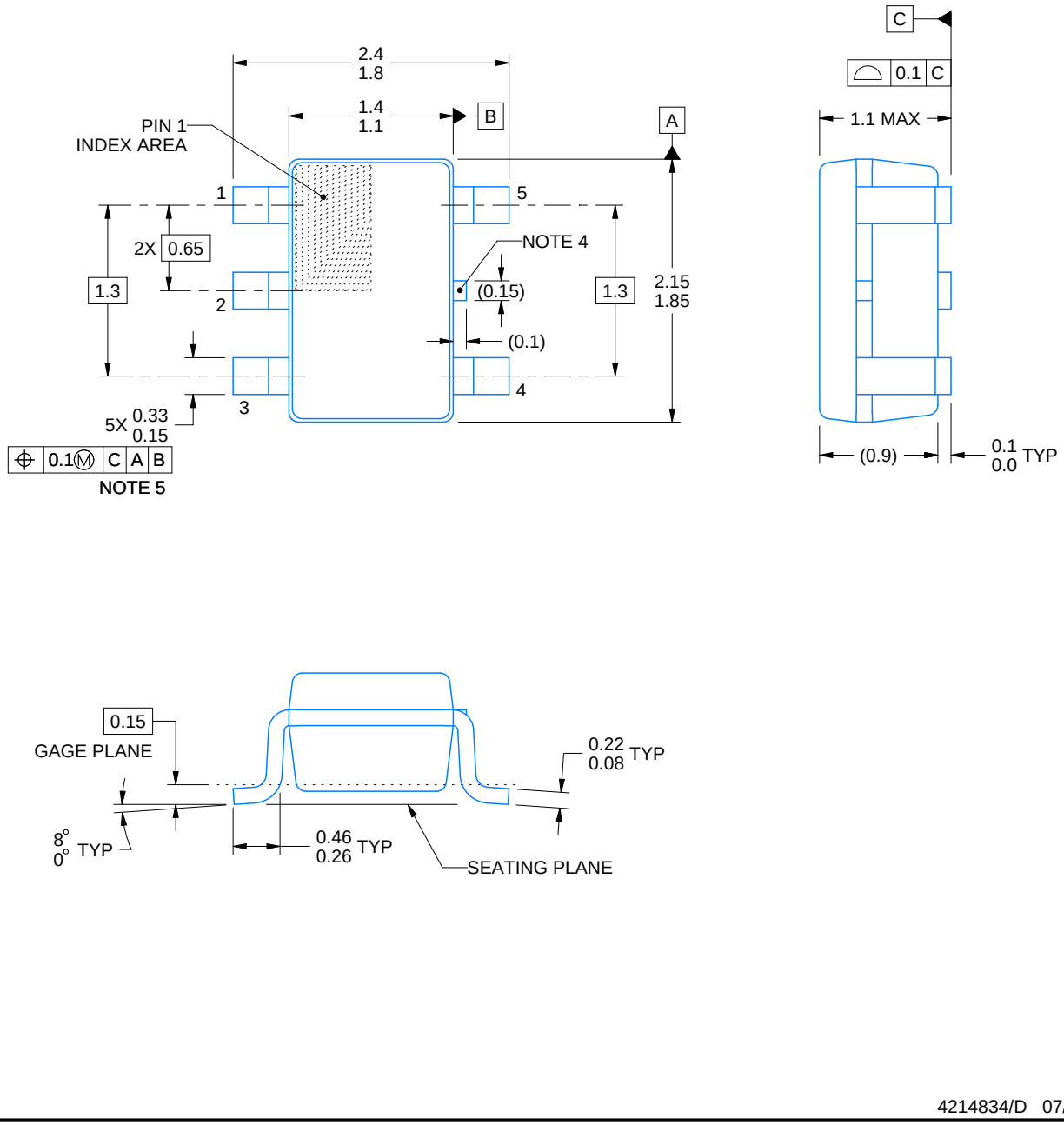
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

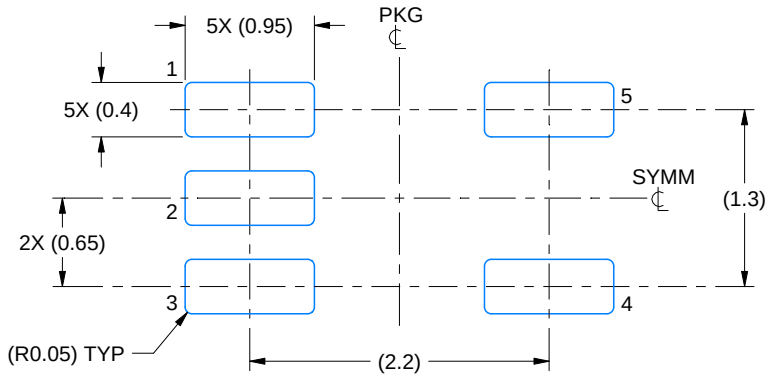
SMALL OUTLINE TRANSISTOR



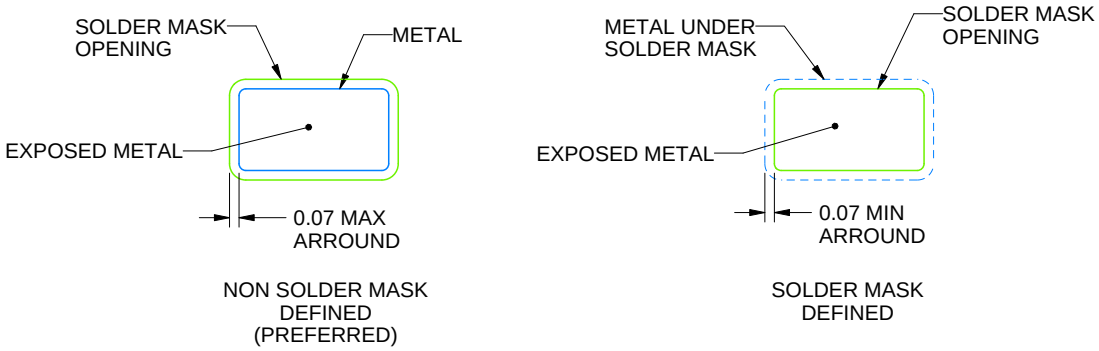
4214834/D 07/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

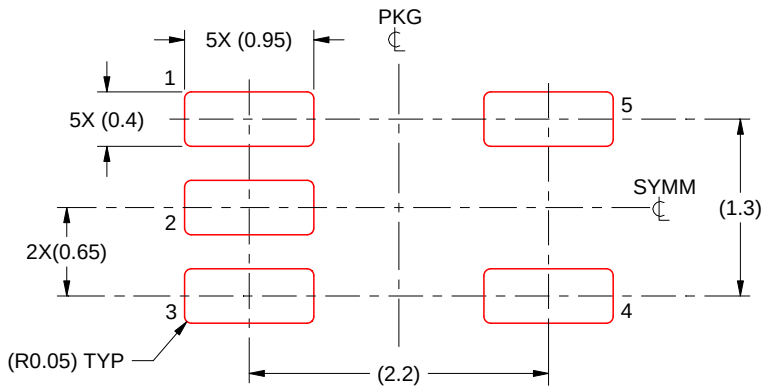


SOLDER MASK DETAILS

4214834/D 07/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/D 07/2023

NOTES: (continued)

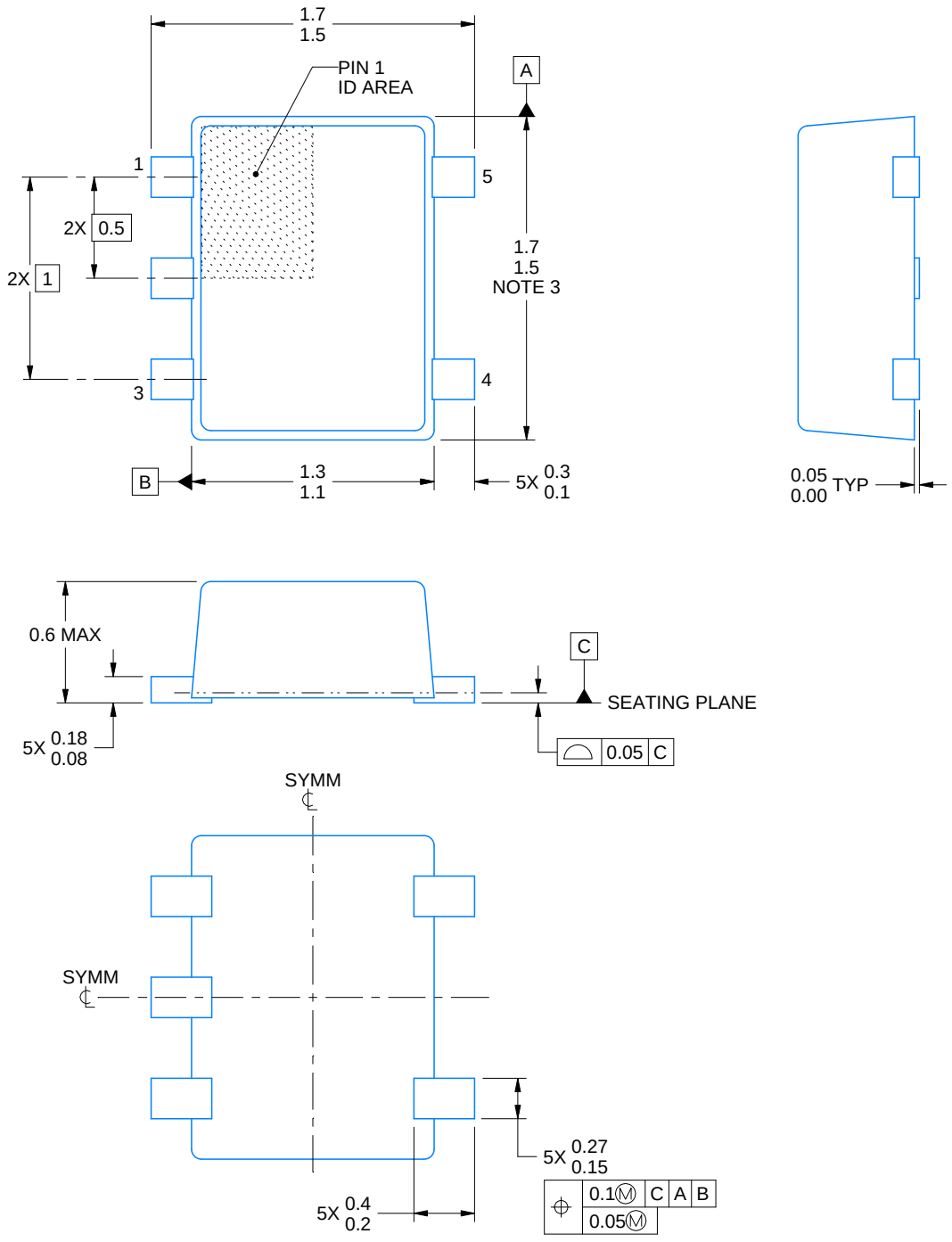
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DRL0005A

SOT - 0.6 mm max height

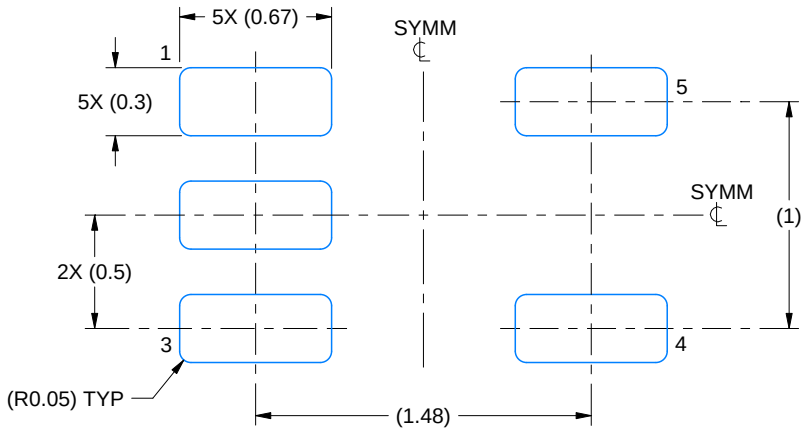
PLASTIC SMALL OUTLINE



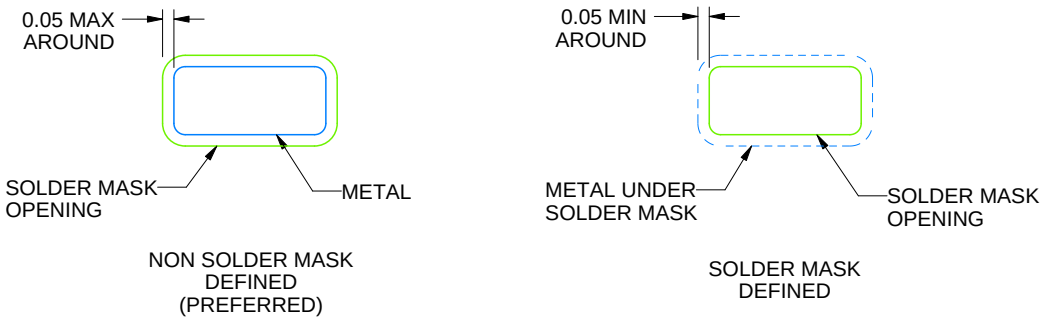
4220753/B 12/2020

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD-1



LAND PATTERN EXAMPLE
SCALE:30X

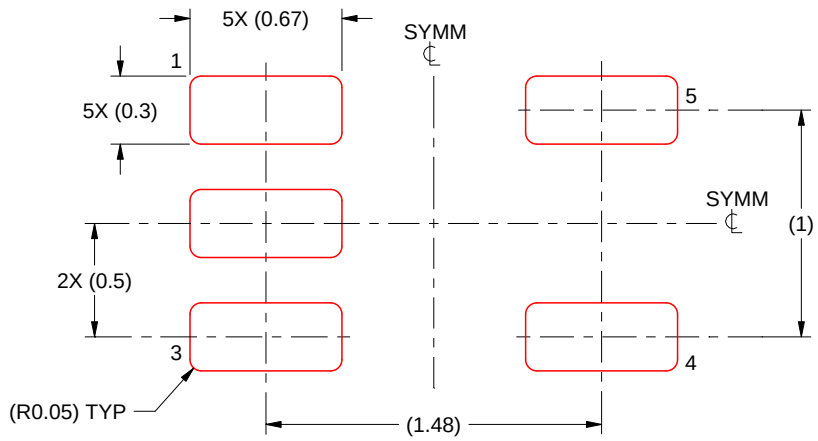


SOLDERMASK DETAILS

4220753/B 12/2020

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4220753/B 12/2020

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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