SN75LBC172A、SN75LBC172A クワッド RS-485 差動ライン ドライバ

1 特長

- TIA/EIA-485、TIA/EIA-422、ISO 8482 アプリケーション用に設計
- 信号レート † 最大 30 Mbps
- 伝搬遅延時間:<11ns
- 低スタンバイ消費電力:1.5mA 未満
- 出力 ESD 保護 :12kV
- ドライバの正および負の電流制限
- 活線挿抜アプリケーションでパワーアップ/パワーダウン時のグリッチなし
- サーマル シャットダウン保護機能
- SN75172、AM26LS31、DS96172、LTC486、MAX3045 と互換の業界標準ピン配置

2 アプリケーション

- モーター ドライブ
- ファクトリ オートメーション / 制御

3 概要

SN65LBC172A および SN75LBC172A は、3 ステート出力のクワッド差動ライン ドライバで、TIA/EIA-485 (RS-485)、TIA/EIA-422 (RS-422)、ISO 8482 アプリケーション用に設計されています。

このデバイスは、最大 30Mbps の信号レートでの平衡マルチポイント バス伝送用に最適化されています。伝送媒体にはプリント基板のトレース、バックプレーン、ケーブルを使用できます。データ転送の最高速度および最大距離は、メディアの減衰特性と周囲からのノイズに依存します。

各ドライバは電流制限およびサーマル シャットダウン回路を備えているため、ノイズの多い環境の高速マルチポイントデータ転送アプリケーションに適しています。これらのデバイスは LinBiCMOS を使用して設計されており、低消費電力と堅牢性を実現しています。

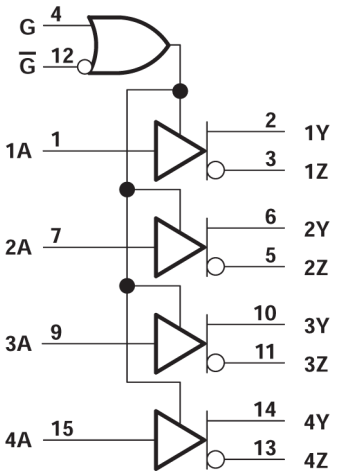
G および $\overline{G}$ 入力により、正論理または負論理を使用したドライバ イネーブル制御が可能です。ディセーブルまたは電源オフ時には、ドライバの出力はバスに対して高インピーダンスになるため、システムの負荷を低減できます。

SN75LBC172A は 0℃～70℃の温度範囲で動作が規定されています。SN65LBC172A は -40℃～85℃の温度範囲で動作が規定されています。

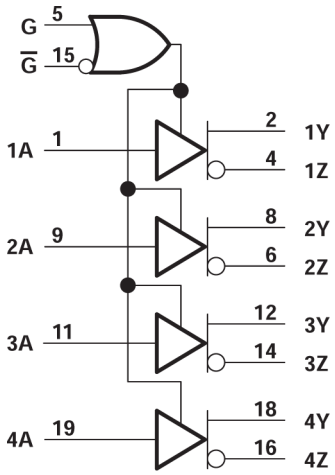
パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
SN65LBC172A SN75LBC172A	SOIC (DW、16)	10.3mm × 10.3mm
	SOIC (DW、20)	12.8mm × 10.3mm
	PDIP (N、16)	19.3mm × 9.4mm

(1) 詳細については、セクション 11 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



論理図 (正論理)



論理図 (正論理)

† ラインの信号レートとは、1 秒あたりの電圧遷移回数を bps (ビット/秒) 単位で表したものです。

このリソースの元の言語は英語です。翻訳は概要を便宜的に提供するもので、自動化ツール (機械翻訳) を使用していることがあり、TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、ti.com で必ず最新の英語版をご参照くださいますようお願いいたします。

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4 Pin Configuration and Functions

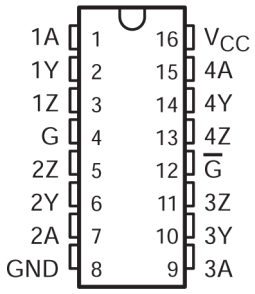

図 4-1. N Package (Top View)

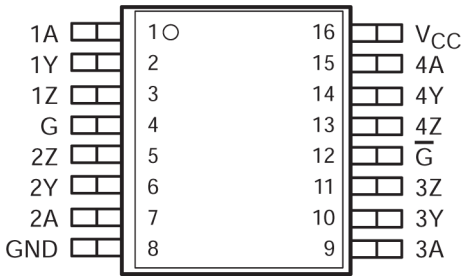

図 4-2. 16-DW Package (Top View)

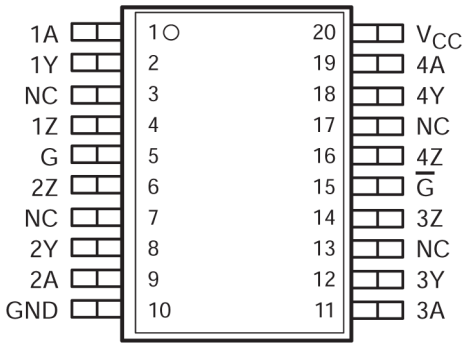

図 4-3. 20-DW Package (Top View)

5 Specifications

5.1 Absolute Maximum Ratings

See Note (1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		−0.3	6	V
V_O	Output voltage range	at any bus (steady state)	−10	15	V
V_O	Output voltage range	at any bus (transient pulse through 100Ω, see 図 6-8)	−30	30	V
V_I	Input voltage range	at any A, G, or $\overline{G}$ terminal	−0.5	V_{CC} + 0.5	V
T_{stg}	Storage temperature range		−65	150	°C
P_D	Continuous power dissipation		See Dissipation Rating Table		
T_{LEAD}	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds			260	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	Y, Z, and GND	±12000	V
		All pins	±5000	
	Charged device model (CDM), per AEC Q100-011(2)	All pins	±1000	

(1) Tested in accordance with JEDEC standard 22, Test Method A114−A.
(2) Tested in accordance with JEDEC standard 22, Test Method C101.

5.3 Dissipation Rating Table

PACKAGE	JEDEC BOARD MODEL	T_A ≤ 25°C POWER RATING	DERATING FACTOR(1) ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
16-PIN DW	Low K	1200mW	9.6mW/°C	769mW	625mW
	High K	2240mW	17.9mW/°C	1434mW	1165mW
20-PIN DW	Low K	1483mW	11.86mW/°C	949mW	771mW
	High K	2753mW	22mW/°C	1762mW	1432mW
16-PIN N	Low K	1150mW	9.2mW/°C	736mW	598mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted with no air flow.

5.4 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Voltage at any bus terminal	Y, Z	−7		12	V
High-level input voltage, V_{IH}	A, G, $\overline{G}$	2		V_{CC}	V
Low-level input voltage, V_{IL}		0		0.8	
Output current		−60		60	mA
Operating free-air temperature, T_A	SN75LBC172A	0		70	°C
	SN65LBC172A	−40		85	

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5.5 Thermal Information

THERMAL METRIC[1]		N (PDIP) 16 PINS	DW (SOIC) 16 PINS	DW (SOIC) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	60.6	71.1	66.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	48.1	37.4	34.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	40.6	36.8	39.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	27.5	13.3	8.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	40.3	36.4	39	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.6 Electrical Characteristics

over recommended operating conditions

PARAMETER		TEST CONDITIONS		MIN	TYP[1]	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = −18mA		−1.5	−0.77		V
V_O	Open-circuit output voltage	Y or Z, No load		0		V_{CC}	V
$\lvert V_{OD(SS)} \rvert$	Steady-state differential output voltage magnitude[2]	No load (open circuit)		3		V_{CC}	V
		R_L = 54Ω, see 図 6-1		1	1.6	2.5	
		With common-mode loading, see 図 6-2		1	1.6	2.5	
$\Delta V_{OD(SS)}$	Change in steady-state differential output voltage between logic states	See 図 6-1		−0.1		0.1	V
$V_{OC(SS)}$	Steady-state common-mode output voltage	See 図 6-3		2	2.4	2.8	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states	See 図 6-3		−0.02		0.02	V
I_I	Input current	A, G, $\overline{G}$		−50		50	μA
I_{OS}	Short-circuit output current	V_{TEST} = −7V to 12V, See 図 6-7	V_I = 0V	−200		200	mA
			V_I = V_{CC}				
I_{OZ}	High-impedance-state output current		G at 0V, $\overline{G}$ at V_{CC}	−50		50	μA
$I_{O(OFF)}$	Output current with power off		V_{CC} = 0V	−10		10	
I_{CC}	Supply current	V_I = 0V or V_{CC}, No load	All drivers enabled			23	mA
			All drivers disabled			1.5	

(1) All typical values are at V_{CC} = 5V and 25°C.
(2) The minimum V_{OD} may not fully comply with TIA/EIA-485-A at operating temperatures below 0°C. System designers should take the possibly of lower output signal into account in determining the maximum signal transmission distance.

5.7 Switching Characteristics

over recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high level output	R_L = 54Ω, C_L = 50pF, see 図 6-4	5.5	8	11	ns
t_{PHL}	Propagation delay time, high-to-low level output		5.5	8	11	ns
t_r	Differential output voltage rise time		2	7.5	11	ns
t_f	Differential output voltage fall time		2	7.5	11	ns
$t_{sk(p)}$	Pulse skew $\|t_{PLH} – t_{PHL}\|$			0.6	2	ns
$t_{sk(o)}$	Output skew(1)				2	ns
$t_{sk(pp)}$	Part-to-part skew(2)				3	ns
t_{PZH}	Propagation delay time, high-impedance-to-high-level output	See 図 6-5			25	ns
t_{PHZ}	Propagation delay time, high-level-output-to-high impedance				25	ns
t_{PZL}	Propagation delay time, high-impedance-to-low-level output	See 図 6-6			30	ns
t_{PLZ}	Propagation delay time, low-level-output-to-high impedance				20	ns

(1) Output skew ($t_{sk(o)}$) is the magnitude of the time delay difference between the outputs of a single device with all of the inputs connected together.
(2) Part-to-part skew ($t_{sk(pp)}$) is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same input signals, the same supply voltages, at the same temperature, and have identical packages and test circuits.

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5.8 Typical Characteristics

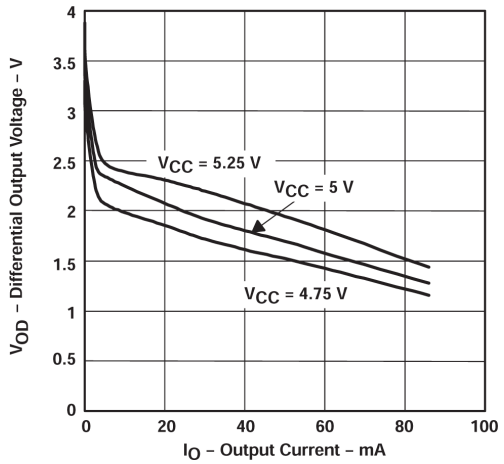

図 5-1. Differential Output Voltage vs Output Current

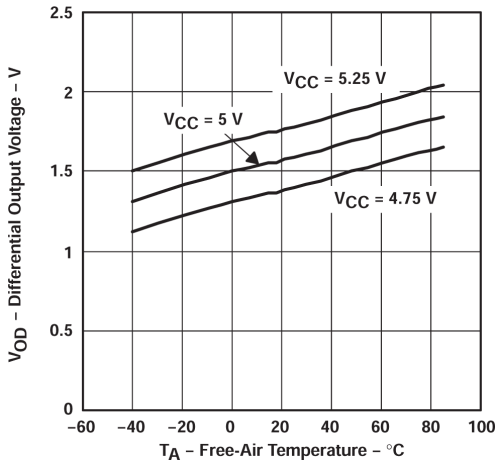

図 5-2. Differential Output Voltage vs Free-air Temperature

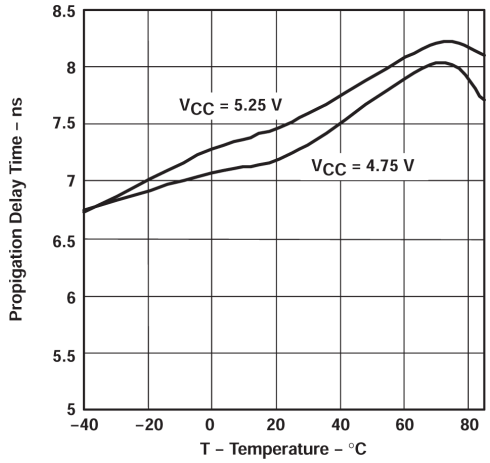

図 5-3. Propagation Delay Time vs Temperature

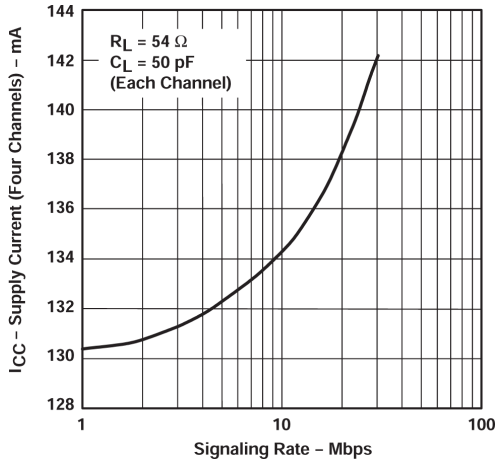

図 5-4. Supply Current (Four Channels) vs Signaling Rate

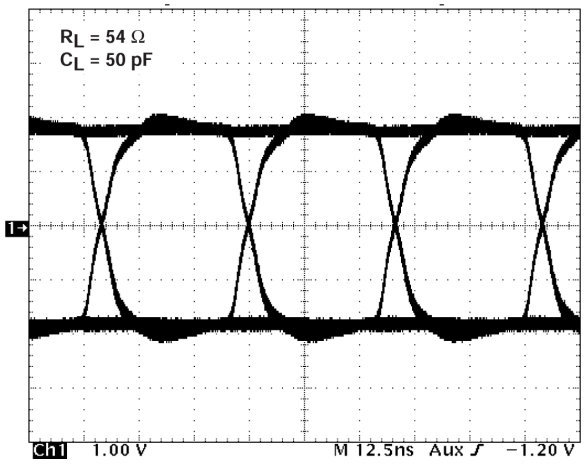

図 5-5. Eye Pattern, Pseudorandom Data at 30Mbps

6 Parameter Measurement Information

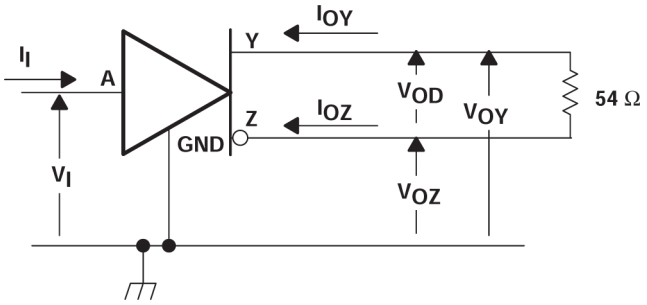

図 6-1. Test Circuit, V_{OD} Without Common-Mode Loading

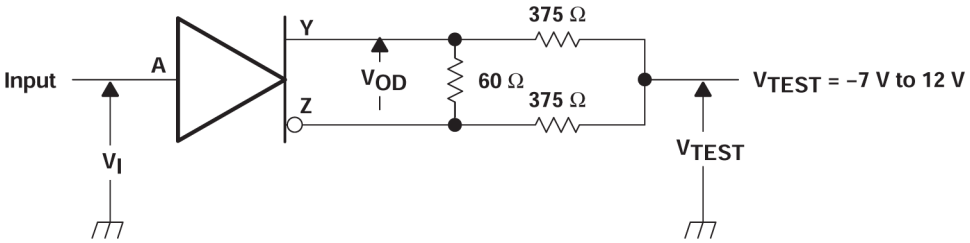

図 6-2. Test Circuit, V_{OD} With Common-Mode Loading

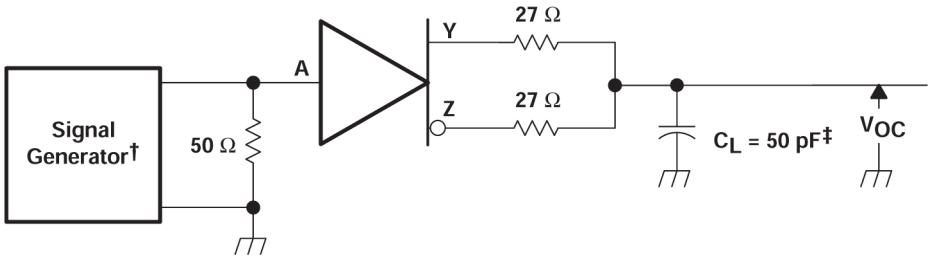

図 6-3. V_{OC} Test Circuit

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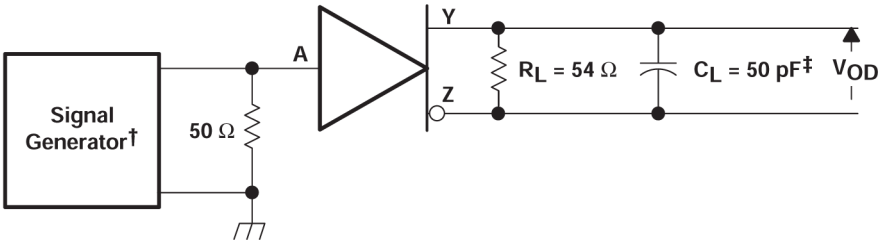


† PRR = 1 MHz, 50% duty cycle, t_r < 6 ns, t_f < 6 ns, Z_O = 50 Ω

‡ Includes probe and jig capacitance

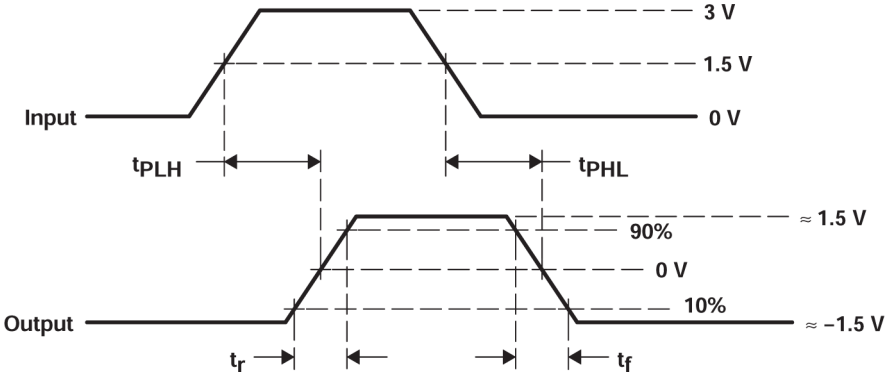
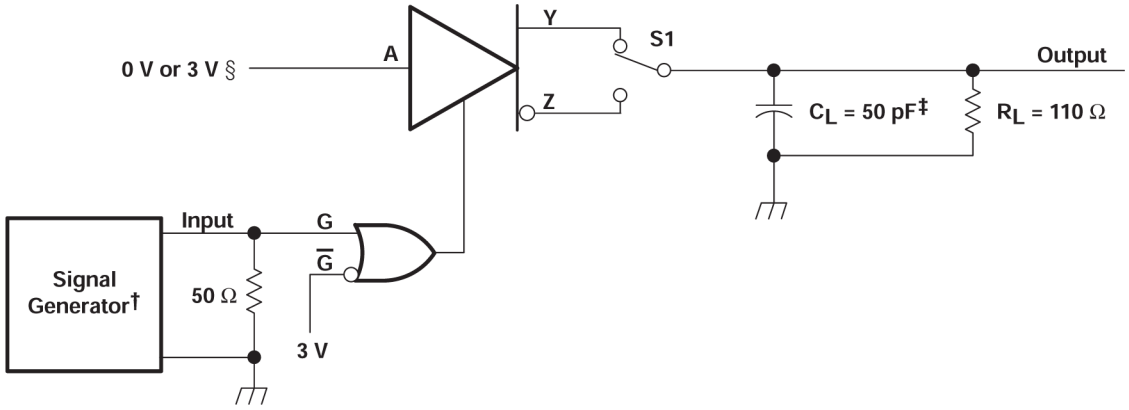


図 6-4. Output Switching Test Circuit and Waveforms



† PRR = 1 MHz, 50% duty cycle, t_r < 6 ns, t_f < 6 ns, Z_O = 50 Ω
‡ Includes probe and jig capacitance
§ 3-V if testing Y output, 0 V if testing Z output

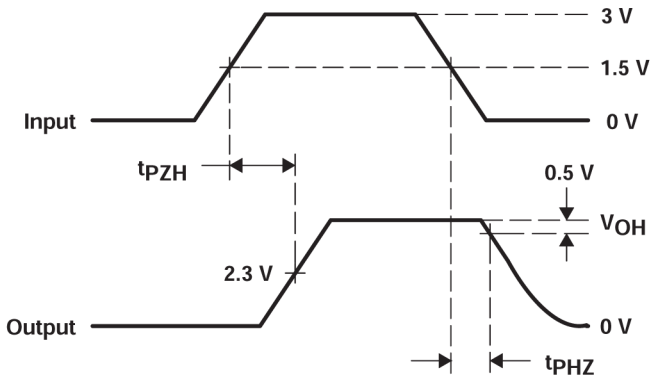


図 6-5. Enable Timing Test Circuit and Waveforms, t_{PZH} and t_{PHZ}

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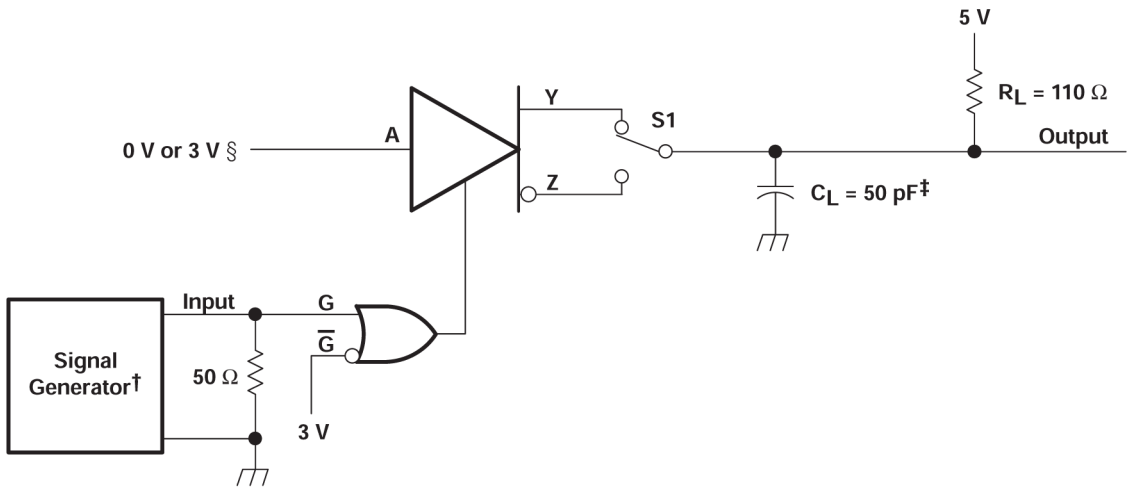

† PRR = 1 MHz, 50% duty cycle, t_r < 6 ns, t_f < 6 ns, Z_O = 50 Ω
‡ Includes probe and jig capacitance
§ 3-V if testing Y output, 0 V if testing Z output

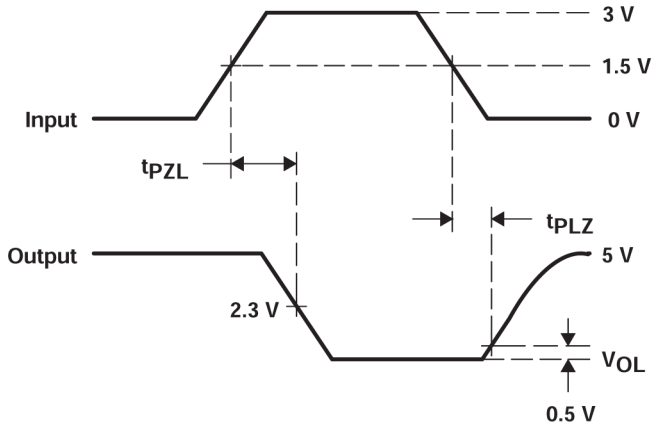

図 6-6. Enable Timing Test Circuit and Waveforms, t_{PZL} and t_{PLZ}

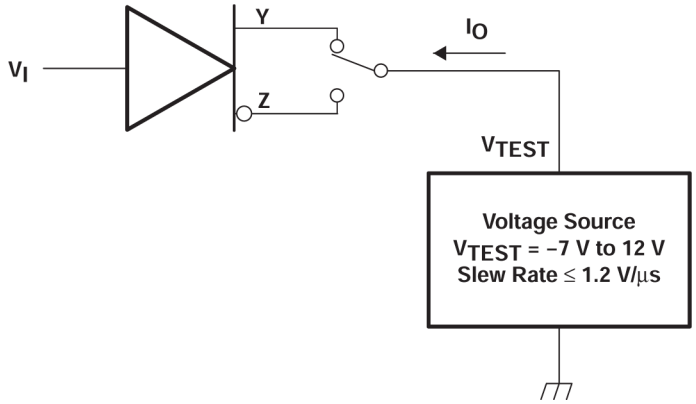

図 6-7. Test Circuit, Short-Circuit Output Current

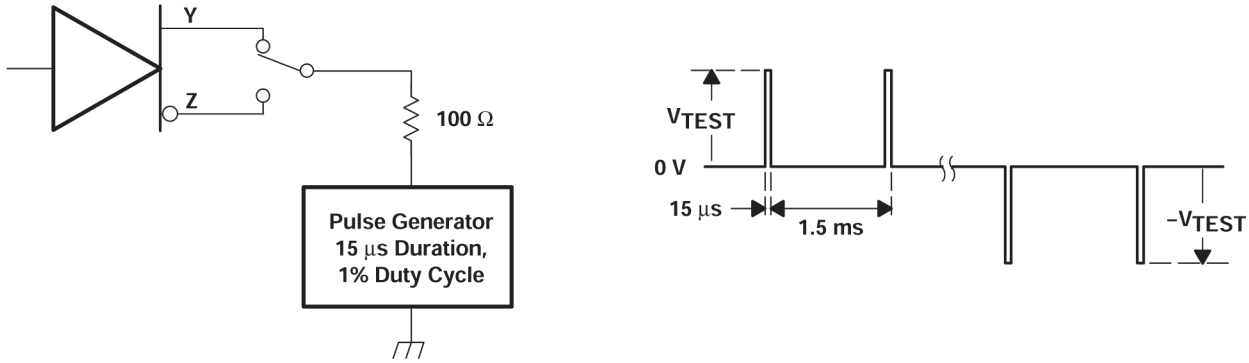

図 6-8. Test Circuit and Waveform, Transient Over-Voltage

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7 Detailed Description

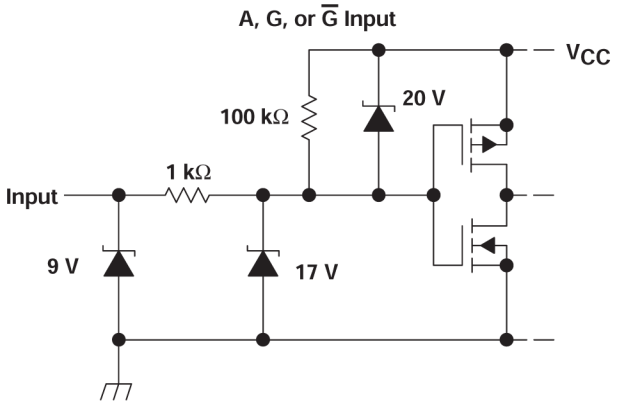
7.1 Device Functional Modes

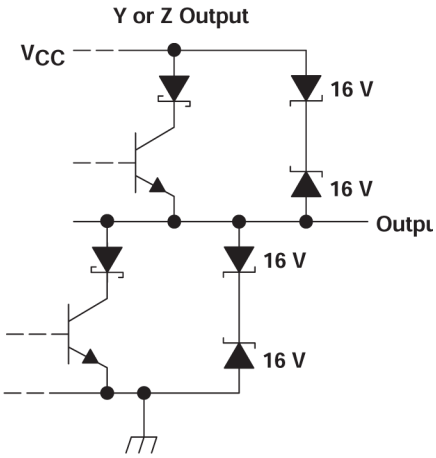
7.1.1 Function Table

表 7-1. (Each Driver)

INPUT	ENABLES		OUTPUTS	
A	G	$\overline{G}$	Y	Z
L	H	X	L	H
L	X	L	L	H
H	H	X	H	L
H	X	L	H	L
OPEN	H	X	H	L
OPEN	X	L	H	L
H	OPEN	X	H	L
L	OPEN	X	L	H
X	L	H	Z	Z
X	L	OPEN	Z	Z

7.1.2 Equivalent Input and Output Schematic Diagrams





8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

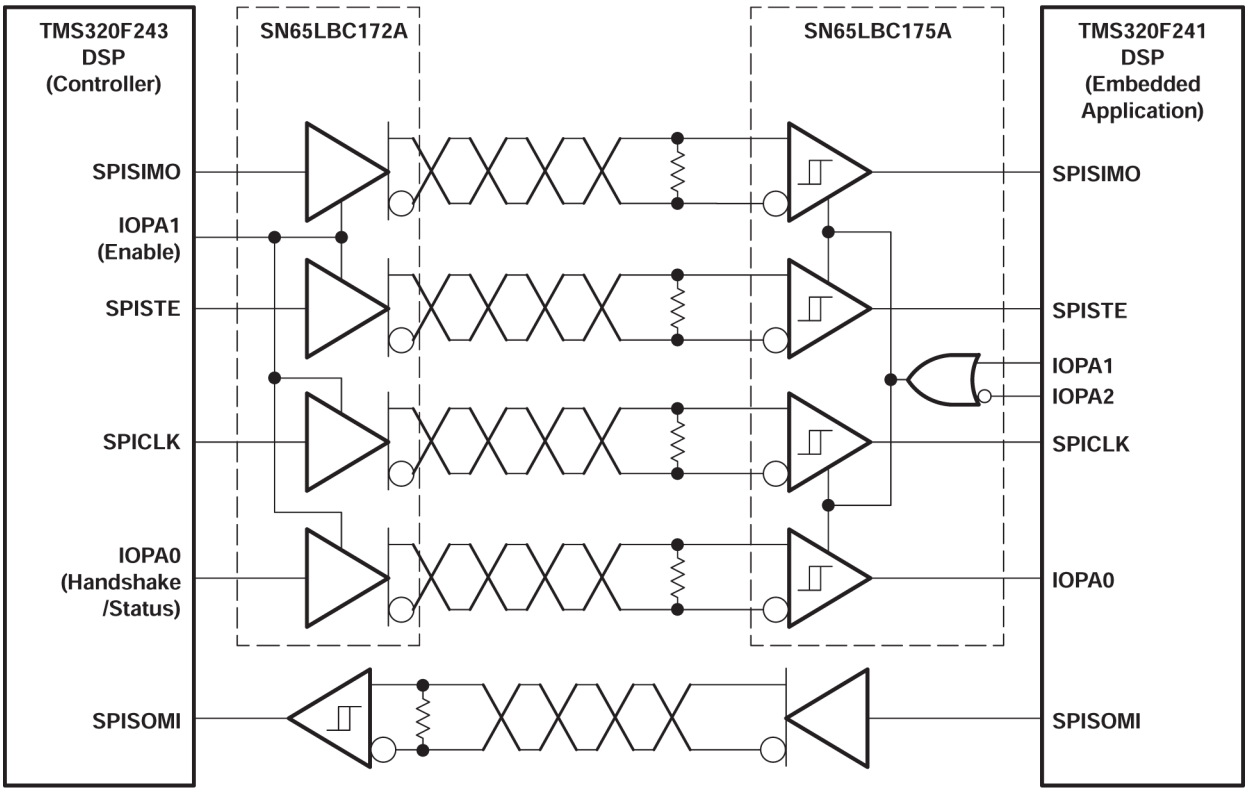


図 8-1. Typical Application Circuit, DSP-to-DSP Link via Serial Peripheral Interface

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9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Documentation Support

9.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

9.3 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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9.4 Trademarks

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9.5 静電気放電に関する注意事項

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9.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision C (August 2008) to Revision D (April 2024)	Page
• ドキュメント全体にわたって表、図、相互参照の採番方法を変更	1
• Added the *Thermal Information* table	5

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65LBC172A16DW	LIFEBUY	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65LBC172A	
SN65LBC172A16DWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65LBC172A	Samples
SN65LBC172ADW	LIFEBUY	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65LBC172A	
SN65LBC172ADWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65LBC172A	Samples
SN65LBC172AN	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	65LBC172A	Samples
SN65LBC172ANE4	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	65LBC172A	Samples
SN75LBC172A16DW	LIFEBUY	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75LBC172A	
SN75LBC172A16DWR	LIFEBUY	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75LBC172A	
SN75LBC172ADW	LIFEBUY	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75LBC172A	
SN75LBC172ADWR	LIFEBUY	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75LBC172A	
SN75LBC172AN	LIFEBUY	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	75LBC172A	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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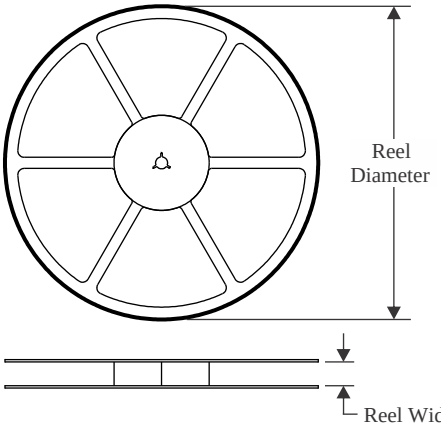
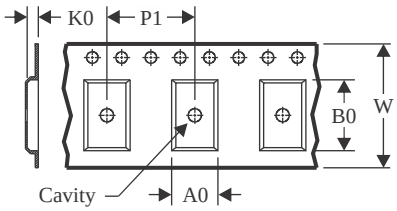
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

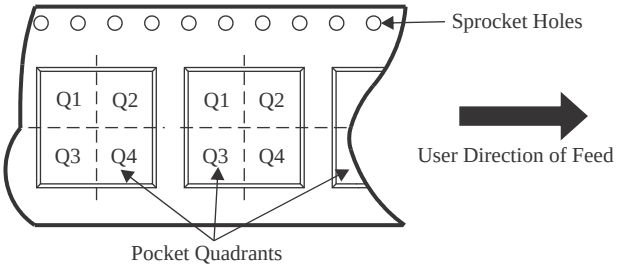


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

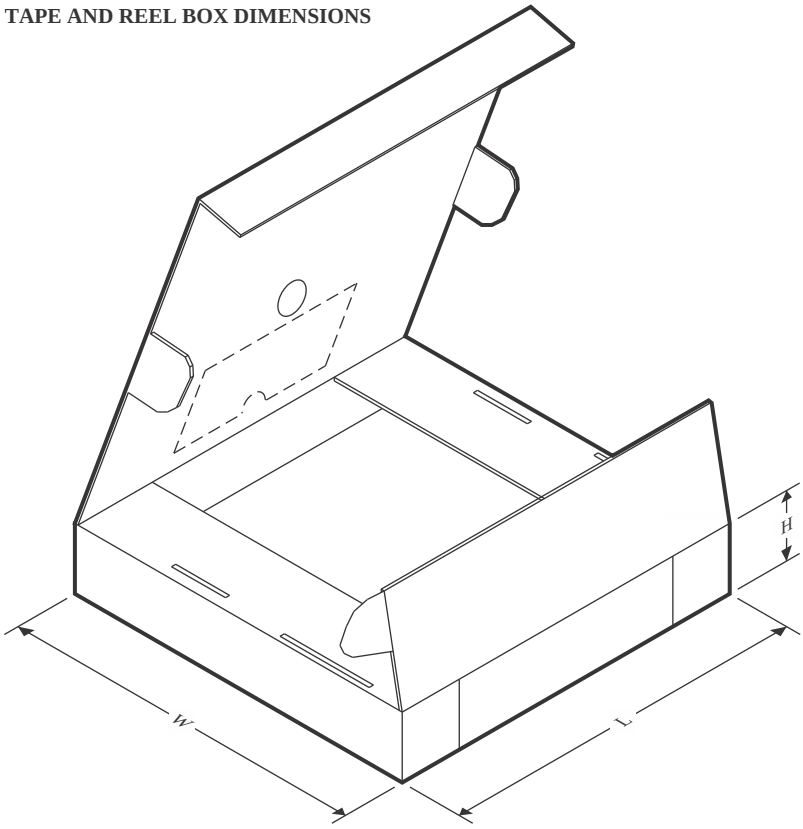
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LBC172A16DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
SN65LBC172ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN75LBC172A16DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
SN75LBC172ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

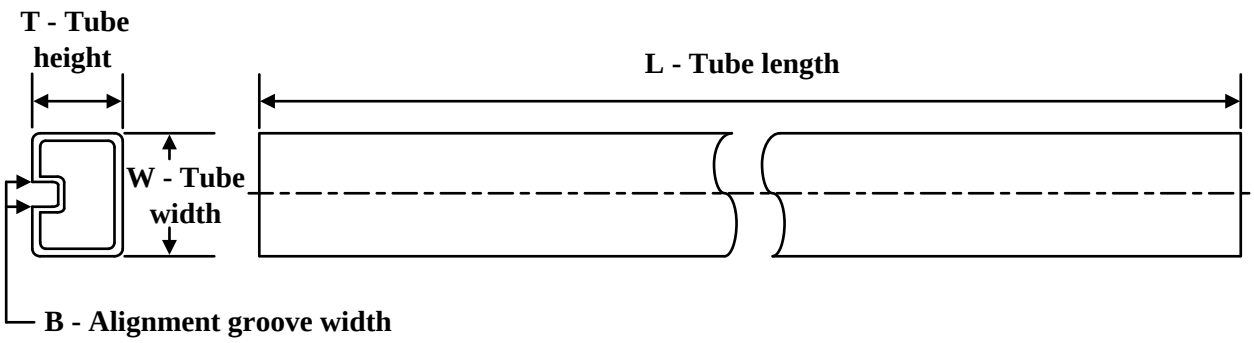
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LBC172A16DWR	SOIC	DW	16	2000	350.0	350.0	43.0
SN65LBC172ADWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN75LBC172A16DWR	SOIC	DW	16	2000	350.0	350.0	43.0
SN75LBC172ADWR	SOIC	DW	20	2000	367.0	367.0	45.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65LBC172A16DW	DW	SOIC	16	40	506.98	12.7	4826	6.6
SN65LBC172ADW	DW	SOIC	20	25	507	12.83	5080	6.6
SN65LBC172ADW	DW	SOIC	20	25	506.98	12.7	4826	6.6
SN65LBC172AN	N	PDIP	16	25	506	13.97	11230	4.32
SN65LBC172ANE4	N	PDIP	16	25	506	13.97	11230	4.32
SN75LBC172A16DW	DW	SOIC	16	40	506.98	12.7	4826	6.6
SN75LBC172ADW	DW	SOIC	20	25	506.98	12.7	4826	6.6
SN75LBC172ADW	DW	SOIC	20	25	507	12.83	5080	6.6
SN75LBC172AN	N	PDIP	16	25	506	13.97	11230	4.32

GENERIC PACKAGE VIEW

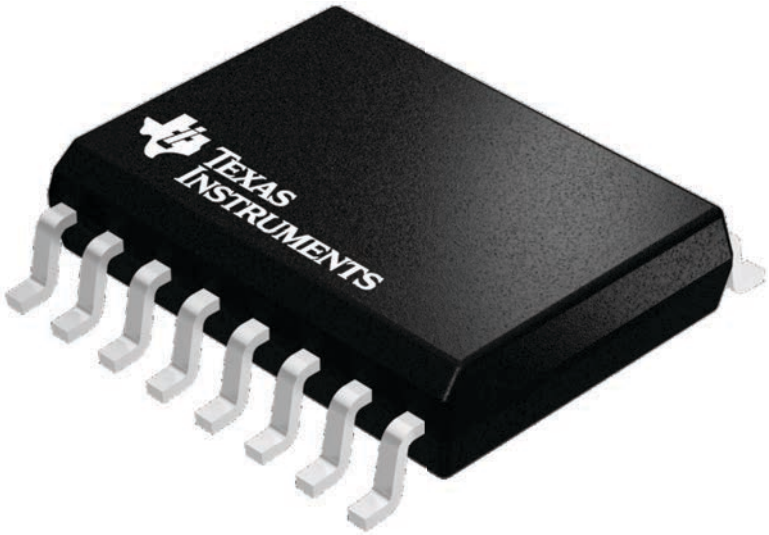
DW 16

SOIC - 2.65 mm max height

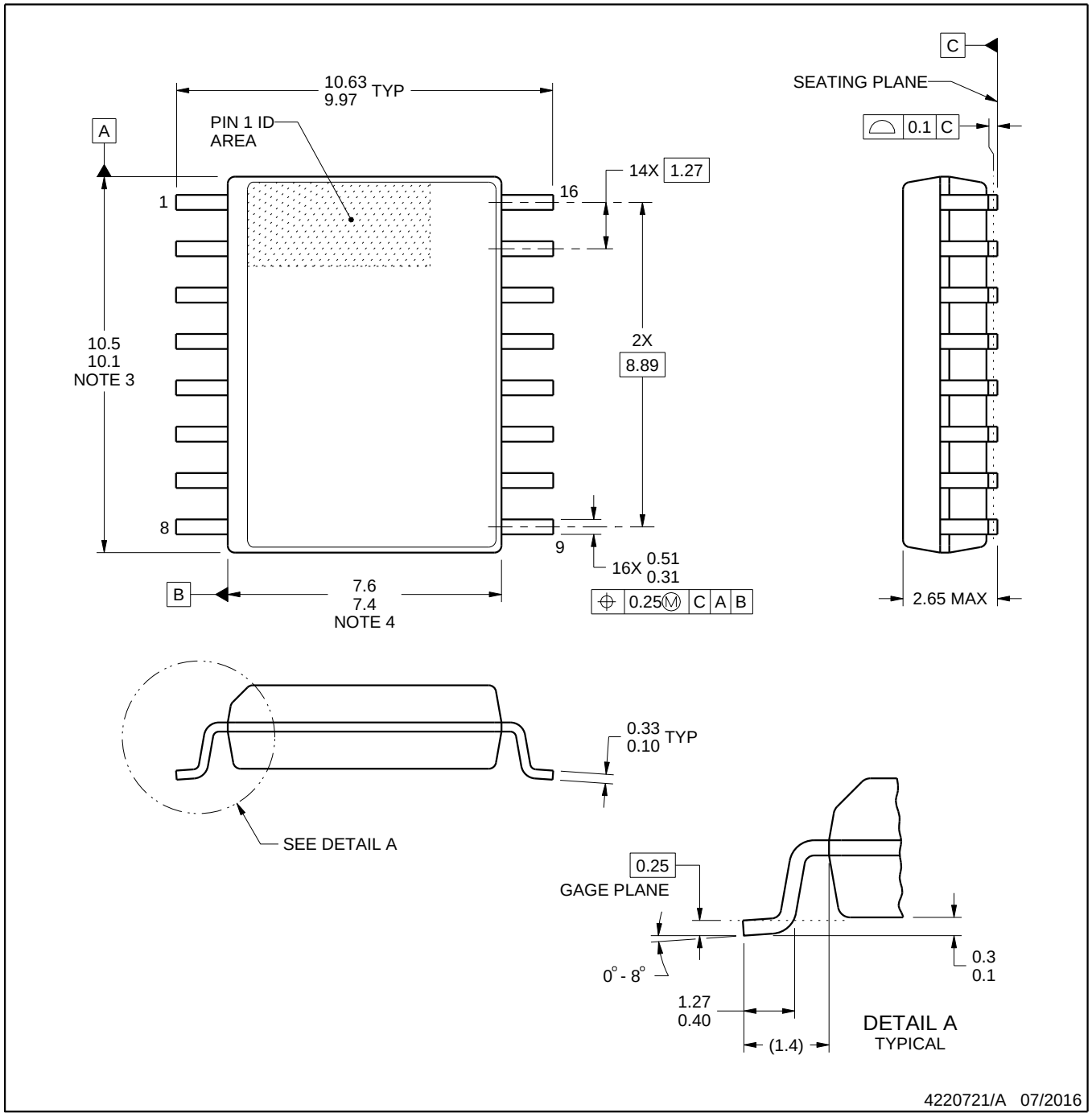
7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

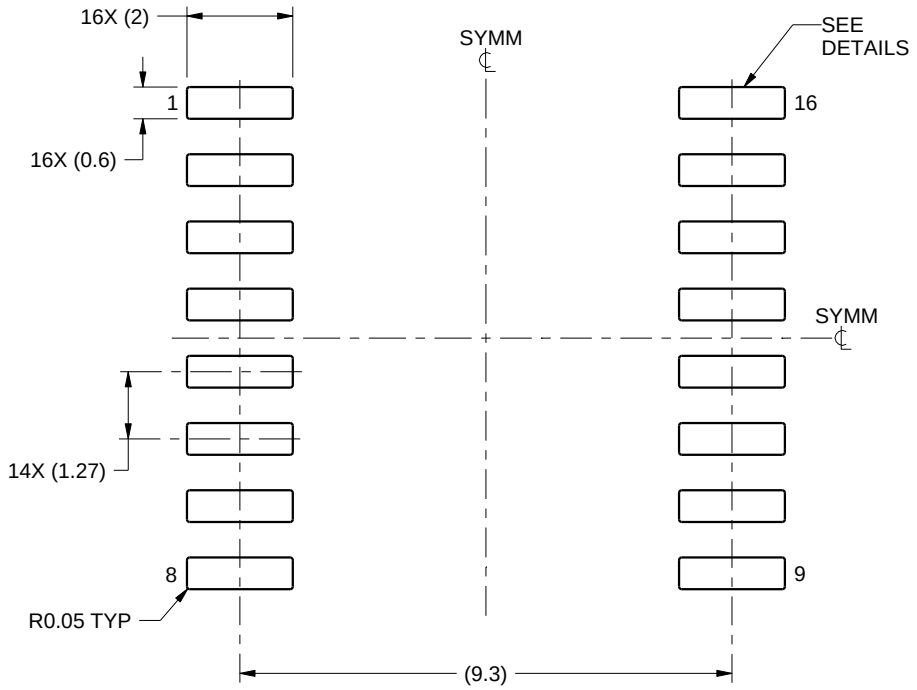


4224780/A

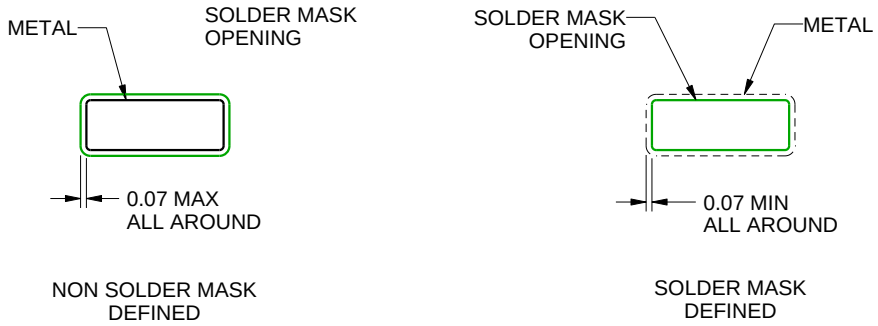


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:7X

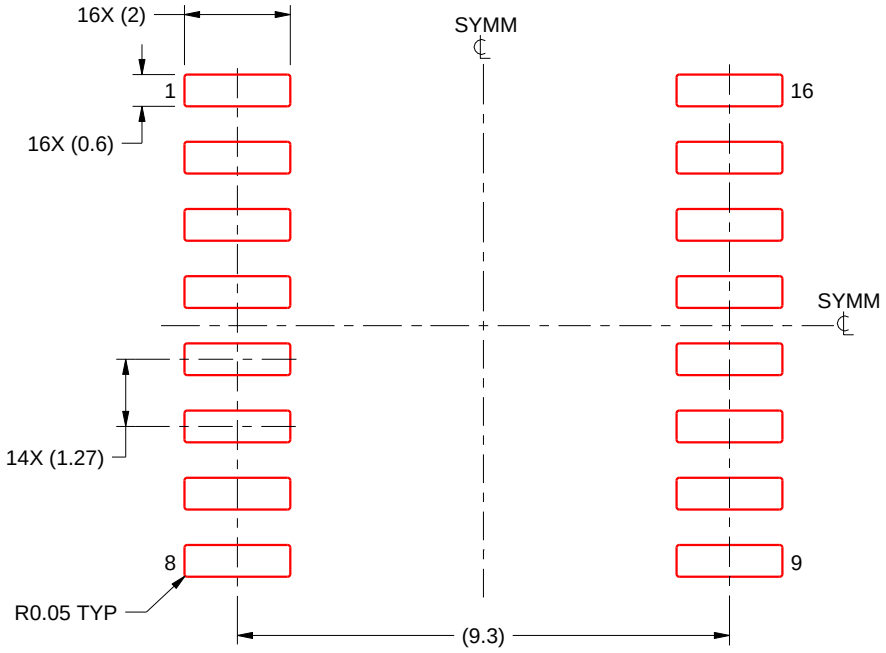


SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

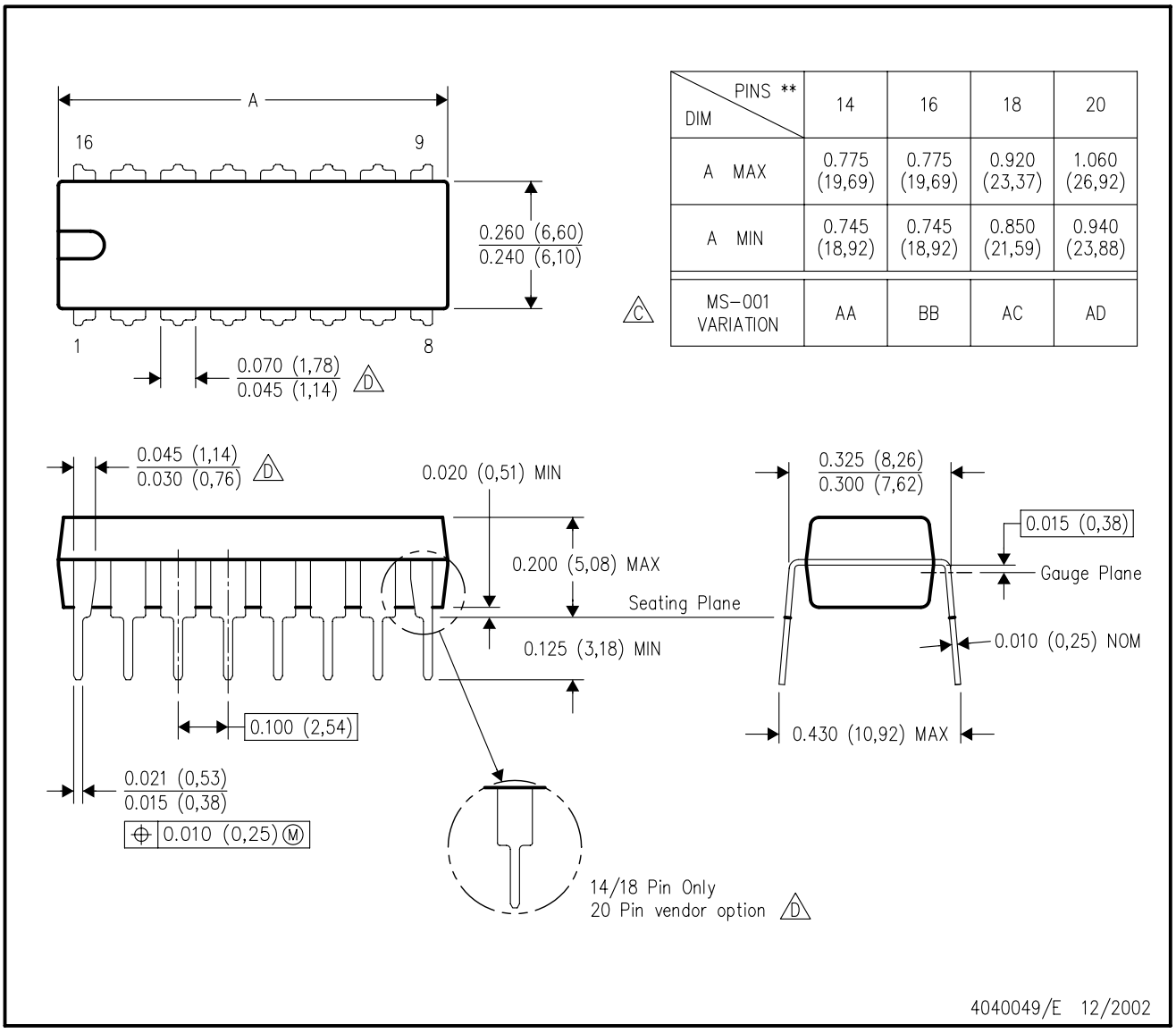
4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

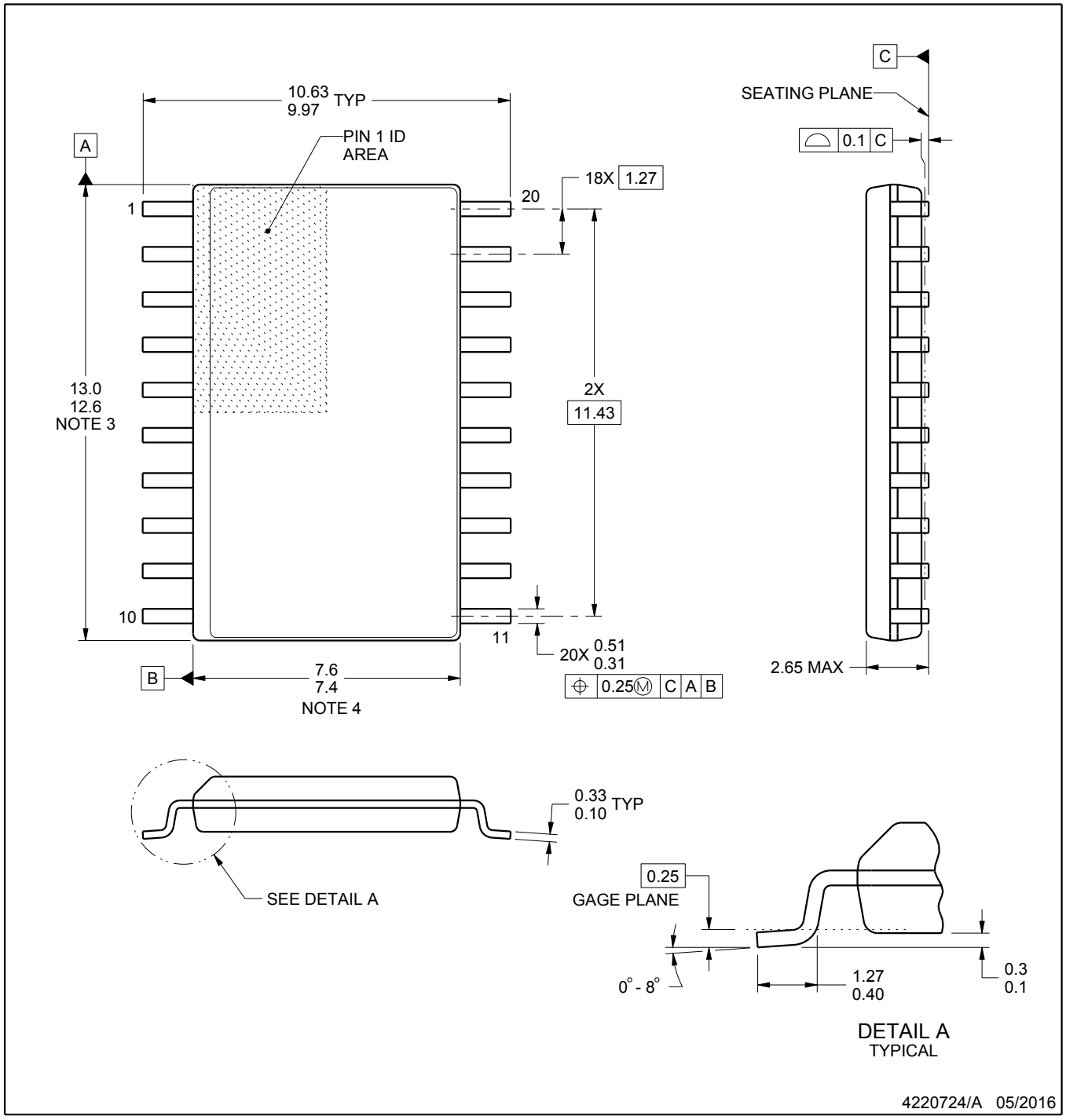
N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



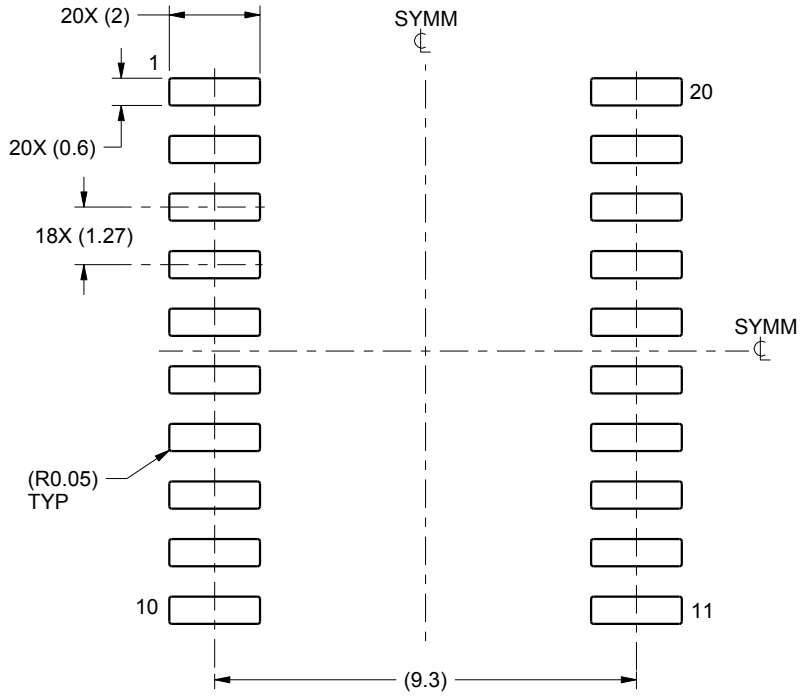
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

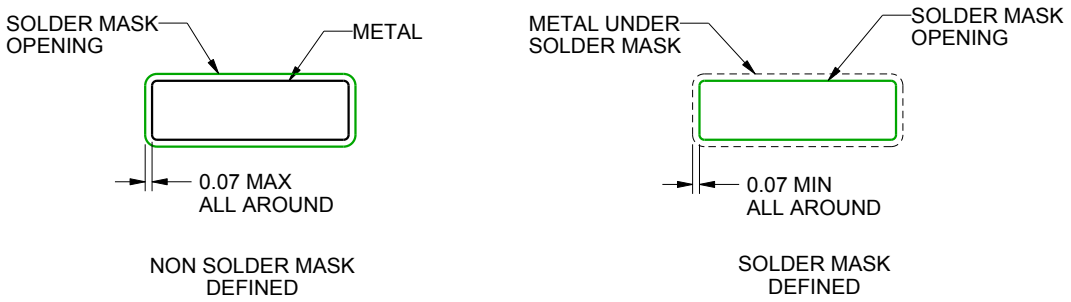


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

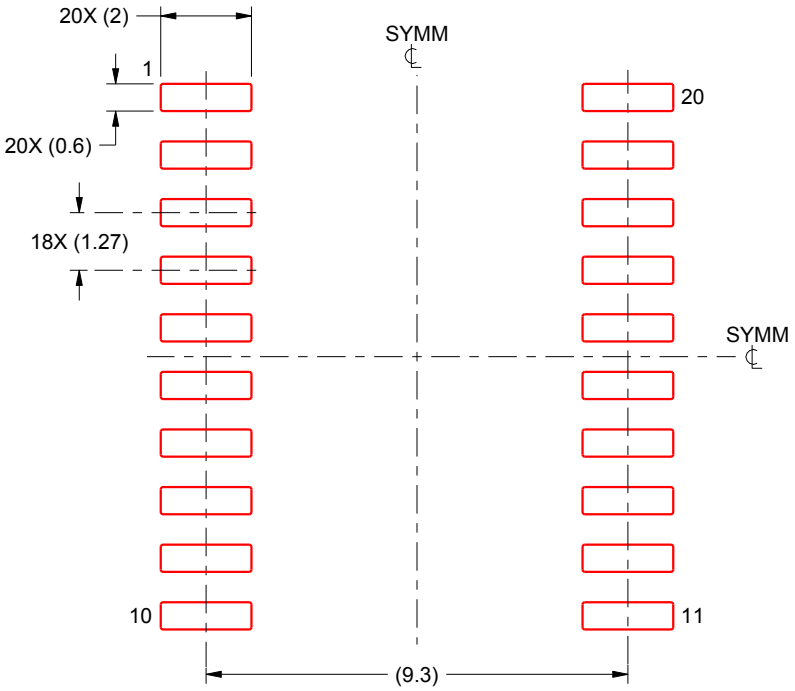


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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