

TLV1704-SEP 2.2V~36V、宇宙向け強化プラスチックの耐放射線マイクロパワー・クワッド・コンパレータ

1 特長

- VID V62/18613
- 耐放射線
 - シングル・イベント・ラッチアップ (SEL) 耐性: 125°Cで 43MeV-cm²/mg まで
 - 30krad(Si) まで ELDRS フリー
 - すべてのウェハー・ロットについて、20krad(Si) までの吸収線量 (TID) RLAT (Radiation Lot Acceptance Test)
- 宇宙向けに強化されたプラスチック
 - 管理されたベースライン
 - 金線
 - NiPdAu リード仕上げ
 - 単一のアセンブリ/テスト施設
 - 単一の製造施設
 - 軍用温度範囲 (-55°C~125°C) で利用可能
 - 長い製品ライフ・サイクル
 - 製品変更通知期間の延長
 - 製品のトレーサビリティ
 - モールド・コンパウンドの改良による低いガス放出
- 電源電圧範囲: 2.2V~36V または $\pm 1.1V \sim \pm 18V$
- 低い静止電流: 55 μA (コンパレータあたり)
- 入力同相範囲に両レールを含む
- 小さい伝搬遅延時間: 560ns
- 低い入力オフセット電圧: 300 μV
- オープン・コレクタ出力:
 - 電源電圧に関係なく負電源を最大 36V 上回る
- 小型パッケージ:
 - クワッド: TSSOP-14

2 アプリケーション

- コマンドとデータの処理 (C&DH)
- 航空機のコックピット・ディスプレイ
- 飛行制御ユニット
- 衛星用電源システム (EPS)

3 概要

TLV1704-SEP (クワッド) デバイスは広い電源電圧範囲、レール・ツー・レール入力、小さい静止電流、短い伝搬遅延が特長です。これらのデバイスは、すべての機能を業界標準の超小型パッケージで提供しており、市販の汎用コンパレータでは最高水準のものです。

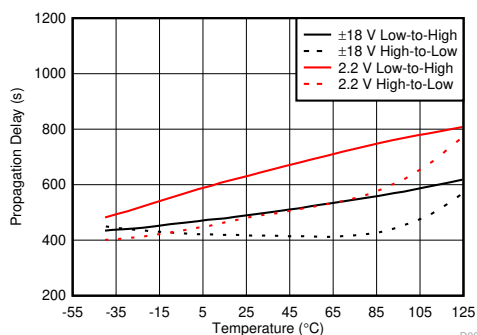
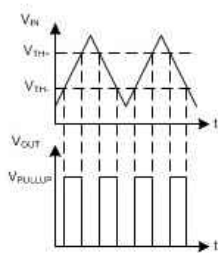
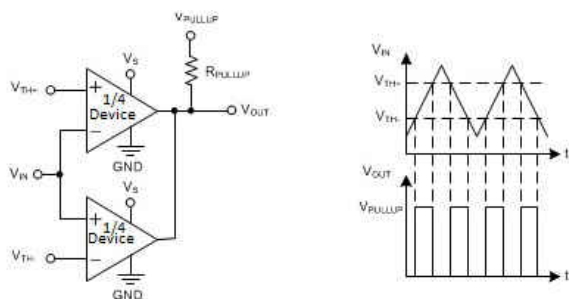
オープン・コレクタ出力により、TLV1704-SEP の電源電圧に関係なく、負電源を最大 36V 上回る電圧レールまで出力を引き上げることができます。

このデバイスはマイクロパワー・コンパレータです。低い入力オフセット電圧、小さい入力バイアス電流、小さい消費電流、およびオープン・コレクタ構成により、TLV1704-SEP デバイスには、単純な電圧検出からシングル・リレーの駆動まで、ほぼすべてのアプリケーションに対応する柔軟性があります。

製品情報

部品番号	グレード (1)	パッケージ
TLV1704AMPWTPSEP	20 krad(Si) RLAT	TSSOP (14)
TLV1704AMPWPSEP		

- (1) 提供されているすべてのパッケージについては、データシートの末尾にあるパッケージ・オプションについての付録を参照してください。



ウィンドウ・コンパレータとしての TLV1704-SEP

安定した伝搬遅延 対 温度



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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (November 2018) to Revision A (November 2022)	Page
• ドキュメント全体にわたって表、図、相互参照の採番方法を更新.....	1
• タイトルを「放射線耐性を強化」から「耐放射線」に更新.....	1
• 「アプリケーション」を更新し、リンクを追加.....	1

5 Pin Configuration and Functions

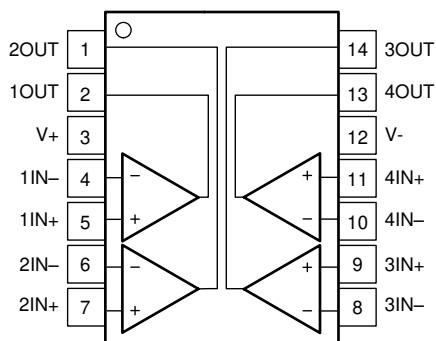


图 5-1. TLV1704-SEP PW Package 14-Pin TSSOP Top View

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
IN+	—	I	Noninverting input.
1IN+	5	I	Noninverting input, channel 1.
2IN+	7	I	Noninverting input, channel 2.
3IN+	9	I	Noninverting input, channel 3.
4IN+	11	I	Noninverting input, channel 4.
IN–	—	I	Inverting input.
1IN–	4	I	Inverting input, channel 1.
2IN–	6	I	Inverting input, channel 2.
3IN–	8	I	Inverting input, channel 3.
4IN–	10	I	Inverting input, channel 4.
OUT	—	O	Output.
1OUT	2	O	Output, channel 1.
2OUT	1	O	Output, channel 2.
3OUT	14	O	Output, channel 3.
4OUT	13	O	Output, channel 4.
V+	3	—	Positive (highest) power supply.
V–	12	—	Negative (lowest) power supply.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Supply voltage			40 (±20)	V
Signal input pins	Voltage ⁽²⁾	$(V_{S-}) - 0.5$	$(V_{S+}) + 0.5$	V
	Current ⁽²⁾		±10	mA
Output short-circuit ⁽³⁾			Continuous	mA
Operating Junction temperature, T_J		–55	125	°C
Storage temperature, T_{stg}		–65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Input pins are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails must be current limited to 10 mA or less.
- (3) Short-circuit to ground; one comparator per package.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 ⁽¹⁾	±1000	V
	Charged-device model (CDM), per AEC Q100-011	±1000	

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage $V_S = (V_{S+}) - (V_{S-})$	2.2 (±1.1)		36 (±18)	V
Specified temperature	–55		125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TLV1704-SEP	UNIT
		PW (TSSOP)	
		14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	128.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	69.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	9.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	69.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

at $T_A = -55^\circ\text{C}$ to 125°C , $V_S = 2.2\text{ V}$ to 36 V , $C_L = 15\text{ pF}$, $R_{PULLUP} = 5.1\text{ k}\Omega$, $V_{CM} = V_S / 2$, and $V_S = V_{PULLUP}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V _{OS}	Input offset voltage	T _A = 25°C, V _S = 2.2 V		±0.5	±3.5	mV
		T _A = 25°C, V _S = 36 V		±0.3	±2.5	mV
		T _A = -55°C to 125°C			±5.5	mV
dV _{OS} /dT	Input offset voltage drift	T _A = -55°C to 125°C		±4	±20	μV/°C
PSRR	Power-supply rejection ratio	T _A = 25°C		15	100	μV/V
		T _A = -55°C to 125°C		20		μV/V
INPUT VOLTAGE RANGE						
V _{CM}	Common-mode voltage range	T _A = -55°C to 125°C	(V-)		(V+)	V
INPUT BIAS CURRENT						
I _B	Input bias current	T _A = 25°C		5	15	nA
		T _A = -55°C to 125°C			20	nA
I _{OS}	Input offset current	T _A = 25°C		0.5		nA
C _{LOAD}	Capacitive load drive		See セクション 6.7			
OUTPUT						
V _O	Voltage output swing from rail	I _O ≤ 4 mA, input overdrive = 100 mV, V _S = 36 V			1100	mV
		I _O = 0 mA, input overdrive = 100 mV, V _S = 36 V			700	mV
I _{SC}	Short circuit sink current	T _A = 25°C		20		mA
	Output leakage current	V _{IN+} > V _{IN-} , T _J = 25°C		70		nA
POWER SUPPLY						
V _S	Specified voltage range		2.2		36	V
I _Q	Quiescent current (per channel)	I _O = 0 A , T _A = 25°C		55	75	μA
		I _O = 0 A, T _A = -55°C to 125°C			100	μA

6.6 Switching Characteristics

at $T_A = -55^\circ\text{C}$ to 125°C , $V_S = 2.2\text{ V}$ to 36 V , $C_L = 15\text{ pF}$, $R_{PULLUP} = 5.1\text{ k}\Omega$, $V_{CM} = V_S / 2$, and $V_S = V_{PULLUP}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pHL} Propagation delay time, high-to-low	Input overdrive = 100 mV, $T_A = 25^\circ\text{C}$		460		ns
t_{pLH} Propagation delay time, low-to-high	Input overdrive = 100 mV, $T_A = 25^\circ\text{C}$		560		ns
t_R Rise time	Input overdrive = 100 mV, $T_A = 25^\circ\text{C}$		365		ns
t_F Fall time	Input overdrive = 100 mV, $T_A = 25^\circ\text{C}$		240		ns

6.7 Typical Characteristics

at $T_A = 25^\circ\text{C}$, $V_S = 5\text{ V}$, $R_{\text{PULLUP}} = 5.1\text{ k}\Omega$, and input overdrive = 100 mV (unless otherwise noted)

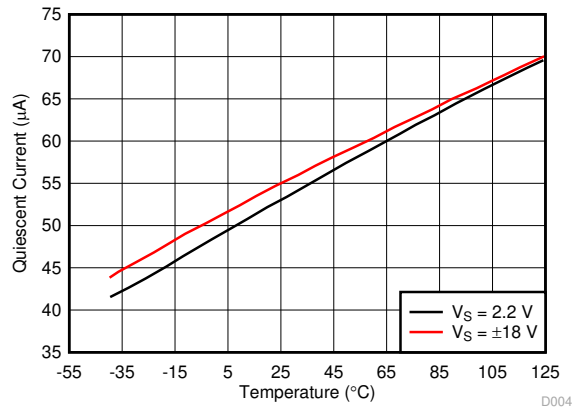


Figure 6-1. Quiescent Current vs Temperature

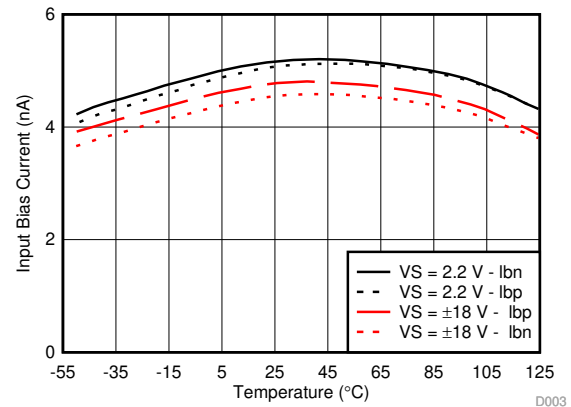


Figure 6-2. Input Bias Current vs Temperature

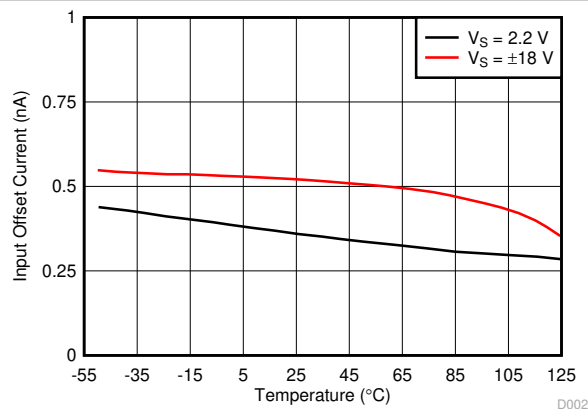


Figure 6-3. Input Offset Current vs Temperature

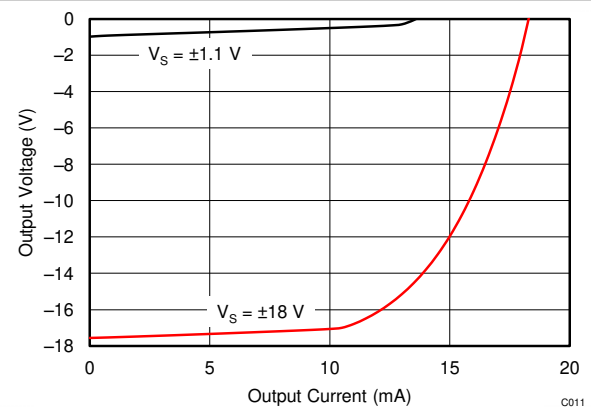


Figure 6-4. Output Voltage vs Output Current

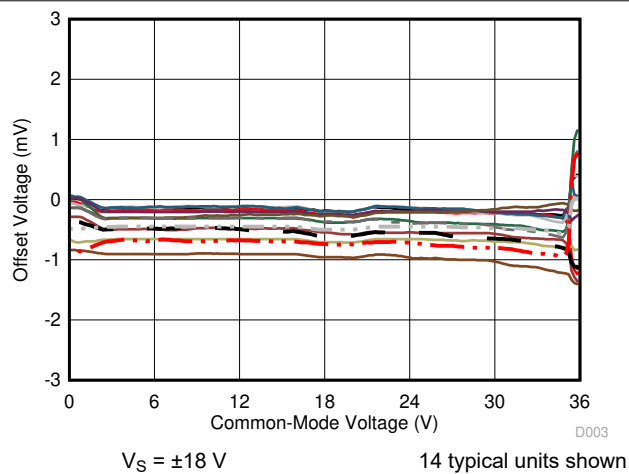


Figure 6-5. Offset Voltage vs Common-Mode Voltage

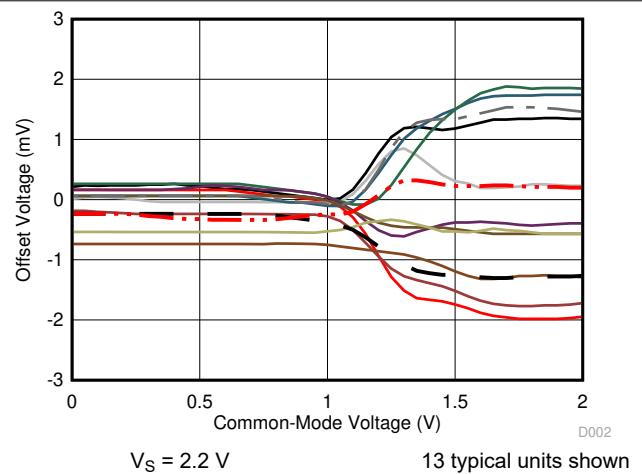


Figure 6-6. Offset Voltage vs Common-Mode Voltage

6.7 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = 5\text{ V}$, $R_{\text{PULLUP}} = 5.1\text{ k}\Omega$, and input overdrive = 100 mV (unless otherwise noted)

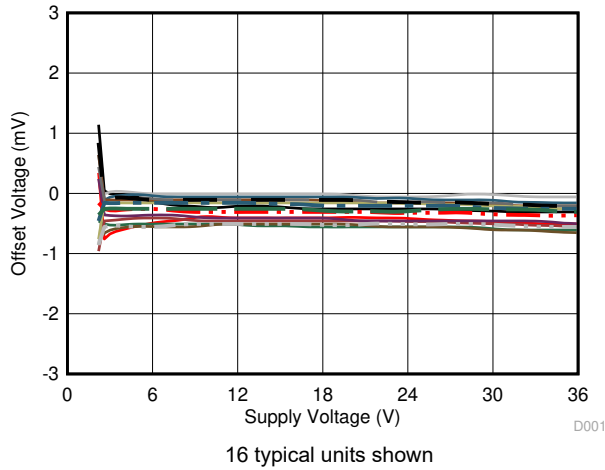


FIG 6-7. Offset Voltage vs Supply Voltage

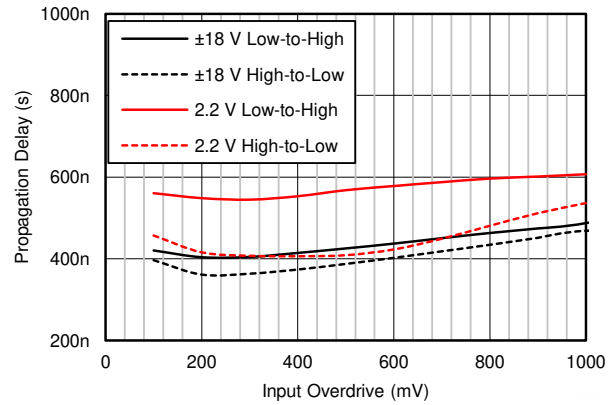


FIG 6-8. Propagation Delay vs Input Overdrive

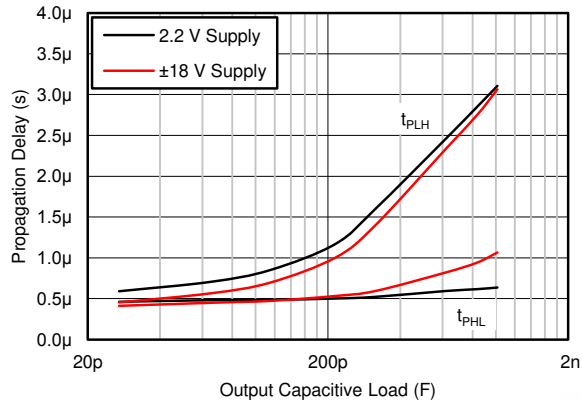
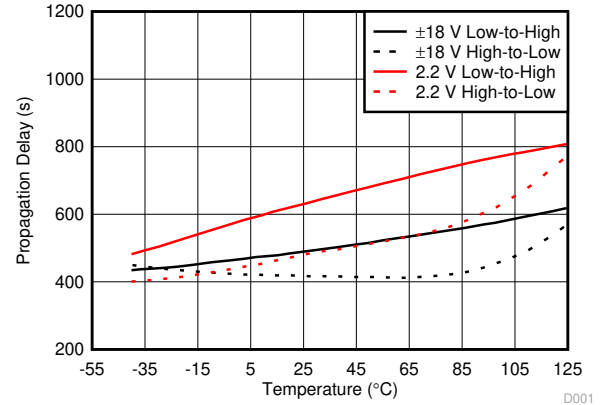
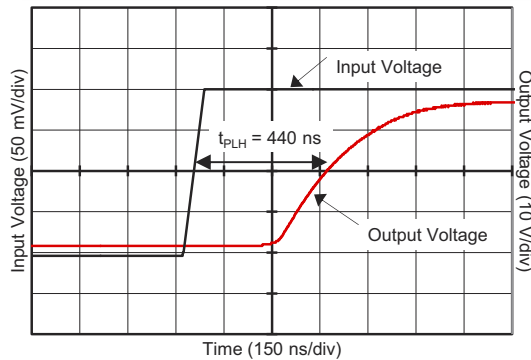


FIG 6-9. Propagation Delay vs Capacitive Load



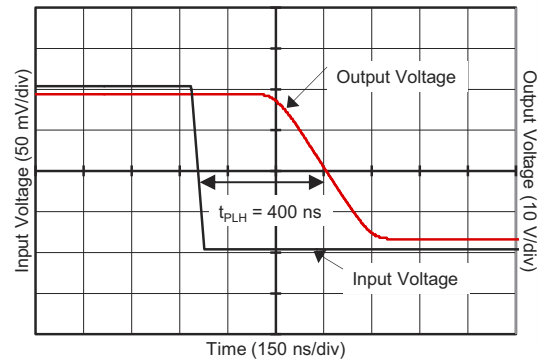
$V_{\text{OD}} = 100\text{ mV}$

FIG 6-10. Propagation Delay vs Temperature



$V_S = 36\text{ V}$ Overdrive = 100 mV

FIG 6-11. Propagation Delay (T_{pLH})

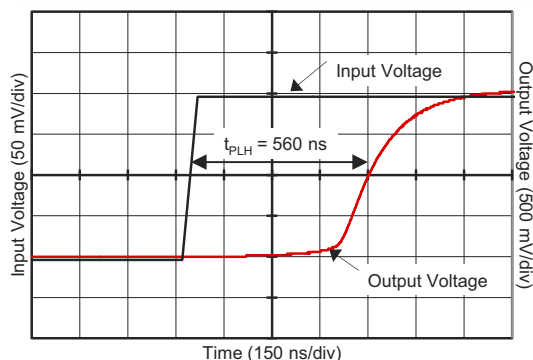


$V_S = 36\text{ V}$ Overdrive = 100 mV

FIG 6-12. Propagation Delay (T_{pHL})

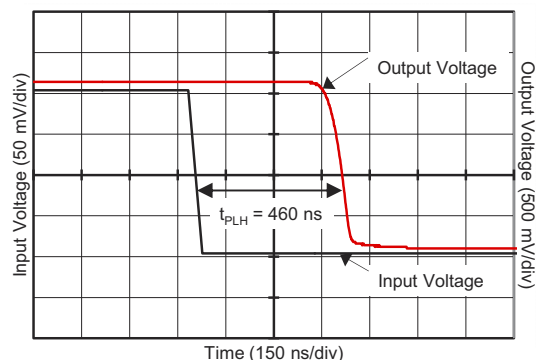
6.7 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = 5\text{ V}$, $R_{\text{PULLUP}} = 5.1\text{ k}\Omega$, and input overdrive = 100 mV (unless otherwise noted)



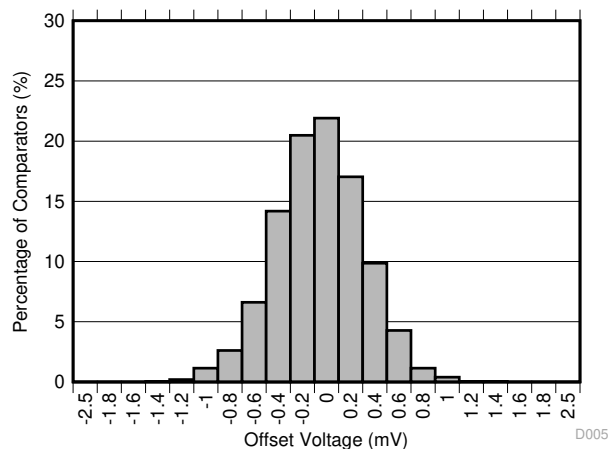
$V_S = 2.2\text{ V}$ Overdrive = 100 mV

FIG 6-13. Propagation Delay (T_{pLH})



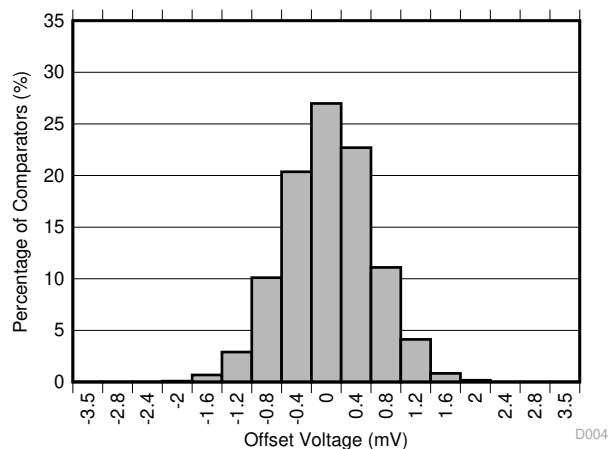
$V_S = 2.2\text{ V}$ Overdrive = 100 mV

FIG 6-14. Propagation Delay (T_{pHL})



$V_S = \pm 18\text{ V}$ Distribution taken from 2524 comparators

FIG 6-15. Offset Voltage Production Distribution



$V_S = 2.2\text{ V}$ Distribution taken from 2524 comparators

FIG 6-16. Offset Voltage Production Distribution

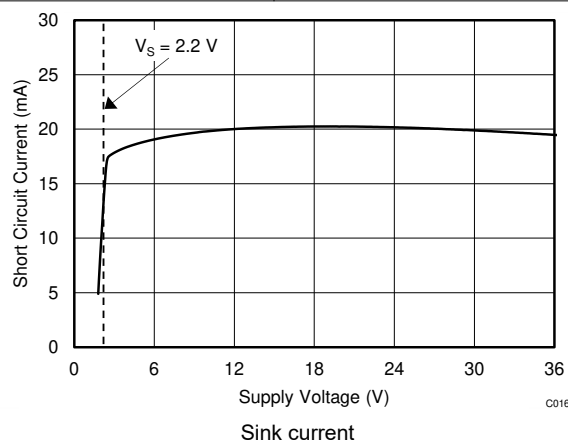


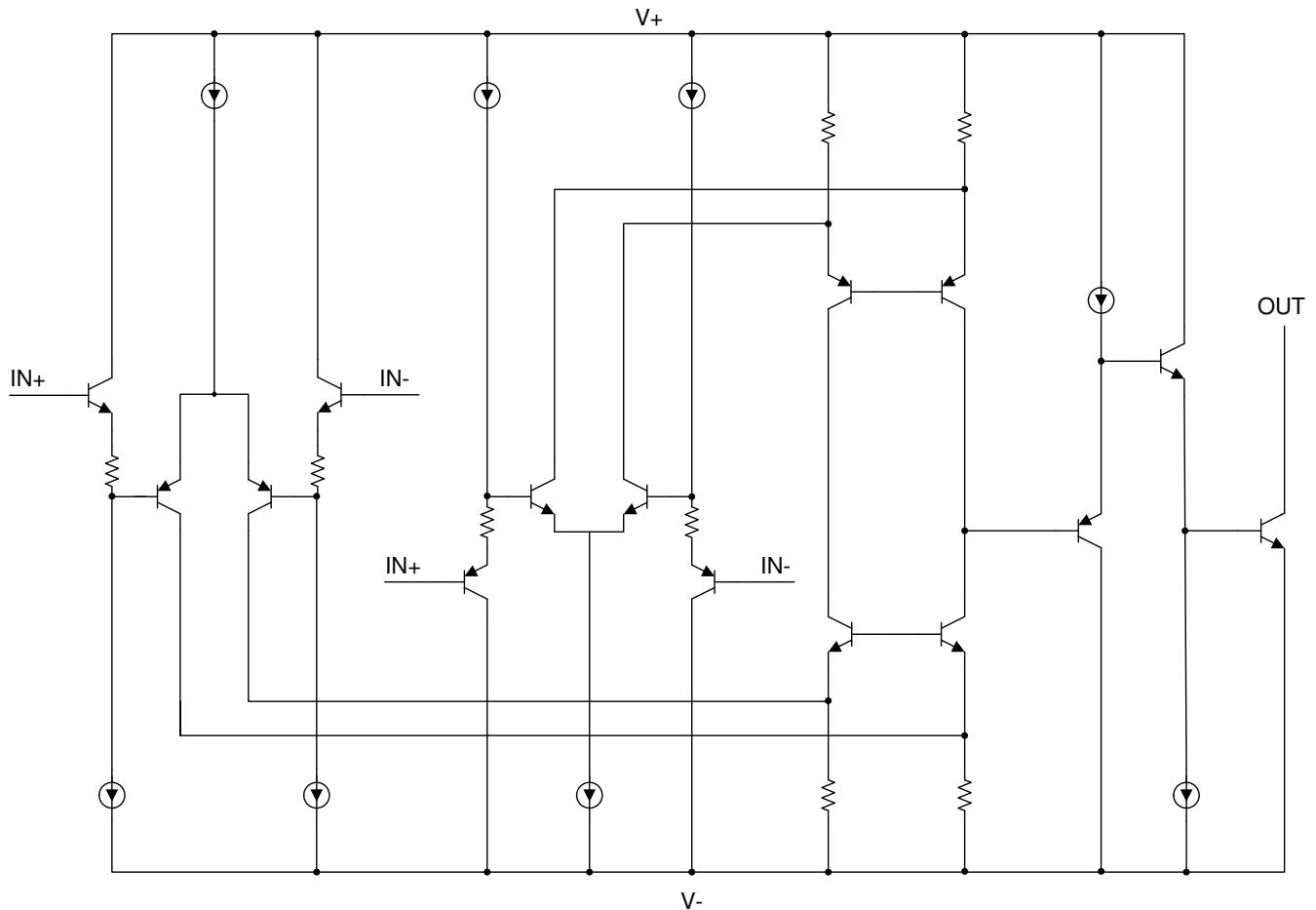
FIG 6-17. Short-Circuit Current vs Supply Voltage

7 Detailed Description

7.1 Overview

The TLV1704-SEP comparator features rail-to-rail input and output on supply voltages as high as 36 V. The rail-to-rail input stage enables detection of signals close to the supply and ground. The open-collector configuration allows the device to be used in wired-OR configurations, such as a window comparator. A low supply current of 55 μA per channel with small, space-saving packages, makes these comparators versatile for use in a wide range of applications, from portable to industrial.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Comparator Inputs

The TLV1704-SEP device is a rail-to-rail input comparator, with an input common-mode range that includes the supply rails. The TLV1704-SEP device is designed to prevent phase inversion when the input pins exceed the supply voltage. [Figure 7-1](#) shows the TLV1704-SEP device response when input voltages exceed the supply, resulting in no phase inversion.

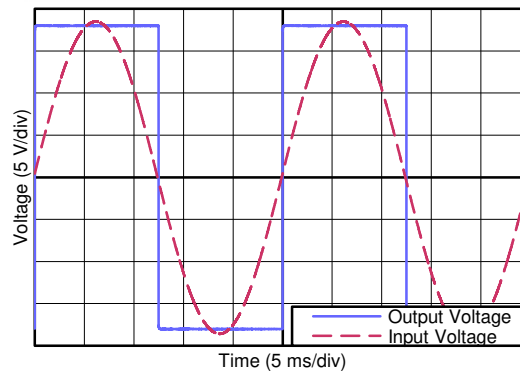


Figure 7-1. No Phase Inversion: Comparator Response to Input Voltage (Propagation Delay Included)

7.4 Device Functional Modes

7.4.1 Setting Reference Voltage

Using a stable reference is important when setting the transition point for the TLV1704-SEP device. The [REF3333](#), as shown in [Figure 7-2](#), provides a 3.3-V reference voltage with low drift and only 3.9 μ A of quiescent current.

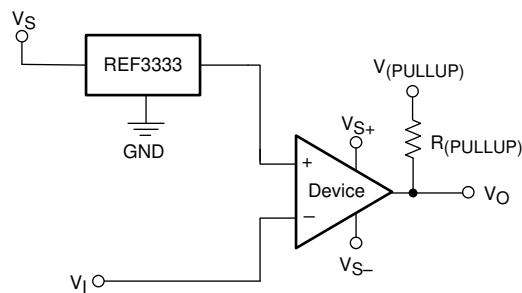


Figure 7-2. Reference Voltage for the TLV1704-SEP

8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

The TLV1704-SEP device can be used in a wide variety of applications, such as zero crossing detectors, window comparators, over and undervoltage detectors, and high-side voltage sense circuits.

8.2 Typical Application

Comparators are used to differentiate between two different signal levels. For example, a comparator differentiates between an overtemperature and normal-temperature condition. However, noise or signal variation at the comparison threshold causes multiple transitions. This application example sets upper and lower hysteresis thresholds to eliminate the multiple transitions caused by noise.

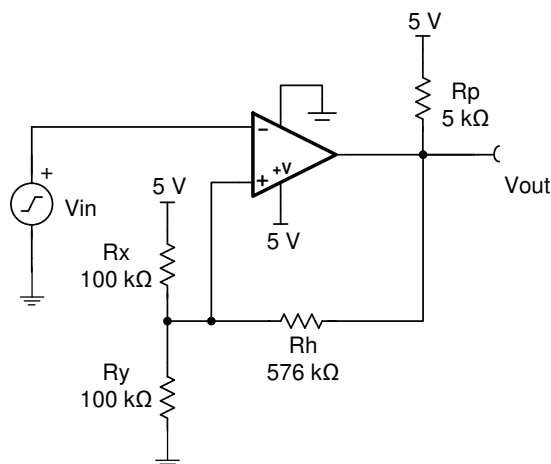


図 8-1. Comparator Schematic With Hysteresis

8.2.1 Design Requirements

The design requirements are as follows:

- Supply voltage: 5 V
- Input: 0 V to 5 V
- Lower threshold (VL) = 2.3 V $\pm$ 0.1 V
- Upper threshold (VH) = 2.7 V $\pm$ 0.1 V
- VH – VL = 2.4 V $\pm$ 0.1 V
- Low-power consumption

8.2.2 Detailed Design Procedure

Make a small change to the comparator circuit to add hysteresis. Hysteresis uses two different threshold voltages to avoid the multiple transitions introduced in the previous circuit. The input signal must exceed the upper threshold (VH) to transition low, or below the lower threshold (VL) to transition high.

✎ 8-1 illustrates hysteresis on a comparator. Resistor Rh sets the hysteresis level. An open-collector output stage requires a pullup resistor (Rp). The pullup resistor creates a voltage divider at the comparator output that introduces an error when the output is at logic high. This error can be minimized if $R_h > 100 R_p$.

When the output is at a logic high (5 V), Rh is in parallel with Rx (ignoring Rp). This configuration drives more current into Ry, and raises the threshold voltage (VH) to 2.7 V. The input signal must drive above $V_H = 2.7$ V to cause the output to transition to logic low (0 V).

When the output is at logic low (0 V), Rh is in parallel with Ry. This configuration reduces the current into Ry, and reduces the threshold voltage to 2.3 V. The input signal must drive below $V_L = 2.3$ V to cause the output to transition to logic high (5 V).

For more details on this design and other alternative devices that can be used in place of the TLV1702, refer to Precision Design [TIPD144](#), *Comparator with Hysteresis Reference Design*.

8.2.3 Application Curve

✎ 8-2 shows the upper and lower thresholds for hysteresis. The upper threshold is 2.76 V and the lower threshold is 2.34 V, both of which are close to the design target.

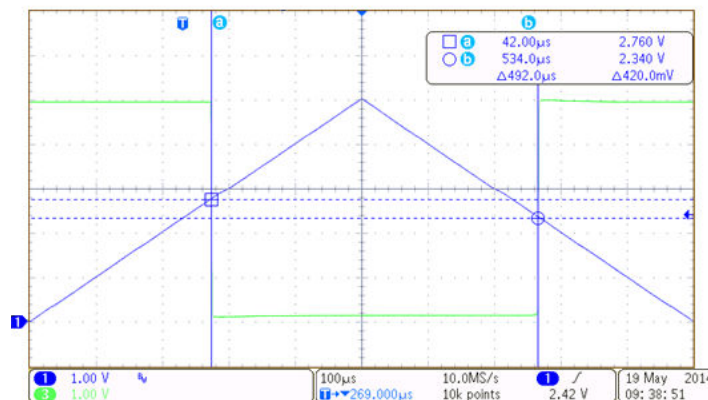


図 8-2. TLV1701 Upper and Lower Threshold With Hysteresis

8.3 Power Supply Recommendations

The TLV1704-SEP device is specified for operation from 2.2 V to 36 V (± 1.1 to ± 18 V); many specifications apply from -55°C to 125°C . Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the [セクション 6.7](#) section.

注意

Supply voltages larger than 40 V can permanently damage the device; see the [セクション 6.1](#).

Place 0.1-μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement; see the [セクション 8.4.1](#) section.

8.4 Layout

8.4.1 Layout Guidelines

Comparators are very sensitive to input noise. For best results, maintain the following layout guidelines:

- Use a printed-circuit board (PCB) with a good, unbroken low-inductance ground plane. Proper grounding (use of ground plane) helps maintain specified performance of the TLV1704-SEP device.
- To minimize supply noise, place a decoupling capacitor (0.1- μ F ceramic, surface-mount capacitor) as close as possible to V_S as shown in [Figure 8-3](#).
- On the inputs and the output, keep lead lengths as short as possible to avoid unwanted parasitic feedback around the comparator. Keep inputs away from the output.
- Solder the device directly to the PCB rather than using a socket.
- For slow-moving input signals, take care to prevent parasitic feedback. A small capacitor (1000 pF or less) placed between the inputs can help eliminate oscillations in the transition region. This capacitor causes some degradation to propagation delay when the impedance is low. Run the topside ground plane between the output and inputs.
- Run the ground pin ground trace under the device up to the bypass capacitor, shielding the inputs from the outputs.

8.4.2 Layout Example

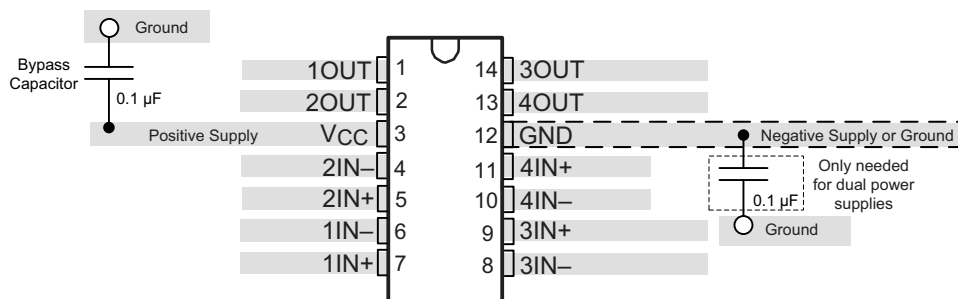


Figure 8-3. Comparator Board Layout

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- [Precision Design, Comparator with Hysteresis Reference Design](#), TIDU020
- [REF33xx 3.9- \$\mu\$ A, SC70-3, SOT-23-3, and UQFN-8, 30-ppm/ \$^{\circ}\$ C Drift Voltage Reference](#), SBOS392

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 サポート・リソース

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9.4 Trademarks

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9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV1704AMPWPSEP	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	1704SEP	Samples
TLV1704AMPWTPSEP	ACTIVE	TSSOP	PW	14	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	1704SEP	Samples
V62/18613-01XE	ACTIVE	TSSOP	PW	14	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	1704SEP	Samples
V62/18613-01XE-T	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	1704SEP	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TLV1704-SEP :

- Automotive : [TLV1704-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

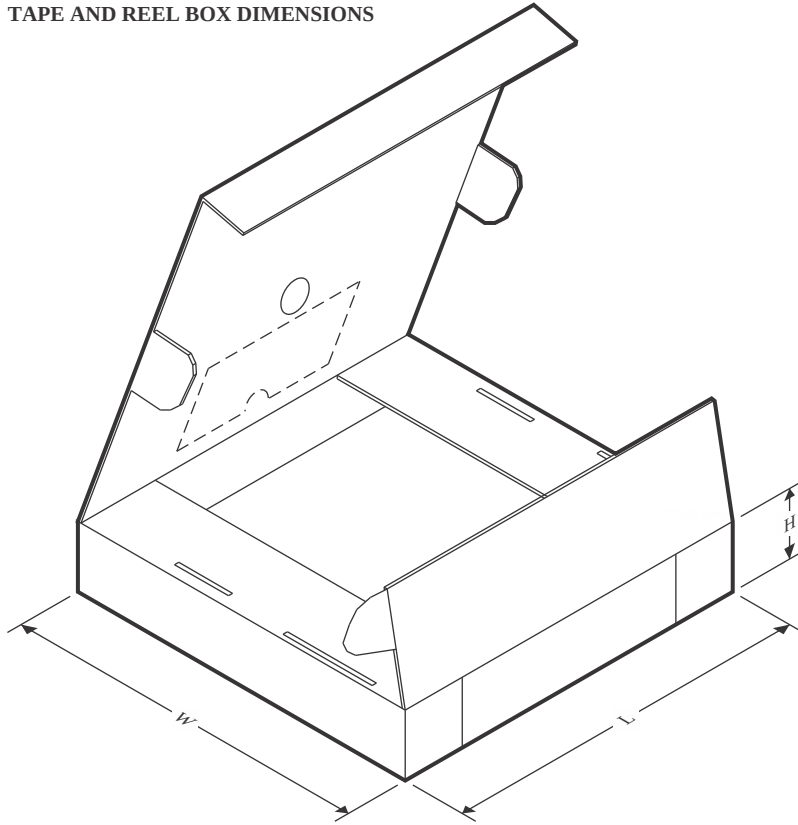
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV1704AMPWTPSEP	TSSOP	PW	14	250	180.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV1704AMPWTPSEP	TSSOP	PW	14	250	210.0	185.0	35.0

TUBE

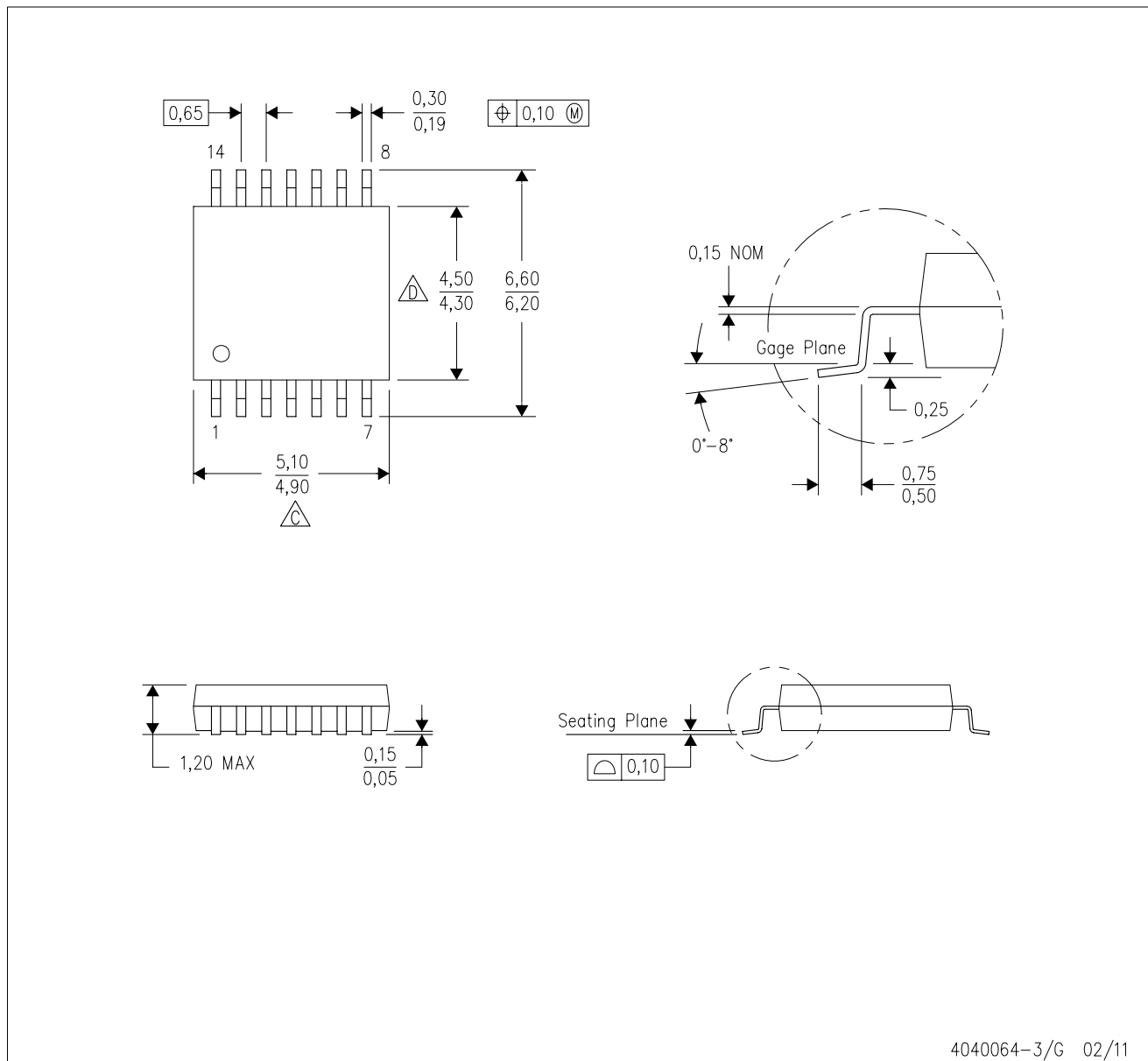


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
TLV1704AMPWPSEP	PW	TSSOP	14	90	530	10.2	3600	3.5
V62/18613-01XE-T	PW	TSSOP	14	90	530	10.2	3600	3.5

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE

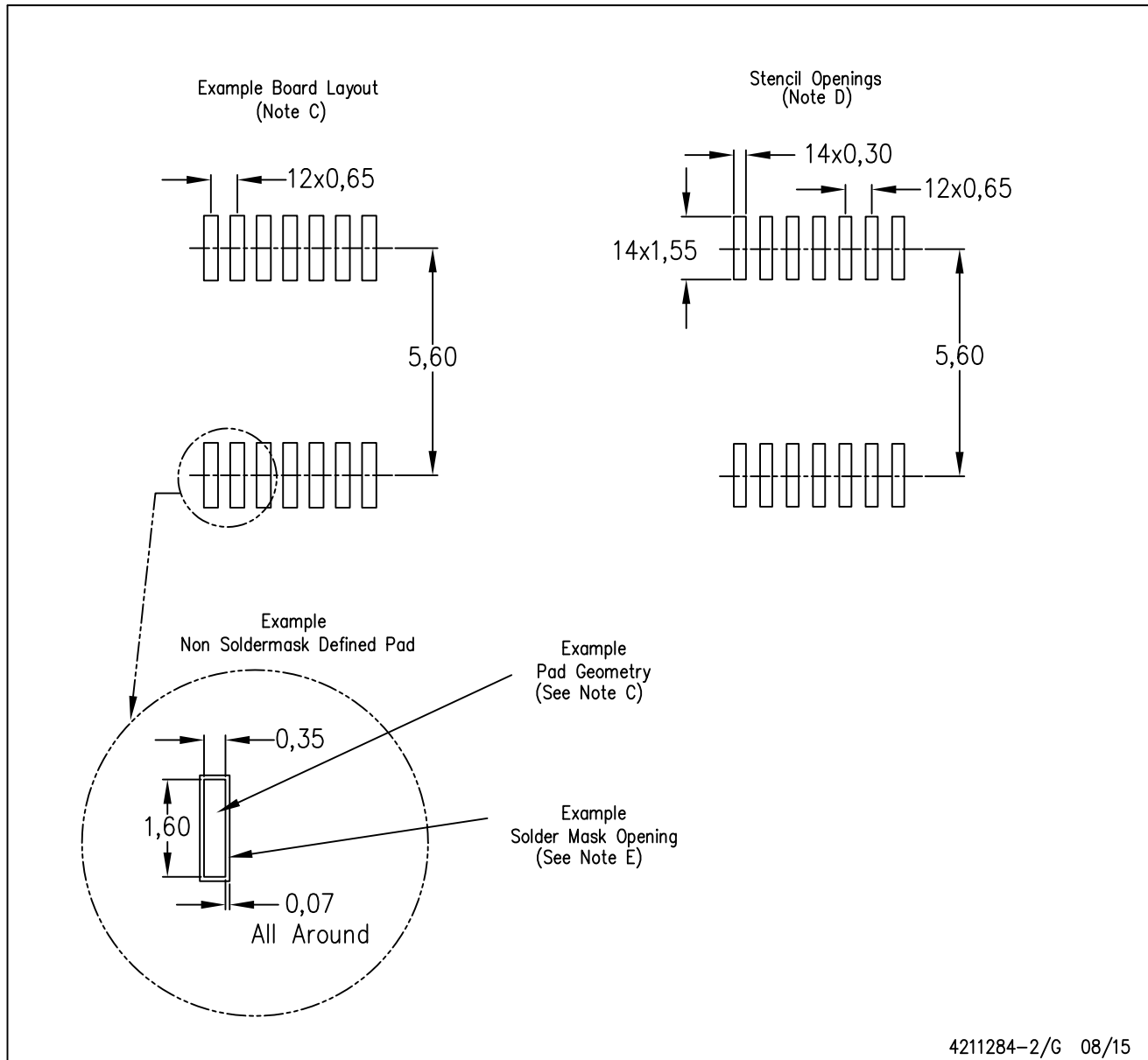


4040064-3/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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