TLVx365 50MHz、ゼロ・クロスオーバー、高 CMRR、RRIO オペアンプ

1 特長

- ゲイン帯域幅:50MHz
- ゼロ・クロスオーバー歪みトポロジ:
  - CMRR:115dB (代表値)
  - レール・ツー・レール入出力
    - 電源レールを 100mV 超える入力
- ノイズ:4.5nV/√Hz
- スルーレート:27V/μs
- 高速セトリング:0.2μs で 0.01%
- 精度:
  - オフセットのドリフト:2μV/℃ (最大値)
  - 入力バイアス電流:20pA (最大値)
- 動作電圧 2.2V～5.5V

2 アプリケーション

- シグナル・コンディショニング
- データ・アクイジション
- アクティブ・フィルタ
- 試験用機器
- オーディオ
- 広帯域アンプ
- ラック・サーバー

3 概要

TLV365 および TLV2365 デバイス (TLVx365) は、ゼロクロスオーバー、レール・ツー・レール入出力の CMOS オペアンプのファミリで、低電圧およびコスト重視のアプリケーション向けに最適化されています。低ノイズ (4.5nV/√Hz) および高速動作 (50MHz のゲイン帯域幅) であることから、これらのデバイスはローサイド電流センシング、オーディオ、シグナル・コンディショニング、センサ増幅などのアプリケーションのサンプリング A/D コンバータ (ADC) を駆動するのに最適です。

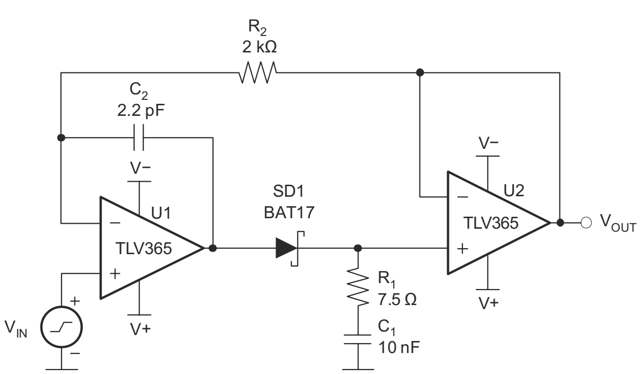
特長として、優れた同相除去比 (CMRR)、クロスオーバー歪みがない入力段、高い入力インピーダンス、およびレール・ツー・レールの入出力スイング能力が挙げられます。入力同相範囲には、負と正の電源の両方が含まれています。出力電圧のスイングは、レールの 10mV の範囲内です。

TLVx365 は、−40℃～+125℃での動作が規定されています。

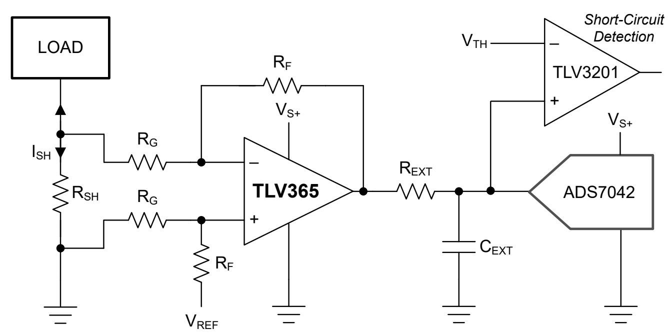
製品情報

部品番号	チャネル数	パッケージ (1)
TLV365	シングル	DBV (SOT-23、5)
TLV2365	デュアル	D (SOIC、8)

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



高速セトリング・ピーク検出器



TLVx365 電流センシング用

Table of Contents

4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (June 2023) to Revision B (September 2023) — **Page**

- TLV2365 のステータスを「事前情報」から「量産データ」(アクティブ) に変更 1

Changes from Revision * (December 2022) to Revision A (June 2023) — **Page**

- TLV2365 のステータスを「開発中製品」から「事前情報」に変更 1
- Added *Device Comparison Table* 3

5 Device Comparison Table

DEVICE	INPUT TYPE	OFFSET DRIFT TYPICAL (µV/C)	MINIMUM GAIN STABLE (V/V)	I_Q/CHANNEL TYPICAL (mA)	GAIN BANDWIDTH (MHz)	SLEW RATE (V/µs)	VOLTAGE NOISE (nV/√Hz)
TLVx365	CMOS	0.4	1	4.6	50	27	4.5
OPAx607	CMOS	0.3	6	0.9	50	24	3.8
OPAx365	CMOS	1	1	4.6	50	25	4.5

6 Pin Configuration and Functions

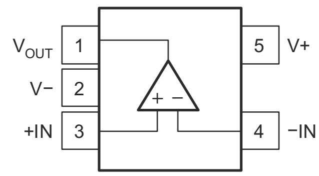


図 6-1. TLV365 DBV Package, 5-Pin SOT-23 (Top View)

表 6-1. Pin Functions: TLV365

PIN		TYPE	DESCRIPTION
NAME	NO.		
–IN	4	Input	Negative (inverting) input
+IN	3	Input	Positive (noninverting) input
V–	2	—	Negative (lowest) power supply
V+	5	—	Positive (highest) power supply
V_{OUT}	1	Output	Output

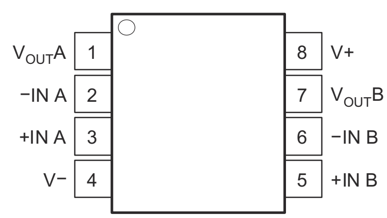


図 6-2. TLV2365 D Package, 8-Pin SOIC (Top View)

Pin Functions: TLV2365

PIN		TYPE	DESCRIPTION
NAME	NO.		
–IN A	2	Input	Negative (inverting) input signal, channel A
+IN A	3	Input	Positive (noninverting) input signal, channel A
–IN B	6	Input	Negative (inverting) input signal, channel B
+IN B	5	Input	Positive (noninverting) input signal, channel B
V–	4	—	Negative (lowest) power supply
V+	8	—	Positive (highest) power supply
V_{OUT}A	1	Output	Output, channel A
V_{OUT}B	7	Output	Output, channel B

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)[(1)]

		MIN	MAX	UNIT
V_S	Supply voltage, V_S = (V+) – (V–)		6	V
V_I	Input voltage	(V–) – 0.5	(V+) + 0.5	V
V_{ID}	Differential input voltage		±5	V
I_I	Continuous input current[(2)]		±10	mA
I_{SC}	Output short-circuit[(3)]	Continuous		
T_A	Operating temperature	–40	125	°C
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Input pins are diode-clamped to the power-supply rails. Limit the current of input signals that can swing more than 0.5 V beyond the supply rails to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002[(2)]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S	Supply voltage, V_S = (V+) – (V–)	2.2		5.5	V
T_A	Specified temperature	–40	25	125	°C

7.4 Thermal Information

THERMAL METRIC[(1)]		TLV365	TLV2365	UNIT
		DBV (SOT-23)	D (SOIC)	
		5 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	179	140	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	78	89	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	46	80	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	19	28	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	46	80	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

at V_S = 2.2 V to 5.5 V, T_A = 25°C, R_L = 10 kΩ, V_{CM},V_{OUT} = mid-supply, and gain = 1 V/V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage			±0.4	±1.9	mV
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to +125°C		±0.4	±2	µV/°C
PSRR	Power-supply rejection ratio	V_S = 2.2 V to 5.5 V, T_A = –40 to +125°C		100		dB
INPUT BIAS CURRENT						
I_B	Input bias current			±5	±20	pA
		T_A = –40°C to +125°C		See 図 7-5		
NOISE						
	Input voltage noise (peak-to-peak)	f = 0.1 Hz to 10 Hz		5.4		$µV_{PP}$
e_N	Input voltage noise density	f = 500 kHz		4.5		nV/√Hz
i_n	Input current noise density	f = 1 kHz		5.8		fA/√Hz
INPUT VOLTAGE						
V_{CM}	Common-mode voltage		(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	(V–) – 100 mV < V_{CM} < (V+) + 100 mV		115		dB
		T_A = –40°C to +125°C		110		
INPUT IMPEDANCE						
C_{IN}	Differential			5		pF
	Common-mode			1		
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	R_L = 10 kΩ, (V–) + 0.1 V < V_{OUT} < (V+) – 0.1 V	100	120		dB
		R_L = 10 kΩ, T_A = –40 to +125°C	95			
		R_L = 600 Ω, (V–) + 0.2 V < V_{OUT} < (V+) – 0.2 V	100	120		
		R_L = 600 Ω, T_A = –40 to +125°C	94			
	Phase margin			56		°
FREQUENCY RESPONSE (V_S = 5 V)						
GBW	Gain-bandwidth product			50		MHz
SR	Slew rate			27		V/µs
t_S	Settling time	0.1%, 4-V step		0.15		µs
		0.01%, 4-V step		0.2		
	Overdrive recovery time	V_{IN+} × gain > V_S		< 0.1		µs
THD + N	Total harmonic distortion + noise(6)	V_{OUT} = 4 V_{PP}, f = 1 kHz, R_L = 600 Ω		0.00025		%
	Channel-to-channel crosstalk (TLV2365 only)	V_{OUT} = 2 V_{PP}, f = 100 kHz		108		dBc
OUTPUT						
	Output voltage swing from supply rails				10	mV
		T_A = –40°C to +125°C			12	
I_{SC}	Short-circuit current			±85		mA
	Capacitive load drive			See 図 7-16		
Z_O	Open-loop output impedance	f = 1 MHz, I_O = 0 mA		40		Ω
POWER SUPPLY						
I_Q	Quiescent current per amplifier	I_O = 0 mA		4.6	5.8	mA
		I_O = 0 mA, T_A = –40°C to +125°C			6.3	

(1) Low-pass-filter bandwidth is 20 kHz for f = 1 kHz.

7.6 Typical Characteristics

at T_A = 25°C, V_S = 5 V, R_L = 10 kΩ, and gain = 1 V/V (unless otherwise noted)

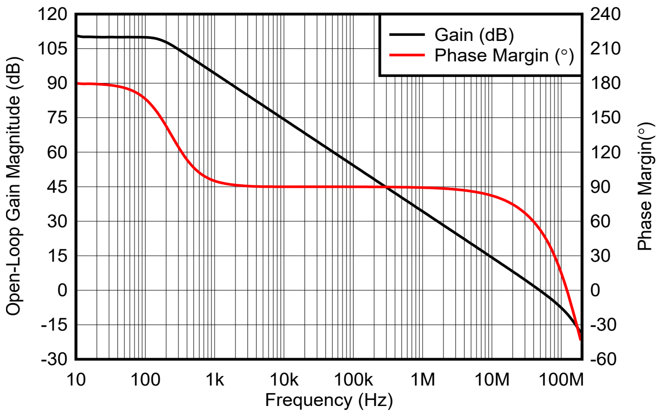


図 7-1. Open-Loop Gain and Phase vs Frequency

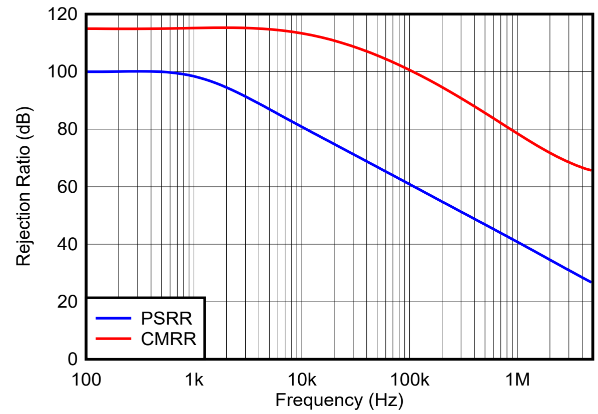
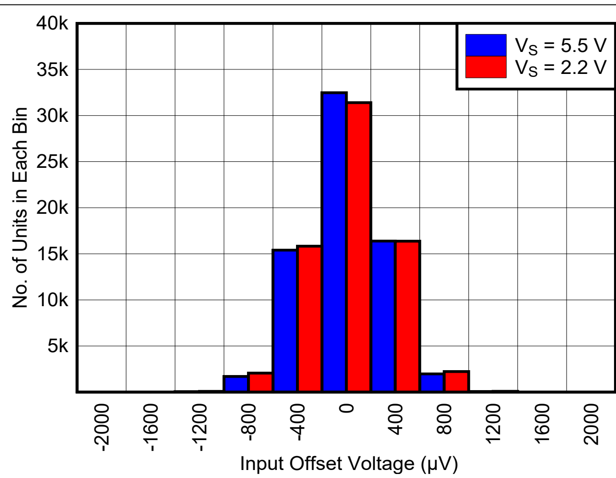
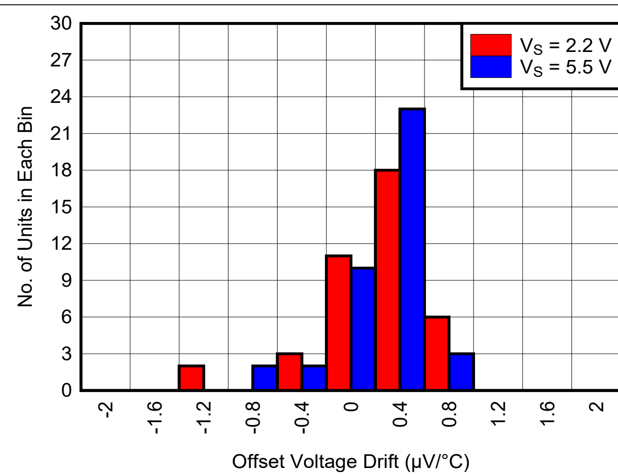


図 7-2. Power-Supply and Common-Mode Rejection Ratio



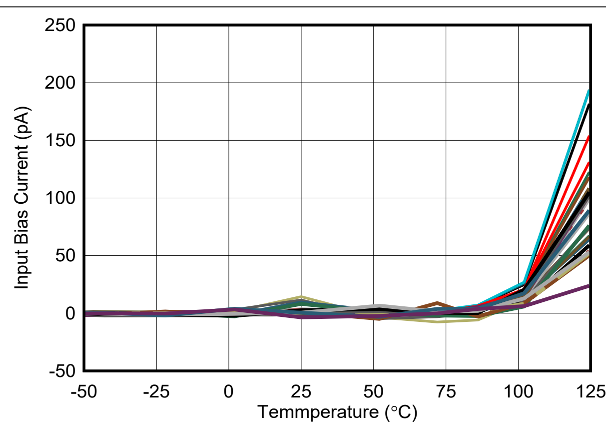
70000 units, μ = 9.3 μV, σ = 320 μV.

図 7-3. Offset Voltage Production Distribution



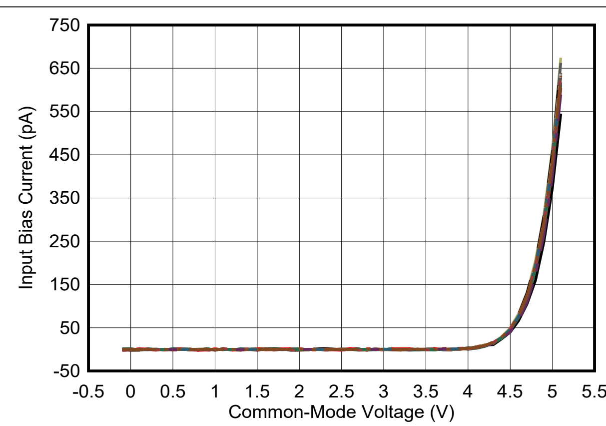
40 units, μ = 0.06 μV/°C, σ = 0.4 μV/°C

図 7-4. Offset Voltage Drift Distribution



40 units

図 7-5. Input Bias Current vs Temperature

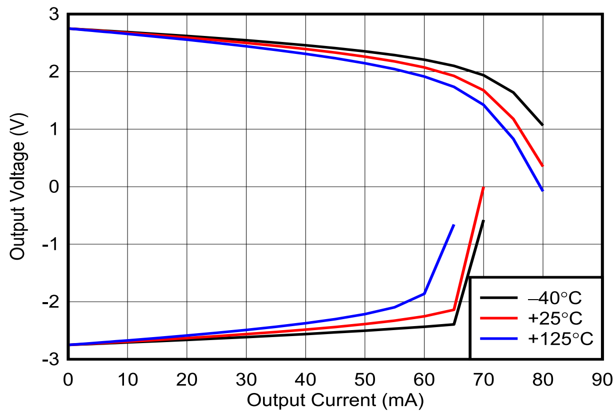


40 units

図 7-6. Input Bias Current vs Common-Mode Voltage

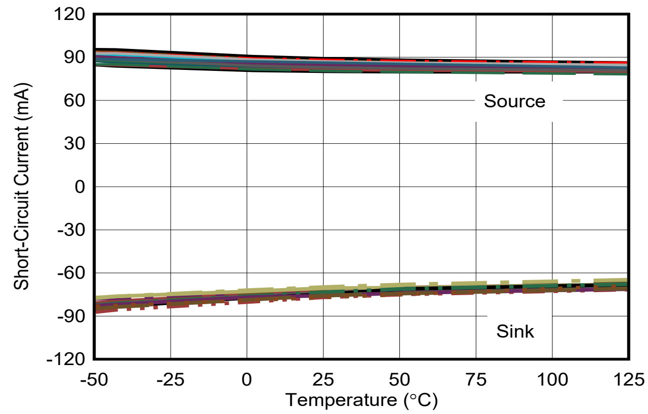
7.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, R_L = 10 kΩ, and gain = 1 V/V (unless otherwise noted)



V_S = ±2.75 V

図 7-7. Output Voltage vs Output Current



20 units

図 7-8. Short-Circuit Current vs Temperature

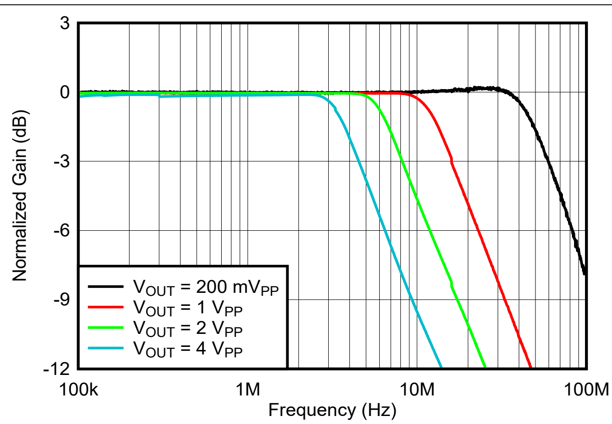


図 7-9. Frequency Response vs Output Voltage

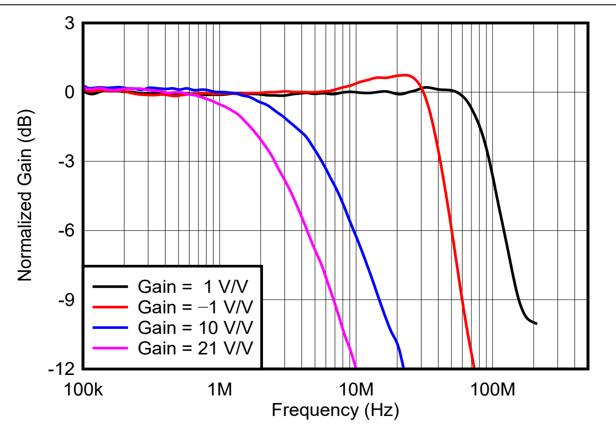


図 7-10. Small-Signal Frequency Response vs Gain

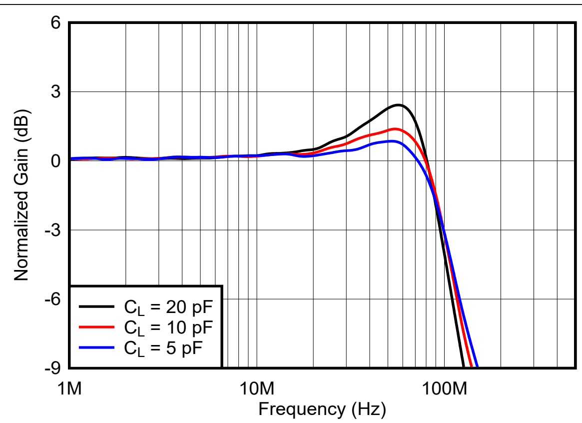
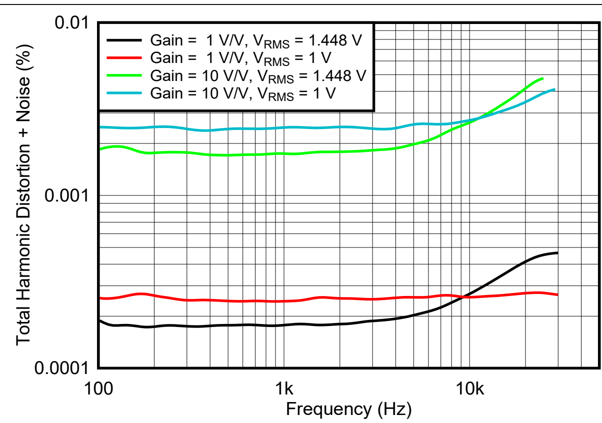


図 7-11. Small-Signal Response vs Capacitive Load



R_L = 600 Ω

図 7-12. Total Harmonic Distortion + Noise vs Frequency

7.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, R_L = 10 kΩ, and gain = 1 V/V (unless otherwise noted)

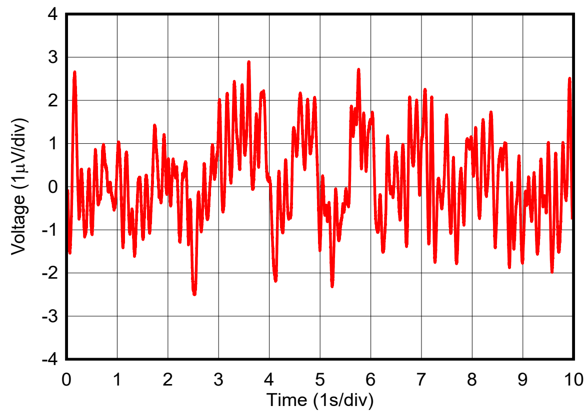


図 7-13. 0.1-Hz to 10-Hz Input Voltage Noise

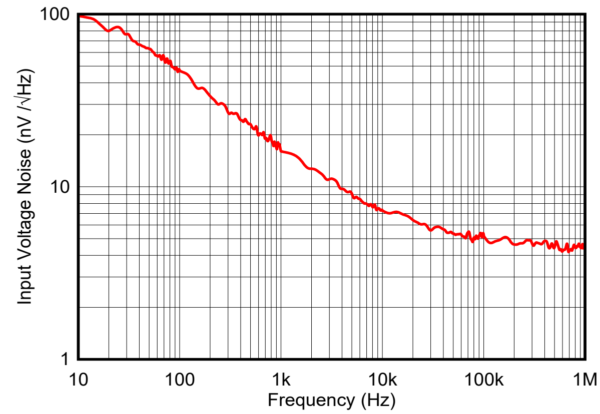


図 7-14. Input Voltage Noise Spectral Density

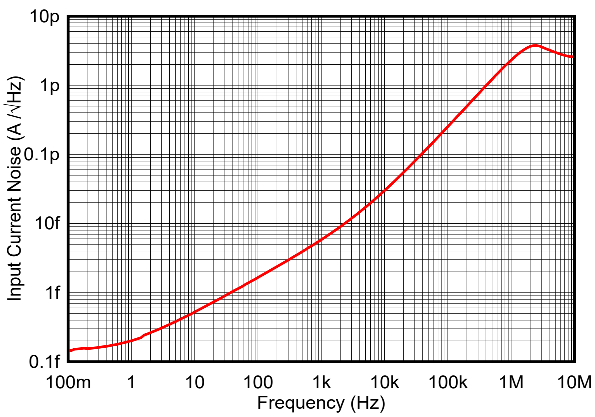
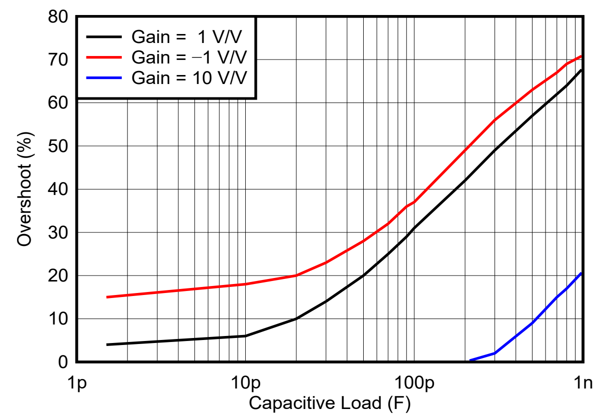
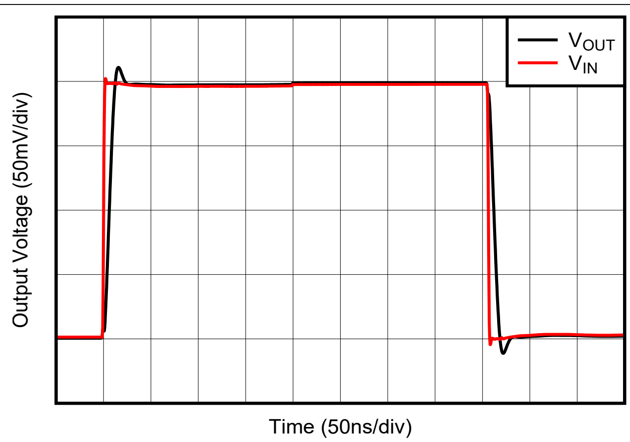


図 7-15. Input Current Noise Spectral Density



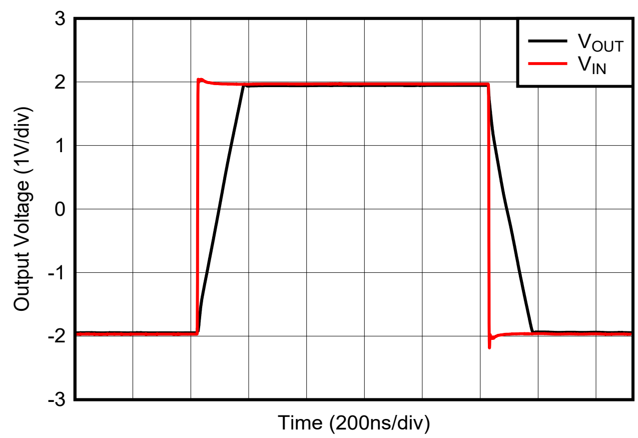
For gain ≠ 1 V/V, R_F = 1 kΩ. For gain = 1 V/V, R_F = 0 Ω.

図 7-16. Overshoot vs Capacitive Load



R_L = 600 Ω

図 7-17. Small-Signal Step Response



R_L = 600 Ω

図 7-18. Large-Signal Step Response

7.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, R_L = 10 kΩ, and gain = 1 V/V (unless otherwise noted)

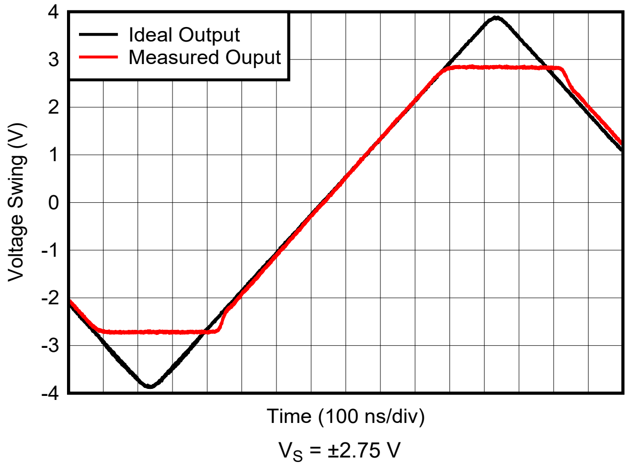


図 7-19. Overdrive Recovery

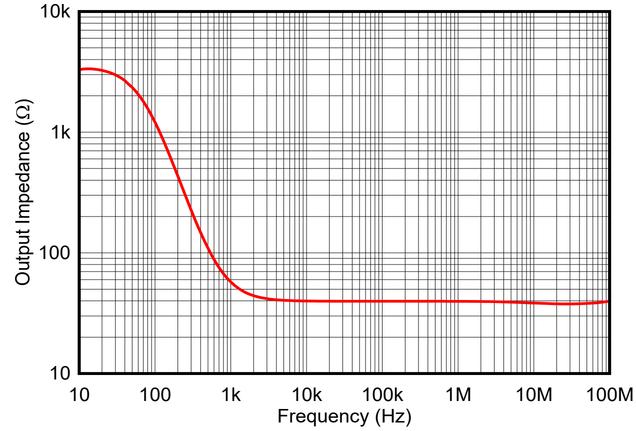


図 7-20. Open-Loop Output Impedance

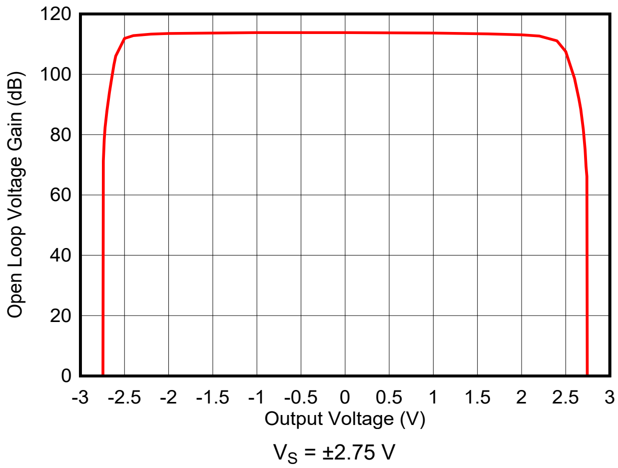


図 7-21. Open Loop Voltage Gain vs Output Voltage

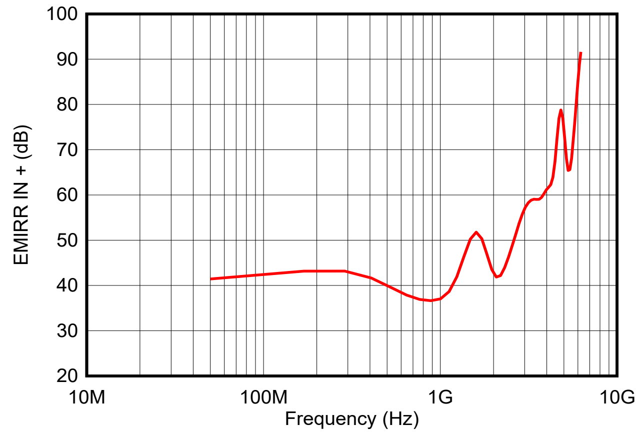


図 7-22. Electromagnetic Interference Rejection Ratio Referred to Noninverting Input (EMIRR+) vs Frequency

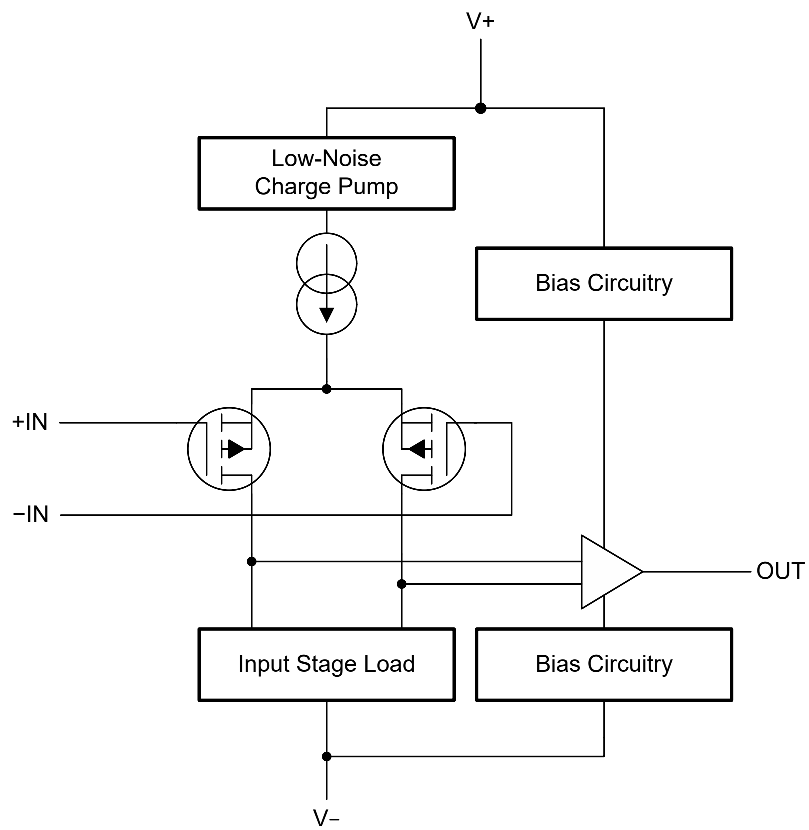
8 Detailed Description

8.1 Overview

The TLVx365 series of operational amplifiers feature rail-to-rail input and output, wide-bandwidth making these devices an excellent choice for driving ADCs. Other typical applications include signal conditioning, low-side current sensing, signal buffering and sensor amplification. The TLVx365 operates with either a single supply or dual supplies.

Furthermore, the TLVx365 amplifier parameters are fully specified from 2.2 V to 5.5 V. Many of the specifications apply from −40°C to +125°C.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Rail-to-Rail Input

The TLVx365 product family features true rail-to-rail input operation, with supply voltages as low as ±1.1 V (2.2 V). A unique zerø-crossover input topology eliminates the input offset transition region typical of many rail-to-rail, complementary stage operational amplifiers. As shown in 図 8-1, this topology also allows the TLVx365 to provide excellent common-mode performance over the entire input range, which extends 100 mV beyond both power-supply rails. When driving ADCs, the highly linear V_{CM} range of the TLVx365 makes sure that the system linearity performance is not compromised. For a simplified schematic illustrating the rail-to-rail input circuitry, see セクション 8.2.

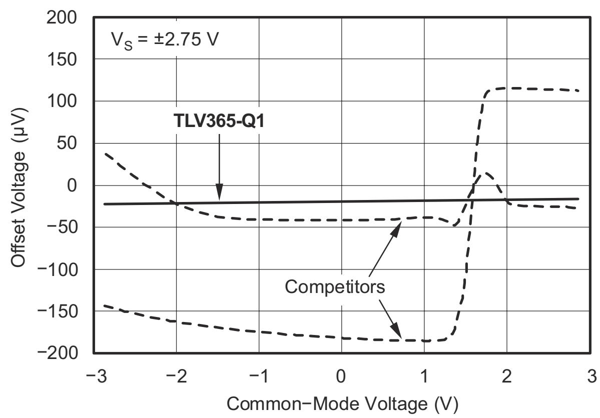


図 8-1. TLVx365 Linear Offset Over the Entire Common-Mode Range

8.3.2 Input and ESD Protection

図 8-2 shows that the TLVx365 incorporates internal electrostatic discharge (ESD) protection circuits on all pins. In the case of input and output pins, this protection primarily consists of current-steering diodes connected between the input and power-supply pins. These ESD protection diodes also provide in-circuit, input overdrive protection if the current is limited to 10 mA; see also セクション 7.1. 図 8-3 shows how a series input resistor can be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input; the resistor must be kept to the minimum value in noise-sensitive applications.

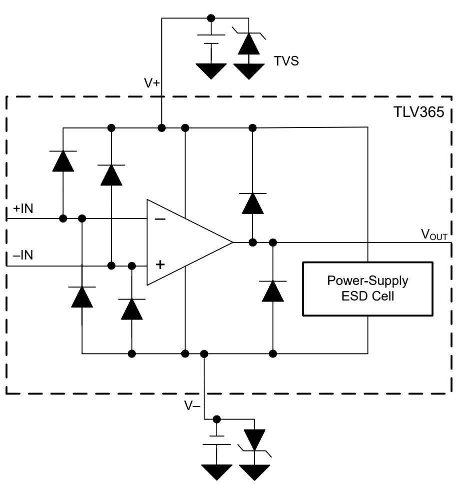


図 8-2. ESD Protection Scheme

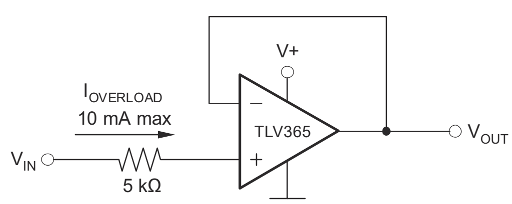


図 8-3. Input Current Protection

8.3.3 Driving Capacitive Loads

The TLVx365 can be used in applications where driving a capacitive load is required. An op amp in a unity-gain, buffer configuration and driving a capacitive load exhibits a greater tendency to be unstable than an amplifier operated at a higher gain. The capacitive load, in conjunction with the op-amp output impedance, creates a pole within the feedback loop that degrades the phase margin. The degradation of the phase margin increases as the capacitive loading increases.

図 8-4 shows one technique to increase the capacitive-load drive capability of the amplifier operating in unity gain is to insert a small resistor, R_{ISO}, in series with the output. This resistor significantly reduces the overshoot and ringing associated with capacitive loads.

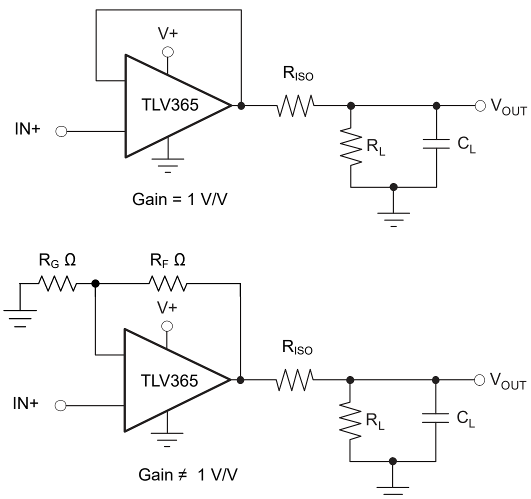
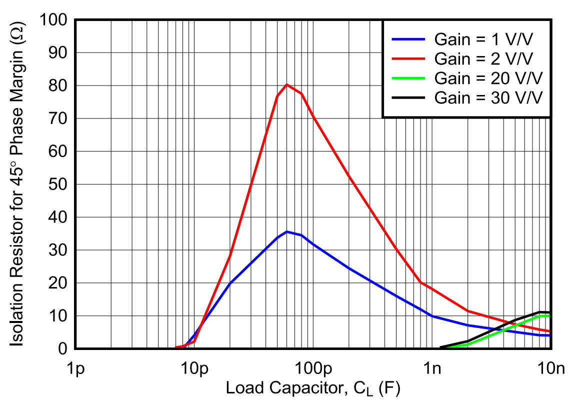


図 8-4. Improving Capacitive Load Drive

A possible drawback of this technique is the voltage divider created with the added series resistor (R_{ISO}) and any resistor (R_L) connected in parallel with the capacitive load. The voltage divider introduces a gain error at the output that also reduces the output swing. The error contributed by the voltage divider can be insignificant. For instance, with a load resistance of R_L = 10 kΩ and R_{ISO} = 20 Ω, the gain error is only approximately 0.2%.

図 8-5 shows the recommended isolation resistor (R_{ISO}) to be connected at the output of TLVx365 for different capacitive loads. The TLVx365 can drive higher capacitive loads without the need of isolation resistors at higher gains.



For gain > 1 V/V, R_F = 1 kΩ

For gain = 1 V/V, R_F = 0 Ω

図 8-5. Recommended Isolation Resistor vs Capacitive Load

8.3.4 Active Filter

The TLVx365 is an excellent choice for active filter applications requiring a wide bandwidth, fast slew rate, low-noise, single-supply operational amplifier. 図 8-6 shows a 500-kHz, second-order, low-pass filter using a multiple-feedback (MFB) topology. The components have been selected to provide a maximally-flat Butterworth response. Beyond the cutoff frequency, rolloff is −40 dB/dec. The Butterworth response is designed for applications requiring predictable gain characteristics, such as the antialiasing filter used ahead of an ADC.

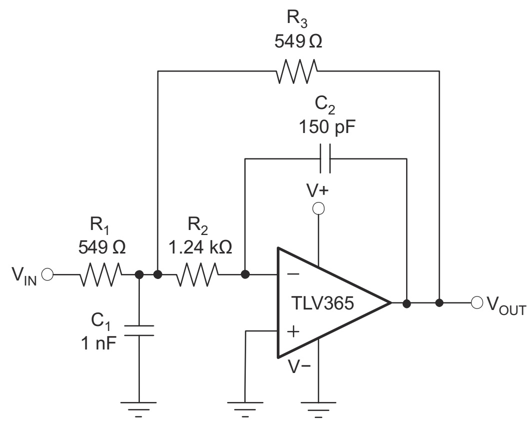


図 8-6. Second-Order Butterworth, 500-kHz Low-Pass Filter

When considering the MFB filter, the output is inverted, relative to the input. If this inversion is not desired, then a noninverting output can be achieved through one of these options:

- add an inverting amplifier
- add an additional second-order MFB stage
- use a noninverting filter topology, such as the Sallen-Key

図 8-7 shows the Sallen-Key topology.

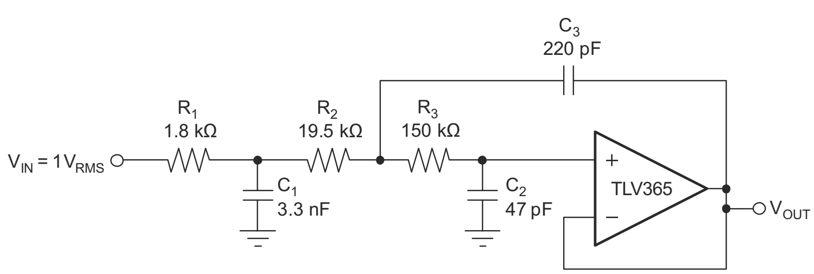


図 8-7. Configured as a Three-Pole, 20-kHz, Sallen-Key Filter

8.4 Device Functional Modes

The device has one mode of operation that applies when operated within the recommended operating conditions.

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TLVx365 offer outstanding dc and ac performance. These devices operate with up to a 5.5-V power supply, offer an ultra-low input bias current and a 50-MHz bandwidth with true rail-to-rail input capability.

9.1.1 Overdrive Recovery Performance

The TLVx365 family exhibits excellent overdrive recovery when the output is driven well beyond the V+ or V– supplies. When configured in a low-side current-sensing configuration (as in 図 9-1), the output of the op amp (TLVx365) is often driven to or less than ground as a result of ground bounce at the power ground or the ≤ 0-A current being measured across shunt resistance R_{SH}. The TLVx365 has the ability to recover from an overdrive event in < 100 ns. 図 9-2 shows the comparison of the overdrive recovery performance of TLVx365 and other popular op amps in the same category.

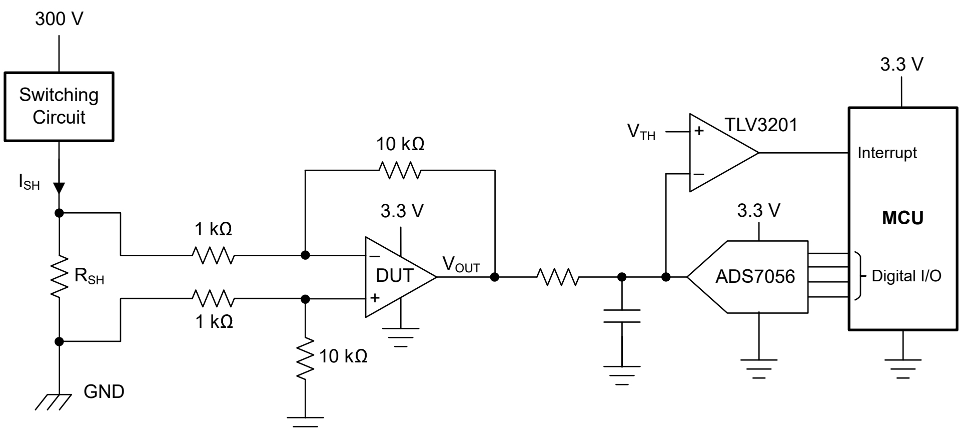
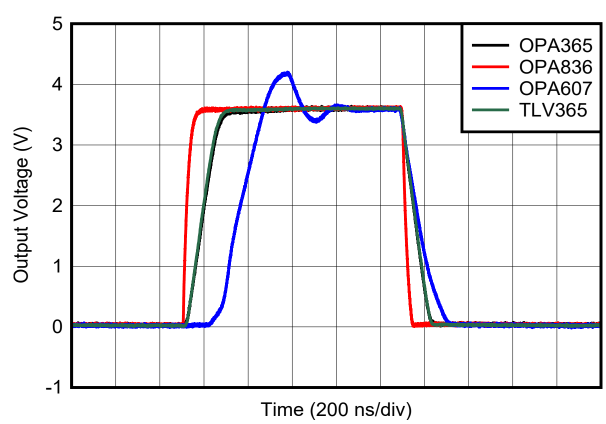


図 9-1. Low Side Current Sensing Application Circuit



Gain = 10 V/V. V_{OUT} driven to (V–) – 1 V

図 9-2. TLVx365 Overdrive Recovery

9.1.2 Achieving an Output Level of Zero Volts

Certain single-supply applications require the op-amp output to swing from 0 V to a positive full-scale voltage and have high accuracy. An example is an op amp employed to drive a single-supply ADC having an input range from 0 V to 3.3 V. Rail-to-rail output amplifiers with very light output loading can achieve an output level within few millivolts of 0 V (or V+ at the high end), but not true 0 V. Furthermore, the deviation from 0 V only becomes greater as the required load current increases. This increased deviation is a result of limitations of the CMOS output stage.

When a pulldown resistor is connected from the amplifier output to a negative voltage source, the TLVx365 can achieve an output level of 0 V, and even a few millivolts below 0 V. 図 9-3 shows a circuit using this technique.

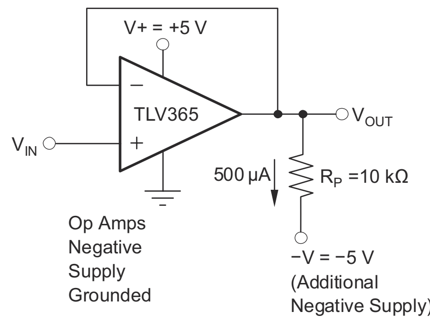


図 9-3. Swing-to-Ground

A pulldown current of approximately 500 µA is required when TLVx365 is connected as a unity-gain buffer. Pulldown resistor R_L is calculated from $R_L = [(V_O - V_{NEG}) / (500\ \mu A)]$.

図 9-4 shows the offset voltage vs output swing.

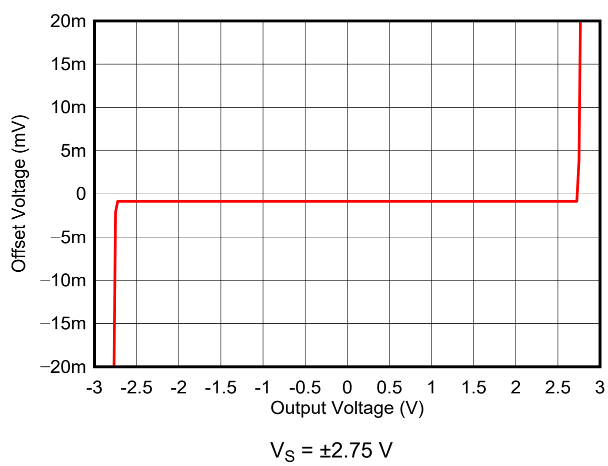


図 9-4. Offset Voltage vs Output Swing

9.2 Typical Applications

9.2.1 Second-Order Low-Pass Filter

Low-pass filters are commonly employed in signal processing applications to reduce noise and prevent aliasing. The TLVx365 is designed to construct high-speed, high-precision active filters. 図 9-5 shows a second-order low-pass filter commonly encountered in signal processing applications.

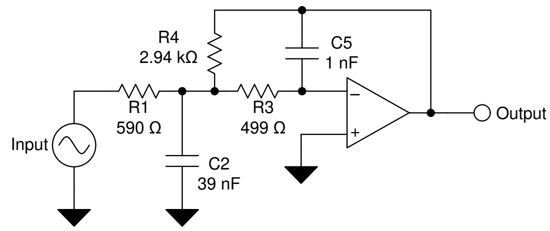


図 9-5. Second-Order Low-Pass Filter

9.2.1.1 Design Requirements

Use the following parameters for this design example:

- Gain = 5 V/V (inverting gain)
- Low-pass cutoff frequency = 25 kHz
- Second-order, Chebyshev filter response with 3-dB gain peaking in the pass band

9.2.1.2 Detailed Design Procedure

図 9-5 shows the infinite-gain, multiple-feedback circuit for a low-pass network function. Use 式 1 to calculate the voltage transfer function.

$$\frac{\text{Output}}{\text{Input}}(s) = \frac{-1/R_1R_3C_2C_5}{s^2 + (s/C_2)(1/R_1 + 1/R_3 + 1/R_4) + 1/R_3R_4C_2C_5} \tag{1}$$

This circuit produces a signal inversion. For this circuit, use 式 2 to calculate the gain at dc and the low-pass cutoff frequency.

$$\text{Gain} = \frac{R_4}{R_1}$$

$$f_C = \frac{1}{2\pi}\sqrt{(1/R_3R_4C_2C_5)} \tag{2}$$

9.2.1.3 Application Curve

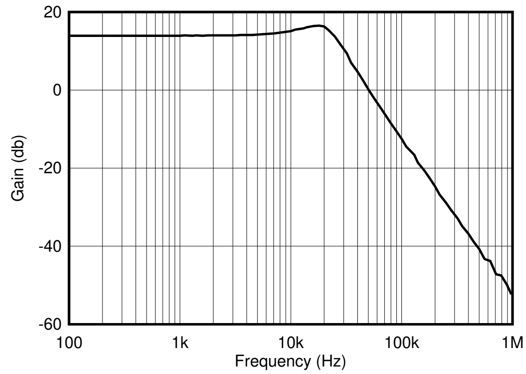


図 9-6. TLVx365 Second-Order 25 kHz, Chebyshev, Low-Pass Filter

9.2.2 ADC Driver and Reference Buffer

図 9-7 shows the use of a TLVx365 op amp as a SAR ADC input and reference pin driver. Sensors, which are used for interfacing with the physical environment, exhibit high output impedance and cannot drive SAR ADC inputs directly. The TLVx365 devices exhibit a very low-input bias current of 20 pA (maximum), and therefore do not load these high-output impedance sensors. A wide-GBW amplifier connected to the output of these sensors is needed to charge the switching capacitors at the SAR ADC input and to settle fast, to the required accuracy, within the given acquisition time.

The ADC core draws transient current from the reference input during the conversion (digitization) phase, which must be driven with a wide-GBW amplifier to offer fast settling and maintain a stable reference voltage for excellent digitization performance. The TLVx365 reference buffer is used in a composite loop with the OPA378 precision amplifier because of limitations in precision performance of wide-GBW amplifiers. The precision amplifier maintains low-offset output, whereas the TLVx365 provide the output drive and fast-settling performance.

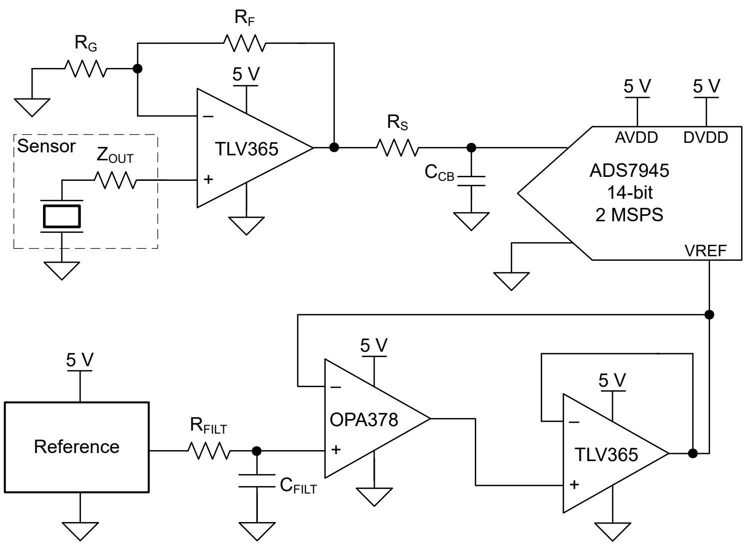


図 9-7. TLVx365 as a SAR ADC Driver

9.3 Power Supply Recommendations

The TLVx365 family is operational when the power-supply voltage is greater than 2.2 V (±1.1 V). The maximum power supply voltage for the TLVx365 family is 5.5 V (±2.75 V). The TLVx365 operate on both single and dual supplies. The maximum permissible voltage, V_S, is 6 V.

9.4 Layout

9.4.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including the following guidelines:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole or through the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-μF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
  - The TLVx365 is capable of peak output current (in excess of 50 mA). Applications with low impedance loads or capacitive loads with fast transient signals demand large currents from the power supplies. Larger bypass capacitors, such as 1-μF solid tantalum capacitors, can improve dynamic performance in these applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. 図 9-8 shows that keeping R_F and R_G close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

9.4.2 Layout Example

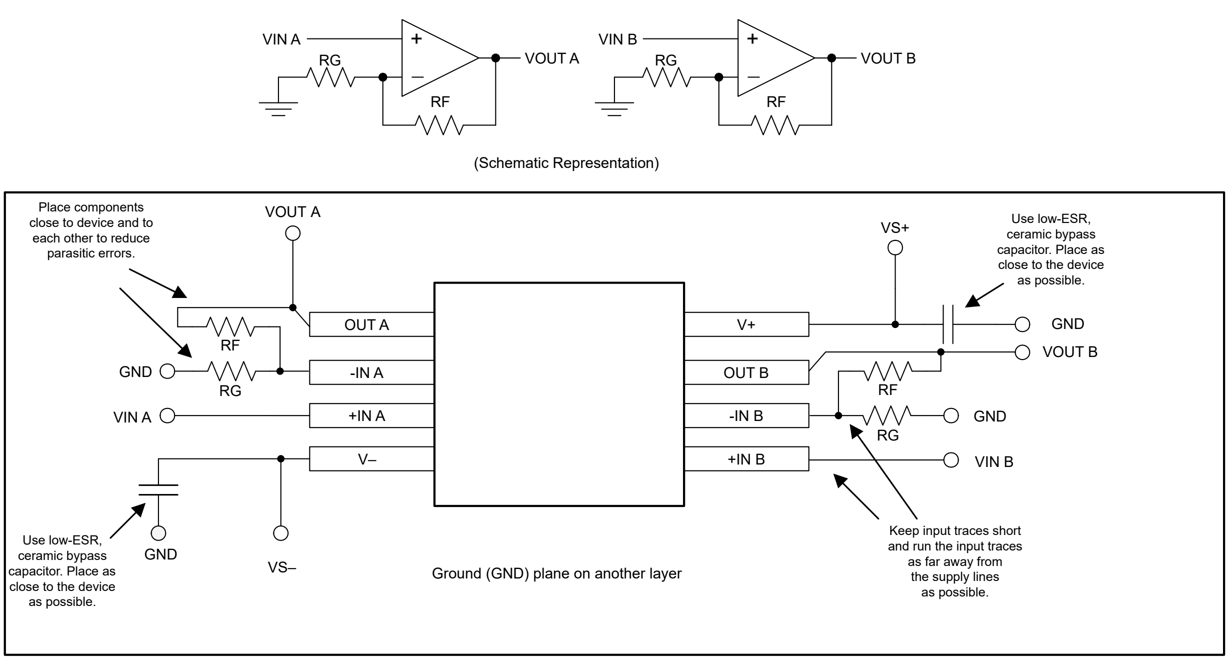


図 9-8. Layout Recommendation for TLV2365 SOIC Package

10 Device and Documentation Support

10.1 Device Support

10.1.1 Development Support

10.1.1.1 PSpice® for TI

PSpice® for TI は、アナログ回路の性能評価に役立つ設計およびシミュレーション環境です。レイアウトと製造に移る前に、サブシステムの設計とプロトタイプ・ソリューションを作成することで、開発コストを削減し、市場投入までの期間を短縮できます。

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TINA-TI™ シミュレーション・ソフトウェアは、SPICE エンジンをベースにした単純かつ強力な、使いやすい回路シミュレーション・プログラムです。TINA-TI シミュレーション・ソフトウェアは、TINA™ ソフトウェアのすべての機能を持つ無償バージョンで、パッシブ・モデルとアクティブ・モデルに加えて、マクロモデルのライブラリがプリロードされています。TINA-TI シミュレーション・ソフトウェアには、SPICE の標準的な DC 解析、過渡解析、周波数ドメイン解析などの全機能に加え、追加の設計機能が搭載されています。

TINA-TI シミュレーション・ソフトウェアは設計ツールとシミュレーション Web ページから無料でダウンロードでき、ユーザーが結果をさまざまな方法でフォーマットできる、広範な後処理機能を備えています。仮想計測器により、入力波形を選択し、回路ノード、電圧、および波形をプローブして、動的なクイック・スタート・ツールを作成できます。

注

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10.1.1.3 DIP アダプタ評価基板

DIP アダプタ評価基板は、オペアンプの迅速なプロトタイプ製作とテストを可能にする評価基板です。小型の表面実装デバイスとのインターフェイスを迅速、容易、低コストで実現します。付属の Samtec 端子ストリップか、直接配線により既存の回路へサポートされているオペアンプを接続します。DIP アダプタ評価基板キットは、以下の業界標準パッケージをサポートしています。D または U (SOIC-8)、PW (TSSOP-8)、DGK (VSSOP-8)、DBV (SOT-23-6、SOT-23-5、および SOT-23-3)、DCK (SC70-6 および SC70-5)、および DRL (SOT563-6)。

10.1.1.4 DIYAMP-EVM

DIYAMP-EVM は、実際のアンプ回路を提供する独自の評価基板 (EVM) であり、設計コンセプトの迅速な評価とシミュレーションの検証を実現します。この評価基板は、3 つの業界標準パッケージ (SC70、SOT23、SOIC) で供給されており、シングル / デュアル電源向けに、アンプ、フィルタ、安定性補償、コンパレータの各構成など、12 の一般的なアンプ構成が可能です。

10.1.1.5 TI のリファレンス・デザイン

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10.1.1.6 フィルタ設計ツール

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10.2 Documentation Support

10.2.1 Related Documentation

The following documents are relevant to using the TLVx365, and recommended for reference. All are available for download at www.ti.com unless otherwise noted.

- Texas Instruments, *FilterPro™ software* user's guide
- Texas Instruments, *Low Power Input and Reference Driver Circuit for ADS8318 and ADS8319* application report
- Texas Instruments, *Op Amp Performance Analysis* application bulletin
- Texas Instruments, *Single-Supply Operation of Operational Amplifiers* application bulletin
- Texas Instruments, *The Best of Baker's Best – Amplifiers eBook* reference book

10.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

10.4 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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10.7 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV2365DR	ACTIVE	SOIC	D	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T2365D	Samples
TLV365DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	T365	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLV365 :

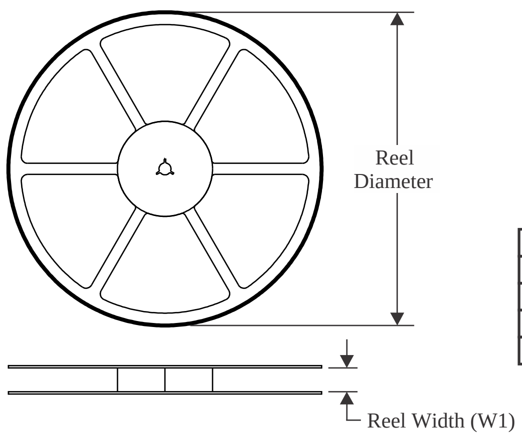
- Automotive : TLV365-Q1

NOTE: Qualified Version Definitions:

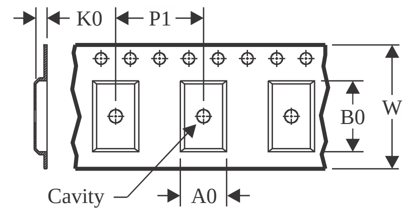
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

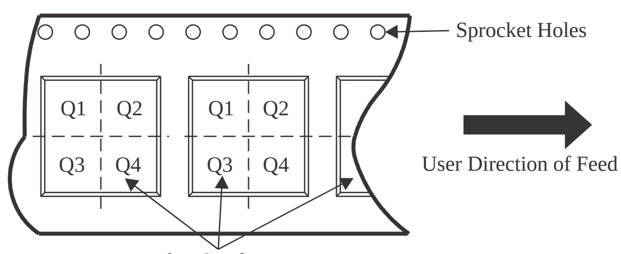


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

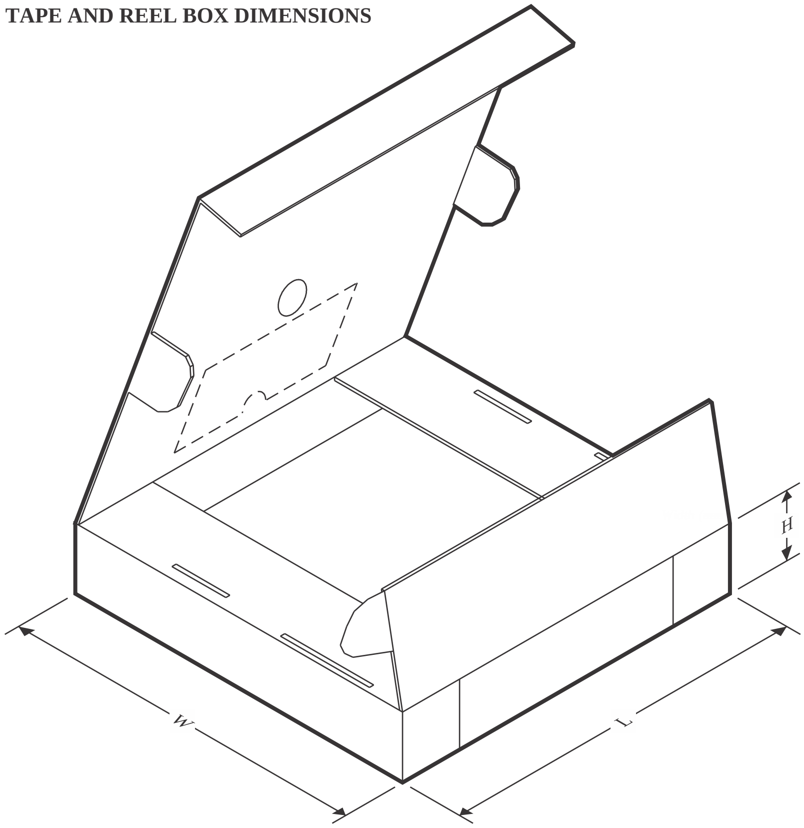
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

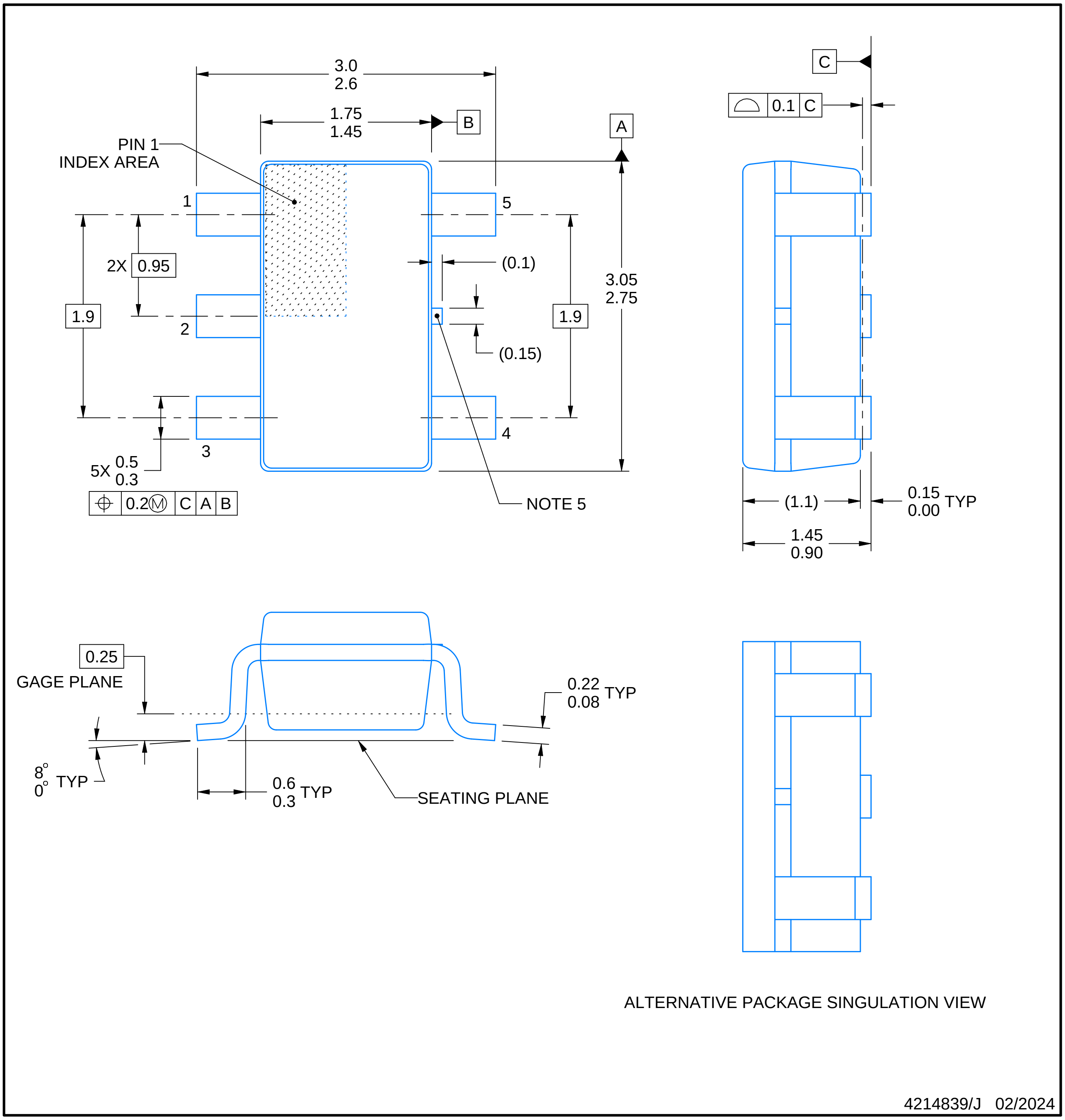
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV2365DR	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV365DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV365DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



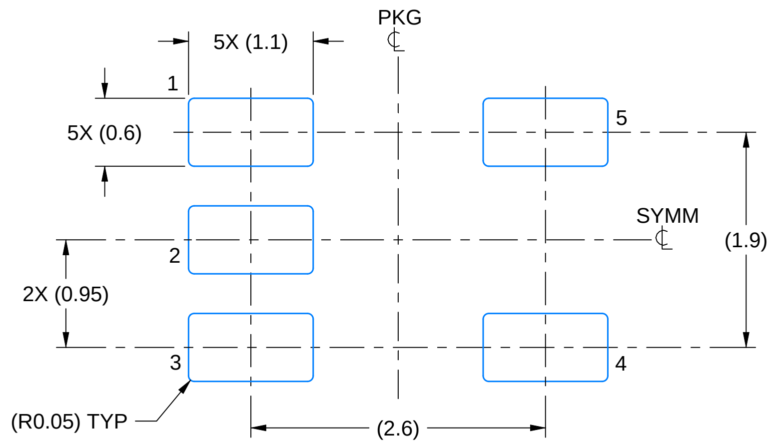
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV2365DR	SOIC	D	8	3000	340.5	338.1	20.6
TLV365DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV365DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0

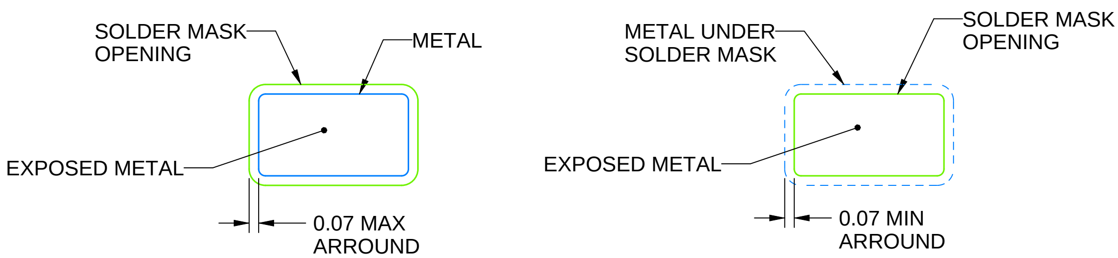


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



NON SOLDER MASK DEFINED (PREFERRED)

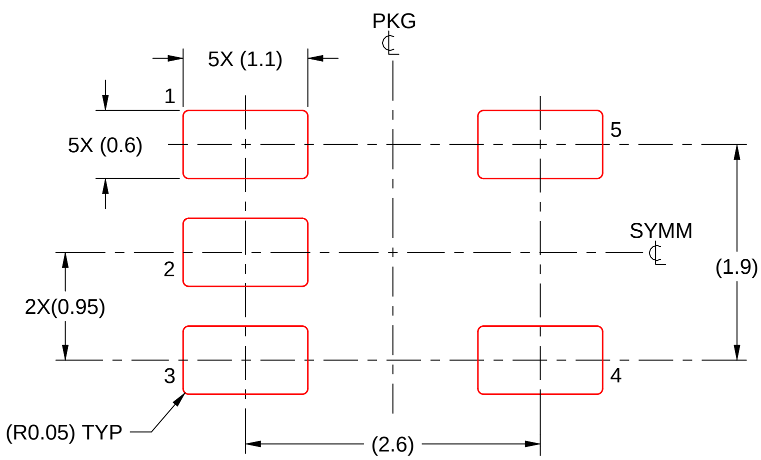
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4214839/J 02/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

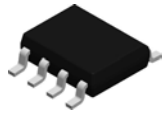


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/J 02/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

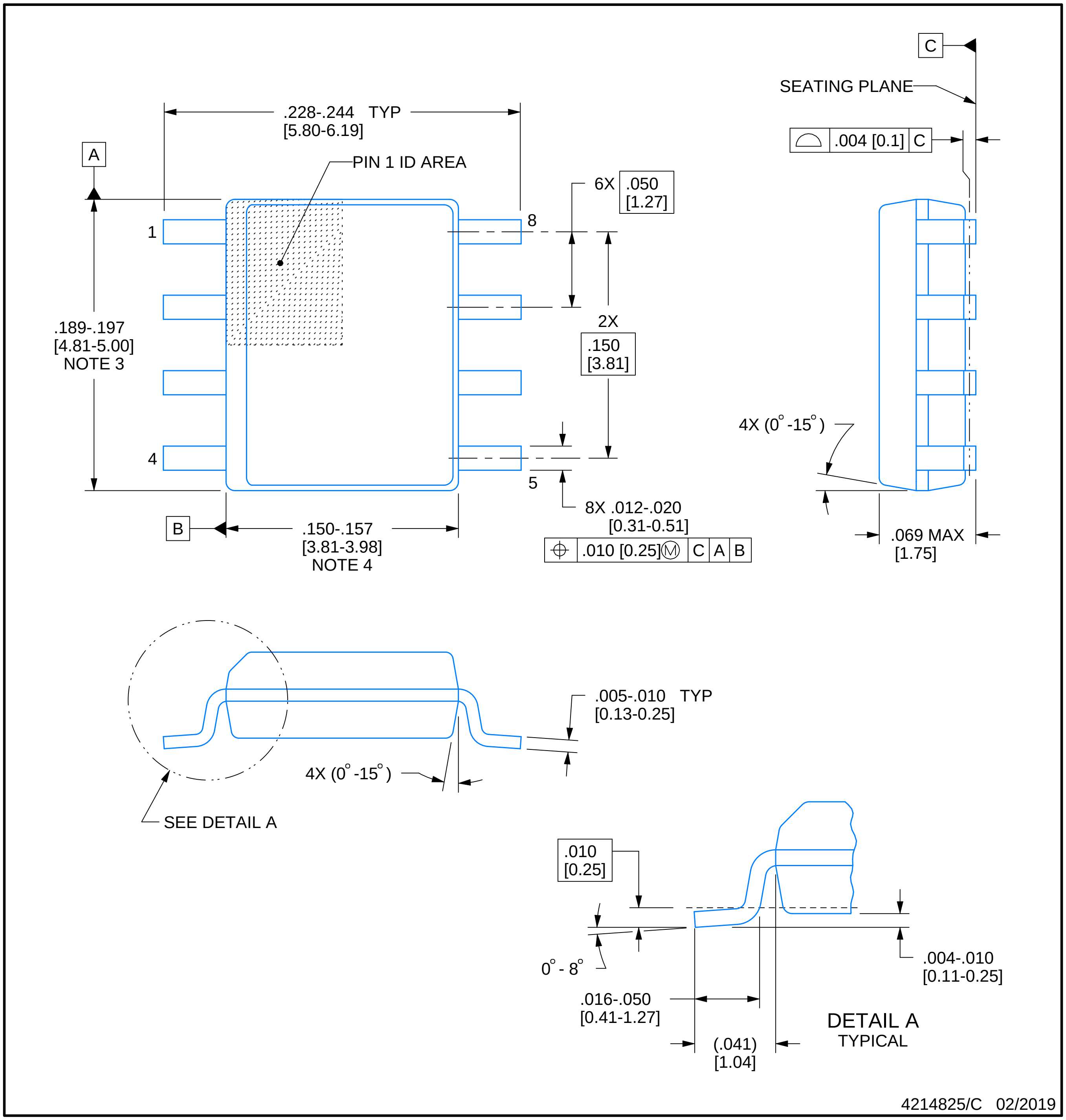


PACKAGE OUTLINE

D0008A

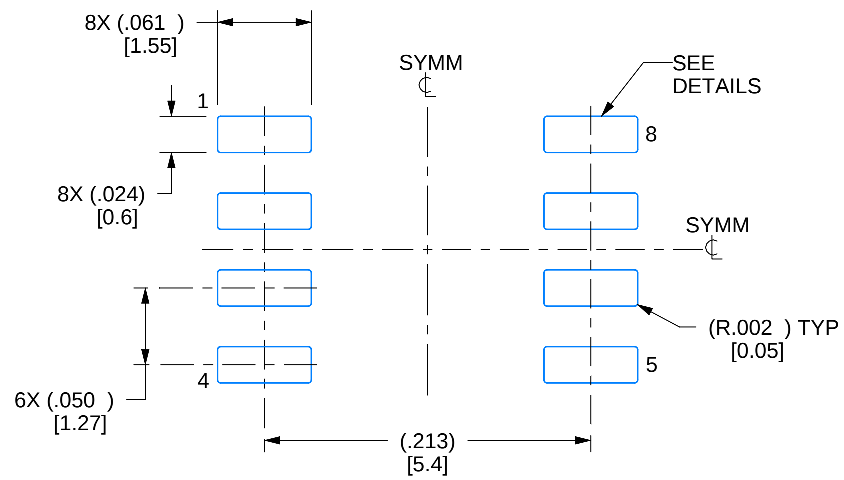
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

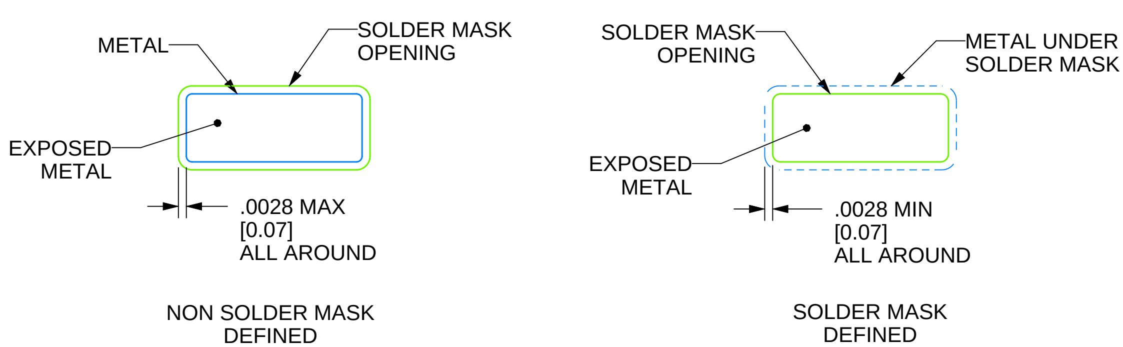


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

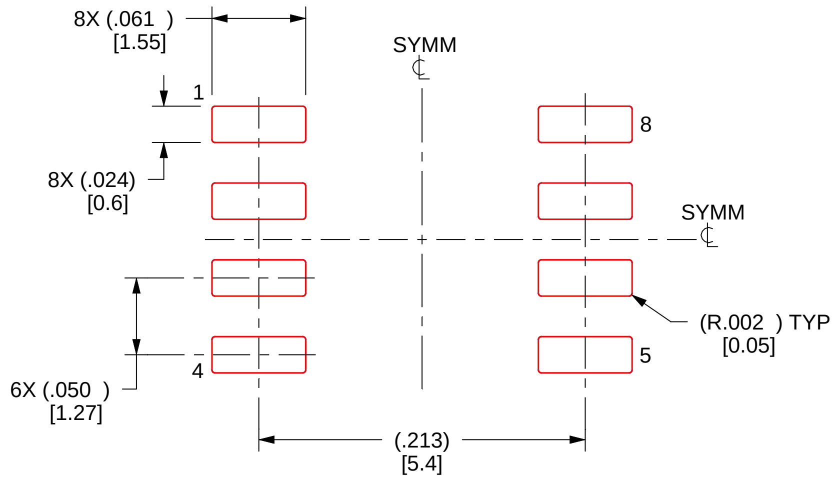


SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

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