TEXAS INSTRUMENTS
TPS65262-1
JAJSQ72B – JUNE 2014 – REVISED MAY 2023

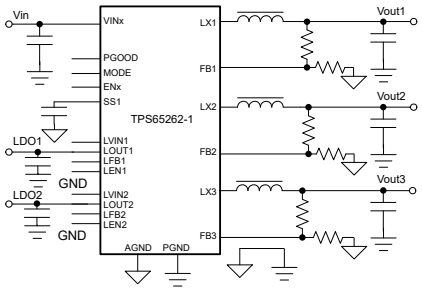
TPS65262-1、入力電圧 4.5V～18V、出力電流 3A/1A/1A、トリプル同期整流降圧型コンバータ、デュアル可変 350mA/150mA LDO 搭載

1 特長

- 動作時入力電圧範囲:4.5～18V
- フィードバック・リファレンス電圧:0.6V±1%
- 最大連続出力電流:3A/1A/1A
- 600kHz の固定スイッチング周波数
- 以下の機能を備えた統合型デュアル LDO:
  - 入力電圧範囲:1.3V～5.5V
  - 連続出力電流:350mA/150mA
- Buck1 のソフトスタート時間をプログラム可能
- Buck2 と Buck3 のソフトスタート時間は 1ms 固定
- Buck2 と Buck3 のループ補償を内蔵
- 各降圧に専用のイネーブル・ピン
- 自動パワーアップ / パワーダウン・シーケンス
- 軽負荷時のパルス・スキップ・モード (PSM)
- 出力電圧パワー・グッド・インジケータ
- 過熱保護

2 アプリケーション

- DTV
- セット・トップ・ボックス
- ホーム・ゲートウェイおよびアクセス・ポイント・ネットワーク
- ワイヤレス・ルータ
- 監視機器
- POS 機器



代表的なアプリケーション

3 概要

TPS65262-1 は、出力電流 3A/1A/1A のモノリシック・トリプル同期降圧型 (バック) コンバータです。4.5V～18V の幅広い入力電源電圧範囲をサポートしており、5V、9V、12V、または 15V のようなほとんどの中間バス電圧入力に対応できます。コンバータは定周波数ピーク電流モードを備え、アプリケーションを単純化しながら、目的のアプリケーションに合わせてシステムを最適化できるよう設計されています。このデバイスは、600kHz の固定スイッチング周波数で動作します。外付け部品数を低減するため、Buck2 と Buck3 のループ補償を内蔵しています。Buck1 と Buck2/Buck3 は位相差 180°で動作するため (Buck2 と Buck3 は同相動作)、入力フィルタの要件が最小化されます。軽負荷時には、デバイスは自動的にパルス・スキップ・モード (PSM) で動作し、スイッチング損失を低減することで高い効率を実現します。

TPS65262-1 は、2 つの低ドロップアウト電圧リニア・レギュレータ (LDO) を内蔵しています。これらの LDO は入力電圧範囲が 1.3～5.5V、連続出力電流が 350/150mA であり、独立したイネーブルを備え、出力電圧は可変です。

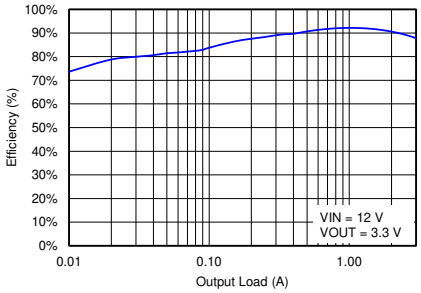
TPS65262-1 には、MODE ピンを High に駆動し、EN1、EN2、EN3 ピンを設定する自動パワー・シーケンスが搭載されています。

本デバイスには、過電圧、過電流、短絡、過熱保護が搭載されています。いずれかの降圧出力電圧がレギュレーション範囲を外れると、パワー・グッド・ピンがアサートされます。

パッケージ情報 (1)

部品番号	パッケージ	本体サイズ (公称)
TPS65262-1	RHB (VQFN、32)	5.00mm × 5.00mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。



効率と出力負荷との関係

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

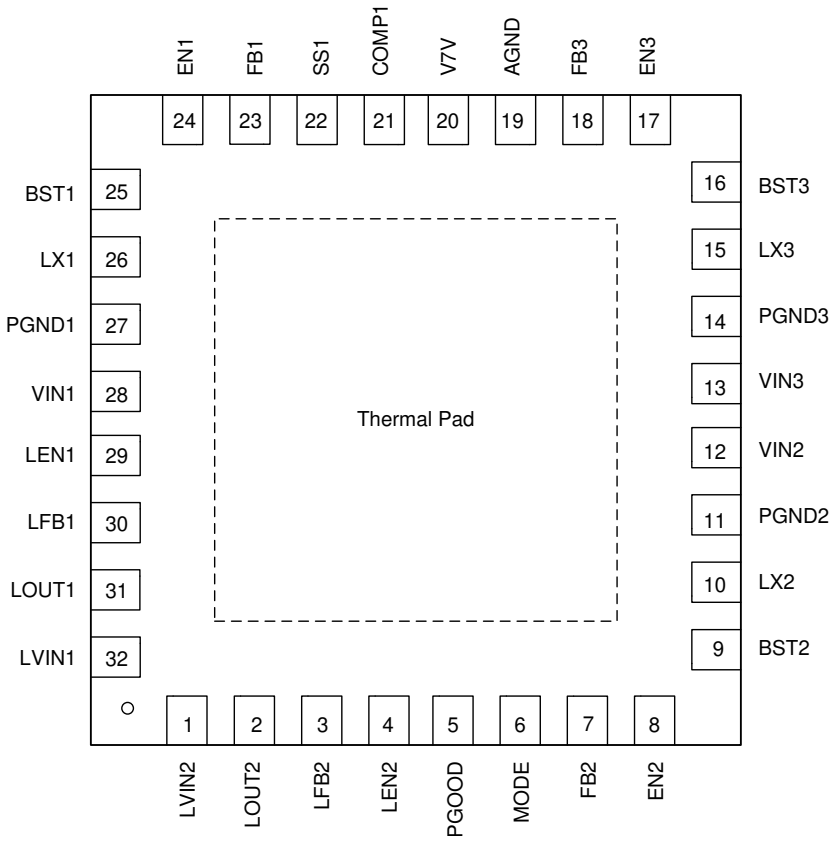
Changes from Revision A (October 2014) to Revision B (May 2023)	Page
• ドキュメント全体にわたって表、図、相互参照の採番方法を更新	1
• ドキュメント全体にわたって画像の色を除去	1
• Changed the description of V7V pin in the *Pin Functions* table	4
• Moved the storage temperature row in the *ESD Ratings* table to the *Absolute Maximum Ratings* table	6
• Renamed the *ESD Ratings* table	6
• Changed the recommended value of capacitor from V7V pin to power ground in *V7V Low Dropout Regulator and Bootstrap*	20
• Changed the recommended value of C8 in the Typical Application Schematic	25

Changes from Revision * (June 2014) to Revision A (October 2014)	Page
• デバイスのステータスを「量産データ」に変更	1

5 Device Comparison Table

PART NUMBER	DESCRIPTION	COMMENTS
TPS65261/-1	4.5 to 18 V, triple buck with input voltage power failure indicator	Triple buck 3-A/2-A/2-A output current, features an open-drain RESET signal to monitor input power failure, automatic power sequencing
TPS65262	4.5 to 18 V, triple buck with dual adjustable LDOs	Triple buck 3-A/1-A/1-A output current, automatic power sequencing. Dual LDOs 200 mA/100 mA
TPS65263	4.5 to 18 V, triple buck with I^2C interface	Triple buck 3-A/2-A/2-A output current, I^2C controlled dynamic voltage scaling (DVS)
TPS65287	4.5 to 18 V, triple buck with power switch and push button control	Triple buck 3-A/2-A/2-A output current, up to 2.1-A USB power with overcurrent setting by external resistor, push-button control for intelligent system power-on and power-off operation
TPS65288	4.5 to 18 V, triple buck with dual power switches	Triple buck 3-A/2-A/2-A output current, two USB power switches current limiting at typical 1.2 A (0.8, 1.0, 1.4, 1.6, 1.8, 2.0, and 2.2 A available with manufacture trim options)

6 Pin Configuration and Functions



(There is no electric signal down bonded to thermal pad inside IC. Exposed thermal pad must be soldered to PCB for optimal thermal performance.)

図 6-1. RHB Package 32 Pins (Top View)

表 6-1. Pin Functions

PIN		DESCRIPTION
NAME	NO.	
LVIN2	1	Input power supply for LDO2. Connect LVIN2 pin as close as possible to the (+) terminal of an input ceramic capacitor (suggest 1 µF).
LOUT2	2	LDO2 output. Connect LOUT2 pin as close as possible to the (+) terminal of an output ceramic capacitor (suggest 1 µF).
LFB2	3	Feedback Kelvin sensing pin for LDO2 output voltage. Connect this pin to LDO2 resistor divider.
LEN2	4	Enable for LDO2. Float to enable.
PGOOD	5	An open-drain output, asserts low if the output voltage of any buck is beyond regulation range due to thermal shutdown, overcurrent, undervoltage, or ENx shut down.
MODE	6	When high, an automatic power-up or power-down sequence is provided according to the states of EN1, EN2, and EN3 pins.
FB2	7	Feedback Kelvin sensing pin for buck2 output voltage. Connect this pin to buck2 resistor divider.
EN2	8	Enable for buck2. Float to enable. Can use this pin to adjust the input undervoltage lockout of buck2 with a resistor divider.
BST2	9	Boot-strapped supply to the high-side floating gate driver in buck2. Connect a capacitor (recommend 47 nF) from BST2 pin to LX2 pin.
LX2	10	Switching node connection to the inductor and bootstrap capacitor for buck2. The voltage swing at this pin is from a diode voltage below the ground up to VIN2 voltage.

表 6-1. Pin Functions (continued)

PIN		DESCRIPTION
NAME	NO.	
PGND2	11	Power ground connection of buck2. Connect PGND2 pin as close as possible to the (–) terminal of VIN2 input ceramic capacitor.
VIN2	12	Input power supply for buck2. Connect VIN2 pin as close as possible to the (+) terminal of an input ceramic capacitor (suggest 10 µF).
VIN3	13	Input power supply for buck3. Connect VIN3 pin as close as possible to the (+) terminal of an input ceramic capacitor (suggest 10 µF).
PGND3	14	Power ground connection of buck3. Connect PGND3 pin as close as possible to the (–) terminal of VIN3 input ceramic capacitor.
LX3	15	Switching node connection to the inductor and bootstrap capacitor for buck3. The voltage swing at this pin is from a diode voltage below the ground up to VIN3 voltage.
BST3	16	Boot-strapped supply to the high-side floating gate driver in buck3. Connect a capacitor (recommend 47 nF) from BST3 pin to LX3 pin.
EN3	17	Enable for buck3. Float to enable. Can use this pin to adjust the input undervoltage lockout of buck3 with a resistor divider.
FB3	18	Feedback Kelvin sensing pin for buck3 output voltage. Connect this pin to buck3 resistor divider.
AGND	19	Analog ground common to buck controllers and other analog circuits. It must be routed separately from high-current power grounds to the (–) terminal of the bypass capacitor of input voltage VIN.
V7V	20	Internal LDO for gate driver and internal controller. Connect a 10-µF capacitor from the pin to power ground.
COMP1	21	Error amplifier output and loop compensation pin for buck1. Connect a series resistor and capacitor to compensate the control loop of buck1 with peak current PWM mode.
SS1	22	Soft-start and tracking input for buck1. An internal 5-µA pullup current source is connected to this pin. The soft-start time can be programmed by connecting a capacitor between this pin and ground.
FB1	23	Feedback Kelvin sensing pin for buck1 output voltage. Connect this pin to buck1 resistor divider.
EN1	24	Enable for buck1. Float to enable. Can use this pin to adjust the input undervoltage lockout of buck1 with a resistor divider.
BST1	25	Boot-strapped supply to the high side floating gate driver in buck1. Connect a capacitor (recommend 47 nF) from BST1 pin to LX1 pin.
LX1	26	Switching node connection to the inductor and bootstrap capacitor for buck1. The voltage swing at this pin is from a diode voltage below the ground up to VIN1 voltage.
PGND1	27	Power ground connection of Buck1. Connect PGND1 pin as close as possible to the (–) terminal of VIN1 input ceramic capacitor.
VIN1	28	Input power supply for buck1. Connect VIN1 pin as close as possible to the (+) terminal of an input ceramic capacitor (suggest 10 µF).
LEN1	29	Enable for LDO1. Float to enable.
LFB1	30	Feedback Kelvin sensing pin for LDO1 output voltage. Connect this pin to LDO1 resistor divider.
LOUT1	31	LDO1 output. Connect LOUT1 pin as close as possible to the (+) terminal of an output ceramic capacitor (suggest 1 µF).
LVIN1	32	Input power supply for LDO1. Connect LVIN1 pin as close as possible to the (+) terminal of an input ceramic capacitor (suggest 1 µF).
PAD	—	There is no electric signal down bonded to thermal pad inside IC. Exposed thermal pad must be soldered to PCB for optimal thermal performance.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted) (1)

		MIN	MAX	UNIT
Voltage	VIN1, VIN2, VIN3	–0.3	20	V
	LX1, LX2, LX3 (maximum withstand voltage transient <20 ns)	–1	20	
	BST1, BST2, BST3 referenced to LX1, LX2, LX3 pins respectively	–0.3	7	
	MODE, LEN1, LEN2, EN1, EN2, EN3, PGOOD, V7V	–0.3	7	
	LOUT1, LOUT2, LVIN1, LVIN2	–0.3	7	
	FB1, FB2, FB3, LFB1, LFB2, COMP1 , SS1	–0.3	3.6	
	AGND, PGND1, PGND2, PGND3	–0.3	0.3	
T_J	Operating junction temperature	–40	125	°C
T_{stg}	Storage temperature range	-55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			MIN	MAX	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	–2000	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	–500	500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Voltage	VIN1, VIN2, VIN3	4.5	18	V
	LX1, LX2, LX3 (maximum withstand voltage transient <20 ns)	–0.8	18	
	BST1, BST2, BST3 referenced to LX1, LX2, LX3 pins respectively	–0.1	6.8	
	MODE, LEN1, LEN2, EN1, EN2, EN3, PGOOD, V7V	–0.1	6.3	
	FB1, FB2, FB3, LFB1, LFB2, COMP1 , SS1	–0.1	3	
	LOUT1, LOUT2, LVIN1, LVIN2	–0.1	5.5	
T_A	Operating ambient temperature	–40	85	°C
T_J	Operating junction temperature	–40	125	°C

7.4 Thermal Information

THERMAL METRIC[1]		TPS65262-1	UNIT
		RHB (32 PINS)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	32.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	24.2	
$R_{\theta JB}$	Junction-to-board thermal resistance	6.4	
ψ_{JT}	Junction-to-top characterization parameter	0.2	
ψ_{JB}	Junction-to-board characterization parameter	6.4	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.3	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

T_A = 25°C, V_{IN} = 12 V, F_{SW} = 600 kHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY VOLTAGE						
VIN	Input voltage range		4.5		18	V
UVLO	VIN undervoltage lockout	VIN rising	4	4.25	4.5	V
		VIN falling	3.5	3.75	4	V
		Hysteresis		500		mV
IDD_{SDN}	Shutdown supply current	EN1 = EN2 = EN3 = MODE = LEN1 = LEN2 = 0 V		12		µA
IDD_{Q_NSW}	Input quiescent current without buck1, buck2, buck3 switching	EN1 = EN2 = EN3 = 5 V, FB1 = FB2 = FB3 = 0.8 V, LEN1 = LEN2 = 0		790		µA
IDD_{Q_NSW1}		EN1 = 5 V, EN2 = EN3 = 0 V, FB1 = 0.8 V, LEN1 = LEN2 = 0		340		µA
IDD_{Q_NSW2}		EN2 = 5 V, EN1 = EN3 = 0 V, FB2 = 0.8 V, LEN1 = LEN2 = 0		370		µA
IDD_{Q_NSW3}		EN3 = 5V, EN1 = EN2 = 0 V, FB3 = 0.8 V, LEN1 = LEN2 = 0		370		µA
IDD_{Q_LDO1}	LDO input quiescent current	EN1 = EN2 = EN3 = LEN2 = 0 V, LFB1 = 0.8 V, LEN1 = 5 V		190		µA
IDD_{Q_LDO2}		EN1 = EN2 = EN3 = LEN1 = 0 V, LFB2 = 0.8 V, LEN2 = 5 V		190		µA
V_{7V}	V7V LDO output voltage	V_{7V} load current = 0 A	6	6.3	6.6	V
I_{OCP_V7V}	V7V LDO current limit			175		mA
FEEDBACK VOLTAGE REFERENCE						
V_{FB}	Feedback voltage	V_{COMP} = 1.2 V, T_J = 25°C	0.595	0.6	0.605	V
		V_{COMP} = 1.2 V, T_J = –40°C to 125°C	0.594	0.6	0.606	V
$V_{LINEREG\_BUCK}$	Line regulation-DC(1)	I_{OUT1} = 1.5 A, I_{OUT2} = 1 A, I_{OUT3} = 1 A, 5 V < VINx < 18 V		0.002		%/V
$V_{LOADREG\_BUCK}$	Load regulation-DC(1)	VIN = 12 V, I_{OUTx} = (10–100%) × I_{OUTx_max}		0.02		%/A
BUCK1, BUCK2, BUCK3						
V_{ENXH}	EN1, EN2, EN3 high-level input voltage			1.2	1.26	V
V_{ENXL}	EN1, EN2, EN3 low-level input voltage		1.1	1.15		V
I_{ENX}	EN1, EN2, EN3 pullup current	ENx = 1 V		3.6		µA
		ENx = 1.5 V		6.6		
I_{ENhys}	Hysteresis current			3		µA
I_{SS1}	Buck1 soft-start charging current		4.3	5	6	µA
$T_{SS2/3}$	Buck2, buck3 soft-start time			1		ms
T_{ON_MIN}	Minimum on time			80	100	ns
$G_{m\_EA1/2/3}$	Error amplifier trans-conductance	–2 µA < ICOMPX < 2 µA		300		µs
$G_{m\_PS1/2/3}$	COMP voltage to inductor current G_m (1)	ILX = 0.5 A		7.4		A/V
I_{LIMIT1}	Buck1 peak inductor current limit		4.4	5.1	6.06	A
$I_{LIMITSOURCE1}$	Buck1 low-side source current limit			4.4		A
$I_{LIMITS1}$	Buck1 low-side sink current limit			1.3		A
$I_{LIMIT2/3}$	Buck2, buck3 peak inductor current limit		1.8	2.4	3	A
$I_{LIMITSOURCE2/3}$	Buck2, buck3 low-side source current limit			1.75		A
$I_{LIMITS2/3}$	Buck2, buck3 low-side sink current limit			1		A
T_{Hiccup_wait}	OC wait time(1)			0.5		ms
T_{Hiccup_re}	Hiccup time before restart(1)			14		ms
Rdson_HS1	Buck1 high-side switch resistance	VIN1 = 12 V		100		mΩ
Rdson_LS1	Buck1 low-side switch resistance	VIN1 = 12 V		65		mΩ
Rdson_HS2	Buck2 high-side switch resistance	VIN1 = 12 V		195		mΩ
Rdson_LS2	Buck2 low-side switch resistance	VIN1 = 12 V		145		mΩ
Rdson_HS3	Buck3 high-side switch resistance	VIN1 = 12 V		195		mΩ

7.5 Electrical Characteristics (continued)

T_A = 25°C, V_{IN} = 12 V, F_{SW} = 600 kHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Rdson_LS3	Buck3 low-side switch resistance	VIN1 = 12 V		145		mΩ

7.5 Electrical Characteristics (continued)

T_A = 25°C, V_{IN} = 12 V, F_{SW} = 600 kHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER GOOD, MODE, POWER SEQUENCE						
V_{th_PG}	Feedback voltage threshold	FBx undervoltage falling		92.5		%V_{REF}
		FBx undervoltage rising		95		
		FBx overvoltage rising		107.5		
		FBx overvoltage falling		105		
$T_{DEGLITCH(PG)\_F}$	PGOOD falling edge deglitch time			0.19		ms
$T_{RDEGLITCH(PG)\_R}$	PGOOD rising edge deglitch time			1		ms
I_{PG}	PGOOD pin leakage				0.05	µA
V_{LOW_PG}	PGOOD pin low voltage	I_{SINK} = 1 mA			0.4	V
V_{MODEH}	MODE high-level input voltage			1.2	1.26	V
V_{MODEL}	MODE low-level input voltage		1.1	1.15		V
I_{MODE}	MODE pullup current	MODE = 1 V		3.6		µA
		MODE = 1.5 V		6.6		
Tpsdelay	Delay time between bucks at automatic power sequencing mode(1)	MODE = 1.5 V		1.7		ms
LDO1 AND LDO2						
V_{LENXH}	LEN1, LEN2 high-level input voltage			1.2	1.26	V
V_{LENXL}	LEN1, LEN2 low-level input voltage		1.1	1.15		V
I_{LENX}	LEN1, LEN2 pullup current	LENx = 1 V		3.6		µA
		LENx = 1.5 V		6.6		
VIN_{LDO1}	LDO input voltage range		1.3		5.5	V
$VOUT_{LDO1}$	LDO output voltage range	Load current = 350 mA	1			V
V_{LDOFB1}	LDO voltage reference	Load current = 10 mA	0.594	0.6	0.606	V
I_{max_LDO1}	LDO current limit		350	455	540	mA
$V_{dropout1}$	LDO dropout voltage	I_{OUT} = 20 mA		12		mV
		I_{OUT} = 350 mA		400		mV
$V_{LINEREG\_LDO1}$	LDO line regulation-DC(1)	V_{OUT} = 1.8 V, I_{OUT} = 10 mA, LVIN1 changes from 2 to 5.5 V		0.002		%/V
$V_{LOADREG\_LDO1}$	LDO load regulation-DC(1)	I_{OUT} = 1 to 350 mA, LVIN1 = 5 V		0.2		%/A
$PSRR_{LDO1}$	Ripple rejection(1)	LVIN1 = 5 V, Vout = 1.8 V, I_{OUT} = 10 mA, f = 10 kHz		56		dB
VIN_{LDO2}	LDO input voltage range		1.3		5.5	V
$VOUT_{LDO2}$	LDO output voltage range	Load current = 150 mA	1			V
V_{LDOFB2}	LDO voltage reference	Load current = 10 mA	0.594	0.6	0.606	V
I_{max_LDO2}	LDO current limit		170	220	290	mA
$V_{dropout2}$	LDO dropout voltage(1)	I_{OUT} = 10 mA		12		mV
		I_{OUT} = 150 mA		250		
$V_{LINEREG\_LDO2}$	LDO line regulation-DC(1)	V_{OUT} = 1.8 V, I_{OUT}= 10 mA, LVIN2 changes from 2 to 5.5 V		0.002		%/V
$V_{LOADREG\_LDO2}$	LDO load regulation-DC(1)	I_{OUT} = 1 to 150 mA, LVIN2 = 5 V		0.2		%/A
$PSRR_{LDO2}$	Ripple rejection(1)	LVIN2 = 5 V, Vout = 1.8 V, I_{OUT} = 10 mA, f = 10 kHz		56		dB
OSCILLATOR						
F_{SW}	Switching frequency		570	600	630	kHz
THERMAL PROTECTION						
T_{TRIP_OTP}	Thermal protection trip point(1)	Temperature rising		160		°C
T_{HYST_OTP}		Hysteresis		20		°C

(1) Lab validation result

7.6 Typical Characteristics

T_A = 25°C, VIN = 12 V, V_{OUT1}= 1.2 V, V_{OUT2}= 1.8 V, V_{OUT3}= 3.3 V F_{SW} = 600 kHz (unless otherwise noted)

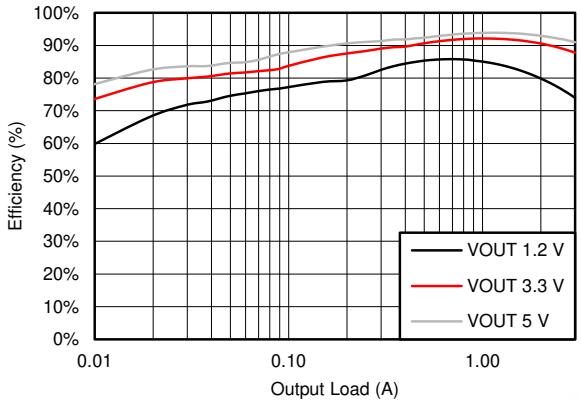


図 7-1. BUCK1 Efficiency

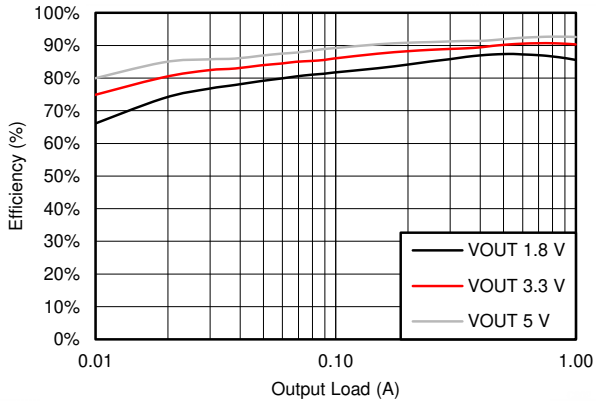


図 7-2. BUCK2 Efficiency

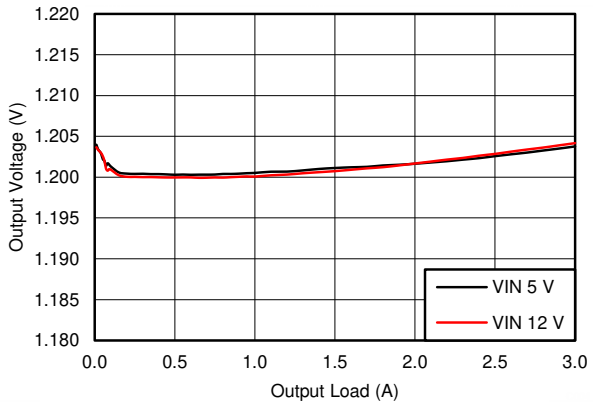


図 7-3. BUCK1, Load Regulation

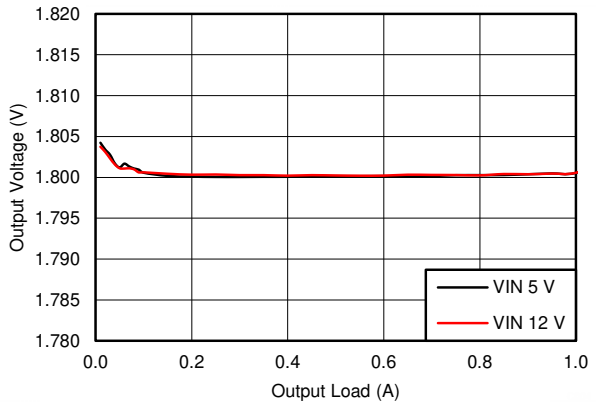


図 7-4. BUCK2, Load Regulation

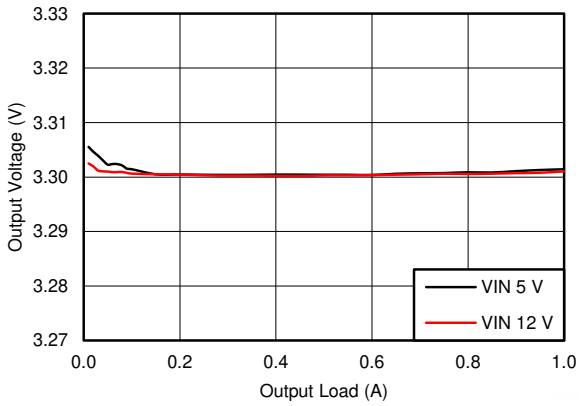


図 7-5. BUCK3, Load Regulation

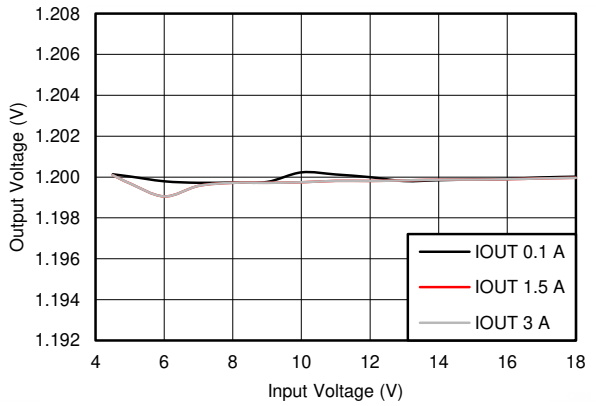


図 7-6. BUCK1, Line Regulation

7.6 Typical Characteristics (continued)

T_A = 25°C, VIN = 12 V, V_{OUT1}= 1.2 V, V_{OUT2}= 1.8 V, V_{OUT3}= 3.3 V F_{SW} = 600 kHz (unless otherwise noted)

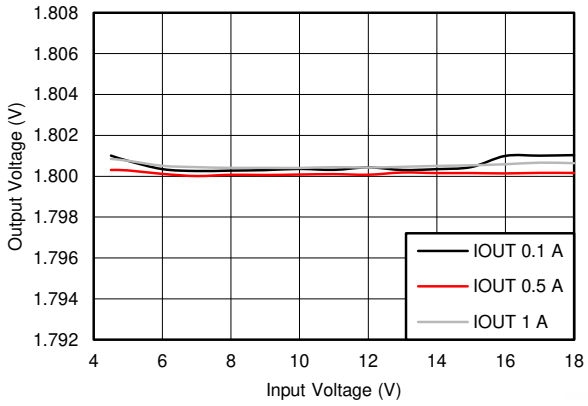


図 7-7. BUCK2, Line Regulation

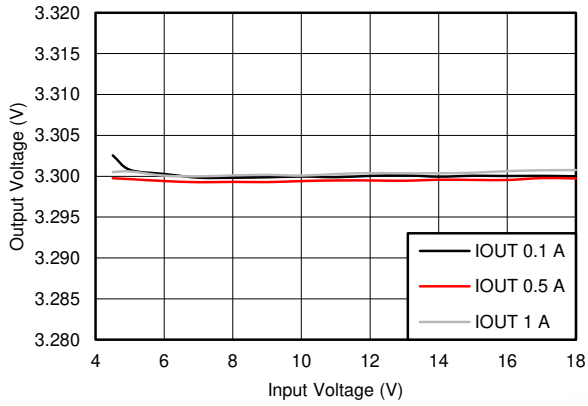


図 7-8. BUCK3, Line Regulation

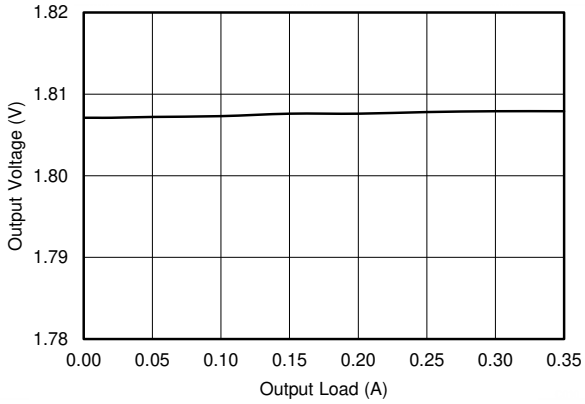


図 7-9. LDO1, Load Regulation

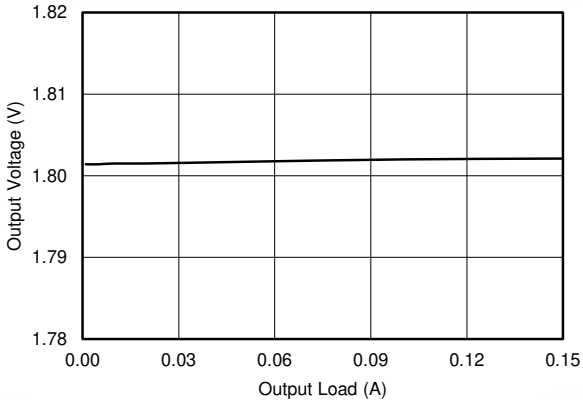


図 7-10. LDO2, Load Regulation

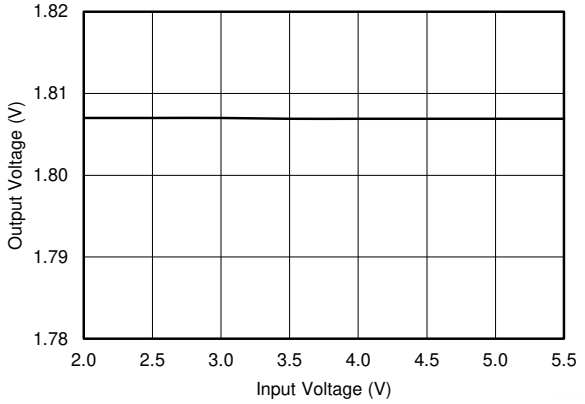


図 7-11. LDO1, Line Regulation

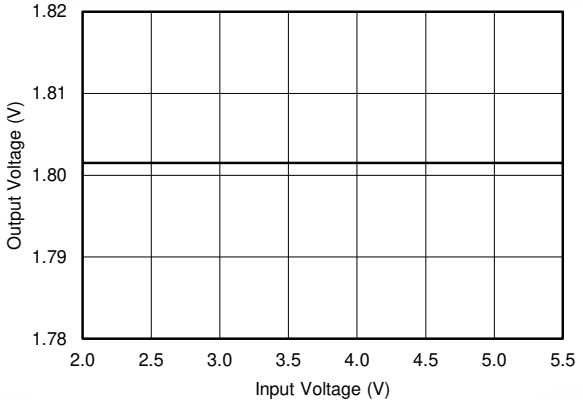


図 7-12. LDO2, Line Regulation

7.6 Typical Characteristics (continued)

T_A = 25°C, VIN = 12 V, V_{OUT1}= 1.2 V, V_{OUT2}= 1.8 V, V_{OUT3}= 3.3 V F_{SW} = 600 kHz (unless otherwise noted)

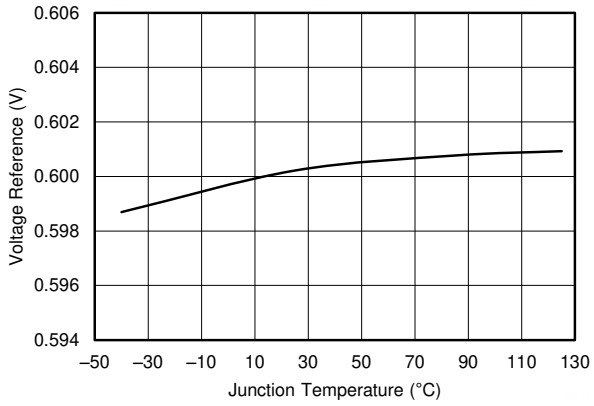


図 7-13. Voltage Reference vs Temperature

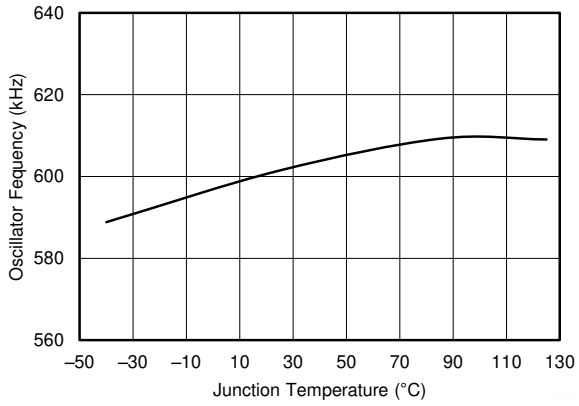


図 7-14. Oscillator Frequency vs Temperature

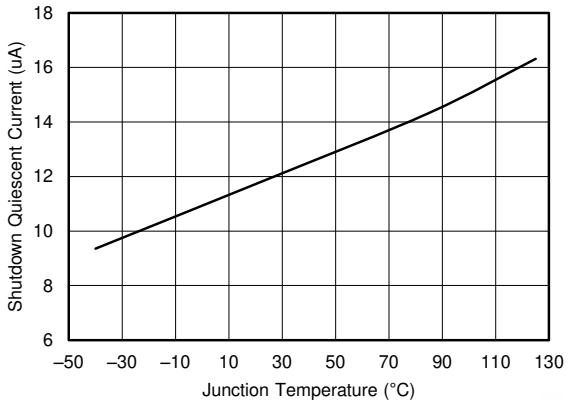


図 7-15. Shutdown Quiescent Current vs Temperature

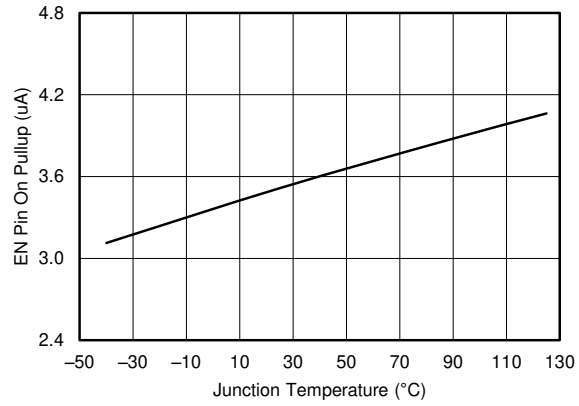


図 7-16. EN Pin Pullup Current vs Temperature, EN = 1 V

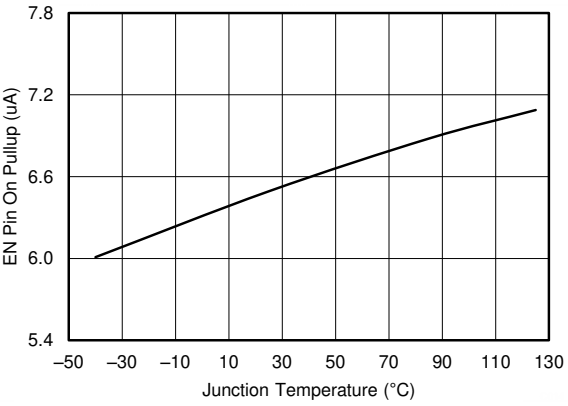


図 7-17. EN Pin Pullup Current vs Temperature, EN = 1.5 V

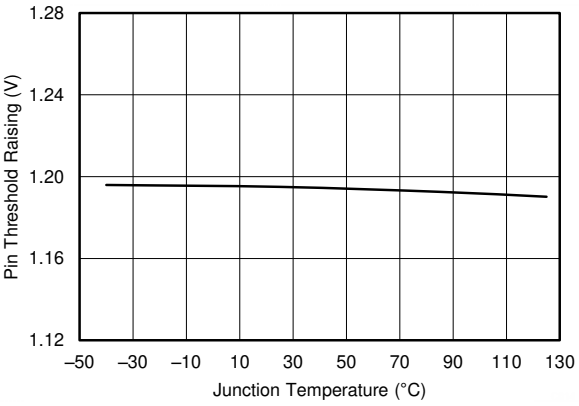


図 7-18. EN Pin Threshold Rising vs Temperature

7.6 Typical Characteristics (continued)

T_A = 25°C, VIN = 12 V, V_{OUT1}= 1.2 V, V_{OUT2}= 1.8 V, V_{OUT3}= 3.3 V F_{SW} = 600 kHz (unless otherwise noted)

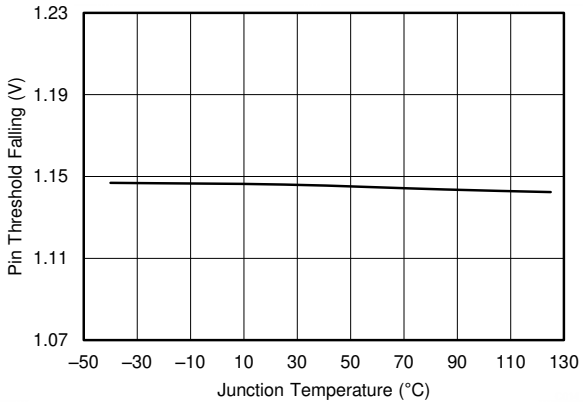


図 7-19. EN Pin Threshold Falling vs Temperature

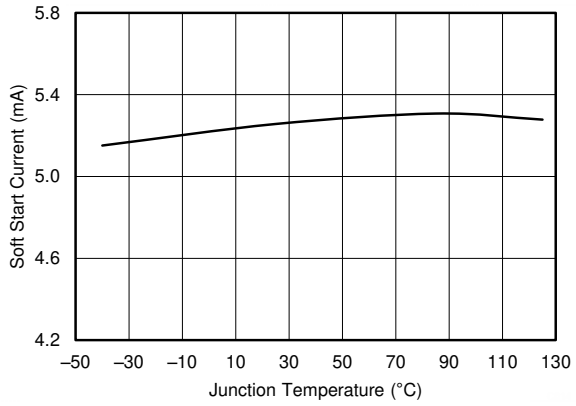


図 7-20. SS Pin Charge Current vs Temperature

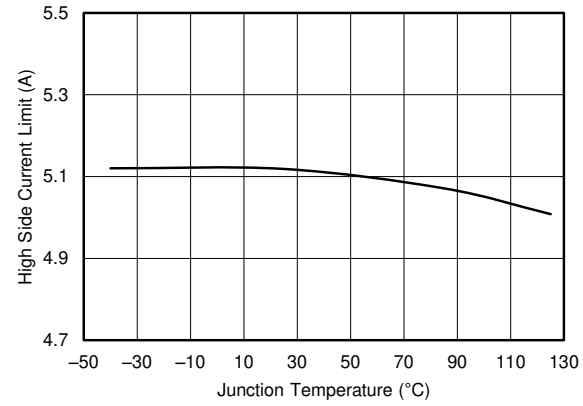


図 7-21. Buck1 High-Side Current Limit vs Temperature

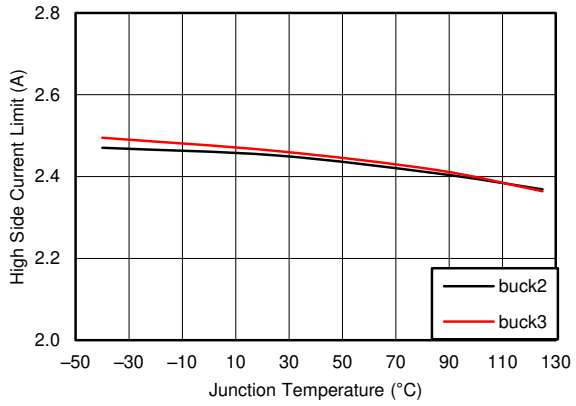


図 7-22. Buck2, 3 High-Side Current Limit vs Temperature

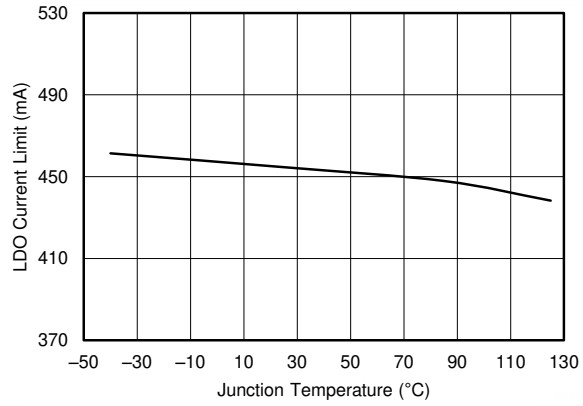


図 7-23. LDO Current Limit vs Temperature

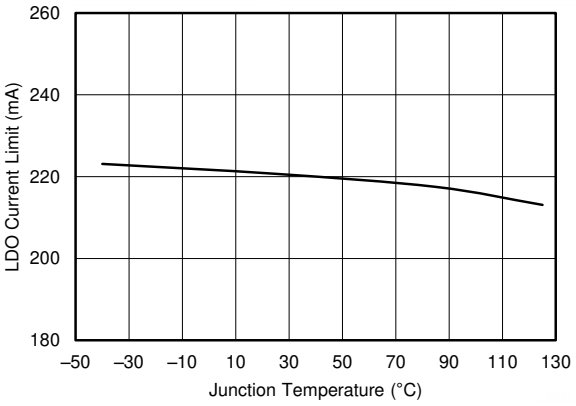


図 7-24. LDO2 Current Limit vs Temperature

8 Detailed Description

8.1 Overview

The TPS65262-1 is a monolithic, triple-synchronous step-down (buck) converter with 3-A/1-A/1-A output currents. A wide 4.5- to 18-V input supply voltage range encompasses most intermediate bus voltages operating off 5-V, 9-V, 12-V, or 15-V power bus. The feedback voltage reference for each buck is 0.6 V. Each buck is independent with dedicated enable, soft-start, and loop compensation.

The TPS65262-1 implements a constant frequency, peak current mode control that simplifies external loop compensation. The switching frequency is fixed 600 kHz. The switching clock of buck1 is 180° out-of-phase operation from the clocks of buck2 and buck3 channels to reduce input current ripple, input capacitor size, and power-supply-induced noise.

The TPS65262-1 is designed for safe monotonic startup into prebiased loads. The default start up is when VIN is typically 4.25 V. The ENx pin can also be used to adjust the input voltage undervoltage lockout (UVLO) with an external resistor divider. In addition, the ENx pin has an internal 3.6-µA current source, so the EN pin can be floating for automatically powering up the converters.

The TPS65262-1 reduces the external component count by integrating the bootstrap circuit. The bias voltage for the integrated high-side MOSFET is supplied by a capacitor between the BST and LX pins. A UVLO circuit monitors the bootstrap capacitor voltage VBST-VLX in each buck. When VBST-VLX voltage drops to the threshold, LX pin is pulled low to recharge the bootstrap capacitor. The TPS65262-1 can operate at 100% duty cycle as long as the bootstrap capacitor voltage is higher than the BOOT-LX UVLO threshold, which is typically 2.1 V.

The TPS65262-1 features a PGOOD pin to supervise each output voltage of buck converters. The TPS65262-1 has power good comparators with hysteresis, which monitor the output voltages through feedback voltages. When all bucks are in regulation range and power sequence is done, PGOOD is asserted to high.

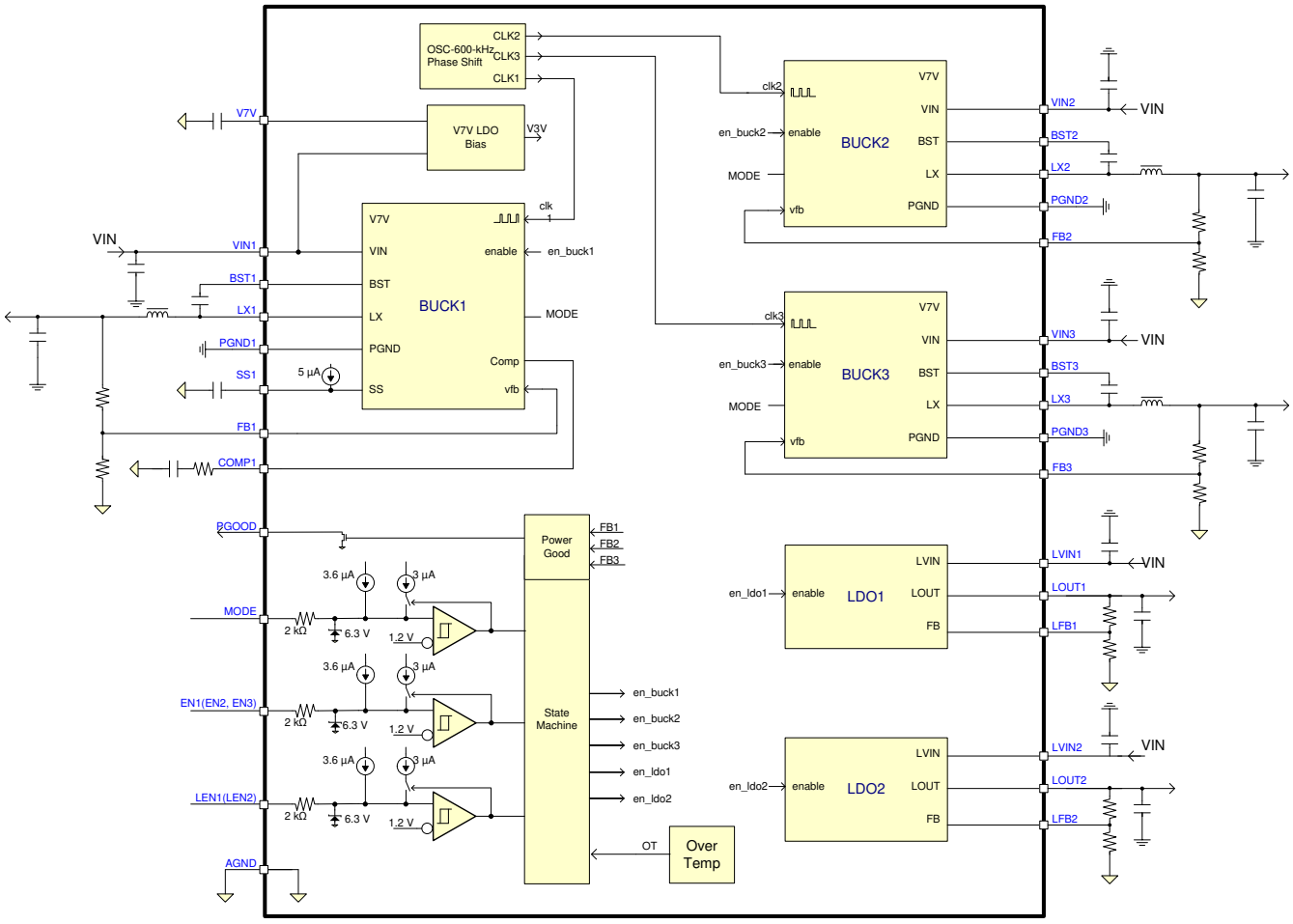
The SS (soft-start/tracking) pin is used to minimize inrush currents during power-up. A small-value capacitor or resistor divider is coupled to the pin for soft-start or voltage tracking.

At light loading, TPS65262-1 automatically operates in PSM to save power.

The TPS65262-1 integrates low dropout voltage linear regulators (LDO) with input voltage from 1.3 to 5.5 V, independent enable, and adjustable outputs, up to 350 mA for LDO1 and 150 mA for LDO2 continuous output current.

The TPS65262-1 is protected from overload and overtemperature fault conditions. The converter minimizes excessive output overvoltage transients by taking advantage of the power good comparator. When the output is more than 107.5% of the 0.6-V reference voltage, the high-side MOSFET is turned off until the internal feedback voltage is lower than 105% of the 0.6-V reference voltage. The TPS65262-1 implements both high-side MOSFET overload protection and bidirectional low-side MOSFET overload protections to avoid inductor current runaway. If the overcurrent condition lasts for more than the OC wait time (0.5 ms), the converter shuts down and restarts after the hiccup time (14 ms). The TPS65262-1 shuts down if the junction temperature is higher than thermal shutdown trip point 160°C. When the junction temperature drops 20°C (typical) below the thermal shutdown trip point, the TPS65262-1 is restarted under control of the soft-start circuit automatically.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Adjusting the Output Voltage

The output voltage of each buck is set with a resistor divider from the output of buck to the FB pin. TI recommends to use 1% tolerance, or better, divider resistors.

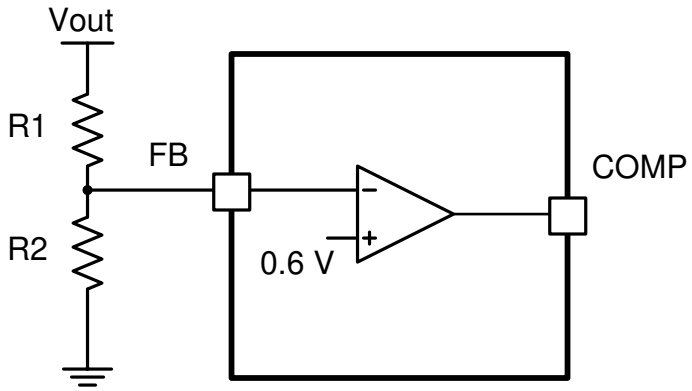


図 8-1. Voltage Divider Circuit

$$R_2 = R_1 \times \frac{0.6}{V_{out} - 0.6} \quad (1)$$

To improve efficiency at light loads, consider using larger value resistors. If the values are too high, the regulator is more sensitive to noise. 表 8-1 shows the recommended resistor values.

表 8-1. Output Resistor Divider Selection

Output Voltage (V)	R1 (kΩ)	R2 (kΩ)
1	10	15
1.2	10	10
1.5	15	10
1.8	20	10
2.5	31.6	10
3.3	45.3	10
3.3	22.6	4.99
5	73.2	10
5	36.5	4.99

8.3.2 Enable and Adjusting UVLO

The EN1, EN2, and EN3 pins provide electrical on and off control of the device. When the EN1, EN2, and EN3 pins' voltage exceeds the threshold voltage, the device starts operation. If each ENx pin voltage is pulled below the threshold voltage, the regulator stops switching and enters low I_q state.

The EN pin has an internal pullup current source, allowing the user to float the EN pin for enabling the device. If an application requires controlling the EN pin, use open-drain or open-collector output logic to interface with the pin.

The device implements internal UVLO circuitry on the VIN pin. The device is disabled when the VIN pin voltage falls below the internal VIN UVLO threshold. The internal VIN UVLO threshold has a hysteresis of 500 mV. If an application requires a higher UVLO threshold on the VIN pin, then the ENx pin can be configured as shown in 図 8-2. When using the external UVLO function, TI recommends to set the hysteresis to be greater than 500 mV.

The EN pin has a small pullup current, I_p, which sets the default state of the pin to enable when no external components are connected. The pullup current is also used to control the voltage hysteresis for the UVLO function because it increases by I_h after the EN pin crosses the enable threshold. The UVLO thresholds can be calculated using 式 2 and 式 3.

$$R_1 = \frac{V_{START}\left(\frac{V_{ENFALLING}}{V_{ENRISING}}\right) - V_{STOP}}{I_P\left(1 - \frac{V_{ENFALLING}}{V_{ENRISING}}\right) + I_h} \quad (2)$$

$$R_2 = \frac{R_1 \times V_{ENFALLING}}{V_{STOP} - V_{ENFALLING} + R_1\left(I_h + I_p\right)} \quad (3)$$

where

- I_h = 3 µA
- I_p = 3.6 µA
- $V_{ENRISING}$ = 1.2 V
- $V_{ENFALLING}$ = 1.15 V

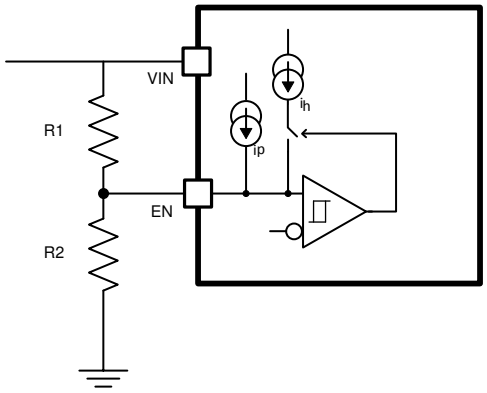


図 8-2. Adjustable VIN UVLO

8.3.3 Soft-Start Time

The voltage on the SS1 pin controls the start-up of buck1 output. When the voltage on the SS1 pin is less than the internal 0.6-V reference, The TPS65262-1 regulates the internal feedback voltage to the voltage on the SS1 pin instead of 0.6 V, allowing VOUT to rise smoothly from 0 V to its regulated voltage without inrush current. The device has an internal pullup current source of 5 µA (typical) that charges an external soft-start capacitor to provide a linear ramping voltage at SS1 pin.

Buck1's soft-start time can be calculated approximately by 式 4.

Buck2 and Buck3 have fixed 1-ms soft-start time.

$$Tss(ms) = \frac{Css(nF) \times Vref(V)}{Iss(\mu A)} \quad (4)$$

8.3.4 Power-Up Sequencing

TPS65262-1 features a comprehensive sequencing circuit for the three bucks. If the MODE pin is driving to high at the same time EN1 or EN2 pin (or both), the automatic power-up and power-down sequence function is active. If MODE pin ties low to ground, three buck on or off is separately controlled by three enable pins.

8.3.4.1 External Power Sequencing

The TPS65262-1 has a dedicated enable pin for each converter. The converter enable pins are biased by a current source that allows for easy sequencing with the addition of an external capacitor. Disabling the converter with an active pulldown transistor on the ENx pin allows for a predictable power-down timing operation. 図 8-3 shows the timing diagram of a typical buck power-up sequence with a capacitor connected at ENx pin.

A typical 1.4-µA current charges the ENx pin from the input supply when the ENx pin voltage is lower than typical 0.4 V. The internal V7V LDO turns on when the ENx pin voltage rises to typical 0.4 V and a 3.6-µA pullup current sources ENx. After the ENx pin voltage reaches 1.2 V typical, 3-µA hysteresis current sources to the pin to improve noise sensitivity. If all output voltages are in regulation, PGOOD is asserted after PGOOD deglitch time.

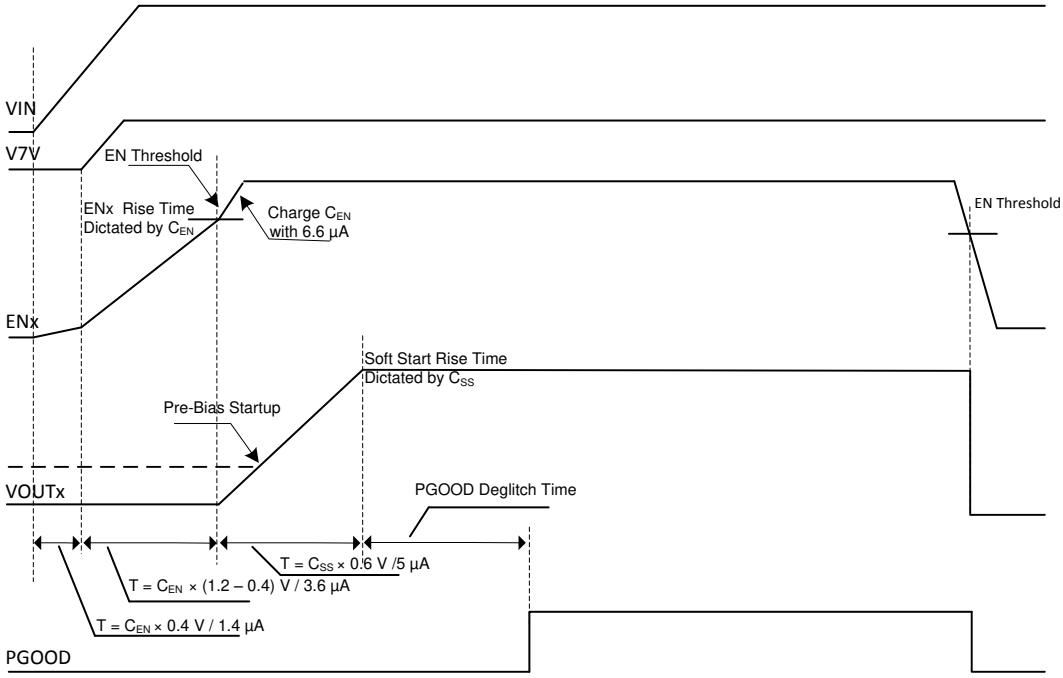


図 8-3. Startup Power Sequence

8.3.4.2 Automatic Power Sequencing

The TPS65262-1 starts with a predefined power-up and power-down sequence when the MODE pin is driven to high. As shown in 表 8-2, the sequence is dictated by different combinations of the EN1 and EN2 status. EN3 is used to start or stop the converters. Buck2 and buck3 are identical converters and can be swapped in the system operation to allow for additional sequencing stages. 図 8-4 shows the power sequencing when EN1 and EN2 are pulled up high.

表 8-2. Power Sequencing

	MODE	EN1	EN2	EN3	Start Sequencing	Shutdown Sequencing
Automatic power sequencing	High	High	High	Used to start or stop bucks in sequence	Buck1→buck2→buck3	Buck3→buck2→buck1
	High	Low	High		Buck2→buck1→buck3	Buck3→buck1→buck2
	High	High	Low		Buck2→buck3→buck1	Buck1→buck3→buck2
	High	Low	Low	Reserved	Reserved	Reserved
Externally controlled sequencing	Low	Used to start or stop buck1	Used to start or stop buck2	Used to start or stop buck3	x	x

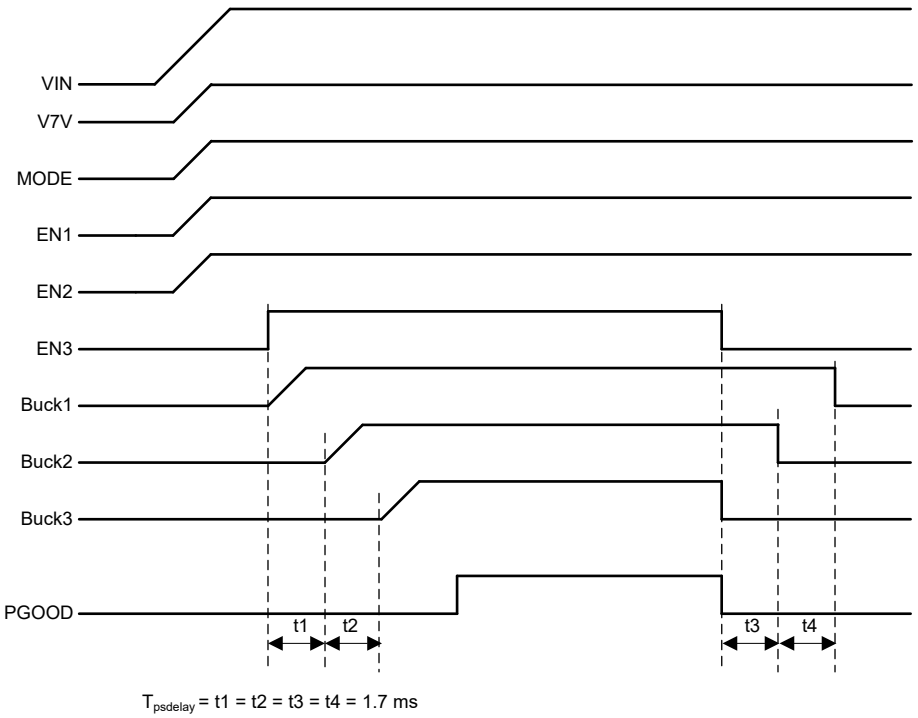


図 8-4. Automatic Power Sequencing

8.3.5 V7V Low Dropout Regulator and Bootstrap

Power for the high-side and low-side MOSFET drivers and most other internal circuitry is derived from the V7V pin. The internal built-in low dropout linear regulator (LDO) supplies 6.3 V (typical) from VIN to V7V. A 10-µF ceramic capacitor must be connected from V7V pin to power ground.

If the input voltage, VIN decreases to UVLO threshold voltage, the UVLO comparator detects V7V pin voltage and forces the converter off.

Each high-side MOSFET driver is biased from the floating bootstrap capacitor, CB, shown in 図 8-5, which is normally recharged during each cycle through an internal low-side MOSFET or the body diode of low-side MOSFET when the high-side MOSFET turns off. The boot capacitor is charged when the BST pin voltage is less than VIN and the BST-LX voltage is below regulation. The recommended value of this ceramic capacitor is 47 nF. TI recommends a ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating of 10 V or higher because of the stable characteristics over temperature and voltage. Each low-side MOSFET driver is powered from V7V pin directly.

To improve dropout, the device is designed to operate at 100% duty cycle as long as the BST to LX pin voltage is greater than the BST-LX UVLO threshold, which is typically 2.1 V. When the voltage between BST and LX drops below the BST-LX UVLO threshold, the high-side MOSFET is turned off and the low-side MOSFET is turned on allowing the boot capacitor to be recharged.

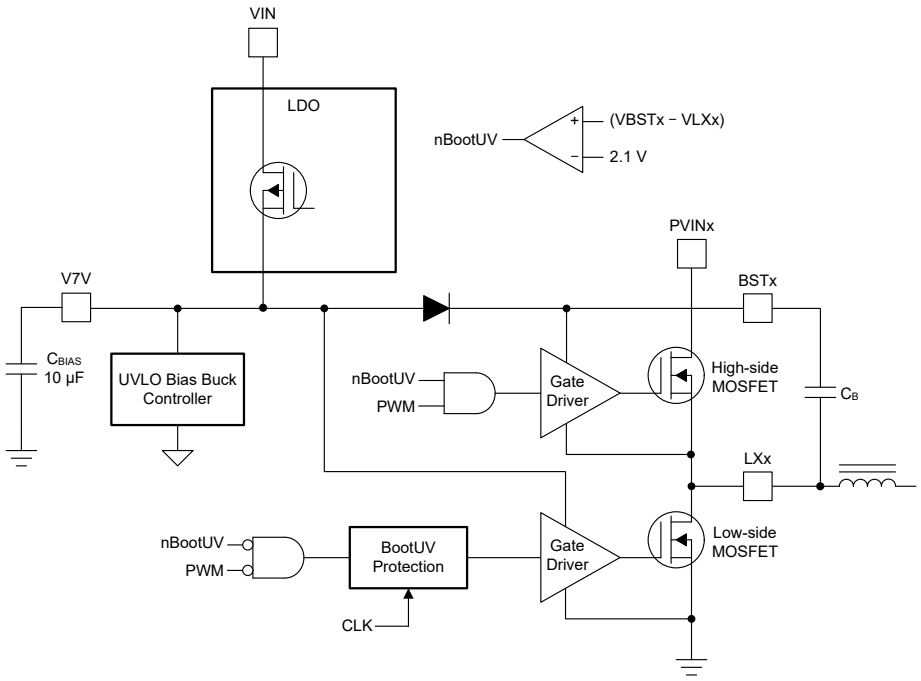


図 8-5. V7V Linear Dropout Regulator and Bootstrap Voltage Diagram

8.3.6 Out-of-Phase Operation

To reduce input ripple current, the switch clock of buck1 is 180° out-of-phase from the clock of buck2 and buck3. This enables the system having less input current ripple to reduce input capacitors' size, cost, and EMI.

8.3.7 Output Overvoltage Protection (OVP)

The device incorporates an output OVP circuit to minimize output voltage overshoot. When the output is overloaded, the error amplifier compares the actual output voltage to the internal reference voltage. If the FB pin voltage is lower than the internal reference voltage for a considerable time, the output of the error amplifier demands maximum output current. After the condition is removed, the regulator output rises and the error amplifier output transitions to the steady-state voltage. In some applications with small output capacitance, the load can respond faster than the error amplifier. This leads to the possibility of an output overshoot. Each buck compares the FB pin voltage to the OVP threshold. If the FB pin voltage is greater than the OVP threshold, the high-side MOSFET is turned off preventing current from flowing to the output and minimizing output overshoot. When the FB voltage drops lower than the OVP threshold, the high-side MOSFET turns on at the next clock cycle.

8.3.8 PSM

The TPS65262-1 can enter high-efficiency PSM operation at light load current.

When the controller is enabled for PSM operation, the peak inductor current is sensed and compared with 230-mA current typically. Because the integrated current comparator catches the peak inductor current only, the average load current entering PSM varies with the applications and external output filters. In PSM, the sensed peak inductor current is clamped at 230 mA.

When a controller operates in PSM, the inductor current is not allowed to reverse. The reverse current comparator turns off the low-side MOSFET when the inductor current reaches 0, preventing it from reversing and going negative.

Due to the delay in the circuit and current comparator tdly (typical 50 ns at Vin = 12 V), the real peak inductor current threshold to turn off high-side power MOSFET can shift higher depending on inductor inductance and

input or output voltages. Calculate the threshold of peak inductor current to turn off high-side power MOSFET with 式 5.

$$IL_{PEAK} = 230mA + \frac{vin - vout}{L} \times tdly \quad (5)$$

After the charge accumulated on the Vout capacitor is more than loading needs, the COMP pin voltage drops to low voltage driven by error amplifier. There is an internal comparator at the COMP pin. If the comp voltage is lower than 0.35 V, the power stage stops switching to save power.

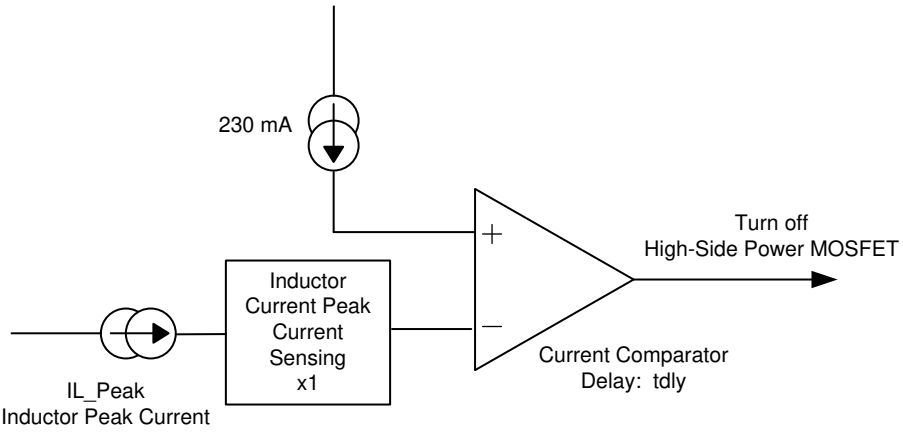


図 8-6. PSM Current Comparator

8.3.9 Slope Compensation

To prevent subharmonic oscillations when the device operates at duty cycles greater than 50%, the device adds built-in slope compensation, which is a compensating ramp to the switch current signal.

8.3.10 Overcurrent Protection (OCP)

The device is protected from overcurrent conditions by cycle-by-cycle current limiting on both the high-side MOSFET and low-side MOSFET.

8.3.10.1 High-Side MOSFET OCP

The device implements current mode control which uses the COMP pin voltage to control the turn off of the high-side MOSFET and the turn on of the low-side MOSFET on a cycle-by-cycle basis. Each cycle the switch current and the current reference generated by the COMP pin voltage are compared. When the peak switch current intersects the current reference, the high-side switch is turned off.

8.3.10.2 Low-Side MOSFET OCP

While the low-side MOSFET is turned on, its conduction current is monitored by the internal circuitry. During normal operation, the low-side MOSFET sources current to the load. At the end of every clock cycle, the low-side MOSFET sourcing current is compared to the internally set low-side sourcing current limit. If the low-side sourcing current is exceeded, the high-side MOSFET is not turned on and the low-side MOSFET stays on for the next cycle. The high-side MOSFET is turned on again when the low-side current is below the low-side sourcing current limit at the start of a cycle.

The low-side MOSFET can also sink current from the load. If the low-side sinking current limit is exceeded, the low-side MOSFET is turned off immediately for the rest of that clock cycle. In this scenario, both MOSFETs are off until the start of the next cycle.

Furthermore, if an output overload condition (as measured by the COMP pin voltage) lasts for more than the hiccup wait time (which is programmed for 0.5 ms, shown in 図 8-7) the device shuts down itself and restarts

after the hiccup time, 14 ms. The hiccup mode helps to reduce the device power dissipation under severe overcurrent condition.

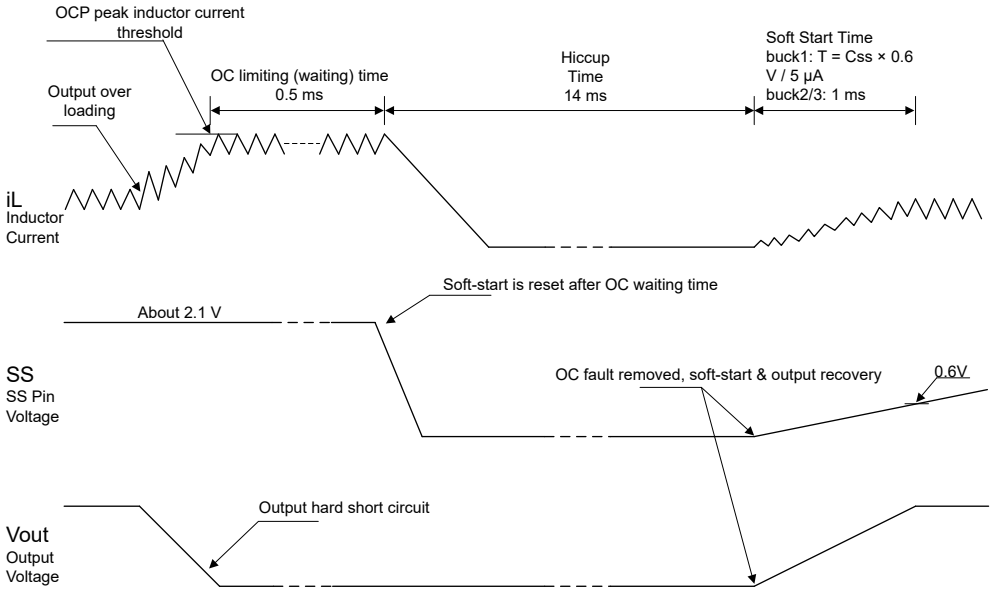


図 8-7. OCP

8.3.11 Power Good

The PGOOD pin is an open-drain output. When feedback voltage of each buck is between 95% (rising) and 105% (falling) of the internal voltage reference, the PGOOD pin pulldown is deasserted and the pin floats. TI recommends to use a pullup resistor between the values of 10 to 100 kΩ to a voltage source that is 6.3 V or less. The PGOOD is in a defined state when the VIN input voltage is greater than 1 V but with reduced current sinking capability. The PGOOD achieves full current sinking capability when the VIN input voltage is above UVLO threshold, which is 4.25 V typically.

The PGOOD pin is pulled low when any feedback voltage of buck is lower than 92.5% (falling) or greater than 107.5% (rising) of the nominal internal reference voltage. Also, the PGOOD is pulled low, if the input voltage is undervoltage locked up, thermal shutdown is asserted, the EN pin is pulled low or the converter is in a soft-start period.

8.3.12 Thermal Shutdown

The internal thermal shutdown circuitry forces the device to stop switching if the junction temperature exceeds 160°C typically. The device reinitiates the power-up sequence when the junction temperature drops below 140°C typically.

8.4 Device Functional Modes

8.4.1 Operation With V_{IN} < 4.5 V (Minimum V_{IN})

The device operates with input voltages above 4.5 V. The maximum UVLO voltage is 4.5 V and operates at input voltages above 4.5 V. The typical UVLO voltage is 4.25 V, and the device can operate at input voltages above that point. The device also can operate at lower input voltages; the minimum UVLO voltage is 4 V (rising) and 3.5 V (falling). At input voltages below the UVLO minimum voltage, the device does not operate.

8.4.2 Operation With EN Control

The enable rising edge threshold voltage is 1.2 V typical and 1.26 V maximum. With EN held below that voltage, the device is disabled and switching is inhibited. The IC quiescent current is reduced in this state. When the input voltage is above the UVLO threshold and the EN voltage is increased above the rising edge threshold, the device becomes active. Switching is enabled, and the soft-start sequence is initiated. The device starts at the soft-start time determined by the external soft start capacitor as shown in 図 9-2 to 図 9-7.

8.4.3 Operation at Light Loads

The device is designed to operate in high-efficiency PSM under light load conditions. Pulse skipping is initiated when the switch current falls to 0.23 A. During pulse skipping, the low-side FET is turned off. The switching node (LX) waveform takes on the characteristics of DCM operation and the apparent switching frequency decreases as shown in 図 9-8, 図 9-10, and 図 9-12.

9 Application and Implementation

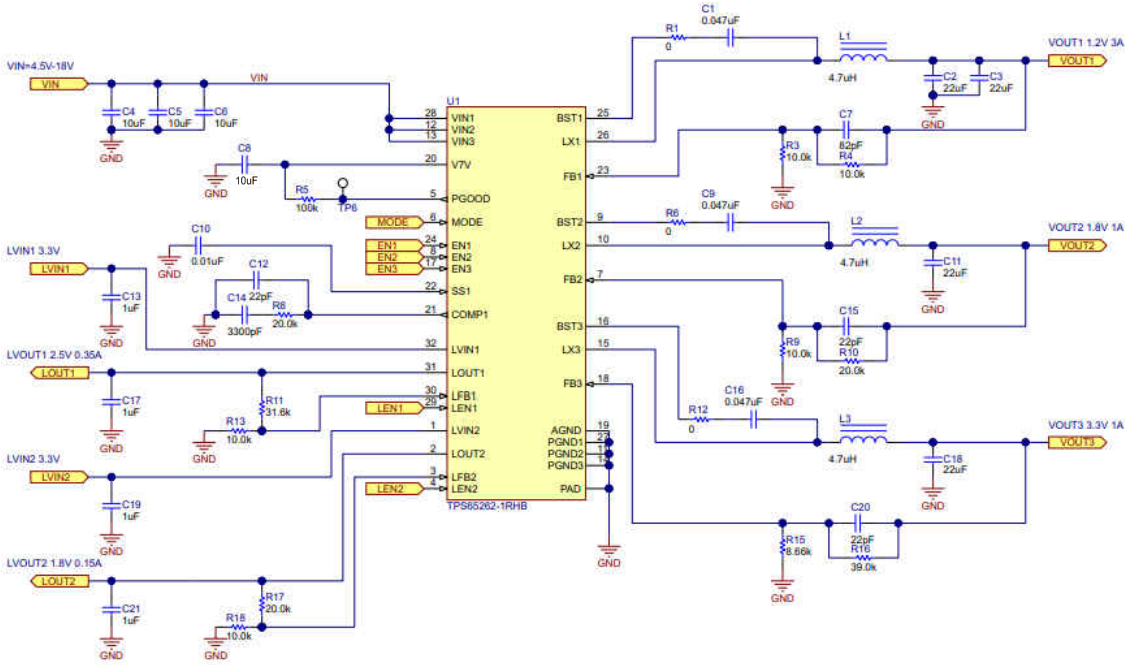
注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

9.1 Application Information

The device is triple-synchronous, step-down DC/DC converter with dual LDOs. The device is typically used to convert a higher DC voltage to lower DC voltages with continuous available output current of 3 A/1 A/1 A. The following design procedure can be used to select component values for the TPS65262-1. This section presents a simplified discussion of the design process.

9.2 Typical Application



9.2.1 Design Requirements

This example details the design of a triple-synchronous step-down converter. A few parameters must be known to start the design process. These parameters are typically determined at the system level. For this example, start with the following known parameters shown in 表 9-1.

表 9-1. Design Parameters

PARAMETER	VALUE
Vout1	1.2 V
Iout1	3 A
Vout2	1.8 V
Iout2	1 A
Vout3	3.3 V
Iout3	1 A
Buck1 transient response 1-A load step	±5%
Buck2, buck3 transient response 0.5-A load step	±5%
Input voltage	12 V normal, 4.5 to 18 V
Output voltage ripple	±1%
Switching frequency	600 kHz

9.2.2 Detailed Design Procedure

9.2.2.1 Output Inductor Selection

To calculate the value of the output inductor, use 式 6. LIR is a coefficient that represents the amount of inductor ripple current relative to the maximum output current. The inductor ripple current is filtered by the output capacitor. Therefore, choosing high inductor ripple currents impact the selection of the output capacitor because the output capacitor must have a ripple current rating equal to or greater than the inductor ripple current. In general, the inductor ripple value is at the discretion of the designer; however, LIR is normally from 0.1 to 0.3 for the majority of applications.

$$L = \frac{V_{inmax} - V_{out}}{I_o \times LIR} \times \frac{V_{out}}{V_{inmax} \times f_{sw}} \tag{6}$$

For the output filter inductor, it is important not to exceed the RMS current and saturation current ratings. The RMS and peak inductor current can be found from 式 8 and 式 9.

$$I_{ripple} = \frac{V_{inmax} - V_{out}}{L} \times \frac{V_{out}}{V_{inmax} \times f_{sw}} \tag{7}$$

$$I_{Lrms} = \sqrt{I_O^2 + \frac{\left(\frac{V_{out} \times (V_{inmax} - V_{out})}{V_{inmax} \times L \times f_{sw}}\right)^2}{12}} \tag{8}$$

$$I_{Lpeak} = I_{out} + \frac{I_{ripple}}{2} \tag{9}$$

The current flowing through the inductor is the inductor ripple current plus the output current. During power-up, faults, or transient load conditions, the inductor current can increase above the calculated peak inductor current level calculated previously. In transient conditions, the inductor current can increase up to the switch current limit of the device. For this reason, the most conservative approach is to specify an inductor with a saturation current rating equal to or greater than the switch current limit rather than the peak inductor current.

9.2.2.2 Output Capacitor Selection

The designer needs to account for three primary considerations when selecting the value of the output capacitor. The output capacitor determines the modulator pole, the output voltage ripple, and how the regulator responds to a large change in load current. The output capacitance must be selected based on the most stringent of these three criteria.

The first criterion is the desired response to a large change in the load current. The output capacitor needs to supply the load with current when the regulator cannot. This situation can occur if there are desired hold-up times for the regulator where the output capacitor must hold the output voltage above a certain level for a specified amount of time after the input power is removed. The regulator is also temporarily not able to supply sufficient output current if there is a large, fast increase in the current needs of the load such as a transition from no load to full load. The regulator usually needs two or more clock cycles for the control loop to see the change in load current and output voltage and adjust the duty cycle to react to the change. The output capacitor must be sized to supply the extra current to the load until the control loop responds to the load change. The output capacitance must be large enough to supply the difference in current for two clock cycles while only allowing a tolerable amount of droop in the output voltage. 式 10 shows the minimum output capacitance necessary to accomplish this.

$$C_o = \frac{2 \times \Delta I_{out}}{f_{sw} \times \Delta V_{out}} \tag{10}$$

where

- ΔI_{out} is the change in output current.
- f_{sw} is the regulator's switching frequency.
- ΔV_{out} is the allowable change in the output voltage.

式 11 calculates the minimum output capacitance needed to meet the output voltage ripple specification.

$$C_o > \frac{1}{8 \times f_{sw}} \times \frac{1}{\frac{V_{oripple}}{I_{oripple}}} \tag{11}$$

where

- f_{sw} is the switching frequency.
- $V_{oripple}$ is the maximum allowable output voltage ripple.
- $I_{oripple}$ is the inductor ripple current.

式 12 calculates the maximum ESR an output capacitor can have to meet the output voltage ripple specification.

$$R_{esr} < \frac{V_{oripple}}{I_{oripple}} \tag{12}$$

Additional capacitance deratings for aging, temperature, and DC bias must be factored in, which increase this minimum value. Capacitors generally have limits to the amount of ripple current they can handle without failing or producing excess heat. An output capacitor that can support the inductor ripple current must be specified. Some capacitor data sheets specify the root mean square (RMS) value of the maximum ripple current. 式 13 can be used to calculate the RMS ripple current the output capacitor needs to support.

$$I_{corms} = \frac{V_{out} \times (V_{inmax} - V_{out})}{\sqrt{12} \times V_{inmax} \times L \times f_{sw}} \tag{13}$$

9.2.2.3 Input Capacitor Selection

The TPS65262-1 requires a high-quality ceramic, type X5R or X7R, input decoupling capacitor of at least 10 µF of effective capacitance on the VIN input voltage pins. In some applications, additional bulk capacitance can also be required for the VIN input. The effective capacitance includes any DC bias effects. The voltage rating of the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum input current ripple of the TPS65262-1. Calculate the input ripple current using 式 14.

$$I_{inrms} = I_{out} \times \sqrt{\frac{V_{out}}{V_{inmin}} \times \frac{(V_{inmin} - V_{out})}{V_{inmin}}} \quad (14)$$

The value of a ceramic capacitor varies significantly over temperature and the amount of DC bias applied to the capacitor. The capacitance variations due to temperature can be minimized by selecting a dielectric material that is stable over temperature. X5R and X7R ceramic dielectrics are usually selected for power regulator capacitors because they have a high capacitance to volume ratio and are fairly stable over temperature. The output capacitor must also be selected with the DC bias taken into account. The capacitance value of a capacitor decreases as the DC bias across a capacitor increases. The input capacitance value determines the input ripple voltage of the regulator. Calculate the input voltage ripple using 式 15.

$$\Delta V_{in} = \frac{I_{outmax} \times 0.25}{C_{in} \times f_{sw}} \quad (15)$$

9.2.2.4 Loop Compensation

The TPS65262-1 incorporates a peak current mode control scheme. The error amplifier is a transconductance amplifier with a gain of 300 µS. A typical type II compensation circuit adequately delivers a phase margin between 60° and 90°. C_b adds a high frequency pole to attenuate high-frequency noise when needed. To calculate the external compensation components, follow these steps.

1. Switching frequency, f_{sw}, 600 kHz is appropriate for application depending on L and C sizes, output ripple, EMI, and so forth. It also gives the best trade-off between performance and cost.
2. Set up crossover frequency, fc, which is typically between 1/5 and 1/20 of f_{sw}.
3. R_C can be determined by 式 16.

$$R_C = \frac{2\pi \times fc \times Vo \times Co}{G_{m-EA} \times Vref \times G_{m-PS}} \quad (16)$$

where

- G_{m_EA} is the error amplifier gain (300 µS)
- G_{m_PS} is the power stage voltage to current conversion gain (7.4 A/V)

4. Calculate C_C by placing a compensation zero at or before the dominant pole $\left(fp = \frac{1}{C_o \times R_L \times 2\pi} \right)$.

$$C_C = \frac{R_L \times Co}{R_C} \quad (17)$$

5. Optional C_b can be used to cancel the zero from the ESR associated with C_O.

$$C_b = \frac{R_{ESR} \times Co}{R_C} \quad (18)$$

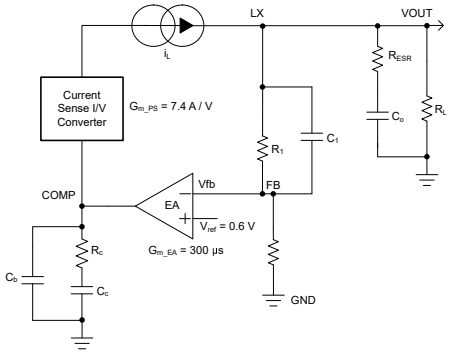


図 9-1. DC/DC Loop Compensation

9.2.3 Application Curves

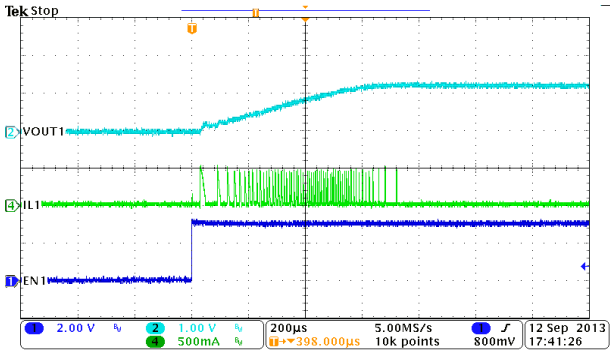


図 9-2. BUCK1, Soft-Start With No Load

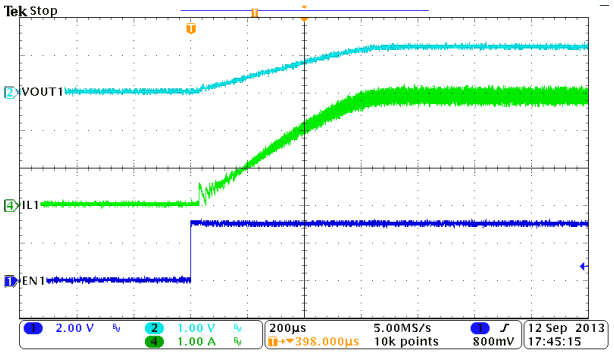


図 9-3. BUCK1, Soft-Start With Full Load

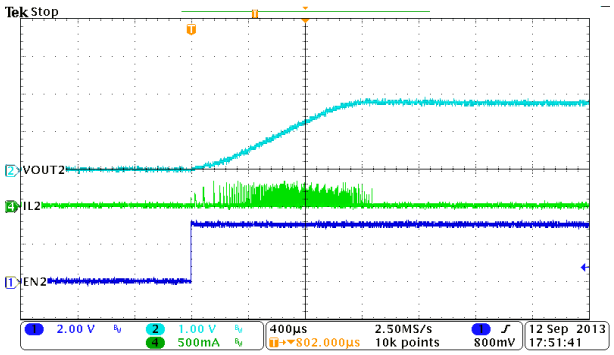


図 9-4. BUCK2, Soft-Start With No Load

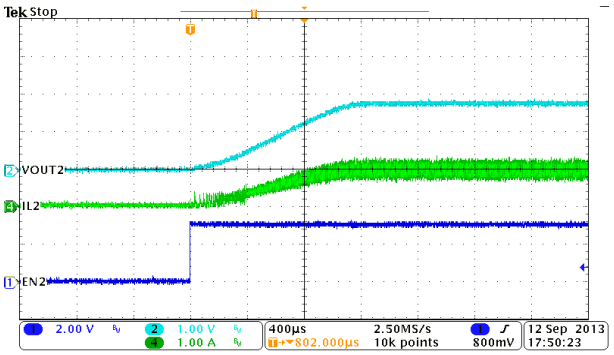


図 9-5. BUCK2, Soft-Start With Full Load

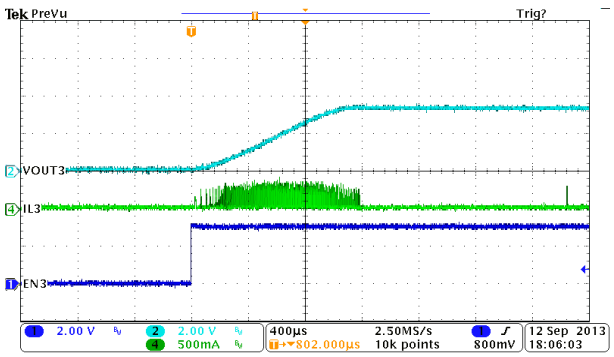


図 9-6. BUCK3, Soft-Start With No Load

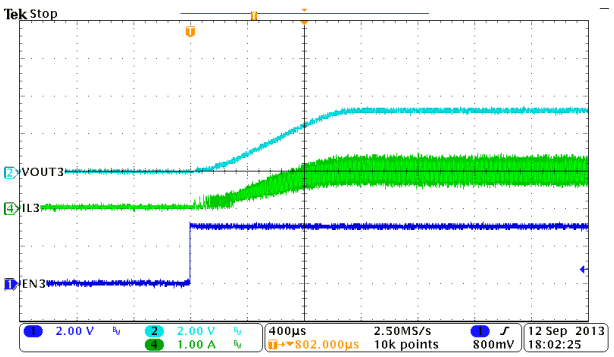


図 9-7. BUCK3, Soft-Start With Full Load

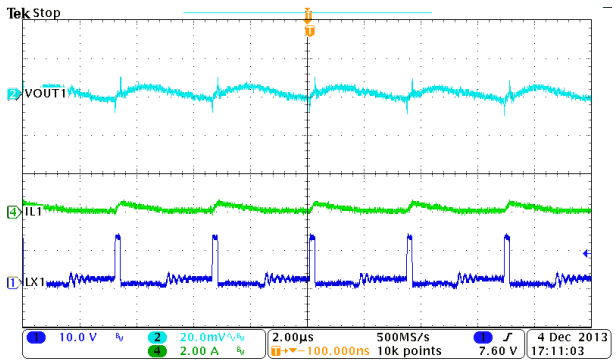


図 9-8. Buck1, Steady State Operation at Light Load

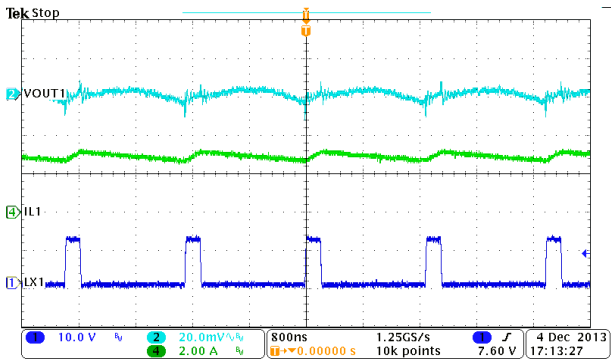


図 9-9. Buck1, Steady State Operation at Full Load

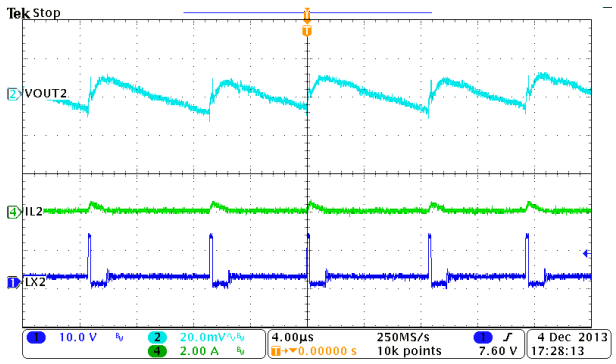


図 9-10. Buck2, Steady State Operation at Light Load

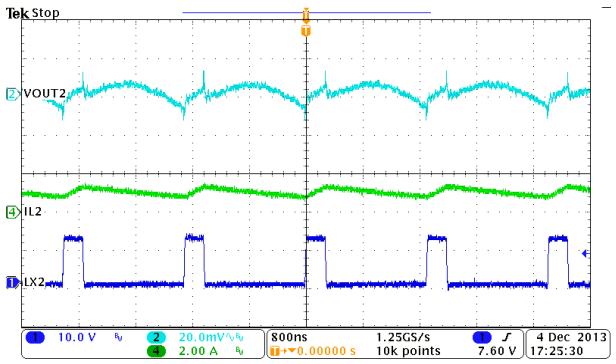


図 9-11. Buck2, Steady State Operation at Full Load

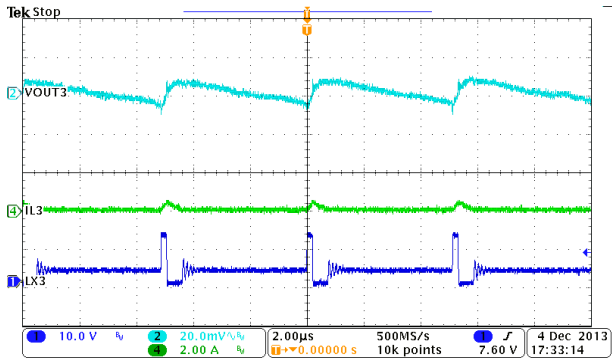


図 9-12. Buck3, Steady State Operation at Light Load

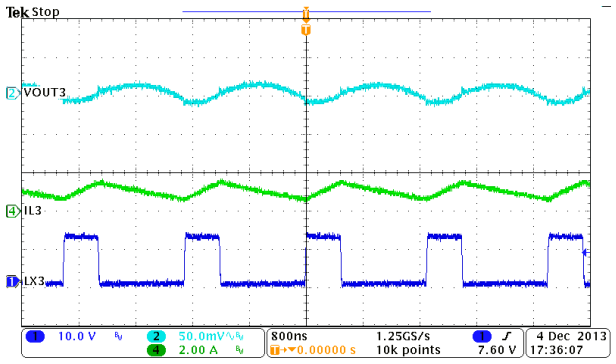


図 9-13. Buck3, Steady State Operation at Full Load

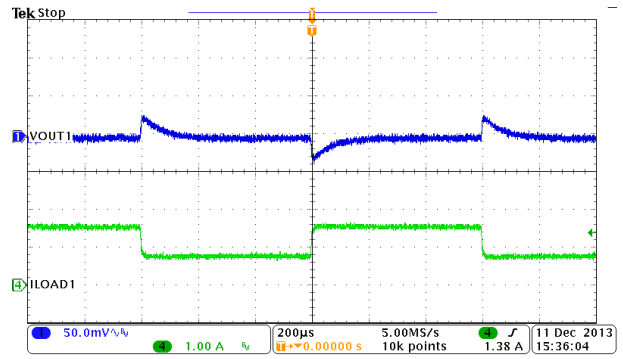


図 9-14. Buck1, Load Transient, 0.75 to 1.5 A SR = 0.25 A/µs

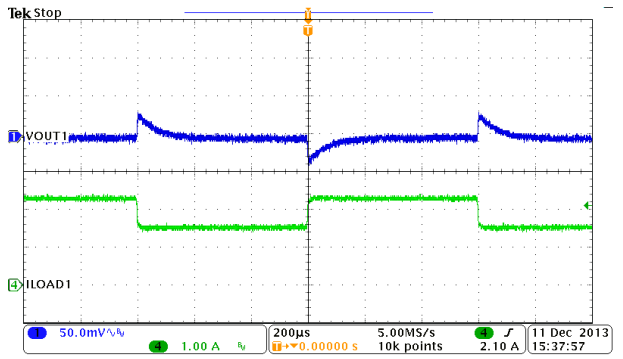


図 9-15. Buck1, Load Transient, 1.5 to 2.25 A SR = 0.25 A/µs

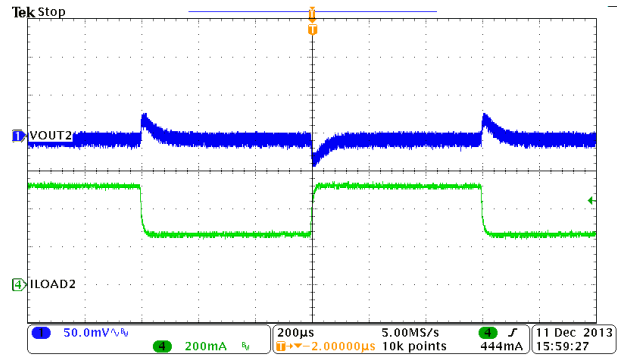


図 9-16. Buck2, Load Transient, 0.25 to 0.5 A SR = 0.25 A/µs

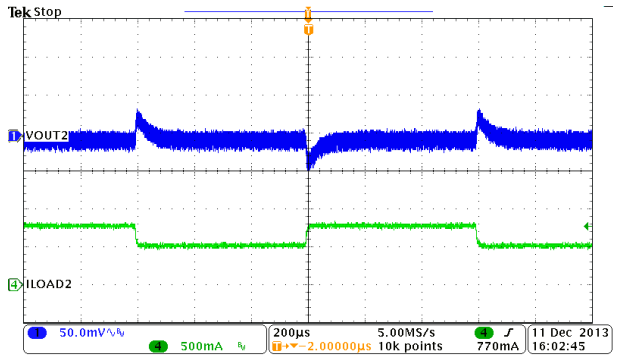


図 9-17. Buck2, Load Transient, 0.5 to 0.75 A SR = 0.25 A/µs

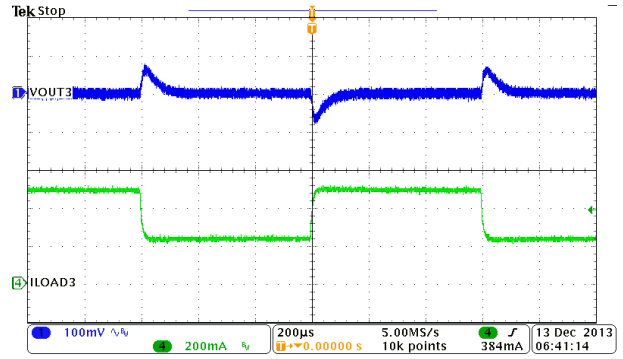


図 9-18. Buck3, Load Transient, 0.25 to 0.5 A SR = 0.25 A/µs

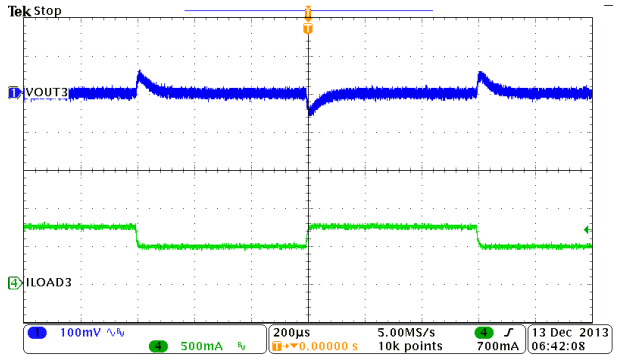


図 9-19. Buck3, Load Transient, 0.5 to 0.75 A SR = 0.25 A/µs

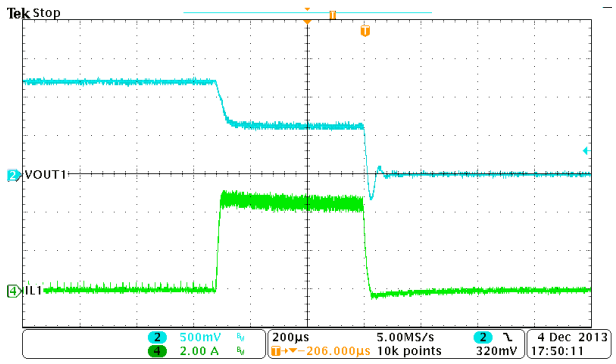


図 9-20. Buck1, OCP

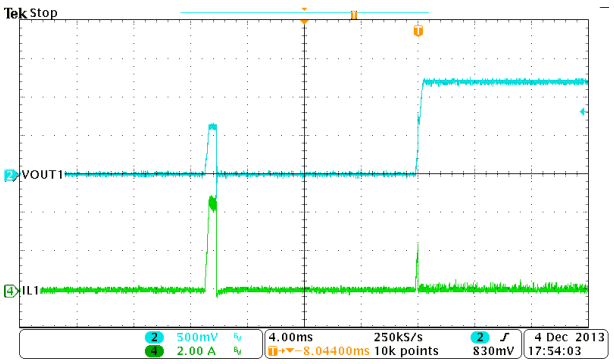


図 9-21. Buck1, Hiccup and Recovery

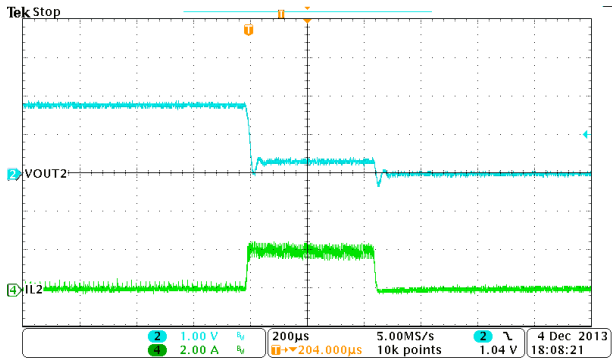


図 9-22. Buck2, OCP

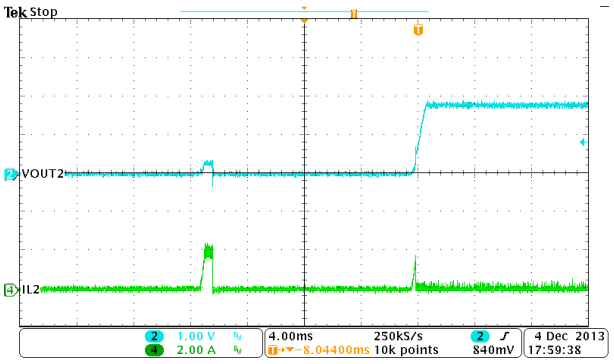


図 9-23. Buck2, Hiccup and Recovery

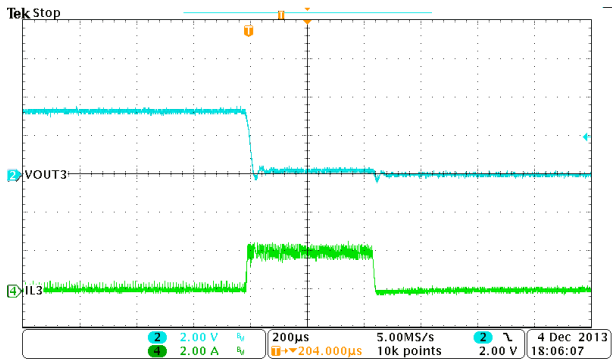


図 9-24. Buck3, OCP

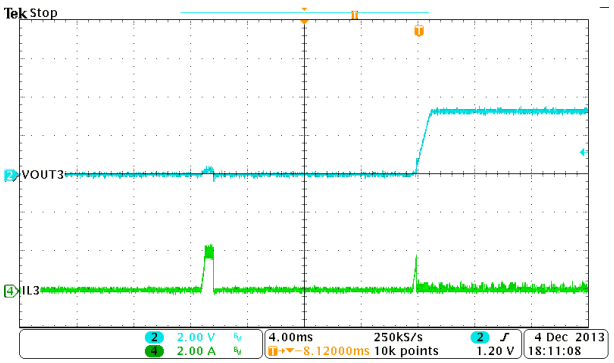


図 9-25. Buck3, Hiccup and Recovery

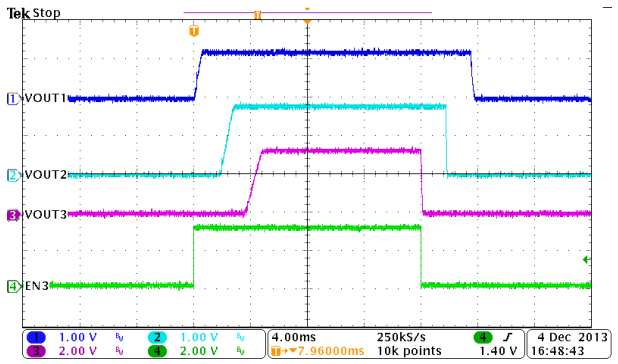


図 9-26. Automatic Power Sequencing, MODE = EN1 = EN2 = HIGH

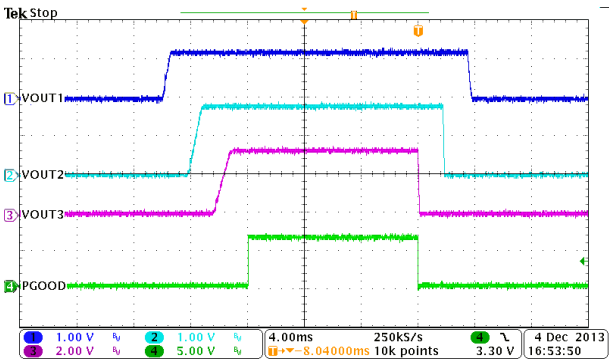


図 9-27. Automatic Power Sequencing, MODE = EN1 = EN2 = HIGH

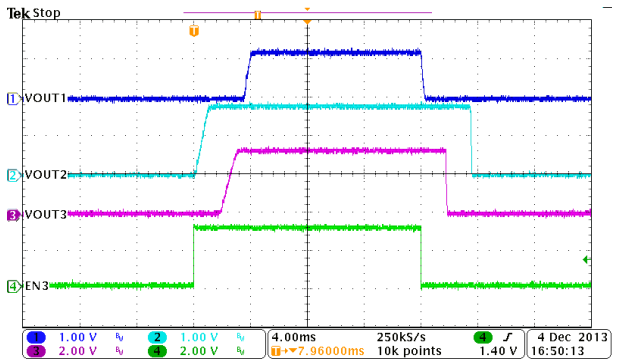


図 9-28. Automatic Power Sequencing, MODE = EN1 = HIGH, EN2 = LOW

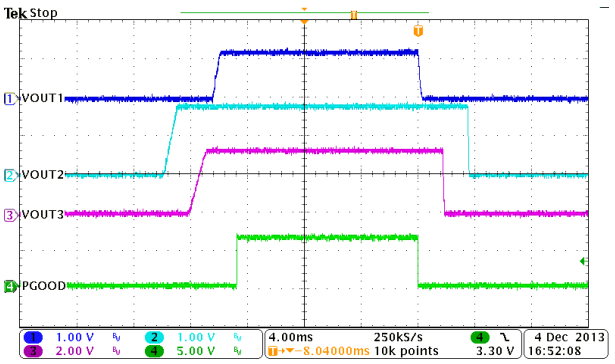


図 9-29. Automatic Power Sequencing, MODE = EN1 = HIGH, EN2 = LOW

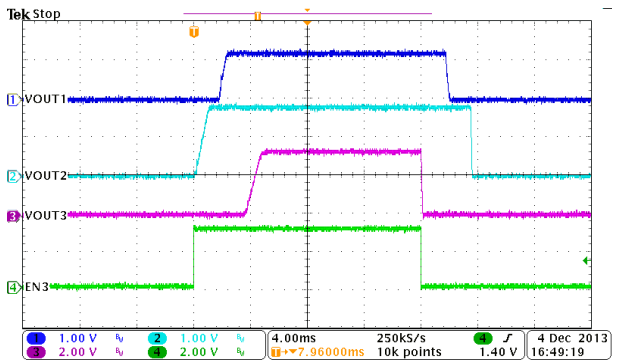


図 9-30. Automatic Power Sequencing, MODE = EN2 = HIGH, EN1 = LOW

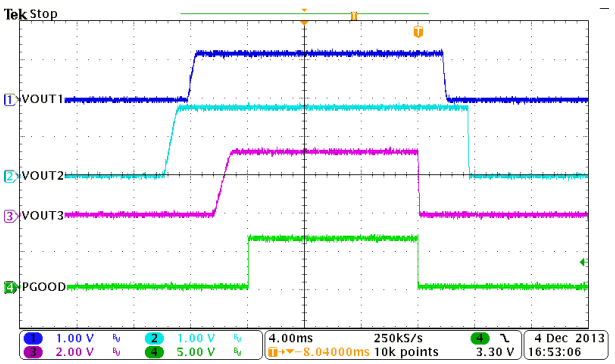
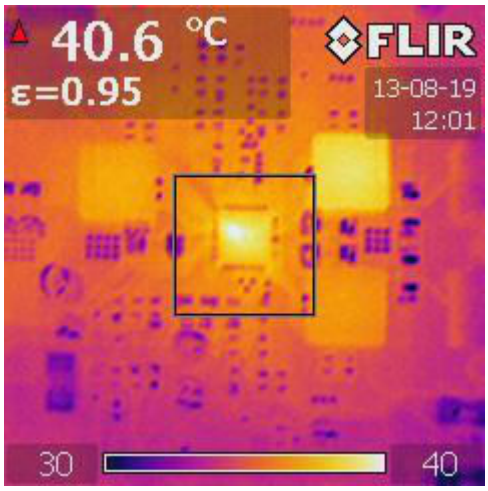
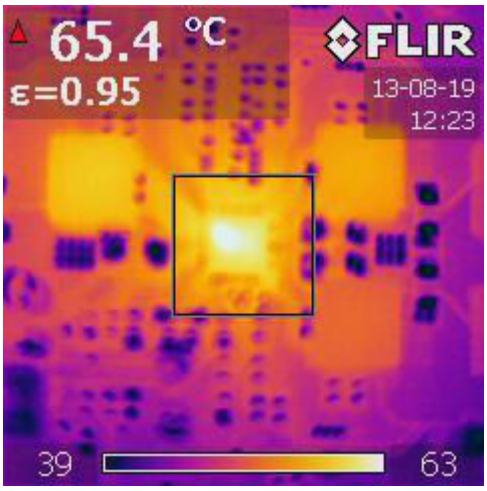


図 9-31. Automatic Power Sequencing, MODE = EN2 = HIGH, EN1 = LOW



Operating at VIN = 12 V, VOUT1 = 1.2 V / 1.5 A, VOUT2 = 1.8 V / 0.5 A, VOUT3 = 3.3 V / 0.5 A,
EVM Condition 4 Layers, 64 mm × 69 mm T_A = 30.5°C

図 9-32. Thermal Signature of TPS65262-1EVM



Operating at VIN = 12 V, VOUT1 = 1.2 V / 3 A, VOUT2 = 1.8 V / 1 A, VOUT3 = 3.3 V / 1 A,
EVM Condition 4 Layers, 64 mm × 69 mm T_A = 30.5°C

図 9-33. Thermal Signature of TPS65262-1EVM

9.3 Power Supply Recommendations

The devices are designed to operate from an input voltage supply range between 4.5 to 18 V. This input power supply must be well regulated. If the input supply is located more than a few inches from the TPS65262-1 converter, additional bulk capacitance can be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 47 µF is a typical choice.

9.4 Layout

9.4.1 Layout Guidelines

The TPS65262-1 supports a 2-layer PCB layout, shown in 図 9-34.

Layout is a critical portion of good power supply design. See 図 9-34 for a PCB layout example. The top contains the main power traces for VIN, VOUT, and LX. The top layer also has connections for the remaining pins of the TPS65262-1 and a large top-side area filled with ground. The top-layer ground area must be connected to the bottom-layer ground using vias at the input bypass capacitor, the output filter capacitor, and directly under the TPS65262-1 device to provide a thermal path from the exposed thermal pad land to ground. The bottom layer acts as a ground plane connecting analog ground and power ground.

For operation at full-rated load, the top-side ground area and bottom-side ground plane must provide adequate heat dissipating area. Several signals paths conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power supply's performance. To help eliminate these problems, the VIN pin must be bypassed to ground with a low-ESR ceramic bypass capacitor with X5R or X7R dielectric. Take care to minimize the loop area formed by the bypass capacitor connections, VIN pins, and ground connections. The VIN pin must also be bypassed to ground using a low-ESR ceramic capacitor with X5R or X7R dielectric.

Because the LX connection is the switching node, the output inductor must be located close to the LX pins, and the area of the PCB conductor minimized to prevent excessive capacitive coupling. The output filter capacitor ground must use the same power ground trace as the VIN input bypass capacitor. Try to minimize this conductor length while maintaining adequate width. The small signal components must be grounded to the analog ground path.

The FB and COMP pins are sensitive to noise so the resistors and capacitors must be located as close as possible to the IC and routed with minimal lengths of trace. The additional external components can be placed approximately as shown in 図 9-34.

9.4.2 Layout Example

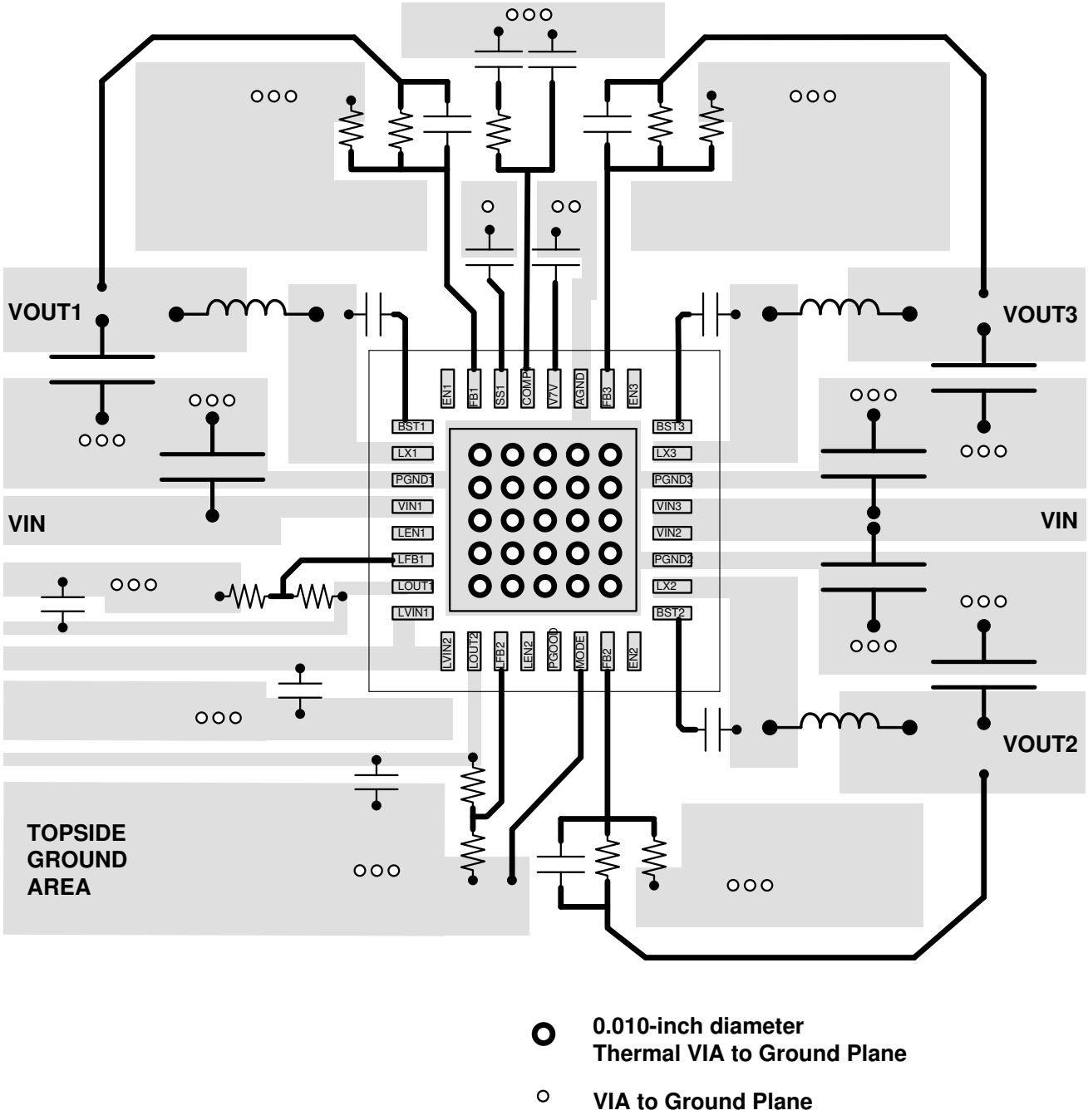


図 9-34. PCB Layout

10 Device and Documentation Support

10.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

10.2 サポート・リソース

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10.4 静電気放電に関する注意事項

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

10.5 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS65262-1RHBR	ACTIVE	VQFN	RHB	32	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 65262-1	Samples
TPS65262-1RHBT	ACTIVE	VQFN	RHB	32	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 65262-1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

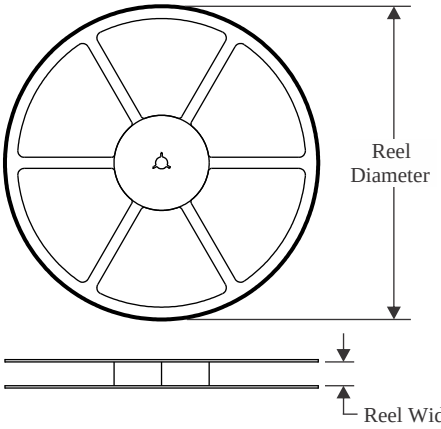
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

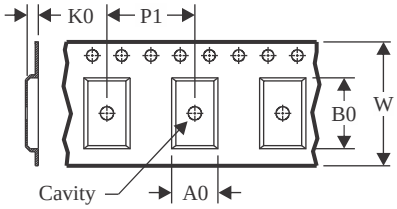
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

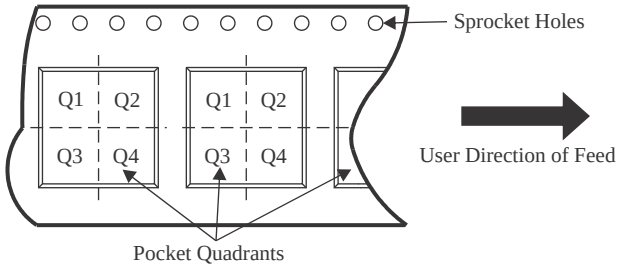


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

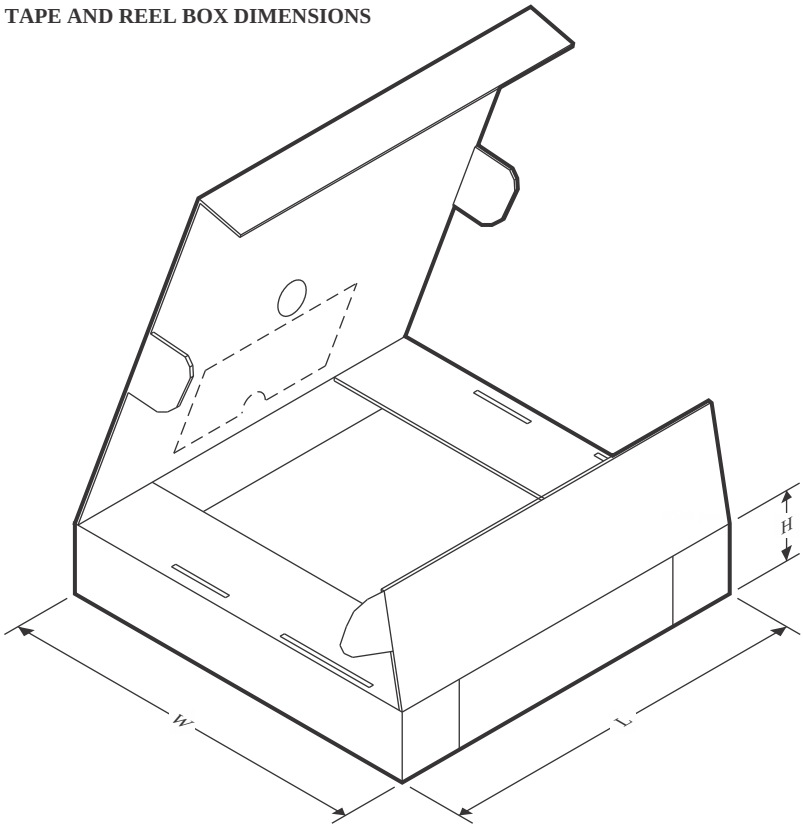
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65262-1RHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
TPS65262-1RHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
TPS65262-1RHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65262-1RHBR	VQFN	RHB	32	3000	346.0	346.0	33.0
TPS65262-1RHBT	VQFN	RHB	32	250	210.0	185.0	35.0
TPS65262-1RHBT	VQFN	RHB	32	250	210.0	185.0	35.0

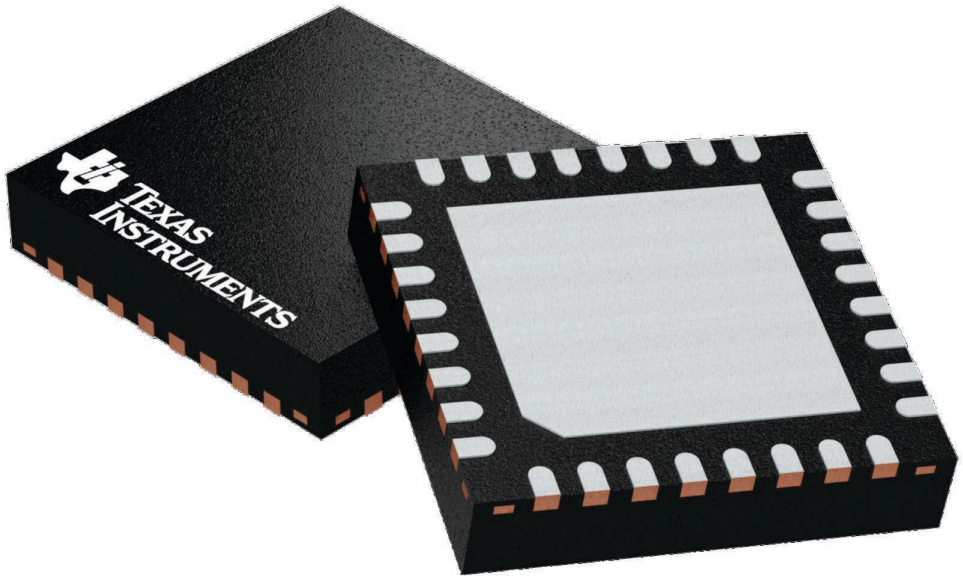
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

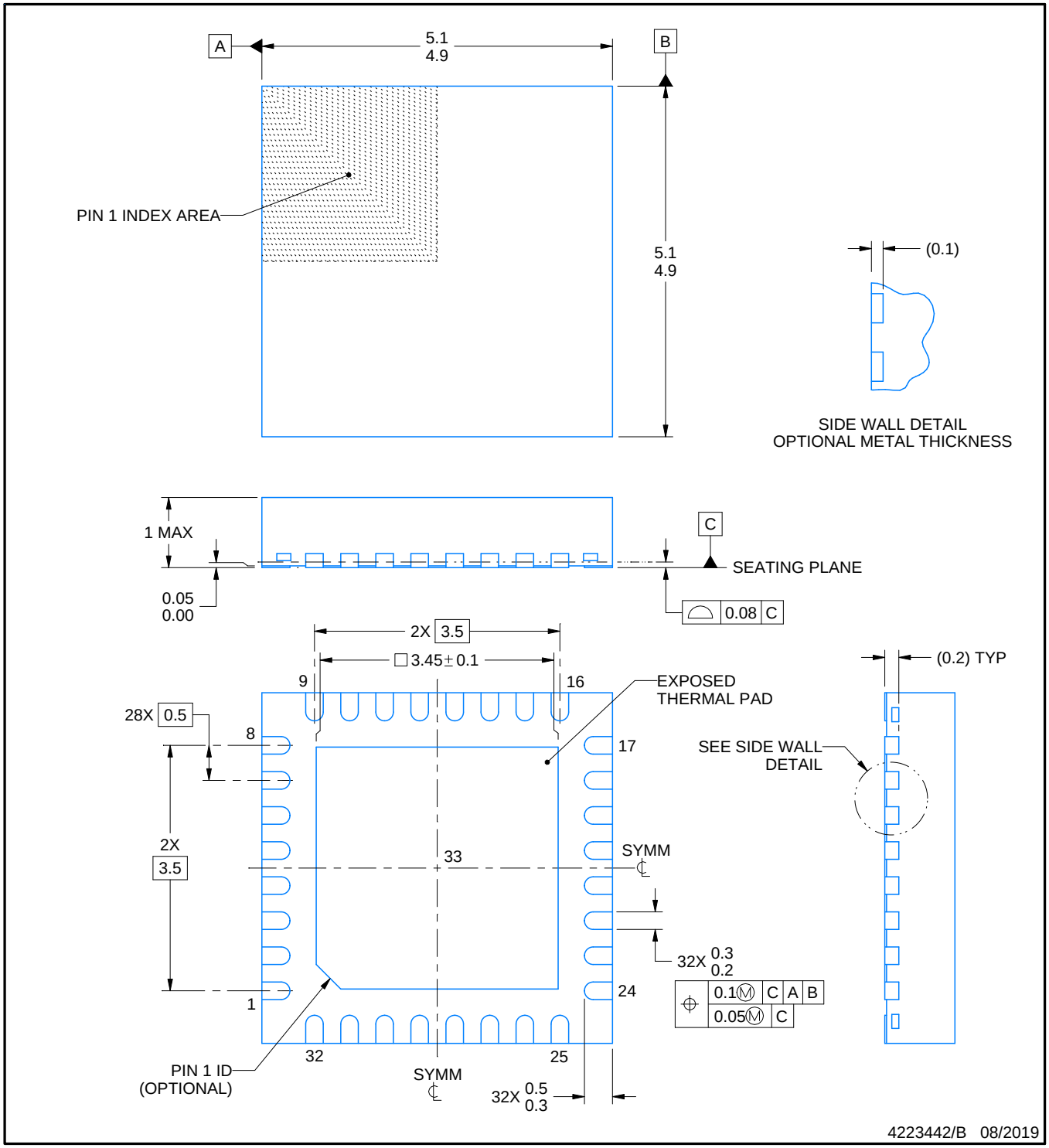
4224745/A

RHB0032E

PACKAGE OUTLINE

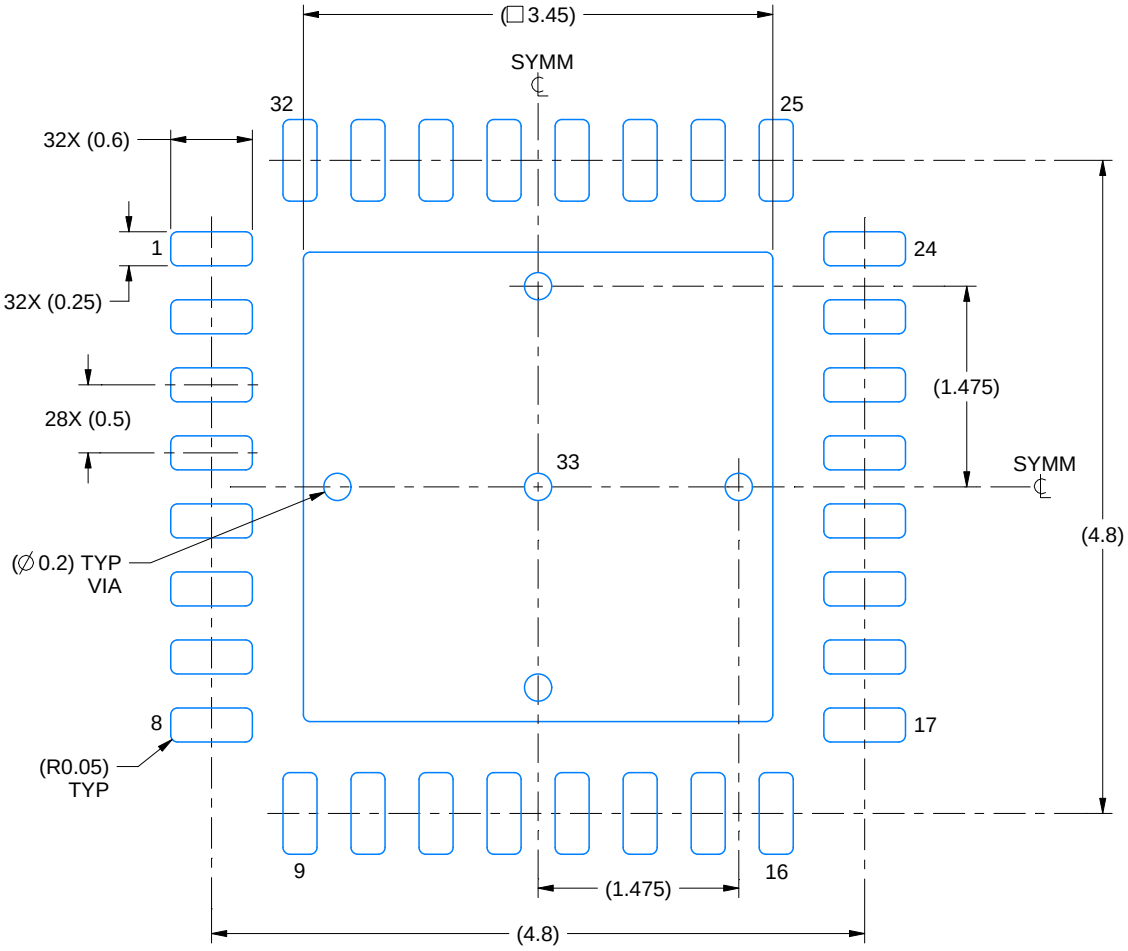
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

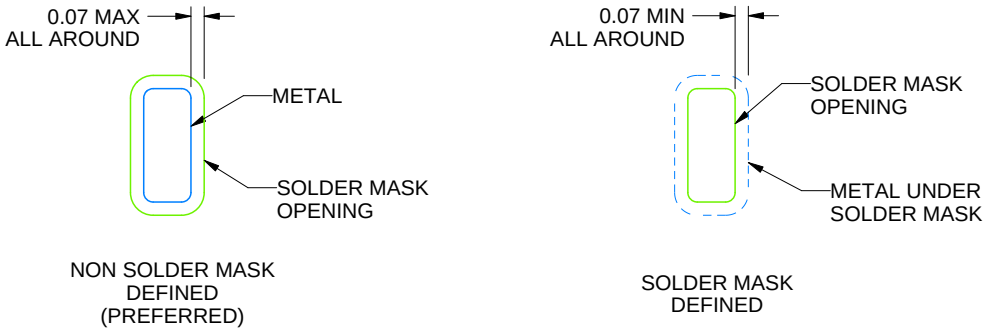


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:18X



SOLDER MASK DETAILS

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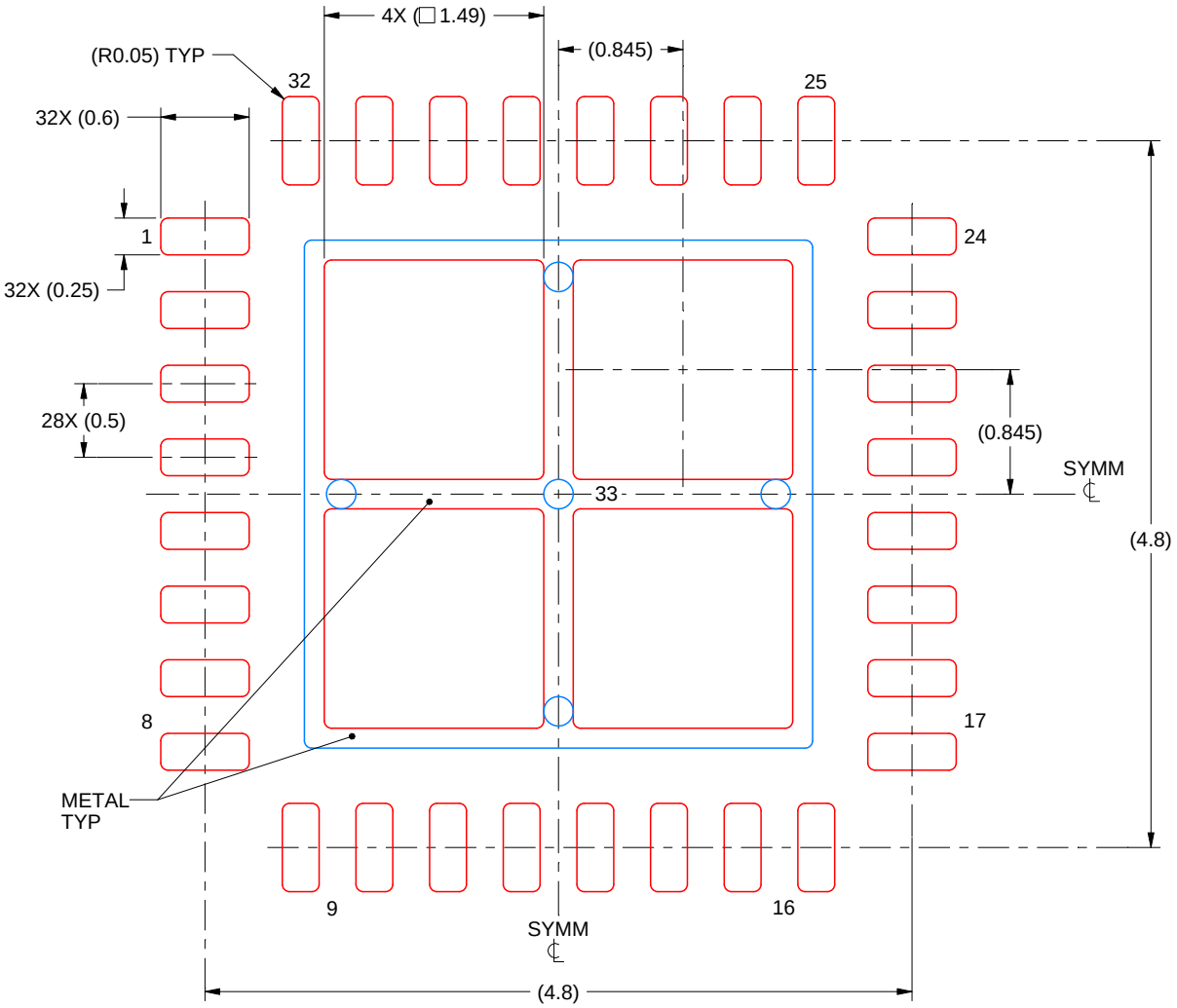
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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