TEXAS INSTRUMENTS

TPS923652, TPS923653, TPS923654, TPS923655
JAJSMG6A – APRIL 2023 – REVISED SEPTEMBER 2023

TPS92365x 65V 2A/4A 昇降圧 LED ドライバ、誘導性高速調光機能付き

1 特長

- 4.5V～65V の広い入力電圧範囲
- LED は、コモン・カソード接続に対応
- 150mΩ MOSFET を内蔵、代表値 3A/6.5A の電流制限機能搭載
- オプションのスイッチング周波数：100kHz～2.2MHz
- TPS923653 および TPS923655 の拡散スペクトラム
- 高度な調光オプション：
  - アナログ調光 (256：1)
  - 高速 PWM 調光 (パルス幅 150ns)
  - ハイブリッドで柔軟な調光 (20kHz PWM で 2,000：1、4kHz PWM で 10,000：1、120Hz PWM で 1,000,000：1)
- CC/CV 充電モード
- 包括的な保護機能を搭載：
  - LED の断線 / 短絡保護
  - スイッチング FET の断線 / 短絡保護
  - 外部部品の障害保護
  - サイクル単位の電流制限
  - サーマル・シャットダウン
  - フォルト出力 (オープン・ドレイン)
- サーマル・フォールドバック曲線を設定可能
- VSON、WSON、SOT23 パッケージ・オプション

2 アプリケーション

- 常時照明：
  - 屋内、屋外、職業上の照明
  - 医療用 / 外科用照明
  - プロジェクタ、レーザー TV、プリンタ、IP カメラ
- 瞬間照明：
  - マシン・ビジョン、カメラ・フラッシュ
  - 火災報知器、ストロボ
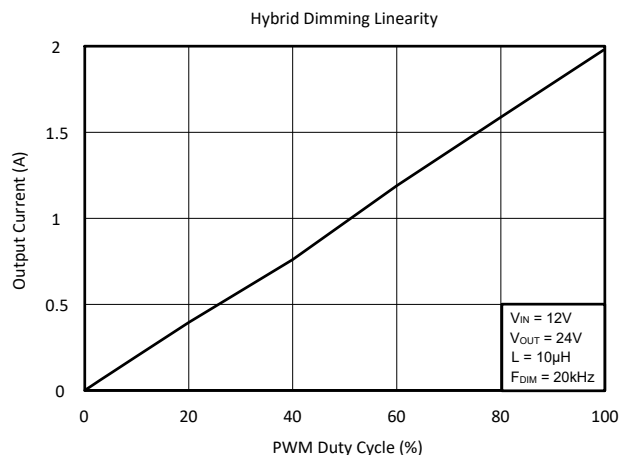- CC と CV ソース：
  - LCD バックライト
  - バッテリ充電
  - TEC 制御
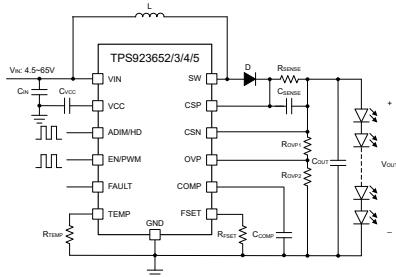
3 概要

TPS92365x ファミリは、2A/4A 非同期整流昇降圧 LED ドライバで、4.5V～65V の広い入力電圧範囲に対応しています。ローサイド NMOS スイッチを内蔵することにより、このデバイスは LED を駆動できるだけでなく、高電力密度および高効率でバッテリを充電することができます。また、このファミリは、コモン・カソード接続および単層 PCB 設計もサポートしています。スイッチング周波数は 100kHz ～2.2MHz で構成可能で、オプションのスペクトラム拡散機能により EMI 性能が向上します。

TPS92365x ファミリは、アナログ、PWM、ハイブリッド、フレキシブル調光を含む 4 つの調光オプションをサポートしています。各調光方法は、PWM および ADIM 入力ピン通して単純な High 信号と Low 信号によって構成できます。このファミリは、適応型オフ時間電流モード制御とスマートで正確なサンプリングを採用して、誘導性高速調光 (IFD) を可能にし、高い調光精度を実現します。

TPS92365x ファミリは、LED の断線と短絡、センス抵抗の開放と短絡、構成可能なサーマル・フォールドバック、サーマル・シャットダウンなど、複数の系統的な保護機能も提供します。フォルト出力は、フォルト状態が検出されるとすぐにアクノリッジ信号を送信します。

製品情報

部品番号	パッケージ	本体サイズ (公称)
TPS92365x	VSON (14)	4.5mm × 3.0mm
	WSON (12)	3.0mm × 3.0mm
TPS923652、TPS923653	SOT-23-THN (14)	4.2mm × 3.3mm

概略回路図

LED 輝度の直線性

English Data Sheet: SLVSGH1

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4 Revision History

Changes from Revision * (June 2023) to Revision A (September 2023)   **Page**

- ドキュメントを「事前情報」から「量産データ」に更新...1

5 Device Comparison Table

Part Number	Package	Typical Current Limit	Spread Spectrum	Operation Junction Temperature
TPS923652DMTR	VSON (14)	3 A	Disabled	-40 °C to 125 °C
TPS923652DRRR	WSON (12)	3 A	Disabled	-40 °C to 125 °C
TPS923652DYYR	SOT-23-THN (14)	3 A	Disabled	-40 °C to 125 °C
TPS923653DMTR	VSON (14)	3 A	Enabled	-40 °C to 125 °C
TPS923653DRRR	WSON (12)	3 A	Enabled	-40 °C to 125 °C
TPS923653DYYR	SOT-23-THN (14)	3 A	Enabled	-40 °C to 125 °C
TPS923654DMTR	VSON (14)	6.5 A	Disabled	-40 °C to 125 °C
TPS923654DRRR	WSON (12)	6.5 A	Disabled	-40 °C to 125 °C
TPS923654MDMTR	VSON (14)	6.5 A	Disabled	-55 °C to 125 °C
TPS923654HMDMTR	VSON (14)	8.5 A	Disabled	-55 °C to 125 °C
TPS923655DMTR	VSON (14)	6.5 A	Enabled	-40 °C to 125 °C
TPS923655DRRR	WSON (12)	6.5 A	Enabled	-40 °C to 125 °C
TPS923655MDMTR	VSON (14)	6.5 A	Enabled	-55 °C to 125 °C
TPS923655HMDMTR	VSON (14)	8.5 A	Enabled	-55 °C to 125 °C

資料に関するフィードバック(ご意見やお問い合わせ) を送信   3

Product Folder Links: *TPS923652 TPS923653 TPS923654 TPS923655*

English Data Sheet: SLVSGH1

6 Pin Configuration and Functions

PGND — 1	14 — SW
AGND — 2	13 — CSP
VIN — 3	12 — CSN
VCC — 4	11 — OVP
ADIM/HD — 5	10 — COMP
EN/PWM — 6	9 — FSET
FAULT — 7	8 — TEMP

Thermal Pad

図 6-1. 14-Pin VSON Top View

VIN — 1	12 — SW
VCC — 2	11 — CSP
ADIM/HD — 3	10 — CSN
EN/PWM — 4	9 — OVP
FAULT — 5	8 — COMP
TEMP — 6	7 — FSET

Thermal Pad
(PGND/AGND)

図 6-2. 12-Pin WSON Top View

PGND — 1	14 — SW
AGND — 2	13 — CSP
VIN — 3	12 — CSN
VCC — 4	11 — OVP
ADIM/HD — 5	10 — COMP
EN/PWM — 6	9 — FSET
FAULT — 7	8 — TEMP
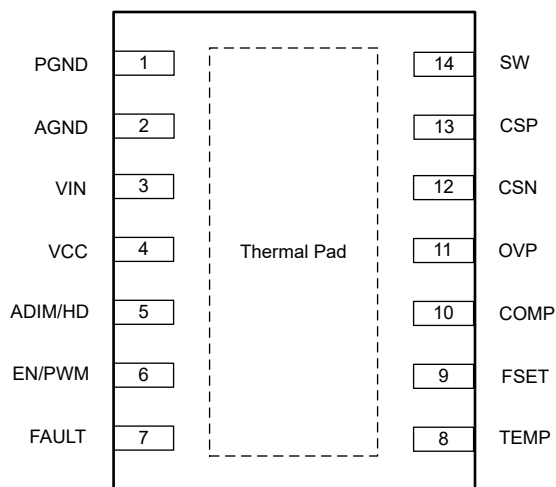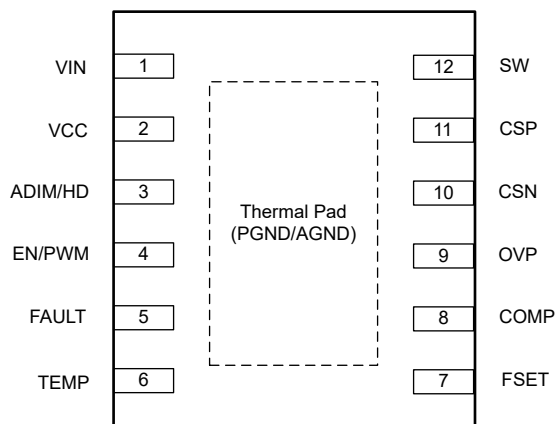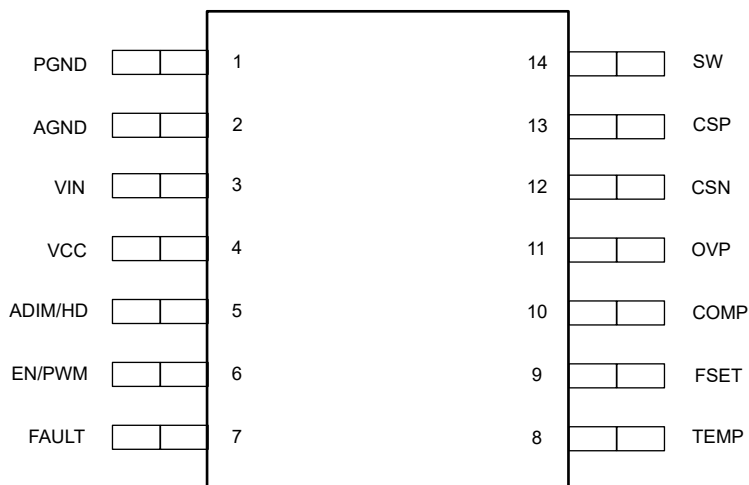
図 6-3. 14-Pin SOT-23-THIN Top View

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Product Folder Links: *TPS923652 TPS923653 TPS923654 TPS923655*

English Data Sheet: SLVSGH1

表 6-1. Pin Functions

PIN				TYPE[1]	DESCRIPTION
NAME	SOT23-14	VSON-14	WSON-12		
PGND	1	1	Thermal Pad	G	Power ground pin.
AGND	2	2	Thermal Pad	G	Analog ground pin.
VIN	3	3	1	P	Input power pin.
VCC	4	4	2	P	Internal LDO output pin. Connect with a 10-V, 1-µF capacitor to AGND.
ADIM/HD	5	5	3	I	Analog dimming or hybrid dimming pin. Pull high for PWM dimming only, pull low for hybrid dimming, input PWM signal for analog dimming.
EN/PWM	6	6	4	I	Enable pin or PWM dimming pin. Pull high for always on, pull low for disabling the device, input PWM signal for PWM dimming.
FAULT	7	7	5	O	Open drain output pin. Pull low when fault is detected.
TEMP	8	8	6	I/O	Thermal foldback pin. Put different resistor values to AGND to set different thermal foldback behavior curves.
FSET	9	9	7	I/O	Switching frequency set pin, with range of 100 kHz to 2.2 MHz. Put different resistor values to AGND for different switching frequencies.
COMP	10	10	8	I/O	Error-amilifier output pin. Connect capacitors to AGND. Different capacitor values determine different softstart times and bandwidths.
OVP	11	11	9	I	Overvoltage detection pin. Put different resistor dividers to set the LED open detection thresholds.
CSN	12	12	10	I	LED current sense positive pin.
CSP	13	13	11	I	LED current sense negative pin.
SW	14	14	12	P	Switching node pin. Internally connected to the low-side MOSFET. Connect with the power inductor and the schottky diode.
Thermal Pad	N/A	Y	Y	G	Power/analog ground pin for WSON-12 package.

(1)   I = Input, O = Output, P = Supply, G = Ground

Product Folder Links: *TPS923652 TPS923653 TPS923654 TPS923655*

English Data Sheet: SLVSGH1

7 Specifications

7.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Voltage on pins	VIN, OVP, CSP, CSN, SW	−0.3	65	V
Voltage on pins	VCC, ADIM/HD, EN/PWM, FAULT, TEMP, FSET, COMP	−0.3	5.5	V
Operation junction temperature	T_J	−40	125	°C
Operation junction temperature (TPS923654MDMTR, TPS923654HMDMTR, TPS923655MDMTR, TPS923655HMDMTR)	T_J	−55	125	°C
Storage temperature	T_{stg}	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Theseare stress ratings only, which do not imply functional operation of the device at these or anyother conditions beyond those indicated under *Recommended OperatingConditions*. Exposure to absolute-maximum-rated conditions for extended periods mayaffect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safemanufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safemanufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Input voltage range	VIN	4.5	63	V
Input voltage range	OVP, CSP, CSN	0	63	V
Input voltage range	VCC, ADIM/HD, EN/PWM, TEMP, FSET	0	5	V
Output voltage range	SW	0	63	V
	FAULT, COMP	0	5	V
Operation junction temperature	T_J	−40	125	°C
Operation junction temperature (TPS923654MDMTR, TPS923654HMDMTR, TPS923655MDMTR, TPS923655HMDMTR)	T_J	−55	125	°C

7.4 Thermal Information

THERMAL METRIC[1]		TPS92365x SOT 14 PINS	TPS92365x WSON 12 PINS	TPS92365x VSON 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	96.0	47.4	39.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	33.5	44.2	39.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	33.1	19.7	14.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.7	1.0	0.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	32.9	19.7	14.7	°C/W

(1) For more information about traditional and new thermalmetrics, see the *Semiconductor and IC Package Thermal Metrics*application report, SPRA953.

Product Folder Links: *TPS923652 TPS923653 TPS923654 TPS923655*

English Data Sheet: SLVSGH1

7.5 Electrical Characteristics

The electrical ratings specified in this section apply to all specifications in this document, unless otherwise noted. These specifications are interpreted as conditions that do not degrade the device parametric or functional specifications for the life of the product containingit. T_J = –40°C to +125°C, V_{IN} = 4.5 V to 60 V, (unlessotherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY						
V_{VIN_UVLO}	V_{IN} undervoltage lockout	Rising V_{IN}	3.0	3.2	3.4	V
		Falling V_{IN}	2.8	3.0	3.2	V
	Hysteresis			0.2		V
I_{SD}	Shut down current from V_{IN}	V_{IN} = 12 V, $V_{EN/PWM}$ = 0 V, device disabled		0.8	2.3	µA
I_{OFF}	PWM off quiesent current from V_{IN}	V_{IN} = 12 V, $V_{EN/PWM}$ = 0 V, device enabled		2.5		mA
I_{OP}	Normal operating current	400-kHz switching frequency		4.6		mA
I_{OP}	Normal operating current	2.2-MHz switching frequency		10.0		mA
V_{VCC}	Internal LDO output voltage	I_{VCC} = 10 mA	5.0	5.15	5.3	V
I_{VCC_LIM}	Internal LDO output current limit		38	47	56	mA
DIMMING						
V_{PWM_L}	Low-level input voltage				0.4	V
V_{PWM_H}	High-level input voltage		1.2			V
V_{ADIM_L}	Low-level input voltage				0.4	V
V_{ADIM_H}	High-level input voltage		1.2			V
$t_{PWM\_OUT\_ON}$	PWM output minimum on time				150	ns
$t_{PWM\_IN\_ON}$	PWM input minimum on time				150	ns
$t_{PWM\_IN\_OFF}$	PWM input minimum off time to disable device		57		77	ms
f_{ADIM}	Analog Dimming input frequency	6-bit ADIM resolution	0.1		156	kHz
f_{ADIM}	Analog Dimming input frequency	8-bit ADIM resolution	0.1		39	kHz
FAULT						
V_{OL}	Output level low	I = 3 mA			0.1	V
$I_{LEAKAGE}$	Output leakage current	V = 5 V			1	µA
FEEDBACK AND ERROR AMPLIFIER						
$g_{M(ea)}$	Transconductance gain	ADIM 100% duty cycle, $V_{CSP-CSN}$ = 200 mV, V_{COMP} = 1.5 V	205	265	325	µA/V
I_{COMP}	Source/sink current	ADIM 100% duty cycle, $V_{CSP-CSN}$ = 200 mV ± 200 mV, V_{COMP} = 1.5 V	±24	±40	±56	µA
$V_{CSP-CSN}$	Current sense threshold	ADIM 100% duty cycle	194	200	206	mV
$V_{CSP-CSN}$	Current sense threshold	ADIM 12.5% duty cycle, compared with 100% duty cycle	11.875	12.5	13.125	%
$V_{CSP-CSN}$	Current sense threshold	ADIM 1.17% duty cycle, compared with 100% duty cycle	0.82	1.17	1.52	%
POWER STAGE						
R_{DSON}	Switching FET on resistance	V_{IN} ≥ 5 V		150		mΩ
t_{min_ON}	Switching FET minimum on time			100		ns
t_{min_OFF}	Switching FET minimum off time			100		ns
f_{SW}	Switching FET frequency		0.1		2.2	MHz
CURRENT LIMIT						
I_{LIM}	Switching FET cycle-by-cycle current limit (TPS923652, TPS923653)		2.6	3	3.6	A
I_{LIM}	Switching FET cycle-by-cycle current limit (TPS923654, TPS923655)		5.8	6.5	7.6	A
I_{LIM}	Switching FET cycle-by-cycle current limit (TPS923654HMDMTR, TPS923655HMDMTR)		7.1	8.5	9.6	A
THERMAL PROTECTION						
T_{th}	Thermal foldback starting temperature threshold	R_{TEMP} = 20 kΩ		130		°C

The electrical ratings specified in this section apply to all specifications in this document, unless otherwise noted. These specifications are interpreted as conditions that do not degrade the device parametric or functional specifications for the life of the product containingit. T_J = –40°C to +125°C, V_{IN} = 4.5 V to 60 V, (unlessotherwise noted).

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{TSD}	Thermal shutdown temperature			165		°C
	Hysteresis			15		°C

Product Folder Links: *TPS923652 TPS923653 TPS923654 TPS923655*

English Data Sheet: SLVSGH1

7.6 Typical Characteristics

V_{IN} = 12 V, I_{OUT} = 1 A, LED count = 12, L = 10 µH, F_{SW} = 400 kHz, unless otherwise specified
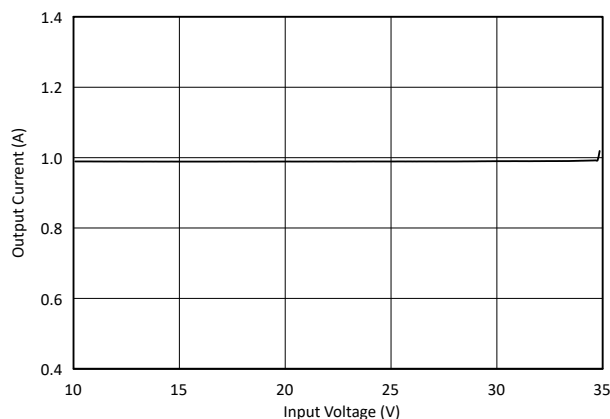
図 7-1. Output Current vs. Input Voltage
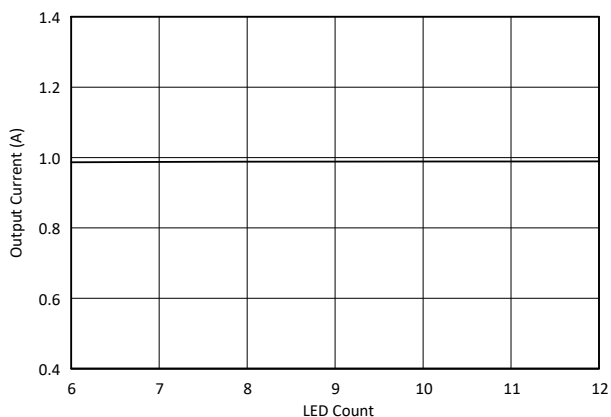
図 7-2. Output Current vs. LED Count
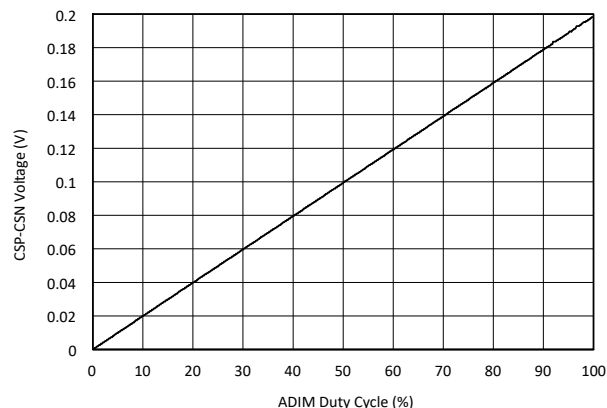
図 7-3. ADIM Duty Cycle vs. CSP-CSN Voltage in Analog Dimming
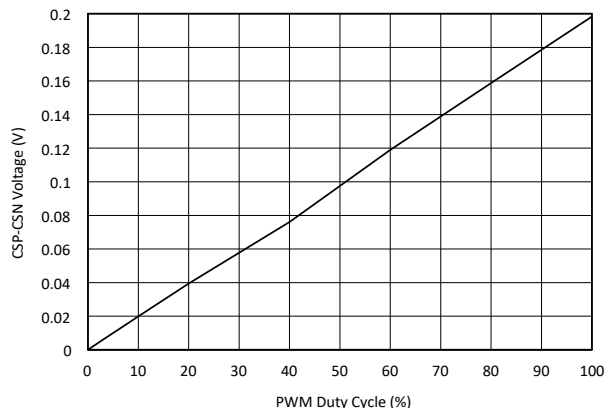
図 7-4. PWM Duty Cycle vs. CSP-CSN Voltage in 20-kHz Hybrid Dimming
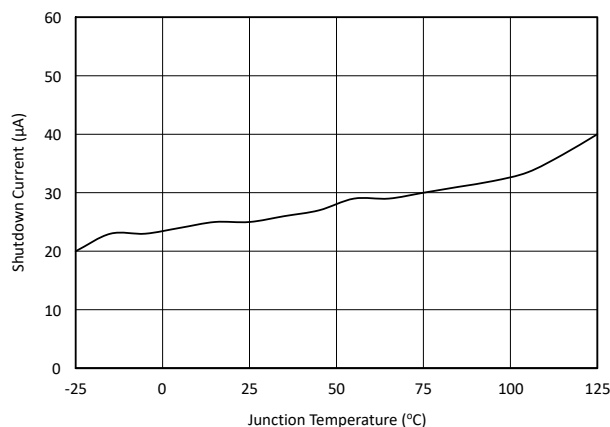
図 7-5. Shutdown Current vs. Junction Temperature
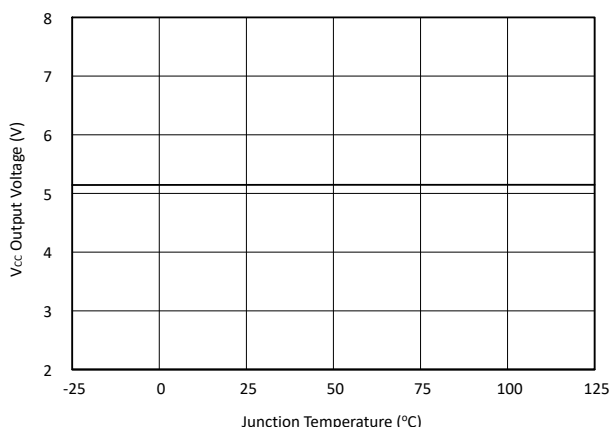
図 7-6. Internal LDO Output vs. Junction Temperature

7.6 Typical Characteristics (続き)
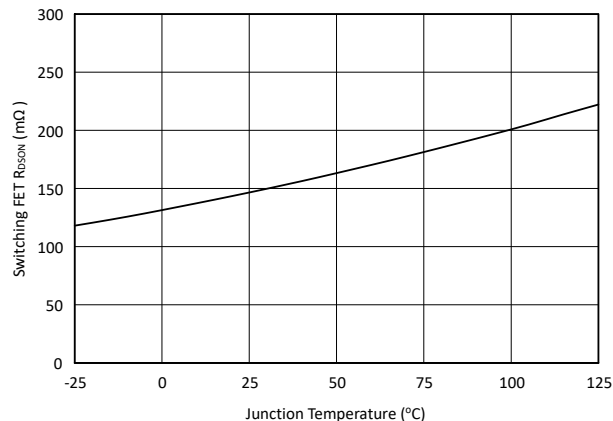
図 7-7. Switching FET R$_{DSON}$ vs. Junction Temperature
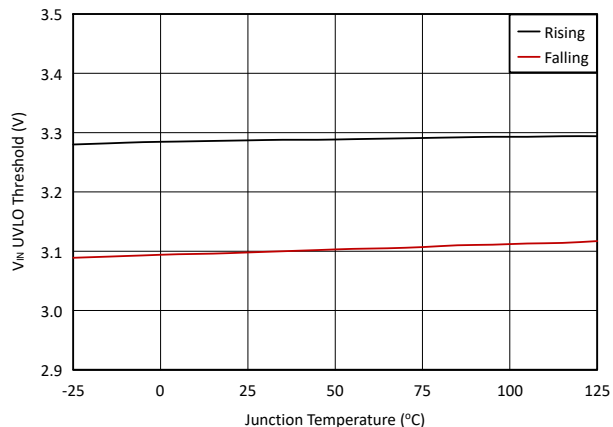
図 7-8. VIN UVLO Threshold vs. Junction Temperature
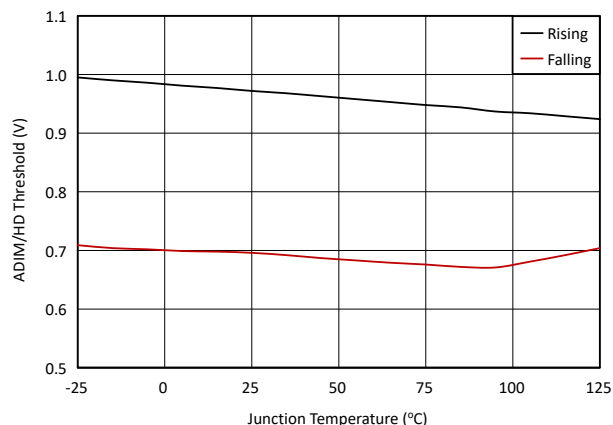
図 7-9. ADIM/HD Threshold vs. Junction Temperature
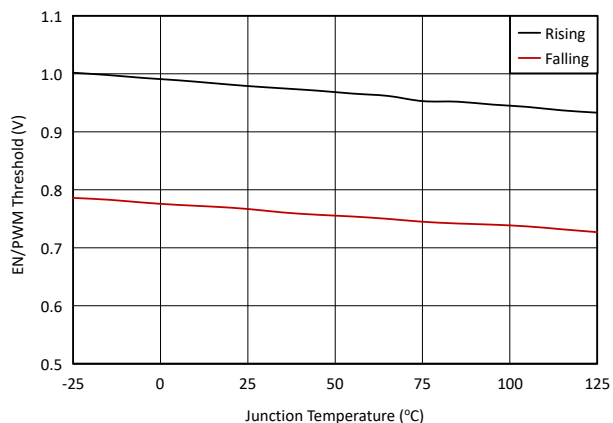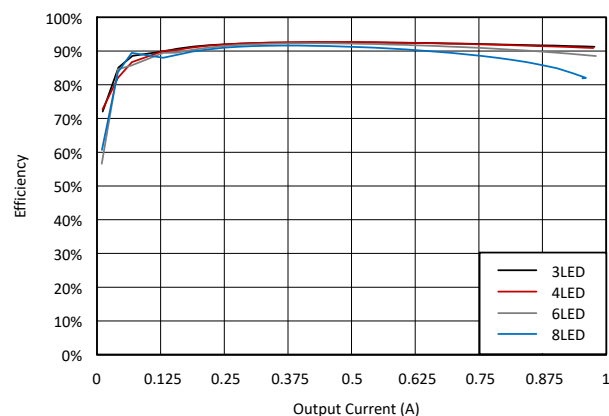

図 7-10. EN/PWM Threshold vs. Junction Temperature

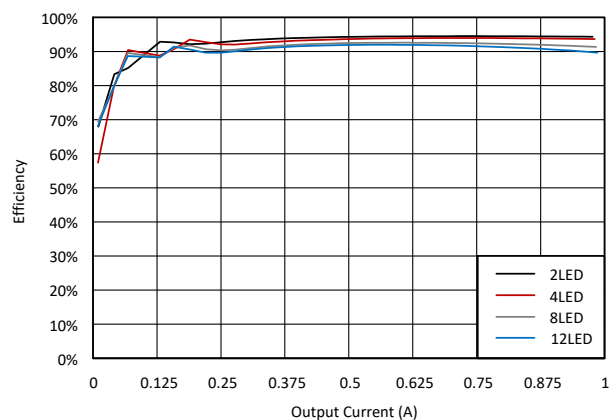図 7-11. Efficiency at 7-V Input Voltage, 1-A Output Current

図 7-12. Efficiency at 13-V Input Voltage, 1-A Output Current

English Data Sheet: SLVSGH1

8 Detailed Description

8.1 Overview

The TPS92365x family is a 2-A / 4-A non-synchronous Boost / Buck-Boost LED driver with 4.5-V to 65-V wide input range. By integrating the low-side NMOS switch with constant current and constant voltage controls, the device is capable of not only driving LEDs but also charging batteries with high power density and high efficiency. The device also supports common cathode connection and single layer PCB design, hence saving cost of connector, harness and PCB. The switching frequency is configurable through FSET pin, ranging from 100 kHz to 2.2 MHz, with optional spread spectrum feature to decrease the EMC emission and reduce the input filter size.

The device supports four dimming options, including analog dimming, PWM dimming, hybrid dimming and flexible dimming. Each dimming method can be configured through the PWM and ADIM input pins by means of simple high/low sequencing signals at startup. In PWM dimming mode, once the dimming mode is configured, LED is turned on and off corresponding to on and off of the PWM input signal at PWM input pin. The PWM dimming mode supports ultra-narrow pulse width down to 150 ns. In analog dimming mode, LED current is regulated corresponding to the pulse width duty cycle of the PWM input signal at ADIM input pin. In hybrid dimming mode, the LED current is controlled by a pre-determined combination of analog dimming and PWM dimming through the PWM input signal at PWM input pin. In flexible dimming mode, the LED current is controlled by analog dimming through the PWM input signal at ADIM input pins and PWM dimming through the PWM input signal at PWM input pins, respectively. The device adopts an adaptive off-time current mode control along with smart and accurate sampling to enable Inductive Fast Dimming (IFD) and achieve high dimming accuracy. The compensation bandwidth can be adjusted through an external capacitor based on system requirement.

For safety and protection, the devices support full systematic protections including LED open and short, sense resistor open and short, configurable thermal foldback and thermal shutdown protection. The fault output pin sends out acknowledge signals as soon as any fault condition is detected.

8.2 Functional Block Diagram
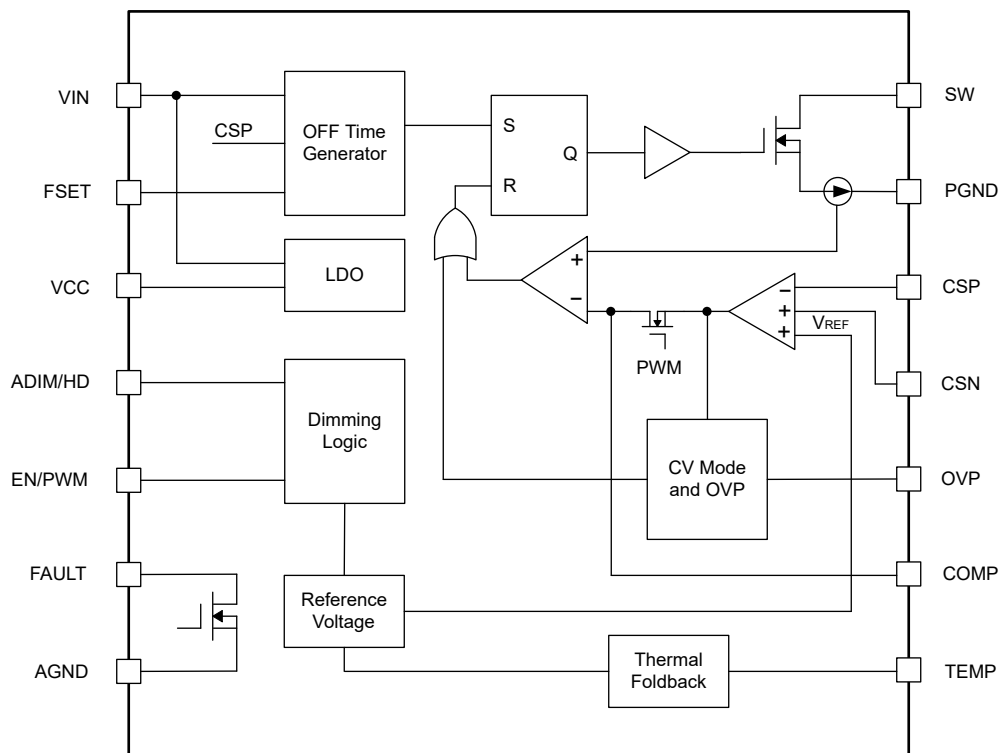
8.3 Feature Description

8.3.1 Adaptive Off-Time Current Mode Control

The TPS92365x device adopts an adaptive off-time current mode control to support fast transient response over a wide range of operation. The switching frequency is configurable through FSET pin, ranging from 100 kHz to 2.2 MHz.

For average output current regulation, the sensed voltage across the sensing resistor between the CSP and CSN pins is compared with the internal voltage reference, V_{REF} , through the error amplifier. The output of the error amplifier, V_{COMP}, passes through an external compensation network and is then compared with the peak current feedback at the PWM comparator. During each switching cycle, when the internal NMOS FET is turned on, the peak currernt is sensed through the internal FET. When the sensed value of peak current reaches V_{COMP} at the input of PWM comparator, the NMOS FET is turned off and the adaptive off-time counter starts counting. Once the adaptive off-time counter stops counting, the counter is reset until when the NMOS FET stays off. The counting off time is determined by the external resistor connected to the FSET pin and the input/output feedforward. Thus, the device is able to maintain a nearly constant switching frequnecy at steady state and regulate the output average current at a desired value.
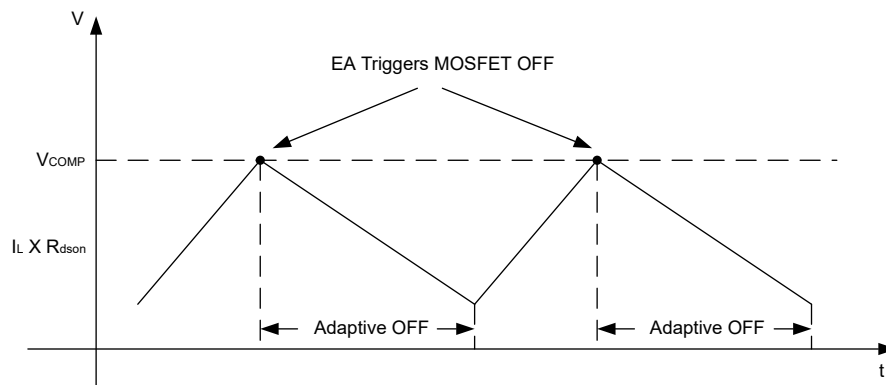

図 8-1. Adaptive off-time current mode control method

8.3.1.1 Switching Frequency Settings

The switching frequency of TPS92365x device is adjustable from 100 kHz to 2.2 MHz by means of changing R_{FSET} connected between FSET pin and AGND. The default switching frequency is 100 kHz when the FSET pin is connected to nothing.

The resistor value and the corresponding switching frequency are listed in the below table:

表 8-1. Switching Frequency vs. R_{FSET} Resistor Value

Switching Frequency	Resistor Value (kΩ)
100 kHz	232
200 kHz	138
300 kHz	83
400 kHz	59
600 kHz	38
800 kHz	28
1 MHz	23
1.2 MHz	18
1.5 MHz	13
1.8 MHz	11

Product Folder Links: *TPS923652 TPS923653 TPS923654 TPS923655*

English Data Sheet: SLVSGH1

表 8-1. Switching Frequency vs. R$_{FSET}$ Resistor Value (続き)

2.2 MHz	9

For example, if R$_{FSET}$ is set to 59 kΩ, the corresponding switching frequency is set to 400 kHz.

In most cases, the lower switching frequency, the higher system efficiency and the better thermal behavior.

8.3.1.2 Spread Spectrum

The TPS923653 and TPS923655 devices enable the spread spectrum feature (±7% from central frequency, 2-kHz modulation frequency) which reduces EMI noise at the switching frequency and its high-order harmonics.

On the other hand, the TPS923652 and TPS923654 devices disable the spread spectrum feature toward better brightness performance in low brightness scenario.

8.3.2 Setting LED Current

The LED current is set by the external sensing resistor between CSP and CSN pins. The internal voltage reference, V$_{REF}$, is fixed at 200 mV for full-scale LED current, I$_{LED\_FS}$, and the sensing resistor can be calculated using 式 1.

$$R_{SENSE} = \frac{V_{REF}}{I_{LED\_FS}} \qquad\qquad (1)$$

where

* V$_{REF}$ = 200 mV

8.3.3 Undervoltage Lockout

The TPS92365x family implements an internal undervoltage-lockout (UVLO) circuitry connecting to the VCC pin. The UVLO is triggered and then the device is disabled when the VCC pin voltage falls below the internal UVLO threshold voltage, V$_{VIN\_UVLO}$ typically 3.0 V, with a typical 0.2-V hysteresis. The VCC pin is the output of an internal regulator of which the input is supplied by the VIN pin. Therefore, if VIN pin voltage falls close to above the V$_{VIN\_UVLO}$ (around 500 mV above), the UVLO will be triggered.

8.3.4 Internal Soft Start

The TPS92365x family implements the internal soft-start function. Once V$_{IN}$ rises above V$_{VIN\_MIN}$, the internal LDO starts to charge V$_{CC}$ capacitor. It takes approximately 800 µs for V$_{CC}$ to rise above V$_{VIN\_UVLO}$ if a 1-µF capacitor is connected to V$_{CC}$ pin. If EN/PWM pin is pulled high before V$_{CC}$ rises above V$_{VIN\_UVLO}$, the POR is enabled right after V$_{CC}$ above V$_{VIN\_UVLO}$ and waits for 100 µs to start dimming mode. EN/PWM pin has to stay high for more than 5 µs after V$_{CC}$ rises above V$_{VIN\_UVLO}$. In this case, if using 1-µF V$_{CC}$ capacitor, it is recommended to wait for 1 ms to start dimming mode after V$_{IN}$ rises above V$_{VIN\_MIN}$.

If EN/PWM pin has the first PWM pulse appearing after V$_{CC}$ rises above V$_{VIN\_UVLO}$, the device waits for 200 µs to enable POR and another 100 µs to start dimming mode. Hence, without triggering V$_{IN}$ UVLO, the device can be renabled after disabled and waits for 300 µs to start dimming mode. Note that the initial enable PWM pulse lasting more than 5 µs is required at EN/PWM input pin to enable the device. After dimming mode is started, the device enters four different dimming modes based on the configuration of ADIM/HD pin and EN/PWM pin.
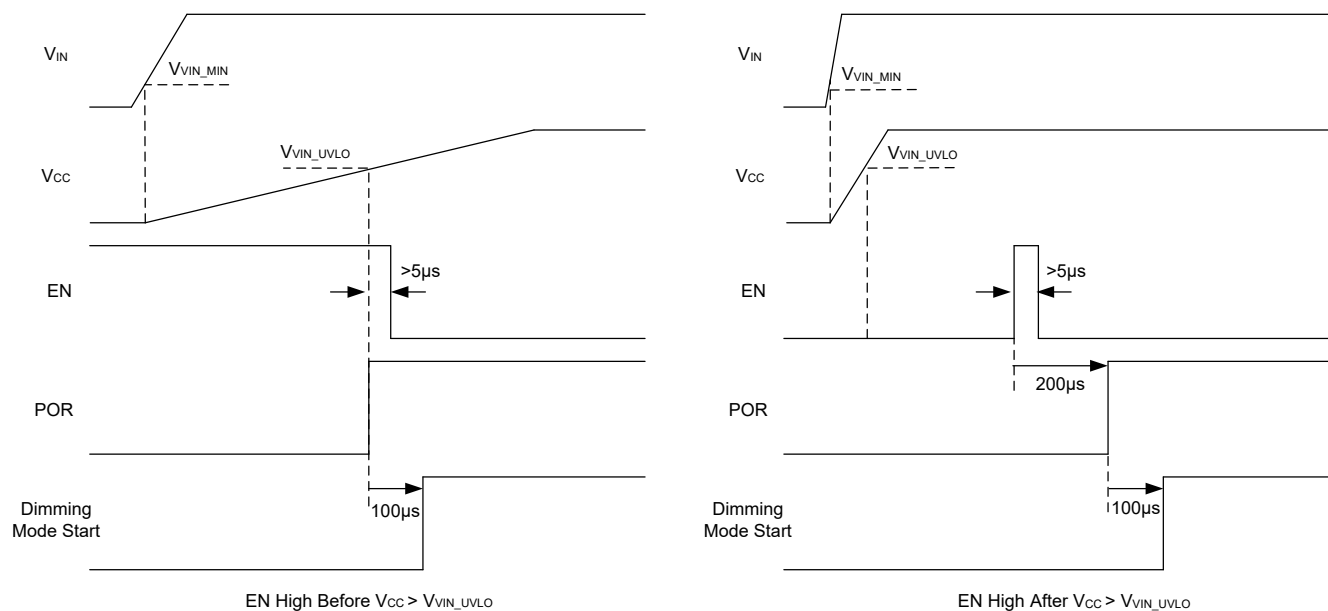
| EN High Before V_{CC} > V_{VIN_UVLO} | EN High After V_{CC} > V_{VIN_UVLO} |

図 8-2. Startup Sequence

8.3.5 Dimming Mode

The TPS92365x family has four optional dimming modes:

- PWM dimming
- Analog dimming
- Hybrid dimming
- Flexible dimming

The dimming mode is started either 1 ms after V_{IN} exits UVLO or 300 µs after renable by EN/PWM pin. The configuration to one of the four dimming modes are shown as below

表 8-2. Dimming Mode Configuration

Dimming Mode	EN/PWM Pin	ADIM/HD Pin
PWM Dimming	PWM signal	High
Analog Dimming	High	PWM signal
Hybrid Dimming	PWM signal	Low
Flexible Dimming	PWM signal	PWM signal

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English Data Sheet: SLVSGH1

8.3.5.1 PWM Dimming

The TPS92365x family supports PWM input signals with ultra-narrow pulse width down to 150 ns for direct PWM dimming. The PWM dimming mode is enabled when the ADIM/HD input pin is always high and the EN/PWM input pin is configured by a PWM input signal.

In PWM dimming mode, when the PWM input signal at the PWM pin turns from low to high, the internal NMOS FET starts switching and the inductor current rises to the determined value. The LED current is then regulated at the determined value as long as the PWM input signal stays high. When the PWM input signal turns from high to low, the internal FET is turned off causing the inductor current falling to zero. The internal FET maintains off and the LED current stays zero as long as the PWM input signal stays low.

8.3.5.2 Analog Dimming

The TPS92365x family supports analog dimming which regulates the LED current through the PWM input signal at the ADIM/HD pin. The analog dimming mode is enabled when the EN/PWM pin is always high and the ADIM/HD pin is configured by a PWM input signal.

The internal voltage reference, V_{REF}, starts to rise after the first PWM pulse appears at the ADIM/HD pin. A 1-μs minimum on-time of the first PWM pulse is required for the internal digital circuits to enter the analog dimming mode. V_{REF} continues to increase until the end of second PWM cycle and then changes to the desired value in proportion to the duty cycle of the PWM pulse. The minimum on-time of the PWM pulse after the first is 100 ns for the digital circuits to detect the duty cycle.

V_{REF} is 200 mV when the PWM input signal at the ADIM/HD pin has a 100% duty cycle, for instance, and V_{REF} is 20 mV when the PWM input signal has a 10% duty cycle. The initial change takes approximately 5 ms if V_{REF} is 200 mV. The analog dimming enables 8-bit resolution which corresponds to 0.4% duty cycle step change at the ADIM/HD pin. Also, the circuit is able to respond to the duty cycle change of the PWM input signal with tens of micro-seconds delay.

8.3.5.3 Hybrid Dimming

The TPS92365x family supports a unique hybid dimming function to maximize the dimming performance, especially when both high dimming frequency and high dimming ratio are needed. The hybrid dimming mode is enabled when the ADIM/HD pin is always low and the EN/PWM pin is configured by a PWM input signal.

In the hybrid dimming mode, the LED current is regulated by the analog dimming at high brightness level (12.5% to 100%) and by the PWM dimming at low brightness level (0% to 12.5%), respectively. At high brightness level, the internal voltage reference, V_{REF}, changes in proportion to the duty cycle of the PWM input signal at the EN/PWM pin with 8-bit resolution. At low brightness level, V_{REF} stays unchanged and an internal PWM generator is enabled. Thus, the LED is turned on and off corresponding to the on and off of the internal PWM signal of which the frequency and the duty cycle are configured by the PWM input signal at the EN/PWM pin. In addition, the internal PWM signal has a 0.4% hystersis response when the PWM input duty cycle changes between increasing and decreasing. The detailed hybrid dimming behavior is illustrated in the below figure.
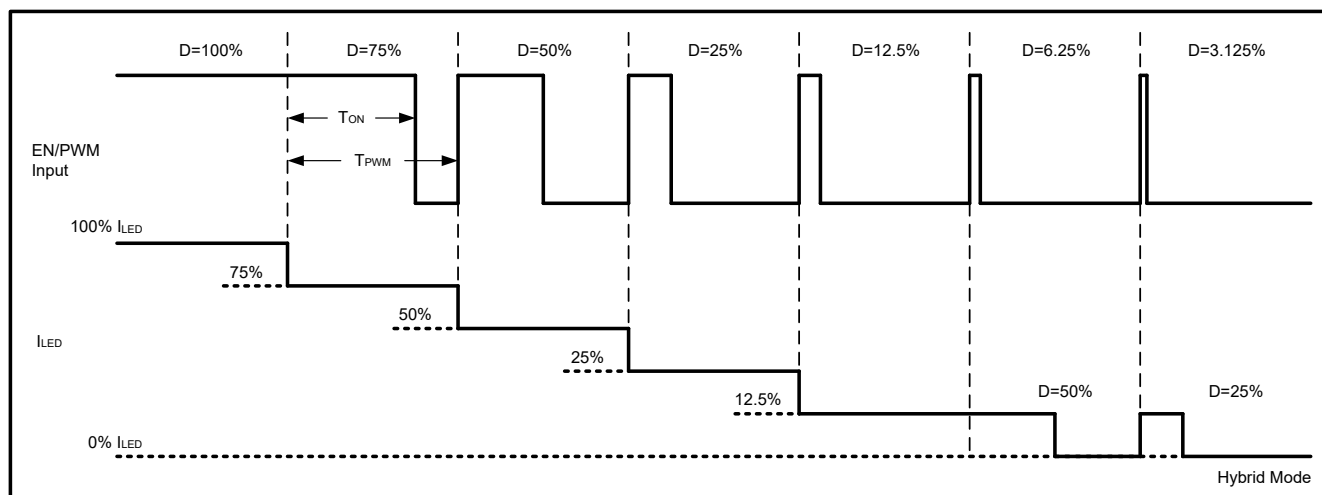
図 8-3. Hybrid Dimming

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Product Folder Links: *TPS923652 TPS923653 TPS923654 TPS923655*

English Data Sheet: SLVSGH1

8.3.5.4 Flexible Dimming

The TPS92365x family also supports flexible dimming to maximize the dimming ratio and the flexibility of dimming control, in which the LED current value and the on/off behavior can be controlled independently. The flexible dimming mode is enabled when both the ADIM/HD pin and the EN/PWM pin are configured by PWM input signals at the same time. Therefore, in fleixble dimming mode, the LED is turned on and off corresponding to the on and off of the PWM input signal at the EN/PWM pin while the reference voltage changes in proportion to the duty cycle of the PWM input signal at the ADIM/HD pin. All the initial conditions and resolutions of PWM dimming and analog dimming apply to the flexible dimming.
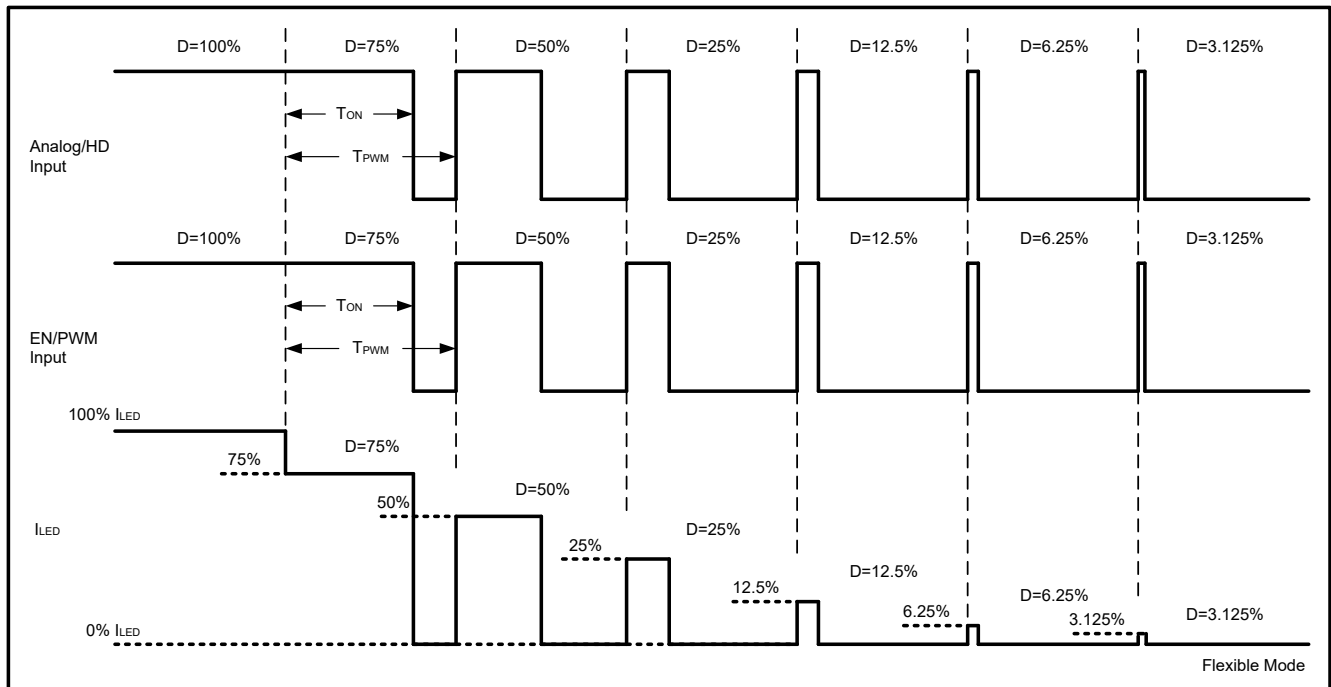
図 8-4. Flexible Dimming

8.3.6 CC/CV Charging Mode

The TPS92365x family enables constant current (CC) / constant voltage (CV) charging operation by configuring OVP pin. When V_{OVP} is below the CC threshold V_{CC_TH} determined by users, the device performs as a controllable constant current source and generates a relatively low output current controlled by a low-duty-cycle PWM signal at ADIM/HD pin for pre-charge. When V_{OVP} is above V_{CC_TH} but below 1.1 V, the device generates a relatively high output current controlled by a high-duty-cycle PWM signal at ADIM/HD pin for CC operation. CV charging mode is enabled and the output current continuously decreases after V_{OVP} rises above 1.1 V. The device then returns to CC operation mode once V_{OVP} falls below 1.1 V.
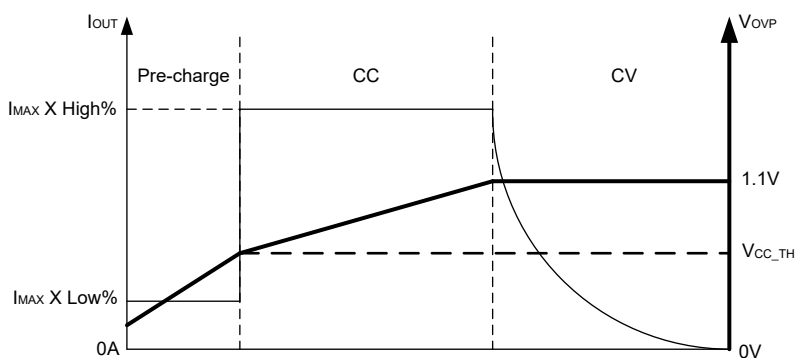
図 **8-5. CC/CV Mode Transition**

8.3.7 Fault Protection

The TPS92365x family is able to provide fault protections and send fault report signals in many fault conditions, including LED open, LED ± short, LED short to PGND, sense resistor open and short, internal switching FET open and short, and thermal shutdown.

表 8-3. Protections

TYPE	CRITERION	BEHAVIOR
LED open load	V_{OVP} > 1.45 V	FAULT pin pull low. The device stops switching and recovers when fault is removed.
LED+ and LED- short circuit (Buck-Boost)	V_{CSN} - V_{IN} < 750 mV	FAULT pin pull low. The device keeps normal behavior.
LED+ short to PGND	V_{CSP} - V_{CSN} > 300 mV	FAULT pin pull low. The device stops switching and recovers when fault is removed.
Sense-resistor open circuit	V_{CSP} - V_{CSN} > 300 mV	FAULT pin pull low. The device stops switching and recovers when fault is removed.
Sense-resistor short circuit	COMP pin is clamped high	FAULT pin pull low. The device keeps switching under the cycle-by-cycle current limit.
Switching FET open circuit	COMP pin is clamped high	FAULT pin pull low. The device stops switching and recovers when fault is removed.
Switching FET short circuit	COMP pin is clamped high	FAULT pin pull low. The device stops switching and recovers when fault is removed.
Thermal shutdown	T_J > T_{TSD}	FAULT pin pull low. The device stops switching and recovers when T_J falls below the hysteresis level.

English Data Sheet: SLVSGH1

8.3.8 Thermal Foldback

The TPS92365x family integrates thermal shutdown protection to prevent the device from overheating. In order to provide design margin of system thermal performance, the device enables a programmable thermal foldback function which automatically reduces the full-scale max output current, I_{MAX}, at high junction temperature. When the device along with the LEDs are mounted on the same thermal substrate, the thermal performance is effectively improved due to the reduction of dissipation need for both device and LED.

As the device junction temperature rises above the thermal foldback threshold temperature, T_{TH}, the full-scale max current starts to reduce following the current-temperature curve shown in the below figure. The current starts to reduce from the 100% level at typically rate of 2% of I_{MAX} per °C until it drops to 50% of the full scale. Once the junction temperature rises 25°C above the T_{TH}, the current continues to decrease at a lower rate until the temperature reaches above the overtemperature shutdown threshold temperature, T_{TSD}.
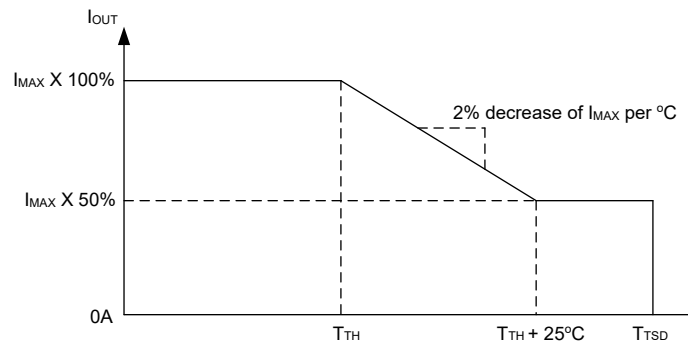
図 8-6. Thermal Foldback

The T_{TH} can be adjusted by changing the resistor R_{TEMP} connected between the TEMP and AGND pin. The T_{TH} and the corresponding R_{TEMP} value are listed in below table.

表 8-4. T_{TH} vs. R_{TEMP} resistor value

| T_{TH} (°C)	Resistor Value (kΩ)
80	200
90	100
100	60
110	40
120	28
130	20
140	15
150	10

9 Application and Implementation

9.1 Application Information

The TPS92365x family is typically used as a Boost / Buck-Boost converter to drive one or more LEDs from an input from 4.5-V to 63-V range.

9.2 Typical Application

9.2.1 TPS923654 Boost, 12-V Input, 1-A Output, 12-piece WLED Driver With Analog Dimming
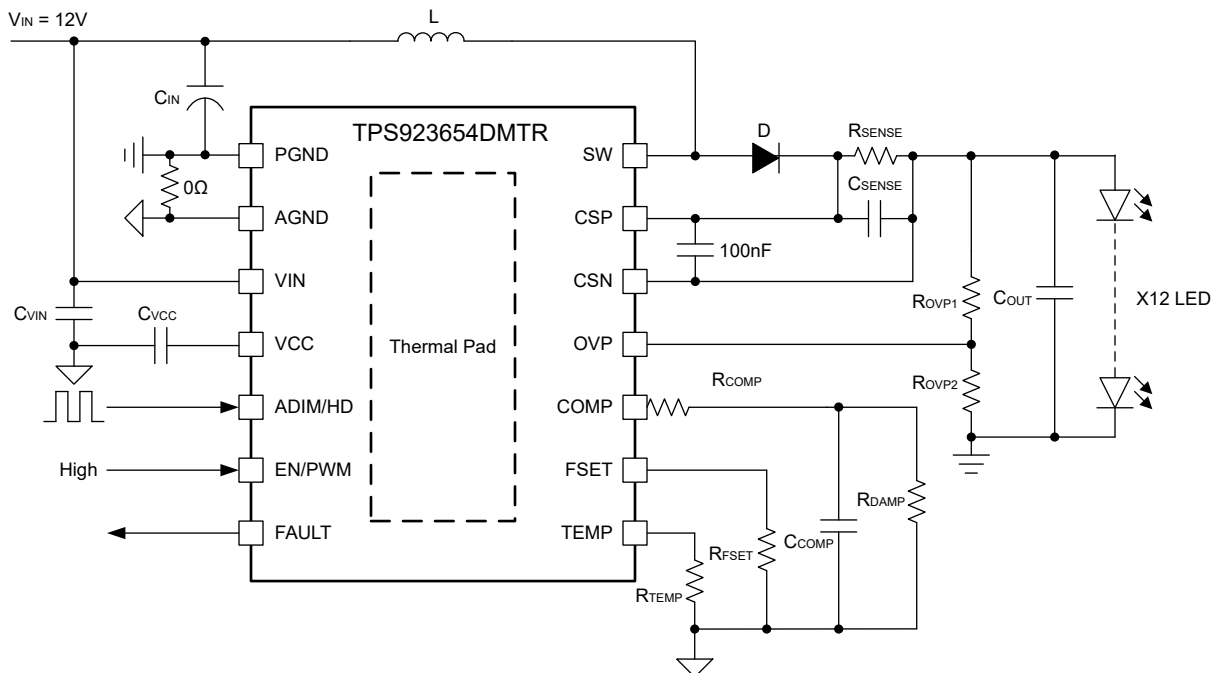
図 9-1. Boost, 12-V Input, 1-A Output, 12-piece WLED, Analog Dimming Reference Design

9.2.1.1 Design Requirements

For this design example, use the parameters in the following table.

表 9-1. Design Parameters

PARAMETER	VALUE
Input voltage range	12 V ±10%
LED forward voltage	3.0 V
Output voltage	36 V (3.0 × 12)
Maximum LED current	1 A
Inductor current ripple	60% of maximum inductor current
LED current ripple	200 mA or less
Input voltage ripple	500 mV or less
Dimming type	Analog dimming with TPS923654: 1-kHz, 1% to 100% PWM input at the ADIM pin

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Inductor Selection

For this design, the input voltage is a 12-V, rail with 10% variation. The output is 12 white LEDs in series and the inductor current ripple by requirement is less than 60% of maximum inductor current. To choose a proper peak-to-peak inductor current ripple, the low-side FET current limit should not be violated when the converter works in full-load condition. This requires half of the peak-to-peak inductor current ripple to be lower than that limit. Another consideration is to ensure reasonable inductor core loss and copper loss caused by the peak-to-peak current ripple. Once this peak-to-peak inductor current ripple is chosen, use 式 2 to calculate the recommended value of the output inductor L.

$$L = \frac{V_{IN(max)} \times \left(V_{OUT} - V_{IN(max)} \right)}{V_{OUT} \times K_{IND} \times I_{L(max)} \times f_{SW}} \tag{2}$$

where

- K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum LED current.
- $I_{L(max)}$ is the maximum inductor current.
- f_{SW} is the switching frequency.
- $V_{IN(max)}$ is the maximum input voltage.
- V_{OUT} is the sum of the voltage across LED load and the voltage across sense resistor.

With the chosen inductor value, the user can calculate the actual inductor current ripple using 式 3.

$$I_{L(ripple)} = \frac{V_{IN(max)} \times \left(V_{OUT} - V_{IN(max)} \right)}{V_{OUT} \times L \times f_{SW}} \tag{3}$$

The ratings of inductor RMS current and saturation current must be greater than those seen in the system requirement. This is to ensure no inductor overheat or saturation occurring. During power up, transient conditions or fault conditions, the inductor current may exceed its normal operating current and reach the current limit. Therefore, it is preferred to select a saturation current rating equal to or greater than the converter current limit. The peak-inductor-current and RMS current equations are shown in 式 4 and 式 5.

$$I_{L(peak)} = I_{L(max)} + \frac{I_{L(ripple)}}{2} \tag{4}$$

$$I_{L(rms)} = \sqrt{I_{L(max)}^2 + \frac{I_{L(ripple)}^2}{12}} \tag{5}$$

In this design, $V_{IN(max)}$ = 12 V, V_{OUT} = 36 V, I_{LED} = 1 A, f_{SW} = 500 kHz, choose K_{IND} = 0.6, the calculated inductance is 8.9 µH. A 10-µH inductor is chosen. With this inductor, the ripple, peak, and rms currents of the inductor are 1.6 A, 3.8 A, and 3.04 A, respectively.

9.2.1.2.2 Input Capacitor Selection

An input capacitor is required to reduce the surge current drawn from the input supply and the switching noise coming from the device. Electrolytic capacitors are recommended for energy storage. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, it is recommended to place a 1-µF ceramic capacitor along with a 0.1-µF capacitor from VIN to PGND/AGND to provide high-frequency filtering. The input capacitor voltage rating must be greater than the maximum input voltage. Use 式 6 to calculate the input ripple voltage, where ESR_{CIN} is the ESR of input capacitor, and K_{DR} is the derating coefficient of ceramic capacitance at the applied DC voltage.

$$V_{IN(ripple)} = \frac{I_{L(ripple)}}{8 \times C_{IN} \times f_{SW}} \tag{6}$$

In this design, a 33-µF, 25V electrolytic capacitor, a 1-µF, 25V X7R ceramic capacitor and a 0.1-µF, 100V X7R ceramic capacitor are chosen, yielding around 400-mV input ripple voltage.

9.2.1.2.3 Output Capacitor Selection

The output capacitor reduces the high-frequency current ripple through the LED string. Excessive current ripple increases the RMS current in the LED string, therefore increasing the LED temperature.

1. Calculate the total dynamic resistance of the LED string (R_{LED}) using the LED manufacturer's datasheet.

2. Calculate the required impedance of the output capacitor (Z_{OUT}) given the acceptable peak-to-peak ripple current through the LED string, $I_{LED(ripple)}$. $I_{L(ripple)}$ is the peak-to-peak inductor ripple current as calculated with the selected inductor.

3. Calculate the minimum effective output capacitance required.

4. Increase the output capacitance appropriately due to the derating effect of applied DC voltage.

See 式 7, 式 8, and 式 9.

$$R_{LED} = \frac{\Delta V_F}{\Delta I_F} \times \#\ of\ LEDs \tag{7}$$

$$Z_{COUT} = \frac{R_{LED} \times I_{LED(ripple)}}{I_{L(max)} - I_{LED(ripple)}} \tag{8}$$

$$C_{COUT} = \frac{1}{2\pi \times f_{SW} \times Z_{COUT}} \tag{9}$$

Once the output capacitor is chosen, 式 10 can be used to estimate the peak-to-peak ripple current through the LED string.

$$I_{LED(ripple)} = \frac{Z_{COUT} \times I_{L(max)}}{Z_{COUT} + R_{LED}} \tag{10}$$

CREE WLED is used here. The dynamic resistance of the LED is 0.67 ohm at 3-A forward current. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. In this design, a 22-µF, 100-V X7R ceramic capacitor and a 0.1-µF, 100-V X7R ceramic capacitor are chosen. The calculated ripple current of the LED is about 65 mA.

9.2.1.2.4 Sense Resistor Selection

The maximum LED current is 1 A at 100% PWM duty and the corresponding V_{REF} is 200 mV. By using 式 1, the sense resistance is calculated as 200 mΩ.

Note that the power consumption of the sense resistor is 200 mW, requiring enough margin of the resistor's power rating in selection.

9.2.1.2.5 Other External Components Selection

In this design, a 0.1-µF, 50-V X7R ceramic capacitor is chosen for high-frequency filtering of sense feedback. Using 式 11, a 10-µF, 50-V X7R ceramic capacitor is chosen for C_{SENSE} to suppress the ac magnitude of sense feedback less than 200 mV.

$$C_{SENSE} = \frac{0.25 \times I_{L(max)}}{200mV \times f_{SW}} \tag{11}$$

For loop stability, it is recommended to select a 1-nF, 10-V X7R ceramic capacitor for C_{COMP} and a 1-kΩ resistor for R_{COMP}. A 1-MΩ resistor is chosen for R_{DAMP} to suppress the overshoot current at rising edge of PWM on.
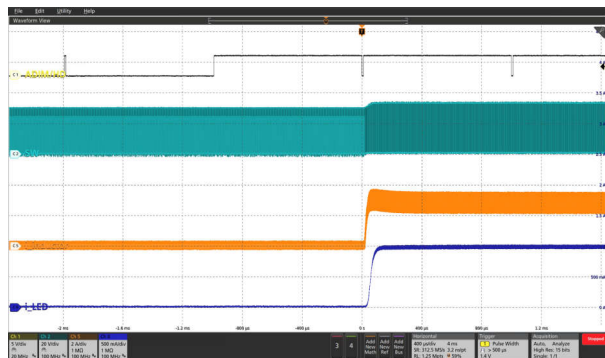
9.2.1.3 Application Curves
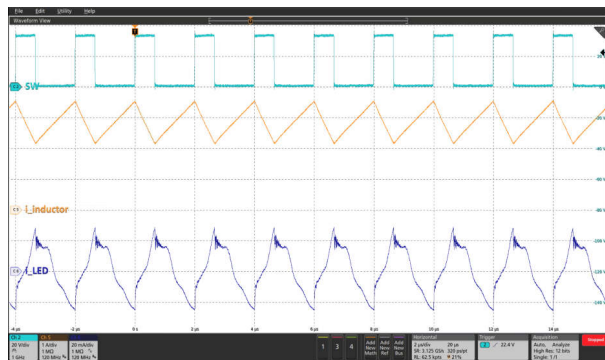
Light Blue: SW, Orange: Inductor Current, Deep Blue: LED
Current Ripple (AC)

図 9-2. LED Current Ripple at PWM$_{ADIM}$ = 100%, 1 kHz and F$_{SW}$ = 500 kHz
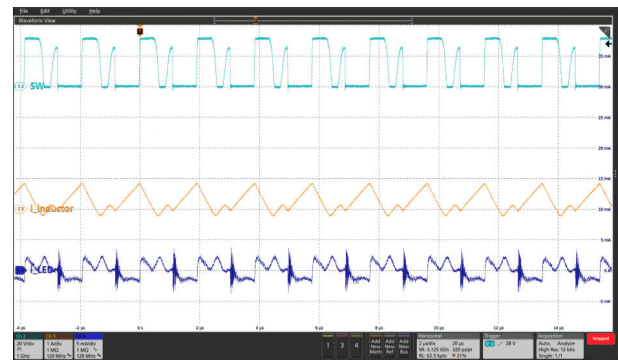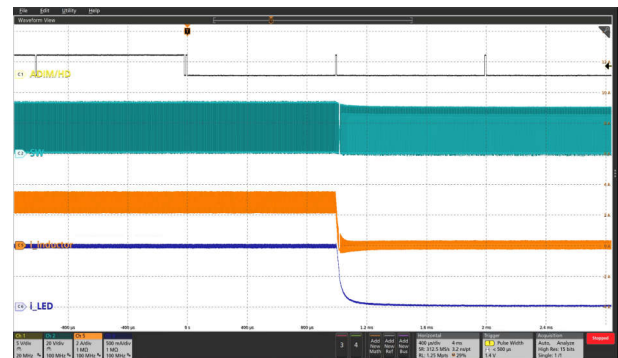

Light Blue: SW, Orange: Inductor Current, Deep Blue: LED
Current Ripple (AC)

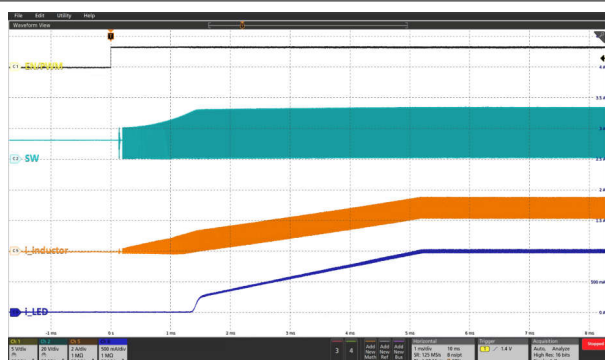**図 9-3. LED Current Ripple at PWM$_{ADIM}$ = 10%, 1 kHz and F$_{SW}$ = 500 kHz**

Black: PWM$_{ADIM}$, Light Blue: SW, Orange: Inductor Current,
Deep Blue: LED Current

図 9-4. LED Current Transient for a PWM$_{ADIM}$ Transition from 1% to 99%, 1 kHz

Black: PWM$_{ADIM}$, Light Blue: SW, Orange: Inductor Current,
Deep Blue: LED Current

図 9-5. LED Current Transient for a PWM$_{ADIM}$ Transition from 99% to 1%, 1 kHz

Black: PWM$_{PWM}$, Light Blue: SW, Orange: Inductor Current,
Deep Blue: LED Current

図 9-6. Start-Up at PWM$_{ADIM}$ = 100%, 1 kHz
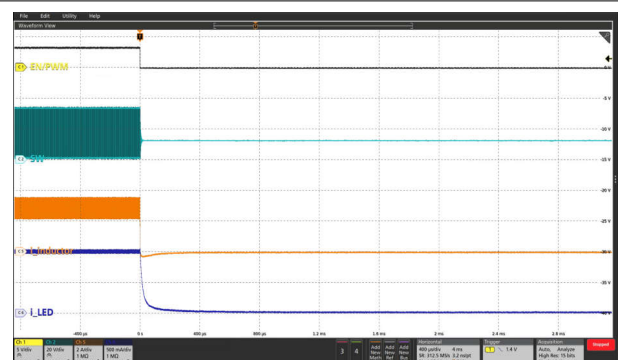
Black: PWM$_{PWM}$, Light Blue: SW, Orange: Inductor Current,
Deep Blue: LED Current

図 9-7. Shutdown at PWM$_{ADIM}$ = 100%, 1 kHz
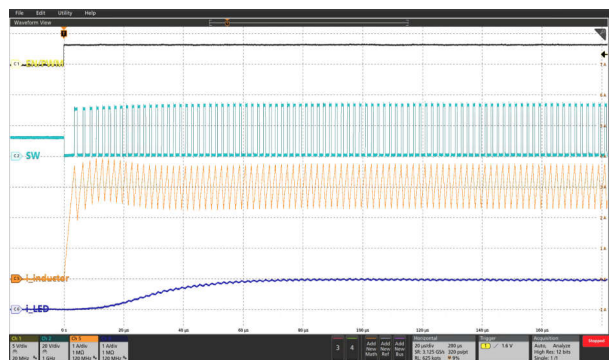
Product Folder Links: *TPS923652 TPS923653 TPS923654 TPS923655*
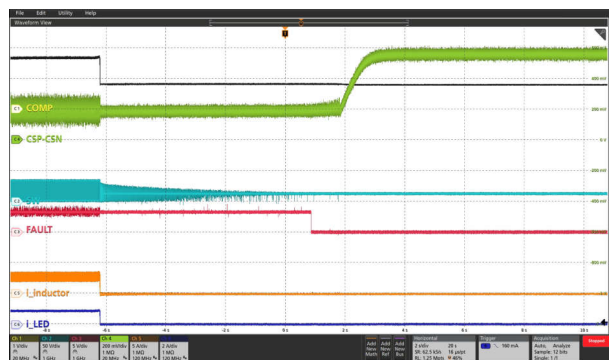
English Data Sheet: SLVSGH1

Black: PWM$_{PWM}$, Light Blue: SW, Orange: Inductor Current,
Deep Blue: LED Current

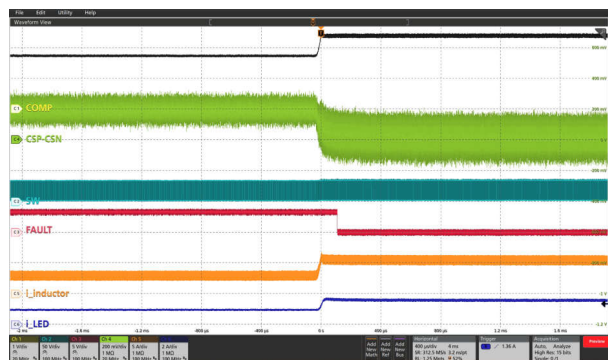**図 9-8. LED PWM Dimmign Rising Edge at PWM$_{PWM}$ = 50%, 20 kHz**
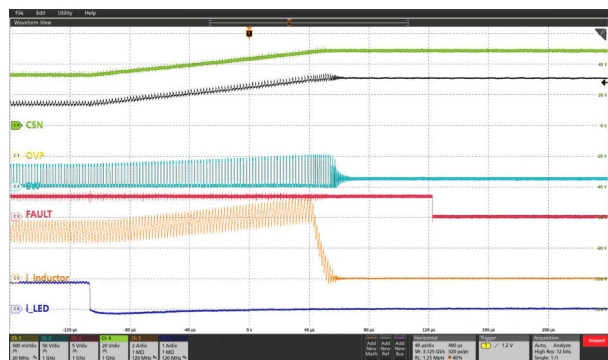
Black: OVP, Light Blue: SW, Red: FAULT, Orange: Inductor
Current, Deep Blue: LED Current, Green: CSN

図 9-9. LED Open-Load Protection

Black: COMP, Light Blue: SW, Red: FAULT, Orange: Inductor
Current, Deep Blue: LED Current, Green: CSP-CSN

図 9-10. Sense-Resistor Open Protection

Black: COMP, Light Blue: SW, Red: FAULT, Orange: Inductor
Current, Deep Blue: LED Current, Green: CSP-CSN

図 9-11. Sense-Resistor Short-Circuit Protection

Product Folder Links: *TPS923652 TPS923653 TPS923654 TPS923655*

English Data Sheet: SLVSGH1

9.2.2 TPS923654 Buck-Boost, 24-V Input, 2-A Output, 4-piece WLED Driver with PWM Dimming
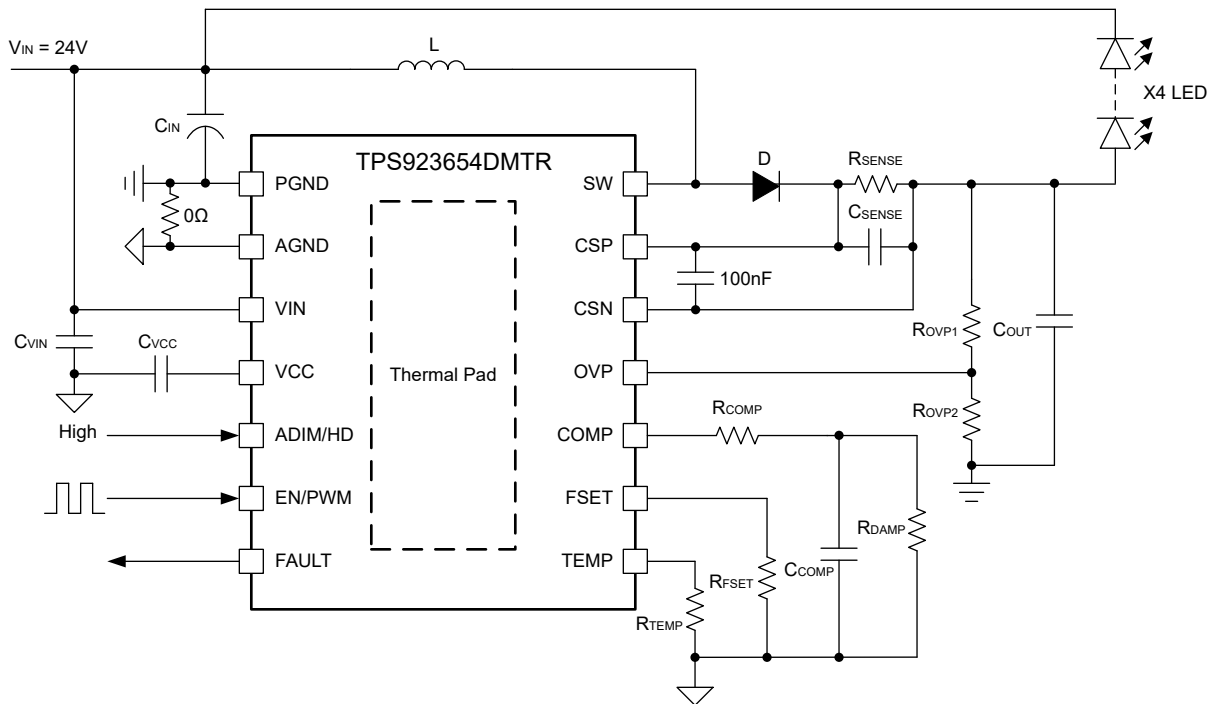

図 9-12. Buck-Boost, 24-V Input, 2-A Output, 4-piece WLED, PWM Dimming Reference Design

9.2.2.1 Design Requirements

For this design example, use the parameters in the following table.

表 9-2. Design Parameters

PARAMETER	VALUE
Input voltage range	24 V ±10%
LED forward voltage	3.0 V
Output voltage	12 V (3.0 × 4)
Maximum LED current	2 A
Inductor current ripple	50% of maximum inductor current
LED current ripple	200 mA or less
Input voltage ripple	200 mV or less
Dimming type	PWM dimming with TPS923654: 1-kHz, 1% to 100% PWM input at the PWM pin

9.2.2.2 Detailed Design Procedure

9.2.2.2.1 Inductor Selection

For this design, the input voltage is a 24-V, rail with 10% variation. The output is 4 white LEDs in series and the inductor current ripple by requirement is less than 50% of maximum inductor current. To choose a proper peak-to-peak inductor current ripple, the low-side FET current limit should not be violated when the converter works in no-load condition. This requires half of the peak-to-peak inductor current ripple to be lower than that limit. Another consideration is to ensure reasonable inductor core loss and copper loss caused by the peak-to-peak current ripple. Once this peak-to-peak inductor current ripple is chosen, use 式 12 to calculate the recommended value of the output inductor L.

$$L = \frac{V_{IN(max)} \times V_{OUT}}{\left(V_{OUT} + V_{IN(max)}\right) \times K_{IND} \times I_{L(max)} \times f_{SW}} \tag{12}$$

where

- K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum LED current.
- $I_{L(max)}$ is the maximum inductor current.
- f_{SW} is the switching frequency.
- $V_{IN(max)}$ is the maximum input voltage.
- V_{OUT} is the sum of the voltage across LED load and the voltage across sense resistor.

With the chosen inductor value, the user can calculate the actual inductor current ripple using 式 13.

$$I_{L(ripple)} = \frac{V_{IN(max)} \times V_{OUT}}{\left(V_{OUT} + V_{IN(max)}\right) \times L \times f_{SW}} \tag{13}$$

The ratings of inductor RMS current and saturation current must be greater than those seen in the system requirement. This is to ensure no inductor overheat or saturation occurring. During power up, transient conditions or fault conditions, the inductor current may exceed its normal operating current and reach the current limit. Therefore, it is preferred to select a saturation current rating equal to or greater than the converter current limit. The peak-inductor-current and RMS current equations are shown in 式 14 and 式 15.

$$I_{L(peak)} = I_{L(max)} + \frac{I_{L(ripple)}}{2} \tag{14}$$

$$I_{L(rms)} = \sqrt{I_{L(max)}^2 + \frac{I_{L(ripple)}^2}{12}} \tag{15}$$

In this design, $V_{IN(max)}$ = 24 V, V_{OUT} = 12 V, I_{LED} = 2 A, f_{SW} = 1.2 MHz, choose K_{IND} = 0.5, the calculated inductance is 4.4 µH. A 4.7-µH inductor is chosen. With this inductor, the ripple, peak, and rms currents of the inductor are 1.4 A, 3.7 A, and 3.03 A, respectively.

9.2.2.2.2 Input Capacitor Selection

An input capacitor is required to reduce the surge current drawn from the input supply and the switching noise coming from the device. Electrolytic capacitors are recommended for energy storage. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, it is recommended to place a 10-µF capacitor along with a 0.1-µF capacitor from VIN to PGND/AGND to provide high-frequency filtering. The input capacitor voltage rating must be greater than the maximum input voltage. Use 式 16 to calculate the input ripple voltage, where ESR_{CIN} is the ESR of input capacitor, and K_{DR} is the derating coefficient of ceramic capacitance at the applied DC voltage.

$$V_{IN(ripple)} = I_{L(max)} \times \left(\frac{V_{OUT}}{K_{DR} \times C_{IN} \times f_{SW} \times \left(V_{IN(max)} + V_{OUT}\right)} + ESR_{CIN} \right) \tag{16}$$

In this design, a 100-µF, 50V electrolytic capacitor, a 4.7-µF, 100V X7R ceramic capacitor and a 0.1-µF, 100V X7R ceramic capacitor are chosen, yielding around 190-mV input ripple voltage.

9.2.2.2.3 Output Capacitor Selection

The output capacitor reduces the high-frequency current ripple through the LED string. Excessive current ripple increases the RMS current in the LED string, therefore increasing the LED temperature.

1. Calculate the total dynamic resistance of the LED string (R_{LED}) using the LED manufacturer's datasheet.

2. Calculate the required impedance of the output capacitor (Z_{OUT}) given the acceptable peak-to-peak ripple current through the LED string, $I_{LED(ripple)}$. $I_{L(ripple)}$ is the peak-to-peak inductor ripple current as calculated with the selected inductor.

3. Calculate the minimum effective output capacitance required.

4. Increase the output capacitance appropriately due to the derating effect of applied DC voltage.

See 式 17, 式 18, and 式 19.

$$R_{LED} = \frac{\Delta V_F}{\Delta I_F} \times \# \ of \ LEDs \tag{17}$$

$$Z_{COUT} = \frac{R_{LED} \times I_{LED(ripple)}}{I_{L(max)} - I_{LED(ripple)}} \tag{18}$$

$$C_{COUT} = \frac{1}{2\pi \times f_{SW} \times Z_{COUT}} \tag{19}$$

Once the output capacitor is chosen, 式 20 can be used to estimate the peak-to-peak ripple current through the LED string.

$$I_{LED(ripple)} = \frac{Z_{COUT} \times I_{L(max)}}{Z_{COUT} + R_{LED}} \tag{20}$$

Cree WLED is used here. The dynamic resistance of the LED is 0.67 ohm at 1-A forward current. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. In this design, a 10-µF, 100-V X7R ceramic capacitor and a 0.1-µF, 100-V X7R ceramic capacitor are chosen. The calculated ripple current of the LED is about 70 mA.

9.2.2.2.4 Sense Resistor Selection

The maximum LED current is 2 A at 100% PWM duty and the corresponding V_{REF} is 200 mV. By using 式 1, the sense resistance is calculated as 100 mΩ.

Note that the power consumption of the sense resistor is 400 mW, requiring enough margin of the resistor's power rating in selection.
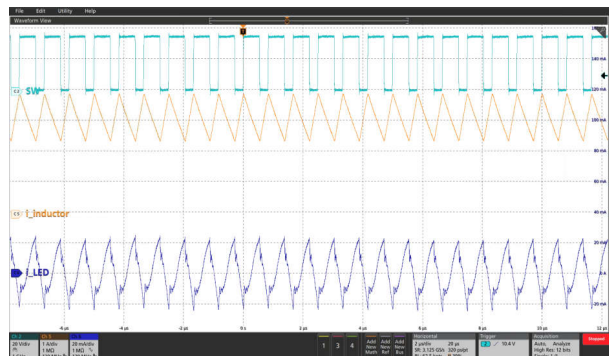
9.2.2.2.5 Other External Components Selection

In this design, a 0.1-µF, 50-V X7R ceramic capacitor is chosen for high-frequency filtering of sense feedback. Using 式 21, a 10-µF, 50-V X7R ceramic capacitor is chosen for C_{SENSE} to suppress the ac magnitude of sense feedback less than 200 mV.

$$C_{SENSE} = \frac{0.25 \times I_{L(max)}}{200mV \times f_{SW}} \tag{21}$$

For loop stability, it is recommended to select a 1-nF, 10-V X7R ceramic capacitor for C_{COMP} and a 1-kΩ resistor for R_{COMP}. A 1-MΩ resistor is chosen for R_{DAMP} to suppress the overshoot current at rising edge of PWM on.

Product Folder Links: *TPS923652 TPS923653 TPS923654 TPS923655*

English Data Sheet: SLVSGH1
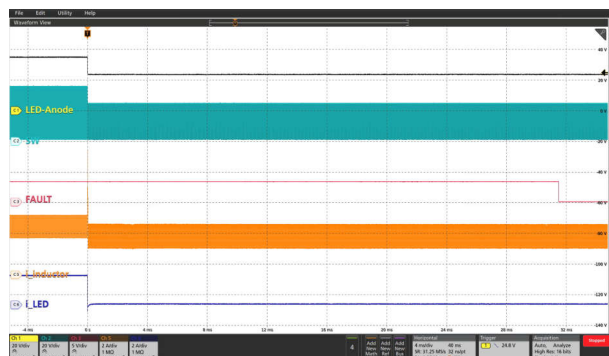
9.2.2.3 Application Curves

Light Blue: SW, Orange: Inductor Current, Deep Blue: LED Current Ripple (AC)

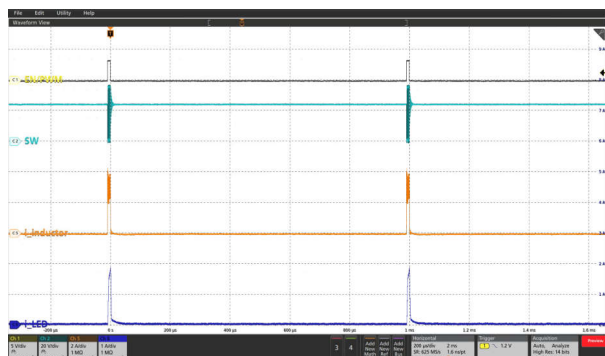**図 9-13. LED Current Ripple at PWM$_{ADIM}$ = 100%, 1 kHz and F$_{SW}$ = 1.2 MHz**
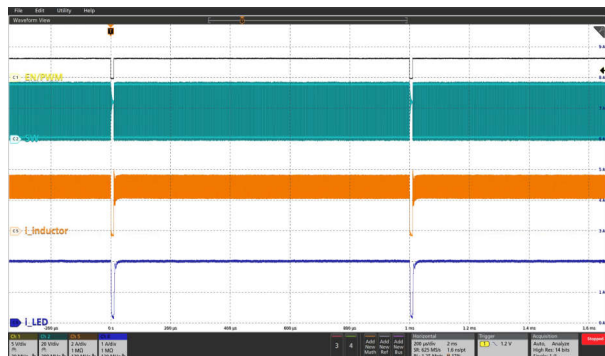
Black: PWM$_{PWM}$, Light Blue: SW, Orange: Inductor Current, Deep Blue: LED Current

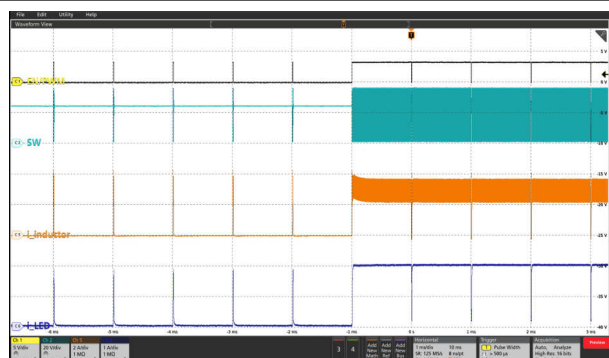**図 9-14. LED PWM Dimming at PWM$_{PWM}$ = 99%, 20 kHz**

Black: PWM$_{PWM}$, Light Blue: SW, Red: FAULT, Orange: Inductor Current, Deep Blue: LED Current
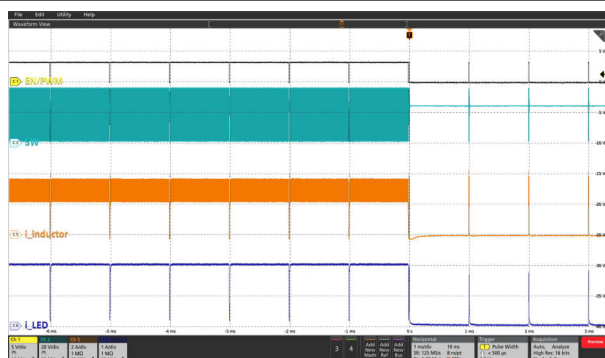
図 9-15. LED+ Short-to-VIN Protection

Black: PWM$_{PWM}$, Light Blue: SW, Orange: Inductor Current, Deep Blue: LED Current

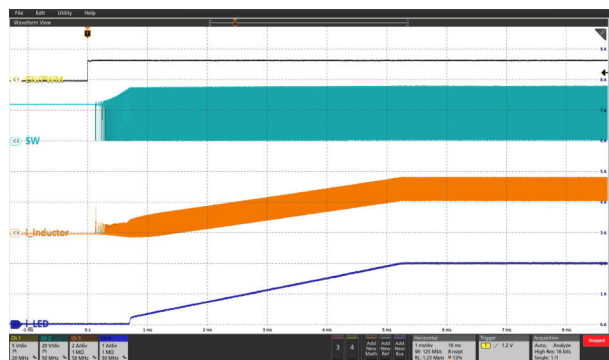**図 9-16. LED PWM Dimming at PWM$_{PWM}$ = 1%, 20 kHz**

Black: PWM$_{PWM}$, Light Blue: SW, Orange: Inductor Current, Deep Blue: LED Current

図 9-17. LED Current Transient for a PWM$_{PWM}$ Transition from 1% to 99%, 20 kHz
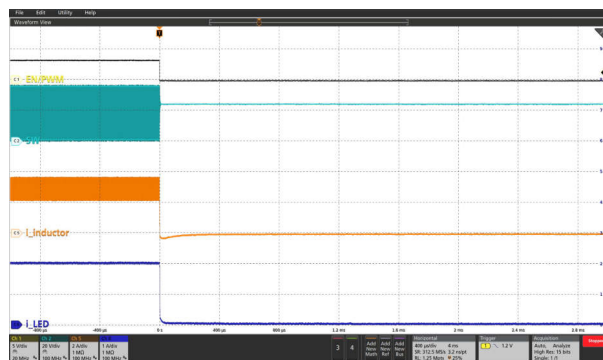

Black: PWM$_{PWM}$, Light Blue: SW, Orange: Inductor Current, Deep Blue: LED Current

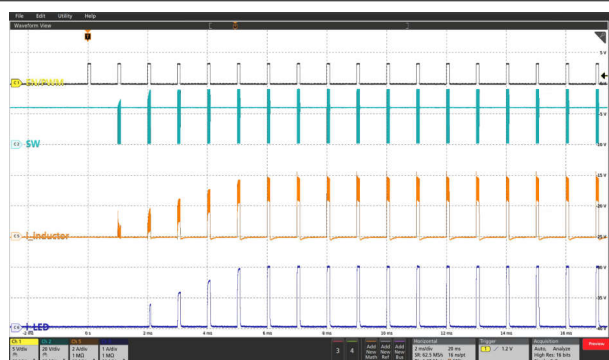**図 9-18. LED Current Transient for a PWM$_{PWM}$ Transition from 99% to 1%, 20 kHz**

Black: PWM$_{PWM}$, Light Blue: SW, Orange: Inductor Current,
Deep Blue: LED Current
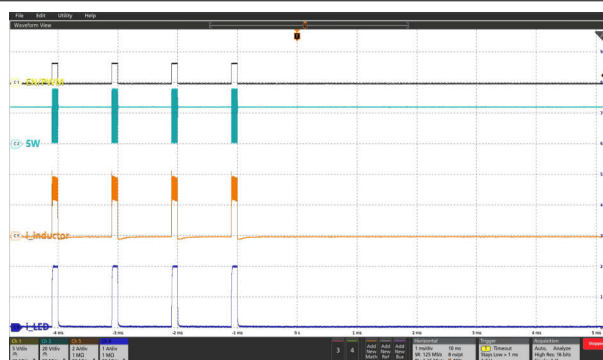
図 9-19. Start-Up at PWM$_{PWM}$ = 100%, 20 kHz

Black: PWM$_{PWM}$, Light Blue: SW, Orange: Inductor Current,
Deep Blue: LED Current

図 9-20. Shutdown at PWM$_{PWM}$ = 100%, 20 kHz

Black: PWM$_{PWM}$, Light Blue: SW, Orange: Inductor Current,
Deep Blue: LED Current

図 9-21. Start-Up at PWM$_{PWM}$ = 10%, 20 kHz

Black: PWM$_{PWM}$, Light Blue: SW, Orange: Inductor Current,
Deep Blue: LED Current

図 9-22. Shutdown at PWM$_{PWM}$ = 10%, 20 kHz

Product Folder Links: *TPS923652 TPS923653 TPS923654 TPS923655*

English Data Sheet: SLVSGH1

9.3 Power Supply Recommendations

The device is designed to operate from an input voltage supply ranging between 4.5 V and 65 V. This input supply must be well regulated. The device requires an input capacitor to reduce the surge current drawn from the input supply and the switching noise from the device. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 10-µF capacitor is enough.

9.4 Layout

The TPS92365x family requires a proper layout for optimal performance. The following section gives some guidelines to ensure a proper layout.

9.4.1 Layout Guidelines

An example of a proper layout for the TPS92365x family is shown in .セクション 9.4.2

- Creating a large PGND plane for good electrical and thermal performance is important.
- The IN and PGND traces should be as wide as possible to reduce trace impedance. Wide traces have the additional advantage of providing excellent heat dissipation.
- Thermal vias can be used to connect the top-side PGND plane to additional printed-circuit board (PCB) layers for heat dissipation and grounding.
- The input capacitors must be located as close as possible to the IN pin and the PGND/AGND pin.
- The VCC capacitor should be placed as close as possible to VCC pin to ensure stable LDO output voltage.
- The SW trace must be kept as short as possible to reduce parasitic inductance and thereby reduce transient voltage spikes. Short SW trace also reduces radiated noise and EMI.
- Do not allow switching current to flow under the device.
- The routing of CSN and CSP traces are recommended to be in parallel and kept as short as possible and placed away from the high-voltage switching trace and the ground shield.
- The compensation capacitor must be placed as close as possible to COMP pin so as to prevent oscillation and system instability.
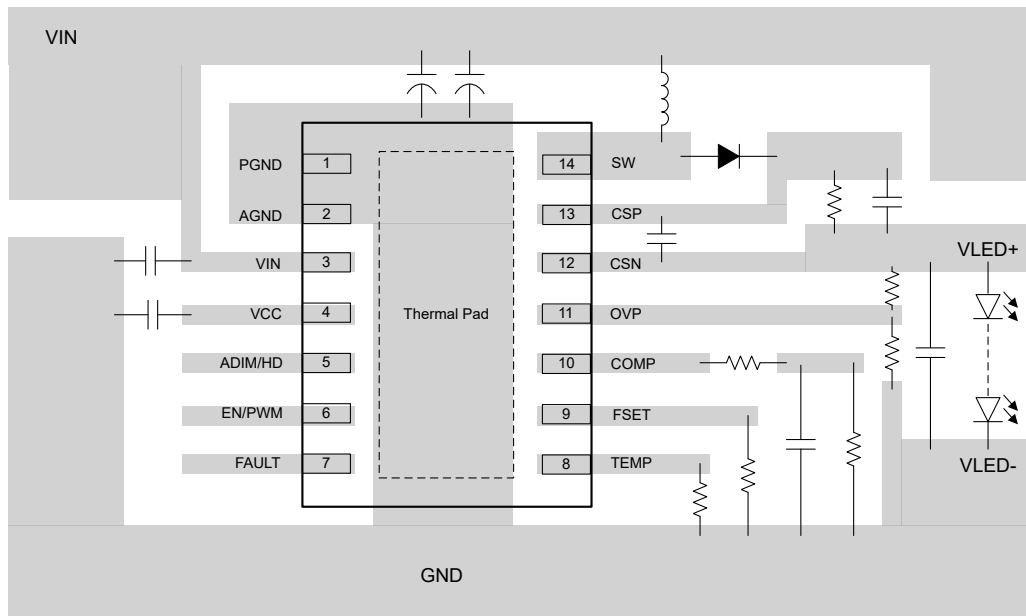
9.4.2 Layout Example

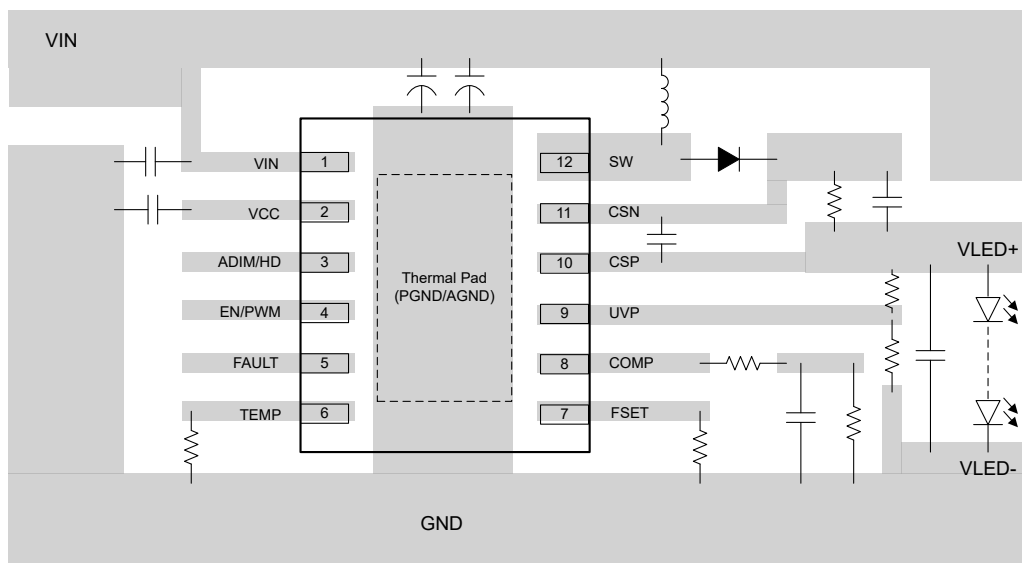**図 9-23. 14-Pin VSON Top View Layout Example**
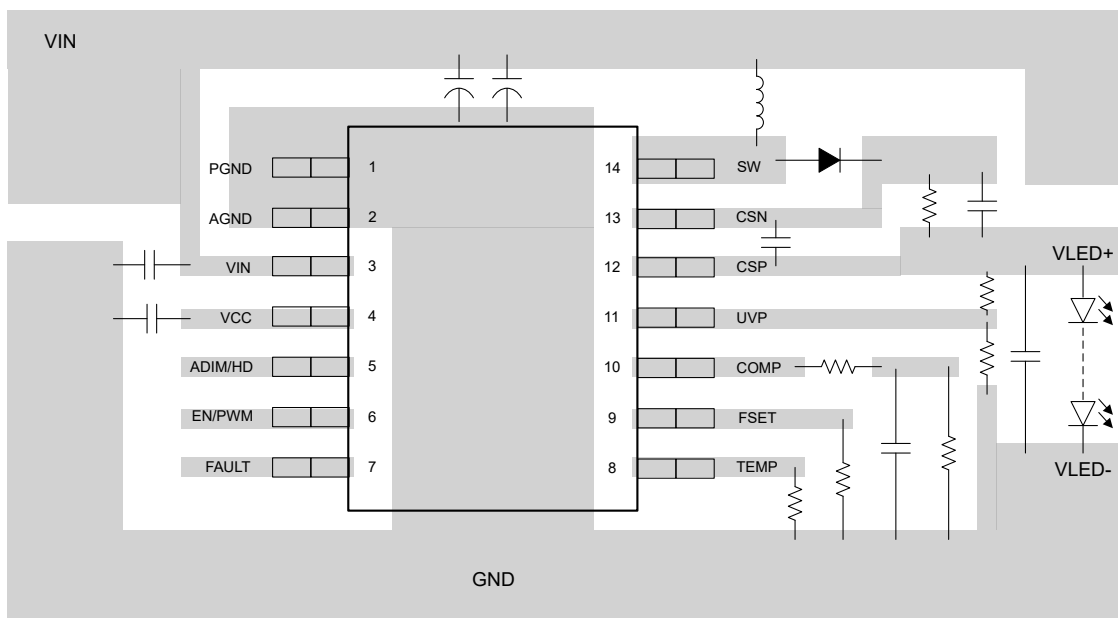
図 9-24. 12-Pin WSON Top View Layout Example

図 9-25. 14-Pin SOT-23-TH Top View Layout Example

Product Folder Links: *TPS923652 TPS923653 TPS923654 TPS923655*

English Data Sheet: SLVSGH1

10 Device and Documentation Support

10.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

10.2 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の使用条件を参照してください。

10.3 Trademarks

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すべての商標は、それぞれの所有者に帰属します。

10.4 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

10.5 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated devices. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS923652DMTR	ACTIVE	VSON	DMT	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T3652	Samples
TPS923652DRRR	ACTIVE	WSON	DRR	12	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T23652	Samples
TPS923652DYYR	ACTIVE	SOT-23-THIN	DYY	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T3652	Samples
TPS923653DMTR	ACTIVE	VSON	DMT	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T3653	Samples
TPS923653DRRR	ACTIVE	WSON	DRR	12	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T23653	Samples
TPS923653DYYR	ACTIVE	SOT-23-THIN	DYY	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T3653	Samples
TPS923654DMTR	ACTIVE	VSON	DMT	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T3654	Samples
TPS923654DRRR	ACTIVE	WSON	DRR	12	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T23654	Samples
TPS923654HMDMTR	ACTIVE	VSON	DMT	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	T364H	Samples
TPS923654MDMTR	ACTIVE	VSON	DMT	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	T364M	Samples
TPS923655DMTR	ACTIVE	VSON	DMT	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T3655	Samples
TPS923655DRRR	ACTIVE	WSON	DRR	12	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T23655	Samples
TPS923655HMDMTR	ACTIVE	VSON	DMT	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	T365H	Samples
TPS923655MDMTR	ACTIVE	VSON	DMT	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	T365M	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.
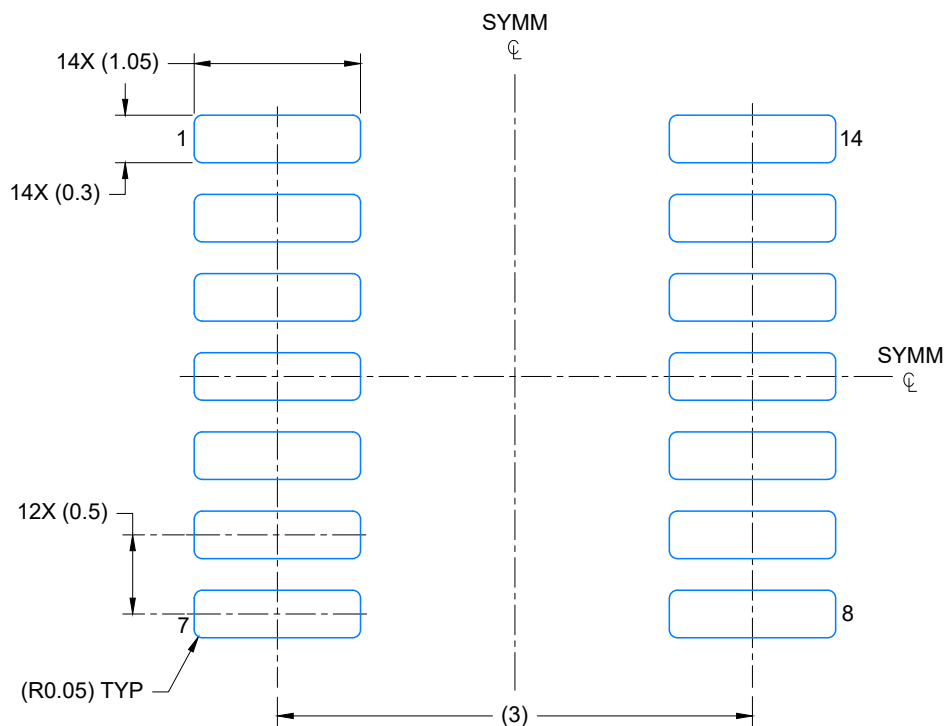
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

3.36
3.16

A

PIN 1 INDEX
AREA

SEATING PLANE

C

0.1 C

12X 0.5

14

1

4.3
4.1
NOTE 3

2X

3

7

8

14X 0.31
0.11

B

2.1
1.9

⊕ 0.1 Ⓜ C AⓈ BⓈ

1.1 MAX

0.2
0.08 TYP

SEE DETAIL A

0.25
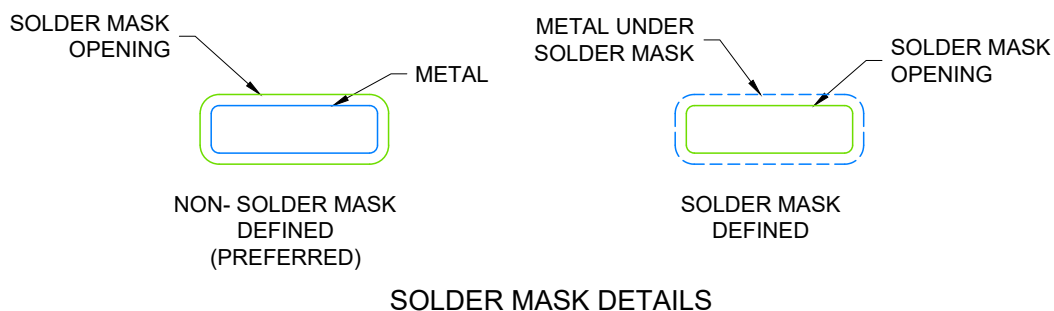GAUGE PLANE

0°- 8°

0.63
0.33

0.1
0.0

DETAIL A
TYP
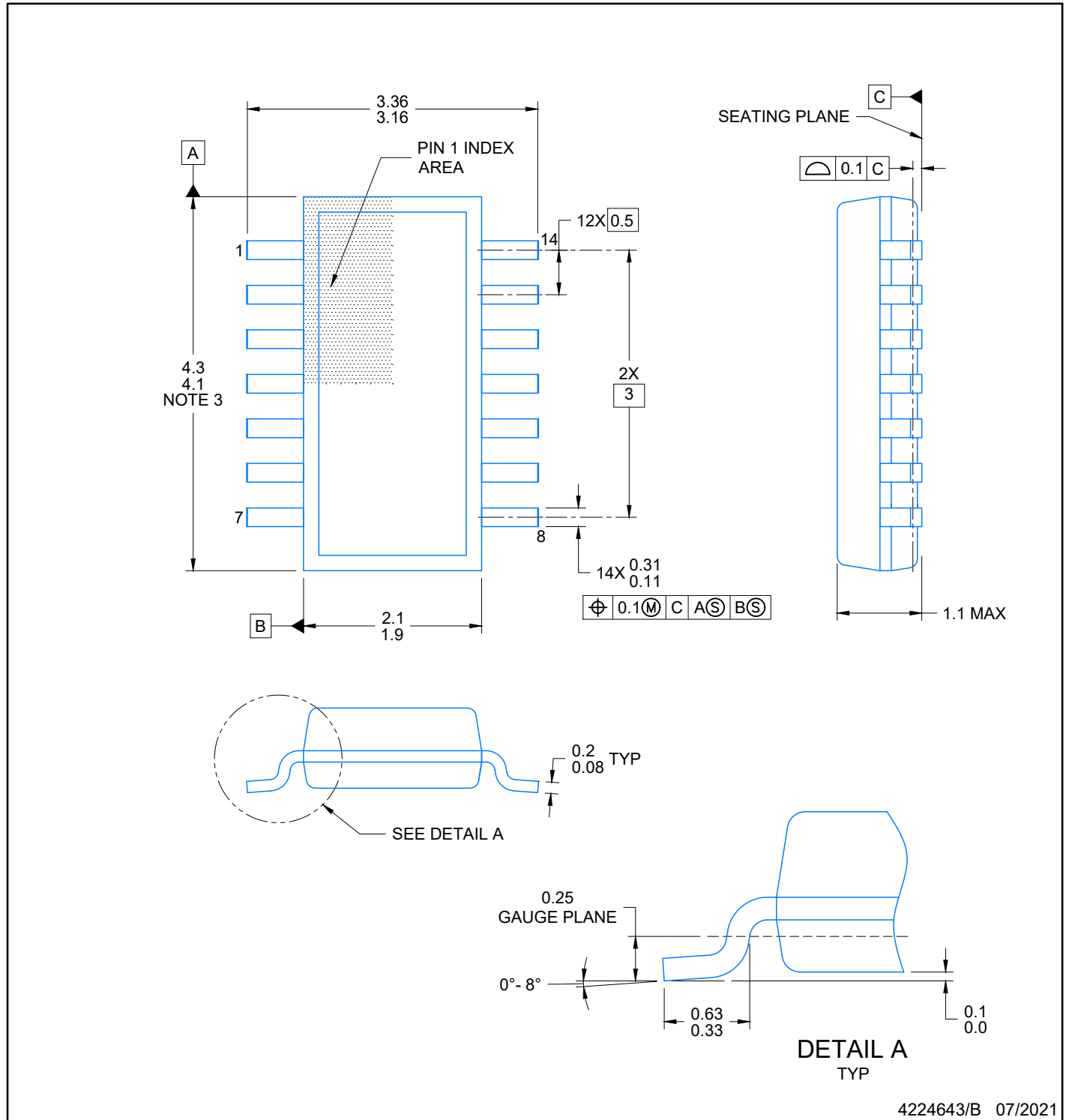
4224643/B   07/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AB

SYMM
℄

14X (1.05)

1

14X (0.3)

14

SYMM
℄

12X (0.5)

7

8

(R0.05) TYP

(3)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

SOLDER MASK
OPENING

METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

NON- SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4224643/B   07/2021

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

SYMM
℄

14X (1.05)

1

14

14X (0.3)

SYMM
℄

12X (0.5)

7

8

(R0.05) TYP

(3)
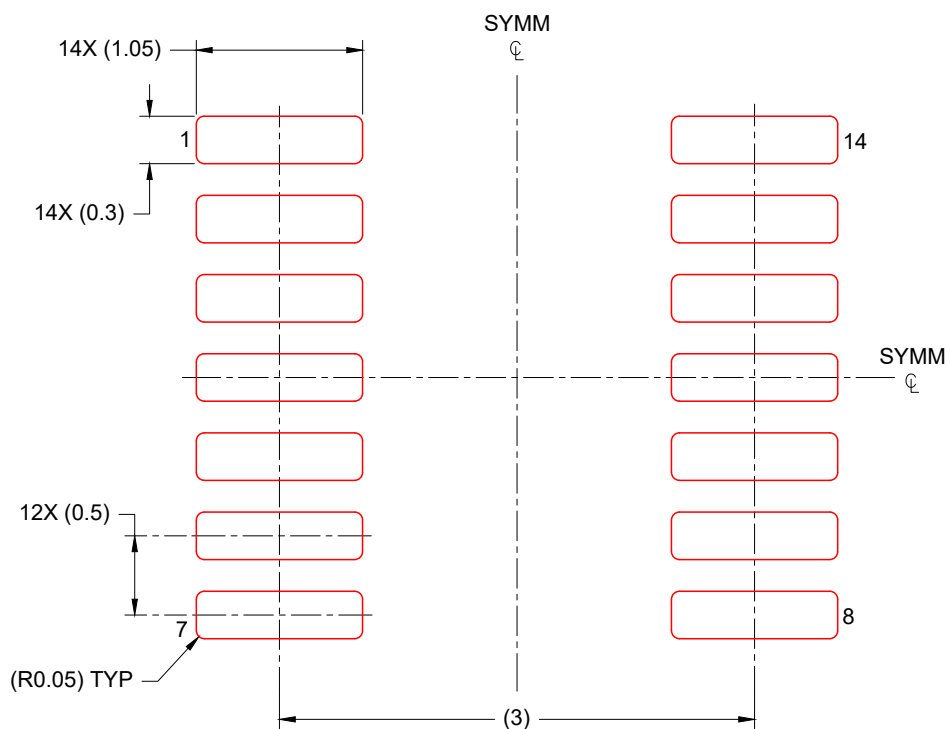
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

4224643/B   07/2021

NOTES: (continued)

8.   Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
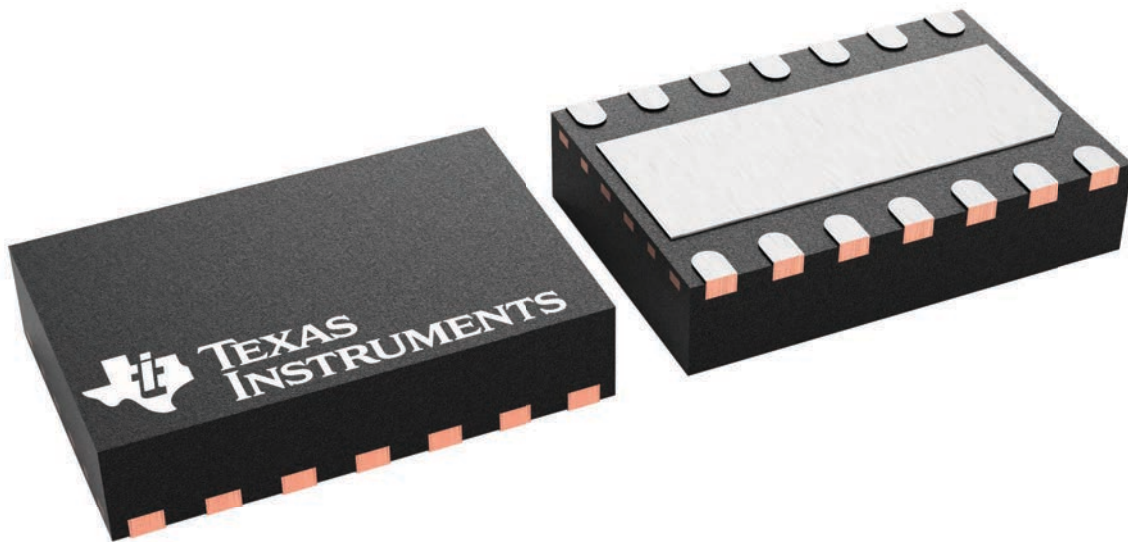9.   Board assembly site may have different recommendations for stencil design.

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4225088/A

B | 3.1 / 2.9 | A
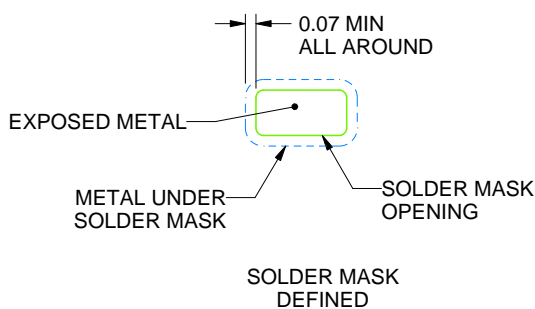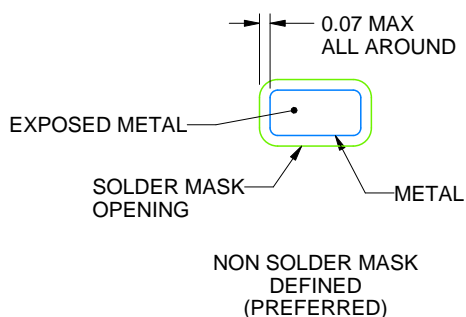
PIN 1 INDEX AREA

4.6 / 4.4

1.0 / 0.8

C

SEATING PLANE

0.05 / 0.00

| 0.08 | C

EXPOSED THERMAL PAD

1.6 ± 0.1

SYMM

(0.1) TYP

7

8

2X 3.9

15

SYMM

4.2 ± 0.1

1

14

12X 0.65

PIN 1 ID
(45° X 0.3)

14X 0.5 / 0.3

14X 0.35 / 0.25

| ⊕ | 0.1 Ⓜ | C | A | B |
| 0.05 Ⓜ | C |

4229426/A   02/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

DMT0014D

14X (0.6)

14X (0.3)

(1.6)

SYMM

1

12X (0.65)

SYMM

15

14

2X
(1.85)

(4.2)

(0.69)
TYP

(Ø 0.2) VIA
TYP

7

(R0.05) TYP

(0.55) TYP

8

(2.8)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

0.07 MAX
ALL AROUND

EXPOSED METAL

SOLDER MASK
OPENING

METAL

NON SOLDER MASK
DEFINED
(PREFERRED)

0.07 MIN
ALL AROUND

EXPOSED METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4229426/A   02/2023

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

14X (0.6)

1

14X (0.3)

12X (0.65)

(1.47)

14

(1.18)

15

SYMM ₵

(1.38)

(R0.05) TYP

METAL TYP

7

8

SYMM ₵

(2.8)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 15
77.4% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

4229426/A   02/2023

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
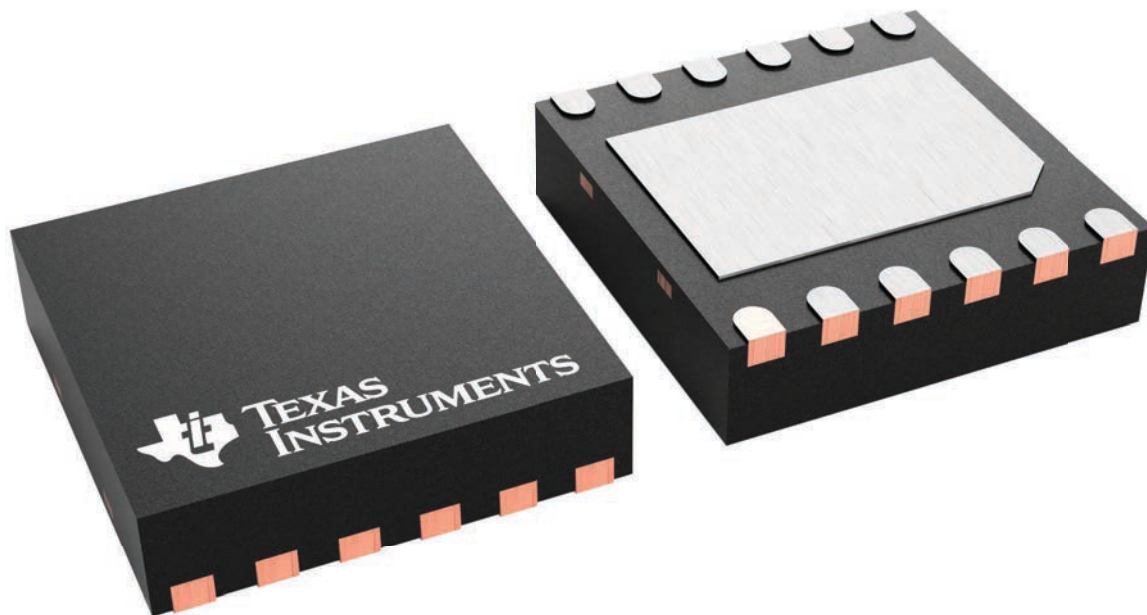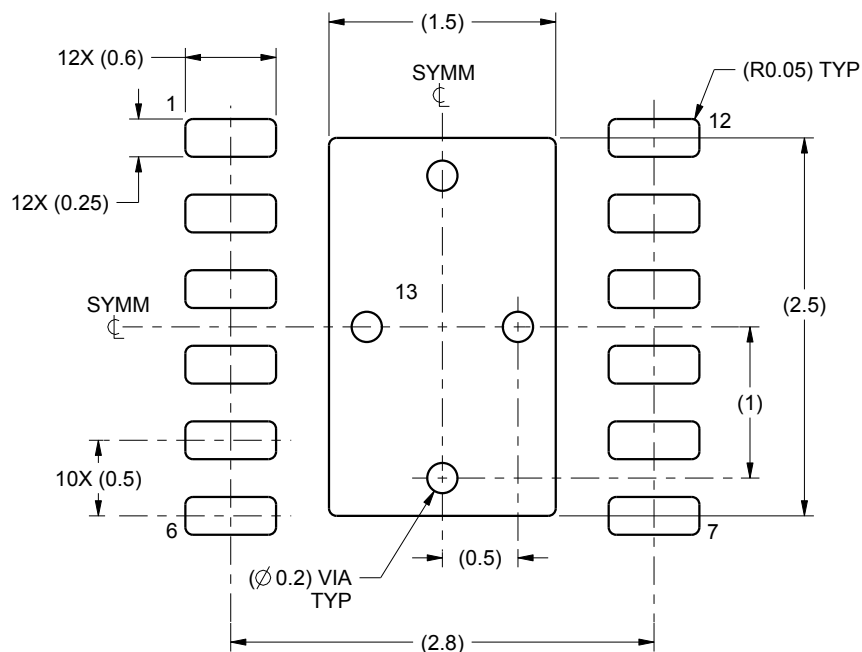
DRR 12

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4223490/B

A ← 3.1 / 2.9 → B

PIN 1 INDEX AREA

3.1
2.9

0.8 MAX

C

0.05
0.00

SEATING PLANE

0.08

EXPOSED
THERMAL PAD

1.5±0.1

10X 0.5

6

7

2X
2.5

13

2.5±0.1

SYMM
Ȼ

(0.1) TYP

1

12

PIN 1 ID
(OPTIONAL)

SYMM
Ȼ

12X 0.3 / 0.2

12X 0.5 / 0.3

⊕ 0.1 Ⓜ C A B
0.05 Ⓜ

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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing
   per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

TEXAS
INSTRUMENTS
www.ti.com

12X (0.6)

1

12X (0.25)

SYMM
℄

10X (0.5)

6

(1.5)

SYMM
℄

13

(Ø 0.2) VIA
TYP

(0.5)

(R0.05) TYP

12

(2.5)

(1)

7

(2.8)

LAND PATTERN EXAMPLE
SCALE:20X

0.07 MAX
ALL AROUND

SOLDER MASK
OPENING

METAL

**NON SOLDER MASK
DEFINED
(PREFERRED)**

0.07 MIN
ALL AROUND

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

**SOLDER MASK
DEFINED**
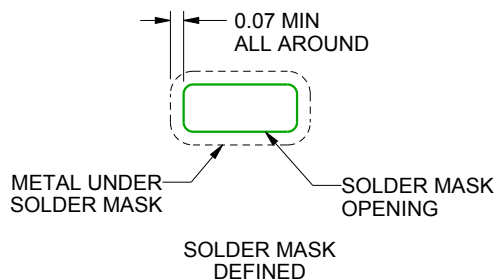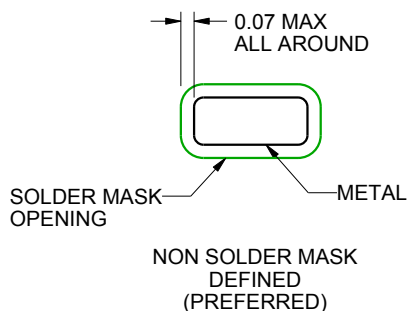
SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature
   number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown
   on this view. It is recommended that vias under paste be filled, plugged or tented.

12X (0.6)

1

12X (0.25)

2X (1.38)

12

2X (1.11)

SYMM

(0.66)

10X (0.5)

6

13

7

SYMM

METAL
TYP

(2.8)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 13
81.7% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.