

UCC2732x/UCC3732x イネーブル機能搭載、シングル、9A 高速ローサイド MOSFET ドライバ

1 特長

- イネーブル機能を追加した業界標準のピン配置
- TrueDrive を使用して、ミラー プラトー領域で $\pm 9A$ の高いピーク電流駆動能力
- 独自のバイポーラおよび CMOS 出力段を使用した効率的な定電流ソーシング
- 電源電圧から独立した TTL/CMOS 互換入力
- 標準立ち上がり時 / 立ち下がり時 20ns (10nF 負荷時)
- 標準伝播遅延時間: 25ns (入力立ち下がり時)、35ns (入力立ち上がり時)
- 電源電圧: 4V ~ 15V
- 熱的に強化された MSOP PowerPAD™ パッケージ、 $4.7^{\circ}\text{C}/\text{W} \theta_{\text{jc}}$ で供給
- $-40^{\circ}\text{C} \sim +105^{\circ}\text{C}$ で仕様を規定
- 8 ピン SOIC および PDIP パッケージでの鉛フリー仕上げ (CU NIPDAU)

2 アプリケーション

- スイッチ・モード電源
- DC/DC コンバータ
- モーター・コントローラ
- Class-D スwitchング アンプ
- ライン・ドライバ
- パルストランスドライバ

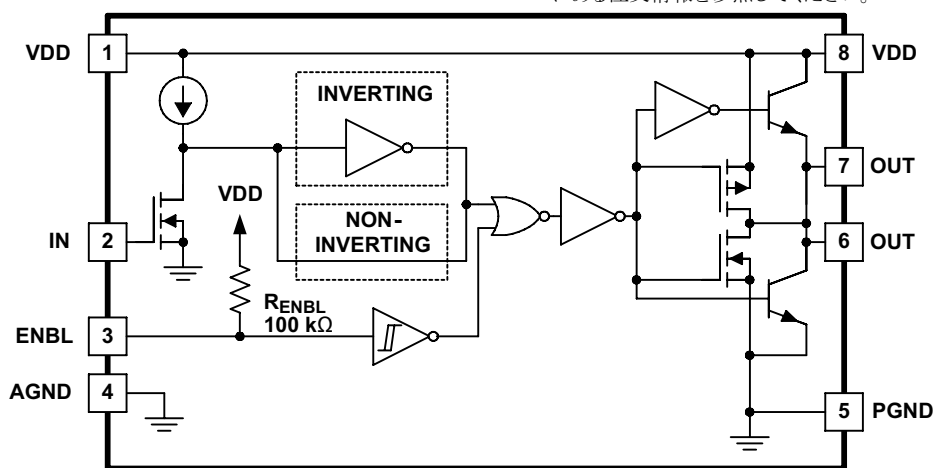
3 概要

UCC2732x/UCC3732x ファミリの高速ドライバは、業界標準のピン配置で 9A のピーク駆動電流を供給します。これらのドライバは、高い dV/dt 遷移により極端なミラー電流を必要とするシステム向けに、最大の MOSFET を駆動できます。この結果、外部回路の追加が不要になり、複数の部品を置き換え、スペースの節減、設計の複雑さの緩和、組み立てコストの削減が可能になります。反転 (UCC37321) と非反転 (UCC37322) の 2 つの標準ロジック オプションが用意されています。

製品情報

部品番号	パッケージ ⁽¹⁾	本体サイズ (公称)
UCC2732x	MSOP-PowerPAD (8)	3.00mm × 3.00mm
UCC3732x	SOIC (8)	3.91mm × 4.90mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。



ブロック図



Table of Contents

1 特長	1	9 Application and Implementation	17
2 アプリケーション	1	9.1 Application Information.....	17
3 概要	1	9.2 Typical Application.....	17
4 概要 (続き)	3	10 Power Supply Recommendations	22
5 Related Products	4	11 Layout	22
6 Pin Configuration and Functions	5	11.1 Layout Guidelines.....	22
7 Specifications	6	11.2 Layout Example.....	23
7.1 Absolute Maximum Ratings.....	6	11.3 Thermal Considerations.....	23
7.2 ESD Ratings.....	6	12 Device and Documentation Support	24
7.3 Recommended Operating Conditions.....	6	12.1 Device Support.....	24
7.4 Thermal Information.....	6	12.2 Documentation Support.....	24
7.5 Electrical Characteristics.....	7	12.3 ドキュメントの更新通知を受け取る方法.....	24
7.6 Switching Characteristics.....	8	12.4 サポート・リソース.....	24
7.7 Power Dissipation Ratings.....	8	12.5 Trademarks.....	24
7.8 Typical Characteristics.....	10	12.6 静電気放電に関する注意事項.....	24
8 Detailed Description	14	12.7 用語集.....	24
8.1 Overview.....	14	13 Revision History	25
8.2 Functional Block Diagram.....	14	14 Mechanical, Packaging, and Orderable Information	25
8.3 Feature Description.....	14		
8.4 Device Functional Modes.....	16		

4 概要 (続き)

貫通電流を本質的に最小化する設計により、これらの出力は、MOSFET のスイッチング遷移中のミラー プラトー領域で最も必要とされる、高いゲート駆動電流を供給できます。バイポーラと MOSFET トランジスタを並列接続した独自のハイブリッド出力段 (TrueDrive) により、低い電源電圧で効率的な電流供給が可能になります。この駆動アーキテクチャにより、UCC3732x は業界標準の 6A、9A、および多くの 12A ドライバ アプリケーションで使用できます。ラッチアップおよび ESD 保護回路も搭載されています。最後に、UCC3732x にはイネーブル (ENBL) 機能があり、ドライバ アプリケーションの動作をより的確に制御できます。ENBL は、業界標準のピン配置では未使用のままにしてあったピン 3 に実装されています。このピンは、アクティブ ハイ ロジックでは内部で V_{DD} にプルアップされ、標準動作時にはオープンのままにできます。

8 ピン SOIC (D) パッケージ製品に加えて、UCC3732x は熱的に強化された小型の 8 ピン MSOP PowerPAD™ (DGN) パッケージでも供給されます。PowerPAD パッケージは熱抵抗を大幅に低減するため、温度動作範囲が拡張され、長期的な信頼性が向上します。

5 Related Products

PRODUCT	DESCRIPTION	PACKAGES
UCC37323/4/5	Dual 4-A Low-Side Drivers	MSOP–8 PowerPAD, SOIC–8, PDIP–8
UCC27423/4/5	Dual 4-A Low-Side Drivers with Enable	MSOP–8 PowerPAD, SOIC–8, PDIP–8
TPS2811/12/13	Dual 2-A Low-Side Drivers with Internal Regulator	TSSOP–8, SOIC–8, PDIP–8
TPS2814/15	Dual 2-A Low-Side Drivers with Two Inputs per Channel	TSSOP–8, SOIC–8, PDIP–8
TPS2816/17/18/19	Single 2-A Low-Side Driver with Internal Regulator	5-Pin SOT–23
TPS2828/29	Single 2-A Low-Side Driver	5-Pin SOT–23

6 Pin Configuration and Functions

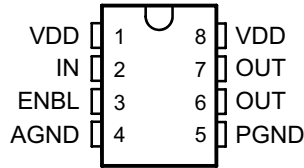


図 6-1. D, and DGN Packages 8-Pin SOIC, and MSOP With PowerPAD Top View

表 6-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AGND	4	—	The AGND and the PGND must be connected by a single thick trace directly under the device. There must be a low ESR, low ESL capacitor of 0.1 μ F between VDD (pin 8) and PGND and a separate 0.1- μ F capacitor between VDD (pin 1) and AGND. The power MOSFETs must be located on the PGND side of the device while the control circuit must be on the AGND side of the device. The control circuit ground must be common with the AGND while the PGND must be common with the source of the power FETs.
ENBL	3	I	Enable input for the driver with logic compatible threshold and hysteresis. The driver output can be enabled and disabled with this pin. It is internally pulled up to V _{DD} with 100-k Ω resistor for active high operation. When the device is disabled, the output state is, low regardless of the input state.
IN	2	I	Input signal of the driver which has logic compatible threshold and hysteresis.
OUT	6, 7	O	Driver outputs that must be connected together externally. The output stage is capable of providing 9-A peak drive current to the gate of a power MOSFET.
PGND	5	—	Common ground for output stage. This ground must be connected very closely to the source of the power MOSFET which the driver is driving. Grounds are separated to minimize ringing affects due to output switching di/dt which can affect the input threshold.
VDD	1, 8	I	Supply voltage and the power input connections for this device. Two pins must be connected together externally.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾ ⁽²⁾

		MIN	MAX	UNIT
Supply voltage, V_{DD}		-0.3	16	V
Output current (OUT) DC, I_{OUT_DC}			0.6	A
Input voltage (IN), V_{IN}		-0.3	6 V or $V_{DD} + 0.3^{(3)}$	V
Enable voltage (ENBL)		-0.3	6 V or $V_{DD} + 0.3^{(3)}$	V
Power dissipation at $T_A = 25^\circ\text{C}$	D package		650	mW
	DGN package		3	W
	P package		350	mW
Lead temperature (soldering, 10 s)			300	$^\circ\text{C}$
Junction operating temperature, T_J		-55	150	$^\circ\text{C}$
Storage temperature, T_{stg}		-65	150	$^\circ\text{C}$

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under [セクション 7.3 Recommended Operating Conditions](#). Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to GND. Currents are positive into, negative out of the specified terminal.
- (3) Whichever is larger

7.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	± 2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	± 1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage, VDD	4.5		15	V

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		UCC27322	UCC27321		UNIT
		D (SOIC)	P (PDIP)	DGN (MSOP-PowerPAD)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	56.6	55.9	56.7	$^\circ\text{C}/\text{W}$
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	52.8	45.3	52.9	$^\circ\text{C}/\text{W}$
$R_{\theta JB}$	Junction-to-board thermal resistance	32.6	32.6	32.7	$^\circ\text{C}/\text{W}$
ψ_{JT}	Junction-to-top characterization parameter	1.8	23.0	1.8	$^\circ\text{C}/\text{W}$
ψ_{JB}	Junction-to-board characterization parameter	32.3	32.5	32.4	$^\circ\text{C}/\text{W}$
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	5.9	—	5.9	$^\circ\text{C}/\text{W}$

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

7.5 Electrical Characteristics

$V_{DD} = 4.5\text{ V to }15\text{ V}$, $T_A = -40^\circ\text{C to }+105^\circ\text{C}$ for UCC2732x, $T_A = 0^\circ\text{C to }70^\circ\text{C}$ for UCC3732x, $T_A = T_J$, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT (IN)						
V_{IN_H} , logic 1 input threshold			1.6	2.2	2.5	V
V_{IN_L} , logic 0 input threshold			0.8	1.2	1.5	V
Input current		$0\text{ V} \leq V_{IN} \leq V_{DD}$	-10	0	10	μA
OUTPUT (OUT)						
Peak output current ⁽¹⁾		$V_{DD} = 14\text{ V}$,		9		A
Output resistance high ⁽²⁾		$I_{OUT} = -10\text{ mA}$		0.6	1.5	Ω
Output resistance low ⁽²⁾		$I_{OUT} = 10\text{ mA}$		0.4	1	Ω
OVERALL						
I_{DD} , static operating current	UCC37321 UCC27321	IN = LOW, EN = LOW, $V_{DD} = 15\text{ V}$		150	225	μA
		IN = HIGH, EN = LOW, $V_{DD} = 15\text{ V}$		440	650	
		IN = LOW, EN = HIGH, $V_{DD} = 15\text{ V}$		370	550	
		IN = HIGH, EN = HIGH, $V_{DD} = 15\text{ V}$		370	550	
	UCC37322 UCC27322	IN = LOW, EN = LOW, $V_{DD} = 15\text{ V}$		150	225	
		IN = HIGH, EN = LOW, $V_{DD} = 15\text{ V}$		450	650	
		IN = LOW, EN = HIGH, $V_{DD} = 15\text{ V}$		75	125	
		IN = HIGH, EN = HIGH, $V_{DD} = 15\text{ V}$		675	1000	
ENABLE (ENBL)						
V_{EN_H} , high-level enable voltage		LOW to HIGH transition	1.7	2.2	2.7	V
V_{EN_L} , low-level enable voltage		HIGH to LOW transition	1.1	1.6	2	V
Hysteresis			0.25	0.55	0.90	
R_{ENBL} , enable impedance		$V_{DD} = 14\text{ V}$, ENBL = GND	75	100	135	k Ω

(1) Not tested in production.

(2) Output pullup resistance here is a DC measurement that measures resistance of PMOS structure only, not N-channel structure.

7.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ENABLE (ENBL)					
t_{D3} , propagation delay time ⁽¹⁾	$C_{LOAD} = 10 \text{ nF}$		60	90	ns
t_{D4} , propagation delay time ⁽¹⁾	$C_{LOAD} = 10 \text{ nF}$		60	90	ns
SWITCHING TIME⁽²⁾					
t_R , rise time (OUT)	$C_{LOAD} = 10 \text{ nF}$		20	70	ns
t_F , fall time (OUT)	$C_{LOAD} = 10 \text{ nF}$		20	30	ns
t_{D1} , propagation delay, IN rising (IN to OUT)	$C_{LOAD} = 10 \text{ nF}$		25	70	ns
t_{D2} , propagation delay, IN falling (IN to OUT)	$C_{LOAD} = 10 \text{ nF}$		35	70	ns

(1) See [Figure 7-2](#).

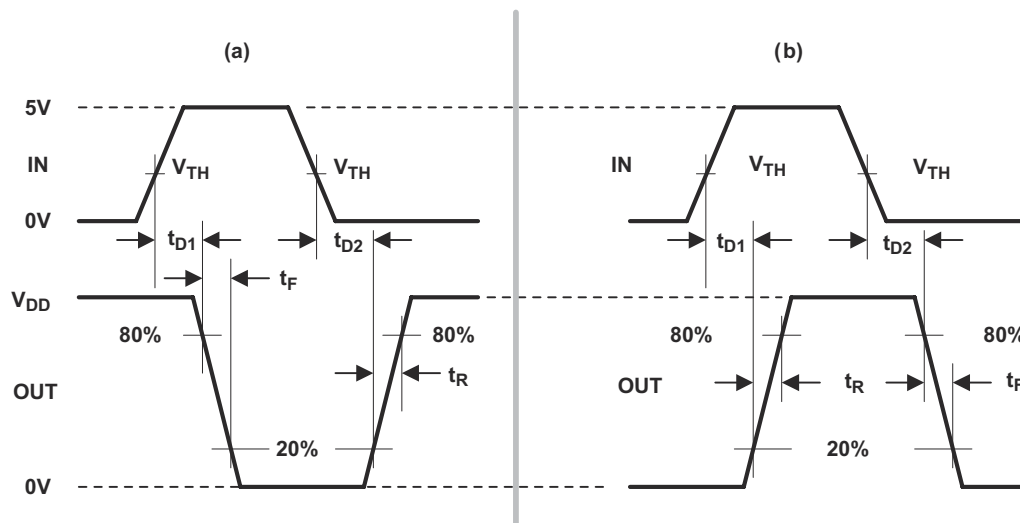
(2) See [Figure 7-1](#) for switching waveforms.

7.7 Power Dissipation Ratings

PACKAGE	SUFFIX	θ_{jc} (°C/W)	θ_{ja} (°C/W)	Power Rating (mW) $T_A = 70^\circ\text{C}$ ⁽¹⁾	Derating Factor Above 70°C (mW/°C) ⁽¹⁾
SOIC-8	D	42	84 to 160 ⁽²⁾	344 to 655 ⁽²⁾	6.25 to 11.9 ⁽²⁾
MSOP PowerPAD-8	DGN	4.7	50 to 59	1370	17.1

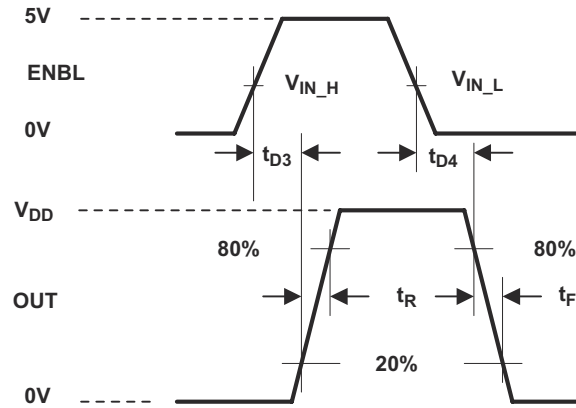
(1) 125°C operating junction temperature is used for power rating calculations

(2) The range of values indicates the effect of the printed-circuit-board. These values are intended to give the system designer an indication of the best and worst case conditions. In general, the system designer should attempt to use larger traces on the printed-circuit-board where possible to spread the heat away from the device more effectively. For additional information on device temperature management, see the *Packaging Information* section of the *Power Supply Control Products Data Book*, ([SLUD003](#)).



The 20% and 80% thresholds depict the dynamics of the BiPolar output devices that dominate the power MOSFET transition through the Miller regions of operation.

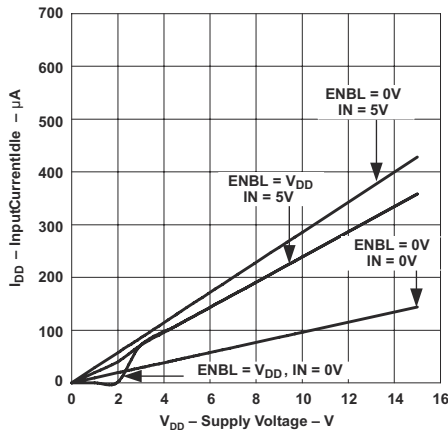
Figure 7-1. Switching Waveforms for (a) Inverting Input to (b) Output Times



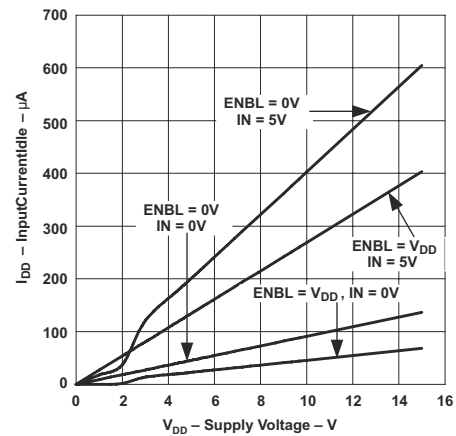
The 20% and 80% thresholds depict the dynamics of the BiPolar output devices that dominate the power MOSFET transition through the Miller regions of operation.

☒ 7-2. Switching Waveform for Enable to Output

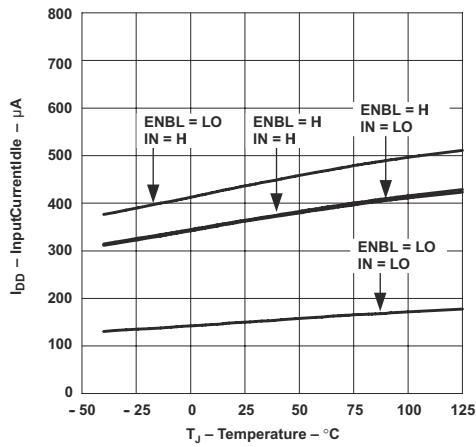
7.8 Typical Characteristics



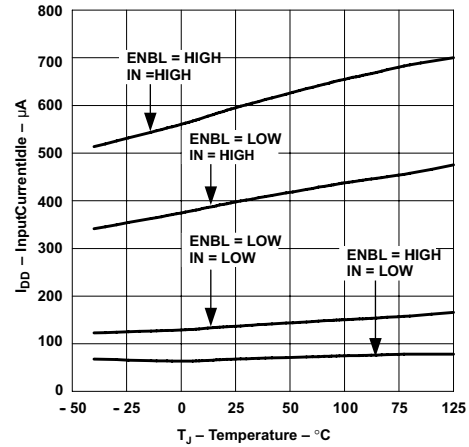
7-3. Input Current Idle vs Supply Voltage (UCCx7321)



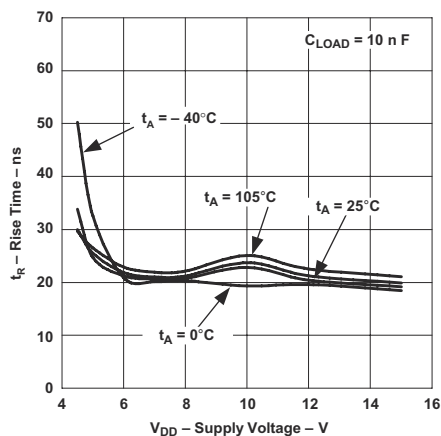
7-4. Input Current Idle vs Supply Voltage (UCCx7322)



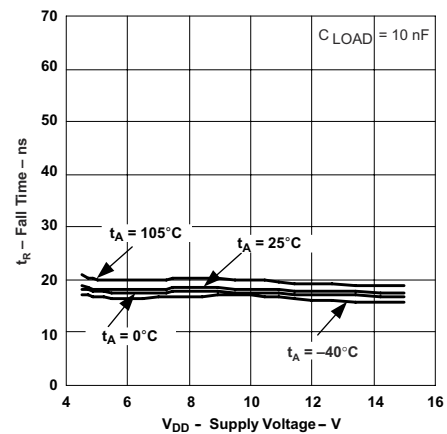
7-5. Input Current Idle vs Temperature (UCCx7321)



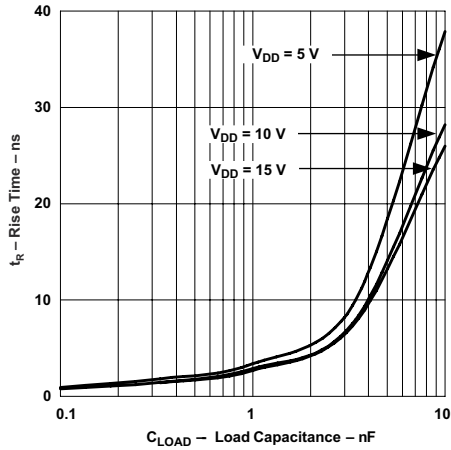
7-6. Input Current Idle vs Temperature (UCCx7322)



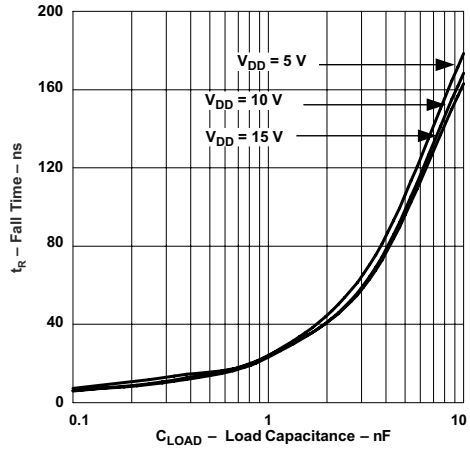
7-7. Rise Time vs Supply Voltage



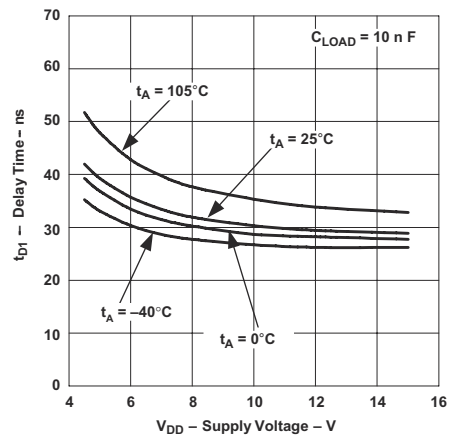
7-8. Fall Time vs Supply Voltage



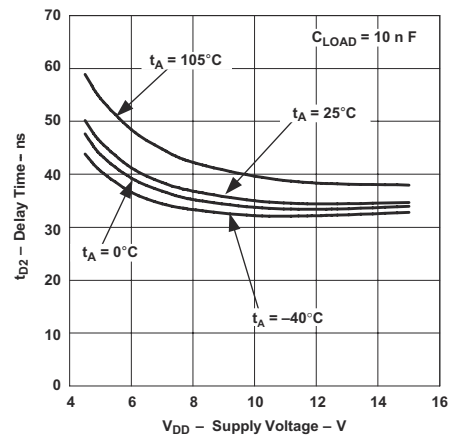
7-9. Rise Time vs Load Capacitance



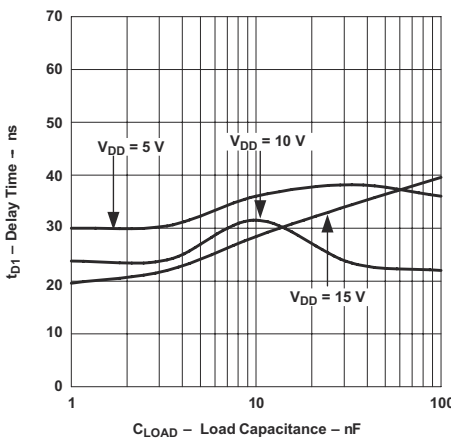
7-10. Fall Time vs Output Capacitance



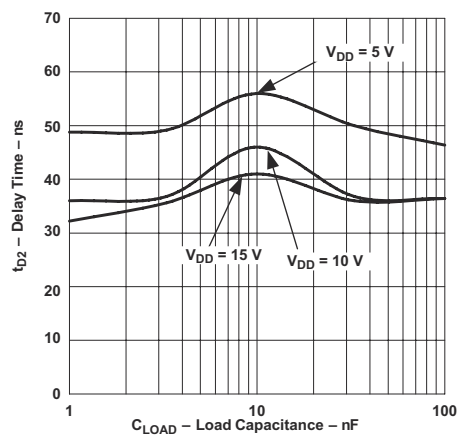
7-11. t_{D1} Delay Time vs Supply Voltage



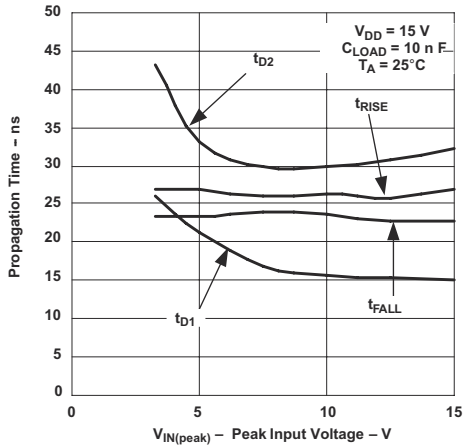
7-12. t_{D2} Delay Time vs Supply Voltage



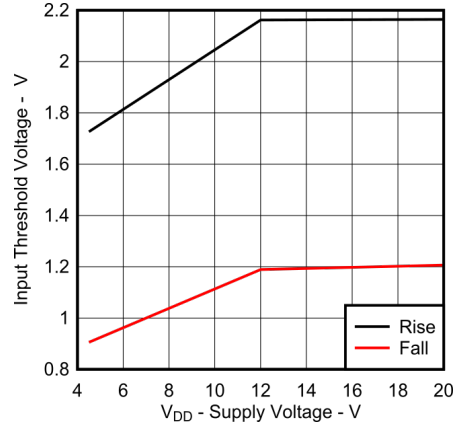
7-13. t_{D1} Delay Time vs Load Capacitance



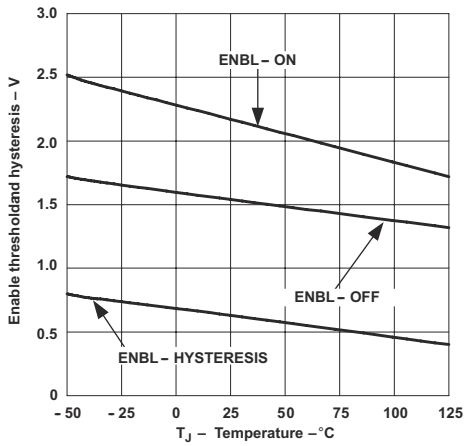
7-14. t_{D2} Delay Time vs Load Capacitance



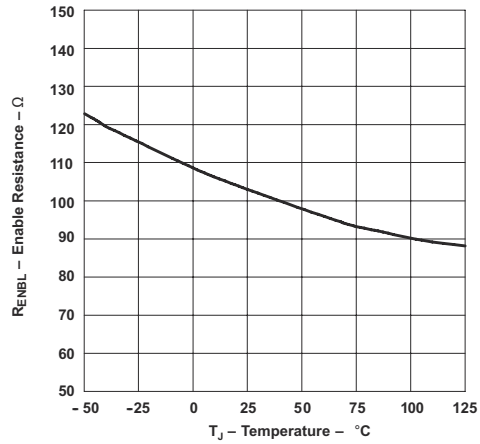
7-15. Propagation Times vs Peak Input Voltage



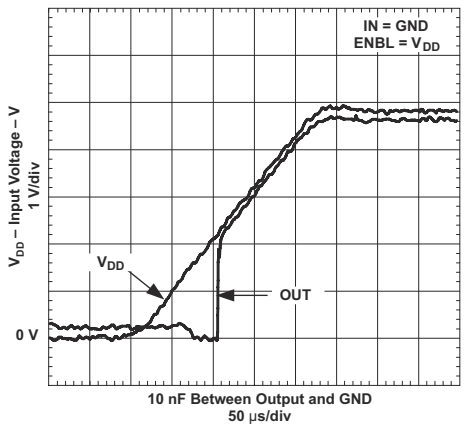
7-16. Input Threshold vs Supply Voltage



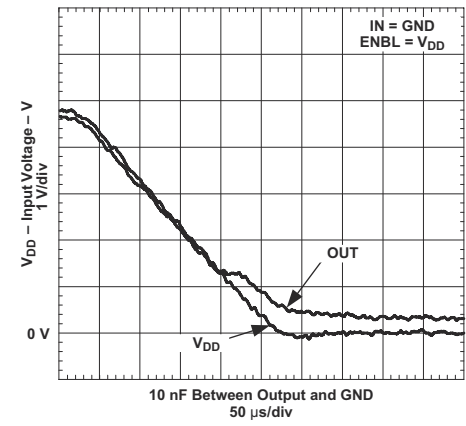
7-17. Enable Threshold and Hysteresis vs Temperature



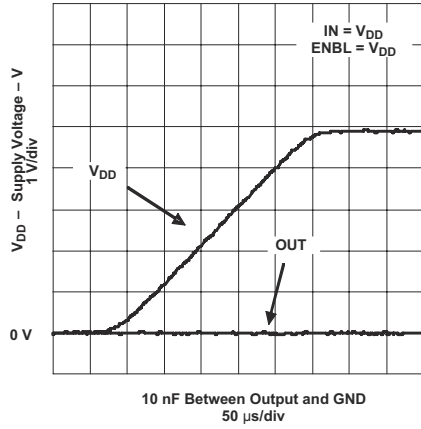
7-18. Enable Resistance vs Temperature



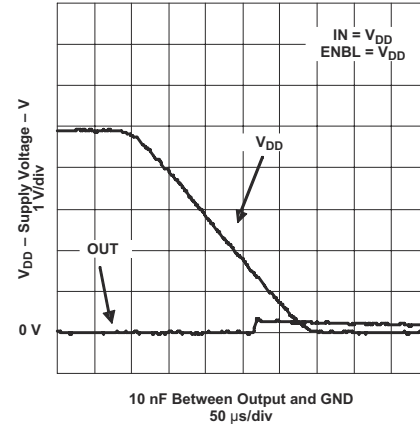
7-19. Output Behavior vs V_{DD} (UCC37321)



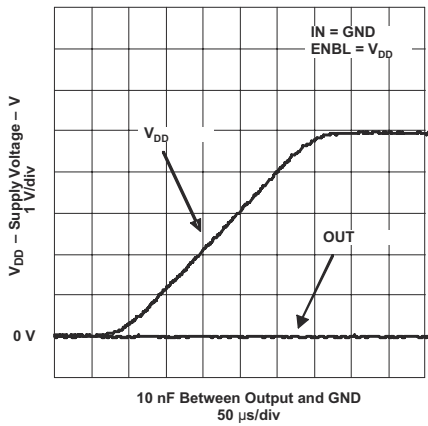
7-20. Output Behavior vs V_{DD} (UCC37321)



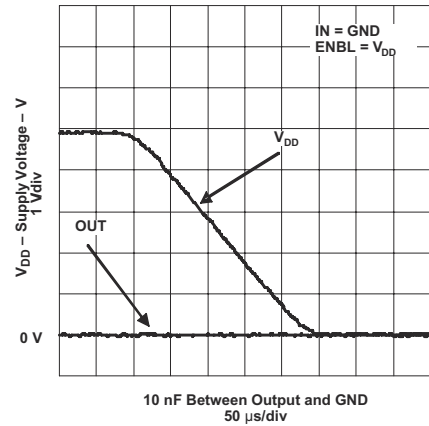

7-21. Output Behavior vs VDD (Inverting)




7-22. Output Behavior vs VDD (Inverting)




7-23. Output Behavior vs VDD (Noninverting)




7-24. Output Behavior vs VDD (Noninverting)

8 Detailed Description

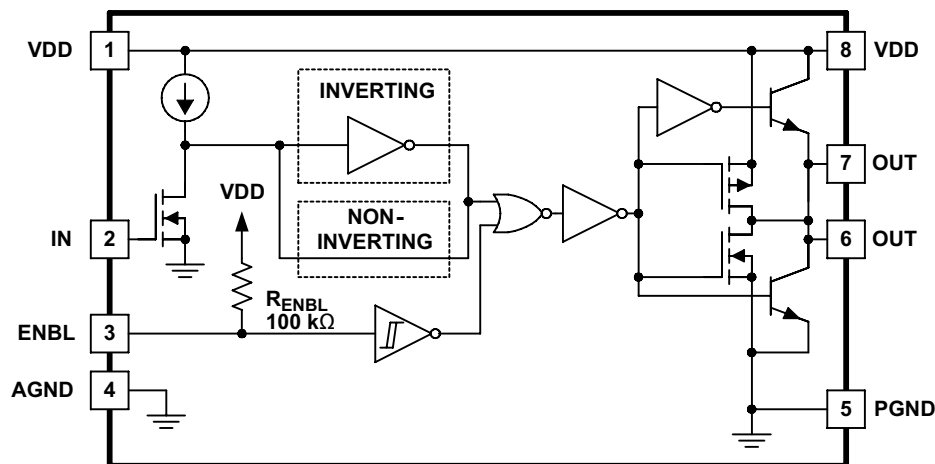
8.1 Overview

The UCC37321 and UCC37322 drivers serve as an interface between low-power controllers and power MOSFETs. They can also be used as an interface between DSPs and power MOSFETs. High-frequency power supplies often require high-speed, high-current drivers such as the UCC3732x family. A leading application is the need to provide a high power buffer stage between the PWM output of the control device and the gates of the primary power MOSFET or IGBT switching devices. In other cases, the device drives the power device gates through a drive transformer. Synchronous rectification supplies must simultaneously drive multiple devices which can present an extremely large load to the control circuitry.

The inverting driver (UCC37321) is useful for generating inverted gate drive signals from controllers that have only outputs of the opposite polarity. For example, this driver can provide a gate signal for ground referenced, N-channel synchronous rectifier MOSFETs in buck derived converters. This driver can also be used for generating a gate drive signal for a P-channel MOSFET from a controller that is designed for N-channel applications.

MOSFET gate drivers are generally used when it is not feasible to have the primary PWM regulator device directly drive the switching devices for one or more reasons. The PWM device may not have the brute drive capability required for the intended switching MOSFET, limiting the switching performance in the application. In other cases there may be a desire to minimize the effect of high-frequency switching noise by placing the high current driver physically close to the load. Also, newer devices that target the highest operating frequencies may not incorporate onboard gate drivers at all. Their PWM outputs are only intended to drive the high impedance input to a driver such as the UCC3732x. Finally, the control device may be under thermal stress due to power dissipation, and an external driver can help by moving the heat from the controller to an external package.

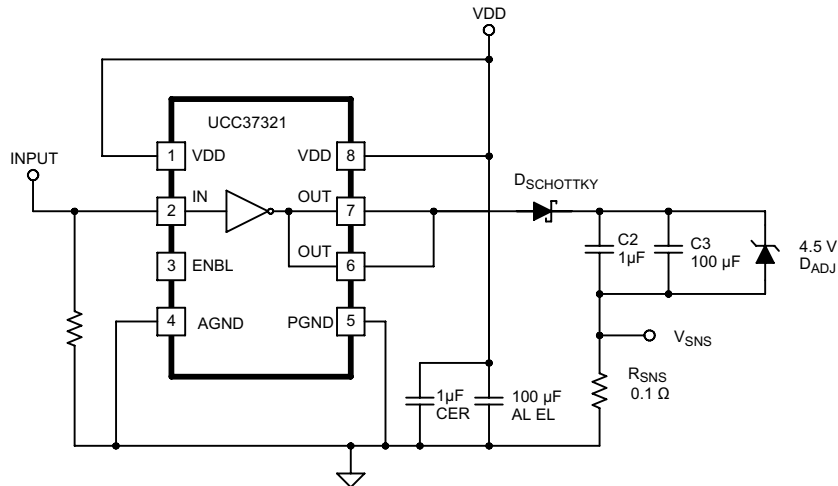
8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Input Stage

The IN threshold has a 3.3-V logic sensitivity over the full range of VDD voltages; yet, it is equally compatible with 0 V to VDD signals. The inputs of UCC3732x family of drivers are designed to withstand 500-mA reverse current without either damage to the device or logic upset. In addition, the input threshold turnoff of the UCC3732x has been slightly raised for improved noise immunity. The input stage of each driver must be driven by a signal with a short rise or fall time. This condition is satisfied in typical power supply applications, where the input signals are provided by a PWM controller or logic gates with fast transition times (< 200 ns). The IN input of the driver functions as a digital gate, and it is not intended for applications where a slow changing input voltage is used to generate a switching output when the logic threshold of the input section is reached. While this may not be harmful to the driver, the output of the driver may switch repeatedly at a high frequency.



UDG-01114

図 8-2. Source Current Test Circuit

Note that the current sink capability is slightly stronger than the current source capability at lower VDD. This is due to the differences in the structure of the bipolar-MOSFET power output section, where the current source is a P-channel MOSFET and the current sink has an N-channel MOSFET.

In most it is advantageous that the turnoff capability of a driver is stronger than the turnon capability. This helps to ensure that the MOSFET is held OFF during common power supply transients which may turn the device back ON.

8.3.4 Enable

The UCC37321/2 provides an enable input for improved control of the driver operation. This input also incorporates logic compatible thresholds with hysteresis. It is internally pulled up to VDD with 100-kΩ resistor for active high operation. When ENBL is high, the device is enabled and when ENBL is low, the device is disabled. The default state of the ENBL pin is to enable the device and therefore it can be left open for standard operation. The output state when the device is disabled is low regardless of the input state. See 表 8-1 for the operation using enable logic.

ENBL input is compatible with both logic signals and slow changing analog signals. It can be directly driven or a power-up delay can be programmed with a capacitor between ENBL and AGND.

8.4 Device Functional Modes

表 8-1 lists the logic of this device.

表 8-1. Device Logic Table

	ENBL	IN	OUT
INVERTING UCC37321	0	0	0
	0	1	0
	1	0	1
	1	1	0
NON-- INVERTING UCC37322	0	0	0
	0	1	0
	1	0	0
	1	1	1

9 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくこととなります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

9.1 Application Information

High-current gate driver devices are required in switching power applications for a variety of reasons. To enable fast switching of power devices and reduce associated power losses, a powerful gate driver can be employed between the PWM output of controllers or signal isolation devices and the gates of the power semiconductor devices. Further, gate drivers are indispensable when sometimes it is just not feasible to have the PWM controller directly drive the gates of the switching devices. The situation may be encountered because the PWM signal from a digital controller or signal isolation device is often a 3.3-V or 5-V logic signal which is not capable of effectively turning on a power switch. A level-shifting circuitry is needed to boost the logic-level signal to the gate-drive voltage to fully turn on the power device and minimize conduction losses. Traditional buffer drive circuits based on NPN/PNP bipolar, (or P- N- channel MOSFET), transistors in totem-pole arrangement, being emitter follower configurations, prove inadequate for this because they lack level-shifting capability and low-drive voltage protection. Gate drivers effectively combine both the level-shifting and buffer drive functions. Gate drivers may also minimize the effect of switching noise by locating the high-current driver physically close to the power switch, drive gate-driver transformers and control floating power device gates, reducing power dissipation and thermal stress in controllers by absorbing gate-charge power losses.

In summary gate drivers are extremely important components in switching power combining benefits of high-performance, low-cost, low component count, board-space reduction, and simplified system design.

9.2 Typical Application

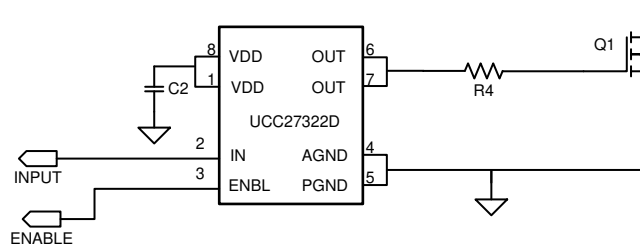


図 9-1. Typical Application Diagram of UCC27322 and UCC37322

9.2.1 Design Requirements

When selecting the proper gate driver device for an end application, some design considerations must be evaluated first to make the most appropriate selection. The following design parameters should be used when selecting the proper gate driver device for an end application: input-to-output configuration, the input threshold type, bias supply voltage levels, peak source and sink currents, availability of independent enable and disable functions, propagation delay, power dissipation, and package type. See the example design parameters and requirements in 表 9-1.

表 9-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input-to-output configuration	Noninverting
Input threshold type	CMOS
Bias supply voltage levels	12 V
dVDS/dt ⁽¹⁾	20 V/ns
Enable function	Yes
Propagation delay	< 50 ns
Power dissipation	< 0.45 W
Package type	SOIC (8)

(1) dVDS/dt is a typical requirement for a given design. This value can be used to find the peak source/sink currents needed as shown in [セクション 9.2.2.4](#).

9.2.2 Detailed Design Procedure

9.2.2.1 Input-to-Output Configuration

The design should specify which type of input-to-out configuration should be used. If turning on the power MOSFET or IGBT when the input signal is in high state is preferred, then a device capable of the noninverting configuration must be selected. If turning off the power MOSFET or IGBT when the input signal is in high state is preferred, then a device capable of the inverting configuration must be chosen. Based on this noninverting requirement of this application, the proper device out of the UCC27322 or UCC37322 should be selected.

9.2.2.2 Input Threshold Type

The type of input voltage threshold determines the type of controller that can be used with the gate driver device. The UCC2732x and UCC3732x devices feature a TTL and CMOS-compatible input threshold logic, with wide hysteresis. The threshold voltage levels are low voltage and independent of the V_{DD} supply voltage, which allows compatibility with both logic-level input signals from microcontrollers as well as higher-voltage input signals from analog controllers. See [セクション 7.5](#) for the actual input threshold voltage levels and hysteresis specifications for the UCC2732x and UCC3732x devices.

9.2.2.3 VDD Bias Supply Voltage

The bias supply voltage to be applied to the V_{DD} pins of the device must never exceed the values listed in [セクション 7.3](#). However, different power switches require different voltage levels to be applied at the gate. With a wide operating range from 4.5 V to 15 V, the UCC2732x and UCC3732x can be used to drive a variety of power switches, such as Si MOSFETs (for example, $V_{GS} = 4.5$ V, 10 V, 12 V), IGBTs ($V_{GE}=15$ V), and wide-bandgap power semiconductors (such as GaN, certain types of which allow no higher than 6 V to be applied to the gate terminals).

9.2.2.4 Peak Source and Sink Currents

Generally, the switching speed of the power switch during turnon and turnoff must be as fast as possible to minimize switching power losses. The gate driver device must be able to provide the required peak current for achieving the targeted switching speeds for the targeted power MOSFET.

Using the example of a power MOSFET, the system requirement for the switching speed is typically described in terms of the slew rate of the drain-to-source voltage of the power MOSFET (such as dV_{DS}/dt). For example, the system requirement might state that a SPP20N60C3 power MOSFET must be turned on with a Dv_{ds}/dt of 20 V/ns or higher under a DC bus voltage of 400 V in a continuous-conduction-mode (CCM) boost PFC-converter application. This type of application is an inductive hard-switching application and reducing switching power loss is critical. This requirement means that the entire drain-to-source voltage swing during power MOSFET turnon event (from 400 V in the OFF state to $V_{DS(on)}$ in ON state) must be completed in approximately 20 ns or less. When the drain-to-source voltage swing occurs, the Miller charge of the power MOSFET (Q_{gd} parameter in SPP20N60C3 power MOSFET data sheet is 33 nC typically) is supplied by the peak current of gate driver.

According to power MOSFET inductive switching mechanism, the gate-to-source voltage of the power MOSFET at this time is the Miller plateau voltage, which is typically a few volts higher than the threshold voltage of the power MOSFET, $V_{GS(th)}$).

To achieve the targeted Dv/dt , the gate driver must be capable of providing the Q_{gd} charge in 20 ns or less. In other words, a peak current of 1.65 A (= 33 nC) / 20 ns) or higher must be provided by the gate driver. The UCC2732x and UCC3732x devices can provide 9-A peak sourcing/sinking current which clearly exceeds the design requirement and has the capability to meet the switching speed needed. This 9-A peak sourcing/sinking current provides an extra margin against part-to-part variations in the Q_{gd} parameter of the power MOSFET along with additional flexibility to insert external gate resistors and fine tune the switching speed for efficiency versus EMI optimizations. However, in practical designs the parasitic trace in the gate driver circuit of the PCB will have a definitive role to play on the power MOSFET switching speed. The effort of this trace inductance is to limit the di/dt of the output current pulse of the gate driver. To illustrate this effect, consider output current pulse waveform from the gate driver to be approximated to a triangular profile, where the area under the triangle ($0.5 \times I_{PEAK} \times \text{time}$) would equal the total gate charge of the power MOSFET (Q_g parameter in SPP20N60C3 power MOSFET data sheet= 87 nC typically). If the parasitic trace inductance limits the di/dt then a situation may occur in which the full peak current capability of the gate driver is not fully achieved in the time required to deliver the Q_g required for the power MOSFET switching. In other words, the time parameter in the equation would dominate and the I_{PEAK} value of the current pulse would be much less than the true peak current capability of the device, while the required Q_g is still delivered. Because of this, the desired switching speed may not be realized, even when theoretical calculations indicate the gate driver can achieve the targeted switching speed. Thus, placing the gate driver device very close to the power MOSFET and designing a tight gate drive-loop with minimal PCB trace inductance is important to realize the full peak-current capability of the gate driver.

9.2.2.5 Enable and Disable Function

Certain applications demand independent control of the output state of the driver without involving the input signal. A pin which offers enable and disable functions achieves the requirements. For these applications, the UCC2732x and UCC3732x are suitable as they feature an input pin and an Enable pin.

9.2.2.6 Propagation Delay

The acceptable propagation delay from the gate driver is dependent on the switching frequency at which it is used and the acceptable level of pulse distortion to the system. The UCC2732x and UCC3732x devices feature 25-ns turnon propagation delay and 35-ns turnoff propagation delay (typical), which ensure very little distortion and allow operation at higher frequencies. See [セクション 7.5](#) for the propagation and [セクション 7.6](#) of the UCC2732x and UCC3732x devices.

9.2.2.7 Power Dissipation

The UCC3732x family of drivers are capable of delivering 9-A of current to a MOSFET gate for a period of several hundred nanoseconds. High peak current is required to turn an N-channel device ON quickly. Then, to turn the device OFF, the driver is required to sink a similar amount of current to ground. This repeats at the operating frequency of the power device. An N-channel MOSFET is used in this discussion because it is the most common type of switching device used in high-frequency power conversion equipment.

References [1](#) and [2](#) contain detailed discussions of the drive current required to drive a power MOSFET and other capacitive-input switching devices. Much information is provided in tabular form to give a range of the current required for various devices at various frequencies. The information pertinent to calculating gate drive current requirements will be summarized here; the original document is available from the TI website.

When a driver device is tested with a discrete, capacitive load it is a fairly simple matter to calculate the power that is required from the bias supply. The energy that must be transferred from the bias supply to charge the capacitor is given by [式 1](#).

$$E = \frac{1}{2} CV^2 \tag{1}$$

where

- C is the load capacitor
- V is the bias voltage feeding the driver

There is an equal amount of energy transferred to ground when the capacitor is discharged. This leads to a power loss given by 式 2.

$$P = 2 \times \frac{1}{2} CV^2 f \quad (2)$$

where

- f is the switching frequency

This power is dissipated in the resistive elements of the circuit. Thus, with no external resistor between the driver and gate, this power is dissipated inside the driver. Half of the total power is dissipated when the capacitor is charged, and the other half is dissipated when the capacitor is discharged. An example using the conditions of the previous gate-drive waveform should help clarify this.

With $V_{DD} = 12\text{ V}$, $C_{LOAD} = 10\text{ nF}$, and $f = 300\text{ kHz}$, the power loss can be calculated as shown in 式 4.

$$P = 10\text{ nF} \times (12)^2 \times (300\text{ kHz}) = 0.432\text{ W} \quad (3)$$

With a 12-V supply, this would equate, as shown in 式 4, to a current of:

$$I = \frac{P}{V} = \frac{0.432\text{ W}}{12\text{ V}} = 0.036\text{ A} \quad (4)$$

The switching load presented by a power MOSFET can be converted to an equivalent capacitance by examining the gate charge required to switch the device. This gate charge includes the effects of the input capacitance plus the added charge needed to swing the drain of the device between the ON and OFF states. Most manufacturers provide specifications that provide the typical and maximum gate charge, in nC, to switch the device under specified conditions. Using the gate charge Q_g , one can determine the power that must be dissipated when charging a capacitor. This is done by using the equivalence $Q_g = C_{eff}V$ to provide 式 5 for power.

$$P = C \times V^2 \times f = Q_g \times V \times f \quad (5)$$

式 5 allows a power designer to calculate the bias power required to drive a specific MOSFET gate at a specific bias voltage.

9.2.3 Application Curves

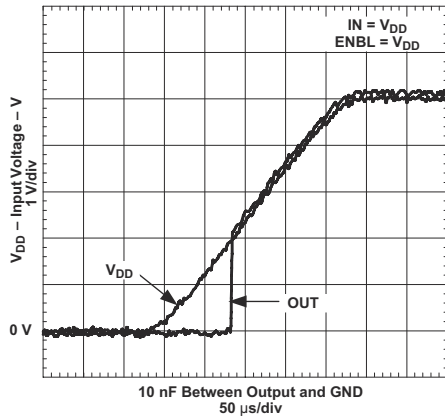


図 9-2. Output Behavior vs VDD (UCC37322)

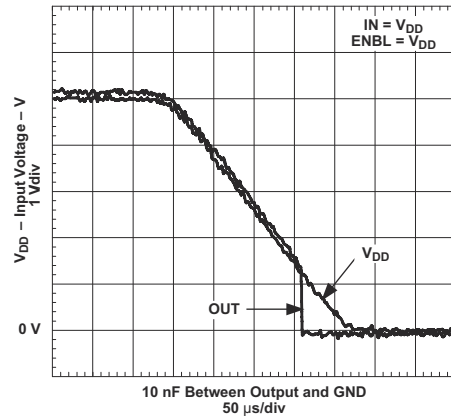


図 9-3. Output Behavior vs VDD (UCC37322)

10 Power Supply Recommendations

Although quiescent VDD current is very low, total supply current is higher, depending on OUTA and OUTB current and the operating frequency. Total VDD current is the sum of quiescent VDD current and the average OUT current. Knowing the operating frequency and the MOSFET gate charge (Qg), average OUT current can be calculated using 式 6.

$$I_{OUT} = Qg \times f \quad (6)$$

where

- f is frequency

For the best high-speed circuit performance, TI recommends two V_{DD} bypass capacitors to prevent noise problems. TI also highly recommends using surface mount components. A 0.1-μF ceramic capacitor must be placed closest to the VDD to ground connection. In addition, a larger capacitor (such as 1 μF) with relatively low ESR should be connected in parallel to help deliver the high current peaks to the load. The parallel combination of capacitors presents a low impedance characteristic for the expected current levels in the driver application.

11 Layout

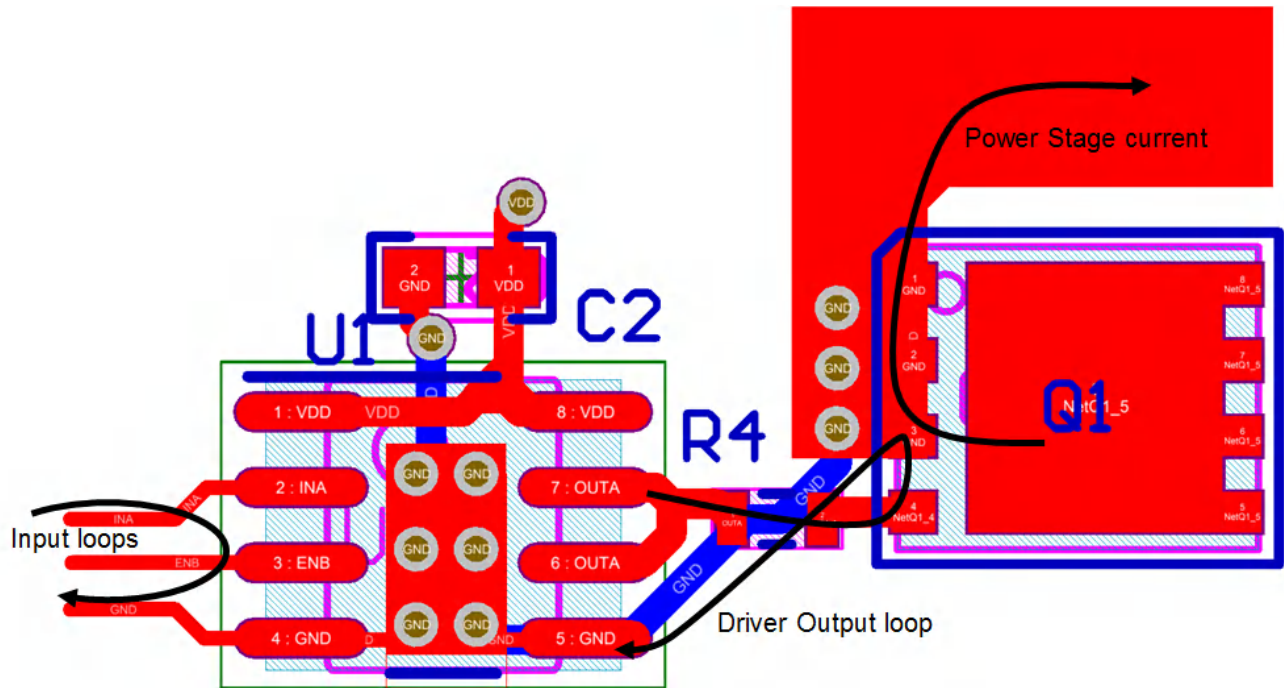
11.1 Layout Guidelines

It can be a significant challenge to avoid the overshoot, undershoot, and ringing issues that can arise from circuit layout. The low impedance of these drivers and their high di/dt can induce ringing between parasitic inductances and capacitances in the circuit. Utmost care must be used in the circuit layout.

In general, position the driver physically as close to its load as possible. Place a 1-μF bypass capacitor as close to the output side of the driver as possible, connecting it to pins 1 and 8. Connect a single trace between the two VDD pins (pin 1 and pin 8); connect a single trace between PGND and AGND (pin 5 and pin 4). If a ground plane is used, it may be connected to AGND; do not extend the plane beneath the output side of the package (pins 5 – 8). Connect the load to both OUT pins (pins 7 and 6) with a single trace on the adjacent layer to the component layer; route the return current path for the output on the component side, directly over the output path.

Extreme conditions may require decoupling the input power and ground connections from the output power and ground connections. The UCCx732x has a feature that allows the user to take these extreme measures, if necessary. There is a small amount of internal impedance of about 15 Ω between the AGND and PGND pins; there is also a small amount of impedance (approximately 30 Ω) between the two VDD pins. To take advantage of this feature, connect a 1-μF bypass capacitor between VDD and PGND (pins 5 and 8) and connect a 0.1-μF bypass capacitor between VDD and AGND (pins 1 and 4). Further decoupling can be achieved by connecting between the two VDD pins with a jumper that passes through a 40-MHz ferrite bead and connect bias power only to pin 8. Even more decoupling can be achieved by connecting between AGND and PGND with a pair of anti-parallel diodes (anode connected to cathode and cathode connected to anode).

11.2 Layout Example



11-1. Layout Recommendation

11.3 Thermal Considerations

The useful range of a driver is greatly affected by the drive power requirements of the load and the thermal characteristics of the device package. For a power driver to be useful over a particular temperature range the package must allow for the efficient removal of the heat produced while keeping the junction temperature within rated limits. The UCC3732x family of drivers is available in three different packages to cover a range of application requirements.

As shown in the power dissipation rating table, the 8-pin SOIC (D) and 8-pin PDIP (P) packages each have a power rating of around 0.5 W with $T_A = 70^\circ\text{C}$. This limit is imposed in conjunction with the power derating factor also given in the table. The power dissipation in our earlier example is 0.432 W with a 10-nF load, 12 VDD, switched at 300 kHz. Thus, only one load of this size could be driven using the D or P packages. The difficulties with heat removal limit the drive available in the D or P packages.

The 8-pin MSOP PowerPAD (DGN) package significantly relieves this concern by offering an effective means of removing the heat from the semiconductor junction. As illustrated in Reference 3, the PowerPAD packages offer a leadframe die pad that is exposed at the base of the package. This pad is soldered to the copper on the PC board directly underneath the device package, reducing the θ_{jc} down to 4.7°C/W . Data is presented in Reference 3 to show that the power dissipation can be quadrupled in the PowerPAD configuration when compared to the standard packages. The PC board must be designed with thermal lands and thermal vias to complete the heat removal subsystem, as summarized in Reference 4. This allows a significant improvement in heatsinking over that available in the D or P packages, and is shown to more than double the power capability of the D and P packages.

The PowerPAD is not directly connected to any leads of the package. However, it is electrically and thermally connected to the substrate which is the ground of the device.

12 Device and Documentation Support

12.1 Device Support

12.1.1 サード・パーティ製品に関する免責事項

サード・パーティ製品またはサービスに関するテキサス・インスツルメンツの出版物は、単独またはテキサス・インスツルメンツの製品、サービスと一緒に提供される場合に関係なく、サード・パーティ製品またはサービスの適合性に関する是認、サード・パーティ製品またはサービスの是認の表明を意味するものではありません。

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

1. SEM-1400, Topic 2, *A Design and Application Guide for High Speed Power MOSFET Gate Drive Circuits*
2. U-137, *Practical Considerations in High Performance MOSFET, IGBT and MCT Gate Drive Circuits*, by Bill Andreyckak ([SLUA105](#))
3. Technical Brief, *PowerPad Thermally Enhanced Package* ([SLMA002](#))
4. Application Brief, *PowerPAD Made Easy* ([SLMA004](#))
5. Data Book, *Power Supply Control Products*, ([SLUD003](#))

12.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

12.4 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの[使用条件](#)を参照してください。

12.5 Trademarks

PowerPAD™ is a trademark of Texas Instruments.

テキサス・インスツルメンツ E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

12.6 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。


12.7 用語集

テキサス・インスツルメンツ用語集

この用語集には、用語や略語の一覧および定義が記載されています。

13 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision H (January 2016) to Revision I (November 2023)	Page
• 「製品情報」表から P パッケージを削除.....	1
• 「概要 (続き)」セクションから P パッケージを削除.....	3
• Deleted P package from Pin Configuration and Functions section.....	5
• Changed ESD Ratings from ± 2500 V and ± 1500 V to ± 2000 V and ± 1000 V.....	6
• Changed input threshold voltage values, deleted V_{OH} output high level and V_{OL} output low level, changed output resistance high and output resistance low values and deleted Latch-up protection from Electrical Characteristics.....	7
• Deleted P package data from Power Dissipations Ratings section.....	8
• Changed  7-16	10

Changes from Revision G (May 2013) to Revision H (January 2016)	Page
• 「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加。	1

Changes from Revision F (March 2012) to Revision G (May 2013)	Page
• Updated AGND pin description.	5
• Changed minimum value for input voltage from -5 to -0.3 V in the <i>Absolute Maximum Ratings</i> table.....	6
• Added $C_{LOAD} = 10$ nF to Fall Time vs Supply Voltage graph.....	10
• Changed Changed x-axis values from 1, 10, 100 to 0.1, 1, 10 in Rise Time vs Load Capacitance graph.....	10
• Changed Changed x-axis values from 1, 10, 100 to 0.1, 1, 10 in Fall Time vs Output Capacitance graph.....	10

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC27321D	LIFEBUY	SOIC	D	8	75	RoHS & Green	Call TI NIPDAU	Level-1-260C-UNLIM	-40 to 105	27321	
UCC27321DGN	LIFEBUY	HVSSOP	DGN	8	80	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 105	27321	
UCC27321DGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 105	27321	Samples
UCC27321DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	Call TI NIPDAU	Level-1-260C-UNLIM	-40 to 105	27321	Samples
UCC27321P	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 105	UCC27321P	Samples
UCC27321PE4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 105	UCC27321P	Samples
UCC27322D	LIFEBUY	SOIC	D	8	75	RoHS & Green	Call TI NIPDAU	Level-1-260C-UNLIM	-40 to 105	27322	
UCC27322DGN	LIFEBUY	HVSSOP	DGN	8	80	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 105	27322	
UCC27322DGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 105	27322	Samples
UCC27322DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	Call TI NIPDAU	Level-1-260C-UNLIM	-40 to 105	27322	Samples
UCC27322DRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 105	27322	Samples
UCC27322P	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 105	UCC27322P	Samples
UCC27322PE4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 105	UCC27322P	Samples
UCC37321D	LIFEBUY	SOIC	D	8	75	RoHS & Green	Call TI NIPDAU	Level-1-260C-UNLIM	0 to 70	37321	
UCC37321DGN	LIFEBUY	HVSSOP	DGN	8	80	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	0 to 70	37321	
UCC37321DGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	0 to 70	37321	Samples
UCC37321DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	Call TI NIPDAU	Level-1-260C-UNLIM	0 to 70	37321	Samples
UCC37321P	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	UCC37321P	Samples
UCC37322D	LIFEBUY	SOIC	D	8	75	RoHS & Green	Call TI NIPDAU	Level-1-260C-UNLIM	0 to 70	37322	
UCC37322DG4	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	37322	
UCC37322DGN	LIFEBUY	HVSSOP	DGN	8	80	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	0 to 70	37322	
UCC37322DGNG4	LIFEBUY	HVSSOP	DGN	8	80	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	0 to 70	37322	
UCC37322DGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	0 to 70	37322	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC37322DGNRG4	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	37322	Samples
UCC37322DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	Call TI NIPDAU	Level-1-260C-UNLIM	0 to 70	37322	Samples
UCC37322P	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	UCC37322P	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF UCC27321, UCC27322 :

- Automotive : [UCC27321-Q1](#), [UCC27322-Q1](#)
- Enhanced Product : [UCC27322-EP](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



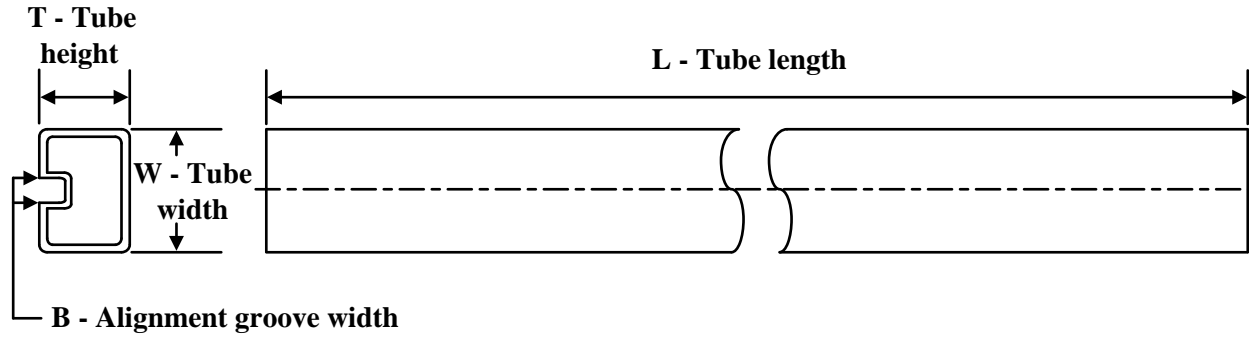
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC27321DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC27321DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC27322DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC27322DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC37321DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC37321DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC37322DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC37322DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC27321DGNR	HVSSOP	DGN	8	2500	364.0	364.0	27.0
UCC27321DR	SOIC	D	8	2500	356.0	356.0	35.0
UCC27322DGNR	HVSSOP	DGN	8	2500	364.0	364.0	27.0
UCC27322DR	SOIC	D	8	2500	356.0	356.0	35.0
UCC37321DGNR	HVSSOP	DGN	8	2500	364.0	364.0	27.0
UCC37321DR	SOIC	D	8	2500	356.0	356.0	35.0
UCC37322DGNR	HVSSOP	DGN	8	2500	364.0	364.0	27.0
UCC37322DR	SOIC	D	8	2500	356.0	356.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
UCC27321D	D	SOIC	8	75	506.6	8	3940	4.32
UCC27321D	D	SOIC	8	75	506.6	8	3940	4.32
UCC27321DGN	DGN	HVSSOP	8	80	330	6.55	500	2.88
UCC27321P	P	PDIP	8	50	506	13.97	11230	4.32
UCC27321PE4	P	PDIP	8	50	506	13.97	11230	4.32
UCC27322D	D	SOIC	8	75	506.6	8	3940	4.32
UCC27322D	D	SOIC	8	75	506.6	8	3940	4.32
UCC27322DGN	DGN	HVSSOP	8	80	330	6.55	500	2.88
UCC27322P	P	PDIP	8	50	506	13.97	11230	4.32
UCC27322PE4	P	PDIP	8	50	506	13.97	11230	4.32
UCC37321D	D	SOIC	8	75	506.6	8	3940	4.32
UCC37321D	D	SOIC	8	75	506.6	8	3940	4.32
UCC37321DGN	DGN	HVSSOP	8	80	330	6.55	500	2.88
UCC37321P	P	PDIP	8	50	506	13.97	11230	4.32
UCC37322D	D	SOIC	8	75	506.6	8	3940	4.32
UCC37322D	D	SOIC	8	75	506.6	8	3940	4.32
UCC37322DG4	D	SOIC	8	75	506.6	8	3940	4.32
UCC37322DG4	D	SOIC	8	75	506.6	8	3940	4.32
UCC37322DGN	DGN	HVSSOP	8	80	330	6.55	500	2.88
UCC37322DGN4	DGN	HVSSOP	8	80	330	6.55	500	2.88
UCC37322P	P	PDIP	8	50	506	13.97	11230	4.32

GENERIC PACKAGE VIEW

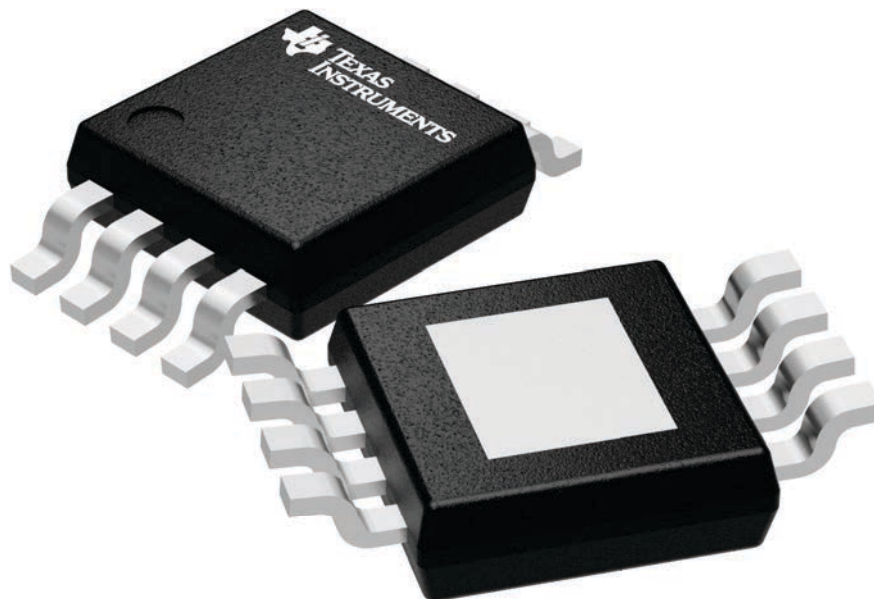
DGN 8

PowerPAD VSSOP - 1.1 mm max height

3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225482/A



D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed $.006$ [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
 EXPOSED METAL SHOWN
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス・デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとし、

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、[TI の販売条件](#)、または [ti.com](#) やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、TI はそれらに異議を唱え、拒否します。

郵送先住所 : Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated