OPA207 低消費電力、高精度、低ノイズ、レール・ツー・レール出力のオペアンプ

1 特長

- 非常に低いオフセット電圧： 150µV (最大値)
- 非常に低いドリフト係数： ±1µV/°C (最大値)
- ゲイン帯域幅： 1MHz (標準値)
- スルー・レート： 3.6V/µs (標準値)
- 高いオープン・ループ・ゲイン： 130dB (最小値)
- 高い同相除去： 115dB (最小値)
- 高い電源除去： 5µV/V (最大値)
- 低いバイアス電流： 2.8nA (最大値)
- 広い電源電圧範囲: ±2.25V～±18V
- 低い静止電流： 375µA (最大値)
- OP-07、OP-77、OP-177の代替

2 アプリケーション

- アナログ入力モジュール
- バッテリ試験装置
- データ・アクイジション (DAQ)
- 圧力トランスミッタ
- 温度トランスミッタ

3 概要

OPA207高精度オペアンプは、業界標準のOP-07、OP-77、OP–177アンプに置き換わる製品です。OPA207は業界標準の同等製品と比較してノイズが低く、出力電圧スイングが広く、2倍の速度で、静止電流は半分です。非常に低い入力オフセット電圧およびドリフト係数、低い入力バイアス電流、高い同相除去比、高い電源除去比といった特長があります。

OPA207オペアンプは±2.25V～±18Vの広い電源電圧範囲で動作し、優れた性能を実現します。アンプが規定された制限までスイングしても、高い性能が維持されます。

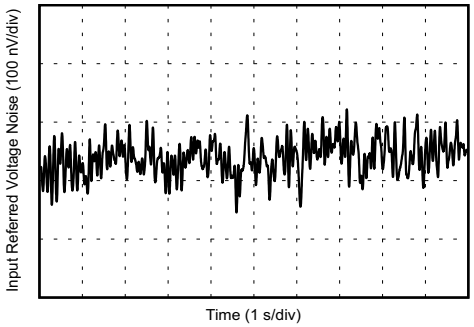
OPA207オペアンプは簡単に使用でき、一部のオペアンプに見られる位相反転や過負荷の問題は発生しません。OPA207はユニティ・ゲイン安定で、広い範囲の負荷状況にわたって優れた動的動作を実現します。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
OPA207	SOIC (8)	4.90mm×3.91mm
	VSSOP (8)	3.00mm×3.00mm
	SOT-23 (5)	2.90mm×1.60mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にあるパッケージ・オプションについての付録を参照してください。

非常に低い0.1Hz～10Hzのノイズ



目次

4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision C (March 2019) から Revision D に変更 **Page**

- SOT-23 (DBV) パッケージをプレビューから量産データ (アクティブ) に 変更 ... 1
- Added specifications for new DBV package ... 4

Revision B (March 2019) から Revision C に変更 **Page**

- Added input offset voltage specification for OPA207DGK ... 5
- Added input offset voltage drift specification for OPA207DGK ... 5

Revision A (December 2018) から Revision B に変更 **Page**

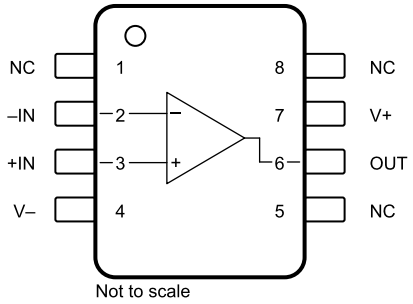
- 量産データ・データシートの初回リリースで VSSOP (DGK) パッケージに関する情報を 追加 ... 1

2017年12月発行のものから更新 **Page**

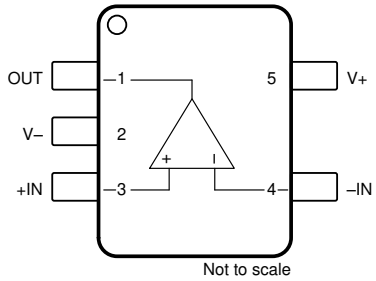
- 事前情報で 5 ピン SOT-23 パッケージに関する情報を 追加 ... 1

5 Pin Configuration and Functions

D and DGK Packages
8-Pin SOIC and 8-Pin VSSOP
Top View



DBV Package
5-Pin SOT-23
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	NO.			
	D (SOIC), DGK(VSSOP)	DBV (SOT-23)		
–IN	2	4	I	Inverting input
+IN	3	3	I	Non-inverting input
NC	1, 5, 8	—	—	No internal connection (can be left floating or connected to ground)
OUT	6	1	O	Output
V–	4	2	—	Negative (lowest) power supply
V+	7	5	—	Positive (highest) power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

	MIN	MAX	UNIT
Supply voltage, Vs = (V+) – (V–)		36	V
Input voltage - Common-mode (2)	(V–) -0.7	(V+) +0.7	V
Input voltage - Differential	–1	1	V
Output short-circuit (3)	Continuous		
Operating temperature	–55	125	°C
Junction temperature		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input current must be limited to 10 mA.
(3) Short circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage, Vs = (V+) – (V–)	Single Supply	4.5	30	36	V
	Dual Supply	±2.25	±15	±18	V
Specified temperature		–40		125	°C

6.4 Thermal Information

THERMAL METRIC (1)		OPA207			UNIT
		DGK (VSSOP)	D (SOIC)	DBV (SOT-23)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	176.7	121.5	166.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	63.9	64.3	116.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	99.4	65.0	63.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.8	18.2	45	°C/W
ψ_{JB}	Junction-to-board characterization parameter	97.6	64.3	62.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package ThermalMetrics* application report.

6.5 Electrical Characteristics

at V_S = ±15 V, T_A = 25°C, R_L = 2 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S/2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage OPA207D				15	±100	µV
		T_A = –40°C to 85°C				±150	
		T_A = –40°C to 125°C				±200	
	Input offset voltage OPA207DGK				15	±125	
		T_A = 0°C to 85°C				±170	
		T_A = –40°C to 125°C				±225	
	Input offset voltage OPA207DBV				15	±130	
		T_A = 0°C to 85°C				±170	
		T_A = –40°C to 125°C				±225	
dV_{OS}/dT	Input offset voltage drift OPA207D	T_A = –40°C to 85°C			±0.2	±.8	µV/°C
		T_A = –40°C to 125°C			±0.2	±.8	
	Input offset voltage drift OPA207DGK and OPA207DBV	T_A = 0°C to 85°C			±0.2	±1.1	
		T_A = –40°C to 125°C			±0.2	±1.1	
PSRR	Input offset voltage versus power supply	V_S = ±2.25 V to ±18 V			±0.5	±3	µV/V
		V_S = ±2.25 V to ±18 V, T_A = –40°C to 85°C				±4.2	
		V_S = ±2.25 V to ±18 V, T_A = –40°C to 125°C				±5	
INPUT BIAS CURRENT							
I_B	Input bias current				±0.2	±1.5	nA
		T_A = –40°C to 85°C				±2	
		T_A = –40°C to 125°C				±7	
I_{OS}	Input offset current				±0.13	±1.5	nA
		T_A = –40°C to 85°C				±2	
		T_A = –40°C to 125°C				±7	
NOISE							
	Input voltage noise	f = 0.1 Hz to 10 Hz			0.16		$µV_{PP}$
					0.024		$µV_{RMS}$
e_N	Input voltage noise density	f = 1 Hz			9.5		$nV/\sqrt{Hz}$
		f = 10 Hz			7.5		
		f = 100 Hz			7.5		
		f = 1 kHz			7.5		
i_N	Input current noise	f = 1 kHz			0.18		$pA/\sqrt{Hz}$
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage range			(V–) + 1.25		(V+) – 1.25	V
CMRR	Common-mode rejection ratio	(V–) + 1.25 V < V_{CM} < (V+) – 1.25 V		120	140		dB
		(V–) + 1.25 V < V_{CM} < (V+) – 1.25 V, T_A = –40°C to 125°C		115	140		
INPUT CAPACITANCE							
Z_{ID}	Differential				3 || 14		MΩ || pF
Z_{ICM}	Common-mode				1 || 1		GΩ || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	(V–) + 200 mV < V_O < (V+) – 200 mV, R_L = 10 kΩ		130	140		dB
			T_A = –40°C to 125°C	126			
		(V–) + 200 mV < V_O < (V+) – 200 mV, R_L = 2 kΩ	OPA207D, OPA207DGK	120	140		
		(V–) + 300 mV < V_O < (V+) – 300 mV, R_L = 2 kΩ	OPA207DBV	130	140		
		(V–) + 200 mV < V_O < (V+) – 200 mV, R_L = 2 kΩ	T_A = –40°C to 125°C, OPA207D, OPA207DGK	114			
		(V–) + 300 mV < V_O < (V+) – 300 mV, R_L = 2 kΩ	T_A = –40°C to 125°C, OPA207DBV	120			

Electrical Characteristics (continued)

at V_S = ±15 V, T_A = 25°C, R_L = 2 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S/2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FREQUENCY RESPONSE						
GBW	Gain-bandwidth product			1.3		MHz
SR	Slew rate	10-V step, G = 1		2.7		V/µs
t_S	Settling time	To 0.1%, 10-V step , G = 1		4.8		µs
		To 0.01%, 10-V step , G = 1		5.4		
		To 0.001%, 10-V step , G = 1		8.1		
	Overload recovery time	V_{IN} × gain > V_S		1.1		µs
	Total harmonic distortion + noise (THD+N)	V_O = 3 V_{RMS}, G = 1, f = 1 kHz, R_L = 10 kΩ		–114		dB
OUTPUT						
	Voltage output swing from rail	T_A = 25°C, no load, OPA207DBV		15	40	mV
		T_A = 25°C, R_L = 10 kΩ, OPA207DBV		40	60	
		T_A = 25°C, R_L = 2 kΩ, OPA207DBV		80	140	
		T_A = 25°C, no load, OPA207D, OPA207DGK		15	30	
		T_A = 25°C, R_L = 10 kΩ, OPA207D, OPA207DGK		40	50	
		T_A = 25°C, R_L = 2 kΩ, OPA207D, OPA207DGK		80	125	
		T_A = –40°C to 125°C, R_L = 10 kΩ		75	200	
I_{SC}	Short-circuit current	Sinking		–40		mA
		Sourcing		40		
C_{LOAD}	Capacitive load drive			200		pf
R_O	Open-loop output impedance	f = 1 MHz		45		Ω
POWER SUPPLY						
I_Q	Quiescent current per amplifier	I_O = 0 A		350	375	µA
		I_O = 0 A, T_A = –40°C to 125°C			450	
	Turnon time	At T_A = 25°C, V_S = 36 V, V_S ramp rate > 0.3 V/µs		27		µs

6.6 Typical Characteristics

at T_A = 25°C, V_S = ±15 V, and R_L = 2 kΩ (unless otherwise noted)

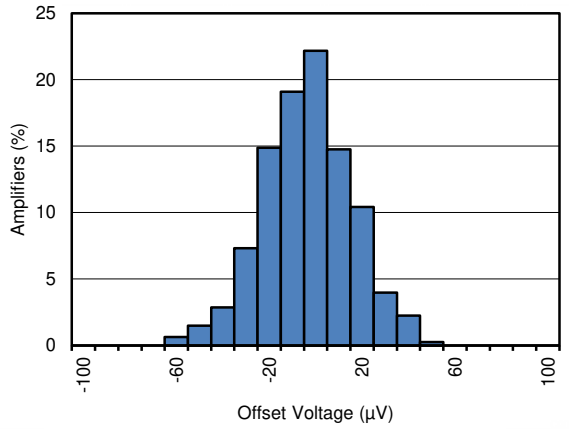


図 1. Input Referred Offset Voltage Distribution

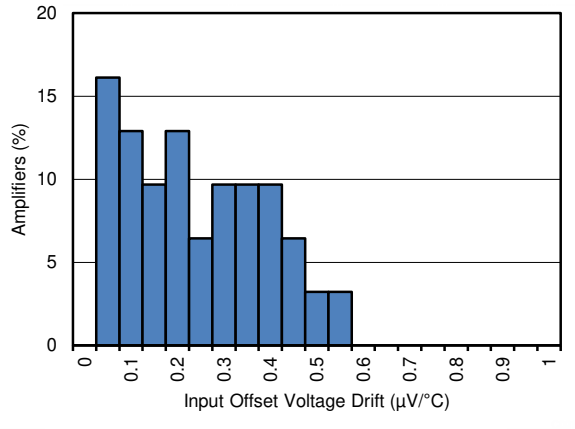


図 2. Input Referred Offset Voltage Drift Distribution

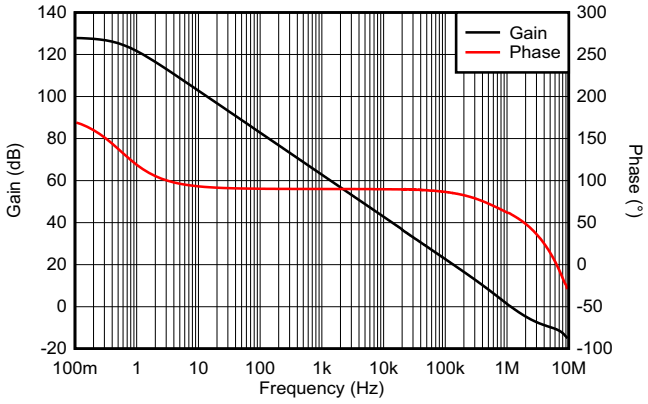


図 3. Open-Loop Gain and Phase vs Frequency

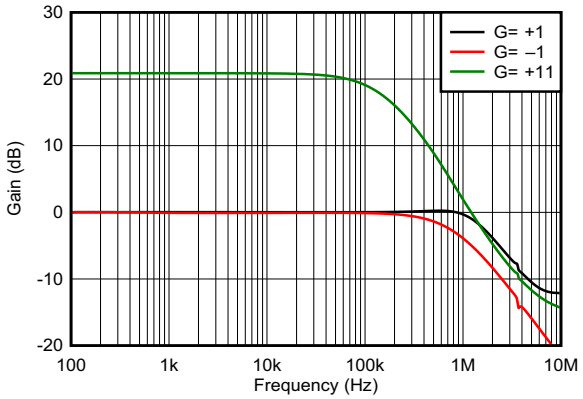


図 4. Closed Loop Gain vs Frequency

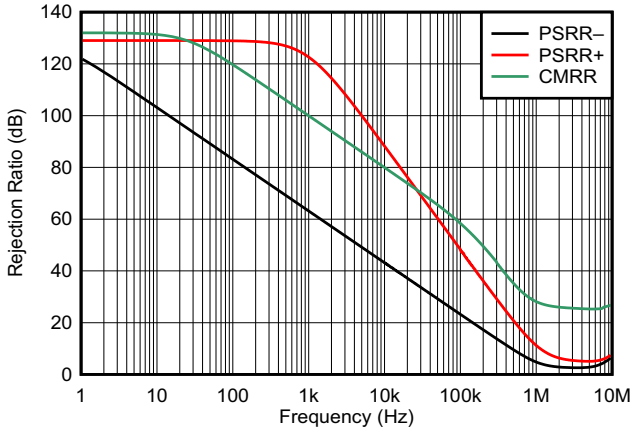


図 5. Power Supply Rejection Ratio and Common-Mode Rejection Ratio vs Frequency

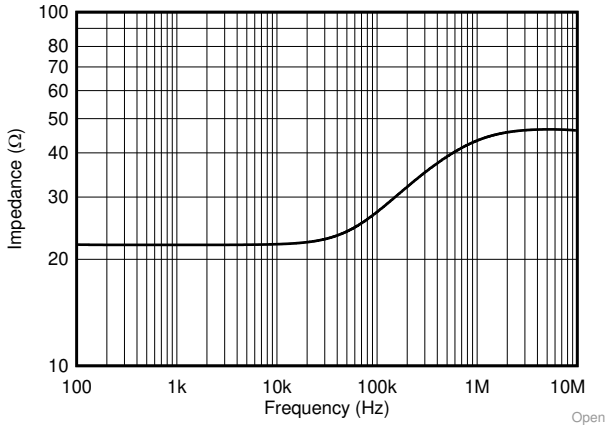


図 6. Open-Loop Output Impedance vs Frequency

Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, and R_L = 2 kΩ (unless otherwise noted)

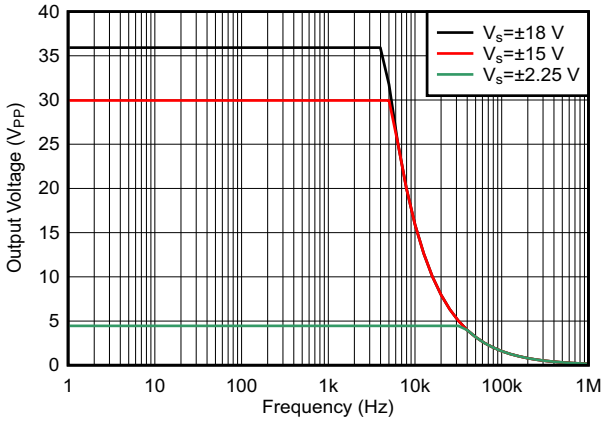


図 7. Full Power Bandwidth

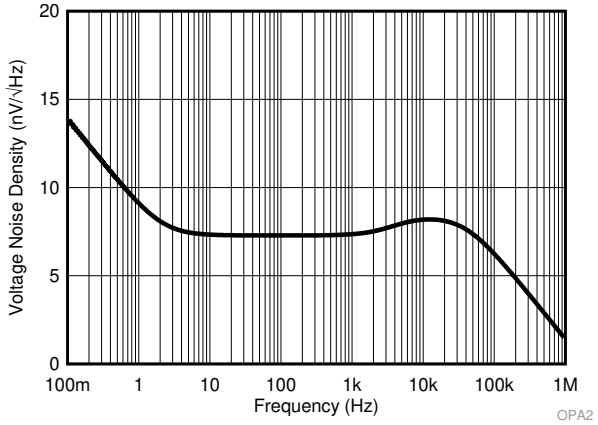


図 8. Input Voltage Noise Spectral Density vs Frequency

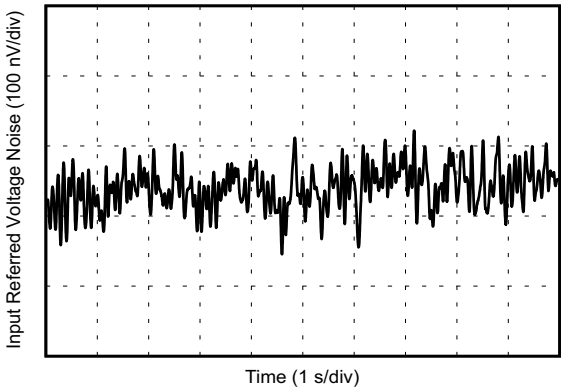


図 9. 0.1-Hz to 10-Hz Noise Voltage

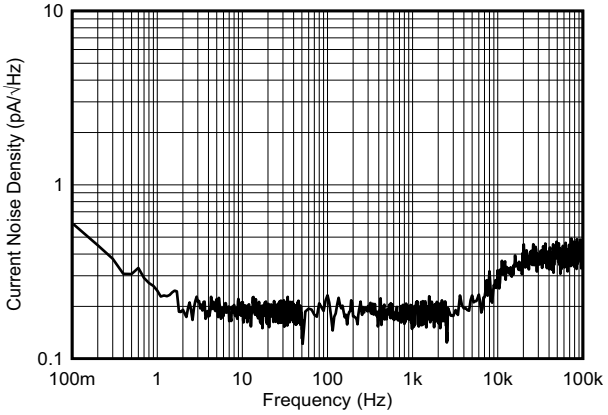


図 10. Input Current Noise vs Frequency

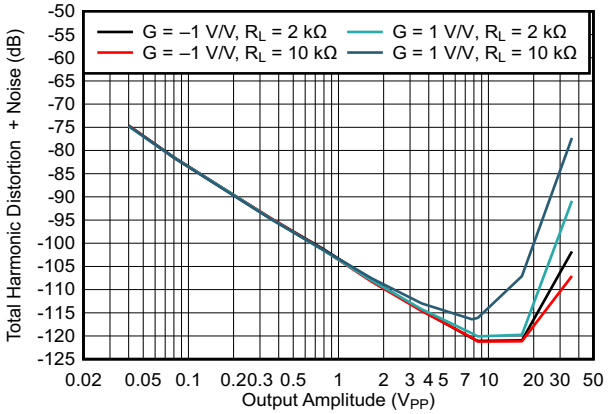


図 11. Total Harmonic Distortion + Noise vs Output Amplitude

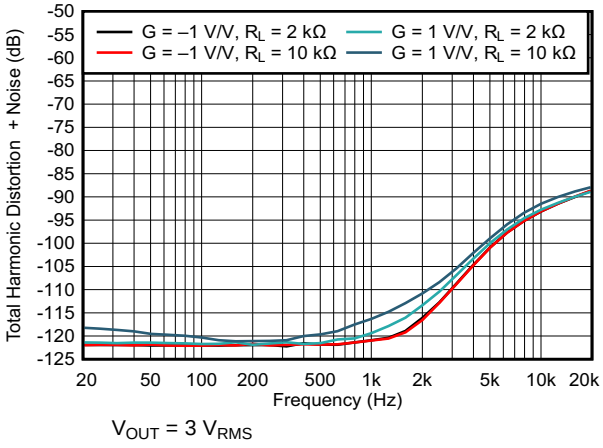


図 12. Total Harmonic Distortion + Noise vs Frequency

Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, and R_L = 2 kΩ (unless otherwise noted)

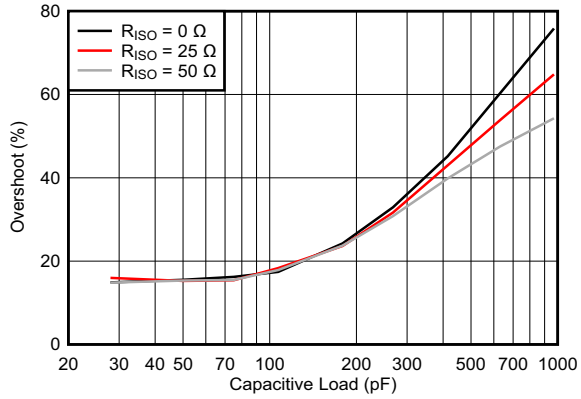


図 13. Overshoot vs Capacitive Load

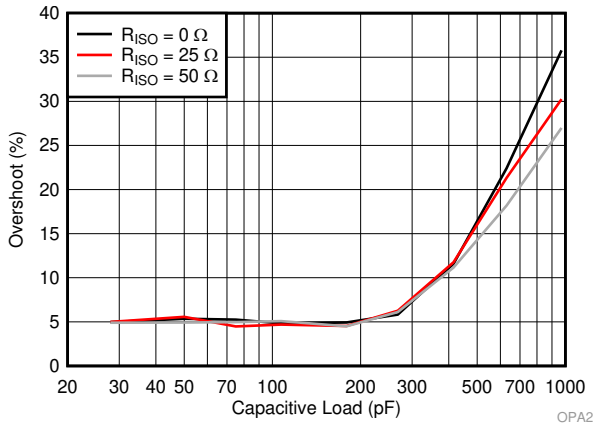


図 14. Overshoot vs Capacitive Load

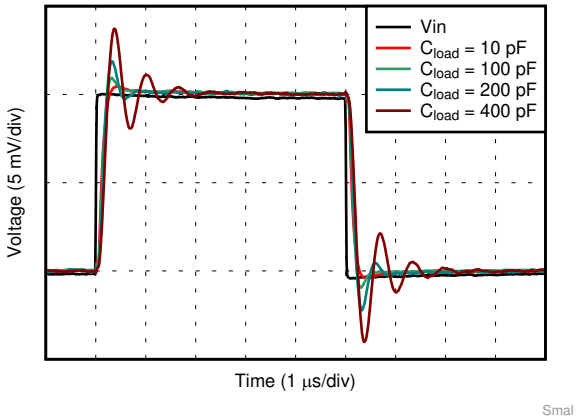


図 15. Small-Signal Step Response

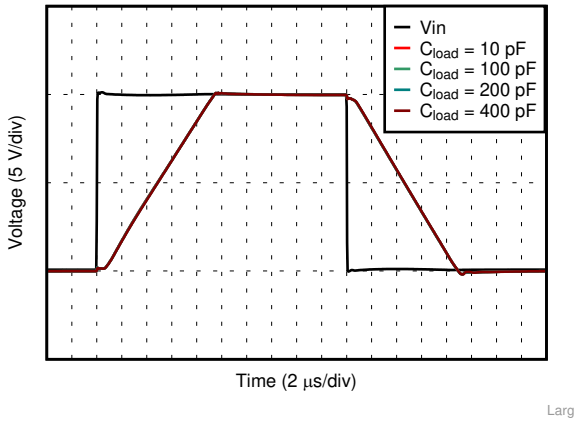


図 16. Large-Signal Step Response

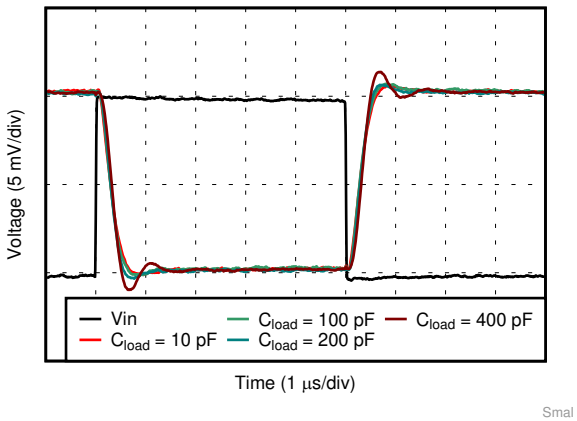


図 17. Small-Signal Step Response

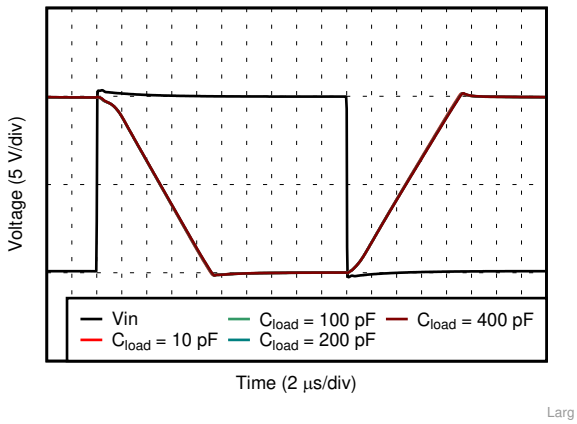


図 18. Large-Signal Step Response

Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, and R_L = 2 kΩ (unless otherwise noted)

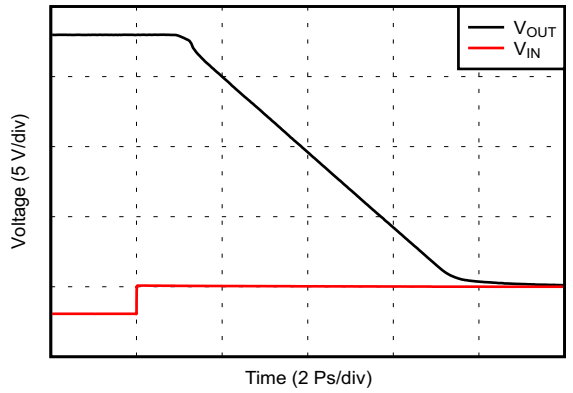


図 19. Overload Recovery From Positive Overload

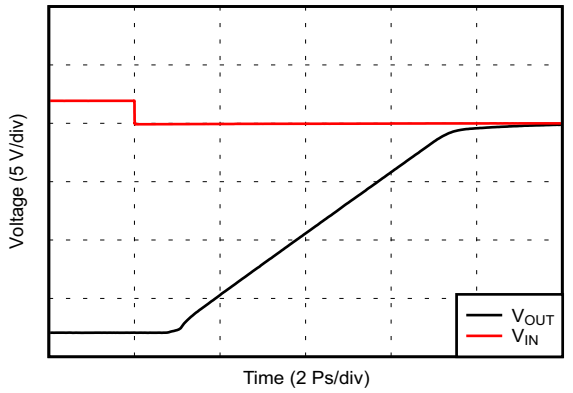
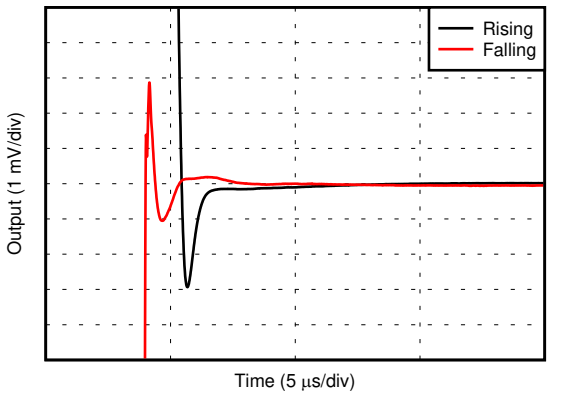
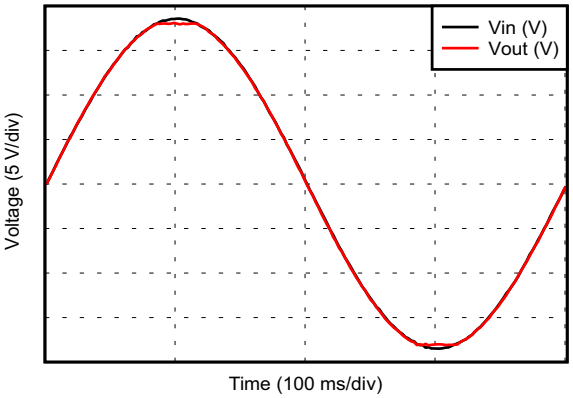


図 20. Overload Recovery from Negative Overload



V_{OUT} = 3 V_{RMS}

図 21. Settling Time



V_{OUT} = 3 V_{RMS}

図 22. No Phase Reversal

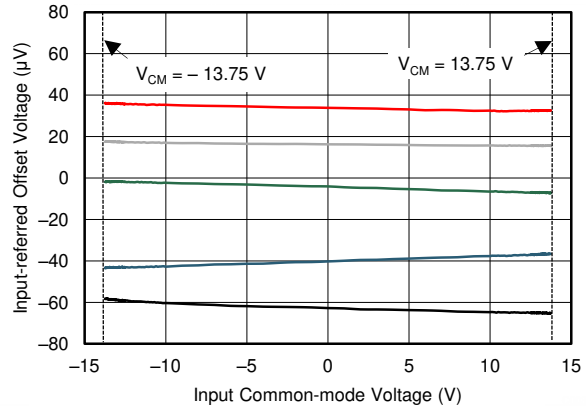


図 23. Input Offset Voltage vs Input Common-mode Voltage

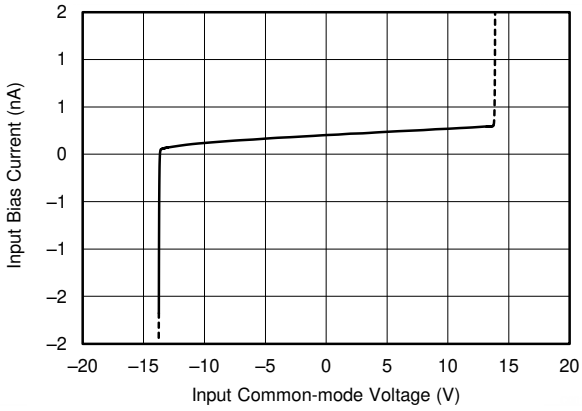


図 24. Input Bias Current vs Input Common-mode Voltage

Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, and R_L = 2 kΩ (unless otherwise noted)

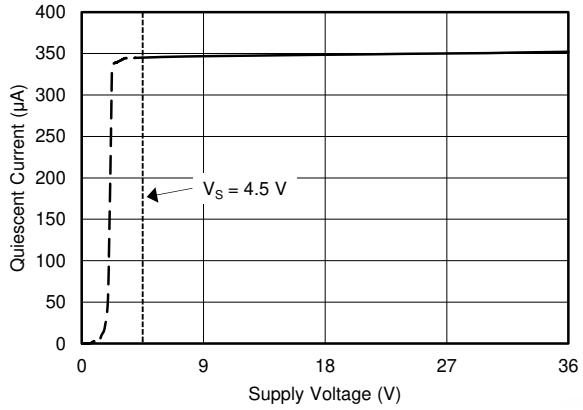


図 25. Quiescent Current vs Power Supply Voltage

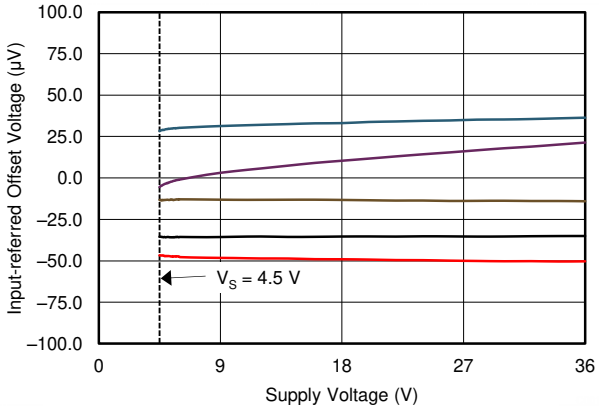


図 26. Input Offset Voltage vs Power Supply Voltage

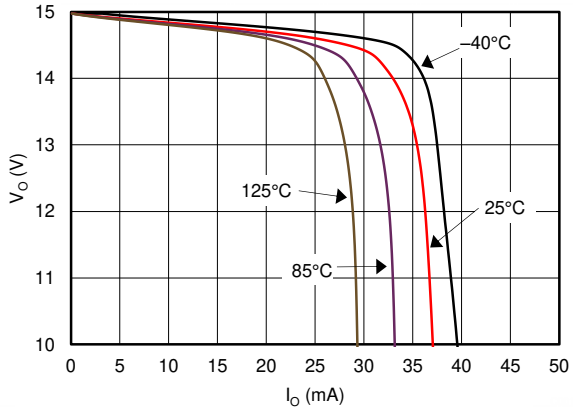


図 27. Output Voltage vs Output Current (Sourcing)

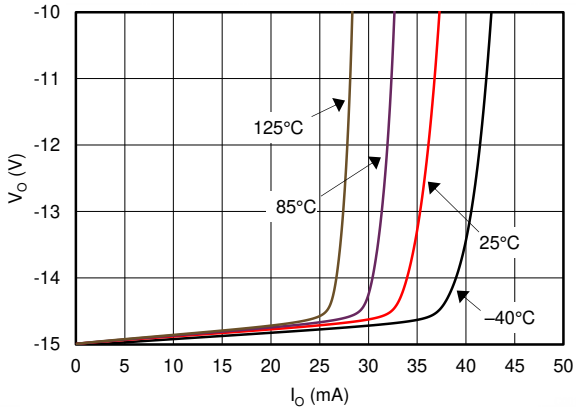


図 28. Output Voltage vs Output Current (Sinking)

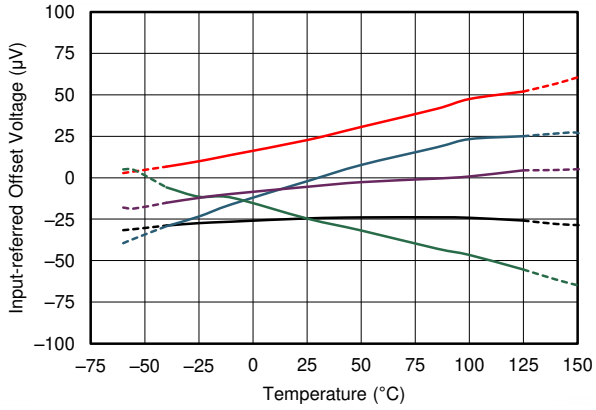


図 29. Input Offset Voltage vs Temperature

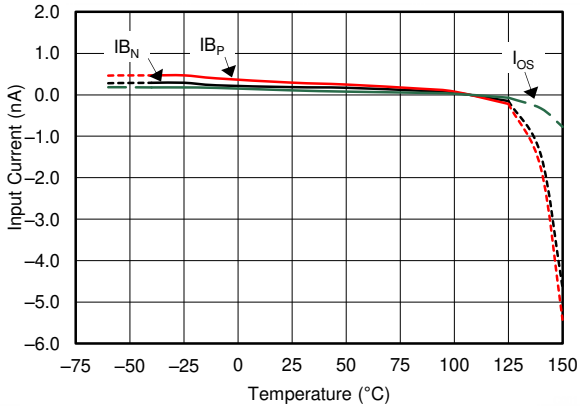


図 30. Input Bias Current vs Temperature

Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, and R_L = 2 kΩ (unless otherwise noted)

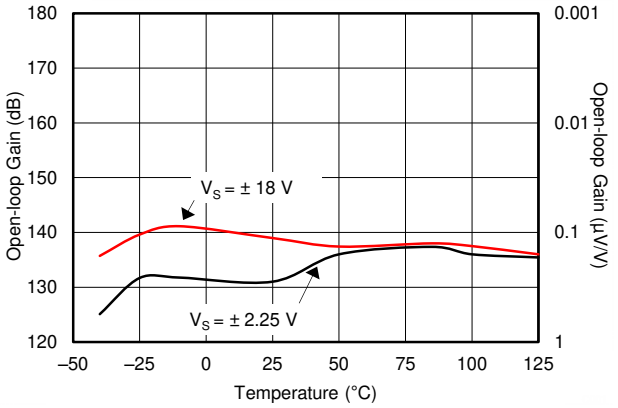


図 31. Open Loop Gain vs Temperature

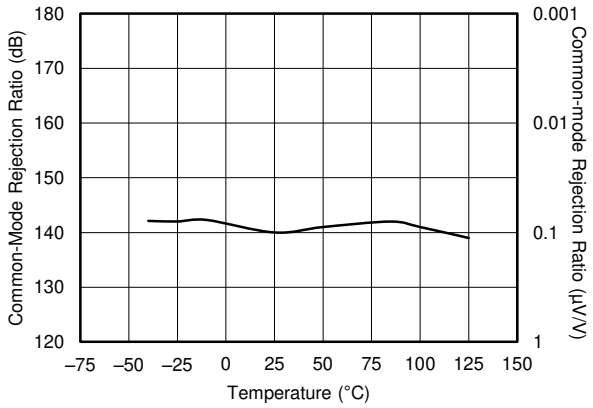


図 32. Common-Mode Rejection Ratio vs Temperature

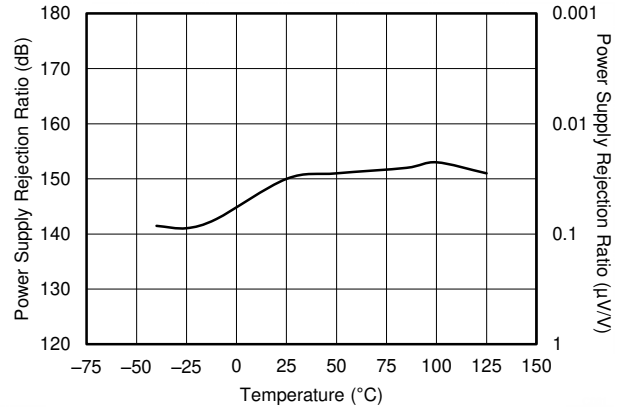


図 33. Power Supply Rejection Ratio vs Temperature

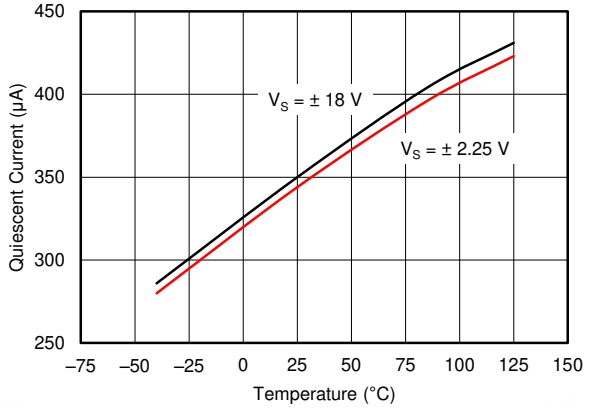


図 34. Quiescent Current vs Temperature

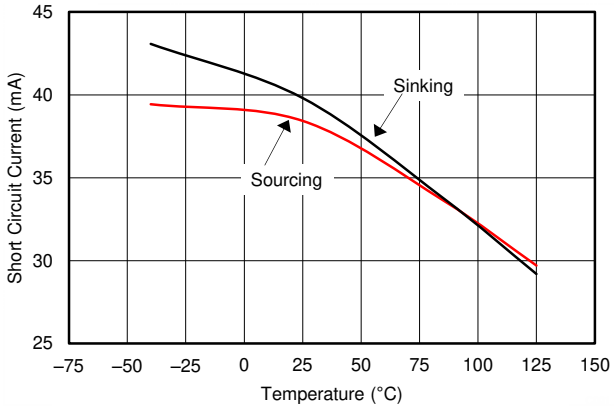


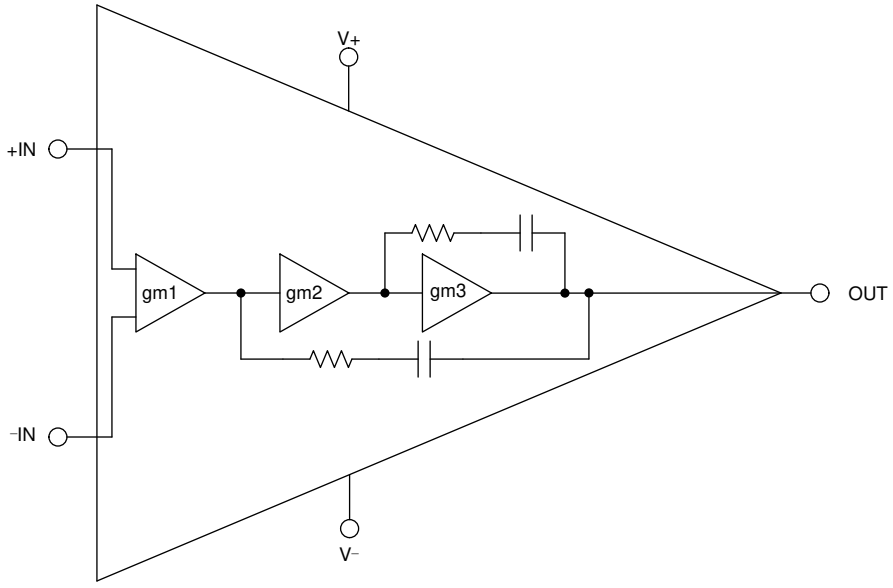
図 35. Output Short Circuit Current vs Temperature

7 Detailed Description

7.1 Overview

The OPA207 precision operational amplifier replaces the industry standard OP-177. The OPA207 offers improved noise, wider output voltage swing, has twice the bandwidth, ten times the slew rate and consumes only half the quiescent current as the OP-177. Additional features include ultralow offset voltage and drift, low bias current, high common-mode rejection, and high power supply rejection.

7.2 Functional Block Diagram



7.3 Feature Description

The OPA207 is unity-gain stable and free from unexpected output phase reversal, making it easy to use in a wide range of applications. Applications with noisy or high-impedance power supplies may require decoupling capacitors close to the device pins. In most cases 0.1-μF capacitors are adequate.

7.3.1 Operating Voltage

The OPA207 operates from ±2.25 V to ±18 V supplies with excellent performance. Key parameters are assured over the specified temperature range, –40°C to 125°C. Most behavior remains unchanged through the full operating voltage range (±2.25 V to ±18 V). Parameters which vary significantly with operating voltage or temperature are shown in *Typical Characteristics*.

Feature Description (continued)

7.3.2 Input Protection

The input stage of the OPA207 is internally protected with resistors in series with diode clamps as shown in 図 36. The inputs can withstand ±10 V differential inputs without damage and the maximum input current should be limited to 10 mA or less.. The protection diodes conduct current when the inputs are over-driven such as when the opamp output is slewing. This may disturb the slewing behavior of unity-gain follower applications, but will not damage the operational amplifier.

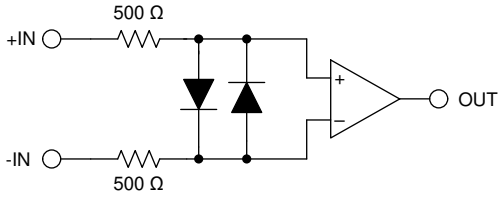


図 36. Simplified OPA207 Input Protection Circuit

7.3.3 ESD Protection

The OPA207 is internally protected against ESD events that can occur during manufacturing, handling, or printed-circuit-board assembly. The internal ESD protection diodes are not intended to protect the OPA207 during normal operation when the device is operating under power. In cases where the inputs or output can be driven above the positive power supply or below the negative power supply care must be taken to limit the current through the internal diodes to 10 mA or less. In harsh electrical environments external protection circuitry may be required and is dependant upon the application requirements and environmental conditions.

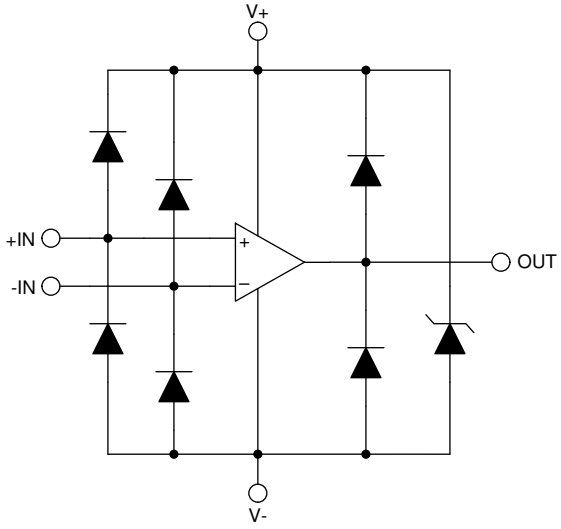


図 37. Simplified OPA207 ESD Protection Circuit

Feature Description (continued)

7.3.4 Input Stage Linearization

The OPA207 uses linearization techniques to reduce the total harmonic distortion. 図 38 illustrates the linearization concept, and 図 38 illustrates the total harmonic distortion performance of the OPA207.

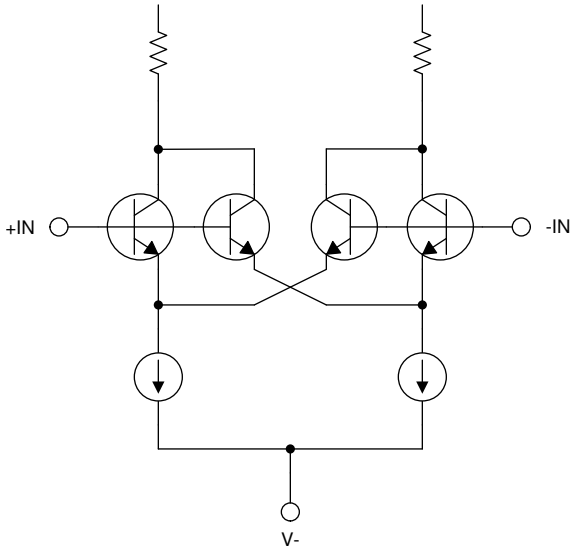


図 38. Simplified Input Stage Linearization Circuit

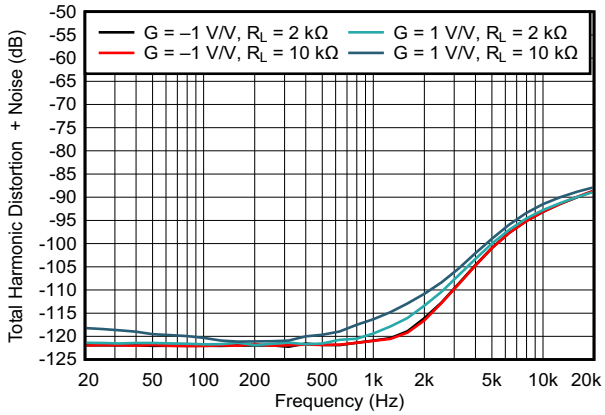


図 39. Total Harmonic Distortion

Feature Description (continued)

7.3.5 Rail-to-Rail Output

The OPA207 uses a rail-to-rail output stage capable of swinging within a few millivolts from either power supply rail while maintaining high open-loop gain. 図 40 shows a simplified drawing of the output stage circuit. Resistors connected in series with each output transistor ensure a consistent output current limit. Limiting the output current in this way ensures reliable operation of the OPA207 under short circuited conditions and protects sensitive loads from being damaged by excessive current. 図 41 and 図 42 illustrate the maximum output current available from the OPA207 at various temperatures.

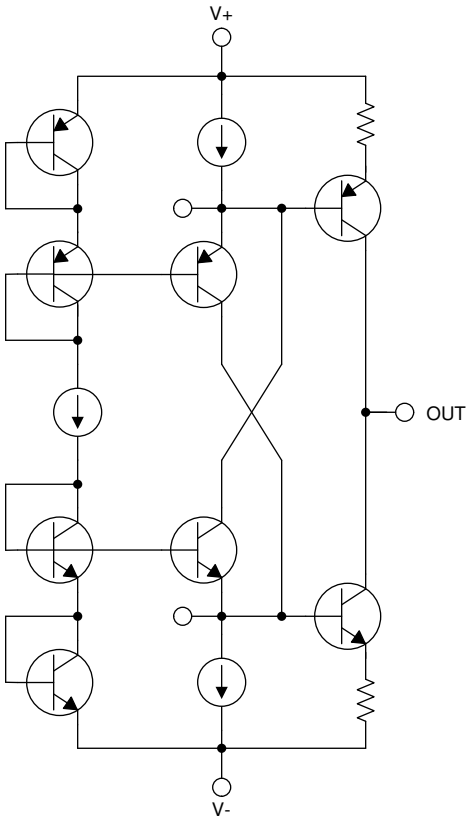


図 40. Simplified Rail-to-Rail Output Stage Circuit

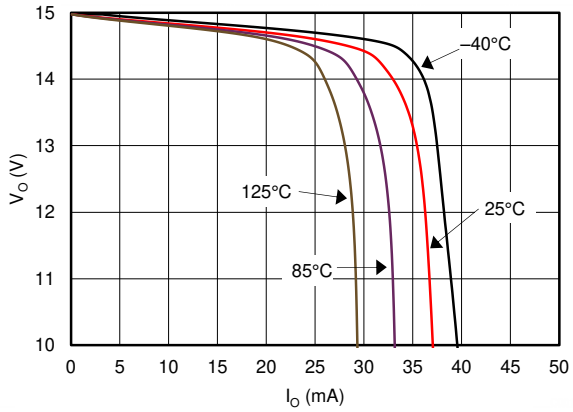


図 41. Output Swing to Rail While Sourcing Current

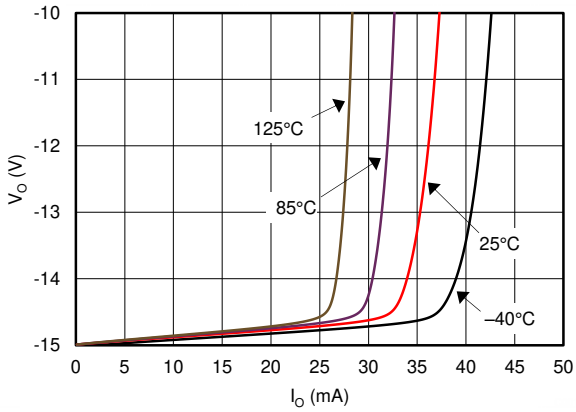


図 42. Output Swing to Rail While Sinking Current

Feature Description (continued)

7.3.6 Low Input Bias Current

The OPA207 uses super-beta bipolar transistors and employs an input bias current cancellation technique. This combination results in very low input bias currents that remain low over the full specified temperature range from –40°C to + 125°C unlike CMOS or JFET amplifiers whose input bias currents typically double every 10°C and can be extremely high at 125°C. 図 43 illustrates the comparison between the OPA207 and typical CMOS or JFET amplifiers.

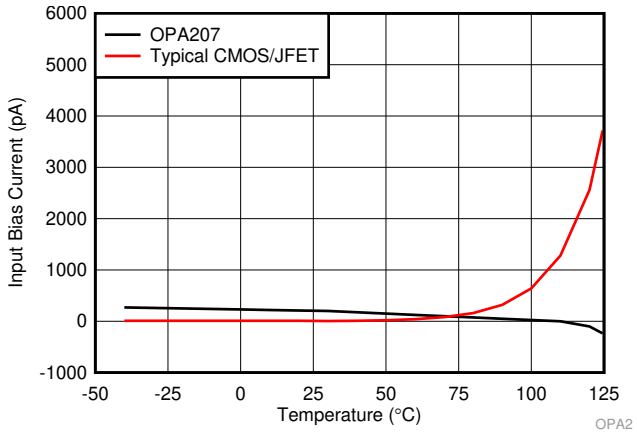


図 43. Input Bias Current vs Temperature

It is common practice to place a bias current cancellation resistor as illustrated in 図 42. This approach works well with amplifiers that do not employ an internal input bias current cancellation technique. Because the OPA207 uses an internal bias current cancellation technique, TI does not recommend the bias cancellation resistor.

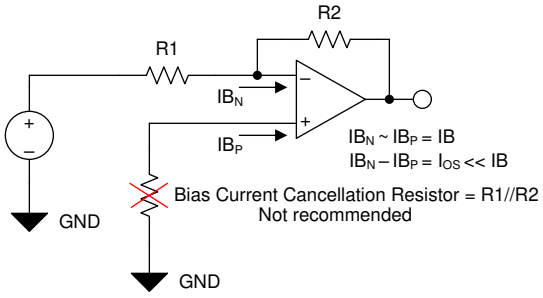


図 44. Bias Current Cancellation Resistor — Not Recommended

Feature Description (continued)

7.3.7 Slew Boost

The OPA207 uses a novel internal slew-boost technique. This method allows the OPA207 to consume very low power yet still achieve a high slew rate of 3.6 V/µs. This makes the OPA207 ideal for applications that require low noise and high out voltage swings where the high slew rate is necessary to achieve fast settling times.

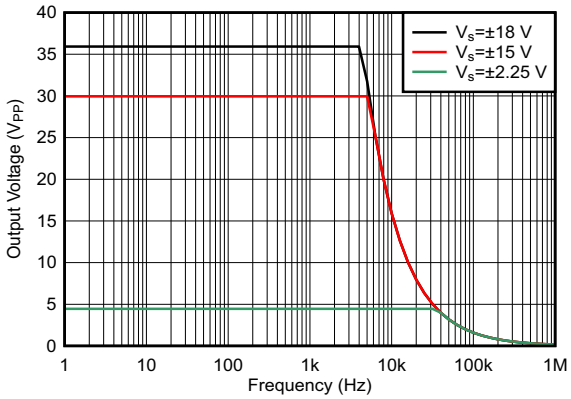


図 45. Full Power Bandwidth

7.3.8 EMI Rejection Ratio (EMIRR)

The electromagnetic interference (EMI) rejection ratio, or EMIRR, describes the EMI immunity of operational amplifiers. An adverse effect that is common to many operational amplifiers is a change in the offset voltage as a result of RF signal rectification. An operational amplifier that is more efficient at rejecting this change in offset as a result of EMI has a higher EMIRR and is quantified by a decibel value. Measuring EMIRR can be performed in many ways, but this report provides the EMIRR IN+, which specifically describes the EMIRR performance when the RF signal is applied to the noninverting input pin of the operational amplifier. In general, only the noninverting input is tested for EMIRR for the following three reasons:

1. Operational amplifier input pins are known to be the most sensitive to EMI, and typically rectify RF signals better than the supply or output pins.
2. The noninverting and inverting operational amplifier inputs have symmetrical physical layouts and exhibit nearly matching EMIRR performance.
3. EMIRR is easier to measure on noninverting pins than on other pins because the noninverting input terminal can be isolated on a printed circuit board (PCB). This isolation allows the RF signal to be applied directly to the noninverting input terminal with no complex interactions from other components or connecting PCB traces.

A more formal discussion of the EMIRR IN+ definition and test method is provided in TI Application Report *EMI Rejection Ratio of Operational Amplifiers*, available for download at www.ti.com. The EMIRR IN+ of the OPA207 is plotted versus frequency as shown in 図 46.

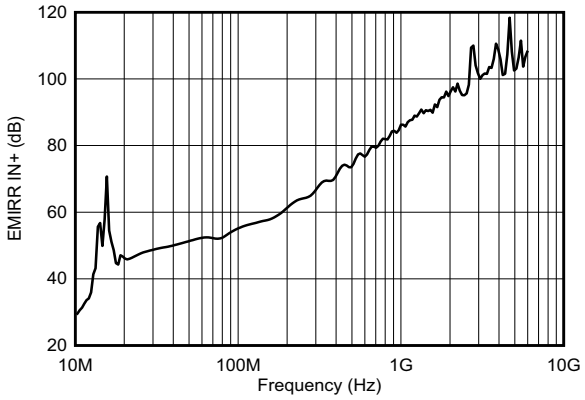


図 46. OPA207 EMIRR IN+ vs Frequency

Feature Description (continued)

If available, any dual and quad operational amplifier device versions have nearly similar EMIRR IN+ performance. The OPA207 unity-gain bandwidth is 1 MHz. EMIRR performance below this frequency denotes interfering signals that fall within the operational amplifier bandwidth.

表 1 shows the EMIRR IN+ values for the OPA207 at particular frequencies commonly encountered in real-world applications. Applications listed in 表 1 may be centered on or operated near the particular frequency shown. This information may be of special interest to designers working with these types of applications, or working in other fields likely to encounter RF interference from broad sources, such as the industrial, scientific, and medical (ISM) radio band.

表 1. OPA207 EMIRR IN+ for Frequencies of Interest

FREQUENCY	APPLICATION/ALLOCATION	EMIRR IN+
400 MHz	Mobile radio, mobile satellite/space operation, weather, radar, UHF	72 dB
900 MHz	GSM, radio com/nav./GPS (to 1.6 GHz), ISM, aeronautical mobile, UHF	83 dB
1.8 GHz	GSM, mobile personal comm. broadband, satellite, L-band	95 dB
2.4 GHz	802.11b/g/n, Bluetooth®, mobile personal comm., ISM, amateur radio/satellite, S-band	94 dB
3.6 GHz	Radiolocation, aero comm./nav., satellite, mobile, S-band	103 dB
5 GHz	802.11a/n, aero comm./nav., mobile comm., space/satellite operation, C-band	102 dB

7.4 Device Functional Modes

The OPA207 has a single functional mode and is operational when the power-supply voltage is greater than 4.5 V (± 2.25 V). The maximum power supply voltage for the OPA207 is 36 V (±18 V).

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

Low-pass filters are commonly employed in signal processing applications to reduce noise and prevent aliasing. The OPA207 is designed to construct high-precision active filters. 図 47 shows a second-order, low-pass filter commonly encountered in signal processing applications.

8.2 Typical Applications

8.2.1 Typical OPA207 Application

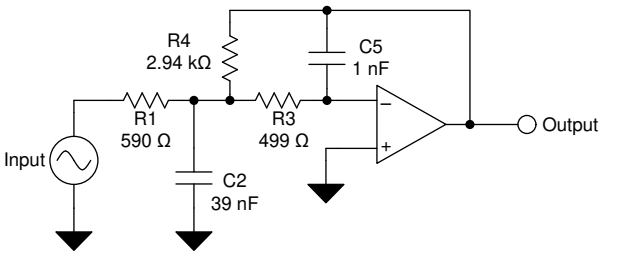


図 47. Typical OPA207 Application Schematic

8.2.1.1 Design Requirements

Use the following parameters for this design example:

- Gain = 5 V/V (inverting gain)
- Low-pass cutoff frequency = 25 kHz
- Second-order Chebyshev filter response with 3-dB gain peaking in the passband

8.2.1.2 Detailed Design Procedure

The infinite-gain multiple-feedback circuit for a low-pass network function is shown in 図 47. Use 式 1 to calculate the voltage transfer function.

$$\frac{\text{Output}}{\text{Input}}(s) = \frac{-1/R_1R_3C_2C_5}{s^2 + (s/C_2)(1/R_1 + 1/R_3 + 1/R_4) + 1/R_3R_4C_2C_5} \quad (1)$$

This circuit produces a signal inversion. For this circuit, the gain at dc and the low-pass cutoff frequency are calculated by 式 2:

$$\text{Gain} = \frac{R_4}{R_1}$$

$$f_c = \frac{1}{2\pi}\sqrt{(1/R_3R_4C_2C_5)} \quad (2)$$

Software tools are readily available to simplify filter design. WEBENCH® Filter Designer is a simple, powerful, and easy-to-use active filter design program. The WEBENCH Filter Designer lets designers create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners.

Available as a web-based tool from the WEBENCH® Design Center, WEBENCH® Filter Designer allows to design, optimize, and simulate complete multi-stage active filter solutions within minutes.

Typical Applications (continued)

8.2.1.3 Application Curve

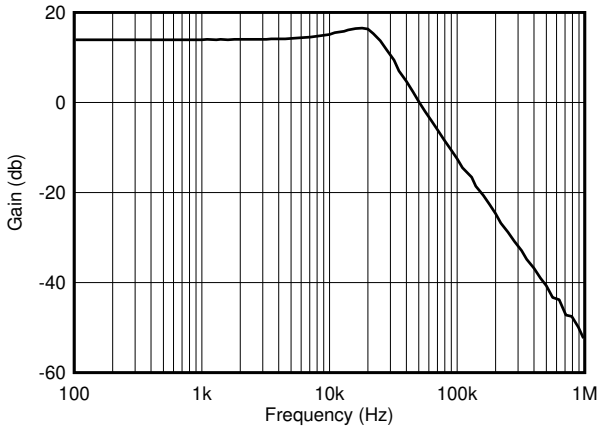


図 48. Low-Pass Filter Transfer Function

8.2.2 Precision Low-Side Current Sensing

With low offset voltage and low offset voltage drift over time and temperature the OPA207 works well for precision low-side current sensing applications as shown in 図 49

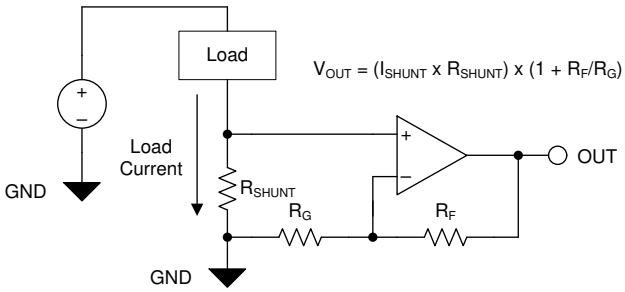


図 49. Precision Low-Side Current Sensing

Typical Applications (continued)

8.2.3 Precision Buffer With Increased Output Current

The OPA207 can be configured as illustrated in 図 50 to drive low impedance loads. In 図 50, the OPA207 is configured in a gain of +10 V/V, and the output current is boosted by the NPN (2N2904) and PNP (2N2906) bipolar transistors. For low output voltages the OPA207 supplies the load current directly through the 100-Ω resistor. The bipolar transistors begin to supply current when the voltage drop across the 100-Ω resistor exceeds approximately 500 mV. 図 50 illustrates the results for a 50-Ω load resistor driven with a 10-V step at the output. This results in a 200-mA current supplied by the circuit.

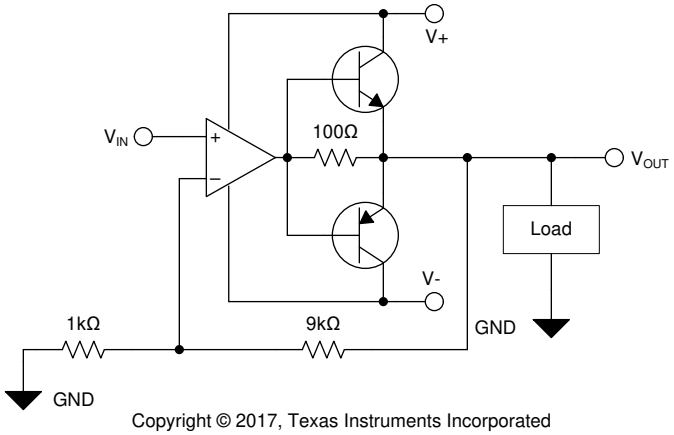


図 50. Precision Buffer (G = 10 V/V) With High Output Drive Capability

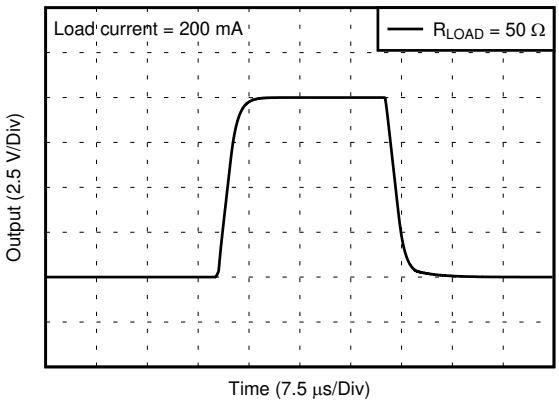


図 51. 50-Ω Load Driven With a 10-V Step

9 Power Supply Recommendations

The OPA207 is specified for operation from 4.5 V to 36 V (±2.25 V to ±18 V); many specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics*.

注意

Supply voltages larger than 36 V can permanently damage the device; see the *Absolute Maximum Ratings*.

Place 0.1-μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, refer to the *Layout Guidelines*.

10 Layout

10.1 Layout Guidelines

The OPA207 series has low offset voltage and drift. To achieve highest performance, optimize the circuit layout and mechanical conditions. Offset voltage and drift can be degraded by small thermoelectric potentials at the op amp inputs. Connections of dissimilar metals generate thermal potential, which can degrade the ultimate performance of the OPA207. These thermal potentials can be made to cancel by assuring that they are equal in both input terminals.

- Keep the thermal mass of the connections to the two input terminals similar.
- Locate heat sources as far as possible from the critical input circuitry.
- Shield operational amplifier and input circuitry from air currents, such as cooling fans.

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1–μF ceramic bypass capacitors between each supply pin and ground, placed as close as possible to the device. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current.
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close as possible to the device. As shown in *Layout Example*, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- For best performance, TI recommends cleaning the PCB following board assembly.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, TI recommends baking the PCB assembly to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

10.2 Layout Example

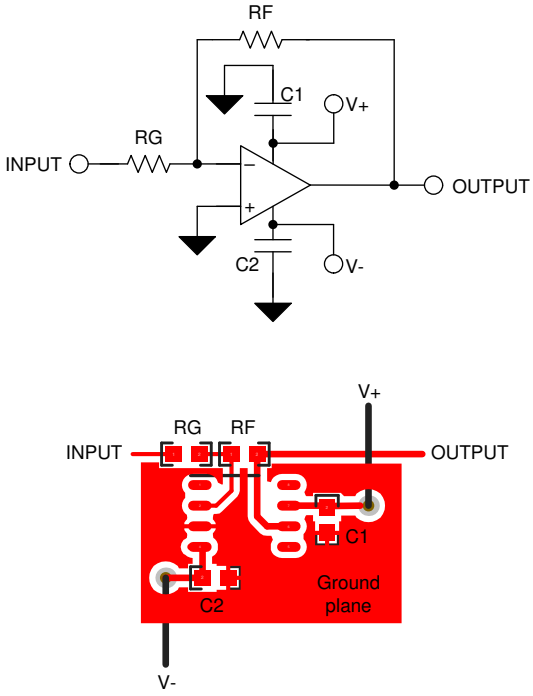


図 52. OPA207 Layout Example for the Inverting Configuration

11 デバイスおよびドキュメントのサポート

11.1 デバイス・サポート

11.1.1 開発サポート

11.1.1.1 WEBENCH Filter Designerツール

WEBENCH® Filter Designerは単純で強力な、使いやすいアクティブ・フィルタ設計プログラムです。WEBENCH Filter Designerを使用すると、TIのベンダ・パートナーからのTI製オペアンプやパッシブ・コンポーネントを使用して、最適なフィルタ設計を作成できます。

11.1.1.2 TINA-TI™(無料のダウンロード・ソフトウェア)

TINA™は、SPICEエンジンをベースにした単純かつ強力な、使いやすい回路シミュレーション・プログラムです。また、TINA-TIは、TINAソフトウェアの完全な機能を持つ無償バージョンで、パッシブ・モデルとアクティブ・モデルに加えて、マクロ・モデルのライブラリがプリロードされています。TINA-TIには、SPICEの標準的なDC解析、過渡解析、周波数ドメイン解析などの全機能に加え、追加の設計機能が搭載されています。

TINA-TIはAnalog eLab Design Centerから無料でダウンロードでき、ユーザーが結果をさまざまな方法でフォーマットできる、広範な後処理機能を備えています。仮想計測器により、入力波形を選択し、回路ノード、電圧、および波形をプローブして、動的なクイック・スタート・ツールを作成できます。

> 注
> これらのファイルを使用するには、TINA ソフトウェア (DesignSoft™製) またはTINA-TIソフトウェアがインストールされている必要があります。TINA-TIフォルダから、無料のTINA-TIソフトウェアをダウンロードしてください。

11.1.1.3 TI Precision Designs

OPA207はいくつかのTI Precision Designsに使用されており、これらは http://www.ti.com/ww/en/analog/precision-designs/からオンラインで入手できます。TI Precision Designsは、TIの高精度アナログ・アプリケーションの専門家により作成されたアナログ・ソリューションで、多くの有用な回路に関して、動作理論、コンポーネント選択、シミュレーション、完全なPCB回路図とレイアウト、部品表、性能測定結果を提供します。

11.2 ドキュメントのサポート

11.2.1 関連資料

関連資料については、以下を参照してください。

- テキサス・インスツルメンツ、*『オペアンプのEMI除去率』*
- テキサス・インスツルメンツ、*『回路基板のレイアウト技法』*

11.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の「アラートを受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.4 サポート・リソース

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.5 商標

TINA-TI, E2E are trademarks of Texas Instruments.
Bluetooth is a registered trademark of Bluetooth SIG, Inc..
TINA, DesignSoft are trademarks of DesignSoft, Inc.
All other trademarks are the property of their respective owners.

11.6 静電気放電に関する注意事項

これらのデバイスは、限定的なESD（静電破壊）保護機能を内 蔵しています。保存時または取り扱い時は、MOSゲートに対す る静電破壊を防止するために、リード線同士をショートさせて おくか、デバイスを導電フォームに入れる必要があります。

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA207ID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA207	Samples
OPA207IDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1NBW	Samples
OPA207IDBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1NBW	Samples
OPA207IDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG | SN	Level-2-260C-1 YEAR	-40 to 125	1I7Q	Samples
OPA207IDGKT	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	NIPDAUAG | SN	Level-2-260C-1 YEAR	-40 to 125	1I7Q	Samples
OPA207IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA207	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

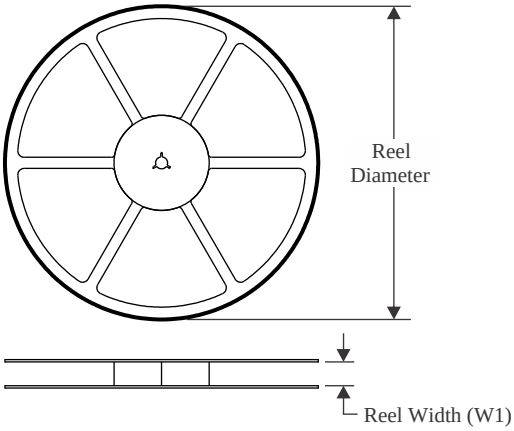
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

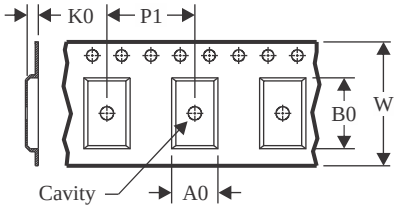
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

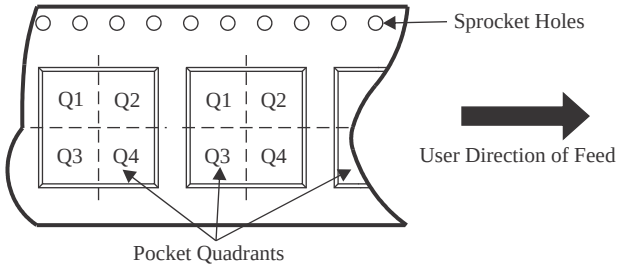


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

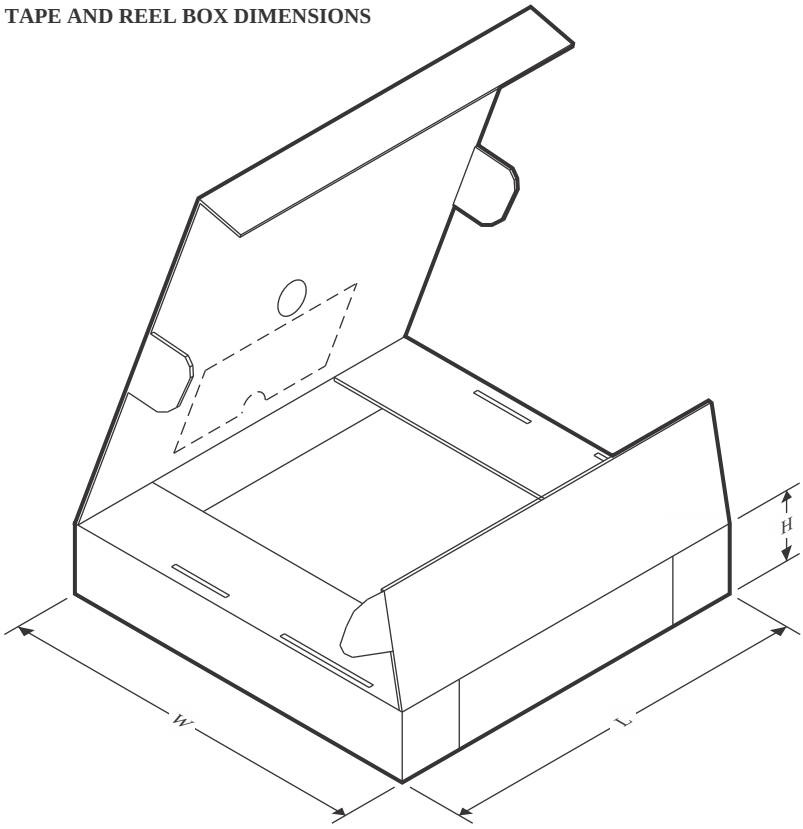
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA207IDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA207IDBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA207IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA207IDGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA207IDR	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1

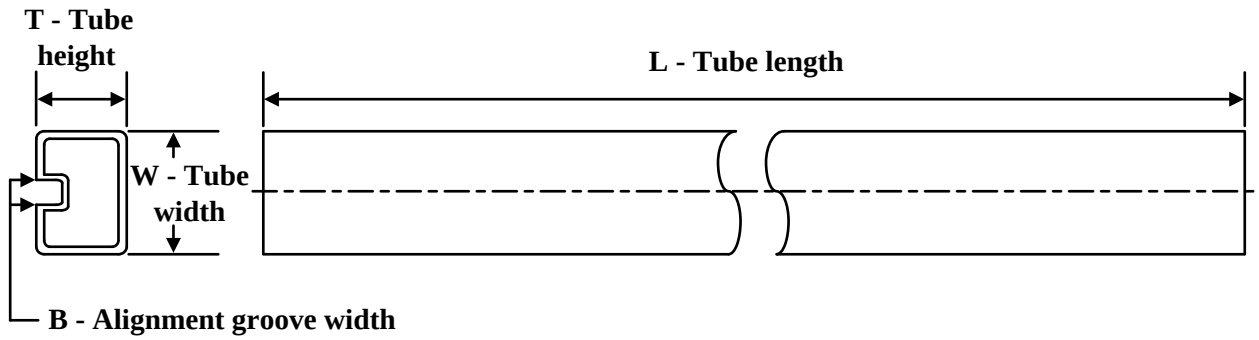
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

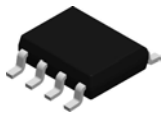
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA207IDBVR	SOT-23	DBV	5	3000	213.0	191.0	35.0
OPA207IDBVT	SOT-23	DBV	5	250	213.0	191.0	35.0
OPA207IDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA207IDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
OPA207IDR	SOIC	D	8	2500	340.5	336.1	25.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA207ID	D	SOIC	8	75	507	8	3940	4.32

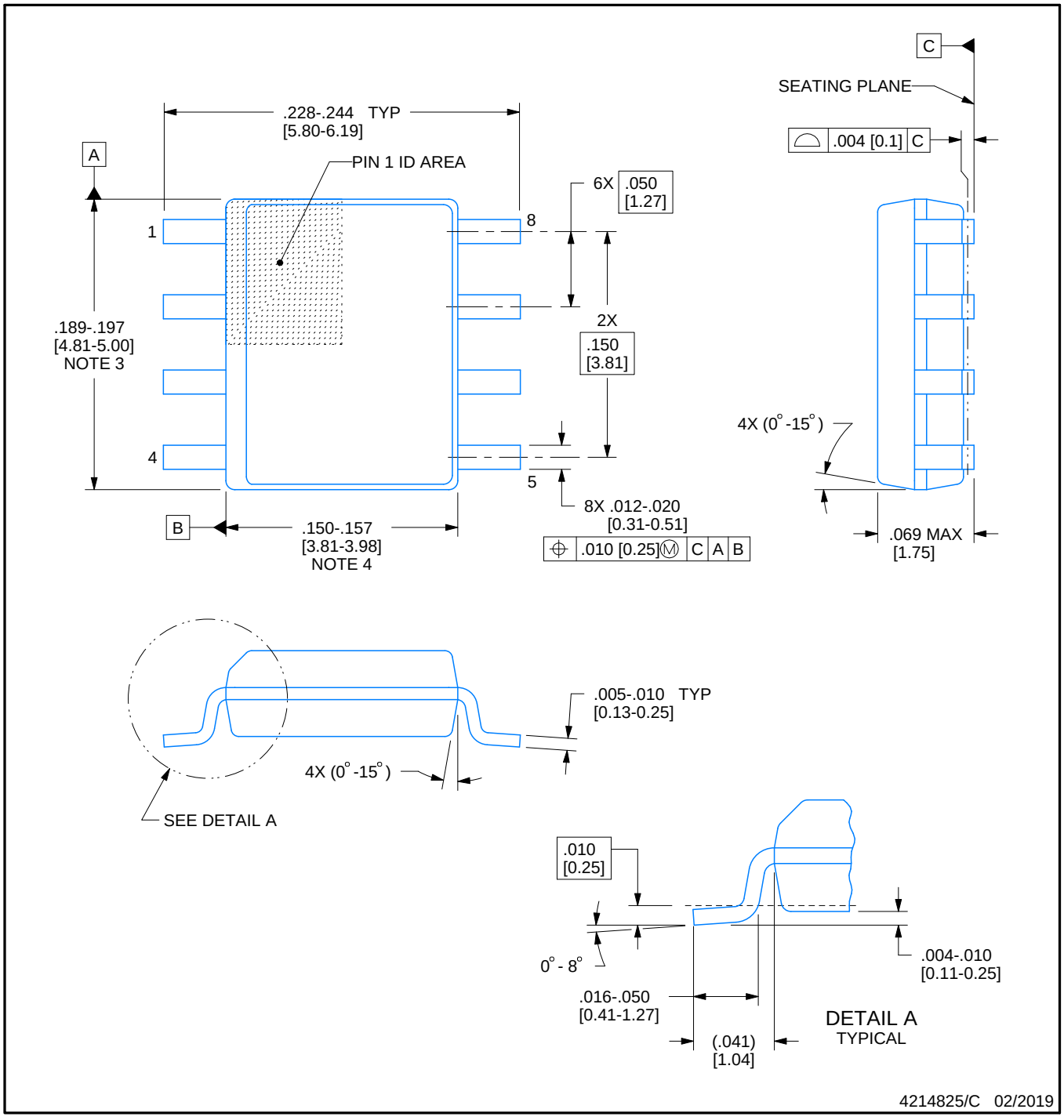


PACKAGE OUTLINE

D0008A

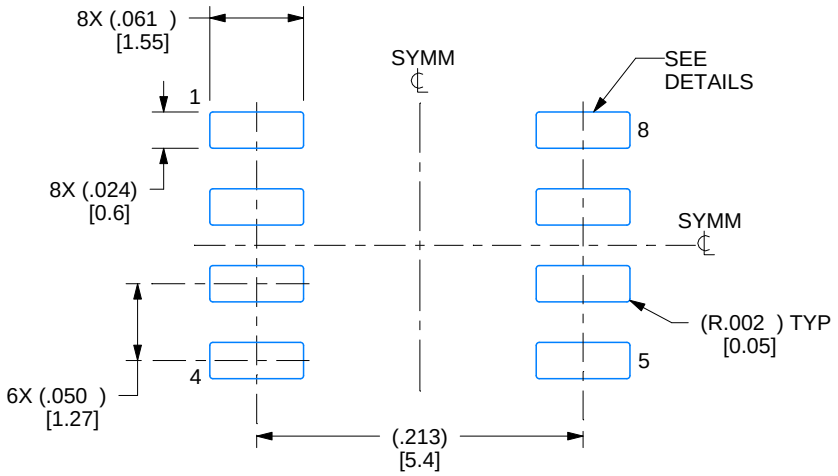
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

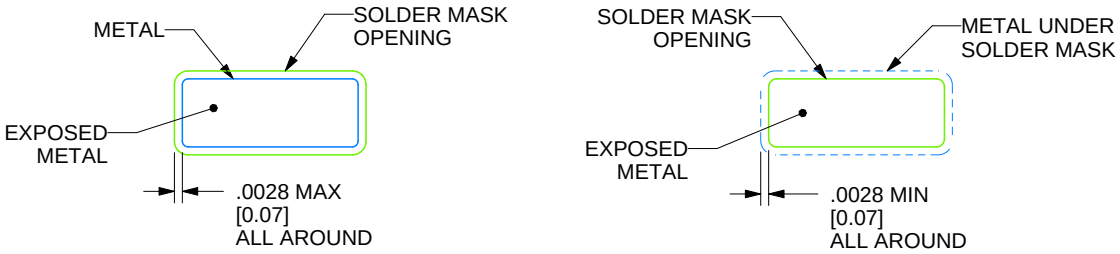


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

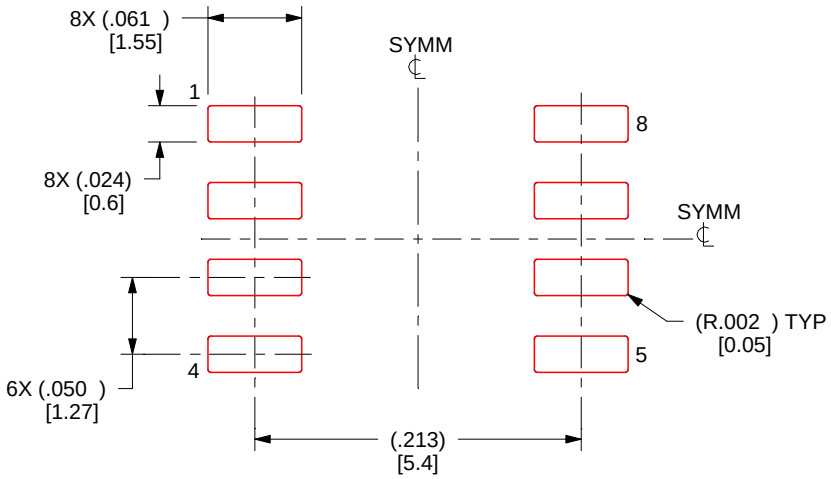
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

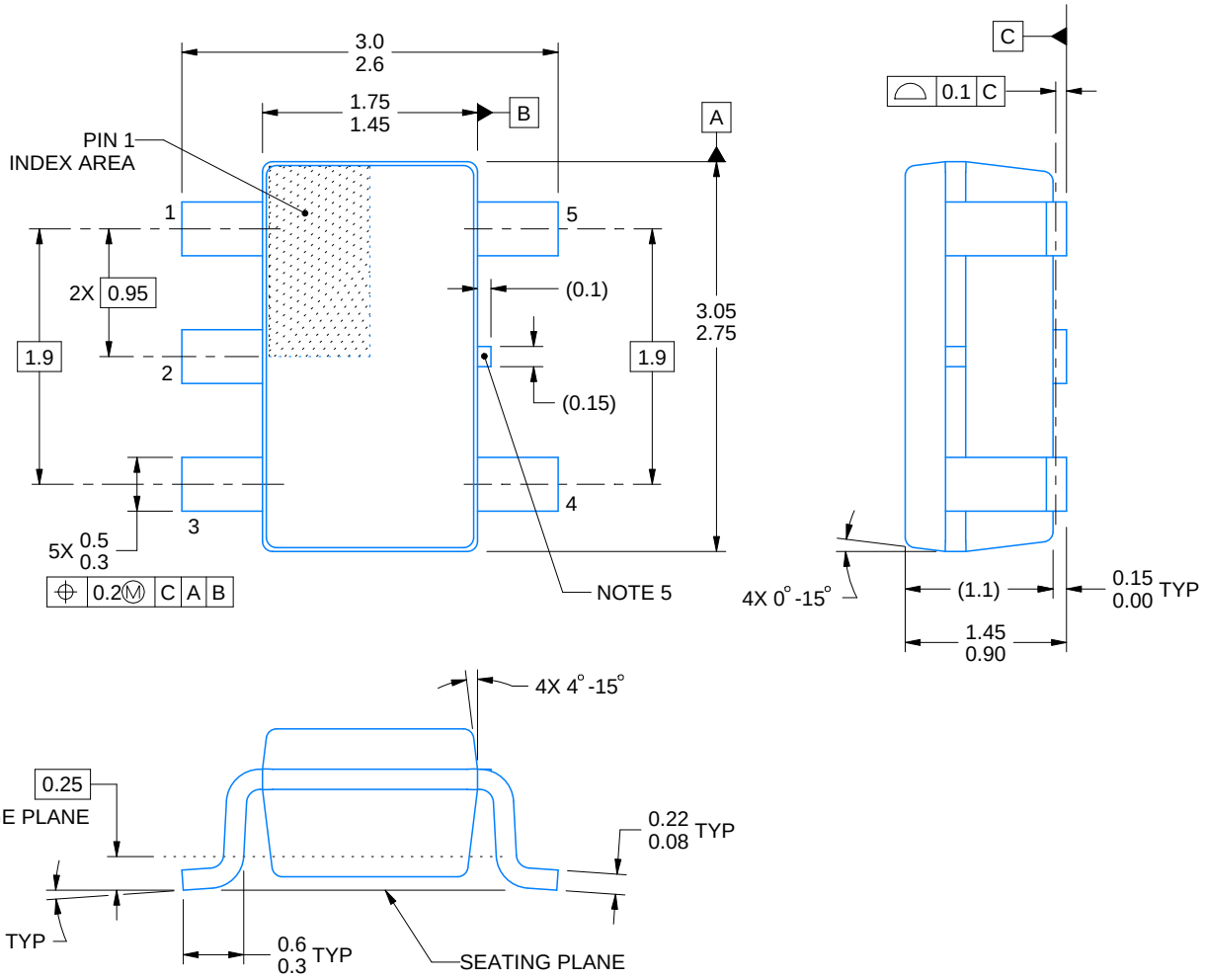
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

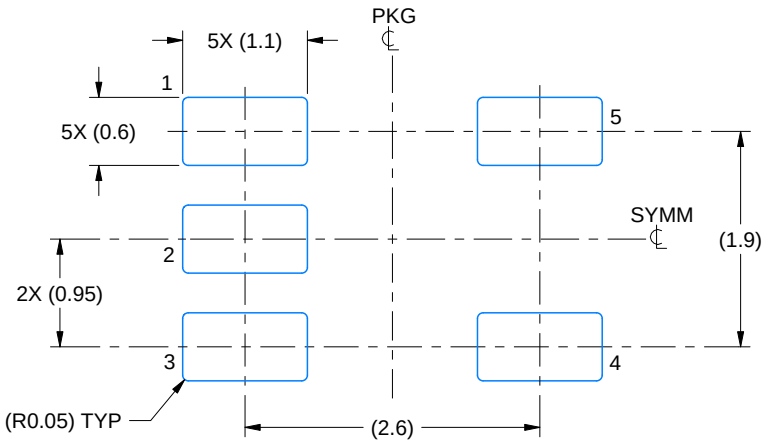
SMALL OUTLINE TRANSISTOR



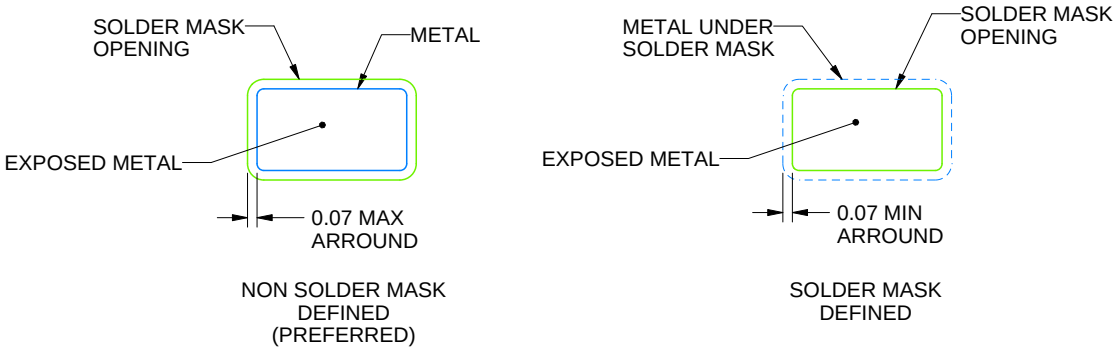
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

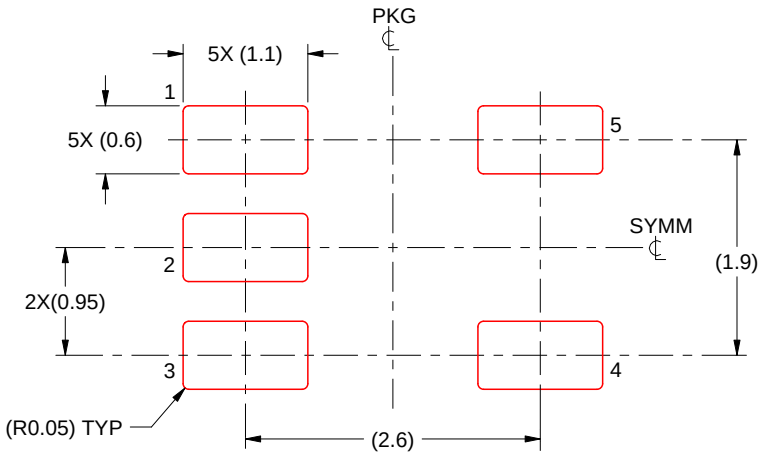


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

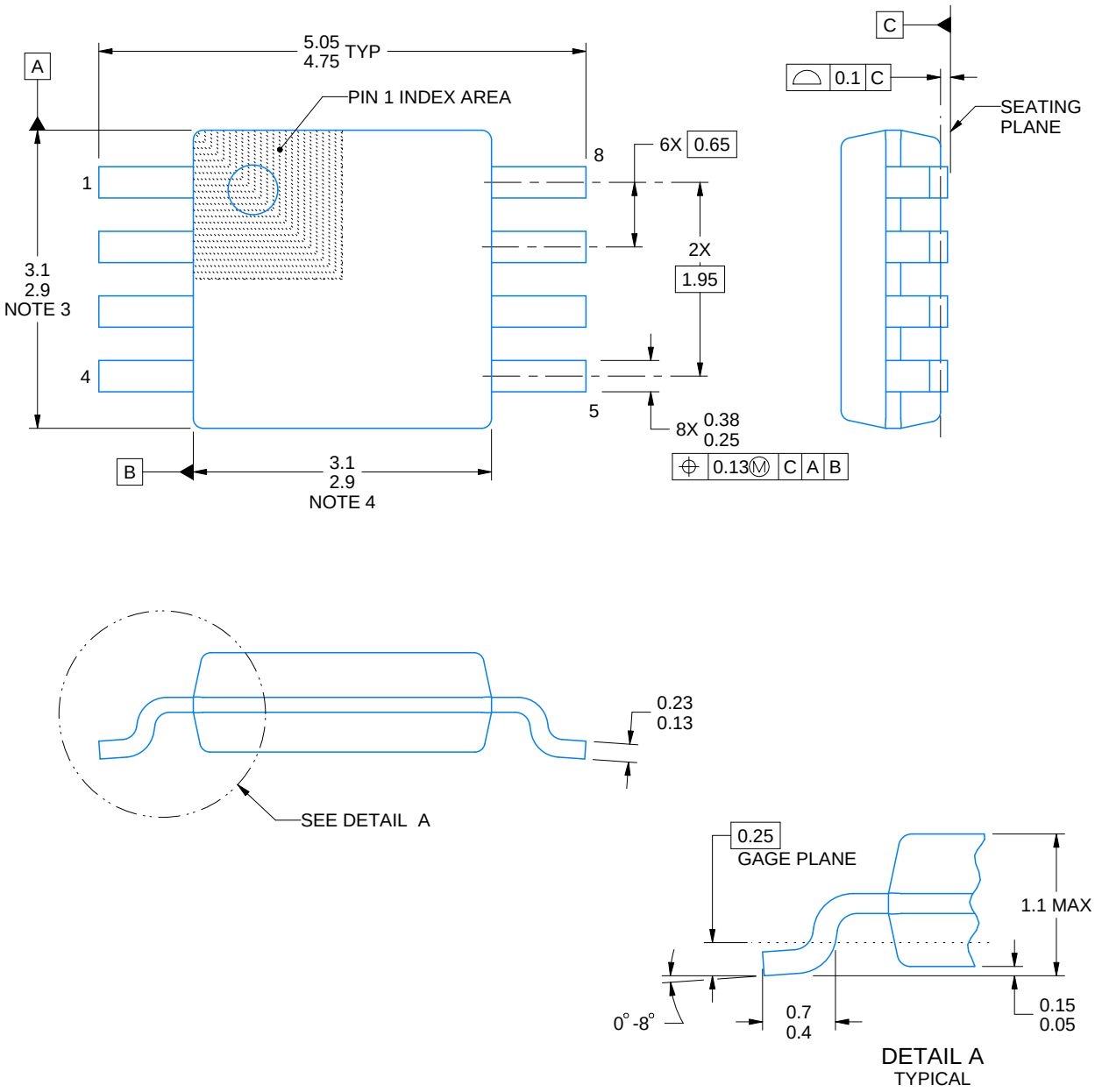
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

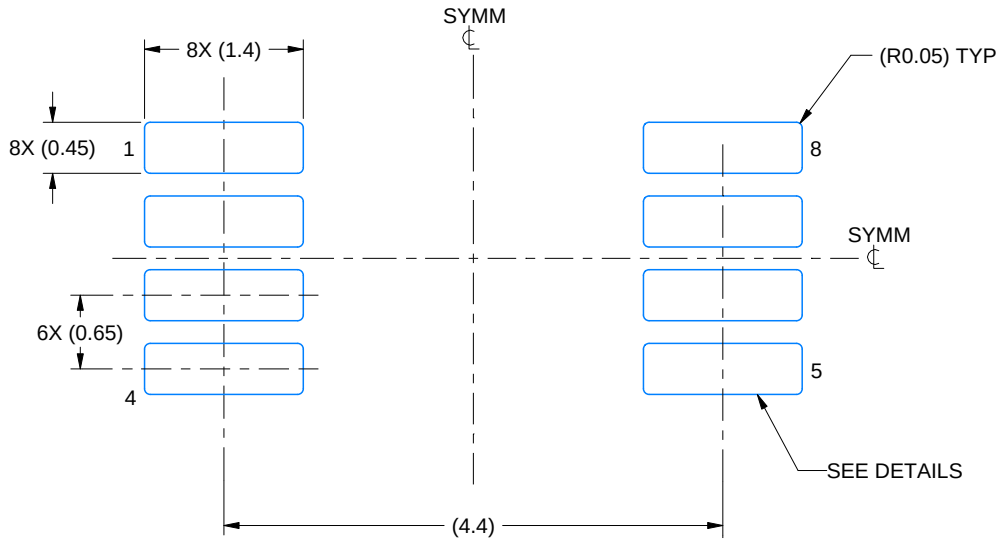
SMALL OUTLINE PACKAGE



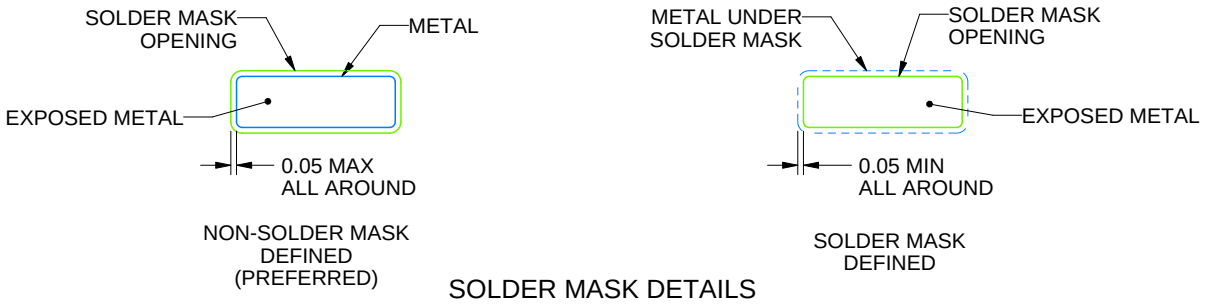
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

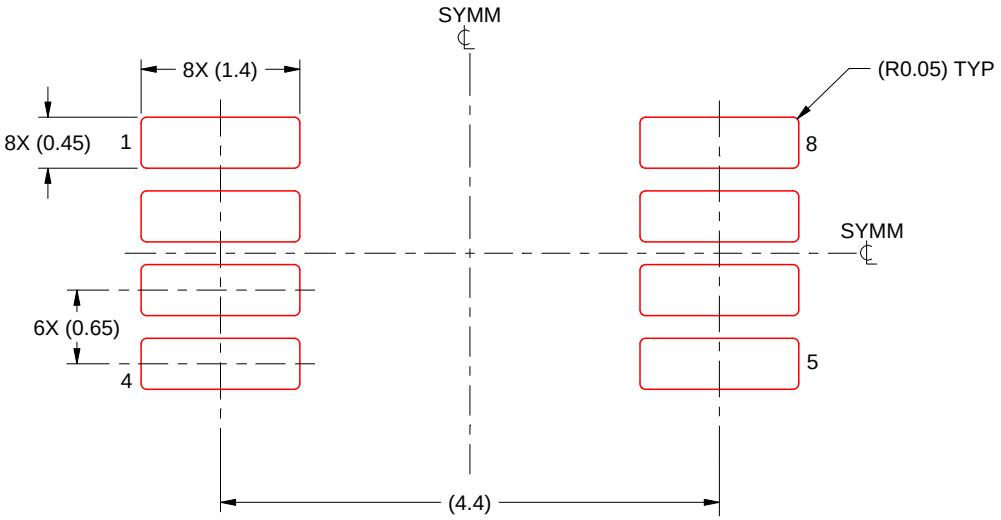


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス· デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、TI の販売条件、または ti.com やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、TI はそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265