TEXAS INSTRUMENTS
OPA171, OPA2171, OPA4171
JAJSFB4F – SEPTEMBER 2010 – REVISED APRIL 2018

OPAx171 36V、単一電源、SOT-553の汎用オペアンプ

1 特長

- 電源電圧範囲: 2.7V～36V、±1.35V～±18V
- 低ノイズ: 14nV/√Hz
- 低いオフセット・ドリフト：±0.3µV/°C（標準値）
- RFIフィルタ付きの入力
- 入力範囲は負の電源電圧にも対応
- 入力範囲は正の電源電圧まで動作
- レール・ツー・レール出力
- ゲイン帯域幅: 3MHz
- 低い静止電流：アンプごとに475µA
- 高い同相除去：120dB（標準値）
- 低い入力バイアス電流: 8pA
- 業界標準パッケージ
  - 8ピンSOIC
  - 8ピンMSOP
  - 14ピンTSSOP
- *micro*パッケージ
  - シングルはSOT-553
  - デュアルはVSSOP-8

2 アプリケーション

- 電源モジュールのトラッキング・アンプ
- 商業施設の電源
- トランスデューサ・アンプ
- ブリッジ・アンプ
- 温度計測
- ひずみゲージ・アンプ
- 高精度積分器
- バッテリ駆動計測器
- 試験装置

3 概要

OPA171、OPA2171、OPA4171 (OPAx171)は36V、単一電源、低ノイズのオペアンプのファミリで、2.7V (±1.35V)～36V (±18V)の範囲の電源で動作できます。microパッケージで供給されるこれらのデバイスは、低オフセット、低ドリフト、必要な帯域幅を小さな静止電流で実現しています。シングル、デュアル、クワッドの各製品で同一の仕様を備え、設計の柔軟性を高めています。

ほとんどのオペアンプでは1つの電源電圧でのみ動作が規定されているのに対し、OPAx171ファミリは2.7V～36Vでの動作が規定されています。入力信号が電源レールの範囲外になっても位相反転を引き起こすことはありません。OPAx171ファミリは、最大300pFの容量性負荷で安定です。通常の動作時に、入力は負のレールより100mV下、および上限レールの2V以内で動作できます。これらのデバイスは、上限レールより100mV上まで完全なレール・ツー・レール入力で動作できますが、上限レールから2V以内では性能が低下することに注意してください。

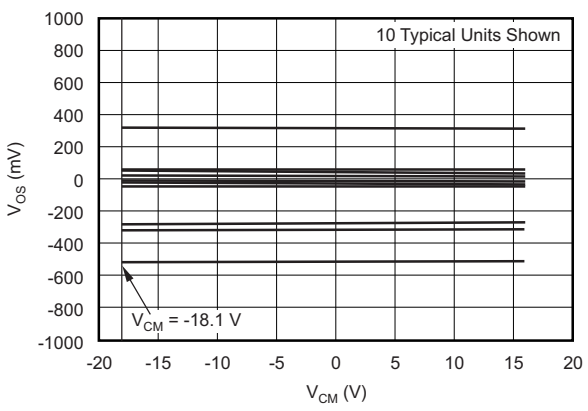
OPAx171シリーズのオペアンプは、-40°C～+125°Cでの動作が規定されています。

製品情報(1)

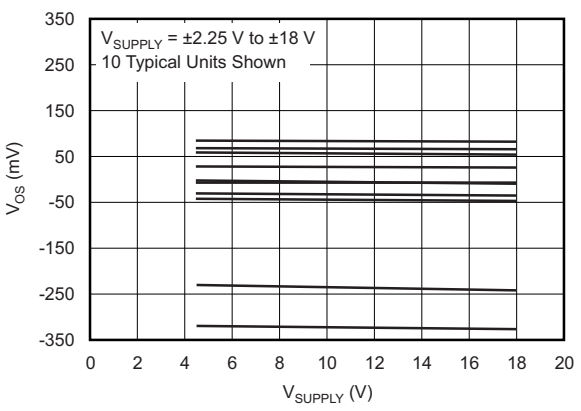
型番	パッケージ	本体サイズ(公称)
OPA171	SOT-23 (5)	1.60mm×2.90mm
OPA2171	SOIC (8)	3.90mm×4.90mm
OPA4171	TSSOP (14)	4.40mm×5.00mm
	SOIC (14)	3.90mm×8.65mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

オフセット電圧とコモンモード電圧との関係



オフセット電圧と電源電圧との関係



英語版のTI製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.comで閲覧でき、その内容が常に優先されます。TIでは翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision E (April 2015) から **Revision F** に変更 **Page**

- Changed minimum supply voltage value from ±20 V to 0 V in *Absolute Maximum Ratings* table ... 7
- Added maximum supply voltage value of 40 V to *Absolute Maximum Ratings* table ... 7
- Rewrote *Electrical Overstress* subsection content in *Application Information* section ... 21

Revision D (September 2012) から **Revision E** に変更 **Page**

- デバイスのタイトル（「バリュー・ライン・シリーズ」を削除）変更 ... 1
- 「*ESD定格*」表、「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクションを追加 ... 1

Revision C (June 2011) から **Revision D** に変更 **Page**

- タイトルに「バリュー・ライン・シリーズ」を追加 ... 1

Revision B (November 2010) から **Revision C** に変更 **Page**

- デバイスの図にMSOP-8パッケージを追加 ... 1
- 「特長」の箇条書きにMSOP-8パッケージを追加 ... 1
- 「製品ファミリ」表にMSOP-8パッケージを追加 ... 1
- Updated pinout configurations for OPA2171 and OPA4171 ... 4
- Added MSOP-8 package to OPA2171 Thermal Information table ... 8
- Added new row for Voltage Output Swing from Rail parameter to *Output* subsection of *Electrical Characteristics* ... 10
- Changed Voltage Output Swing from Rail parameter to over temperature in *Output* subsection of *Electrical Characteristics* ... 10
- Changed 図 9 ... 12

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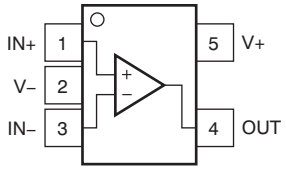
Revision A (November, 2010) から Revision B に変更 **Page**

- Changed input offset voltage specification 9
- Changed input offset voltage, over temperature specification 9
- Changed quiescent current per amplifier, over temperature specification 10

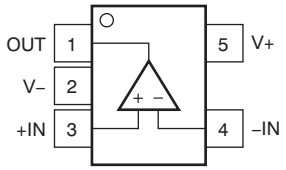
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5 Pin Configuration and Functions

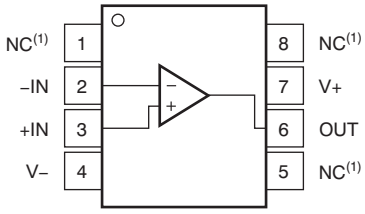
OPA171 DRL Package
5-Pin SOT-553
Top View



OPA171 DBV Package
5-Pin SOT-23
Top View



OPA171 D Package
8-Pin SOIC
Top View



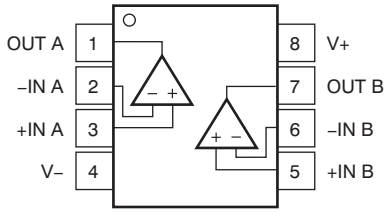
(1) NC- no internal connection

Pin Functions: OPA171

PIN				I/O	DESCRIPTION
NAME	DRL	DBV	D		
+IN	1	3	3	I	Noninverting input
–IN	3	4	2	I	Inverting input
OUT	4	1	6	O	Output
V+	5	5	7	—	Positive (highest) supply
V–	2	2	4	—	Negative (lowest) supply
NC	—	—	1, 5, 8	—	No internal connection (can be left floating)

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OPA2171 D, DCU, and DCK Packages
8-Pin SO, VSSOP and MSOP
Top View

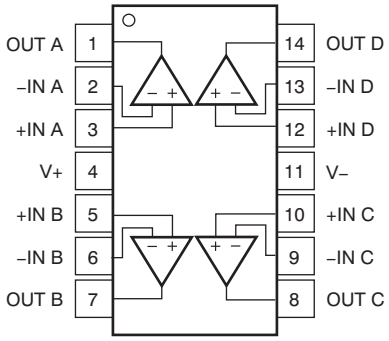


Pin Functions: OPA2171

PIN		I/O	DESCRIPTION
NAME	NO.		
+IN A	3	I	Noninverting input
+IN B	5	I	Noninverting input
–IN A	2	I	Inverting input
–IN B	6	O	Inverting input
OUT A	1	O	Output
OUT B	7	—	Output
V+	8	—	Positive (highest) supply
V–	4	—	Negative (lowest) supply

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OPA4171 D and PW Packages
14-Pin SO and TSSOP
Top View



Pin Functions: OPA4171

PIN		I/O	DESCRIPTION
NAME	NO.		
+IN A	3	I	Noninverting input
+IN B	5	I	Noninverting input
+IN C	10	I	Noninverting input
+IN D	12	I	Noninverting input
–IN A	2	I	Inverting input
–IN B	6	I	Inverting input
–IN C	9	I	Inverting input
–IN D	13	I	Inverting input
OUT A	1	O	Output
OUT B	7	O	Output
OUT C	8	O	Output
OUT D	14	O	Output
V+	4	—	Positive (highest) supply
V–	11	—	Negative (lowest) supply

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range, (unless otherwise noted) (1)

		MIN	MAX	UNIT
Supply voltage		0	40	V
Signal input terminals	Voltage	(V–) – 0.5	(V+) + 0.5	V
	Current	–10	10	mA
Output short circuit (2)		Continuous		
Operating temperature		–55	150	°C
Junction temperature			150	°C
Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage (V+ – V–)	4.5 (±2.25)		36 (±18)	V
Specified temperature	–40		125	°C

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6.4 Thermal Information: OPA171

THERMAL METRIC(1)		OPA171			UNIT
		D (SO)	DBV (SOT-23)	DRL (SOT-553)	
		8 PINS	5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	149.5	245.8	208.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	97.9	133.9	0.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	87.7	83.6	42.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	35.5	18.2	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	89.5	83.1	42.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Thermal Information: OPA2171

THERMAL METRIC(1)		OPA2171			UNIT
		D (SO)	DGK (MSOP)	DCU (VSSOP)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	134.3	175.2	195.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	72.1	74.9	59.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	60.6	22.2	115.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	18.2	1.6	4.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	53.8	22.8	114.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report .

6.6 Thermal Information: OPA4171

THERMAL METRIC(1)		OPA4171		UNIT
		D (SOIC)	PW (TSSOP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	93.2	106.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	51.8	24.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	49.4	59.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	13.5	0.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	42.2	54.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.7 Electrical Characteristics

at T_A = 25°C, V_S = 2.7 to 36 V, V_{CM} = V_{OUT} = V_S / 2, and R_{LOAD} = 10 kΩ connected to V_S / 2, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage			0.25	±1.8	mV
	Over temperature	T_A = –40°C to +125°C		0.3	±2	mV
dV_{OS}/dT	Drift	T_A = –40°C to +125°C		0.3	±2	µV/°C
	vs power supply	V_S = 4 to 36 V T_A = –40°C to +125°C		1	±3	µV/V
	Channel separation, DC	DC		5		µV/V
INPUT BIAS CURRENT						
I_B	Input bias current			±8	±15	pA
	Over temperature	T_A = –40°C to +125°C			±3.5	nA
I_{OS}	Input offset current			±4		pA
	Over temperature	T_A = –40°C to +125°C			±3.5	nA
NOISE						
	Input voltage noise	f = 0.1 Hz to 10 Hz		3		μV_{PP}
e_n	Input voltage noise density	f = 100 Hz		25		$nV/\sqrt{Hz}$
		f = 1 kHz		14		$nV/\sqrt{Hz}$
INPUT VOLTAGE						
V_{CM}	Common-mode voltage range(1)		(V–) – 0.1 V		(V+) – 2 V	V
CMRR	Common-mode rejection ratio	V_S = ±2 V (V–) – 0.1 V < V_{CM} < (V+) – 2 V T_A = –40°C to +125°C	90	104		dB
		V_S = ±18 V (V–) – 0.1 V < V_{CM} < (V+) – 2 V T_A = –40°C to +125°C	104	120		dB
INPUT IMPEDANCE						
	Differential			100 || 3		MΩ || pF
	Common-mode			6 || 3		10^{12}Ω || pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	V_S = 4 V to 36 V (V–) + 0.35 V < V_O < (V+) – 0.35 V T_A = –40°C to +125°C	110	130		dB
FREQUENCY RESPONSE						
GBP	Gain bandwidth product			3		MHz
SR	Slew rate	G = 1		1.5		V/µs
t_S	Settling time	To 0.1% V_S = ±18 V, G = 1 10-V step		6		µs
		To 0.01% (12 bit) V_S = ±18 V, G = 1 10-V step		10		µs
	Overload recovery time	V_{IN} × gain > V_S		2		µs
THD+N	Total harmonic distortion + noise	G = 1, f = 1 kHz V_O = 3 V_{RMS}		0.0002%		
OUTPUT						

(1) The input range can be extended beyond (V+) – 2 V up to V+. See *Typical Characteristics* and *Application and Implementation* for additional information.

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Electrical Characteristics (continued)

at T_A = 25°C, V_S = 2.7 to 36 V, V_{CM} = V_{OUT} = V_S / 2, and R_{LOAD} = 10 kΩ connected to V_S / 2, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_O	Voltage output swing from rail	V_S = 5 V R_L = 10 kΩ		30		mV
	Over temperature	R_L = 10 kΩ A_{OL} ≥ 110 dB T_A = –40°C to +125°C	(V–) + 0.35		(V+) – 0.35	V
I_{SC}	Short-circuit current			+25/–35		mA
C_{LOAD}	Capacitive load drive			See *Typical Characteristics*		pF
R_O	Open-loop output resistance	f = 1 MHz I_O = 0 A		150		Ω
POWER SUPPLY						
V_S	Specified voltage range		2.7		36	V
I_Q	Quiescent current per amplifier	I_O = 0 A		475	595	µA
	Over temperature	I_O = 0 A T_A = –40°C to +125°C			650	µA
TEMPERATURE						
	Specified range		–40		125	°C
	Operating range		–55		150	°C

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6.8 Typical Characteristics: Table of Graphs

表 1. Characteristic Performance Measurements

DESCRIPTION	FIGURE
Offset Voltage Production Distribution	図 1
Offset Voltage Drift Distribution	図 2
Offset Voltage vs Temperature	図 3
Offset Voltage vs Common-Mode Voltage	図 4
Offset Voltage vs Common-Mode Voltage (Upper Stage)	図 5
Offset Voltage vs Power Supply	図 6
I_B and I_{OS} vs Common-Mode Voltage	図 7
Input Bias Current vs Temperature	図 8
Output Voltage Swing vs Output Current (Maximum Supply)	図 9
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Maximum Output Voltage vs Frequency	図 35
Channel Separation vs Frequency	図 36

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6.9 Typical Characteristics

V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, (unless otherwise noted)

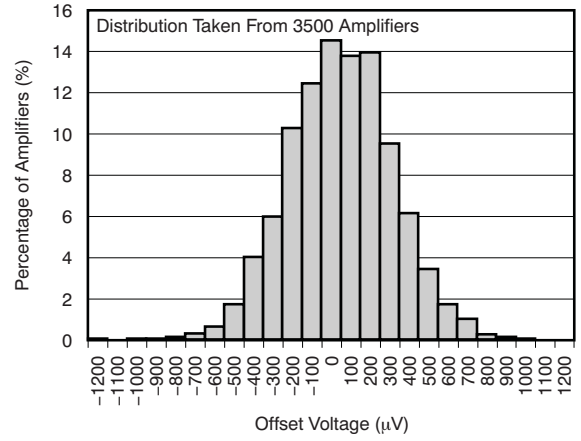


図 1. Offset Voltage Production Distribution

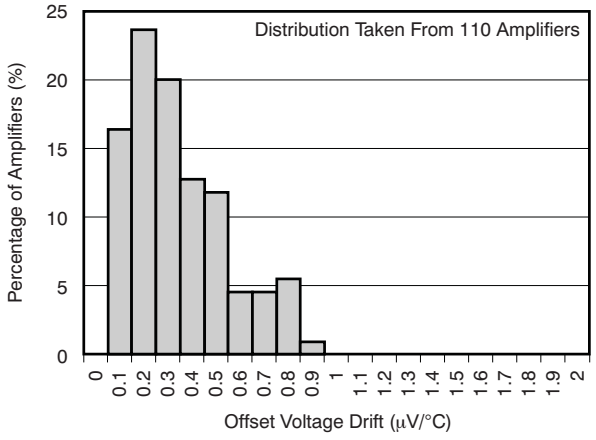


図 2. Offset Voltage Drift Distribution

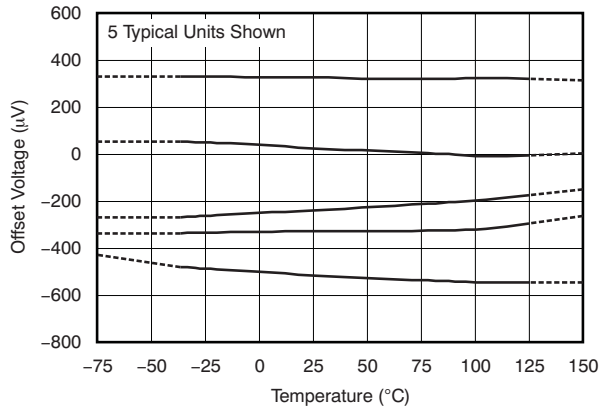


図 3. Offset Voltage vs Temperature

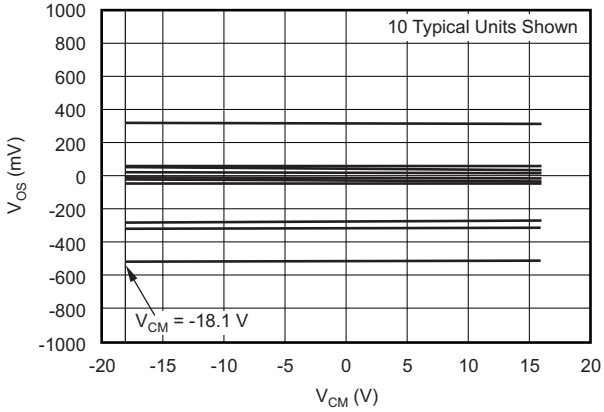


図 4. Offset Voltage vs Common-Mode Voltage

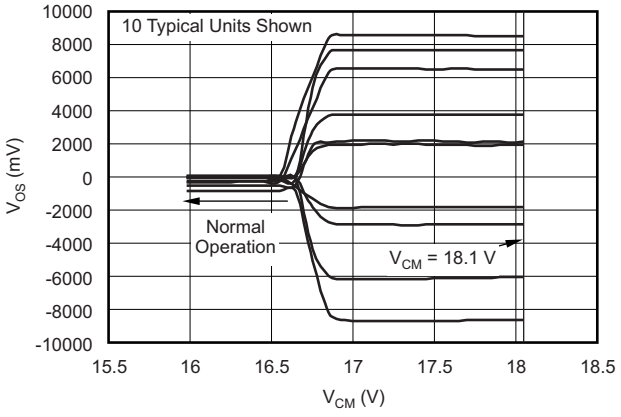


図 5. Offset Voltage vs Common-Mode Voltage (Upper Stage)

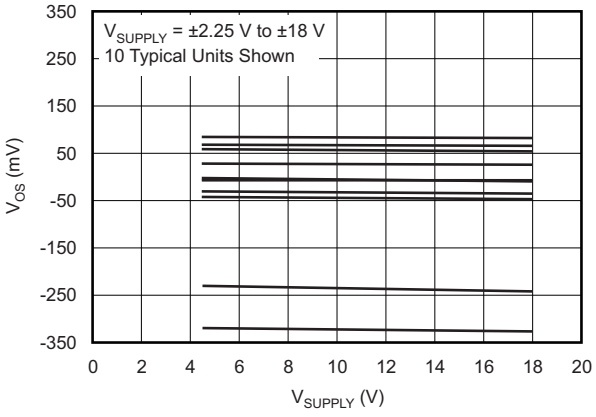


図 6. Offset Voltage vs Power Supply

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Typical Characteristics (continued)

V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, (unless otherwise noted)

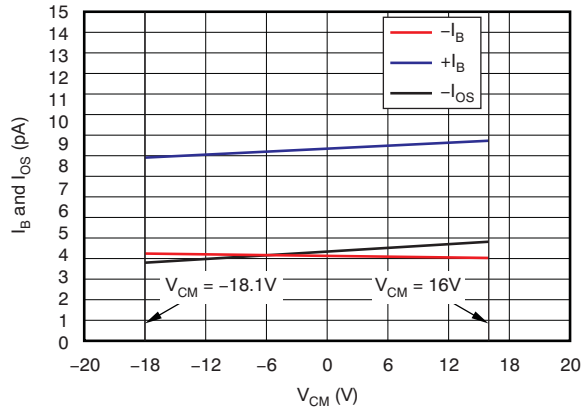


図 7. I_B and I_{OS} vs Common-Mode Voltage

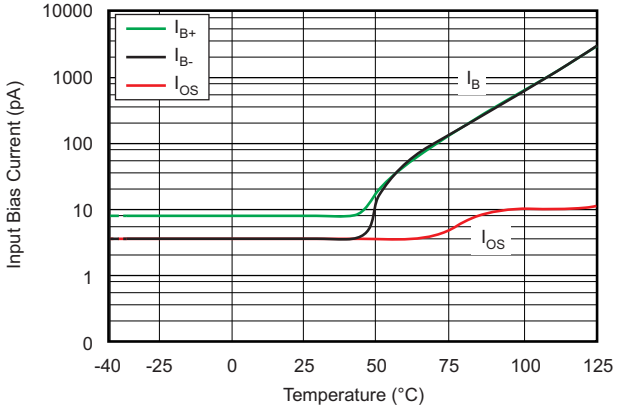


図 8. Input Bias Current vs Temperature

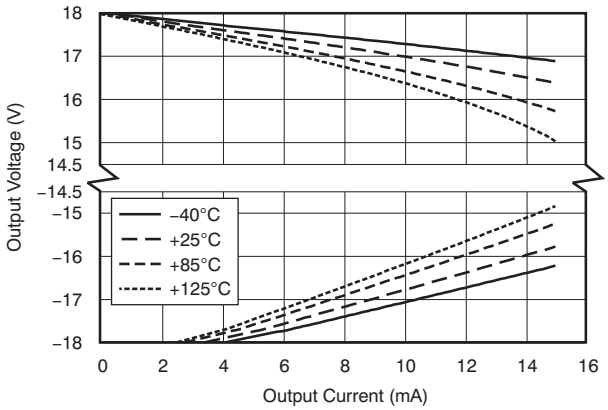


図 9. Output Voltage Swing vs Output Current (Maximum Supply)

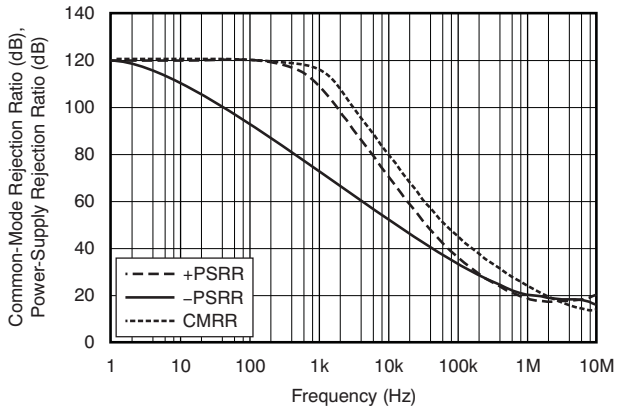


図 10. CMRR and PSRR vs Frequency (Referred-to Input)

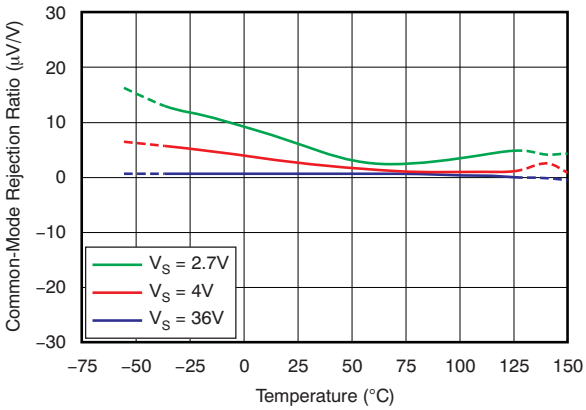


図 11. CMRR vs Temperature

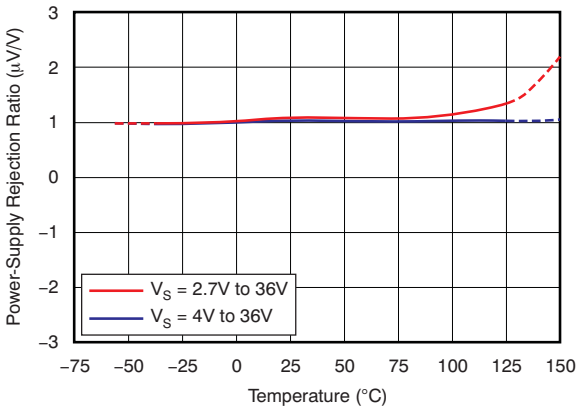


図 12. PSRR vs Temperature

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Typical Characteristics (continued)

V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, (unless otherwise noted)

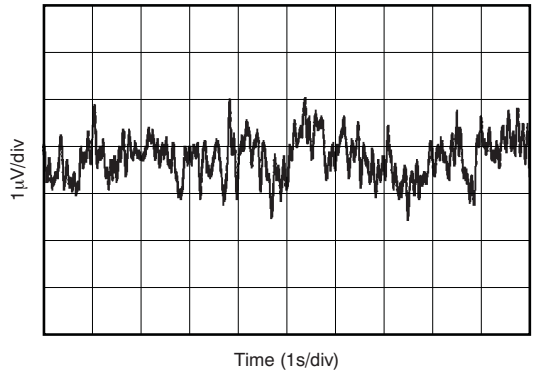


図 13. 0.1-Hz to 10-Hz Noise

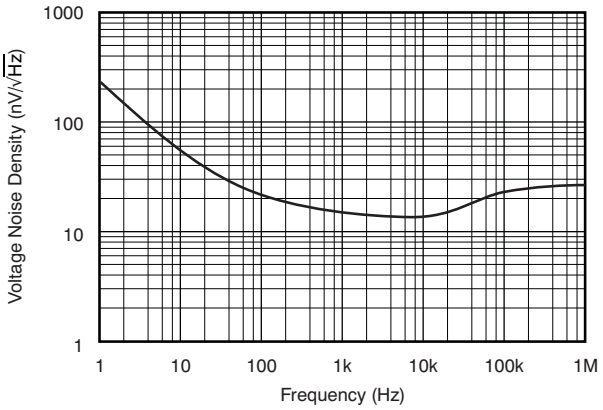


図 14. Input Voltage Noise Spectral Density vs Frequency

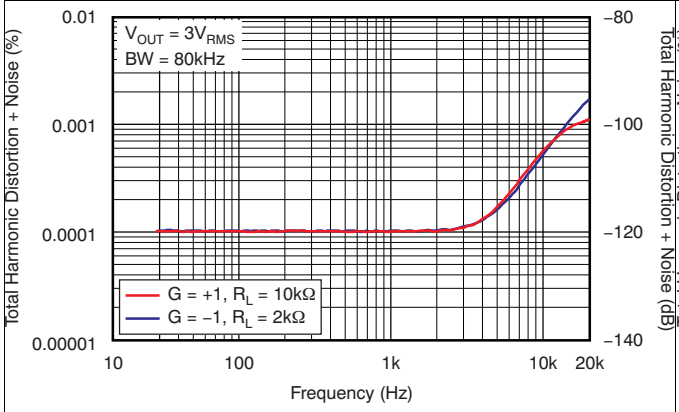


図 15. THD+N Ratio vs Frequency

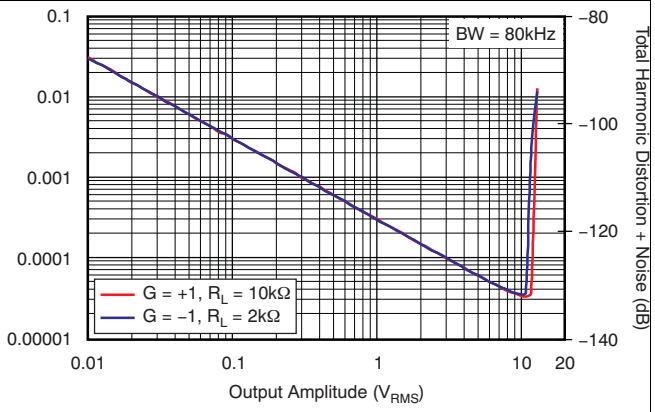


図 16. THD+N vs Output Amplitude

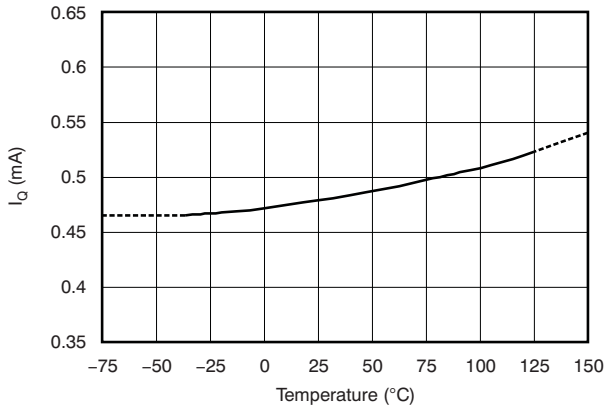


図 17. Quiescent Current vs Temperature

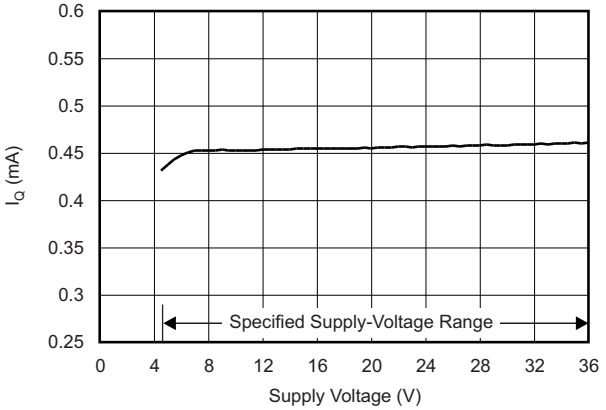


図 18. Quiescent Current vs Supply Voltage

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Typical Characteristics (continued)

V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, (unless otherwise noted)

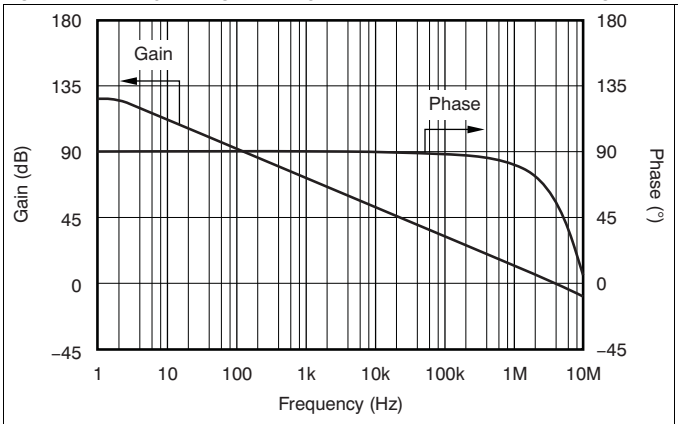


図 19. Open-Loop Gain and Phase vs Frequency

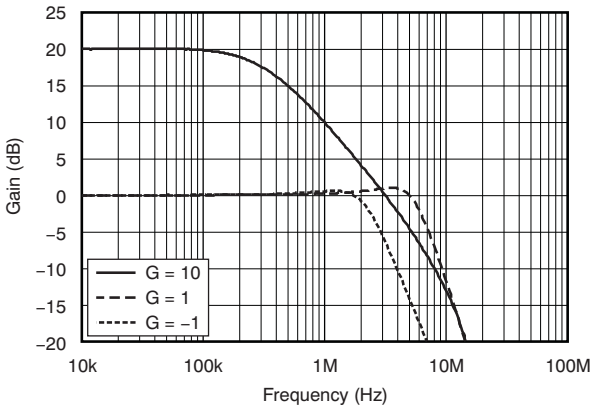


図 20. Closed-Loop Gain vs Frequency

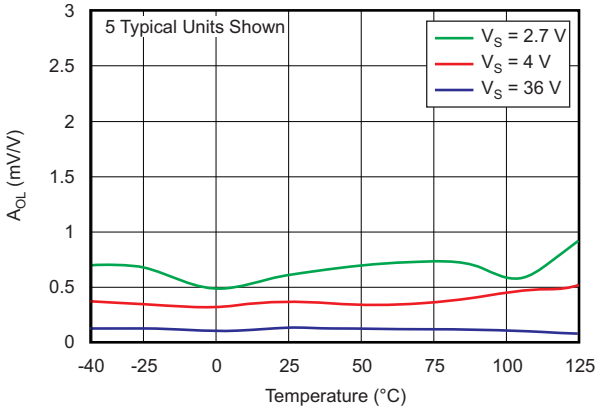


図 21. Open-Loop Gain vs Temperature

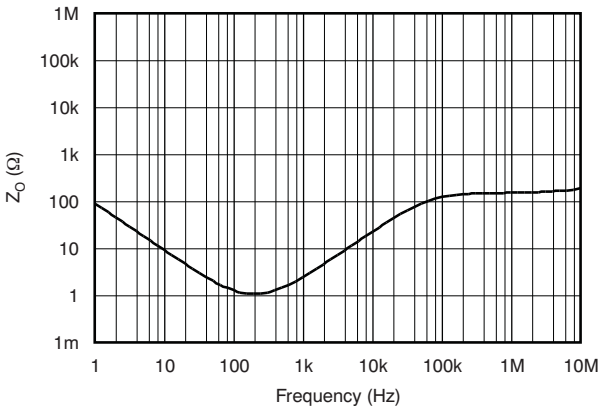


図 22. Open-Loop Output Impedance vs Frequency

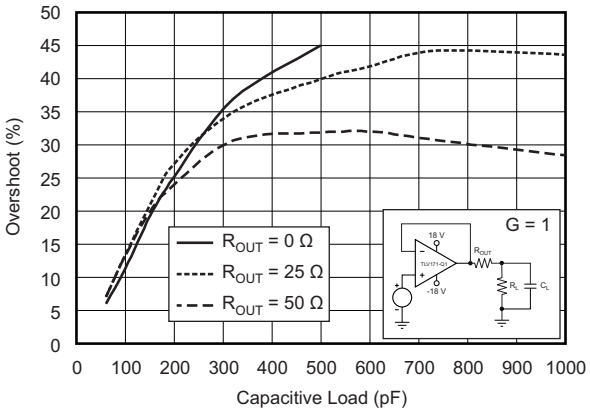


図 23. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

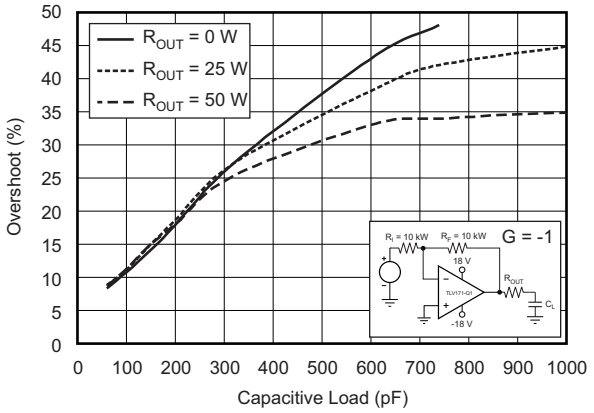


図 24. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

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Typical Characteristics (continued)

V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, (unless otherwise noted)

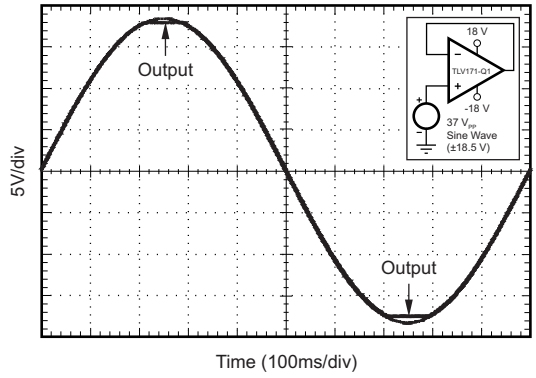


図 25. No Phase Reversal

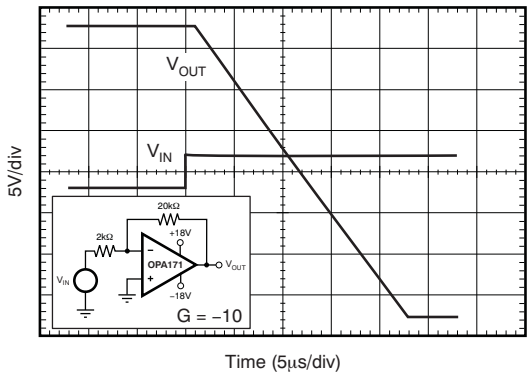


図 26. Positive Overload Recovery

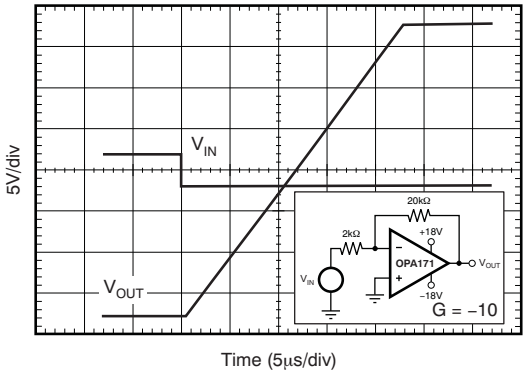


図 27. Negative Overload Recovery

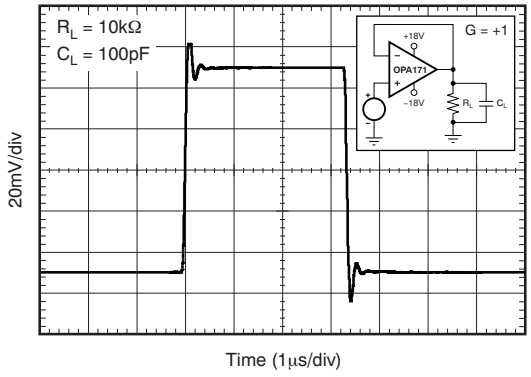


図 28. Small-Signal Step Response (100 mV)

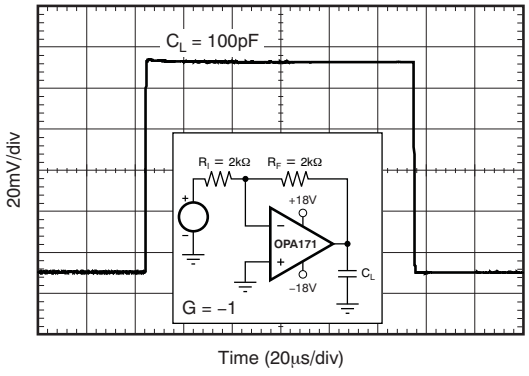


図 29. Small-Signal Step Response (100 mV)

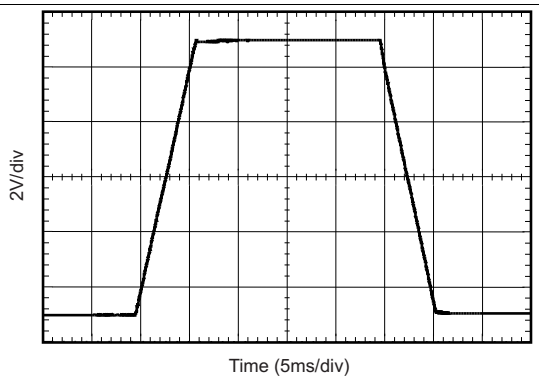


図 30. Large-Signal Step Response

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Typical Characteristics (continued)

V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, (unless otherwise noted)

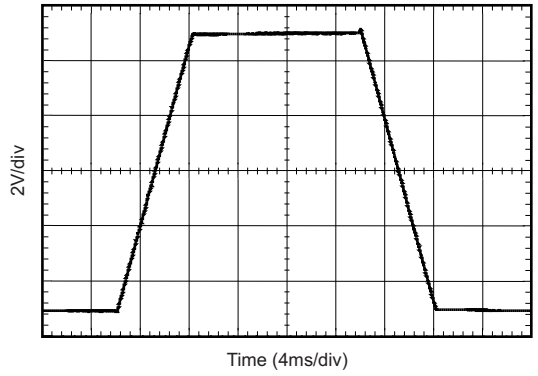


図 31. Large-Signal Step Response

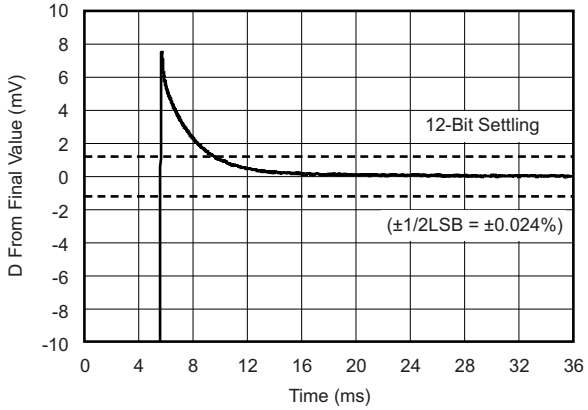


図 32. Large-Signal Settling Time (10-V Positive Step)

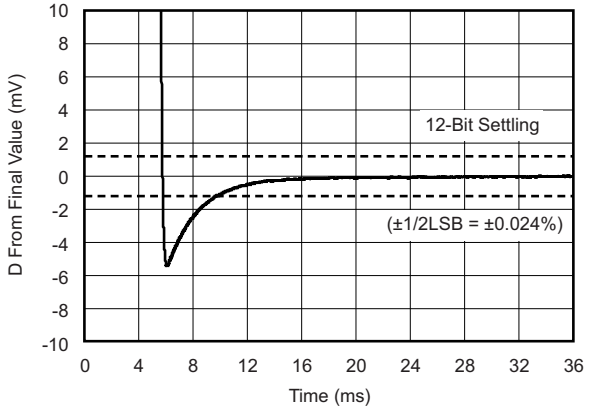


図 33. Large-Signal Settling Time (10-V Negative Step)

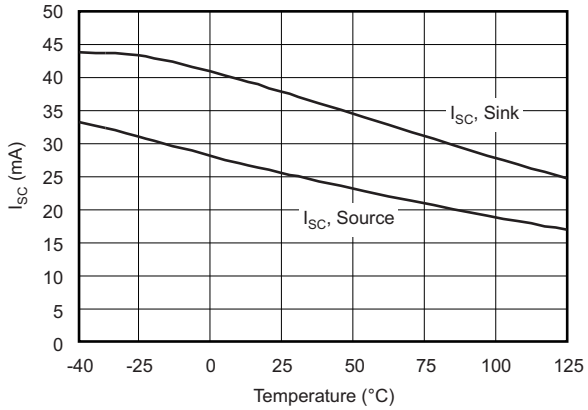


図 34. Short-Circuit Current vs Temperature

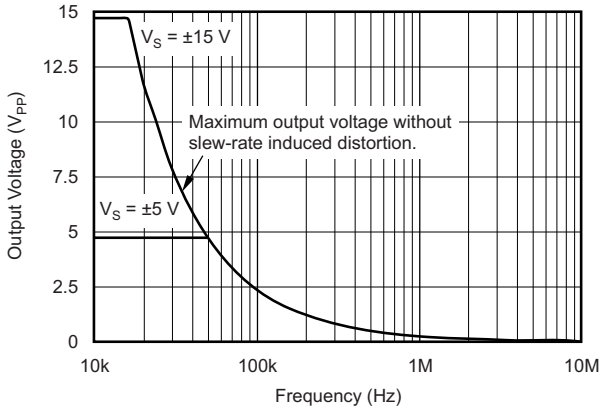


図 35. Maximum Output Voltage vs Frequency

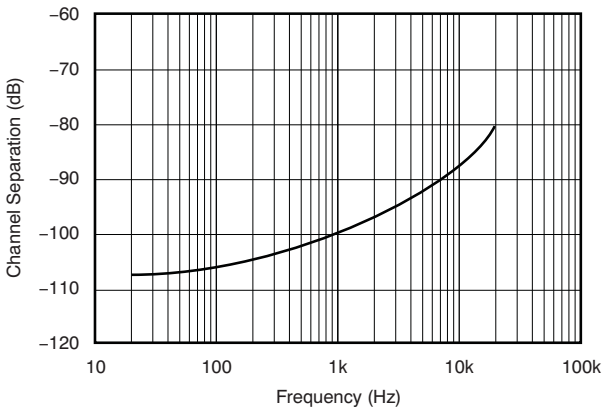


図 36. Channel Separation vs Frequency

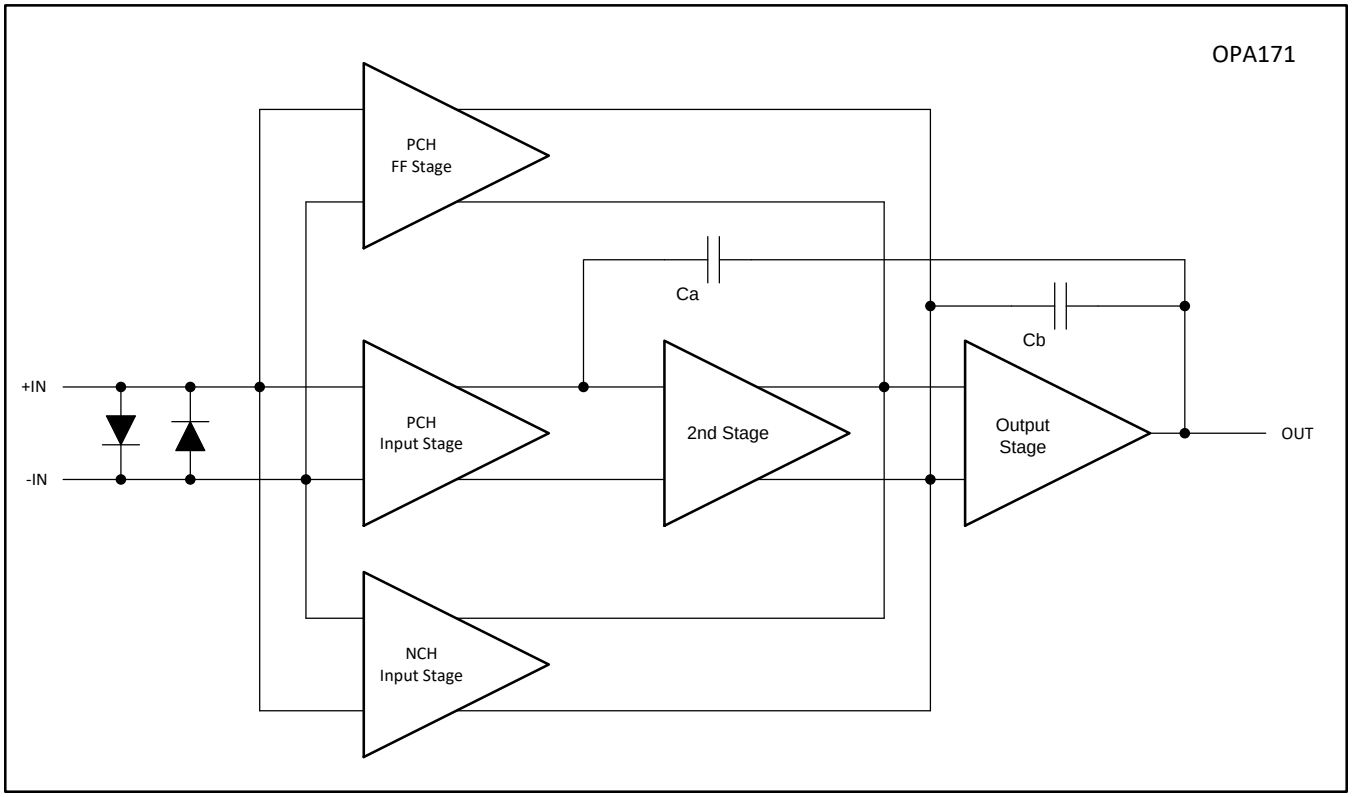
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7 Detailed Description

7.1 Overview

The OPAx171 operational amplifiers provide high overall performance, and are designed for many general-purpose applications. The excellent offset drift of only 2 µV/°C provides excellent stability over the entire temperature range. In addition, the series offers good overall performance with high CMRR, PSRR, and A_{OL}. As with all amplifiers, applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, 0.1-µF capacitors are adequate.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Operating Characteristics

The OPAx171 family of amplifiers is specified for operation from 2.7 to 36 V (±1.35 to ±18 V). Many of the specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in *Typical Characteristics* .

7.3.2 Common-Mode Voltage Range

The input common-mode voltage range of the OPAx171 series extends 100 mV below the negative rail and within 2 V of the top rail for normal operation.

This family can operate with full rail-to-rail input 100 mV beyond the top rail, but with reduced performance within 2 V of the top rail. The typical performance in this range is summarized in 表 2.

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Feature Description (continued)

7.3.3 Phase-Reversal Protection

The OPAx171 family has an internal phase-reversal protection. Many operational amplifiers exhibit a phase reversal when the input is driven beyond its linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The input of the OPAx171 prevents phase reversal with excessive common-mode voltage. Instead, the output limits into the appropriate rail. This performance is shown in 図 37.

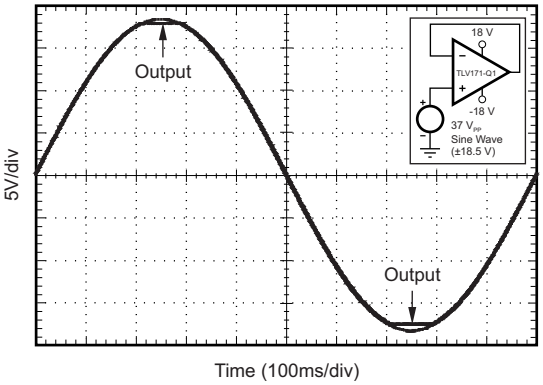


図 37. No Phase Reversal

表 2. Typical Performance Range

PARAMETER	MIN	TYP	MAX	UNIT
Input common-mode voltage	(V+) – 2		(V+) + 0.1	V
Offset voltage		7		mV
vs temperature		12		µV/°C
Common-mode rejection		65		dB
Open-loop gain		60		dB
GBW		0.7		MHz
Slew rate		0.7		V/µs
Noise at f = 1 kHz		30		nV/√Hz

7.3.4 Capacitive Load and Stability

The dynamic characteristics of the OPAx171-Q1 family of devices have been optimized for commonly encountered operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the phase margin of the amplifier and can lead to gain peaking or oscillations. As a result, heavier capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor (for example, R_{OUT} equal to 50 Ω) in series with the output. 図 38 and 図 39 show small-signal overshoot versus capacitive load for several values of R_{OUT}. For details of analysis techniques and application circuits, see *Applications Bulletin AB-028*, available for download from TI.com.

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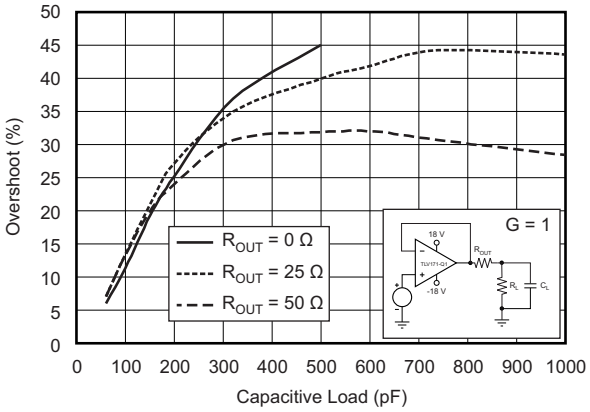


図 38. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

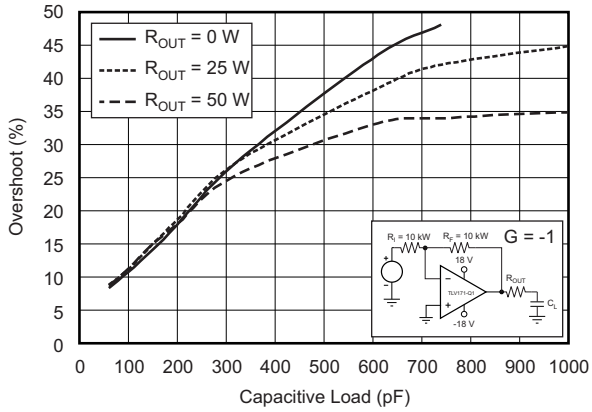


図 39. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

7.4 Device Functional Modes

7.4.1 Common-Mode Voltage Range

The input common-mode voltage range of the OPAx171 family extends 100 mV below the negative rail and within 2 V of the top rail for normal operation.

These devices can operate with full rail-to-rail input 100 mV beyond the top rail, but with reduced performance within 2 V of the top rail. The typical performance in this range is summarized in 表 2.

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8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The OPAx171 operational amplifiers provide high overall performance, and are designed for many general-purpose applications. The excellent offset drift of only 2 µV/°C provides excellent stability over the entire temperature range. In addition, the series offers good overall performance with high CMRR, PSRR, and A_{OL}. As with all amplifiers, applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, 0.1-µF capacitors are adequate.

8.1.1 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but can involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits for protection from accidental ESD events both before and during product assembly.

A good understanding of this basic ESD circuitry and the relevance to an electrical overstress event is helpful. 図 40 shows the ESD circuits contained in the OPAx171 (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power supply lines, where the diodes meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

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Application Information (continued)

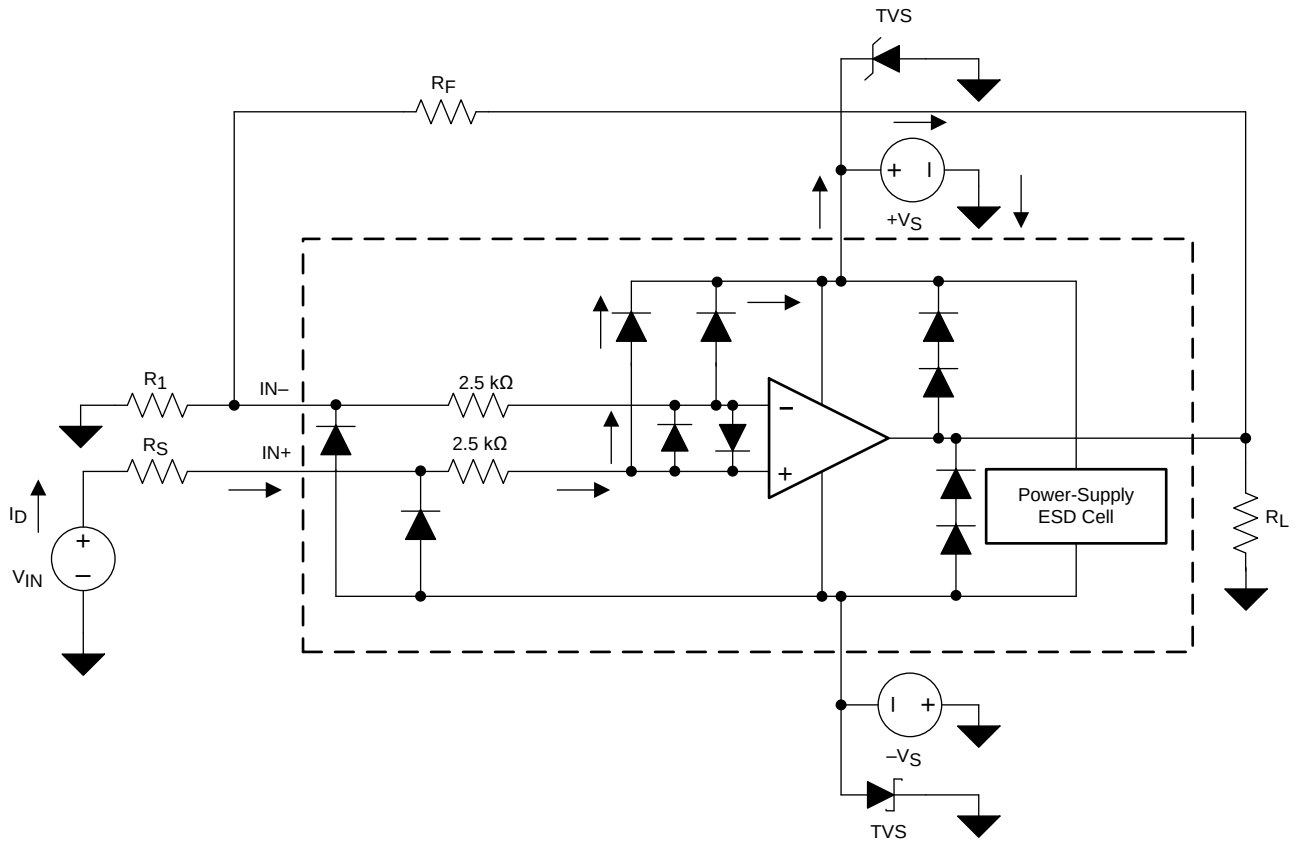


図 40. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application

An ESD event produces a short duration, high-voltage pulse that is transformed into a short duration, high-current pulse when discharging through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent damage. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more amplifier device pins, current flows through one or more steering diodes. Depending on the path that the current takes, the absorption device can activate. The absorption device contains a trigger (or threshold voltage) that is above the normal operating voltage of the OPAx171 but below the device breakdown level. When this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

When the operational amplifier connects into a circuit (as shown in 図 40), the ESD protection components are intended to remain inactive and do not become involved in the application circuit operation. However, circumstances may arise when an applied voltage exceeds the operating voltage of a given pin. If this condition occurs, there is a risk that some internal ESD protection circuits can turn on and conduct current. Any such current flow occurs through steering-diode paths and rarely involves the absorption device.

図 40 shows a specific example where the input voltage (V_{IN}) exceeds the positive supply voltage (V+) by 500 mV or more. Much of what happens in the circuit depends on the supply characteristics. If V+ can sink the current, one of the upper steering diodes conducts and directs current to V+. Excessively high current levels can flow with increasingly higher V_{IN}. As a result, the data sheet specifications recommend that applications limit the input current to 10 mA.

If the supply is not capable of sinking the current, V_{IN} begins sourcing current to the operational amplifier and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings.

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Application Information (continued)

Another common question involves what happens to the amplifier if an input signal is applied to the input when the power supplies (V+ or V–) are at 0 V. This question depends on the supply characteristic when at 0 V, or at a level below the input signal amplitude. If the supplies appear to be high-impedance, then the input source supplies the operational amplifier current through the current-steering diodes. This state is not a normal bias condition. Most likely, the amplifier does not operate normally. If the supplies are low-impedance, then the current through the steering diodes can be quite high. The current level depends on the ability of the input source to deliver current and any resistance in the input path.

If there is any uncertainty about the ability of the supply to absorb this current, add external Zener diodes to the supply pins; see 図 40. Select the Zener voltage so that the diode does not turn on during normal operation. However, the Zener voltage must be low enough so that the Zener diode conducts if the supply pin begins to rise above the safe operating, supply-voltage level.

The OPAx171 input pins are protected from excessive differential voltage with back-to-back diodes; see 図 40. In most circuit applications, the input protection circuitry does not affect the application. However, in low gain or G = 1 circuits, fast-ramping input signals can forward bias these diodes because the output of the amplifier cannot respond rapidly enough to the input ramp. If the input signal is fast enough to create this forward-bias condition, limit the input signal current to 10 mA or less. If the input signal current is not inherently limited, an input series resistor can be used to limit the input signal current. This input series resistor degrades the low noise performance of the OPAx171. 図 40 shows an example configuration that implements a current-limiting feedback resistor.

8.2 Typical Application

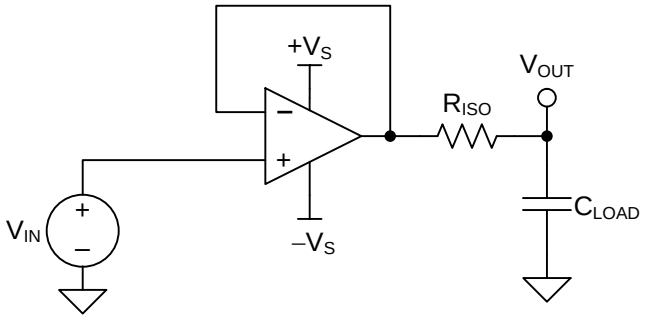


図 41. Unity-Gain Buffer With R_{ISO} Stability Compensation

8.2.1 Design Requirements

The design requirements are:

- Supply voltage: 30 V (±15 V)
- Capacitive loads: 100 pF, 1000 pF, 0.01 μF, 0.1 μF, and 1 μF
- Phase margin: 45° and 60°

8.2.2 Detailed Design Procedure

図 42 shows a unity-gain buffer driving a capacitive load. 式 1 shows the transfer function for the circuit in 図 42. Not shown in 図 42 is the open-loop output resistance of the operational amplifier, R_o.

$$T(s) = \frac{1 + C_{LOAD} \times R_{ISO} \times s}{1 + \left(R_o + R_{ISO}\right) \times C_{LOAD} \times s} \quad (1)$$

The transfer function in 式 1 contains a pole and a zero. The frequency of the pole (f_p) is determined by (R_o + R_{ISO}) and C_{LOAD}. Components R_{ISO} and C_{LOAD} determine the frequency of the zero (f_z). Select R_{ISO} such that the rate of closure (ROC) between the open-loop gain (A_{OL}) and 1/β is 20 dB/decade to obtain a stable system. 図 42 shows the concept. The 1/β curve for a unity-gain buffer is 0 dB.

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Typical Application (continued)

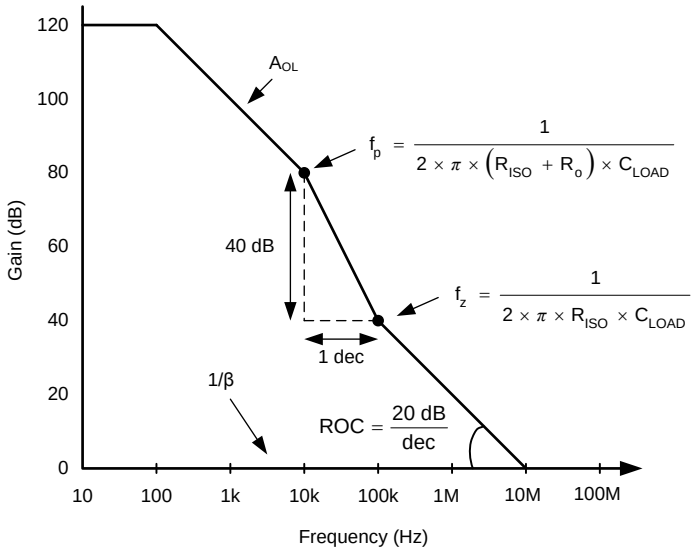


図 42. Unity-Gain Amplifier With R_{ISO} Compensation

ROC stability analysis is typically simulated. The validity of the analysis depends on multiple factors, especially the accurate modeling of R_o. In addition to simulating the ROC, a robust stability analysis includes a measurement of overshoot percentage and AC gain peaking of the circuit using a function generator, oscilloscope, and gain and phase analyzer. Phase margin is then calculated from these measurements. 表 3 shows the overshoot percentage and AC gain peaking that correspond to phase margins of 45° and 60°. For more details on this design and other alternative devices that can be used in place of the OPAx171, see *Capacitive Load Drive Solution using an Isolation Resistor*.

表 3. Phase Margin versus Overshoot and AC Gain Peaking

PHASE MARGIN	OVERSHOOT	AC GAIN PEAKING
45°	23.3%	2.35 dB
60°	8.8%	0.28 dB

8.2.2.1 Capacitive Load and Stability

The dynamic characteristics of the OPAx171 are optimized for commonly encountered operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the phase margin of the amplifier and can lead to gain peaking or oscillations. As a result, heavier capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor (for example, R_{OUT} equal to 50 Ω) in series with the output. 図 38 and 図 39 illustrate graphs of small-signal overshoot versus capacitive load for several values of R_{OUT}. See *Applications Bulletin AB-028*, available for download from the TI website for details of analysis techniques and application circuits.

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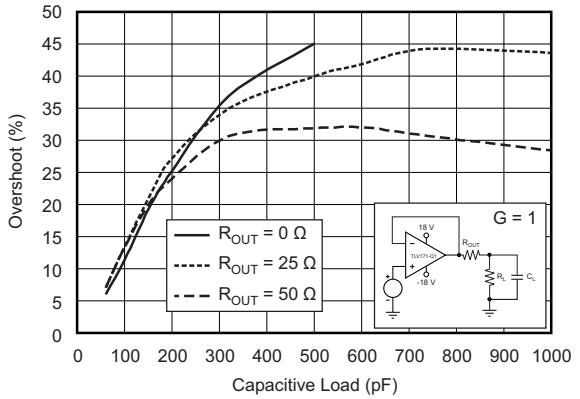


図 43. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

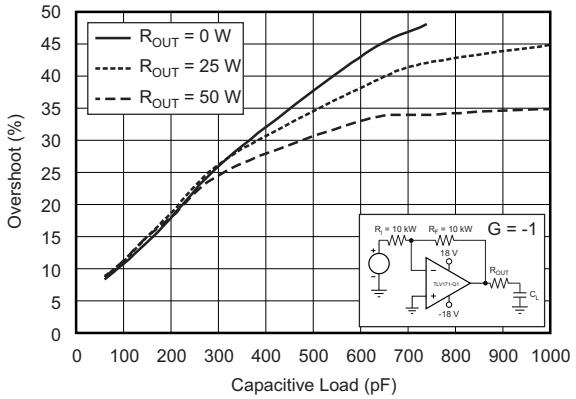


図 44. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

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8.2.3 Application Curve

The OPAx171 meets the supply voltage requirements of 30 V. The OPAx171 is tested for various capacitive loads and RISO is adjusted to get an overshoot corresponding to 表 3. The results of the these tests are summarized in 図 45.

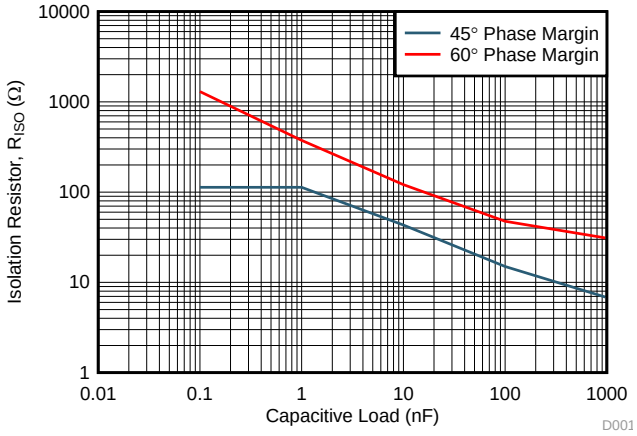


図 45. R_{ISO} vs C_{LOAD}

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9 Power Supply Recommendations

The OPAx171 family is specified for operation from 4.5 V to 36 V (±2.25 V to ±18 V); many specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Specifications* section.

注意

Supply voltages larger than 40 V can permanently damage the device; see the *Absolute Maximum Ratings* table.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For detailed information on bypass capacitor placement, see the *Layout Guidelines* section.

10 Layout

10.1 Layout Guidelines

For best operational performance of the devices, good printed circuit board (PCB) layout practices are recommended. Low-loss, 0.1-µF bypass capacitors must be connected between each supply pin and ground, placed as close to the devices as possible. A single bypass capacitor from V+ to ground is applicable to single-supply applications.

10.2 Layout Example

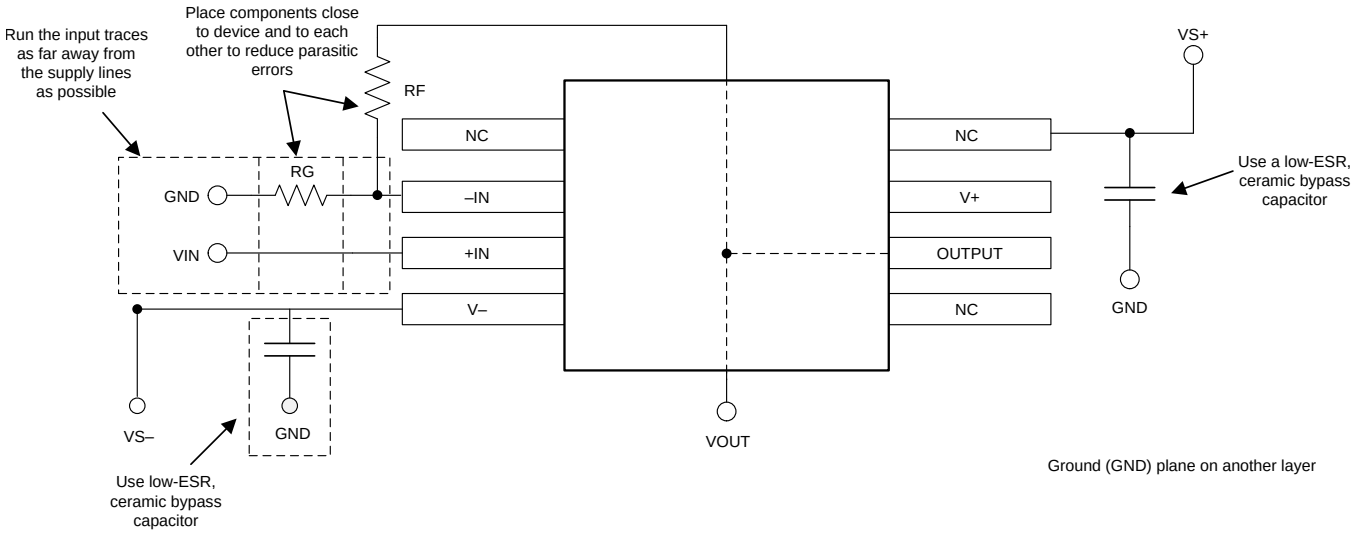


図 46. Operational Amplifier Board Layout for Noninverting Configuration

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11 デバイスおよびドキュメントのサポート

11.1 関連リンク

次の表に、クイック・アクセス・リンクを示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびサンプル注文またはご購入へのクイック・アクセスが含まれます。

表 4. 関連リンク

製品	プロダクト・フォルダ	ご注文はこちら	技術資料	ツールとソフトウェア	サポートとコミュニティ
OPA171	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
OPA2171	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
OPA4171	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

11.2 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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設計サポート ***TIの設計サポート*** 役に立つE2Eフォーラムや、設計サポート・ ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

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11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA171AID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O171A	Samples
OPA171AIDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OSUI	Samples
OPA171AIDBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OSUI	Samples
OPA171AIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O171A	Samples
OPA171AIDRLR	ACTIVE	SOT-5X3	DRL	5	4000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	DAP	Samples
OPA171AIDRLT	ACTIVE	SOT-5X3	DRL	5	250	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	DAP	Samples
OPA2171AID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2171A	Samples
OPA2171AIDCUR	ACTIVE	VSSOP	DCU	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OPOC	Samples
OPA2171AIDCUT	ACTIVE	VSSOP	DCU	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OPOC	Samples
OPA2171AIDGK	ACTIVE	VSSOP	DGK	8	80	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	OPMI	Samples
OPA2171AIDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU | SN | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	OPMI	Samples
OPA2171AIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2171A	Samples
OPA4171AID	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA4171	Samples
OPA4171AIDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA4171	Samples
OPA4171AIPW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4171	Samples
OPA4171AIPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4171	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF OPA171, OPA2171, OPA4171 :

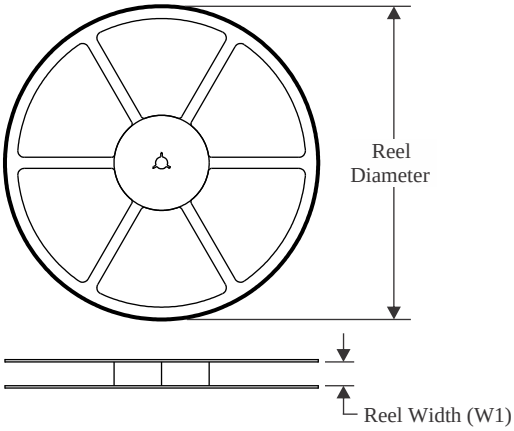
- Automotive : OPA171-Q1, OPA2171-Q1, OPA4171-Q1
- Enhanced Product : OPA2171-EP

NOTE: Qualified Version Definitions:

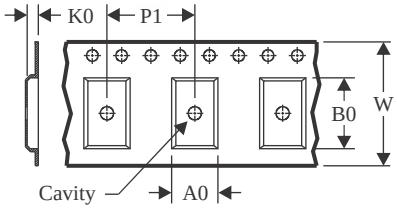
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

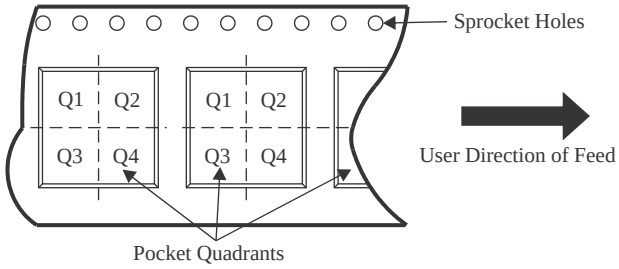


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

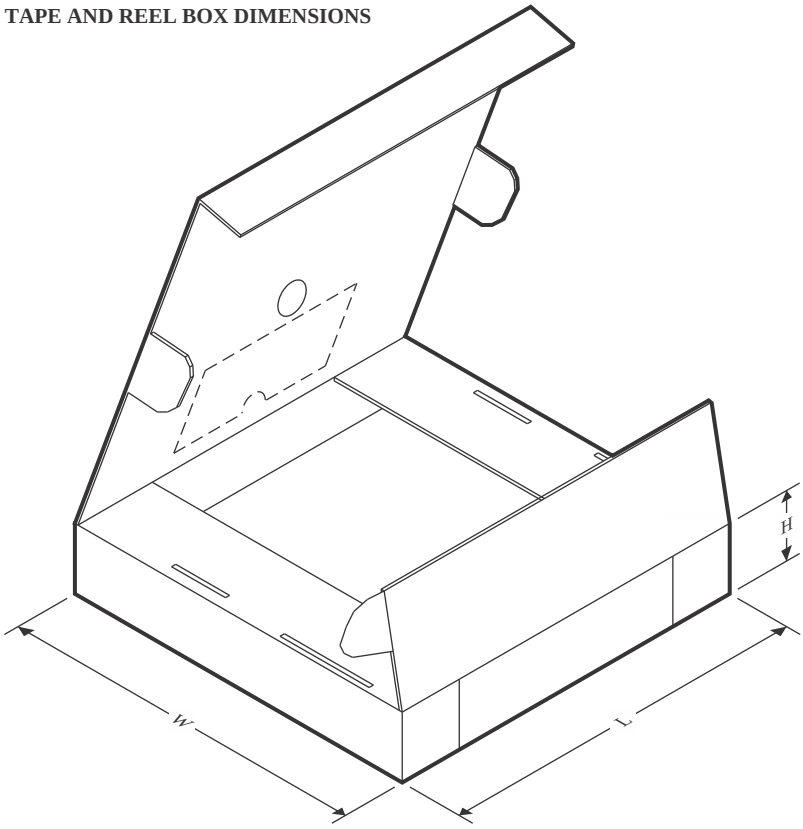
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA171AIDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA171AIDBVR	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA171AIDBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA171AIDBVT	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA171AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA171AIDRLR	SOT-5X3	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
OPA171AIDRLT	SOT-5X3	DRL	5	250	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
OPA2171AIDCUR	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
OPA2171AIDCUT	VSSOP	DCU	8	250	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
OPA2171AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2171AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4171AIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
OPA4171AIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

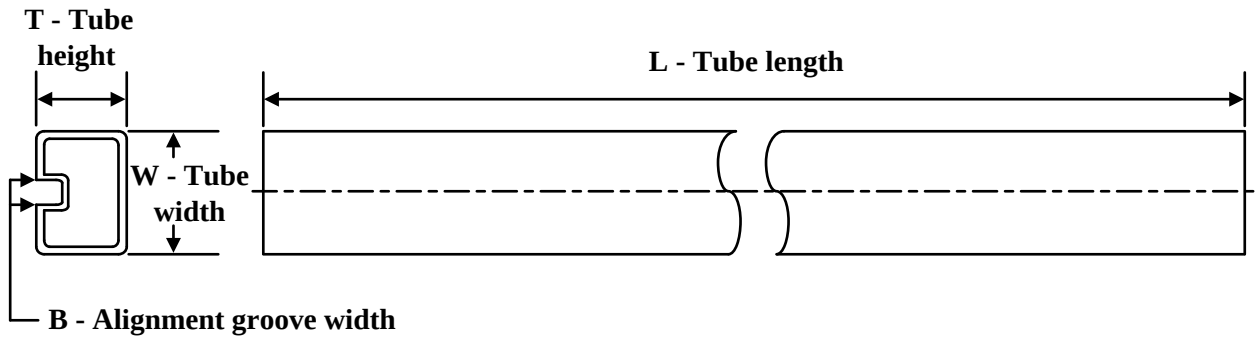
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA171AIDBVR	SOT-23	DBV	5	3000	213.0	191.0	35.0
OPA171AIDBVR	SOT-23	DBV	5	3000	195.0	200.0	45.0
OPA171AIDBVT	SOT-23	DBV	5	250	223.0	270.0	35.0
OPA171AIDBVT	SOT-23	DBV	5	250	213.0	191.0	35.0
OPA171AIDR	SOIC	D	8	2500	356.0	356.0	35.0
OPA171AIDRLR	SOT-5X3	DRL	5	4000	202.0	201.0	28.0
OPA171AIDRLT	SOT-5X3	DRL	5	250	202.0	201.0	28.0
OPA2171AIDCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0
OPA2171AIDCUT	VSSOP	DCU	8	250	202.0	201.0	28.0
OPA2171AIDGKR	VSSOP	DGK	8	2500	356.0	356.0	35.0
OPA2171AIDR	SOIC	D	8	2500	356.0	356.0	35.0
OPA4171AIDR	SOIC	D	14	2500	356.0	356.0	35.0
OPA4171AIPWR	TSSOP	PW	14	2000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

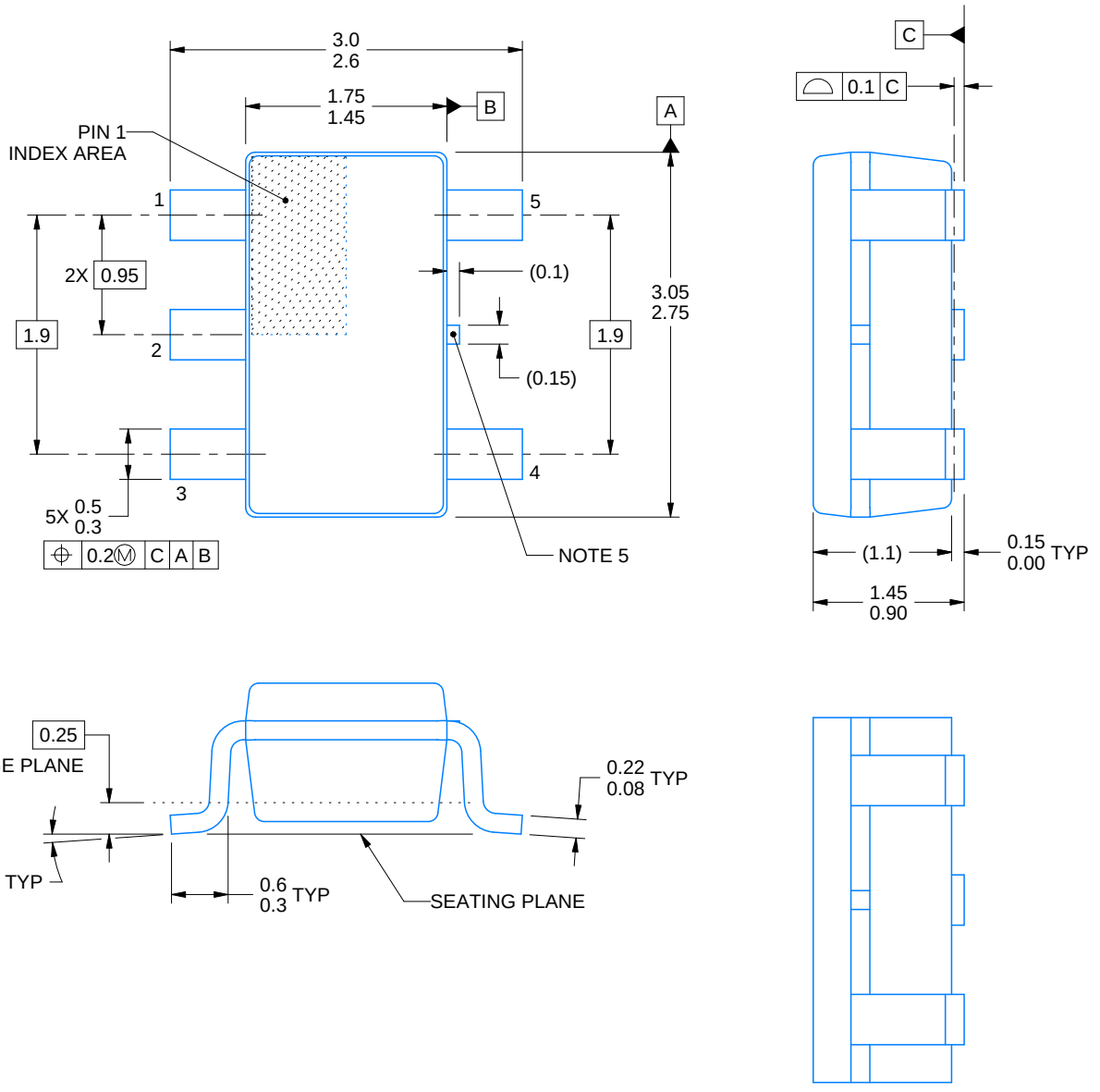
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA171AID	D	SOIC	8	75	506.6	8	3940	4.32
OPA2171AID	D	SOIC	8	75	506.6	8	3940	4.32
OPA2171AIDGK	DGK	VSSOP	8	80	330	6.55	500	2.88
OPA4171AID	D	SOIC	14	50	506.6	8	3940	4.32
OPA4171AIPW	PW	TSSOP	14	90	530	10.2	3600	3.5

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

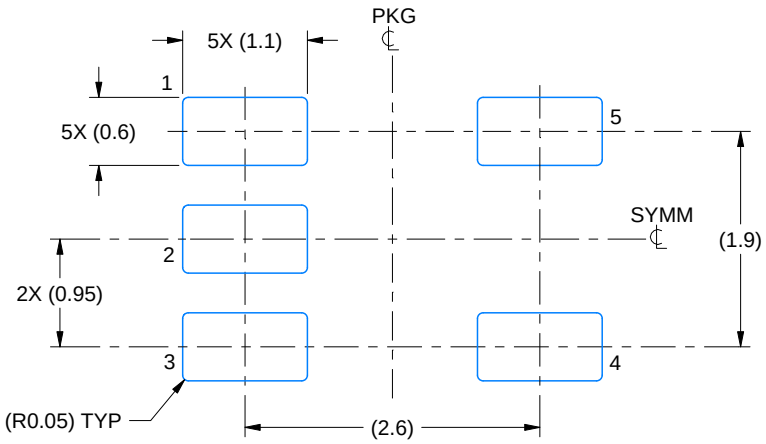


ALTERNATIVE PACKAGE SINGULATION VIEW

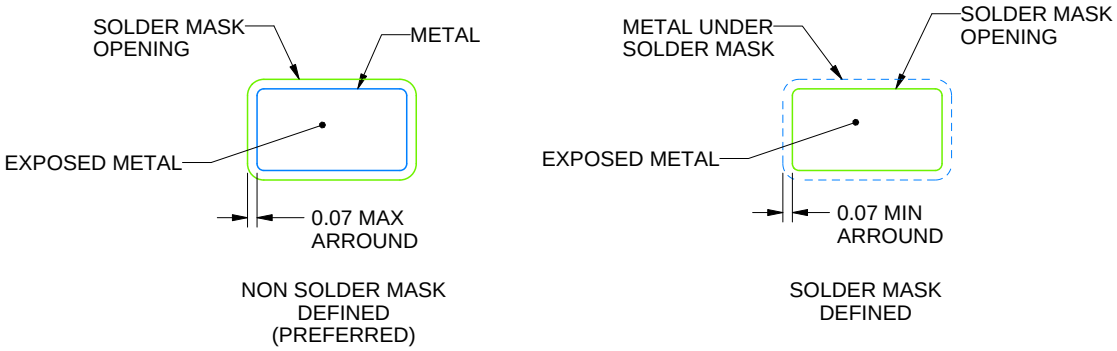
4214839/J 02/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

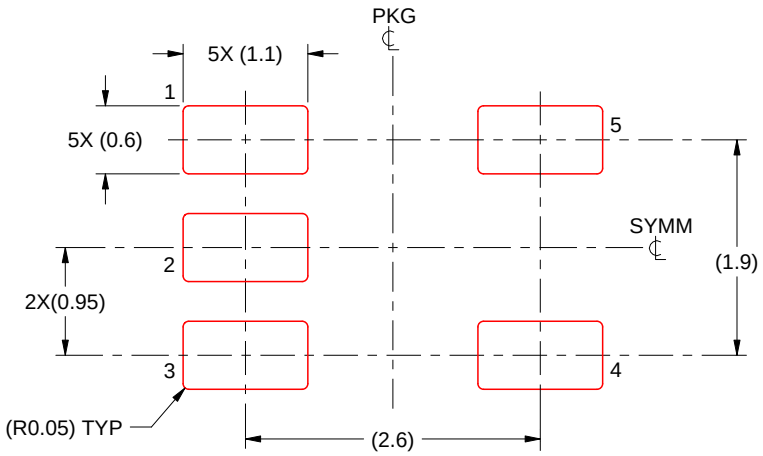


SOLDER MASK DETAILS

4214839/J 02/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/J 02/2024

NOTES: (continued)

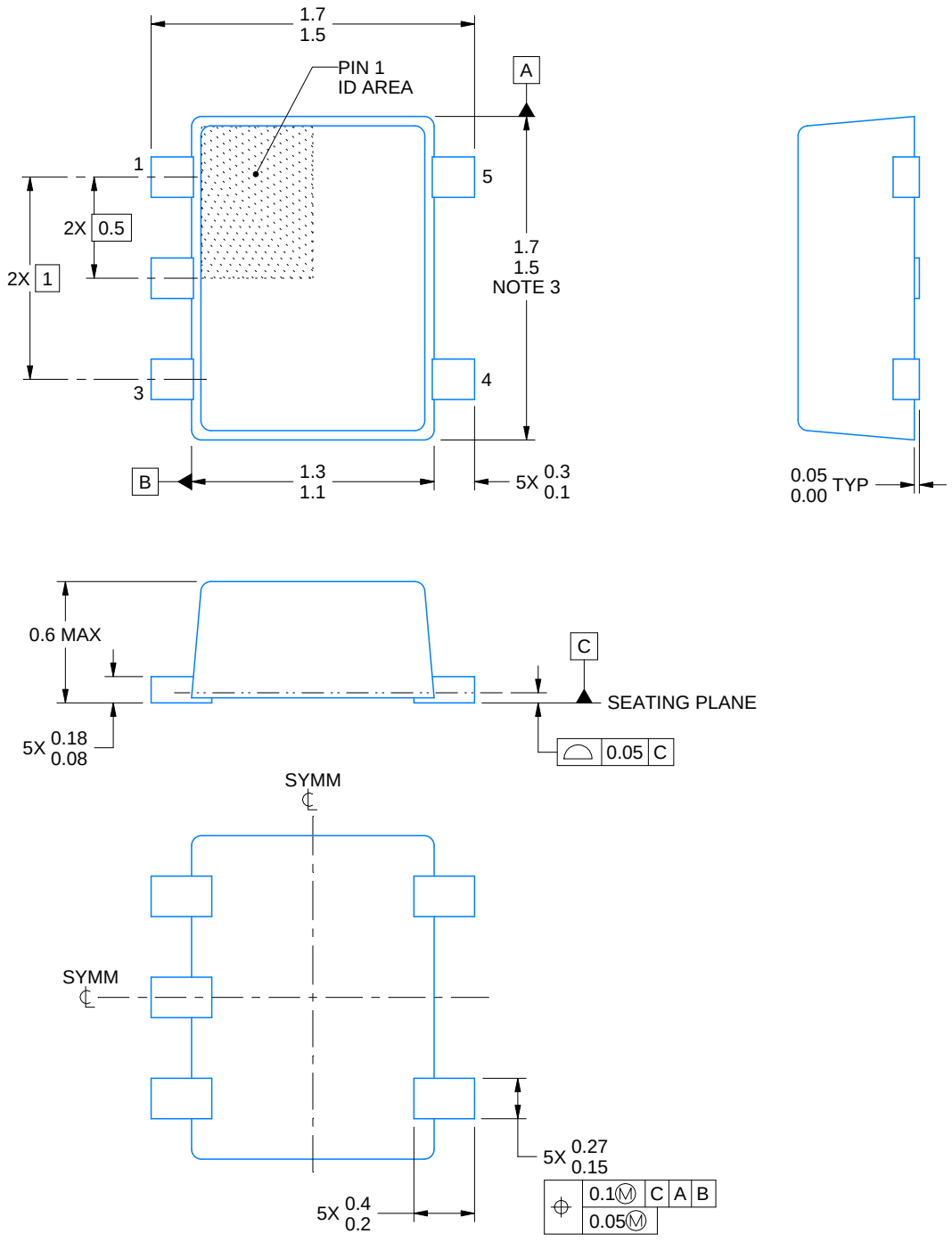
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DRL0005A

SOT - 0.6 mm max height

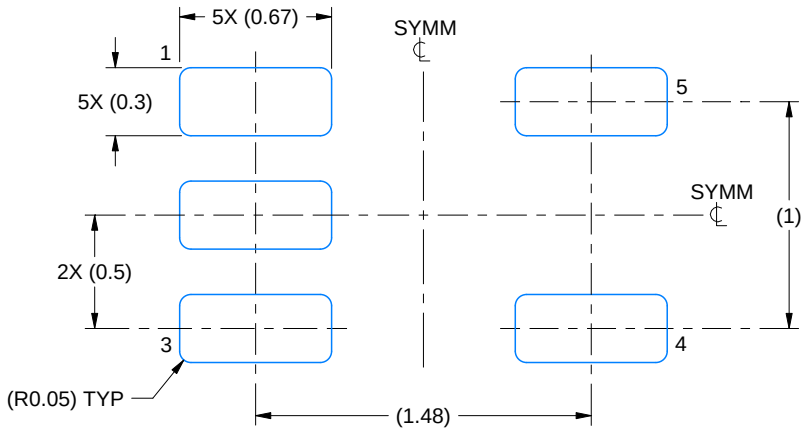
PLASTIC SMALL OUTLINE



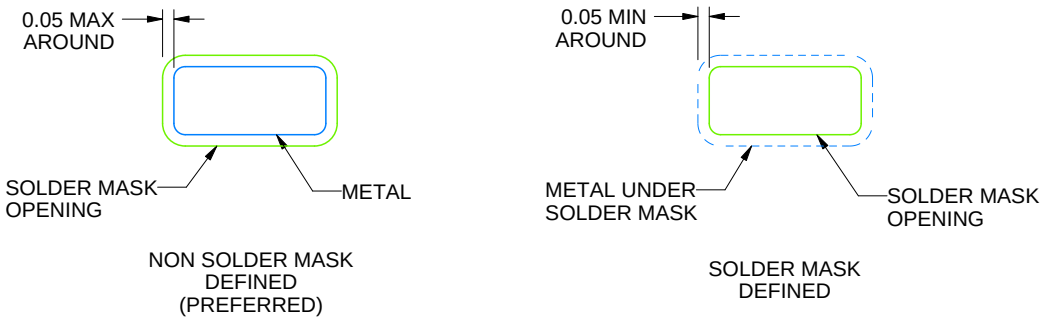
4220753/B 12/2020

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD-1



LAND PATTERN EXAMPLE
SCALE:30X

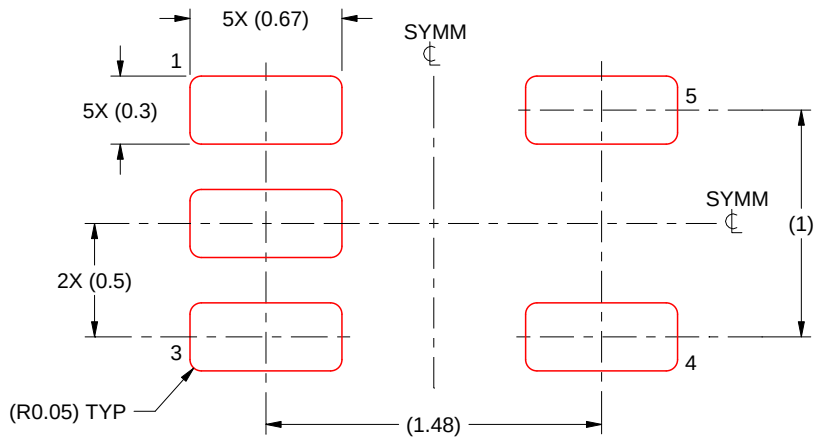


SOLDERMASK DETAILS

4220753/B 12/2020

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



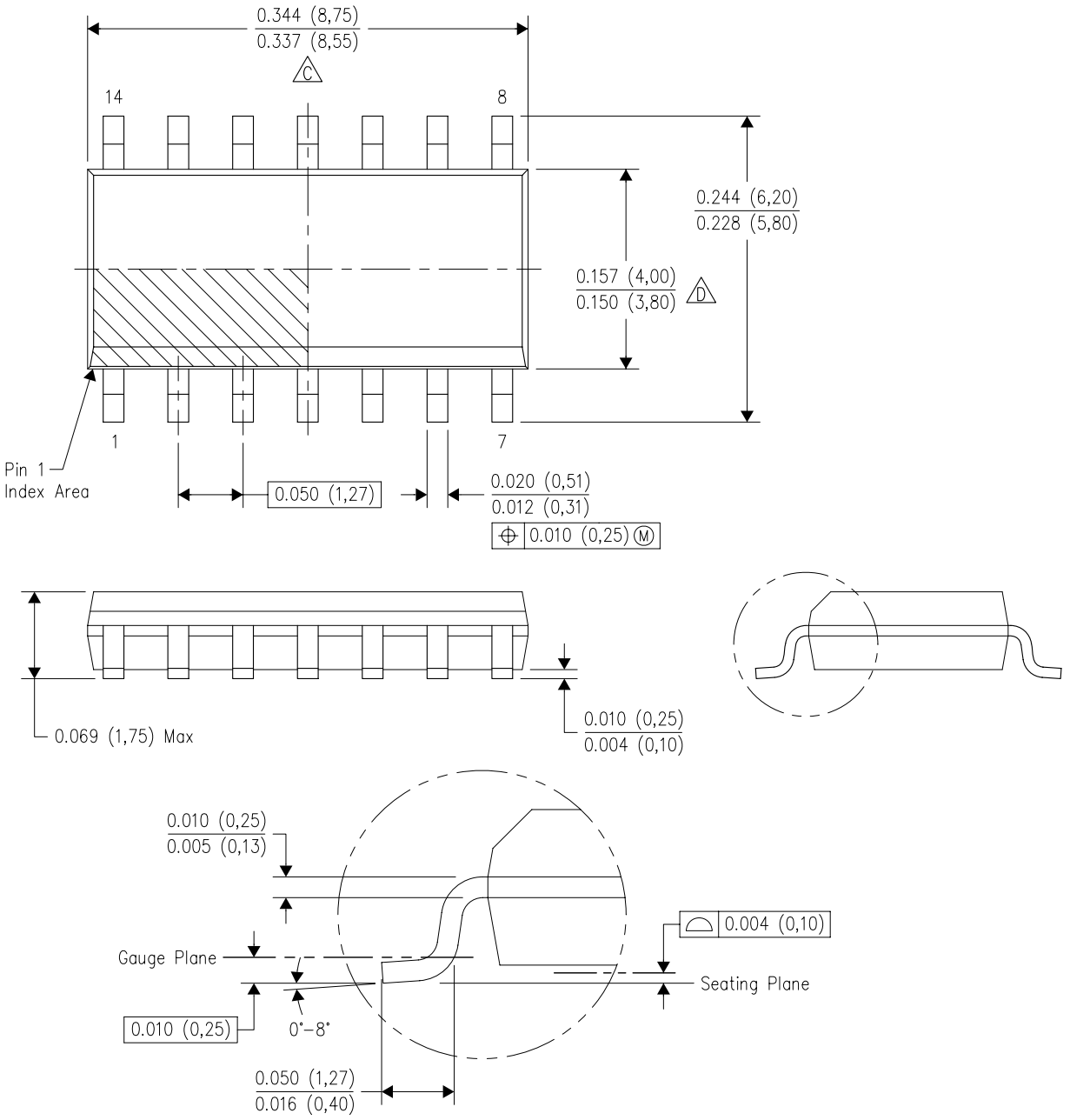
SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4220753/B 12/2020

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

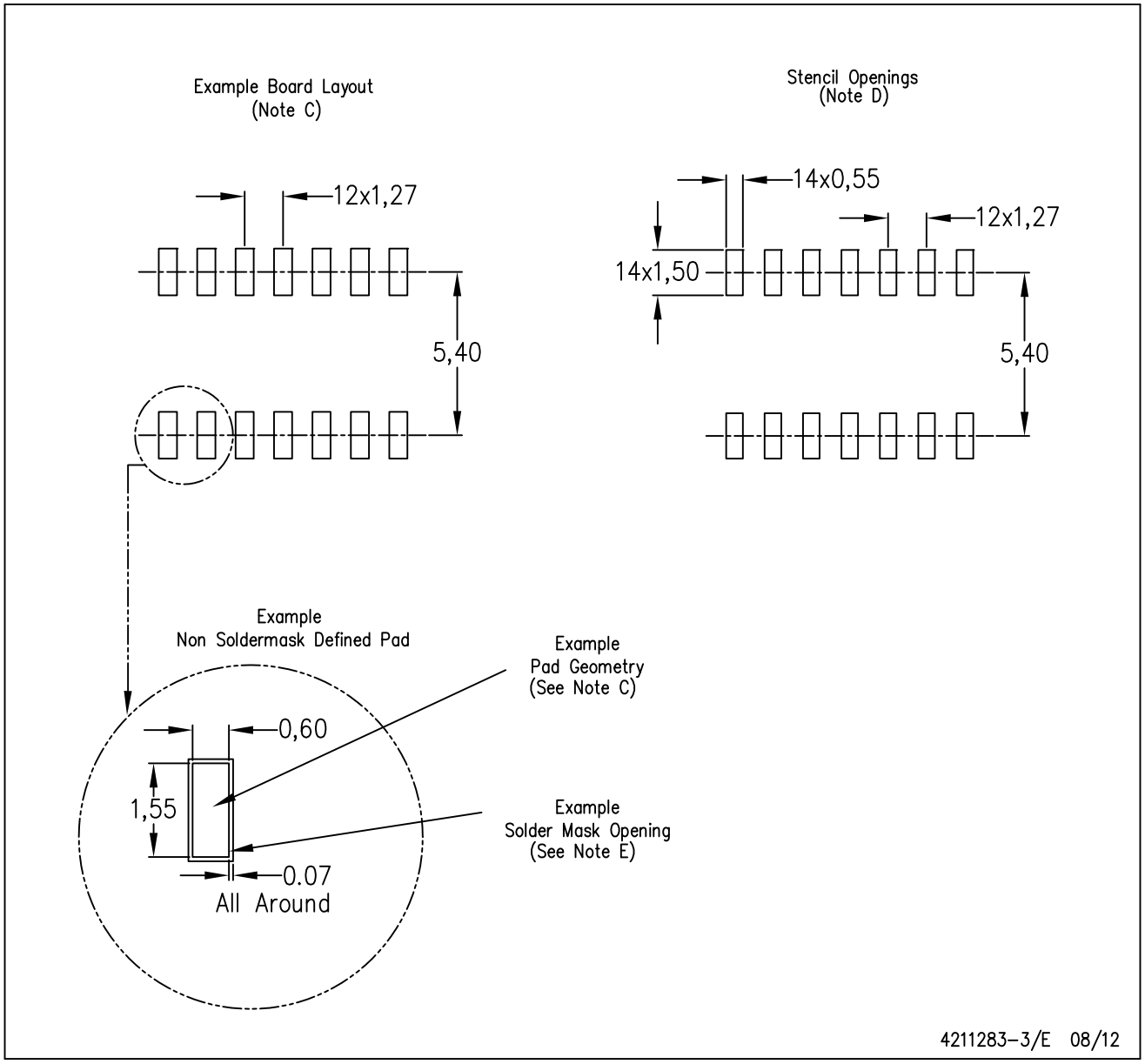
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

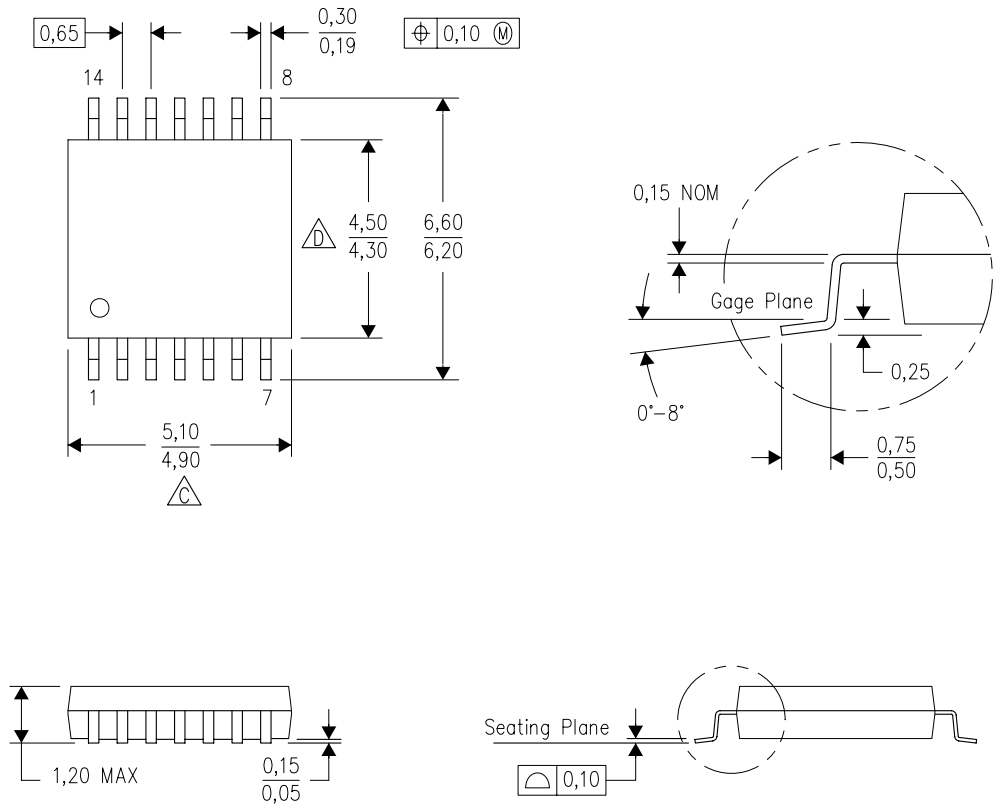
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

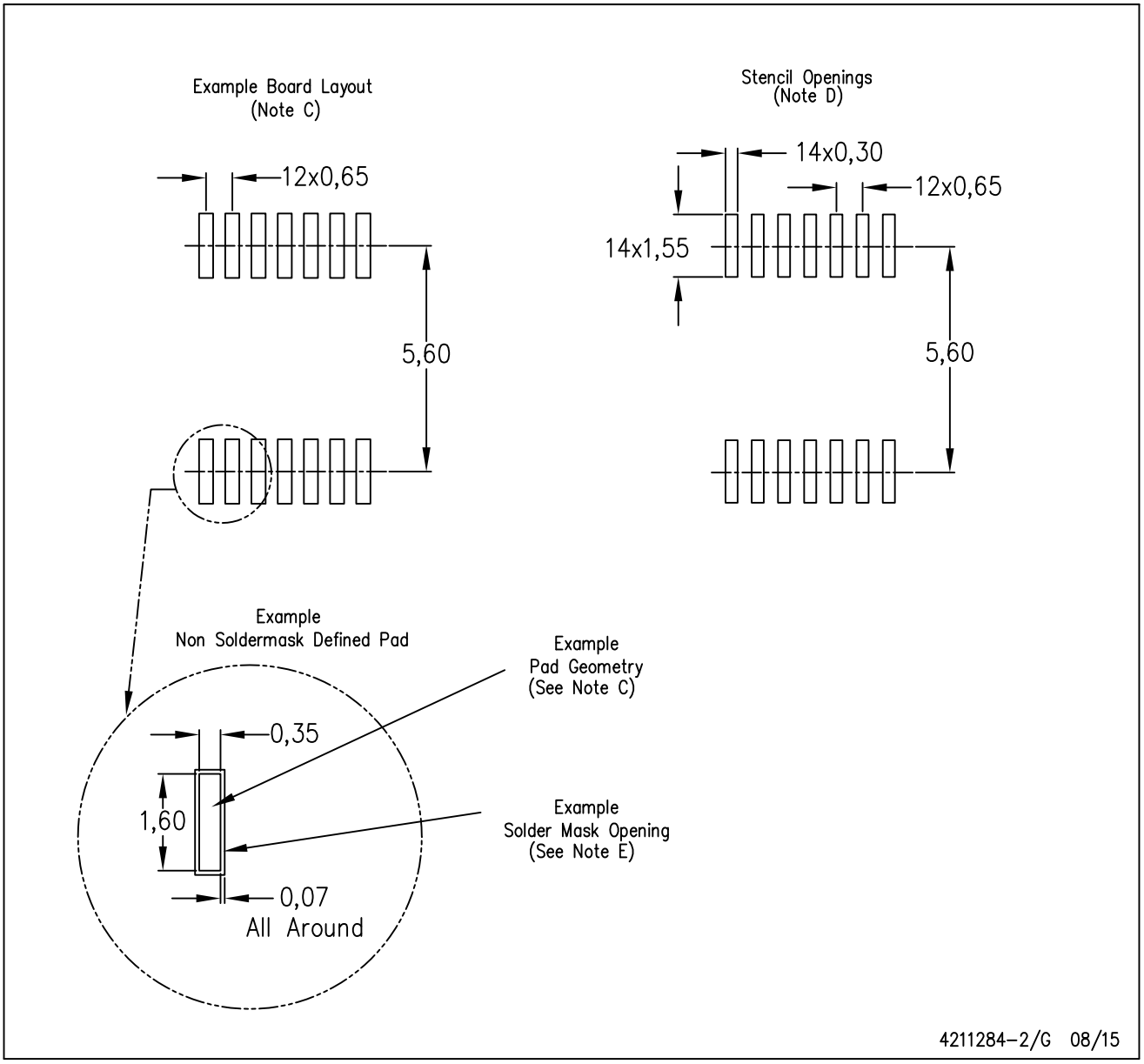
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



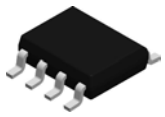
4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

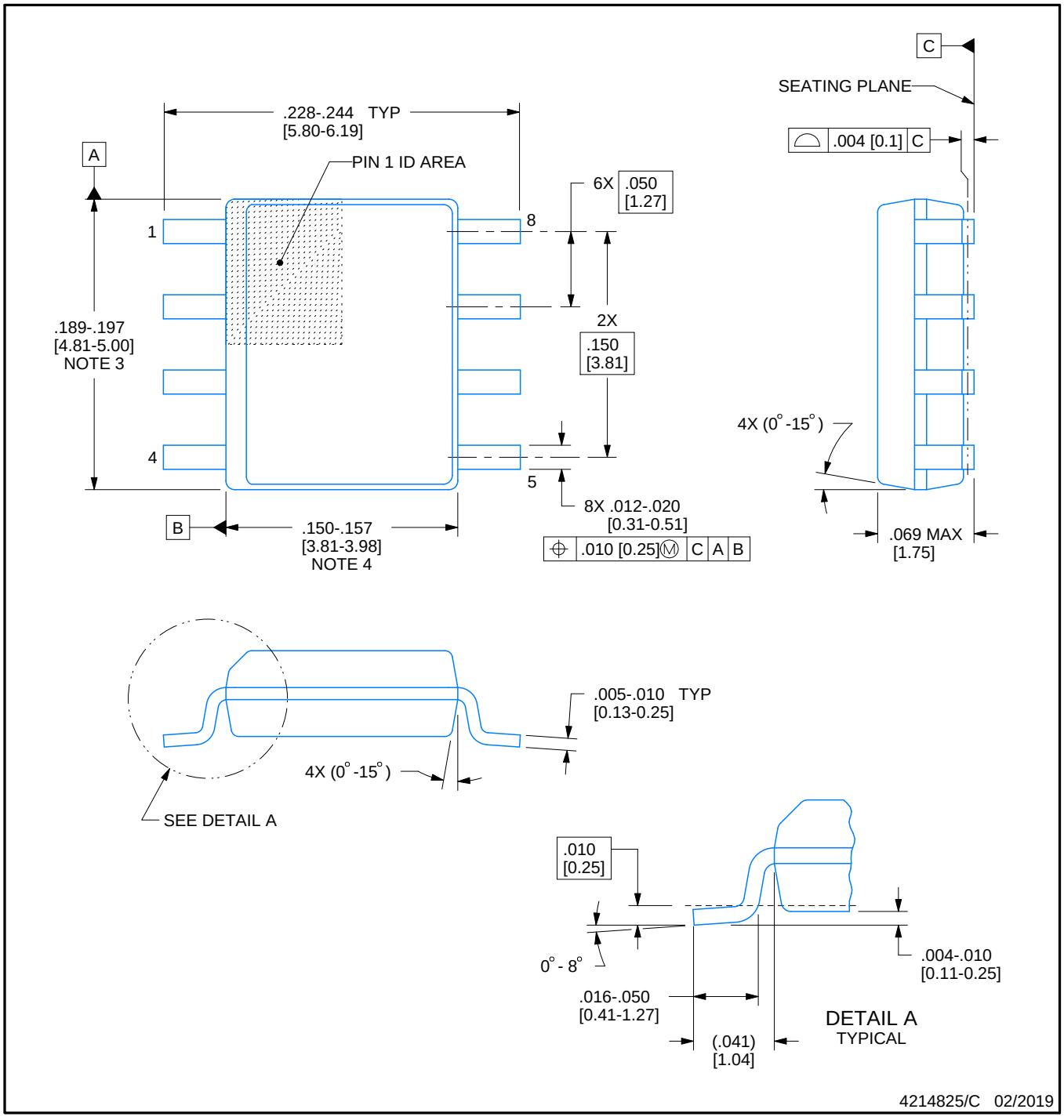


PACKAGE OUTLINE

D0008A

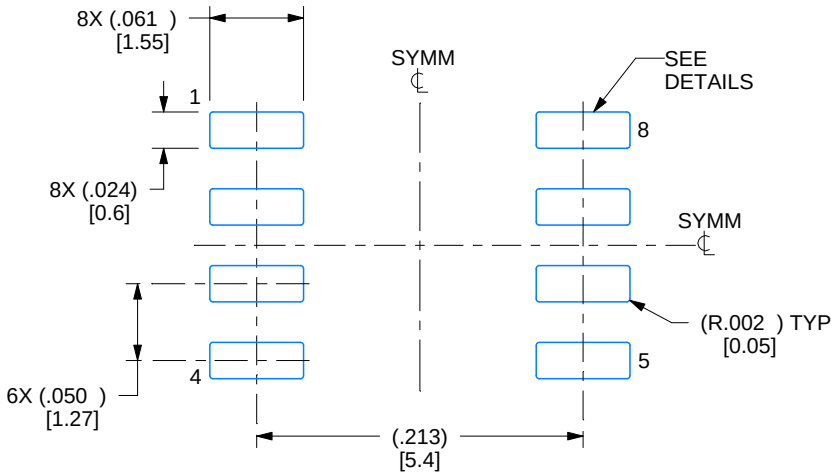
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

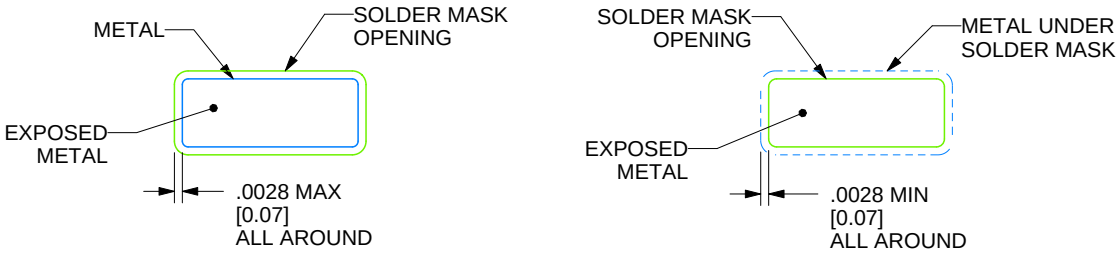


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

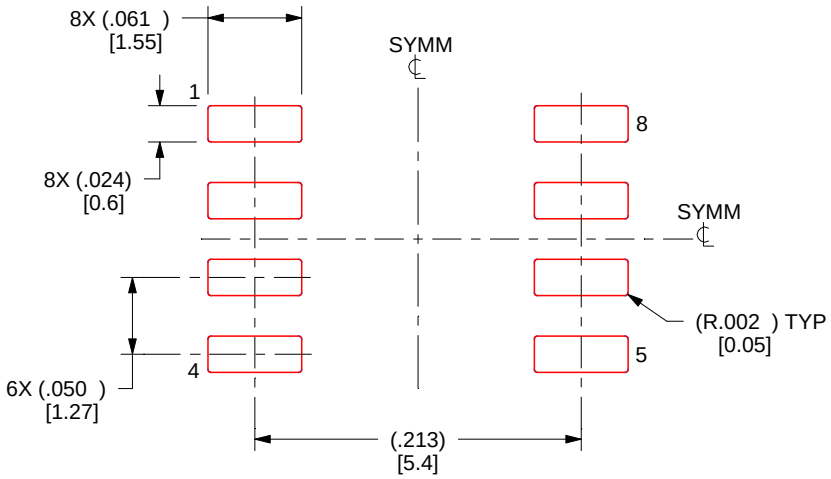
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



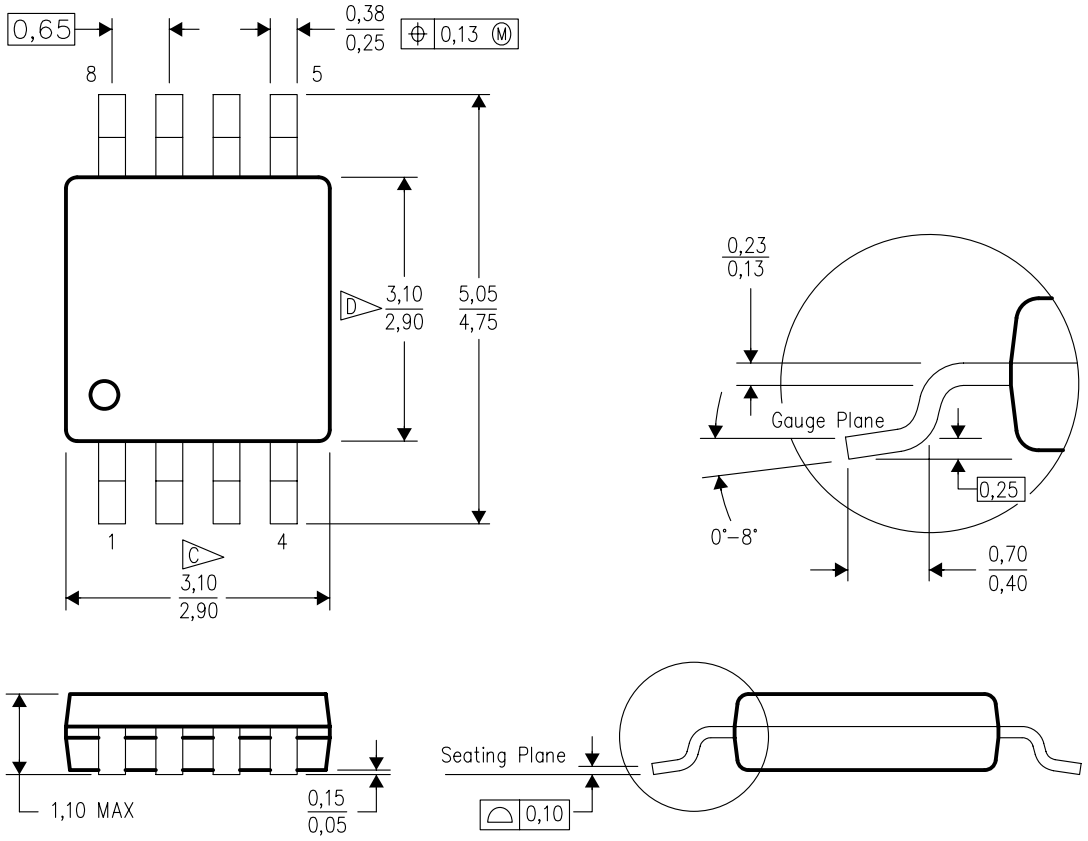
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

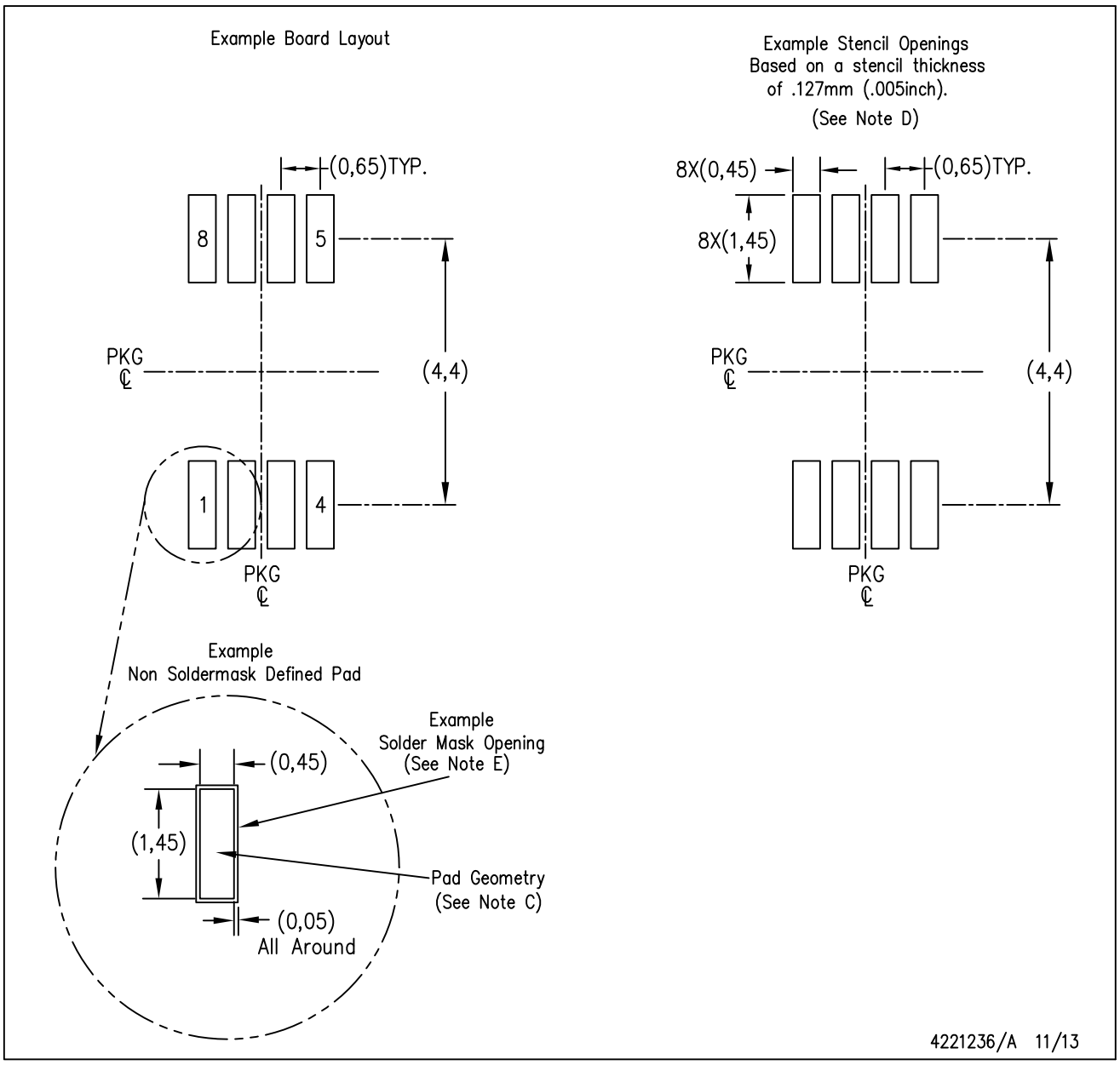
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

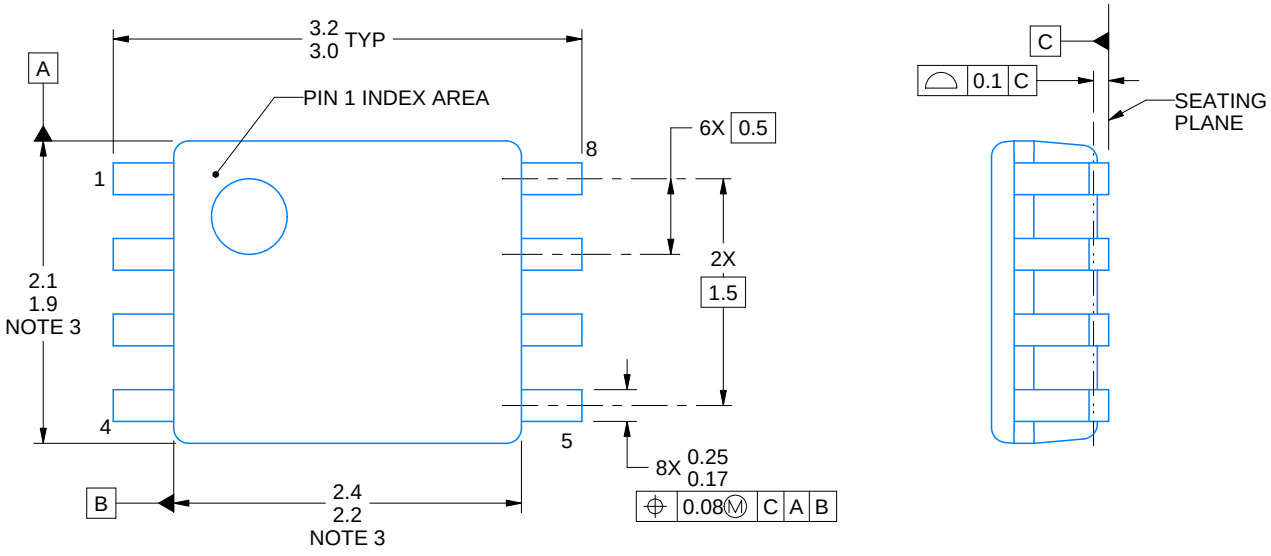
DCU0008A

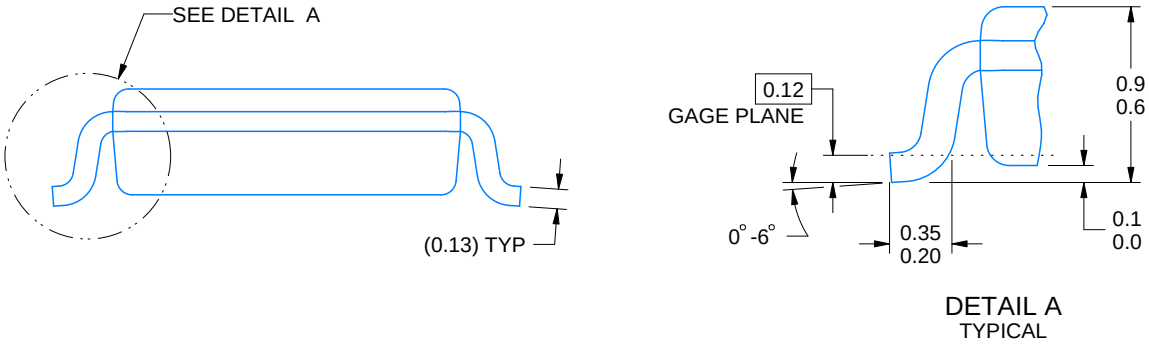


PACKAGE OUTLINE

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE

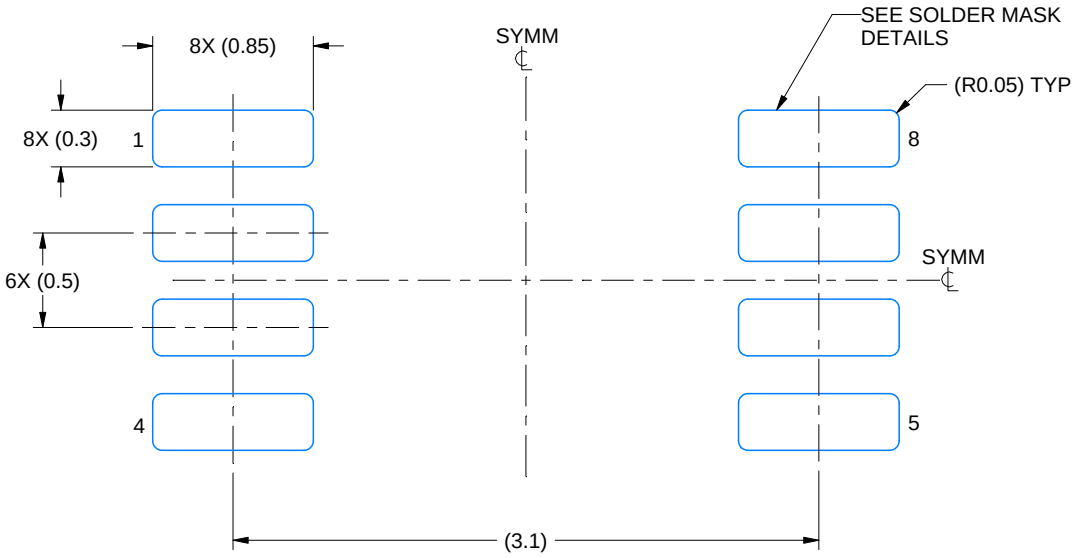




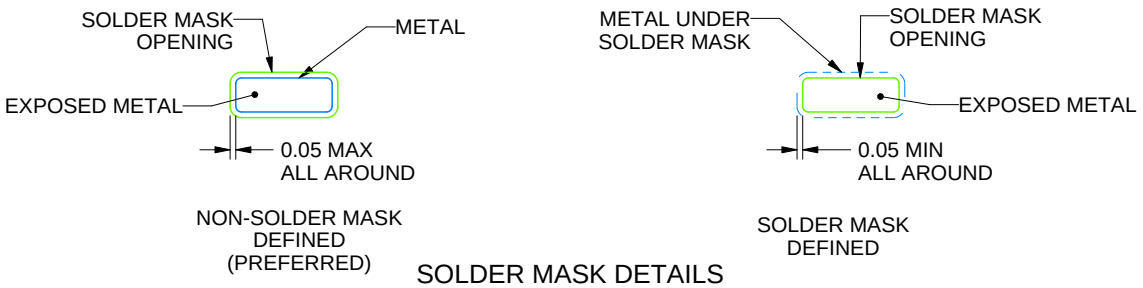
4225266/A 09/2014

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-187 variation CA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X

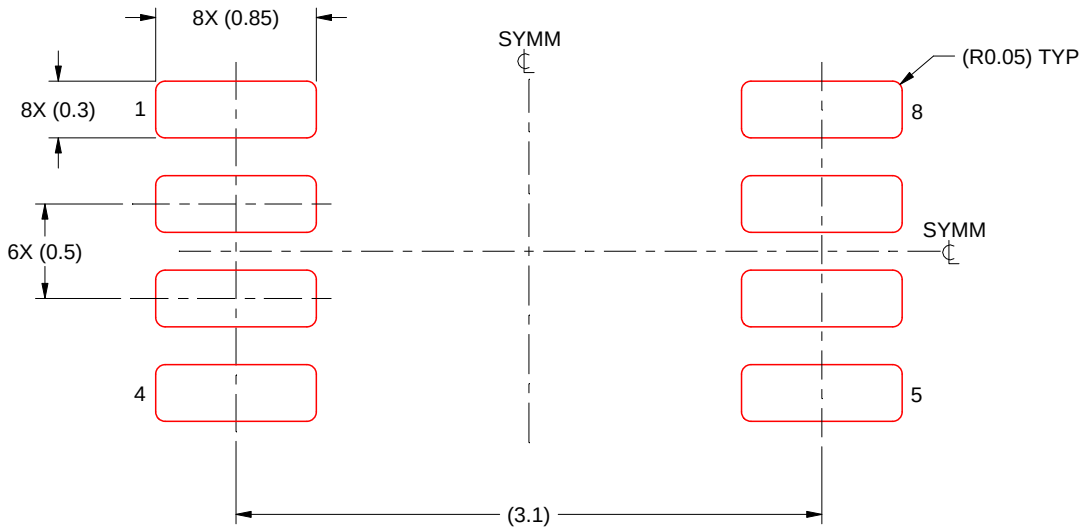


SOLDER MASK DETAILS

4225266/A 09/2014

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 25X

4225266/A 09/2014

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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