OPAx354-Q1 250MHz、レール・ツー・レールI/O、CMOSオペアンプ

1 特長

- 車載アプリケーションに対応
- 下記内容でAEC-Q100認定済み：
  - デバイス温度グレード: 動作時周囲温度範囲 –40°C～+125°C
  - デバイスHBM ESD分類レベル2
  - デバイスCDM ESD分類レベル
    - OPA354A-Q1およびOPA2354A-Q1: C6
    - OPA4354-Q1: C3
- ユニティ・ゲイン帯域幅: 250MHz
- 広い帯域幅: 100MHz GBW積
- 高いスルー・レート: 150V/µs
- 低ノイズ: 6.5nV/√Hz
- レール・ツー・レールI/O
- 高い出力電流: 100mA超
- 非常に優れたビデオ性能
  - 差動ゲイン誤差: 0.02%
  - 差動位相誤差: 0.09°
  - 0.1dBのゲイン・フラットネス(40MHz)
- 低い入力バイアス電流: 3pA
- 静止電流: 4.9mA
- サーマル・シャットダウン
- 電源電圧範囲: 2.5V～5.5V

2 アプリケーション

- ナビゲーションおよびラジオ・システム
- 死角検知
- 短距離から中距離のレーダー
- ビデオ処理
- 超音波
- 光ネットワーク、調節可能なレーザー
- フォトダイオード・トランスインピーダンス・アンプ
- アクティブ・フィルタ
- 高速積分器
- A/Dコンバータ(ADC)入力バッファ
- D/Aコンバータ(DAC)出力アンプ
- バーコード・スキャナ
- 通信

3 概要

OPAx354-Q1ファミリの高速、電圧帰還CMOSオペアンプは、広い帯域幅を必要とするビデオやその他のアプリケーション用に設計されています。いずれもユニティ・ゲイン安定で、大きな出力電流を駆動できます。差動ゲインは0.02%、差動位相は0.09°です。静止電流はチャネルごとにわずか4.9mAです。

OPAx354-Q1ファミリのオペアンプは、最低2.5V (±1.25V)、最高5.5V (±2.75V)のシングルまたはデュアル電源で動作するよう最適化されています。同相入力範囲は電源の範囲よりも拡大されています。出力スイングはレールから100mV以内で、広いダイナミック・レンジに対応しています。

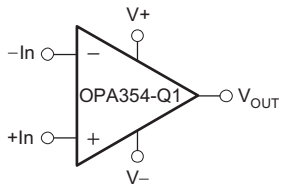
単一電源バージョン(OPA354A-Q1)は、小型のSOT–23-5 (DBV)パッケージで供給されます。デュアル電源バージョン(OPA2354A-Q1)は小型のVSSOP-8 (DGK)パッケージで供給され、クロストークが最小で干渉を受けないよう、完全に独立した回路が採用されています。クワッド電源バージョン(OPA4354-Q1)は、TSSOP-14 (PW)パッケージで供給されます。このデバイスは、-40℃～+125℃の車載用温度範囲で動作が規定されています。

製品情報(1)

型番	パッケージ(ピン)	本体サイズ(公称)
OPA354A-Q1	SOT-23 (5)	2.90mm×1.60mm
OPA2354A-Q1	VSSOP (8)	3.00mm×3.00mm
OPA4354-Q1	TSSOP (14)	5.00mm×4.40mm

(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

概略回路図



英語版のTI製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.comで閲覧でき、その内容が常に優先されます。TIでは翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision E (August 2016) から **Revision F** に変更 **Page**

- Deleted table note about input terminals and input signals from *Absolute Maximum Ratings* table ... 6

Revision D (July 2016) から **Revision E** に変更 **Page**

- Changed the gain-bandwidth product typical value from 10 MHz back to 100 MHz in the *Electrical Characteristics* table .. 8

Revision C (June 2016) から **Revision D** に変更 **Page**

- Changed the gain-bandwidth product typical value from 100 MHz to 10 MHz in the *Electrical Characteristics* table ... 8
- 追加「*ドキュメントの更新通知を受け取る方法*」および「*コミュニティ・リソース*」セクション ... 28

Revision B (December 2014) から **Revision C** に変更 **Page**

- 「*アプリケーション*」セクションに3つのアプリケーションを 追加 ... 1
- Updated *ESD Ratings* table to show CDM value for OPA354A-Q1 and OPA2354A-Q1 ... 6

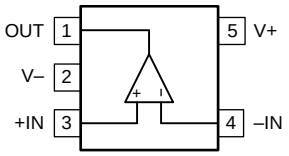
Revision A (August 2009) から **Revision B** に変更 **Page**

- 「*取り扱い定格*」表、「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクション 追加 ... 1
- データシートにOPA4354-Q1デバイスを 追加 ... 1

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5 Pin Configuration and Functions

OPA354A-Q1 DBV Package
5-Pin SOT-23
Top View

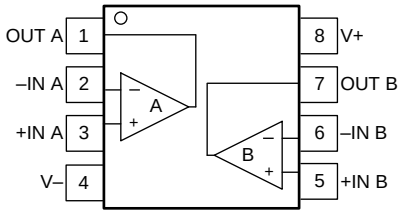


Pin Functions: OPA354A-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
+IN	3	I	Noninverting input
–IN	4	I	Inverting input
OUT	1	O	Output
V+	5	—	Positive (highest) supply
V–	2	—	Negative (lowest) supply

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OPA2354A-Q1 DGK Package
8-Pin VSSOP
Top View

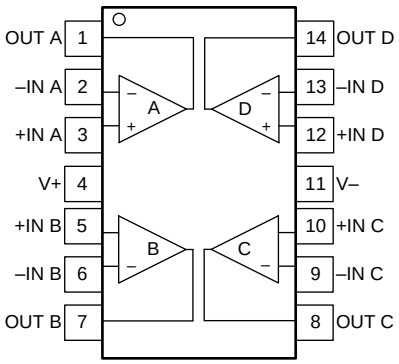


Pin Functions: OPA2354A-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
+IN A	3	I	Noninverting input, channel A
+IN B	5	I	Noninverting input, channel B
–IN A	2	I	Inverting input, channel A
–IN B	6	I	Inverting input, channel B
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
V+	5	—	Positive (highest) supply
V–	2	—	Negative (lowest) supply

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OPA4354-Q1 PW Package
14-Pin TSSOP
Top View



Pin Functions: OPA4354-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
+IN A	3	I	Noninverting input, channel A
+IN B	5	I	Noninverting input, channel B
+IN C	10	I	Noninverting input, channel C
+IN D	12	I	Noninverting input, channel D
–IN A	2	I	Inverting input, channel A
–IN B	6	I	Inverting input, channel B
–IN C	9	I	Inverting input, channel C
–IN D	13	I	Inverting input, channel D
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
OUT C	1	O	Output, channel C
OUT D	7	O	Output, channel D
V+	5	—	Positive (highest) supply
V–	2	—	Negative (lowest) supply

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

	MIN	MAX	UNIT
Supply voltage, V+ to V–, V_S		7.5	V
Signal input terminals voltage, V_{IN}	(V–) – 0.5	(V+) + 0.5	V
Output short-circuit duration (2)	Continuous		
Operating temperature, T_A	–55	150	°C
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Short circuit to ground, one amplifier per package

6.2 ESD Ratings

			VALUE	UNIT
OPA354A-Q1 IN DBV (SOT-23) PACKAGE AND OPA2354A-Q1 IN DGK (VSSOP) PACKAGE				
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 (1)	±2000	V
		Charged device model (CDM), per AEC Q100-011	±1000	
OPA4354-Q1 IN PW (TSSOP) PACKAGE				
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 (1)	±2000	V
		Charged device model (CDM), per AEC Q100-011	±250	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_S	Supply voltage, V– to V+	2.5	5.5	V
T_A	Operating free-air temperature	–40	125	°C

6.4 Thermal Information: OPA354A-Q1

THERMAL METRIC (1)		OPA354A-Q1 DBV (SOT-23) 5 PINS	OPA2354A-Q1 DGK (VSSOP) 8 PINS	OPA4354-Q1 PW (TSSOP) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	216.3	175.9	92.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	84.3	67.8	27.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.1	97.1	33.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.8	9.3	1.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	42.3	95.5	33.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 Thermal Information: OPA2354A-Q1

THERMAL METRIC(1)		OPA2354A-Q1 DGK (VSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	175.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	67.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	97.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	9.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	95.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.6 Thermal Information: OPA4354A-Q1

THERMAL METRIC(1)		OPA4354-Q1 PW (TSSOP) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	92.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	27.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	33.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	33.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.7 Electrical Characteristics

V_S = 2.5 V to 5.5 V, R_F (feedback resistor) = 0 Ω, R_L (load resistor) = 1 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OS}	Input offset voltage	V_S = 5 V V_{CM} = (V–) + 0.8 V	T_A = 25°C		±2	±8	mV
			T_A = Full range			±10	
ΔV_{OS} / ΔT	Offset voltage drift over temperature	T_A = Full range			±4		µV/°C
PSRR	Offset voltage drift vs power supply	V_S = 2.7 V to 5.5 V, V_{CM} = V_S / 2 – 0.15 V	T_A = 25°C		±200	±800	µV/V
			T_A = Full range			±900	
I_B	Input bias current	T_A = 25°C			3	±50	pA
I_{OS}	Input offset current	T_A = 25°C			±1	±50	pA
V_n	Input voltage noise density	f = 1 MHz, T_A = 25°C			6.5		nV/√Hz
I_n	Input current noise density	f = 1 MHz, T_A = 25°C			50		fA/√Hz
V_{CM}	Input common-mode voltage range	T_A = 25°C		(V–) – 0.1		(V+) + 0.1	V
CMRR	Input common-mode rejection ratio	V_S = 5.5 V –0.1 V < V_{CM} < 3.5 V	T_A = 25°C	66	80		dB
			T_A = Full range	64			
		V_S = 5.5 V –0.1 V < V_{CM} < 5.6 V	T_A = 25°C	56	68		
			T_A = Full range	55			
Z_{ID}	Differential input impedance	T_A = 25°C			10^{13} || 2		Ω || pF
Z_{ICM}	Common-mode input impedance	T_A = 25°C			10^{13} || 2		Ω || pF
A_{OL}	Open-loop gain	V_S = 5 V, 0.3 V < V_O < 4.7 V T_A = 25°C		94	110		dB
		V_S = 5 V, 0.4 V < V_O < 4.6 V T_A = Full range		90			
$f_{–3dB}$	Small-signal bandwidth	G = 1, V_O = 100 mVp-p, R_F = 25 Ω, T_A = 25°C			250		MHz
		G = 2, V_O = 100 mVp-p, T_A = 25°C			90		
GBW	Gain-bandwidth product	G = 10 T_A = 25°C			100		MHz
$f_{0.1dB}$	Bandwidth for 0.1-dB gain flatness	G = 2, V_O = 100 mVp-p, T_A = 25°C			40		MHz
SR	Slew rate	V_S = 5 V, G = 1, 4-V step, T_A = 25°C			150		V/µs
		V_S = 5 V, G = 1, 2-V step			130		
		V_S = 3 V, G = 1, 2-V step			110		
t_{rf}	Rise-and-fall time	G = 1, V_O = 200 mVp-p, 10% to 90%, T_A = 25°C			2		ns
		G = 1, V_O = 2 Vp-p, 10% to 90%, T_A = 25°C			11		
t_{settle}	Settling time	V_S = 5 V, G = +1, 2-V output step, T_A = 25°C	0.1%		30		ns
			0.01%		60		
	Overload recovery time	V_{IN} × Gain = V_S T_A = 25°C			5		ns
	Second-order harmonic distortion	G = 1, f = 1 MHz, V_O = 2 Vp-p, R_L = 200 Ω, V_{CM} = 1.5 V T_A = 25°C			–75		dBc
	Third-order harmonic distortion	G = 1, f = 1 MHz, V_O = 2 Vp-p R_L = 200 Ω, V_{CM} = 1.5 V T_A = 25°C			–83		dBc
	Differential gain error	NTSC, R_L = 150 Ω, T_A = 25°C			0.02%		
	Differential phase error	NTSC, R_L = 150 Ω, T_A = 25°C			0.09		°

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Electrical Characteristics (continued)

V_S = 2.5 V to 5.5 V, R_F (feedback resistor) = 0 Ω, R_L (load resistor) = 1 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
	Channel-to-channel crosstalk (OPA2354A-Q1) (OPA4354-Q1)	f = 5 MHz, T_A = 25°C			–100		dB
	Voltage output swing from rail	V_S = 5 V, R_L = 1 kΩ, A_{OL} > 94 dB T_A = 25°C			0.1	0.3	V
		V_S = 5 V, R_L = 1 kΩ A_{OL} > 90 dB, T_A = Full range				0.4	
I_O	Output current(1) (2)	V_S = 5 V		100			mA
		V_S = 3 V			50		
	Closed-loop output impedance	f < 100 kHz			0.05		Ω
R_O	Open-loop output resistance				35		Ω
I_Q	Quiescent current (per amplifier)	V_S = 5 V, I_O = 0, enabled	T_A = 25°C		4.9	6	mA
			T_A = Full range			7.5	
	Thermal shutdown junction temperature	Shutdown			160		°C
		Reset from shutdown			140		

(1) See typical characteristic graph *Output Voltage Swing vs Output Current* (図 20).
(2) Not production tested

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6.8 Typical Characteristics

T_A = 25°C, V_S = 5 V, R_F = 0 Ω, R_L = 1 kΩ connected to V_S / 2 (unless otherwise noted)

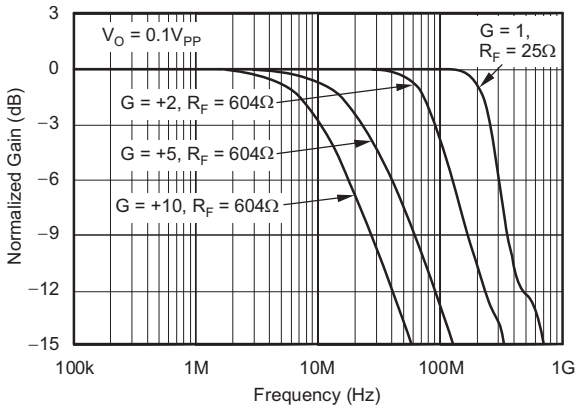


図 1. Noninverting Small-Signal Frequency Response

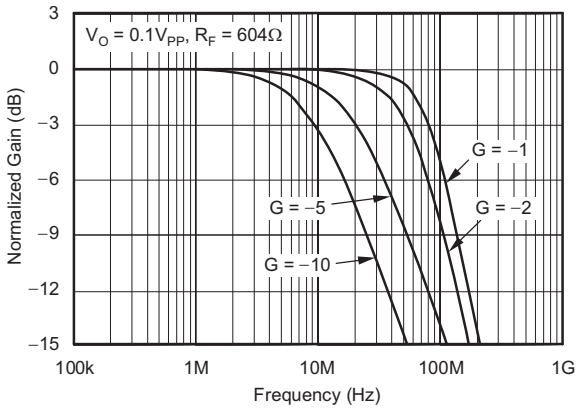


図 2. Inverting Small-Signal Frequency Response

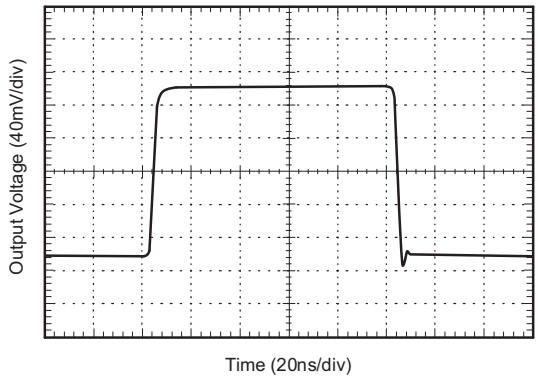


図 3. Noninverting Small-Signal Step Response

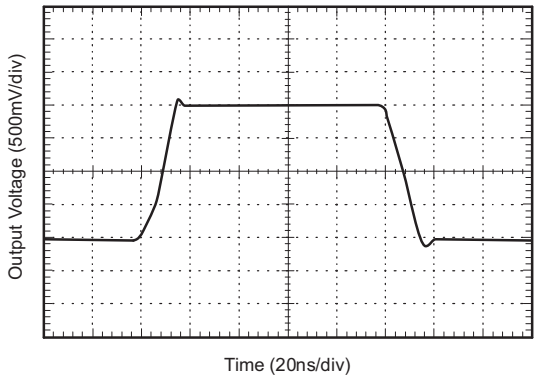


図 4. Noninverting Large-Signal Step Response

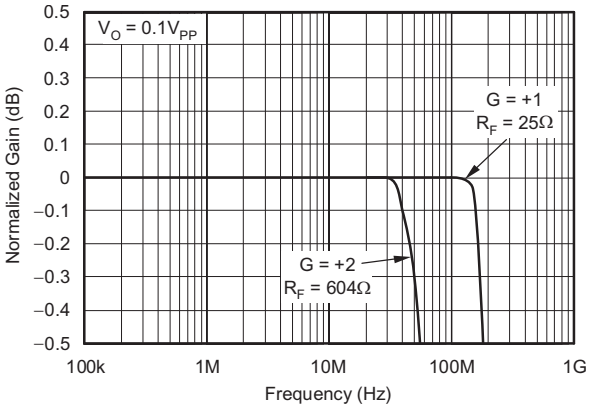


図 5. 0.1-dB Gain Flatness

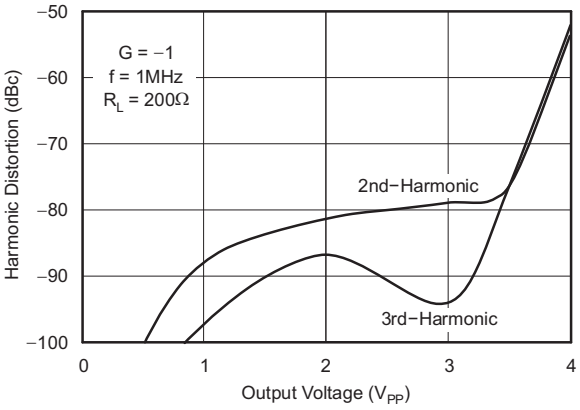


図 6. Harmonic Distortion vs Output Voltage

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Typical Characteristics (continued)

T_A = 25°C, V_S = 5 V, R_F = 0 Ω, R_L = 1 kΩ connected to V_S / 2 (unless otherwise noted)

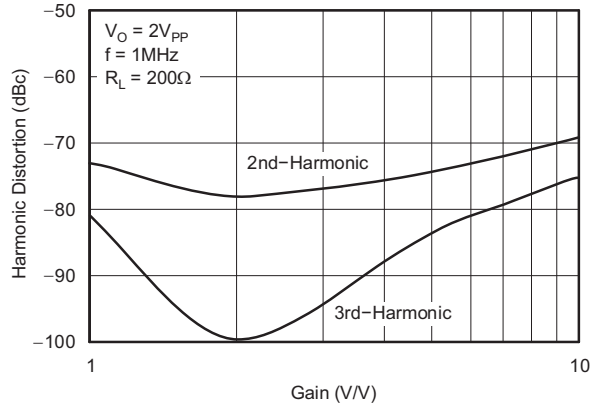


図 7. Harmonic Distortion vs Noninverting Gain

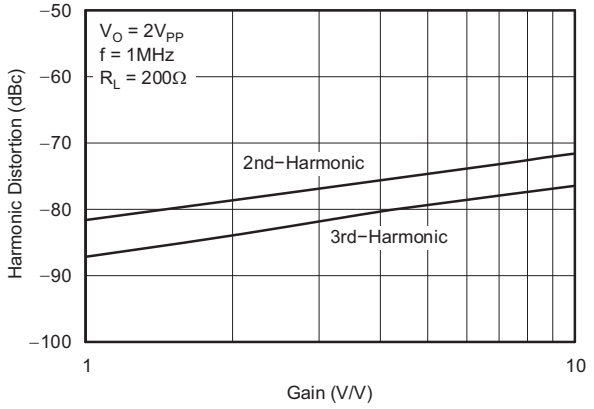


図 8. Harmonic Distortion vs Inverting Gain

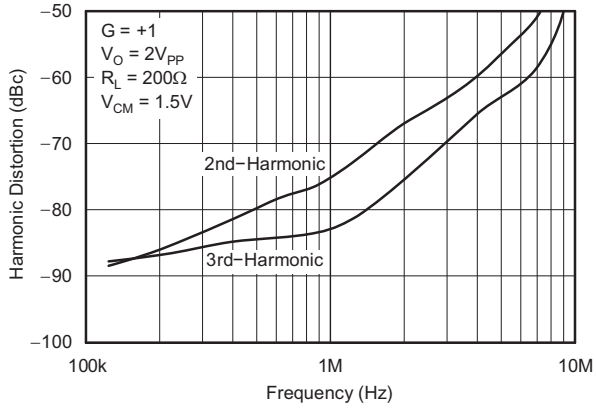


図 9. Harmonic Distortion vs Frequency

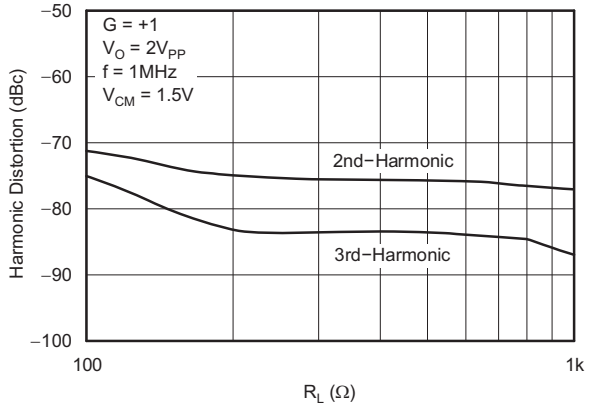


図 10. Harmonic Distortion vs Load Resistance

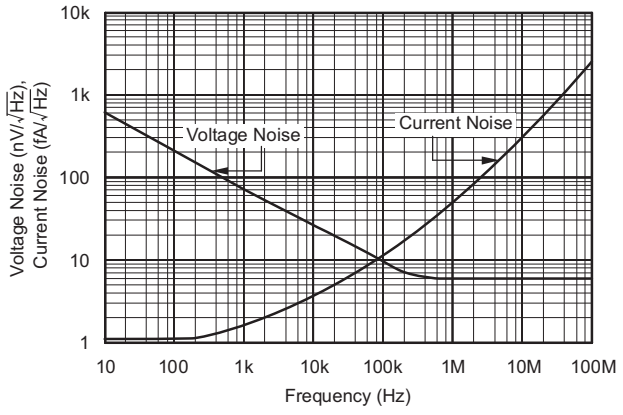


図 11. Input Voltage and Current Noise Spectral Density vs Frequency

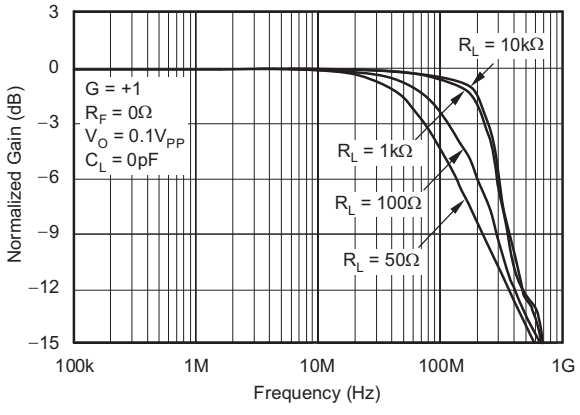


図 12. Frequency Response for Various R_L Values

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Typical Characteristics (continued)

T_A = 25°C, V_S = 5 V, R_F = 0 Ω, R_L = 1 kΩ connected to V_S / 2 (unless otherwise noted)

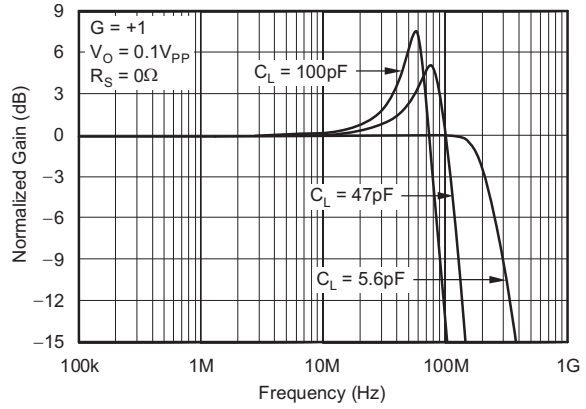


図 13. Frequency Response for Various C_L Values

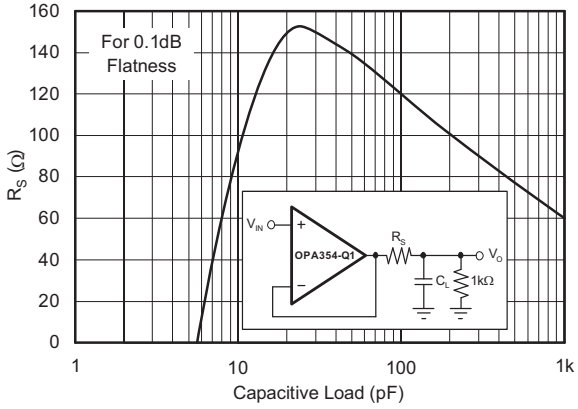


図 14. Recommended R_S vs Capacitive Load

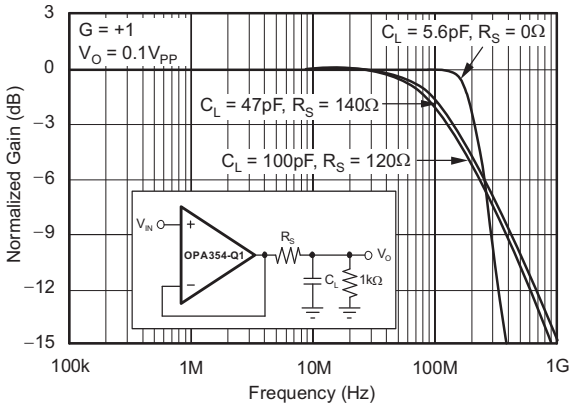


図 15. Frequency Response vs Capacitive Load

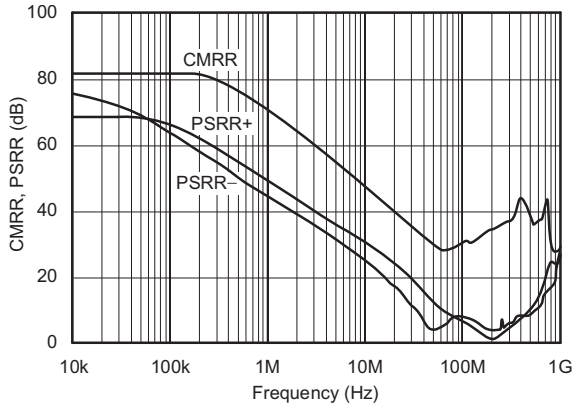


図 16. Common-Mode Rejection Ratio and Power-Supply Rejection Ratio vs Frequency

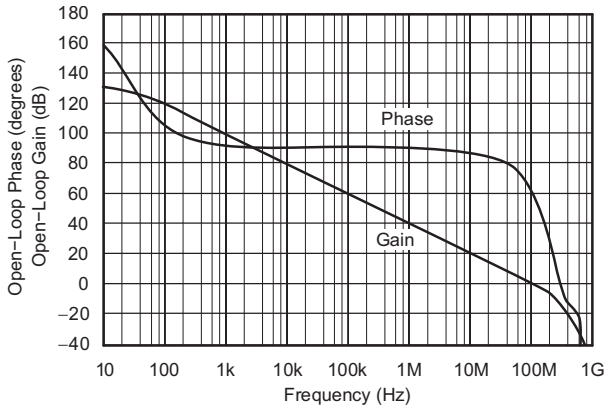


図 17. Open-Loop Gain and Phase

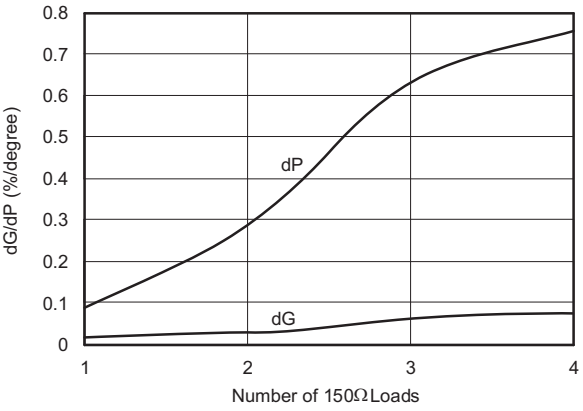


図 18. Composite Video Differential Gain and Phase

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Typical Characteristics (continued)

T_A = 25°C, V_S = 5 V, R_F = 0 Ω, R_L = 1 kΩ connected to V_S / 2 (unless otherwise noted)

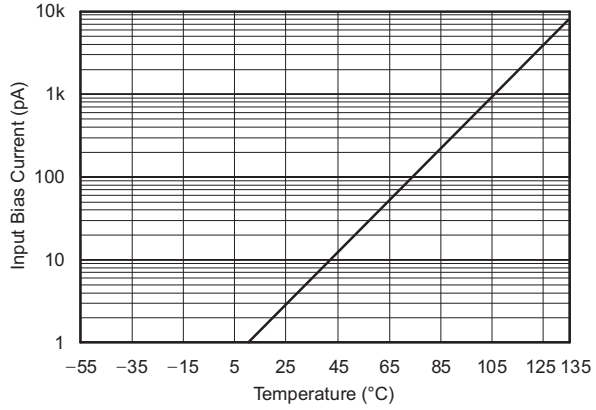


図 19. Input Bias Current vs Temperature

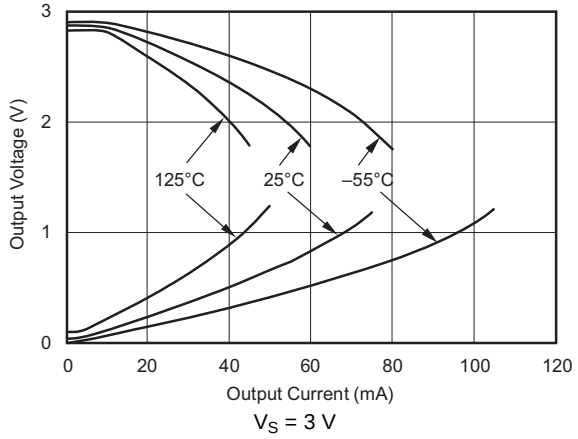


図 20. Output Voltage Swing vs Output Current

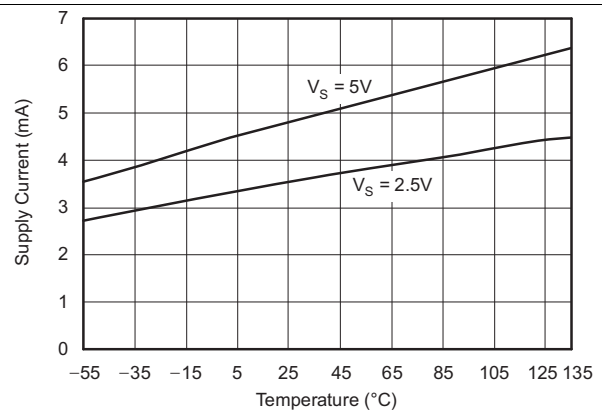


図 21. Supply Current vs Temperature

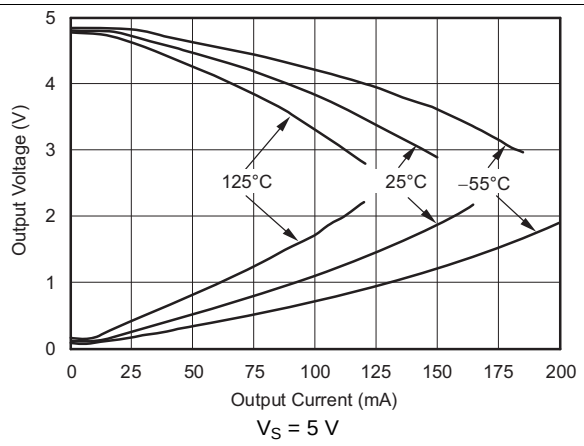


図 22. Output Voltage Swing vs Output Current

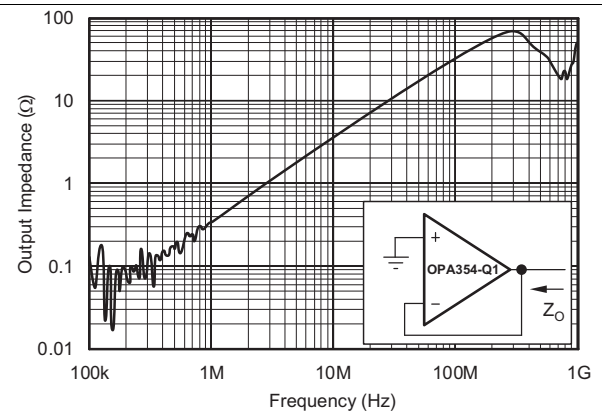


図 23. Closed-Loop Output Impedance vs Frequency

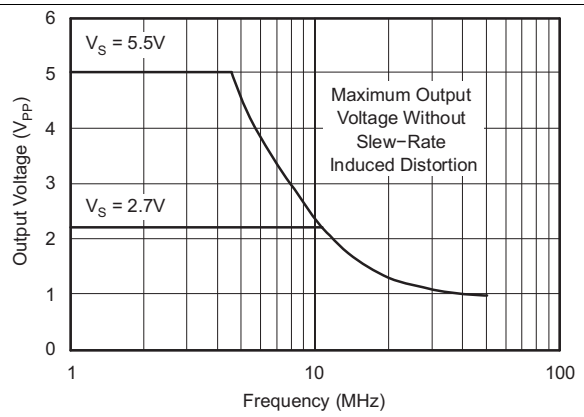


図 24. Maximum Output Voltage vs Frequency

Typical Characteristics (continued)

T_A = 25°C, V_S = 5 V, R_F = 0 Ω, R_L = 1 kΩ connected to V_S / 2 (unless otherwise noted)

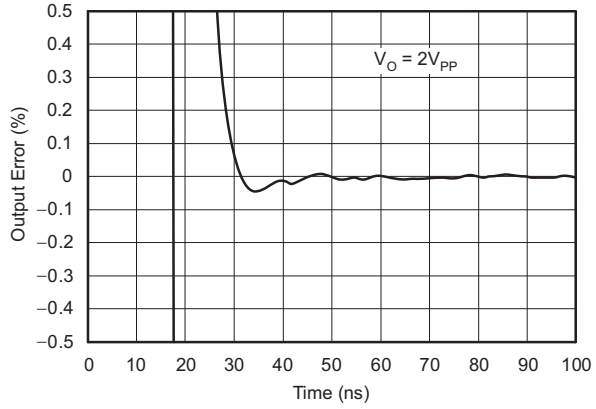


図 25. Output Settling Time to 0.1%

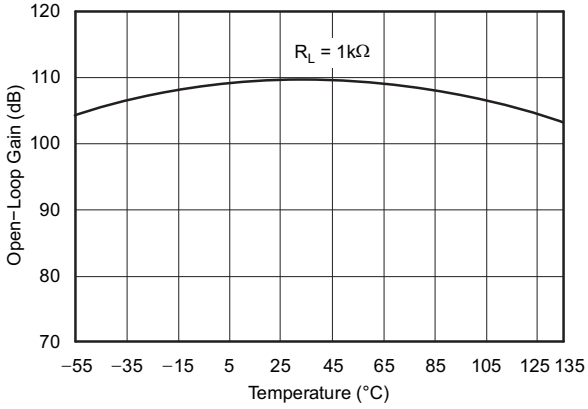


図 26. Open-Loop Gain vs Temperature

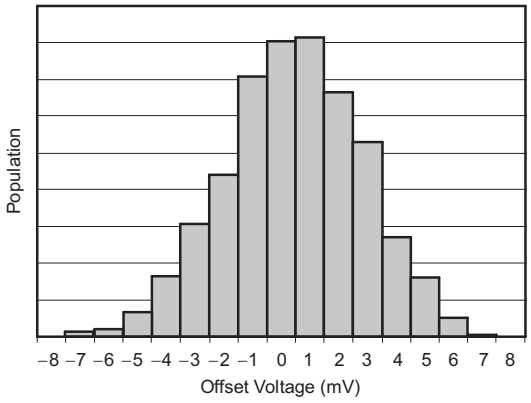


図 27. Offset Voltage Production Distribution

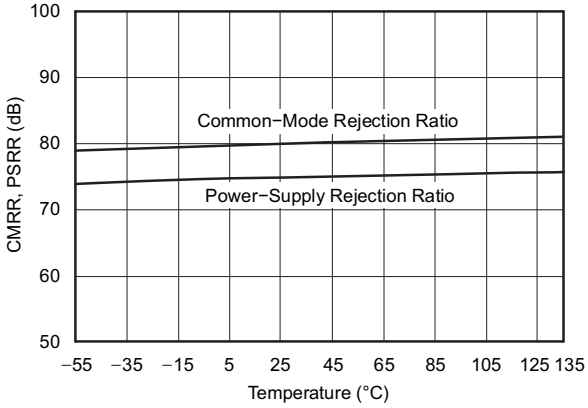


図 28. Common-Mode Rejection Ratio and Power-Supply Rejection Ratio vs Temperature

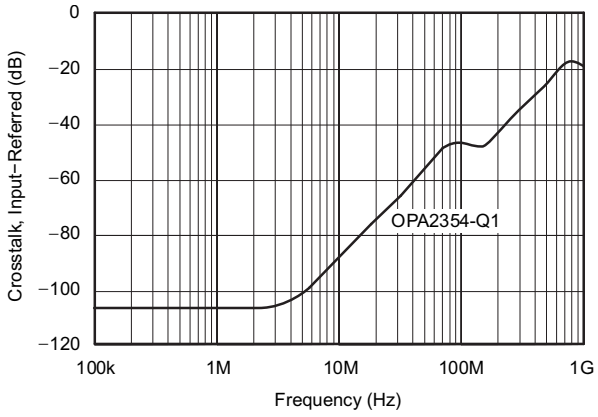


図 29. Channel-to-Channel Crosstalk (OPAx354-Q1)

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7 Detailed Description

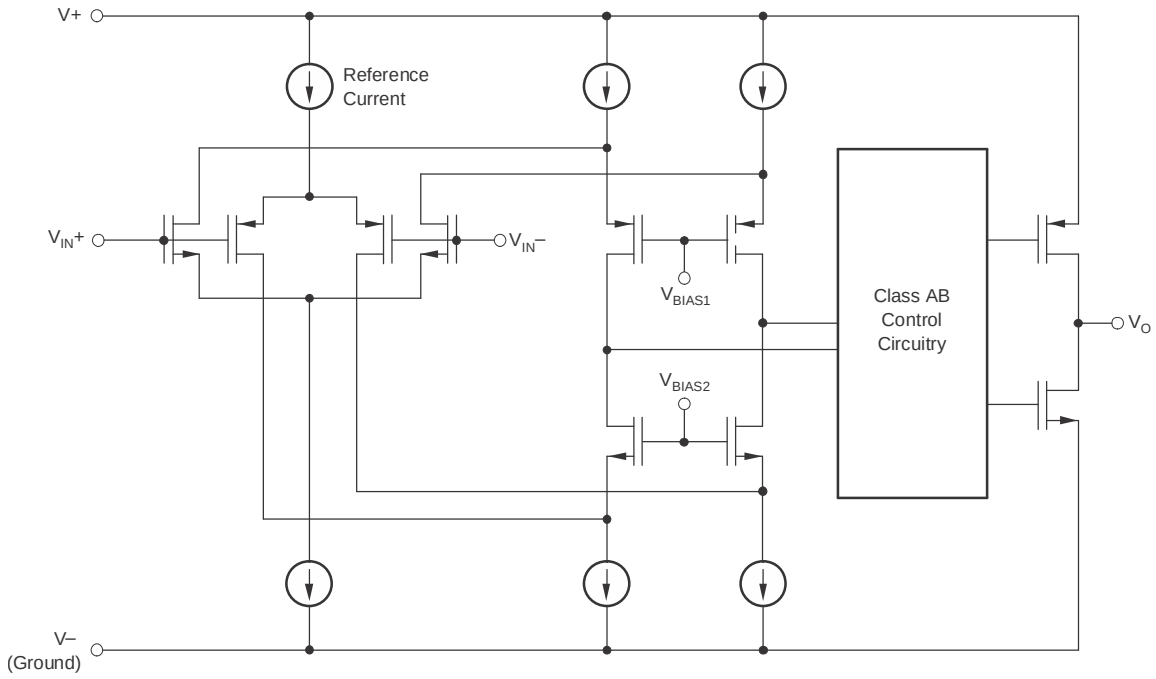
7.1 Overview

The OPAx354-Q1 operational amplifiers are high-speed,150-V/μs, amplifiers making them excellent choices for transimpedance applications. The devices are unity-gain stable and can operate on a single-supply voltage (2.5 V to 5.5 V), or a split-supply voltage (±1.25 V to ±2.75 V), making them highly versatile and easy to use. The OPAx354A-Q1 amplifiers are specified from 2.5 V to 5.5 V and over the automotive temperature range of –40°C to +125°C.

表 1. OPAx354-Q1 Related Products

FEATURES	PRODUCT
Shutdown Version of OPA354 Family	OPAx357
200-MHz GBW, Rail-to-Rail Output, CMOS, Shutdown	OPAx355
200-MHz GBW, Rail-to-Rail Output, CMOS	OPAx356
38-MHz GBW, Rail-to-Rail Input/Output, CMOS	OPAx350/3
75-MHz BW, G = 2, Rail-to-Rail Output	OPAx631
150-MHz BW, G = 2, Rail-to-Rail Output	OPAx634
100-MHz BW, Differential Input/Output, 3.3-V Supply	THS412x

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Operating Voltage

The specifications of the OPAx354-Q1 family of devices apply over a power-supply range of 2.5 V to 5.5 V (±1.25 V to ±2.75 V). Supply voltages higher than 7.5 V (absolute maximum) can permanently damage the amplifier.

The *Typical Characteristics* section of this data sheet shows the parameters that vary over supply voltage or temperature.

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Feature Description (continued)

7.3.2 Rail-to-Rail Input

The specified input common-mode voltage range of the OPAx354-Q1 family of devices extends 100 mV beyond the supply rails. A complementary input stage (an N-channel input differential pair in parallel with a P-channel differential pair) achieves this extension. The N-channel pair is active for input voltages close to the positive rail, typically (V+) – 1.2 V to 100 mV above the positive supply, while the P-channel pair is on for inputs from 100 mV below the negative supply to approximately (V+) – 1.2 V. A small transition region exists, typically (V+) – 1.5 V to (V+) – 0.9 V, in which both pairs are on. This 600-mV transition region can vary ±500 mV with process variation. As a result, the transition region (both input stages on) range from (V+) – 2 V to (V+) – 1.5 V on the low end, up to (V+) – 0.9 V to (V+) – 0.4 V on the high end.

A double-folded cascode adds the signal from the two input pairs and presents a differential signal to the class-AB output stage.

7.3.3 Rail-to-Rail Output

The device uses a class-AB output stage with common-source transistors to achieve rail-to-rail output. For high-impedance loads (> 200 Ω), the output voltage swing is typically 100 mV from the supply rails. With 10-Ω loads, a user can achieve a useful output swing while maintaining high open-loop gain; see 図 20 (*Output Voltage Swing vs Output Current*).

7.3.4 Output Drive

The OPAx354-Q1 output stage supplies a continuous output current of ±100 mA and still provide approximately 2.7-V output swing on a 5-V supply, as shown in 図 30.

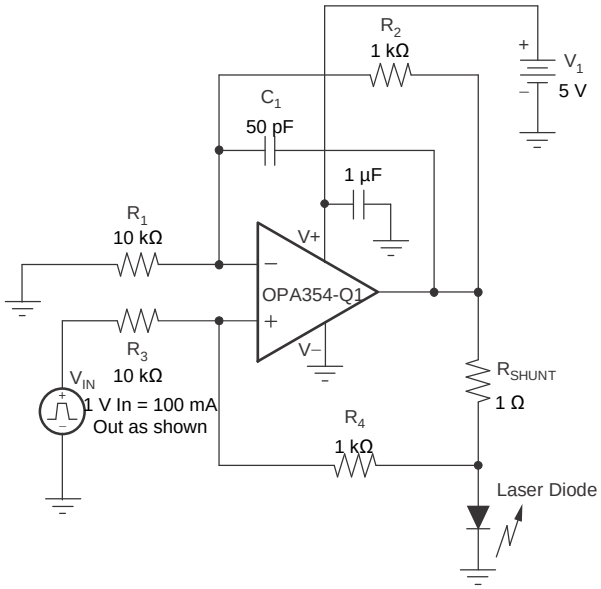


図 30. Laser Diode Driver

For maximum reliability, TI does not recommend running a continuous DC current greater than ±100 mA; see 図 20 (*Output Voltage Swing vs Output Current*). Operate the OPAx354-Q1 family of devices in parallel to supply continuous output currents greater than ±100 mA, as shown in 図 31.

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Feature Description (continued)

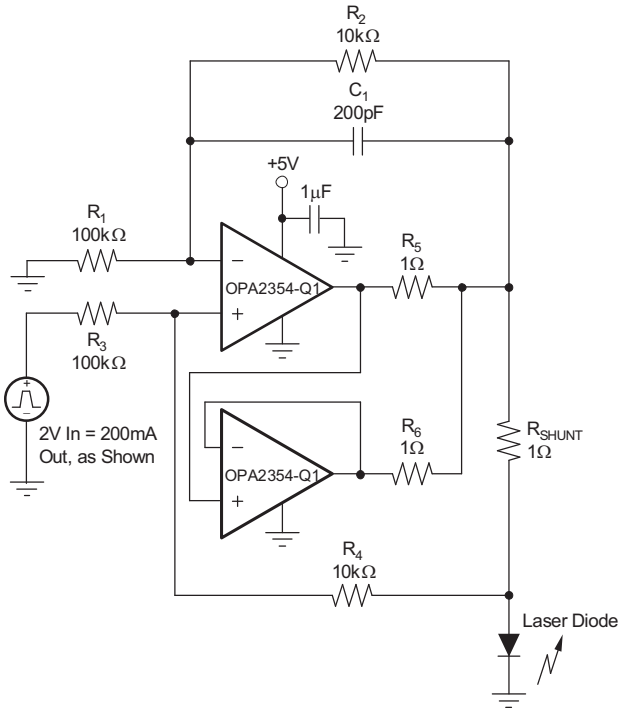


図 31. Parallel Operation

The OPAx354-Q1 family of devices provides peak currents up to 200 mA, which correspond to the typical short-circuit current. Therefore, an on-chip thermal shutdown circuit protects the OPAx354-Q1 family of devices from dangerously high junction temperatures. At 160°C, the protection circuit shuts down the amplifier. Normal operation resumes when the junction temperature cools below 140°C.

7.3.5 Video

The OPAx354-Q1 output stage is capable of driving standard back-terminated 75-Ω video cables (see 図 32). A back-terminated transmission line does not exhibit a capacitive load to the driver. A properly back-terminated 75-Ω cable does not appear as capacitance; the cable presents a 150-Ω resistive load to the OPAx354-Q1 output.

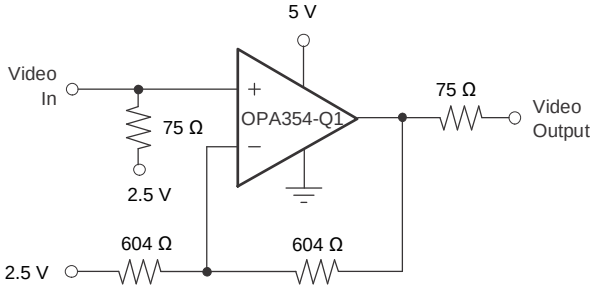
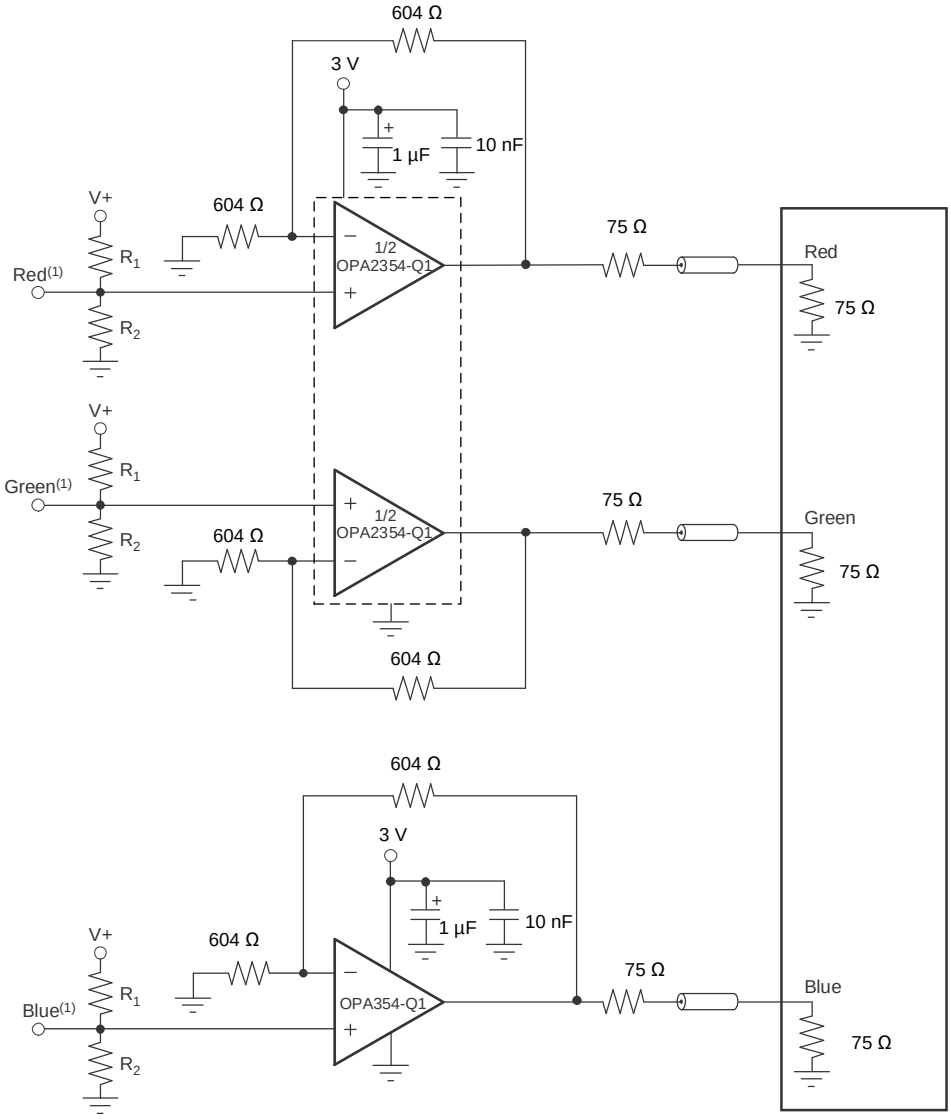


図 32. Single-Supply Video Line Driver

This series of amplifiers can be used as an amplifier for RGB graphic signals, which have a voltage of zero at the video black level by offsetting and AC-coupling the signal (see 図 33).

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Feature Description (continued)



(1) Source video signal offset 300 mV above ground to accommodate op amp swing to ground capability.

図 33. RGB Cable Driver

7.3.6 Driving Analog-to-Digital Converters

The OPAx354-Q1 family of op-amps offers a 60-ns settling time to 0.01%, which makes the devices a viable option for driving high- and medium-speed sampling ADCs and reference circuits. The OPAx354-Q1 family of devices provides an effective means of buffering the input capacitance and resulting charge injection of the ADC while providing signal gain. The OPAx354-Q1 family of devices is designed for applications requiring high DC accuracy.

図 34 shows the OPAx354-Q1 family of devices driving an ADC. With the OPAx354-Q1 family of devices in an inverting configuration, using a capacitor across the feedback resistor can filter high-frequency noise in the signal.

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Feature Description (continued)

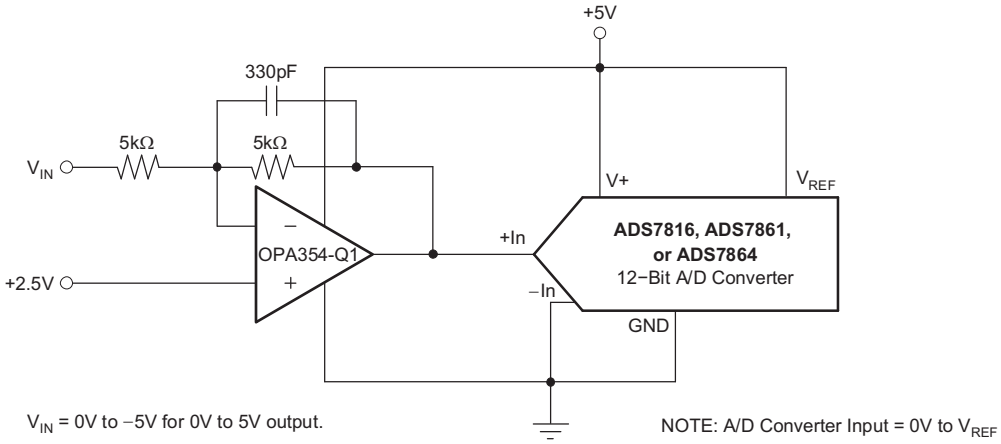


図 34. OPA354A-Q1 Inverting Configuration Driving the ADS7816

7.3.7 Capacitive Load and Stability

The OPAx354-Q1 family op amps can drive a wide range of capacitive loads. However, all op-amps under certain conditions can become unstable. Op amp configuration, gain, and load value are a few of the factors to consider when determining stability. An op amp in unity-gain configuration is most susceptible to the effects of capacitive loading. The capacitive load reacts with the output resistance of the op amp, along with any additional load resistance, to create a pole in the small-signal response that degrades the phase margin. For details, see 図 15 (*Frequency Response vs Capacitive Load*.)

The OPAx354-Q1 topology enhances the ability of the device to drive capacitive loads. In unity gain, these op-amps perform well with large capacitive loads. For details see 図 14, Recommended R_S *vs Capacitive Load*, and 図 15, *Frequency Response vs Capacitive Load*.

Insert a 10-Ω to 20-Ω resistor in series with the output to improve capacitive laod drive in the unity-gain configuration, as shown in 図 35. This configuration significantly reduces ringing with large capacitive loads; see 図 15 (*Frequency Response vs Capacitive Load*.) However, if a resistive load is in parallel with the capacitive load, R_S creates a voltage divider. This configuration introduces a DC error at the output and slightly reduces output swing. This error may be insignificant. For example, if R_L = 10 kΩ and R_S = 20 Ω, the error at the output is approximately 0.2%.

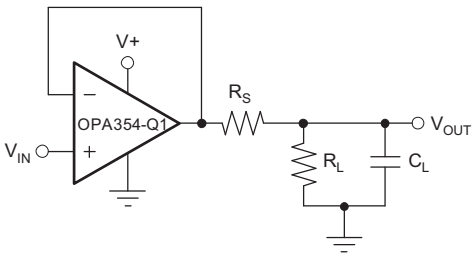


図 35. Series Resistor in Unity-Gain Configuration Improves Capacitive Load Drive

7.3.8 Wideband Transimpedance Amplifier

Wide bandwidth, low-input bias current, and low input voltage and current noise make the OPAx354-Q1 family of devices is designed as a wideband photodiode transimpedance amplifier for low-voltage single-supply applications. Low-voltage noise is important because photodiode capacitance causes the effective noise gain of the circuit to increase at high frequency.

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Feature Description (continued)

The key elements to a transimpedance design, as shown in 図 36, are the expected diode capacitance [including the parasitic input common-mode and differential-mode input capacitance (2 + 2) pF for the OPAx354-Q1], the desired transimpedance gain (R_F), and the gain-bandwidth product (GBW) for the OPAx354-Q1 family of devices (100 MHz). With these three variables set, the feedback capacitor value (C_F) is set to control the frequency response.

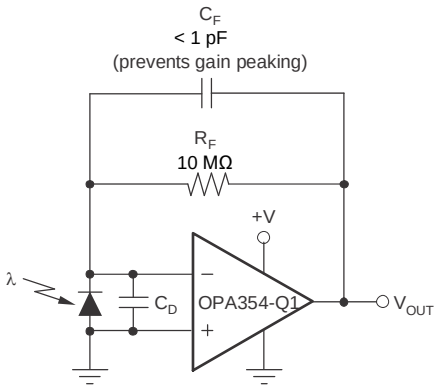


図 36. Transimpedance Amplifier

To achieve a maximally flat second-order Butterworth frequency response, set the feedback pole as shown in 式 1.

$$\frac{1}{2\pi R_F C_F} = \sqrt{\frac{GBP}{4\pi R_F C_D}} \quad (1)$$

Typical surface-mount resistors have a parasitic capacitance of approximately 0.2 pF that required deduction from the calculated feedback capacitance value.

Use 式 2 to calculate the bandwidth.

$$f_{-3dB} = \sqrt{\frac{GBP}{2\pi R_F C_D}} Hz \quad (2)$$

For even higher transimpedance bandwidth, use the high-speed CMOS OPA355-Q1 (200-MHz GBW) or the OPA655-Q1 (400-MHz GBW).

7.4 Device Functional Modes

The OPAx354-Q1 family of devices is powered on when the supply is connected. The devices operates as a single-supply operational amplifier or dual-supply amplifier depending on the application. The devices are used with asymmetrical supplies as long as the differential voltage (V– to V+) is at least 1.8 V and no greater than 5.5 V (example: V– set to –3.5 V and V+ set to 1.5 V).

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8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The OPAx354-Q1 family of devices is a CMOS, rail-to-rail I/O, high-speed, voltage-feedback operational amplifier designed for video, high-speed, and other applications. The OPAx354-Q1 family of devices is available as a single, dual, or quad op-amp.

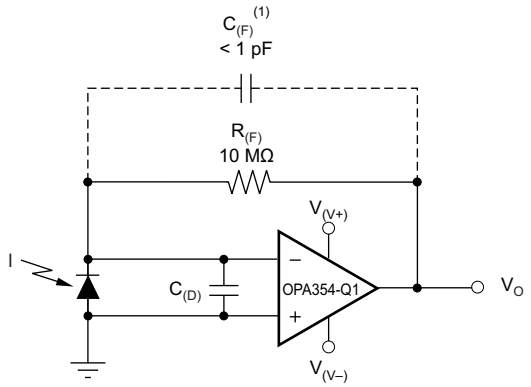
The amplifier features a 100-MHz gain bandwidth, and 150 V/μs slew rate, but the device is unity-gain stable and operates as a 1-V/V voltage follower.

8.2 Typical Applications

8.2.1 Transimpedance Amplifier

Wide gain bandwidth, low input bias current, low input voltage, and current noise make the OPAx354-Q1 family of devices a preferred wideband photodiode transimpedance amplifier. Low-voltage noise is important because photodiode capacitance causes the effective noise gain of the circuit to increase at high frequency.

The key elements to a transimpedance design, as shown in 図 37, are the expected diode capacitance ($C_{(D)}$), which must include the parasitic input common-mode and differential-mode input capacitance (4 pF + 5 pF); the desired transimpedance gain ($R_{(FB)}$); and the gain-bandwidth (GBW) for the OPAx354-Q1 family of devices (20 MHz). With these three variables set, the feedback capacitor value ($C_{(FB)}$) is set to control the frequency response. $C_{(FB)}$ includes the stray capacitance of $R_{(FB)}$, which is 0.2 pF for a typical surface-mount resistor.



(1) $C_{(FB)}$ is optional to prevent gain peaking. $C_{(FB)}$ includes the stray capacitance of $R_{(FB)}$.

図 37. Dual-Supply Transimpedance Amplifier

8.2.1.1 Design Requirements

PARAMETER	VALUE
Supply voltage $V_{(V+)}$	2.5 V
Supply voltage $V_{(V–)}$	–2.5 V

8.2.1.2 Detailed Design Procedure

To achieve a maximally-flat, second-order Butterworth frequency response, the feedback pole must be set to:

$$\frac{1}{2 \times \pi \times R_{(FB)} \times C_{(FB)}} = \sqrt{\frac{GBW}{4 \times \pi \times R_{(FB)} \times C_{(D)}}} \quad (3)$$

Use 式 4 to calculate the bandwidth.

$$f_{(-3\ dB)} = \sqrt{\frac{GBW}{2 \times \pi \times R_{(FB)} \times C_{(D)}}} \quad (4)$$

For other transimpedance bandwidths, consider the high-speed CMOS OPA380 (90-MHz GBW), OPA354 (100-MHz GBW), OPA300 (180-MHz GBW), OPA355 (200-MHz GBW), or OPA656 and OPA657 (400-MHz GBW).

For single-supply applications, the +INx input can be biased with a positive DC voltage to allow the output to reach true zero when the photodiode is not exposed to any light, and respond without the added delay that results from coming out of the negative rail; this configuration is shown in 図 38. This bias voltage appears across the photodiode, providing a reverse bias for faster operation.

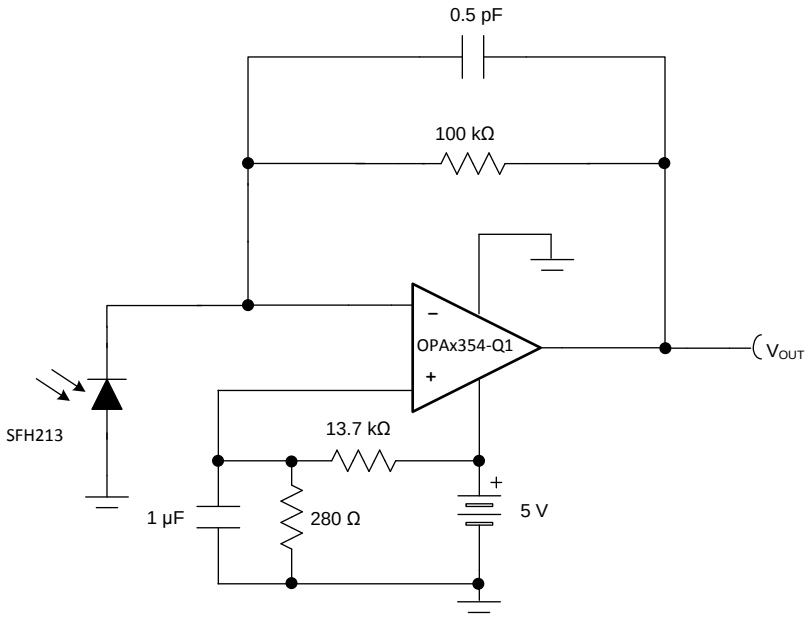


図 38. Single-Supply Transimpedance Amplifier

For additional information, see the *Compensate Transimpedance Amplifiers Intuitively* application bulletin.

8.2.1.2.1 Optimizing The Transimpedance Circuit

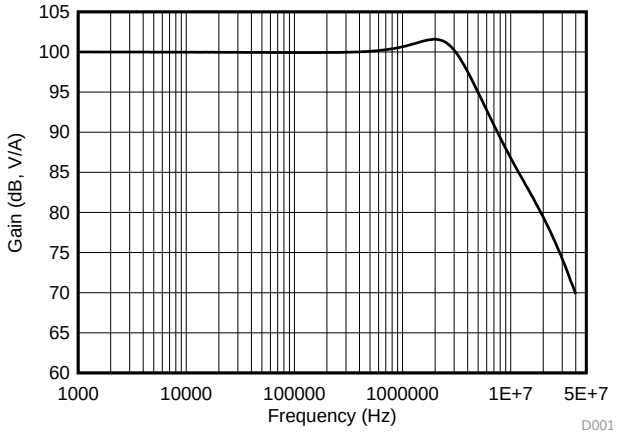
To achieve the best performance, components must be selected according to the following guidelines:

1. For lowest noise, select $R_{(FB)}$ to create the total required gain. Using a lower value for $R_{(FB)}$ and adding gain after the transimpedance amplifier generally produces poorer noise performance. The noise produced by $R_{(FB)}$ increases with the square-root of $R_{(FB)}$, whereas the signal increases linearly. Therefore, signal-to-noise ratio improves when all the required gain is placed in the transimpedance stage.
2. Minimize photodiode capacitance and stray capacitance at the summing junction (inverting input). This capacitance causes the voltage noise of the op amp to be amplified (increasing amplification at high frequency). Using a low-noise voltage source to reverse-bias a photodiode can significantly reduce the capacitance. Smaller photodiodes have lower capacitance. Use optics to concentrate light on a small photodiode.
3. Noise increases with increased bandwidth. Limit the circuit bandwidth to only that required. Use a capacitor across the $R_{(FB)}$ to limit bandwidth, even if not required for stability.
4. Circuit board leakage can degrade the performance of an otherwise well-designed amplifier. Clean the circuit board carefully. A circuit board guard trace that encircles the summing junction and is driven at the same voltage can help control leakage.

For additional information, see the *Noise Analysis of FET Transimpedance Amplifiers*, and *Noise Analysis for High-Speed Op Amps*) application bulletins.

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8.2.1.3 Application Curve



–3 dB bandwidth is 4.56 MHz

図 39. AC Transfer Function

8.2.2 High-Impedance Sensor Interface

Many sensors have high source impedances that may range up to 10 MΩ, or even higher. The output signal of sensors often must be amplified or otherwise conditioned by an amplifier. The input bias current of this amplifier can load the sensor output and cause a voltage drop across the source resistance, as shown in 図 40, where ($V_{(+INx)} = V_S – I_{(BIAS)} × R_{(S)}$). The last term, $I_{(BIAS)} × R_{(S)}$, shows the voltage drop across $R_{(S)}$. To prevent errors introduced to the system as a result of this voltage, use an op amp with low input bias current and high-impedance sensors. This low current keeps the error contribution by $I_{(BIAS)} × R_{(S)}$ less than the input voltage noise of the amplifier, so that the amplifier does not become the dominant noise factor. The OPAx354-Q1 family of devices series of op amps feature low input bias current (typically 200 fA), and are therefore designed for such applications.

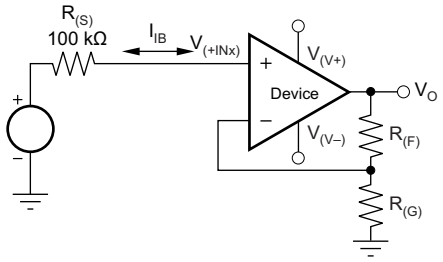
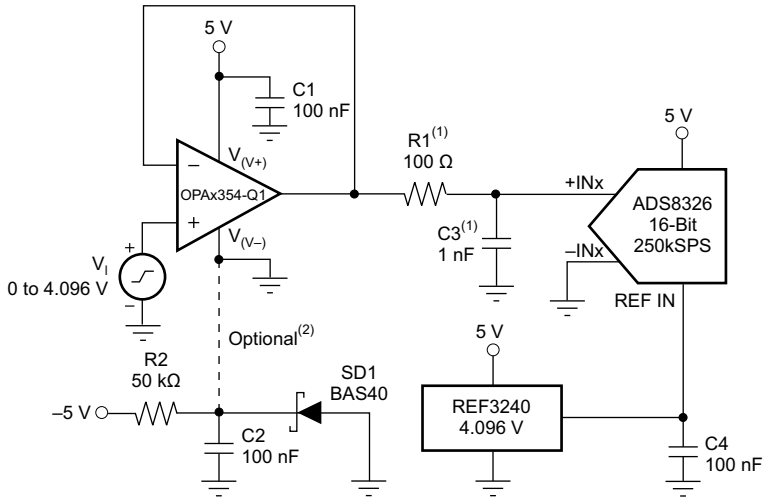


図 40. Noise as a Result of $I_{(BIAS)}$

8.2.3 Driving ADCs

The OPAx354-Q1 op amps are designed for driving sampling analog-to-digital converters (ADCs) with sampling speeds up to 1 MSPS. The zero-crossover distortion input stage topology allows the OPAx354-Q1 family of devices to drive ADCs without degradation of differential linearity and THD.

The OPAx354-Q1 family of devices can be used to buffer the ADC switched input capacitance and resulting charge injection while providing signal gain. 図 41 shows the OPAx354-Q1 family of devices configured to drive the ADS8326.



(1) Suggested value; may require adjustment based on specific application.

(2) Single-supply applications lose a small number of ADC codes near ground as a result of op amp output swing limitation. If a negative power supply is available, this simple circuit creates a –0.3-V supply to allow output swing to true ground potential.

図 41. Driving the ADS8326

8.2.4 Active Filter

The OPAx354-Q1 family of devices is designed for active filter applications that require a wide bandwidth, fast slew rate, low-noise, single-supply operational amplifier. 図 42 shows a 500 kHz, second-order, low-pass filter using the multiple-feedback (MFB) topology. The components are selected to provide a maximally-flat Butterworth response. Beyond the cutoff frequency, roll-off is –40 dB/dec. The Butterworth response is designed for applications requiring predictable gain characteristics, such as the anti-aliasing filter used in front of an ADC.

One point to observe when considering the MFB filter is that the output is inverted relative to the input. If this inversion is not required, or not desired, a noninverting output can be achieved through one of the following options:

1. Adding an inverting amplifier
2. Adding an additional second-order MFB stage
3. Using a noninverting filter topology, such as the Sallen-Key (see 図 43).

MFB and Sallen-Key, low-pass and high-pass filter synthesis is accomplished using TI's FilterPro™ program. This software is available as a free download on www.ti.com.

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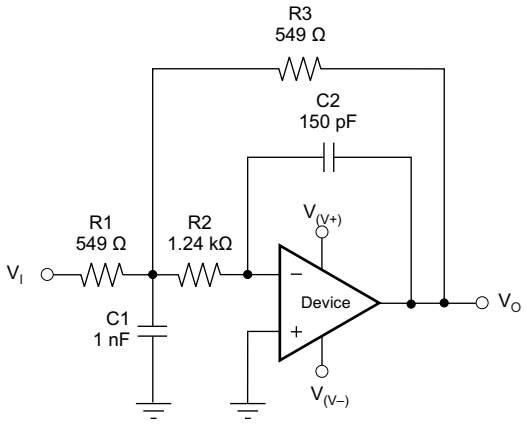


図 42. Second-Order Butterworth 500-kHz Low-Pass Filter

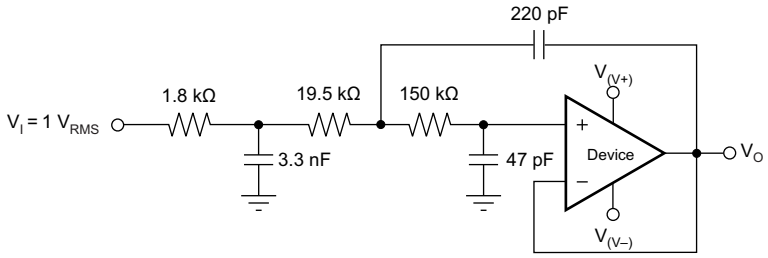


図 43. OPAx354-Q1 Configured as a Three-Pole, 20-kHz, Sallen-Key Filter

9 Power Supply Recommendations

The OPAx354-Q1 family of devices is specified for operation from 2.5 to 5.5 V (±1.25 to ±2.75 V); many specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are shown in the *Typical Characteristics* section.

注意

Supply voltages larger than 7.5 V can permanently damage the device (see the *Absolute Maximum Ratings* table).

Place 0.1-μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the *Layout Guidelines* section.

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9.1 Power Dissipation

Power dissipation depends on power-supply voltage, signal and load conditions. With dc signals, power dissipation is equal to the product of output current times the voltage across the conducting output transistor (V_S – V_O). Minimize power dissipation by using the lowest possible power-supply voltage required to ensure the required output voltage swing.

For resistive loads, the maximum power dissipation occurs at a DC output voltage of one-half the power-supply voltage. Dissipation with AC signals is lower. The *Power Amplifier Stress and Power Handling Limitations* application bulletin from www.ti.com explains how to calculate or measure power dissipation with unusual signals and loads.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat sink. For reliable operation, limit junction temperature to 150°C, maximum. To estimate the margin of safety in a complete design, increase the ambient temperature to trigger the thermal protection at 160°C. The thermal protection must trigger more than 35°C above the maximum expected ambient condition of the application.

10 Layout

10.1 Layout Guidelines

Use good high-frequency printed circuit board (PCB) layout techniques for the OPAx354-Q1 family of devices. Generous use of ground planes, short and direct signal traces, and a suitable bypass capacitor located at the V+ pin ensure clean, stable operation. Large areas of copper provide a means of dissipating heat that is generated in normal operation. Sockets are not recommended for use with any high-speed amplifier. A 10-nF ceramic bypass capacitor is the minimum recommended value; adding a 1-μF or larger tantalum capacitor in parallel can be beneficial when driving a low-resistance load. Providing adequate bypass capacitance is essential to achieving very low harmonic and intermodulation distortion.

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-μF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of the circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, see *Circuit Board Layout Techniques*.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicularly is much better than crossing in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance, as shown in *図 44*.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

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10.2 Layout Example

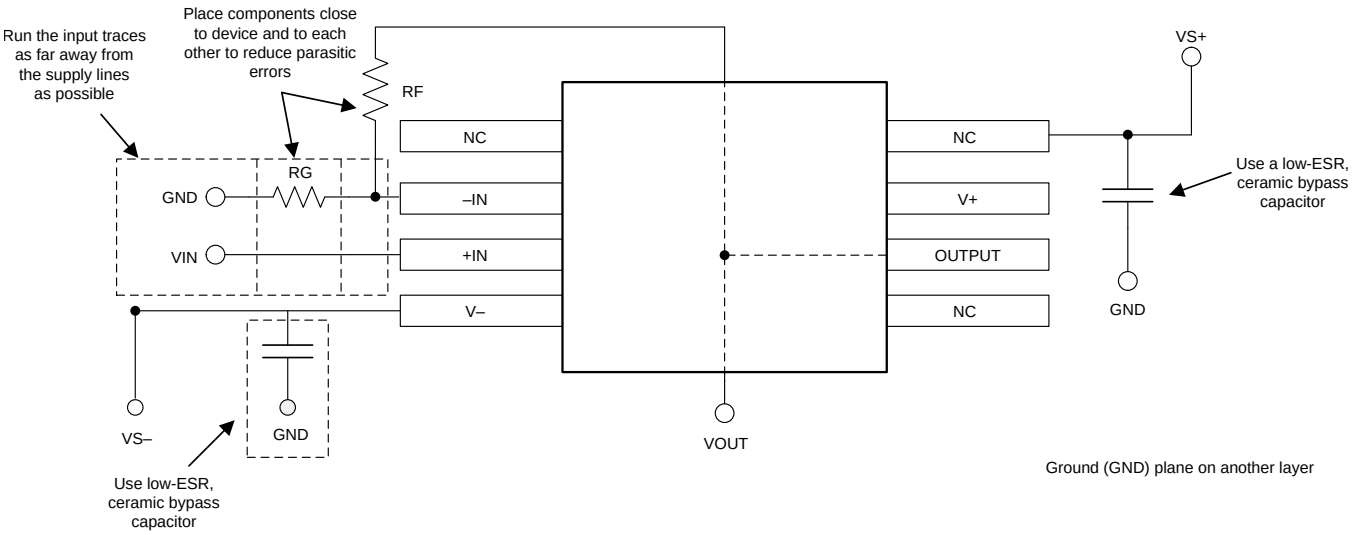


図 44. Operational Amplifier Board Layout for Noninverting Configuration

11 デバイスおよびドキュメントのサポート

11.1 ドキュメントのサポート

11.1.1 関連資料

関連資料については、以下を参照してください。

- テキサス・インスツルメンツ、『ADS8326 16ビット、高速、2.7V～5.5V microPowerサンプリングのアナログ/デジタル・コンバータ』
- テキサス・インスツルメンツ、『回路基板のレイアウト技法』
- テキサス・インスツルメンツ、『トランスインピーダンス・アンプの直感的な補償』
- テキサス・インスツルメンツ、『FilterPro™ユーザー・ガイド』
- テキサス・インスツルメンツ、『FETトランスインピーダンス・アンプのノイズ解析』
- テキサス・インスツルメンツ、『高速オペアンプのノイズ解析』
- テキサス・インスツルメンツ、『OPA380およびOPA2380 高精度、高速トランスインピーダンス・アンプ』
- テキサス・インスツルメンツ、『OPA354、OPA2354、OPA4354 250MHz、レール・ツー・レールI/O、CMOSオペアンプ』
- テキサス・インスツルメンツ、『OPA355、OPA2355、OPA3355 シャットダウン機能付き200MHz、CMOSオペアンプ』
- テキサス・インスツルメンツ、『OPA656 広帯域、ユニティ・ゲイン安定、FET入力オペアンプ』
- テキサス・インスツルメンツ、『パワー・アンプのストレスと電力処理の制限』

11.2 関連リンク

次の表に、クイック・アクセス・リンクを示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびサンプル注文またはご購入へのクイック・アクセスが含まれます。

表 2. 関連リンク

製品	プロダクト・フォルダ	ご注文はこちら	技術資料	ツールとソフトウェア	サポートとコミュニティ
OPA354A-Q1	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
OPA2354A-Q1	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
OPA4354-Q1	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

11.3 ドキュメントの更新通知を受け取る方法

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11.4 コミュニティ・リソース

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設計サポート ***TIの設計サポート*** 役に立つE2Eフォーラムや、設計サポート・ ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

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All other trademarks are the property of their respective owners.

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11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2354AQDGKRQ1	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	OSLQ	Samples
OPA354AQDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OSFQ	Samples
OPA4354AQPWRQ1	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	4354Q1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

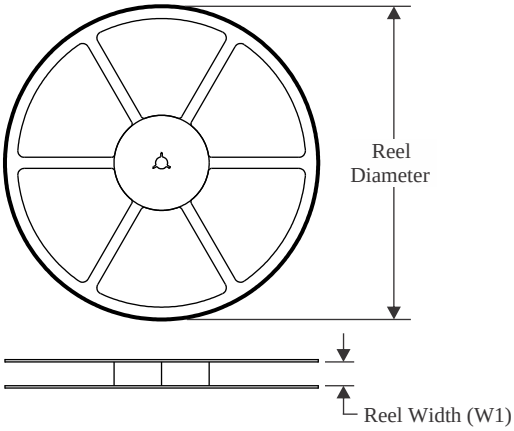
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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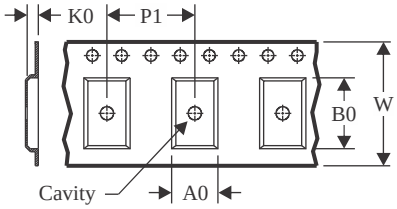
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

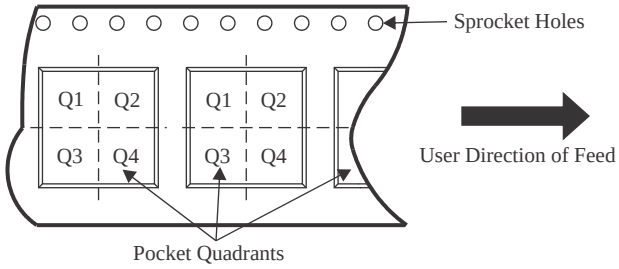


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

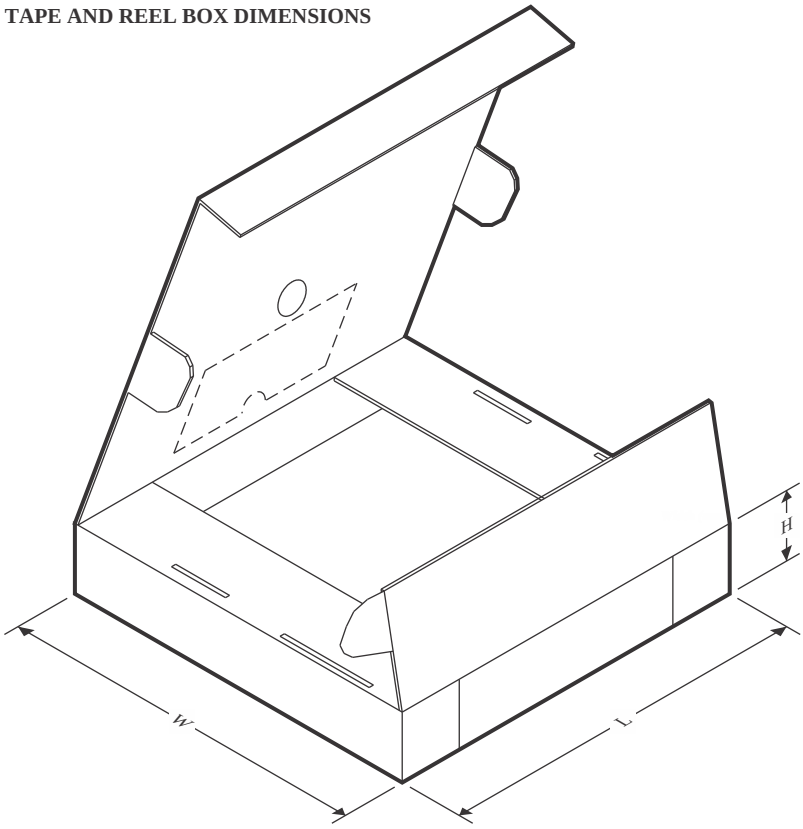
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA354AQDBVRQ1	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA4354AQPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

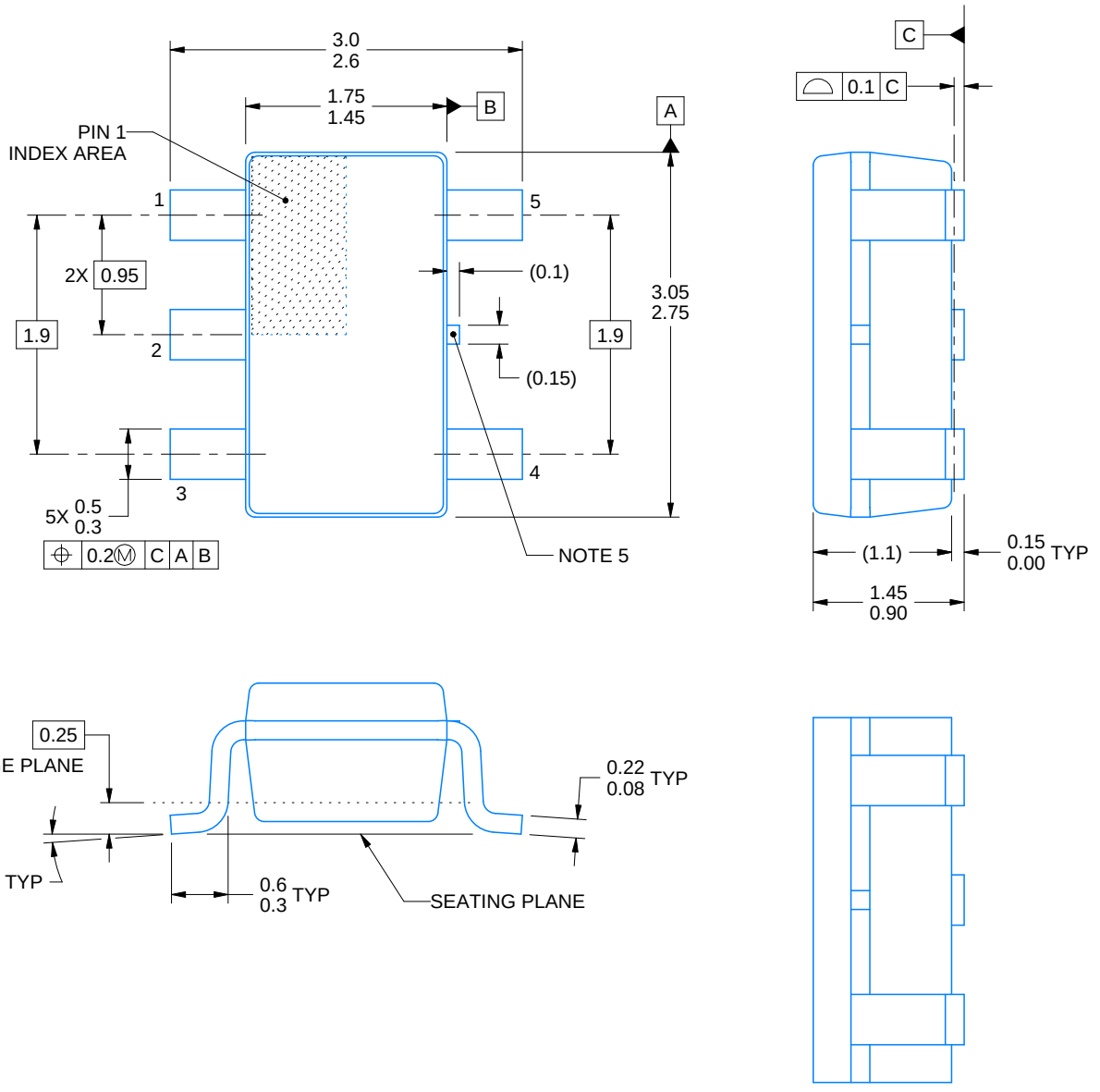
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA354AQDBVRQ1	SOT-23	DBV	5	3000	213.0	191.0	35.0
OPA4354AQPWRQ1	TSSOP	PW	14	2000	356.0	356.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

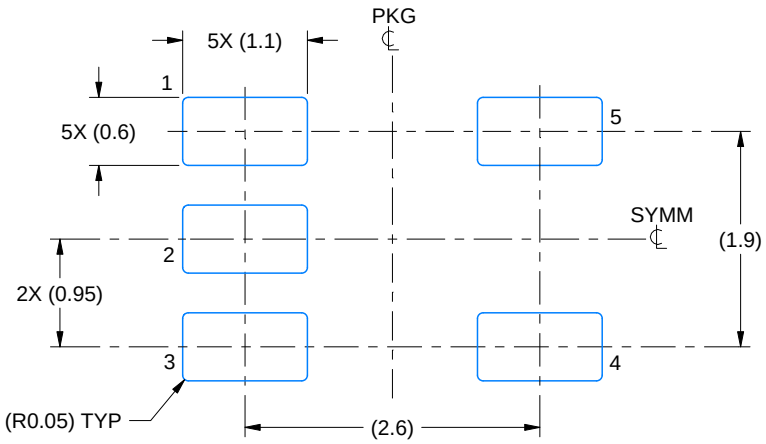


ALTERNATIVE PACKAGE SINGULATION VIEW

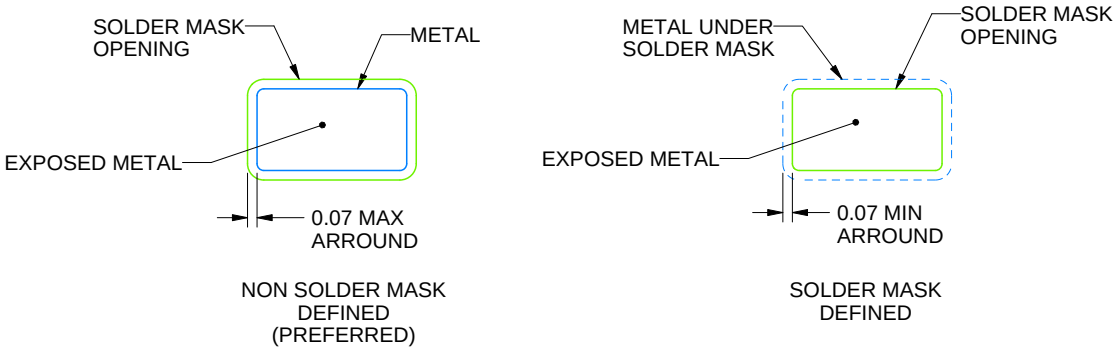
4214839/J 02/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

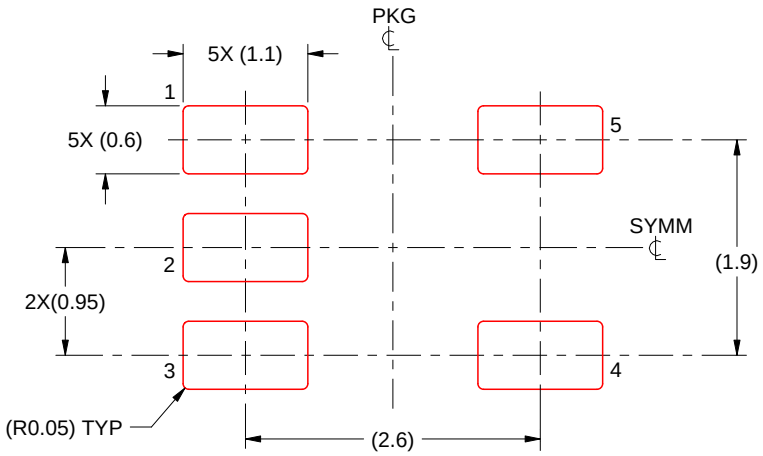


SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



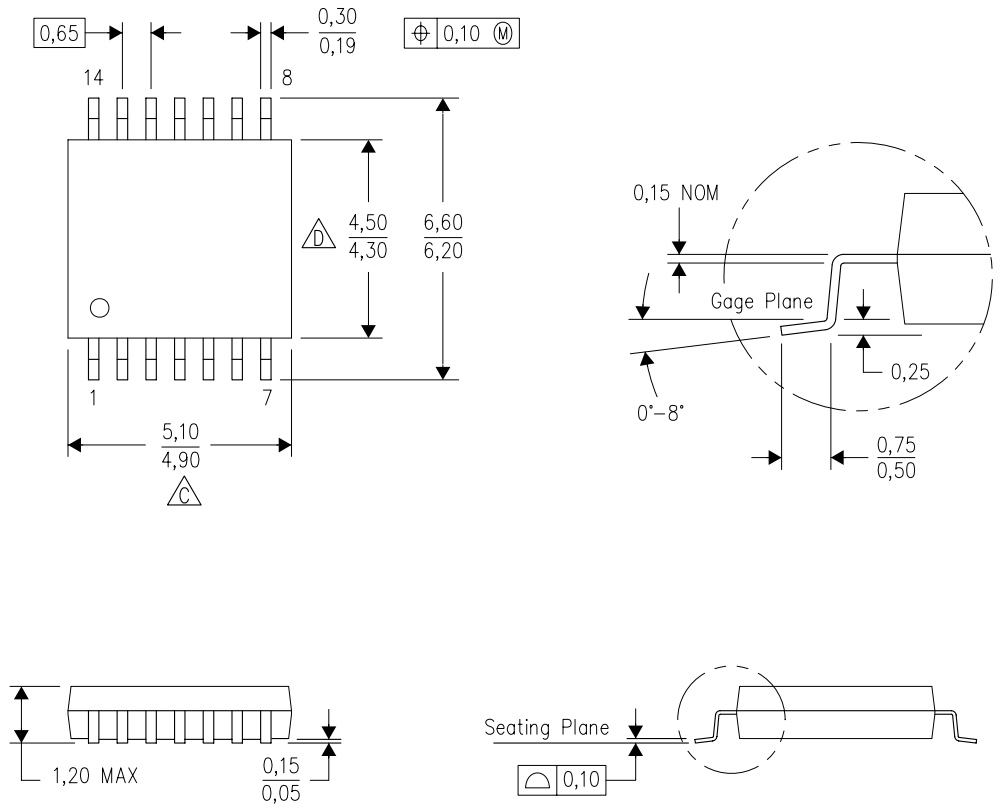
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/J 02/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

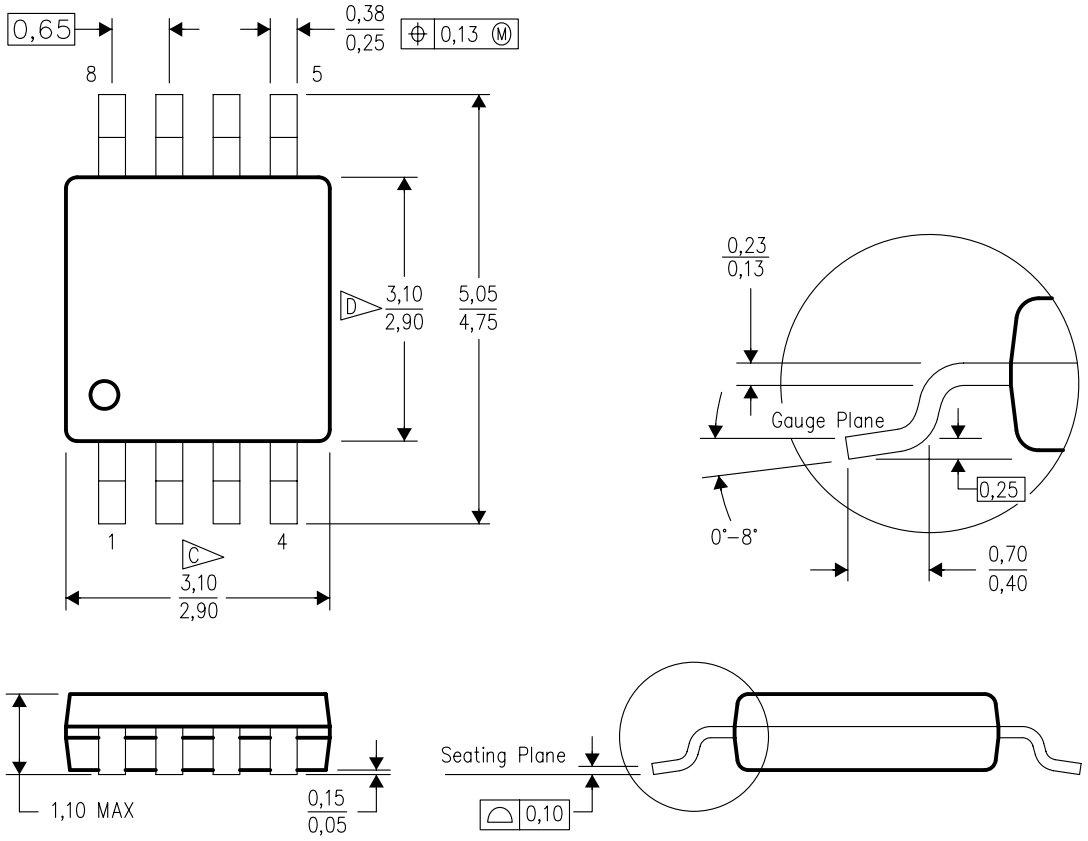
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

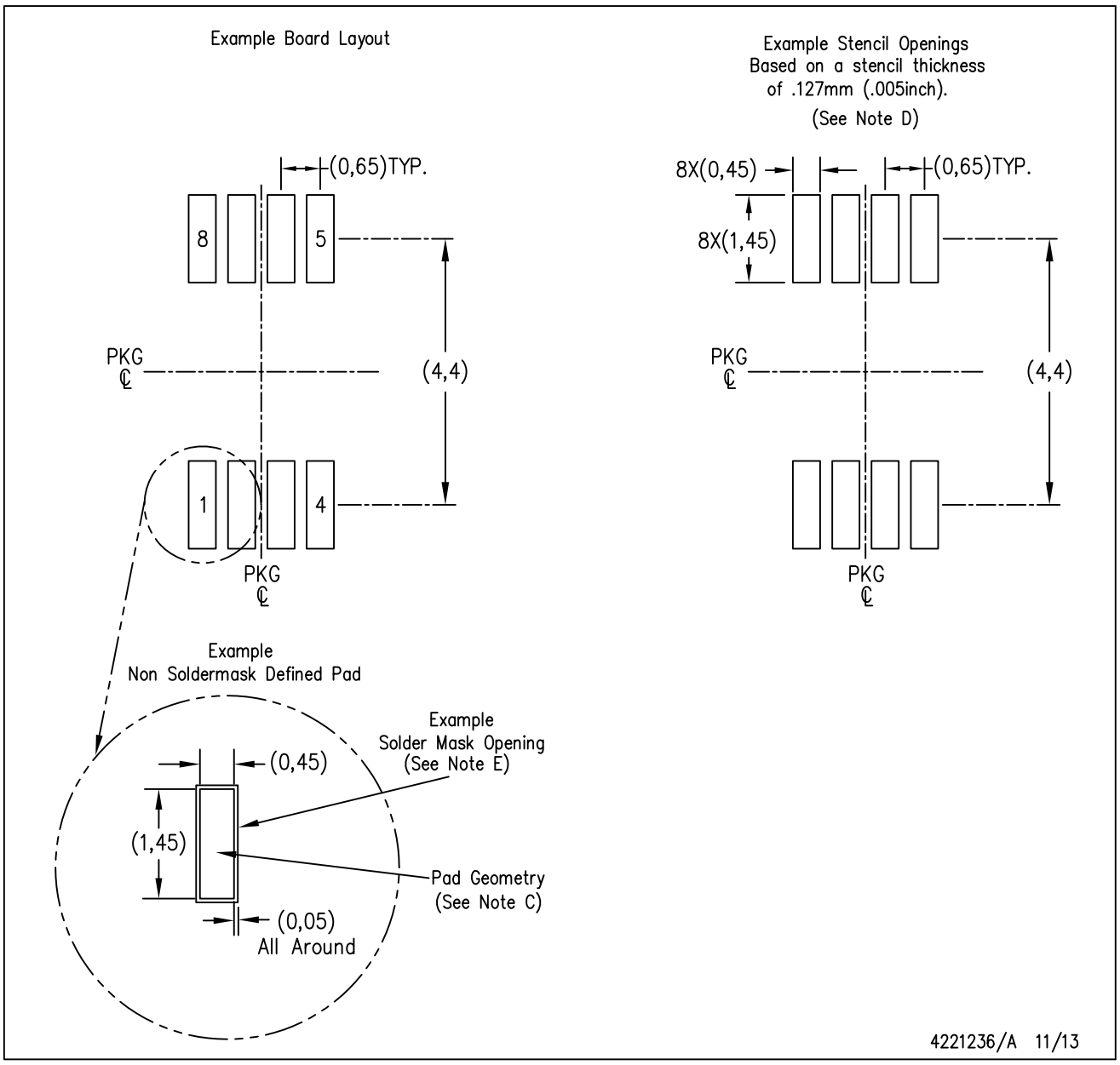
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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