



AM654x、AM652xSitara™ プロセッサ

1 デバイスの概要

1.1 特長

プロセッサ・コア

- デュアルまたはクワッド・コア Arm® Cortex®-A53 マイクロプロセッサ・サブシステム (最高 1.1GHz)
 - 最大 2 つのデュアル・コアまたは 2 つのシングル・コア Arm® Cortex®-A53 クラスに、SECEDED を含む 512KB L2 キャッシュを搭載
 - 各 A53 コアに、32KB L1 I キャッシュと 32KB L1 D キャッシュを搭載
- 最高 400MHz のデュアル・コア Arm® Cortex®-R5F
 - ロックステップ・モード対応
 - 各 R5F コアに 16KB I キャッシュ、16KB D キャッシュ、64KB RAM を搭載

産業用サブシステム

- 3 つの産業用ギガビット通信サブシステム (PRU_ICSSG)
 - 各 PRU_ICSSG に最大 2 つの 10/100/1000 イーサネット・ポートを搭載
 - 2 つの SGMII ポートをサポート ⁽²⁾
 - 10/100Mb PRU-ICSS と互換
 - 各 PRU_ICSSG に 24 の PWM を搭載
 - サイクル単位の制御
 - 強化されたトリップ制御
 - 各 PRU_ICSSG に 18 のシグマ・デルタ・フィルタを搭載
 - 短絡ロジック
 - 過電流ロジック
 - 各 PRU_ICSSG に 6 つのマルチプロトコル位置エンコーダ・インターフェイスを搭載

メモリ・サブシステム

- 最大 2MB のオンチップ L3 RAM、SECEDED 機能付き
- マルチコア共有メモリ・コントローラ (MSMC)
 - 最大 2MB (2 バンク × 1MB) の SRAM、SECEDED 機能付き
 - 共有コヒーレントの L2 または L3 メモリ・マップ SRAM
 - 共有コヒーレントの L3 キャッシュ
 - 256 ビットのプロセッサ・ポート・バスと 40 ビットの物理アドレス・バス
 - コヒーレント統合双方向インターフェイスによりプロセッサまたはデバイス・マスタに接続
 - L2、L3 キャッシュのブリ・ウォーミングとポスト・フラッシング
 - スタベーション・バウンドによる帯域幅管理
 - 1 つのインフラストラクチャ・マスタ・インターフェイス
 - 1 つの外部メモリ・マスタ・インターフェイス
 - 分散仮想システムをサポート

- 内蔵 DMA エンジン (データ・ルーティング・ユニット (DRU)) をサポート
- ECC エラー保護
- DDR サブシステム (DDRSS)
 - DDR-1600 までの DDR3L/DDR4 メモリ・タイプをサポート
 - DDR-1333 までの LPDDR4 メモリ・タイプをサポート
 - 32 ビットのデータ・バスと 7 ビットの SECEDED バス
 - 32GB の総アドレス空間
- 汎用メモリ・コントローラ (GPMC)
 - SafeTI™ 半導体コンポーネント
- 機能安全アプリケーション向けに設計
- IEC 61508 の要件に従って開発
- SIL-3 のインテグリティ・レベルを実現
- MCU 安全アイランドには、SIL-2 ランダム・フォルト・インテグリティ要件を達成するのに十分な診断機能を搭載
- SoC の他の部分には、SIL-2 ランダム・フォルト・インテグリティ要件を達成するのに十分な診断機能を搭載
- さらに、適切な安全性コンセプト (例: ソフトウェアによる相互比較) を前提として SIL-3 アプリケーションを実行するのに十分なアーキテクチャ指標を完備
- 機能安全マニュアルを提供
- 安全性関連の認証
 - TÜV SÜD によるコンポーネント・レベルの機能安全認証 [認証作業中]
- 機能安全関連の機能
 - 計算に重要なメモリと内部バス・インターコネクトの ECC またはパリティ
 - ファイアウォールにより無干渉 (FFI) の実現を支援
 - CPU、ハイエンド・タイマ、オンチップ RAM の内蔵セルフテスト (BIST)
 - ハードウェア・エラー注入のサポートにより診断用テストを支援
 - エラー信号モジュール (ESM) により機能安全関連のエラーを捕捉
 - 電圧、温度、およびクロック監視
 - 複数のクロック・ドメインのウィンドウ/非ウィンドウ・ウォッチドッグ・タイマ
- MCU アイランド
 - デュアル・コア Arm® Cortex®-R5F マイクロプロセッサ・サブシステムの分離
 - 個別の電圧、クロック、リセット、専用ペリフェラル
 - 内蔵 MCSPI により SoC の他の部分に接続



- セキュア・ブート対応
 - ハードウェアによる信頼の基点
 - バックアップ・キーによる信頼の基点の切り替えをサポート
 - テイクオーバー保護、IP 保護、ロールバック禁止保護のサポート
- 暗号化アクセラレーション対応
 - 受信データ・ストリームに基づいてキーマテリアルを自動的に切り替えできるセッション認識暗号化エンジン
 - 暗号化コアをサポート
 - AES - 128/192/256 ビットのキー・サイズ
 - 3DES - 56/112/168 ビットのキー・サイズ
 - MD5、SHA1
 - SHA2 - 224/256/384/512
 - DRBG と真性乱数発生器
 - PKA (公開鍵アクセラレータ) により RSA/ECC 処理を支援
 - DMA サポート
- デバッグのセキュリティ
 - ソフトウェア制御によるセキュアなデバッグ・アクセス
 - セキュリティ対応のデバッグ
- 信頼できる実行環境 (TEE) に対応
 - Arm® TrustZone®をベースとする TEE
 - 分離用の広範なファイアウォール・サポート
 - セキュアなDMAパスとインターコネクト
 - セキュアなウォッチドッグ/タイマ/IPC
- セキュアなストレージのサポート
- OSPI™ インターフェイスでのオンザフライ暗号化/認証のサポート
- パケット・ベースのハードウェア暗号化エンジンによるデータ (ペイロード) 暗号化/認証でのネットワーク・セキュリティ・サポート
- セキュリティ・コプロセッサ (DMSC) によりキーおよびセキュリティ管理を実現、専用のデバイス・レベル・インターコネクトによりセキュリティを確保
- SoC サービス
- デバイス管理セキュリティ・コントローラ (DMSC)
 - 集中 SoC システム・コントローラ
 - 初期ブート、セキュリティ、機能安全、クロック/リセット/電源管理を含むシステム・サービスを管理
 - アクティブおよび低消費電力モードの電源管理コントローラ
 - メッセージ・マネージャを介したさまざまな処理ユニットとの通信
 - シンプルなインターフェイスにより未使用ペリフェラルを最適化
 - トレース/デバッグ機能
- 16 個の 32 ビット汎用タイマ
- 2 つのデータ移動/制御ナビゲータ・サブシステム (NAVSS)
 - リング・アクセラレータ (RA)
 - 統合 DMA (UDMA)
 - 最大 2 つのタイマ・マネージャ (TM) (それぞれ 1024 個のタイマ)
- マルチメディア
 - ディスプレイ・サブシステム
 - 2 つのディスプレイ出力に関連付けられた 2 つの完全入力マップ・オーバーレイ・マネージャ
 - 1 ポートの MIPI® DPI 平行ル・インターフェイス
 - 1 ポートの OLDI
 - PowerVR® SGX544-MP1 3D グラフィック処理ユニット (GPU)
 - 1 つのカメラ・シリアル・インターフェイス -2 (MIPI CSI-2)
 - 1 ポートのビデオ・キャプチャ: BT.656/1120 (組み込み同期なし)
- 高速インターフェイス
 - 次の機能をサポートする 1 つのギガビット・イーサネット (CPSW) インターフェイス
 - RMII (10/100)または RGMII (10/100/1000)
 - IEEE1588 (2008 Annex D、Annex E、Annex F)と 802.1AS PTP
 - オーディオ/ビデオ・ブリッジ (P802.1Qav/D6.0)
 - Energy-Efficient Ethernet (802.3az)
 - ジャンボ・フレーム (2024 バイト)
 - Clause 45 MDIO PHY 管理
- 2 つの PCI-Express® (PCIe®) Revision 3.1 サブシステム (2)
 - Gen3 (8.0GT/s) 動作対応
 - 2 つの独立した 1 レーン・ポート、または 1 つの 2 レーン・ポート
 - ルートコンプレックス/エンドポイントの同時動作に対応
- USB 3.1 デュアルロール・デバイス (DRD) サブシステム (2)
 - 1 つの Enhanced SuperSpeed Gen1 ポート
 - 1 つの USB 2.0 ポート
 - 各ポートを個別に USB ホスト、USB ペリフェラル、USB DRD として構成可能
- 一般的な接続機能
 - 6 つの I²C™ (Inter-Integrated Circuit) ポート
 - 5 つの構成可能な UART/IrDA/CIR モジュール
 - 2 つの同時フラッシュ・インターフェイスを以下のように構成可能
 - 2 つの OSPI フラッシュ・インターフェイス
 - または HyperBus™ および OSPI1 フラッシュ・インターフェイス
 - 2 つの 12 ビット・アナログ/デジタル・コンバータ (ADC)
 - 最大 4M サンプル/秒
 - 8 つの多重アナログ入力
 - 8 つのマルチチャネル・シリアル・ペリフェラル・インターフェイス (MCSPI) コントローラ
 - 内部接続用×2
 - 外部インターフェイス用×6
- 汎用 I/O (GPIO) ピン

制御インターフェイス

- 6つの拡張高分解能パルス幅変調器 (EHRPWM) モジュール
- 1つの拡張キャプチャ (ECAP) モジュール
- 3つの拡張直交エンコーダ・パルス (EQEP) モジュール

車載インターフェイス

- CAN-FD をフルサポートする 2つのモジュラー・コントローラ・エリア・ネットワーク (MCAN) モジュール

オーディオ・インターフェイス

- 3つのマルチチャネル・オーディオ・シリアル・ポート (MCASP) モジュール

メディアおよびデータ・ストレージ

- 2つのマルチメディア・カード/ Secure Digital[®] (MMC[™]/ SD[®]) インターフェイス

シンプルな電源管理

- シンプルな電源シーケンスでデュアル電圧 I/O をフルサポート
- 内蔵 LDO により電源ソリューションの複雑さを軽減
- 内蔵 SDIO LDO により SD インターフェイスでの自動

電圧遷移に対応

- 内蔵のパワー・オン・リセット (POR) 生成機能により電源ソリューションの複雑さを低減
- 内蔵の電圧スーパーバイザにより機能的安全性を監視
- 内蔵の電源グリッチ検出器により高速電源過渡を検出
- アナログシステム統合
- USB VBUS 検出機能を内蔵
- DDR RESET 用のフェイルセーフ I/O
- リセット中にすべての I/O ピン・ドライバをディセーブルにすることでバス競合を回避
- リセット中にデフォルトの I/O プルをディセーブルにすることでシステム競合を回避
- 動的な I/O ピンのマルチプレクサ構成変更に対応
- システム・オン・チップ (SoC) アーキテクチャ
- UART、I2C、OSPI、HyperBus、パラレル NOR フラッシュ、SD または eMMC[™]、USB、PCIe、イーサネット・インターフェイスからのプライマリ・ブートをサポート
- 28nm CMOS テクノロジー
- 23mm × 23mm、0.8mm ピッチ、784 ピンの FCBGA (ACD)

1.2 アプリケーション

- 産業用プログラマブル・コントローラ (PLC)
- 安全機能付きファクトリ・オートメーション
- マルチプロトコル・フィールドバス通信
- 産業用 PC
- 産業用ロボット
- ヒューマン・マシン・インターフェイス (HMI)
- 電力網インフラストラクチャの保護リレー
- ロボット用モータ・ドライブ

1.3 概要

AM654x および AM652x Sitara™ プロセッサは、最新のインダストリー 4.0 組み込み製品の複雑な処理の要求を満たすように設計した Arm® アプリケーション・プロセッサです。

AM654x および AM652x デバイスは、産業用接続性と処理能力を備えた機能安全性用途向け高性能産業用制御 SoC を実現するため、4 つまたは 2 つの Arm® Cortex®-A53 コア、お客様が最終製品の機能安全性の目標を達成するのに役立つ機能を内蔵したデュアル Arm® Cortex®-R5F MCU サブシステム、3 つの産業用ギガビット通信サブシステム (PRU_ICSSG) を組み合わせています。AM65xx は現在、TÜV SÜD により IEC 61508 認証評価中です。

AM654x の 4 つの Arm® Cortex®-A53 コアは共有 L2 メモリを持つ 2 つのデュアルコア・クラスタに配置され 2 つの処理チャネルを形成しています。AM652x の 2 つの Arm® Cortex®-A53 コアは、1 つのデュアルコア・クラスタまたは 2 つのシングルコア・クラスタとして使用できます。拡張 ECC をオンチップ・メモリ、ペリフェラル、およびインターコネクに内蔵することで信頼性を確保しています。SoC 全体として、機能安全目標を達成するシステム設計の支援を特長としています (TÜV SÜD による評価待ち)。一部の AM654x および AM652x では、DMSC が管理する粒度の細かいファイアウォールに加えて、暗号化アクセラレーションとセキュア・ブートも使用できます。

プログラミング機能は Arm® Cortex®-A53 RISC CPU と Arm® Neon™ 拡張機能で提供します。デュアル Arm® Cortex®-R5F MCU サブシステムは 2 つのコアとして汎用用途に使用できます。または、機能安全性アプリケーションの要求を満たすのに便利なロックステップでも使用できます。PRU_ICSSG サブシステムは、Profinet IRT、TSN、イーサネット/IP、EtherCAT®、その他各種の産業用イーサネット向けに最大 6 ポートを提供することも、標準のギガビット・イーサネット接続に使用することもできます。

TI は、Arm® コア向けに、C コンパイラとソースコードの実行を見通すためのデバッグ・インターフェイスだけでなく、Linux、Linux-RT、RTOS、Android 用プロセッサ SDK を含むソフトウェアおよび開発ツール一式を提供しています。機能安全とセキュリティに関する資料も提供し、機能安全またはセキュリティ関連システムの開発を支援します。

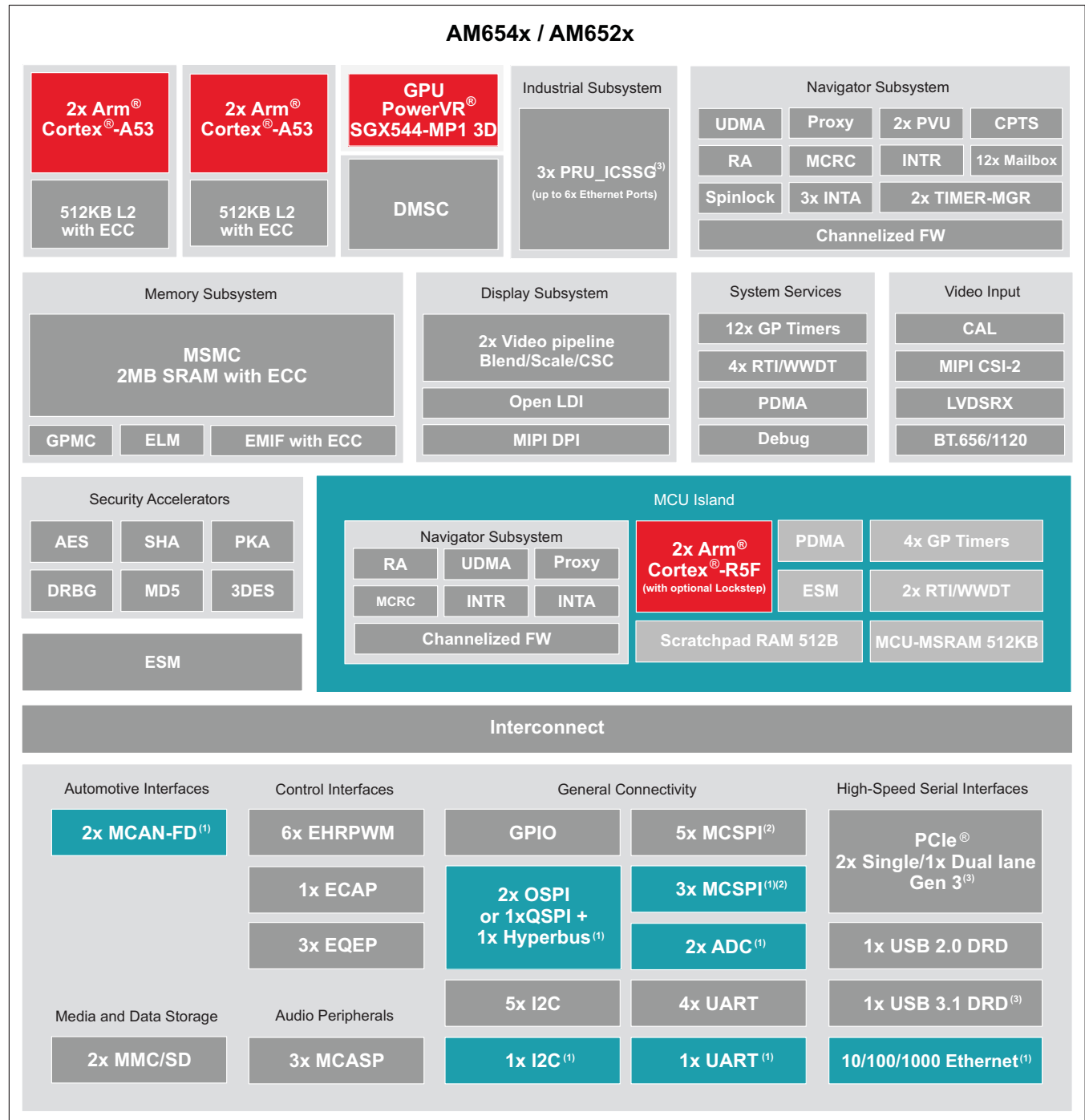
製品情報⁽¹⁾

型番	パッケージ	本体サイズ
AM6548ACD	FCBGA (784)	23.0mm×23.0mm
AM6528ACD	FCBGA (784)	23.0mm×23.0mm
AM6546ACD	FCBGA (784)	23.0mm×23.0mm
AM6526ACD	FCBGA (784)	23.0mm×23.0mm
AM6527ACD	FCBGA (784)	23.0mm×23.0mm

(1) 詳細については、9、「メカニカル、パッケージ、および注文情報」を参照してください。

1.4 機能ブロック図

図 1-1 は、デバイスの機能ブロック図です。



- (1) このインターフェイスはMCUアイランドに位置しますが、システム全体からアクセス可能です。
 (2) ポートの1つは内部接続のみで、どのピンにも接続されていません。
 (3) SGMII, USB3.1, PCIeで計2つのSerDesレーンを共有しています。

図 1-1. AM654x、AM652xブロック図

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2 改訂履歴

2019年3月23日発行分から2019年06月21日発行分への変更 (from G Revision (March 2019) to H Revision)	Page
1.1、「特長」に、GPU 特定のため「PowerVR SGX544-MP1 3D」を追加 2 - Added clarification for PRU_ICSSG MII support in 表 3-1, <i>Device Comparison</i> 8 - Added PowerVR SGX544-MP1 3D to Identify the GPU in 表 3-1, <i>Device Comparison</i> 8 - Updated type, I/O Voltage Value, Power, Buffer Type and IO Daisy Chain of MON pins in 表 4-1, <i>Pin Attributes</i> 10 - Updated MMC SDCCD and SDWP Power Connection 10 - Updated footnotes under MMC Signal Description Tables 82 - Updated note (6) regarding VDDA_VSYS_MON 105 - Added 表 4-77, <i>Reserved Balls to Reserved Balls Specific Connection Requirements</i> and Updated 表 4-76, <i>Unused Balls Specific Connection Requirements</i> 117 - Added electrical characteristics for monitor pins in Section 5.1, <i>Absolute Maximum Ratings</i> and Section 5.4, <i>Recommended Operating Conditions</i> 119 - Updated Transient Overshoot and Undershoot specification at IO pin parameter 121 - Updated JEDEC specification for CDM method in Section 5.2, <i>ESD Ratings</i> 121 - Removed Power Consumption Summary section 125 - Updated Impact to Your Hardware Warranty section 134 - Updated the default state of WKUP_LFOSC0 and HFOSC1 in Section 5.9.2, <i>Power Supply Sequencing</i> and Section 5.9.4.1, <i>Input Clocks / Oscillators</i> 137 - Removed table PLL Power Supply Requirements and the information is moved in Section 5.4, <i>Recommended Operating Conditions</i> 154 - Updated MDIO Timing Diagram and MDIO7 parameter values 156 - Updated delay time in 表 5-42, <i>Timing Requirements for eHRPWM</i> 164 - Added 表 5-76, <i>MMC DLL Delay Mapping for all Timing Modes</i> 210 - Updated timing specification values in 5.9.5.19, <i>OLDI</i> 217 - Updated all sections in 6, <i>Detailed Description</i> and aligned with the device TRM. 236 - Added PowerVR SGX544-MP1 3D to Identify the GPU in 6, <i>Detailed Description</i> 244 - Added 6.5, <i>Identification</i> and 6.6, <i>Boot Modes</i> 280 - Added VDDA_VSYS_MON voltage divider details in 7.5, <i>System Power Supply Design Guidelines</i> 289 - Updated Figures in 7.8.1, <i>LVC MOS External Capacitor Connections</i> 292	

3 Device Comparison

表 3-1 shows a comparison between devices, highlighting the differences.

表 3-1. Device Comparison

FEATURES	REFERENCE NAME	AM6548	AM6528	AM6546	AM6526	AM6527
Features						
CTRLMMR_WKUP_JTAG_DEVICE_ID [31:11] DEVICE_ID register bitfield value ⁽⁵⁾		AM6548: 0x140FA	AM6528: 0x140BA	AM6546: 0x14178	AM6526: 0x14138	AM6527-E: 0x14239
		AM6548-E: 0x140FB	AM6528-E: 0x140BB	AM6546-E: 0x14179	AM6526-E: 0x14139	
		AM6548-F: 0x140FE	AM6528-F: 0x140BE	AM6546-F: 0x1417C	AM6526-F: 0x1413C	AM6527-E,F: 0x1423D
		AM6548-E,F: 0x140FF	AM6528-E,F: 0x140BF	AM6546-E,F: 0x1417D	AM6526-E,F: 0x1413D	
PROCESSORS AND ACCELERATORS						
Speed Grades		See 表 5-1				
Arm Cortex-A53 Microprocessor Subsystem	Arm A53	Quad Core (Cluster 0, Cluster 1)	Dual Core (Cluster 0)	Quad Core (Cluster 0, Cluster 1)	Dual Core (Cluster 0)	Dual Core (Cluster 0 Core 0, Cluster 1 Core 0)
Dual-Core Arm Cortex-R5F	Arm R5F	Yes (optional lockstep ⁽⁴⁾)				
Device Management Security Controller	DMSC	Yes				
Graphics Accelerator (SGX544-MP1)	GPU	Yes		Not Supported ⁽¹⁾		
Safety Features	Safety	Optional ⁽⁴⁾		Optional ⁽⁴⁾		
PROGRAM AND DATA STORAGE						
On-Chip Shared Memory (RAM)	MCU_MSRAM	512KB				
Multicore Shared Memory Controller	MSMC	2MB (On-Chip Shared SRAM with ECC)				
DDR3L/DDR4/LPDDR4 DDR Subsystem	DDRSS	Up to 32GB (32-Bit data)				
	SECDED	7-Bit				
General-Purpose Memory Controller	GPMC	Up to 1GB with ECC				
Error Location Module	ELM	Yes				
PERIPHERALS						
Display Subsystem	DSS	Yes				
Modular Controller Area Network Interface	MCAN	2				
Peripheral Direct Memory Access	PDMA	Yes				
Navigator Subsystem	NAVSS	2				
General-Purpose I/O	GPIO	Up to 242				
Inter-Integrated Circuit Interface	I2C	6				
Analog-to-Digital Converter	ADC	2				
Camera Adaptation Layer (CAL) with Camera Serial Interface (CSI2) and Video Input Port (VIN)	CSI2	1 CLK + 4 Data				
	VIN0	Yes				
Multichannel Serial Peripheral Interface	MCSPI	8				
Multichannel Audio Serial Port	MCASP0	16 Serializers				
	MCASP1	10 Serializers				
	MCASP2	4 Serializers				
MultiMedia Card/ Secure Digital Interface	MMCS0	8-bits				
	MMCS01	4-bits				

表 3-1. Device Comparison (continued)

FEATURES	REFERENCE NAME	AM6548	AM6528	AM6546	AM6526	AM6527
Features						
Flash Subsystem (FSS)	OSPI0	8-bits ⁽³⁾				
	OSPI1	4-bits				
	HyperBus	Yes ⁽³⁾				
Security Accelerator	SA	Yes				
Error Signalling Module	ESM	Yes				
2x PCI Express 3.1 Port with Integrated PHY	PCIE0	Up to Two Lanes ⁽²⁾				
	PCIE1	Single Lane ⁽²⁾				
3x Programmable Real-Time Unit Subsystem and Industrial Communication Subsystem	PRU_ICSSG0	Yes (2× RGMII, 2× MII)				
	PRU_ICSSG1	Yes (2× RGMII, 2× MII)				
	PRU_ICSSG2	Yes (2× RGMII, 2× MII, 2× SGMII ⁽²⁾)				
Gigabit Ethernet Interface	CPSW	RMII or RGMII				
General-Purpose Timers	TIMER	16				
Enhanced High Resolution Pulse-Width Modulator Module	EHRPWM	6				
Enhanced Capture Module	ECAP	1				
Enhanced Quadrature Encoder Pulse Module	EQEP	3				
Universal Asynchronous Receiver and Transmitter	UART	5				
Universal Serial Bus (USB3.1) SuperSpeed Dual-Role-Device (DRD) Ports with SS PHY	USB0	Yes ⁽²⁾				
Universal Serial Bus (USB2.0) HighSpeed Dual-Role-Device (DRD) Ports with HS/FS PHY	USB1	Yes				

(1) Features noted as “not supported”, must not be used. Their functionality is not supported by TI for this family of devices. These features are subject to removal without notice on future device revisions. Any information regarding the unsupported features has been retained in the documentation solely for the purpose of clarifying signal names or for consistency with previous feature descriptions.

(2) SGMII0, SGMII1, USB3.1, PCIE0, and PCIE1 share total of two SerDes lanes.

(3) Two simultaneous flash interfaces configured as OSPI0 and OSPI1, or HyperBus and OSPI1.

(4) Device supports features to aid in functional safety system designs such as lockstep Arm R5F if the part number is designated with the F option.

(5) For more details about the CTRLMMR_WKUP_JTAG_DEVICE_ID register and DEVICE_ID bitfield, see the device TRM.

3.1 Related Products

Sitara™ processors Scalable processors based on Arm Cortex-A cores with flexible peripherals, connectivity & unified software support – perfect for sensors to servers.

Sitara™ processors – Applications Sitara processors provide scalable solutions for a wide range of applications from HMIs and gateways to more complex equipment such as drives and substation automation equipment. Sitara Arm processors offer scalability and reliability as well as multi-protocol support for industrial communication protocols such as EtherCAT, Ethernet/IP and Profinet.

Sitara™ processors – Reference designs TI provides many reference designs containing ‘building block’ solutions to enable customers to rapidly development of their unique products and solutions.

Companion Products for AM654x, AM652x Review products that are frequently purchased or used in conjunction with this product.

4 Terminal Configuration and Functions

4.1 Pin Diagram

注: The terms "ball", "pin", and "terminal" are used interchangeably throughout the document. An attempt is made to use "ball" only when referring to the physical package.

图 4-1 shows the ball locations for the 784 plastic ball grid array (FCBGA) package that are used in conjunction with 表 4-1 through to locate signal names and ball grid numbers.

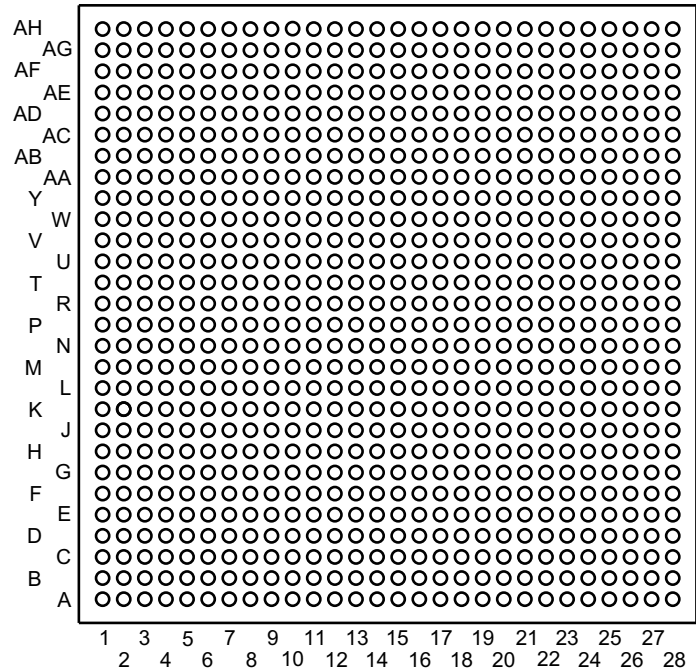


图 4-1. ACD FCBGA-N784 Package (Bottom View)

4.2 Pin Attributes

表 4-1 describes the terminal characteristics and the signals multiplexed on each ball.

表 4-1. Pin Attributes

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE [7]	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABL E [14]	IO Daisy Chain [15]
P17	CAP_VDDAR_CORE0	CAP_VDDAR_CORE0		CAP										
V17	CAP_VDDAR_CORE1	CAP_VDDAR_CORE1		CAP										
W16	CAP_VDDAR_CORE2	CAP_VDDAR_CORE2		CAP										
M14	CAP_VDDAR_CORE3	CAP_VDDAR_CORE3		CAP										
L15	CAP_VDDAR_CORE4	CAP_VDDAR_CORE4		CAP										
U10	CAP_VDDAR_MCU	CAP_VDDAR_MCU		CAP										
M12	CAP_VDDAR_MPU0_0	CAP_VDDAR_MPU0_0		CAP										
N12	CAP_VDDAR_MPU0_1	CAP_VDDAR_MPU0_1		CAP										
N18	CAP_VDDAR_MPU1_0	CAP_VDDAR_MPU1_0		CAP										
N15	CAP_VDDAR_MPU1_1	CAP_VDDAR_MPU1_1		CAP										
Y10	CAP_VDDAR_WKUP	CAP_VDDAR_WKUP		CAP										
AA8	CAP_VDDA_1P8_IOLDO_WKU P	CAP_VDDA_1P8_IOLDO_WKUP		CAP										
J17	CAP_VDDA_1P8_SDIO	CAP_VDDA_1P8_SDIO		CAP										
G19	CAP_VDDA_1P8_IOLDO0	CAP_VDDA_1P8_IOLDO0		CAP										
Y19	CAP_VDDA_1P8_IOLDO1	CAP_VDDA_1P8_IOLDO1		CAP										
H18	CAP_VDDSHV_SDIO	CAP_VDDSHV_SDIO		CAP										
V9	CAP_VDD_WKUP	CAP_VDD_WKUP		CAP										
G28	CSI0_RXN0	CSI0_RXN0		I	PD		1.8 V	VDDA_1P8_CSI 0		DPHY	PU/PD			No
H27	CSI0_RXN1	CSI0_RXN1		I	PD		1.8 V	VDDA_1P8_CSI 0		DPHY	PU/PD			No
F26	CSI0_RXN2	CSI0_RXN2		I	PD		1.8 V	VDDA_1P8_CSI 0		DPHY	PU/PD			No
H25	CSI0_RXN3	CSI0_RXN3		I	PD		1.8 V	VDDA_1P8_CSI 0		DPHY	PU/PD			No
G24	CSI0_RXN4	CSI0_RXN4		I	PD		1.8 V	VDDA_1P8_CSI 0		DPHY	PU/PD			No
F28	CSI0_RXP0	CSI0_RXP0		I	PD		1.8 V	VDDA_1P8_CSI 0		DPHY	PU/PD			No
G27	CSI0_RXP1	CSI0_RXP1		I	PD		1.8 V	VDDA_1P8_CSI 0		DPHY	PU/PD			No
G26	CSI0_RXP2	CSI0_RXP2		I	PD		1.8 V	VDDA_1P8_CSI 0		DPHY	PU/PD			No
G25	CSI0_RXP3	CSI0_RXP3		I	PD		1.8 V	VDDA_1P8_CSI 0		DPHY	PU/PD			No
F24	CSI0_RXP4	CSI0_RXP4		I	PD		1.8 V	VDDA_1P8_CSI 0		DPHY	PU/PD			No
A10	DDR_AC0	DDR_AC0		IO	OFF		1.1 V/1.2 V/1.35 V	VDDSDDR		DDR	PU/PD			No

表 4-1. Pin Attributes (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE [7]	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABL E [14]	IO Daisy Chain [15]
D9	DDR_AC1	DDR_AC1		IO	OFF		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
C9	DDR_AC2	DDR_AC2		IO	OFF		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
E9	DDR_AC3	DDR_AC3		IO	OFF		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
A9	DDR_AC4	DDR_AC4		IO	OFF		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
E8	DDR_AC5	DDR_AC5		IO	OFF		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
F8	DDR_AC6	DDR_AC6		IO	OFF		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
C7	DDR_AC7	DDR_AC7		IO	OFF		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
C8	DDR_AC8	DDR_AC8		IO	OFF		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
D7	DDR_AC9	DDR_AC9		IO	OFF		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
E7	DDR_AC10	DDR_AC10		IO	OFF		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
A6	DDR_AC11	DDR_AC11		IO	OFF		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
F7	DDR_AC12	DDR_AC12		IO	OFF		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
D6	DDR_AC13	DDR_AC13		IO	OFF		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
C6	DDR_AC14	DDR_AC14		IO	OFF		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
F6	DDR_AC15	DDR_AC15		IO	OFF		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
E6	DDR_AC16	DDR_AC16		IO	OFF		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
E5	DDR_AC17	DDR_AC17		IO	OFF		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
D8	DDR_AC18	DDR_AC18		IO	OFF		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
D10	DDR_AC19	DDR_AC19		IO	OFF		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
E10	DDR_AC20	DDR_AC20		IO	OFF		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
C10	DDR_AC21	DDR_AC21		IO	OFF		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
F11	DDR_AC22	DDR_AC22		IO	OFF		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
B10	DDR_AC23	DDR_AC23		IO	OFF		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No

表 4-1. Pin Attributes (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE [7]	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABL E [14]	IO Daisy Chain [15]
D11	DDR_AC24	DDR_AC24		IO	OFF		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
B11	DDR_AC25	DDR_AC25		IO	OFF		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
C11	DDR_AC26	DDR_AC26		IO	OFF		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
E11	DDR_AC27	DDR_AC27		IO	OFF		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
E12	DDR_AC28	DDR_AC28		IO	OFF		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
D12	DDR_AC29	DDR_AC29		IO	OFF		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
D5	DDR_ALERTn	DDR_ALERTn		IO	OFF		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
B8	DDR_CK0N	DDR_CK0N		IO	drive 1 (OFF)		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
A8	DDR_CK0P	DDR_CK0P		IO	drive 0 (OFF)		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
B7	DDR_CK1N	DDR_CK1N		IO	drive 1 (OFF)		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
A7	DDR_CK1P	DDR_CK1P		IO	drive 0 (OFF)		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
E1	DDR_DM0	DDR_DM0		IO	OFF		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
C5	DDR_DM1	DDR_DM1		IO	OFF		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
D14	DDR_DM2	DDR_DM2		IO	OFF		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
B17	DDR_DM3	DDR_DM3		IO	OFF		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
A3	DDR_DQ0	DDR_DQ0		IO	OFF		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
B2	DDR_DQ1	DDR_DQ1		IO	OFF		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
C2	DDR_DQ2	DDR_DQ2		IO	OFF		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
D2	DDR_DQ3	DDR_DQ3		IO	OFF		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
E2	DDR_DQ4	DDR_DQ4		IO	OFF		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
G1	DDR_DQ5	DDR_DQ5		IO	OFF		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
F2	DDR_DQ6	DDR_DQ6		IO	OFF		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
F1	DDR_DQ7	DDR_DQ7		IO	OFF		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No

表 4-1. Pin Attributes (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE [7]	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABL E [14]	IO Daisy Chain [15]
E3	DDR_DQ8	DDR_DQ8		IO	OFF		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
C3	DDR_DQ9	DDR_DQ9		IO	OFF		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
D3	DDR_DQ10	DDR_DQ10		IO	OFF		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
B3	DDR_DQ11	DDR_DQ11		IO	OFF		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
D4	DDR_DQ12	DDR_DQ12		IO	OFF		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
C4	DDR_DQ13	DDR_DQ13		IO	OFF		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
B4	DDR_DQ14	DDR_DQ14		IO	OFF		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
B5	DDR_DQ15	DDR_DQ15		IO	OFF		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
E13	DDR_DQ16	DDR_DQ16		IO	OFF		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
C14	DDR_DQ17	DDR_DQ17		IO	OFF		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
B14	DDR_DQ18	DDR_DQ18		IO	OFF		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
A14	DDR_DQ19	DDR_DQ19		IO	OFF		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
E14	DDR_DQ20	DDR_DQ20		IO	OFF		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
B13	DDR_DQ21	DDR_DQ21		IO	OFF		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
C13	DDR_DQ22	DDR_DQ22		IO	OFF		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
D13	DDR_DQ23	DDR_DQ23		IO	OFF		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
D15	DDR_DQ24	DDR_DQ24		IO	OFF		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
C15	DDR_DQ25	DDR_DQ25		IO	OFF		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
E16	DDR_DQ26	DDR_DQ26		IO	OFF		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
E15	DDR_DQ27	DDR_DQ27		IO	OFF		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
D16	DDR_DQ28	DDR_DQ28		IO	OFF		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
B16	DDR_DQ29	DDR_DQ29		IO	OFF		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
C16	DDR_DQ30	DDR_DQ30		IO	OFF		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No

表 4-1. Pin Attributes (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE [7]	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABL E [14]	IO Daisy Chain [15]
A17	DDR_DQ31	DDR_DQ31		IO	OFF		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
C1	DDR_DQS0N	DDR_DQS0N		IO	OFF		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
D1	DDR_DQS0P	DDR_DQS0P		IO	OFF		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
A4	DDR_DQS1N	DDR_DQS1N		IO	OFF		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
A5	DDR_DQS1P	DDR_DQS1P		IO	OFF		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
A12	DDR_DQS2N	DDR_DQS2N		IO	OFF		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
A13	DDR_DQS2P	DDR_DQS2P		IO	OFF		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
A16	DDR_DQS3N	DDR_DQS3N		IO	OFF		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
A15	DDR_DQS3P	DDR_DQS3P		IO	OFF		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
B19	DDR_ECC_D0	DDR_ECC_D0		IO	OFF		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
B18	DDR_ECC_D1	DDR_ECC_D1		IO	OFF		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
C18	DDR_ECC_D2	DDR_ECC_D2		IO	OFF		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
D18	DDR_ECC_D3	DDR_ECC_D3		IO	OFF		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
E18	DDR_ECC_D4	DDR_ECC_D4		IO	OFF		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
E17	DDR_ECC_D5	DDR_ECC_D5		IO	OFF		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
D17	DDR_ECC_D6	DDR_ECC_D6		IO	OFF		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
C17	DDR_ECC_DM	DDR_ECC_DM		IO	OFF		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
A18	DDR_ECC_DQSN	DDR_ECC_DQSN		IO	OFF		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
A19	DDR_ECC_DQSP	DDR_ECC_DQSP		IO	OFF		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
F16	DDR_FS_RESETn	DDR_FS_RESETn		IO	drive 0 (OFF)		1.1 V/1.2 V/1.35 V	VDDS_DDR		LVC MOS	PD			No
A11	DDR_RESETn	DDR_RESETn		IO	drive 0 (OFF)		1.1 V/1.2 V/1.35 V	VDDS_DDR		DDR	PU/PD			No
F12	DDR_VREF0	DDR_VREF0		A			0.5*VDDS_DDR	VDDS_DDR		DDR				No
F15	DDR_VREF_ZQ	DDR_VREF_ZQ		A				VDDS_DDR		DDR				No

表 4-1. Pin Attributes (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE [7]	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABLE [14]	IO Daisy Chain [15]
F13	DDR_VTP	DDR_VTP		A			1.1 V/1.2 V/1.35 V	VDDSDR		DDR				No
D21	ECAP0_IN_APWM_OUT	ECAP0_IN_APWM_OUT	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD	0	0/1	Yes
		SYNC0_OUT	1	O										
		CPTS0_RFT_CLK	2	I								0		
		GPIO1_86	7	IO								0		
AA2	EMU0	EMU0	0	IO	PU	0	1.8 V/3.3 V	VDDSHV0_WKUP	Yes	LVCMOS	PU/PD		1/1	Yes
AA1	EMU1	EMU1	0	IO	PU	0	1.8 V/3.3 V	VDDSHV0_WKUP	Yes	LVCMOS	PU/PD		1/1	Yes
A22	EXT_REFCLK1	EXT_REFCLK1	0	I	OFF	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD	0	0/1	Yes
		SYNC1_OUT	1	O										
		GPIO1_87	7	IO								0		
P25	GPMC0_ADVn_ALE	GPMC0_ADVn_ALE	0	O	OFF	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD		1/1	Yes
		VOUT1_DATA17	1	O										
		GPIO0_17	7	IO								0		
		BOOTMODE16	Bootstrap	I								0		
R28	GPMC0_CLK	GPMC0_CLK	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD	0	0/1	Yes
		VOUT1_DATA16	1	O										
		VIN0_PCLK	2	I								0		
		GPIO0_16	7	IO								0		
T24	GPMC0_DIR	GPMC0_DIR	0	O	OFF	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD		0/1	Yes
		VOUT1_HSYNC	1	O										
		VIN0_DATA8	2	I								0		
		PRG2_PWM1_B0	3	IO								1		
		PRG2_IEP1_EDC_SYNC_OUT0	4	O										
		TIMER_IO6	5	IO								0		
		PRG2_IEP0_EDIO_DATA_IN_OUT29	6	IO								0		
		GPIO0_25	7	IO								0		
P26	GPMC0_OEn_REn	GPMC0_OEn_REn	0	O	OFF	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD		1/1	Yes
		VOUT1_DATA18	1	O										
		GPIO0_18	7	IO								0		
		BOOTMODE17	Bootstrap	I								0		
U28	GPMC0_WEn	GPMC0_WEn	0	O	OFF	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD		1/1	Yes
		VOUT1_DATA19	1	O										
		GPIO0_19	7	IO								0		
		BOOTMODE18	Bootstrap	I								0		

表 4-1. Pin Attributes (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE [7]	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABL E [14]	IO Daisy Chain [15]
T25	GPMC0_WPn	GPMC0_WPn	0	O	OFF	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD		0/1	Yes
		VOUT1_VSYNC	1	O										
		GPIO0_24	7	IO								0		
M27	GPMC0_AD0	GPMC0_AD0	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD	0	1/1	Yes
		VOUT1_DATA0	1	O										
		VIN0_DATA12	2	I								0		
		GPIO0_0	7	IO								0		
		BOOTMODE00	Bootstrap	I								0		
M23	GPMC0_AD1	GPMC0_AD1	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD	0	1/1	Yes
		VOUT1_DATA1	1	O										
		VIN0_DATA13	2	I								0		
		GPIO0_1	7	IO								0		
		BOOTMODE01	Bootstrap	I								0		
M28	GPMC0_AD2	GPMC0_AD2	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD	0	1/1	Yes
		VOUT1_DATA2	1	O										
		VIN0_DATA14	2	I								0		
		GPIO0_2	7	IO								0		
		BOOTMODE02	Bootstrap	I								0		
M24	GPMC0_AD3	GPMC0_AD3	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD	0	1/1	Yes
		VOUT1_DATA3	1	O										
		VIN0_DATA15	2	I								0		
		GPIO0_3	7	IO								0		
		BOOTMODE03	Bootstrap	I								0		
N24	GPMC0_AD4	GPMC0_AD4	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD	0	1/1	Yes
		VOUT1_DATA4	1	O										
		GPIO0_4	7	IO								0		
		BOOTMODE04	Bootstrap	I								0		
N27	GPMC0_AD5	GPMC0_AD5	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD	0	1/1	Yes
		VOUT1_DATA5	1	O										
		GPIO0_5	7	IO								0		
		BOOTMODE05	Bootstrap	I								0		
N28	GPMC0_AD6	GPMC0_AD6	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD	0	1/1	Yes
		VOUT1_DATA6	1	O										
		GPIO0_6	7	IO								0		
		BOOTMODE06	Bootstrap	I								0		

表 4-1. Pin Attributes (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE [7]	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABL E [14]	IO Daisy Chain [15]
M25	GPMC0_AD7	GPMC0_AD7	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD	0	1/1	Yes
		VOUT1_DATA7	1	O										
		GPIO0_7	7	IO								0		
		BOOTMODE07	Bootstrap	I								0		
N23	GPMC0_AD8	GPMC0_AD8	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD	0	1/1	Yes
		VOUT1_DATA8	1	O										
		VIN0_DATA0	2	I								0		
		PRG2_PRU0_GPO12	3	IO								0		
		PRG2_PRU0_GPI12	4	I								0		
		PRG2_PWM2_A0	5	IO								0		
		GPIO0_8	7	IO								0		
		BOOTMODE08	Bootstrap	I								0		
												0		
M26	GPMC0_AD9	GPMC0_AD9	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD	0	1/1	Yes
		VOUT1_DATA9	1	O										
		VIN0_DATA1	2	I								0		
		PRG2_PRU0_GPO13	3	IO								0		
		PRG2_PRU0_GPI13	4	I								0		
		PRG2_PWM2_B0	5	IO								1		
		GPIO0_9	7	IO								0		
		BOOTMODE09	Bootstrap	I								0		
												0		
P28	GPMC0_AD10	GPMC0_AD10	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD	0	1/1	Yes
		VOUT1_DATA10	1	O										
		VIN0_DATA2	2	I								0		
		PRG2_PRU0_GPO14	3	IO								0		
		PRG2_PRU0_GPI14	4	I								0		
		PRG2_PWM0_TZ_IN	6	I								0		
		GPIO0_10	7	IO								0		
		BOOTMODE10	Bootstrap	I								0		
P27	GPMC0_AD11	GPMC0_AD11	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD	0	1/1	Yes
		VOUT1_DATA11	1	O										
		VIN0_DATA3	2	I								0		
		PRG2_PRU0_GPO15	3	IO								0		
		PRG2_PRU0_GPI15	4	I								0		
		PRG2_PWM2_A1	5	IO								0		
		GPIO0_11	7	IO								0		
		BOOTMODE11	Bootstrap	I								0		

表 4-1. Pin Attributes (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE [7]	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABLE [14]	IO Daisy Chain [15]
N26	GPMC0_AD12	GPMC0_AD12	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD	0	1/1	Yes
		VOUT1_DATA12	1	O										
		VIN0_DATA4	2	I								0		
		PRG2_PRU1_GPO12	3	IO								0		
		PRG2_PRU1_GPI12	4	I								0		
		PRG2_PWM2_B1	5	IO								1		
		GPIO0_12	7	IO								0		
		BOOTMODE12	Bootstrap	I								0		
N25	GPMC0_AD13	GPMC0_AD13	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD	0	1/1	Yes
		VOUT1_DATA13	1	O										
		VIN0_DATA5	2	I								0		
		PRG2_PRU1_GPO13	3	IO								0		
		PRG2_PRU1_GPI13	4	I								0		
		PRG2_PWM2_A2	5	IO								0		
		GPIO0_13	7	IO								0		
		BOOTMODE13	Bootstrap	I								0		
P24	GPMC0_AD14	GPMC0_AD14	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD	0	1/1	Yes
		VOUT1_DATA14	1	O										
		VIN0_DATA6	2	I								0		
		PRG2_PRU1_GPO14	3	IO								0		
		PRG2_PRU1_GPI14	4	I								0		
		PRG2_PWM0_TZ_OUT	6	O										
		GPIO0_14	7	IO								0		
		BOOTMODE14	Bootstrap	I								0		
R27	GPMC0_AD15	GPMC0_AD15	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD	0	1/1	Yes
		VOUT1_DATA15	1	O										
		VIN0_DATA7	2	I								0		
		PRG2_PRU1_GPO15	3	IO								0		
		PRG2_PRU1_GPI15	4	I								0		
		PRG2_PWM2_B2	5	IO								1		
		GPIO0_15	7	IO								0		
		BOOTMODE15	Bootstrap	I								0		
T28	GPMC0_BE0n_CLE	GPMC0_BE0n_CLE	0	O	OFF	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD		0/1	Yes
		VOUT1_DATA20	1	O										
		GPIO0_20	7	IO								0		

表 4-1. Pin Attributes (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE [7]	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABLE [14]	IO Daisy Chain [15]
P23	GPMC0_BE1n	GPMC0_BE1n	0	O	OFF	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD		0/1	Yes
		VOUT1_DATA21	1	O										
		VIN0_HD	2	I								0		
		PRG2_PRU0_GPO17	3	IO								0		
		PRG2_PRU0_GPI17	4	I								0		
		TIMER_IO2	5	IO								0		
		PRG2_PWM2_TZ_IN	6	I								0		
		GPIO0_21	7	IO								0		
R24	GPMC0_CSn0	GPMC0_CSn0	0	O	OFF	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD		0/1	Yes
		VOUT1_PCLK	1	O										
		GPIO0_26	7	IO								0		
T23	GPMC0_CSn1	GPMC0_CSn1	0	O	OFF	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD		0/1	Yes
		VOUT1_DE	1	O										
		VIN0_DATA9	2	I								0		
		PRG2_PRU1_GPO17	3	IO								0		
		PRG2_PRU1_GPI17	4	I								0		
		TIMER_IO7	5	IO								0		
		PRG2_PWM2_TZ_OUT	6	O										
		GPIO0_27	7	IO								0		
R25	GPMC0_CSn2	GPMC0_CSn2	0	O	OFF	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD		0/1	Yes
		VOUT1_EXTPCLKIN	1	I								0		
		VIN0_DATA10	2	I								0		
		GPMC0_A27	3	OZ										
		PRG2_IEP1_EDC_LATCH_IN1	4	I								0		
		I2C2_SDA	5	IOD								1		
		PRG2_IEP0_EDIO_DATA_IN_OUT30	6	IO								0		
		GPIO0_28	7	IO								0		
T27	GPMC0_CSn3	GPMC0_CSn3	0	O	OFF	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD		0/1	Yes
		VIN0_DATA11	2	I								0		
		GPMC0_A26	3	OZ										
		PRG2_IEP1_EDC_SYNC_OUT1	4	O										
		I2C2_SCL	5	IOD								1		
		PRG2_IEP0_EDIO_DATA_IN_OUT31	6	IO								0		
		GPIO0_29	7	IO								0		
R26	GPMC0_WAIT0	GPMC0_WAIT0	0	I	OFF	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD	1	0/1	Yes
		VOUT1_DATA22	1	O										
		GPIO0_22	7	IO								0		

表 4-1. Pin Attributes (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE [7]	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABLE [14]	IO Daisy Chain [15]
R23	GPMC0_WAIT1	GPMC0_WAIT1	0	I	OFF	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD	1	0/1	Yes
		VOUT1_DATA23	1	O										
		VIN0_VD	2	I								0		
		PRG2_PWM1_A0	3	IO								0		
		PRG2_IEP1_EDC_LATCH_IN0	4	I								0		
		TIMER_IO3	5	IO								0		
		PRG2_IEP0_EDIO_DATA_IN_OUT28	6	IO								0		
		GPIO0_23	7	IO								0		
D20	I2C0_SCL	I2C0_SCL	0	IOD	OFF	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS-FS	PU/PD	1	1/1	Yes
C21	I2C0_SDA	I2C0_SDA	0	IOD	OFF	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS-FS	PU/PD	1	1/1	Yes
B21	I2C1_SCL	I2C1_SCL	0	IOD	OFF	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS-FS	PU/PD	1	1/1	Yes
		CPTS0_HW1TSPUSH	1	I								0		
E21	I2C1_SDA	I2C1_SDA	0	IOD	OFF	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS-FS	PU/PD	1	1/1	Yes
		CPTS0_HW2TSPUSH	1	I								0		
K2	MCU_ADC0_REFN	MCU_ADC0_REFN		A			1.8 V	VDDA_ADC_MC U		Analog				No
K3	MCU_ADC0_REFP	MCU_ADC0_REFP		A			1.8 V	VDDA_ADC_MC U		Analog				No
H3	MCU_ADC1_REFN	MCU_ADC1_REFN		A			1.8 V	VDDA_ADC_MC U		Analog				No
H2	MCU_ADC1_REFP	MCU_ADC1_REFP		A			1.8 V	VDDA_ADC_MC U		Analog				No
K5	MCU_ADC0_AIN0	MCU_ADC0_AIN0		A			1.8 V	VDDA_ADC_MC U		Analog				No
J3	MCU_ADC0_AIN1	MCU_ADC0_AIN1		A			1.8 V	VDDA_ADC_MC U		Analog				No
J1	MCU_ADC0_AIN2	MCU_ADC0_AIN2		A			1.8 V	VDDA_ADC_MC U		Analog				No
J5	MCU_ADC0_AIN3	MCU_ADC0_AIN3		A			1.8 V	VDDA_ADC_MC U		Analog				No
K4	MCU_ADC0_AIN4	MCU_ADC0_AIN4		A			1.8 V	VDDA_ADC_MC U		Analog				No
J4	MCU_ADC0_AIN5	MCU_ADC0_AIN5		A			1.8 V	VDDA_ADC_MC U		Analog				No
J2	MCU_ADC0_AIN6	MCU_ADC0_AIN6		A			1.8 V	VDDA_ADC_MC U		Analog				No
J6	MCU_ADC0_AIN7	MCU_ADC0_AIN7		A			1.8 V	VDDA_ADC_MC U		Analog				No
F4	MCU_ADC1_AIN0	MCU_ADC1_AIN0		A			1.8 V	VDDA_ADC_MC U		Analog				No

表 4-1. Pin Attributes (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE [7]	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABL E [14]	IO Daisy Chain [15]
G6	MCU_ADC1_AIN1	MCU_ADC1_AIN1		A			1.8 V	VDDA_ADC_MC U		Analog				No
G4	MCU_ADC1_AIN2	MCU_ADC1_AIN2		A			1.8 V	VDDA_ADC_MC U		Analog				No
H5	MCU_ADC1_AIN3	MCU_ADC1_AIN3		A			1.8 V	VDDA_ADC_MC U		Analog				No
F5	MCU_ADC1_AIN4	MCU_ADC1_AIN4		A			1.8 V	VDDA_ADC_MC U		Analog				No
G5	MCU_ADC1_AIN5	MCU_ADC1_AIN5		A			1.8 V	VDDA_ADC_MC U		Analog				No
G3	MCU_ADC1_AIN6	MCU_ADC1_AIN6		A			1.8 V	VDDA_ADC_MC U		Analog				No
H4	MCU_ADC1_AIN7	MCU_ADC1_AIN7		A			1.8 V	VDDA_ADC_MC U		Analog				No
V5	MCU_BYP_POR	MCU_BYP_POR		I	OFF		1.8 V/3.3 V	VDDSHV0_WKU P	Yes	LVC MOS				No
AD8	MCU_I2C0_SCL	MCU_I2C0_SCL	0	IOD	OFF	0	1.8 V/3.3 V	VDDSHV0_WKU P	Yes	I2C OPEN DRAIN		1	1/0	Yes
AD7	MCU_I2C0_SDA	MCU_I2C0_SDA	0	IOD	OFF	0	1.8 V/3.3 V	VDDSHV0_WKU P	Yes	I2C OPEN DRAIN		1	1/0	Yes
W2	MCU_MCAN0_RX	MCU_MCAN0_RX	0	I	OFF	7	1.8 V/3.3 V	VDDSHV0_WKU P	Yes	LVC MOS	PU/PD	0	0/1	Yes
		WKUP_GPIO0_55	7	IO								0		
W1	MCU_MCAN0_TX	MCU_MCAN0_TX	0	O	OFF	7	1.8 V/3.3 V	VDDSHV0_WKU P	Yes	LVC MOS	PU/PD	0	0/1	Yes
		WKUP_GPIO0_54	7	IO								0		
L1	MCU_MDIO0_MDC	MCU_MDIO0_MDC	0	O	OFF	7	1.8 V/3.3 V	VDDSHV2_WKU P	Yes	LVC MOS	PU/PD		0/1	Yes
		WKUP_GPIO0_47	7	IO								0		
L4	MCU_MDIO0_MDIO	MCU_MDIO0_MDIO	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV2_WKU P	Yes	LVC MOS	PU/PD	0	0/1	Yes
		WKUP_GPIO0_46	7	IO								0		
V1	MCU_OSPI0_CLK	MCU_OSPI0_CLK	0	O	OFF	7	1.8 V/3.3 V	VDDSHV1_WKU P	Yes	LVC MOS	PU/PD		0/1	Yes
		MCU_HYPERBUS0_CK	1	O										
		WKUP_GPIO0_12	7	IO								0		
U2	MCU_OSPI0_DQS	MCU_OSPI0_DQS	0	I	OFF	7	1.8 V/3.3 V	VDDSHV1_WKU P	Yes	LVC MOS	PU/PD	0	0/1	Yes
		MCU_HYPERBUS0_RWDS	1	IO								0		
		WKUP_GPIO0_14	7	IO								0		
U1	MCU_OSPI0_LBCLKO	MCU_OSPI0_LBCLKO	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV1_WKU P	Yes	LVC MOS	PU/PD		0/1	Yes
		MCU_HYPERBUS0_CK _n	1	O										
		WKUP_GPIO0_13	7	IO								0		
T1	MCU_OSPI1_CLK	MCU_OSPI1_CLK	0	O	OFF	7	1.8 V/3.3 V	VDDSHV1_WKU P	Yes	LVC MOS	PU/PD		0/1	Yes
		WKUP_GPIO0_25	7	IO								0		

表 4-1. Pin Attributes (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE [7]	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABL E [14]	IO Daisy Chain [15]
P2	MCU_OSPI1_DQS	MCU_OSPI1_DQS	0	I	OFF	7	1.8 V/3.3 V	VDDSHV1_WKU P	Yes	LVCMOS	PU/PD	0	0/1	Yes
		MCU_OSPI0_CS _n 3	1	O										
		MCU_HYPERBUS0_INT _n	2	I								1		
		WKUP_GPIO0_27	7	IO								0		
R1	MCU_OSPI1_LBCLKO	MCU_OSPI1_LBCLKO	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV1_WKU P	Yes	LVCMOS	PU/PD	0	0/1	Yes
		MCU_OSPI0_CS _n 2	1	O										
		MCU_HYPERBUS0_RESE _T _n	2	I								1		
		WKUP_GPIO0_26	7	IO								0		
R4	MCU_OSPI0_CS _n 0	MCU_OSPI0_CS _n 0	0	O	OFF	7	1.8 V/3.3 V	VDDSHV1_WKU P	Yes	LVCMOS	PU/PD		0/1	Yes
		MCU_HYPERBUS0_CS _n 0	1	O										
		WKUP_GPIO0_23	7	IO								0		
R5	MCU_OSPI0_CS _n 1	MCU_OSPI0_CS _n 1	0	O	OFF	7	1.8 V/3.3 V	VDDSHV1_WKU P	Yes	LVCMOS	PU/PD		0/1	Yes
		MCU_HYPERBUS0_RESE _T _n	1	O										
		WKUP_GPIO0_24	7	IO								0		
U4	MCU_OSPI0_D0	MCU_OSPI0_D0	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV1_WKU P	Yes	LVCMOS	PU/PD	0	0/1	Yes
		MCU_HYPERBUS0_DQ0	1	IO								0		
		WKUP_GPIO0_15	7	IO								0		
U5	MCU_OSPI0_D1	MCU_OSPI0_D1	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV1_WKU P	Yes	LVCMOS	PU/PD	0	0/1	Yes
		MCU_HYPERBUS0_DQ1	1	IO								0		
		WKUP_GPIO0_16	7	IO								0		
T2	MCU_OSPI0_D2	MCU_OSPI0_D2	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV1_WKU P	Yes	LVCMOS	PU/PD	0	0/1	Yes
		MCU_HYPERBUS0_DQ2	1	IO								0		
		WKUP_GPIO0_17	7	IO								0		
T3	MCU_OSPI0_D3	MCU_OSPI0_D3	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV1_WKU P	Yes	LVCMOS	PU/PD	0	0/1	Yes
		MCU_HYPERBUS0_DQ3	1	IO								0		
		WKUP_GPIO0_18	7	IO								0		
T4	MCU_OSPI0_D4	MCU_OSPI0_D4	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV1_WKU P	Yes	LVCMOS	PU/PD	0	0/1	Yes
		MCU_HYPERBUS0_DQ4	1	IO								0		
		WKUP_GPIO0_19	7	IO								0		
T5	MCU_OSPI0_D5	MCU_OSPI0_D5	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV1_WKU P	Yes	LVCMOS	PU/PD	0	0/1	Yes
		MCU_HYPERBUS0_DQ5	1	IO								0		
		WKUP_GPIO0_20	7	IO								0		
R2	MCU_OSPI0_D6	MCU_OSPI0_D6	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV1_WKU P	Yes	LVCMOS	PU/PD	0	0/1	Yes
		MCU_HYPERBUS0_DQ6	1	IO								0		
		WKUP_GPIO0_21	7	IO								0		

表 4-1. Pin Attributes (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE [7]	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABL E [14]	IO Daisy Chain [15]
R3	MCU_OSPiO_D7	MCU_OSPiO_D7	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV1_WKU P	Yes	LVCMOS	PU/PD	0	0/1	Yes
		MCU_HYPERBUS0_DQ7	1	IO								0		
		WKUP_GPIO0_22	7	IO								0		
N2	MCU_OSPi1_CSn0	MCU_OSPi1_CSn0	0	O	OFF	7	1.8 V/3.3 V	VDDSHV1_WKU P	Yes	LVCMOS	PU/PD		0/1	Yes
		WKUP_GPIO0_32	7	IO								0		
N3	MCU_OSPi1_CSn1	MCU_OSPi1_CSn1	0	O	OFF	7	1.8 V/3.3 V	VDDSHV1_WKU P	Yes	LVCMOS	PU/PD		0/1	Yes
		MCU_HYPERBUS0_WPn	1	O										
		MCU_TIMER_IO0	2	IO								0		
		MCU_HYPERBUS0_CSn1	3	O										
		MCU_UART0_RTSn	4	O										
		MCU_SPI0_CS2	5	IO								1		
		WKUP_GPIO0_33	7	IO								0		
P3	MCU_OSPi1_D0	MCU_OSPi1_D0	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV1_WKU P	Yes	LVCMOS	PU/PD	0	0/1	Yes
		WKUP_GPIO0_28	7	IO								0		
P4	MCU_OSPi1_D1	MCU_OSPi1_D1	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV1_WKU P	Yes	LVCMOS	PU/PD	0	0/1	Yes
		MCU_UART0_RXD	4	I								1		
		MCU_SPI1_CS1	5	IO								1		
		WKUP_GPIO0_29	7	IO								0		
P5	MCU_OSPi1_D2	MCU_OSPi1_D2	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV1_WKU P	Yes	LVCMOS	PU/PD	0	0/1	Yes
		MCU_UART0_TXD	4	O										
		MCU_SPI1_CS2	5	IO								1		
		WKUP_GPIO0_30	7	IO								0		
P1	MCU_OSPi1_D3	MCU_OSPi1_D3	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV1_WKU P	Yes	LVCMOS	PU/PD	0	0/1	Yes
		MCU_UART0_CTSn	4	I								1		
		MCU_SPI0_CS1	5	IO								1		
		WKUP_GPIO0_31	7	IO								0		
W5	MCU_PORz	MCU_PORz		I	OFF		1.8 V/3.3 V	VDDSHV0_WKU P	Yes	LVCMOS				No
V2	MCU_PORz_OUT	MCU_PORz_OUT	0	O	OFF	0	1.8 V/3.3 V	VDDSHV0_WKU P	Yes	LVCMOS	PU/PD		0/0	No
V3	MCU_RESETSTATz	MCU_RESETSTATz	0	O	OFF	0	1.8 V/3.3 V	VDDSHV0_WKU P	Yes	LVCMOS	PU/PD		0/0	No
W4	MCU_RESETz	MCU_RESETz	0	I	PU	0	1.8 V/3.3 V	VDDSHV0_WKU P	Yes	LVCMOS	PU/PD		1/1	No
M1	MCU_RGMII1_RXC	MCU_RGMII1_RXC	0	I	OFF	7	1.8 V/3.3 V	VDDSHV2_WKU P	Yes	LVCMOS	PU/PD	0	0/1	Yes
		MCU_RMII1_REF_CLK	1	I								0		
		WKUP_GPIO0_41	7	IO								0		

表 4-1. Pin Attributes (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE [7]	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABL E [14]	IO Daisy Chain [15]
N5	MCU_RGMII1_RX_CTL	MCU_RGMII1_RX_CTL	0	I	OFF	7	1.8 V/3.3 V	VDDSHV2_WKU P	Yes	LVCMOS	PU/PD	0	0/1	Yes
		MCU_RMII1_RX_ER	1	I								0		
		WKUP_GPIO0_35	7	IO								0		
N1	MCU_RGMII1_TXC	MCU_RGMII1_TXC	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV2_WKU P	Yes	LVCMOS	PU/PD	0	0/1	Yes
		MCU_RMII1_TX_EN	1	O								0		
		WKUP_GPIO0_40	7	IO								0		
N4	MCU_RGMII1_TX_CTL	MCU_RGMII1_TX_CTL	0	O	OFF	7	1.8 V/3.3 V	VDDSHV2_WKU P	Yes	LVCMOS	PU/PD	0	0/1	Yes
		MCU_RMII1_CRSDV	1	I								0		
		WKUP_GPIO0_34	7	IO								0		
L6	MCU_RGMII1_RD0	MCU_RGMII1_RD0	0	I	OFF	7	1.8 V/3.3 V	VDDSHV2_WKU P	Yes	LVCMOS	PU/PD	0	0/1	Yes
		MCU_RMII1_RXD0	1	I								0		
		WKUP_GPIO0_45	7	IO								0		
M6	MCU_RGMII1_RD1	MCU_RGMII1_RD1	0	I	OFF	7	1.8 V/3.3 V	VDDSHV2_WKU P	Yes	LVCMOS	PU/PD	0	0/1	Yes
		MCU_RMII1_RXD1	1	I								0		
		WKUP_GPIO0_44	7	IO								0		
L5	MCU_RGMII1_RD2	MCU_RGMII1_RD2	0	I	OFF	7	1.8 V/3.3 V	VDDSHV2_WKU P	Yes	LVCMOS	PU/PD	0	0/1	Yes
		WKUP_GPIO0_43	7	IO								0		
L2	MCU_RGMII1_RD3	MCU_RGMII1_RD3	0	I	OFF	7	1.8 V/3.3 V	VDDSHV2_WKU P	Yes	LVCMOS	PU/PD	0	0/1	Yes
		WKUP_GPIO0_42	7	IO								0		
M5	MCU_RGMII1_TD0	MCU_RGMII1_TD0	0	O	OFF	7	1.8 V/3.3 V	VDDSHV2_WKU P	Yes	LVCMOS	PU/PD	0	0/1	Yes
		MCU_RMII1_TXD0	1	O								0		
		WKUP_GPIO0_39	7	IO								0		
M4	MCU_RGMII1_TD1	MCU_RGMII1_TD1	0	O	OFF	7	1.8 V/3.3 V	VDDSHV2_WKU P	Yes	LVCMOS	PU/PD	0	0/1	Yes
		MCU_RMII1_TXD1	1	O								0		
		WKUP_GPIO0_38	7	IO								0		
M3	MCU_RGMII1_TD2	MCU_RGMII1_TD2	0	O	OFF	7	1.8 V/3.3 V	VDDSHV2_WKU P	Yes	LVCMOS	PU/PD	0	0/1	Yes
		WKUP_GPIO0_37	7	IO								0		
M2	MCU_RGMII1_TD3	MCU_RGMII1_TD3	0	O	OFF	7	1.8 V/3.3 V	VDDSHV2_WKU P	Yes	LVCMOS	PU/PD	0	0/1	Yes
		WKUP_GPIO0_36	7	IO								0		
W3	MCU_SAFETY_ERRORn	MCU_SAFETY_ERRORn	0	IO	PD	0	1.8 V/3.3 V	VDDSHV0_WKU P	Yes	LVCMOS	PU/PD	0	1/0	No
Y1	MCU_SPI0_CLK	MCU_SPI0_CLK	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV0_WKU P	Yes	LVCMOS	PU/PD	0	1/1	Yes
		WKUP_GPIO0_48	7	IO								0		
		MCU_BOOTMODE06	Bootstrap	I								0		
Y4	MCU_SPI0_CS0	MCU_SPI0_CS0	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV0_WKU P	Yes	LVCMOS	PU/PD	1	0/1	Yes
		WKUP_GPIO0_51	7	IO								0		

表 4-1. Pin Attributes (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE [7]	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABLE [14]	IO Daisy Chain [15]
Y3	MCU_SPI0_D0	MCU_SPI0_D0	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV0_WKUP	Yes	LVCMOS	PU/PD	0	1/1	Yes
		WKUP_GPIO0_49	7	IO								0		
		MCU_BOOTMODE07	Bootstrap	I								0		
Y2	MCU_SPI0_D1	MCU_SPI0_D1	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV0_WKUP	Yes	LVCMOS	PU/PD	0	1/1	Yes
		WKUP_GPIO0_50	7	IO								0		
		MCU_BOOTMODE05	Bootstrap	I								0		
D24	MMC0_CALPAD	MMC0_CALPAD		A			1.8 V/3.3 V	VDDSHV6		UHS-I (8bit PHY)				No
B25	MMC0_CLK	MMC0_CLK	0	O	PD	7	1.8 V/3.3 V	VDDSHV6		UHS-I (8bit PHY)	PU/PD	1		No
		GPIO1_10	7	O								0		
B27	MMC0_CMD	MMC0_CMD	0	IO	PU	7	1.8 V/3.3 V	VDDSHV6		UHS-I (8bit PHY)	PU/PD	1		No
		GPIO1_11	7	IO								0		
C25	MMC0_DS	MMC0_DS	0	I	PD	7	1.8 V/3.3 V	VDDSHV6		UHS-I (8bit PHY)	PU/PD	1		No
		GPIO1_12	7	I								0		
A23	MMC0_SDCD	MMC0_SDCD	0	I	OFF	7	1.8 V	VDDS_OSC1	Yes	LVCMOS	PU/PD	1	0/1	Yes
		PRG2_IEP0_EDIO_OUTVALID	6	O										
		GPIO1_13	7	IO								0		
B23	MMC0_SDWP	MMC0_SDWP	0	I	OFF	7	1.8 V	VDDS_OSC1	Yes	LVCMOS	PU/PD	1	0/1	Yes
		GPIO1_14	7	IO								0		
F23	MMC1_CALPAD	MMC1_CALPAD		A			1.8 V/3.3 V	VDDSHV7		UHS-I (4bit PHY)				No
C27	MMC1_CLK	MMC1_CLK	0	O	PD	7	1.8 V/3.3 V	VDDSHV7		UHS-I (4bit PHY)	PU/PD	1		No
		GPIO1_77	7	O								0		
C28	MMC1_CMD	MMC1_CMD	0	IO	PU	7	1.8 V/3.3 V	VDDSHV7		UHS-I (4bit PHY)	PU/PD	1		No
		GPIO1_78	7	IO								0		
B24	MMC1_SDCD	MMC1_SDCD	0	I	OFF	7	1.8 V	VDDS_OSC1	Yes	LVCMOS	PU/PD	1	0/1	Yes
		GPIO1_79	7	IO								0		
C24	MMC1_SDWP	MMC1_SDWP	0	I	OFF	7	1.8 V	VDDS_OSC1	Yes	LVCMOS	PU/PD	1	0/1	Yes
		GPIO1_80	7	IO								0		
A26	MMC0_DAT0	MMC0_DAT0	0	IO	PU	7	1.8 V/3.3 V	VDDSHV6		UHS-I (8bit PHY)	PU/PD	1		No
		GPIO1_9	7	IO								0		
E25	MMC0_DAT1	MMC0_DAT1	0	IO	PU	7	1.8 V/3.3 V	VDDSHV6		UHS-I (8bit PHY)	PU/PD	1		No
		GPIO1_8	7	IO								0		
C26	MMC0_DAT2	MMC0_DAT2	0	IO	PU	7	1.8 V/3.3 V	VDDSHV6		UHS-I (8bit PHY)	PU/PD	1		No
		GPIO1_7	7	IO								0		
A25	MMC0_DAT3	MMC0_DAT3	0	IO	PU	7	1.8 V/3.3 V	VDDSHV6		UHS-I (8bit PHY)	PU/PD	1		No
		GPIO1_6	7	IO								0		

表 4-1. Pin Attributes (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE [7]	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABLE [14]	IO Daisy Chain [15]
E24	MMC0_DAT4	MMC0_DAT4	0	IO	PU	7	1.8 V/3.3 V	VDDSHV6		UHS-I (8bit PHY)	PU/PD	1		No
		UART0_RIN	1	I								1		
		EQEP2_S	5	IO								0		
		GPIO1_5	7	IO								0		
A24	MMC0_DAT5	MMC0_DAT5	0	IO	PU	7	1.8 V/3.3 V	VDDSHV6		UHS-I (8bit PHY)	PU/PD	1		No
		UART0_DTRn	1	O										
		EQEP2_I	5	IO								0		
		GPIO1_4	7	IO								0		
B26	MMC0_DAT6	MMC0_DAT6	0	IO	PU	7	1.8 V/3.3 V	VDDSHV6		UHS-I (8bit PHY)	PU/PD	1		No
		UART0_DSRn	1	I								1		
		EQEP2_B	5	I								0		
		GPIO1_3	7	IO								0		
D25	MMC0_DAT7	MMC0_DAT7	0	IO	PU	7	1.8 V/3.3 V	VDDSHV6		UHS-I (8bit PHY)	PU/PD	1		No
		UART0_DCDn	1	I								1		
		EQEP2_A	5	I								0		
		GPIO1_2	7	IO								0		
D28	MMC1_DAT0	MMC1_DAT0	0	IO	PU	7	1.8 V/3.3 V	VDDSHV7		UHS-I (4bit PHY)	PU/PD	1		No
		GPIO1_76	7	IO								0		
E27	MMC1_DAT1	MMC1_DAT1	0	IO	PU	7	1.8 V/3.3 V	VDDSHV7		UHS-I (4bit PHY)	PU/PD	1		No
		GPIO1_75	7	IO								0		
D26	MMC1_DAT2	MMC1_DAT2	0	IO	PU	7	1.8 V/3.3 V	VDDSHV7		UHS-I (4bit PHY)	PU/PD	1		No
		GPIO1_74	7	IO								0		
D27	MMC1_DAT3	MMC1_DAT3	0	IO	PU	7	1.8 V/3.3 V	VDDSHV7		UHS-I (4bit PHY)	PU/PD	1		No
		GPIO1_73	7	IO								0		
F18	NMIn	NMIn	0	I	PU	0	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS-FS	PU/PD	1	1/1	Yes
		PRG2_PWM1_TZ_IN	6	I								0		
L25	OLDIO_CLKN	OLDIO_CLKN		IO	OFF		1.8 V	VDDA_1P8_OL DIO		OLDI_LVD S				No
K25	OLDIO_CLKP	OLDIO_CLKP		IO	OFF		1.8 V	VDDA_1P8_OL DIO		OLDI_LVD S				No
J28	OLDIO_A0N	OLDIO_A0N		IO	OFF		1.8 V	VDDA_1P8_OL DIO		OLDI_LVD S				No
K28	OLDIO_A0P	OLDIO_A0P		IO	OFF		1.8 V	VDDA_1P8_OL DIO		OLDI_LVD S				No
L27	OLDIO_A1N	OLDIO_A1N		IO	OFF		1.8 V	VDDA_1P8_OL DIO		OLDI_LVD S				No
K27	OLDIO_A1P	OLDIO_A1P		IO	OFF		1.8 V	VDDA_1P8_OL DIO		OLDI_LVD S				No
K24	OLDIO_A2N	OLDIO_A2N		IO	OFF		1.8 V	VDDA_1P8_OL DIO		OLDI_LVD S				No

表 4-1. Pin Attributes (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE [7]	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABLE [14]	IO Daisy Chain [15]
J24	OLDIO_A2P	OLDIO_A2P		IO	OFF		1.8 V	VDDA_1P8_OL DIO		OLDI_LVD S				No
J26	OLDIO_A3N	OLDIO_A3N		IO	OFF		1.8 V	VDDA_1P8_OL DIO		OLDI_LVD S				No
K26	OLDIO_A3P	OLDIO_A3P		IO	OFF		1.8 V	VDDA_1P8_OL DIO		OLDI_LVD S				No
C22	OSC1_XI	OSC1_XI		I	OFF		1.8 V	VDDS_OSC1		Analog				No
E22	OSC1_XO	OSC1_XO		O	OFF		1.8 V	VDDS_OSC1		Analog				No
Y5	PMIC_POWER_EN0	PMIC_POWER_EN0	0	O	OFF	0	1.8 V/3.3 V	VDDSHV0_WKU P	Yes	LVC MOS	PU/PD		0/0	No
AA5	PMIC_POWER_EN1	PMIC_POWER_EN1	0	O	OFF	0	1.8 V/3.3 V	VDDSHV0_WKU P	Yes	LVC MOS	PU/PD		0/0	No
E19	PORz	PORz	0	I	OFF	0	1.8 V/3.3 V	VDDSHV0	Yes	LVC MOS				Yes
C19	PORz_OUT	PORz_OUT	0	O	OFF	0	1.8 V/3.3 V	VDDSHV0	Yes	LVC MOS	PU/PD		0/0	Yes
AE28	PRG0_MDIO0_MDC	PRG0_MDIO0_MDC	0	O	OFF	7	1.8 V/3.3 V	VDDSHV3	Yes	LVC MOS	PU/PD		0/1	Yes
		PRG2_PWM1_B2	3	IO								1		
		MCASP2_AXR3	5	IO								0		
		GPIO1_70	7	IO								0		
AE26	PRG0_MDIO0_MDIO	PRG0_MDIO0_MDIO	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV3	Yes	LVC MOS	PU/PD	0	0/1	Yes
		PRG2_PWM1_A2	3	IO								0		
		MCASP2_AXR2	5	IO								0		
		GPIO1_69	7	IO								0		
V24	PRG0_PRU0_GPO0	PRG0_PRU0_GPO0	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV3	Yes	LVC MOS	PU/PD	0	0/1	Yes
		PRG0_PRU0_GPI0	1	I								0		
		PRG0_RGMII1_RD0	2	I								0		
		PRG0_PWM3_A0	3	IO								0		
		MCASP0_ACLKX	5	IO								0		
		GPIO1_29	7	IO								0		
												0		
W25	PRG0_PRU0_GPO1	PRG0_PRU0_GPO1	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV3	Yes	LVC MOS	PU/PD	0	0/1	Yes
		PRG0_PRU0_GPI1	1	I								0		
		PRG0_RGMII1_RD1	2	I								0		
		PRG0_PWM3_B0	3	IO								1		
		MCASP0_AFSX	5	IO								0		
		GPIO1_30	7	IO								0		
												0		

表 4-1. Pin Attributes (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE [7]	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABL E [14]	IO Daisy Chain [15]
W24	PRG0_PRU0_GPO2	PRG0_PRU0_GPO2	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG0_PRU0_GPI2	1	I								0		
		PRG0_RGMII1_RD2	2	I								0		
		PRG0_PWM2_A0	3	IO								0		
		MCASP0_ACLKR	5	IO								0		
		GPIO1_31	7	IO								0		
AA27	PRG0_PRU0_GPO3	PRG0_PRU0_GPO3	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG0_PRU0_GPI3	1	I								0		
		PRG0_RGMII1_RD3	2	I								0		
		PRG0_PWM3_A2	3	IO								0		
		MCASP0_AFSR	5	IO								0		
		GPIO1_32	7	IO								0		
Y24	PRG0_PRU0_GPO4	PRG0_PRU0_GPO4	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG0_PRU0_GPI4	1	I								0		
		PRG0_RGMII1_RX_CTL	2	I								0		
		PRG0_PWM2_B0	3	IO								1		
		MCASP0_AXR0	5	IO								0		
		GPIO1_33	7	IO								0		
V28	PRG0_PRU0_GPO5	PRG0_PRU0_GPO5	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG0_PRU0_GPI5	1	I								0		
		PRG0_PWM3_B2	3	IO								1		
		MCASP0_AXR1	5	IO								0		
		GPIO1_34	7	IO								0		
Y25	PRG0_PRU0_GPO6	PRG0_PRU0_GPO6	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG0_PRU0_GPI6	1	I								0		
		PRG0_RGMII1_RXC	2	I								0		
		PRG0_PWM3_A1	3	IO								0		
		MCASP0_AXR2	5	IO								0		
		GPIO1_35	7	IO								0		
U27	PRG0_PRU0_GPO7	PRG0_PRU0_GPO7	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG0_PRU0_GPI7	1	I								0		
		PRG0_IEP0_EDC_LATCH_IN1	2	I								0		
		PRG0_PWM3_B1	3	IO								1		
		PRG0_ECAP0_SYNC_IN	4	I								0		
		MCASP0_AXR3	5	IO								0		
		GPIO1_36	7	IO								0		

表 4-1. Pin Attributes (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE [7]	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABLE [14]	IO Daisy Chain [15]
V27	PRG0_PRU0_GPO8	PRG0_PRU0_GPO8	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG0_PRU0_GPI8	1	I								0		
		PRG0_PWM2_A1	3	IO								0		
		MCASP0_AXR4	5	IO								0		
		GPIO1_37	7	IO								0		
V26	PRG0_PRU0_GPO9	PRG0_PRU0_GPO9	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG0_PRU0_GPI9	1	I								0		
		PRG0_UART0_CTSn	2	I								1		
		PRG0_PWM3_TZ_IN	3	I								0		
		SPI3_CS1	4	IO								1		
		MCASP0_AXR5	5	IO								0		
		PRG0_IEP0_EDIO_DATA_IN_OUT28	6	IO								0		
		GPIO1_38	7	IO								0		
U25	PRG0_PRU0_GPO10	PRG0_PRU0_GPO10	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG0_PRU0_GPI10	1	I								0		
		PRG0_UART0_RTSn	2	O										
		PRG0_PWM2_B1	3	IO								1		
		SPI3_CS2	4	IO								1		
		MCASP0_AXR6	5	IO								0		
		PRG0_IEP0_EDIO_DATA_IN_OUT29	6	IO								0		
		GPIO1_39	7	IO								0		
AB25	PRG0_PRU0_GPO11	PRG0_PRU0_GPO11	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG0_PRU0_GPI11	1	I								0		
		PRG0_RGMII1_TX_CTL	2	O										
		PRG0_PWM3_TZ_OUT	3	O										
		MCASP0_AXR7	5	IO								0		
AD27	PRG0_PRU0_GPO12	PRG0_PRU0_GPO12	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG0_PRU0_GPI12	1	I								0		
		PRG0_RGMII1_TD0	2	O										
		PRG0_PWM0_A0	3	IO								0		
		MCASP0_AXR8	5	IO								0		
		GPIO1_41	7	IO								0		

表 4-1. Pin Attributes (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE [7]	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABL E [14]	IO Daisy Chain [15]
AC26	PRG0_PRU0_GPO13	PRG0_PRU0_GPO13	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG0_PRU0_GPI13	1	I								0		
		PRG0_RGMII1_TD1	2	O										
		PRG0_PWM0_B0	3	IO								1		
		MCASP0_AXR9	5	IO								0		
		GPIO1_42	7	IO								0		
AD26	PRG0_PRU0_GPO14	PRG0_PRU0_GPO14	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG0_PRU0_GPI14	1	I								0		
		PRG0_RGMII1_TD2	2	O										
		PRG0_PWM0_A1	3	IO								0		
		MCASP0_AXR10	5	IO								0		
		GPIO1_43	7	IO								0		
AA24	PRG0_PRU0_GPO15	PRG0_PRU0_GPO15	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG0_PRU0_GPI15	1	I								0		
		PRG0_RGMII1_TD3	2	O										
		PRG0_PWM0_B1	3	IO								1		
		MCASP0_AXR11	5	IO								0		
		GPIO1_44	7	IO								0		
AD28	PRG0_PRU0_GPO16	PRG0_PRU0_GPO16	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG0_PRU0_GPI16	1	I								0		
		PRG0_RGMII1_TXC	2	IO								0		
		PRG0_PWM0_A2	3	IO								0		
		MCASP0_AXR12	5	IO								0		
		MCASP1_AHCLKR	6	IO								0		
		GPIO1_45	7	IO								0		
U26	PRG0_PRU0_GPO17	PRG0_PRU0_GPO17	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG0_PRU0_GPI17	1	I								0		
		PRG0_IEP0_EDC_SYNC_OUT1	2	O										
		PRG0_PWM0_B2	3	IO								1		
		PRG0_ECAP0_SYNC_OUT	4	O										
		MCASP0_AXR13	5	IO								0		
		MCASP1_AHCLKX	6	IO								0		
		GPIO1_46	7	IO								0		

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表 4-1. Pin Attributes (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE [7]	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABL E [14]	IO Daisy Chain [15]
V25	PRG0_PRU0_GPO18	PRG0_PRU0_GPO18	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG0_PRU0_GPI18	1	I								0		
		PRG0_IEP0_EDC_LATCH_IN0	2	I								0		
		PRG0_PWM0_TZ_IN	3	I								0		
		PRG0_ECAP0_IN_APWM_OUT	4	IO								0		
		MCASP0_AXR14	5	IO								0		
		MCASP2_AHCLKR	6	IO								0		
		GPIO1_47	7	IO								0		
U24	PRG0_PRU0_GPO19	PRG0_PRU0_GPO19	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG0_PRU0_GPI19	1	I								0		
		PRG0_IEP0_EDC_SYNC_OUT0	2	O										
		PRG0_PWM0_TZ_OUT	3	O										
		MCASP0_AXR15	5	IO								0		
		MCASP2_AHCLKX	6	IO								0		
		GPIO1_48	7	IO								0		
AB28	PRG0_PRU1_GPO0	PRG0_PRU1_GPO0	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG0_PRU1_GPI0	1	I								0		
		PRG0_RGMII2_RD0	2	I								0		
		MCASP1_ACLKX	5	IO								0		
		GPIO1_49	7	IO								0		
AC28	PRG0_PRU1_GPO1	PRG0_PRU1_GPO1	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG0_PRU1_GPI1	1	I								0		
		PRG0_RGMII2_RD1	2	I								0		
		MCASP1_AFSX	5	IO								0		
		GPIO1_50	7	IO								0		
AC27	PRG0_PRU1_GPO2	PRG0_PRU1_GPO2	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG0_PRU1_GPI2	1	I								0		
		PRG0_RGMII2_RD2	2	I								0		
		PRG0_PWM2_A2	3	IO								0		
		MCASP1_ACLKR	5	IO								0		
		GPIO1_51	7	IO								0		
AB26	PRG0_PRU1_GPO3	PRG0_PRU1_GPO3	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG0_PRU1_GPI3	1	I								0		
		PRG0_RGMII2_RD3	2	I								0		
		EQEP0_A	4	I								0		
		MCASP1_AFSR	5	IO								0		
		GPIO1_52	7	IO								0		

表 4-1. Pin Attributes (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE [7]	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABL E [14]	IO Daisy Chain [15]
AA25	PRG0_PRU1_GPO4	PRG0_PRU1_GPO4	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG0_PRU1_GPI4	1	I								0		
		PRG0_RGMII2_RX_CTL	2	I								0		
		PRG0_PWM2_B2	3	IO								1		
		EQEP0_B	4	I								0		
		MCASP1_AXR0	5	IO								0		
		MCASP0_AHCLKR	6	IO								0		
		GPIO1_53	7	IO								0		
U23	PRG0_PRU1_GPO5	PRG0_PRU1_GPO5	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG0_PRU1_GPI5	1	I								0		
		EQEP0_S	4	IO								0		
		MCASP1_AXR1	5	IO								0		
		MCASP0_AHCLKX	6	IO								0		
		GPIO1_54	7	IO								0		
AB27	PRG0_PRU1_GPO6	PRG0_PRU1_GPO6	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG0_PRU1_GPI6	1	I								0		
		PRG0_RGMII2_RXC	2	I								0		
		MCASP1_AXR2	5	IO								0		
		GPIO1_55	7	IO								0		
W28	PRG0_PRU1_GPO7	PRG0_PRU1_GPO7	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG0_PRU1_GPI7	1	I								0		
		PRG0_IEP1_EDC_LATCH_IN1	2	I								0		
		SPI3_CS0	4	IO								1		
		MCASP1_AXR3	5	IO								0		
		UART2_TXD	6	O										
		GPIO1_56	7	IO								0		
W27	PRG0_PRU1_GPO8	PRG0_PRU1_GPO8	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG0_PRU1_GPI8	1	I								0		
		PRG0_PWM2_TZ_OUT	3	O										
		MCASP1_AXR4	5	IO								0		
		GPIO1_57	7	IO								0		

表 4-1. Pin Attributes (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE [7]	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABL E [14]	IO Daisy Chain [15]
Y28	PRG0_PRU1_GPO9	PRG0_PRU1_GPO9	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG0_PRU1_GPI9	1	I								0		
		PRG0_UART0_RXD	2	I								1		
		SPI3_CS3	4	IO								1		
		MCASP1_AXR5	5	IO								0		
		PRG0_IEP0_EDIO_DATA_IN_OUT30	6	IO								0		
		GPIO1_58	7	IO								0		
AA28	PRG0_PRU1_GPO10	PRG0_PRU1_GPO10	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG0_PRU1_GPI10	1	I								0		
		PRG0_UART0_TXD	2	O										
		PRG0_PWM2_TZ_IN	3	I								0		
		EQEP0_I	4	IO								0		
		MCASP1_AXR6	5	IO								0		
		PRG0_IEP0_EDIO_DATA_IN_OUT31	6	IO								0		
AB24	PRG0_PRU1_GPO11	PRG0_PRU1_GPO11	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG0_PRU1_GPI11	1	I								0		
		PRG0_RGMII2_TX_CTL	2	O										
		MCASP1_AXR7	5	IO								0		
		GPIO1_60	7	IO								0		
AC25	PRG0_PRU1_GPO12	PRG0_PRU1_GPO12	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG0_PRU1_GPI12	1	I								0		
		PRG0_RGMII2_TD0	2	O										
		PRG0_PWM1_A0	3	IO								0		
		MCASP1_AXR8	5	IO								0		
		GPIO1_61	7	IO								0		
AD25	PRG0_PRU1_GPO13	PRG0_PRU1_GPO13	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG0_PRU1_GPI13	1	I								0		
		PRG0_RGMII2_TD1	2	O										
		PRG0_PWM1_B0	3	IO								1		
		MCASP1_AXR9	5	IO								0		
		GPIO1_62	7	IO								0		

表 4-1. Pin Attributes (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE [7]	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABL E [14]	IO Daisy Chain [15]
AD24	PRG0_PRU1_GPO14	PRG0_PRU1_GPO14	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG0_PRU1_GPI14	1	I								0		
		PRG0_RGMII2_TD2	2	O										
		PRG0_PWM1_A1	3	IO								0		
		MCASP2_AFSR	5	IO								0		
		GPIO1_63	7	IO								0		
AE27	PRG0_PRU1_GPO15	PRG0_PRU1_GPO15	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG0_PRU1_GPI15	1	I								0		
		PRG0_RGMII2_TD3	2	O										
		PRG0_PWM1_B1	3	IO								1		
		MCASP2_ACLKR	5	IO								0		
		GPIO1_64	7	IO								0		
AC24	PRG0_PRU1_GPO16	PRG0_PRU1_GPO16	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG0_PRU1_GPI16	1	I								0		
		PRG0_RGMII2_TXC	2	IO								0		
		PRG0_PWM1_A2	3	IO								0		
		MCASP2_AXR0	5	IO								0		
		GPIO1_65	7	IO								0		
Y27	PRG0_PRU1_GPO17	PRG0_PRU1_GPO17	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG0_PRU1_GPI17	1	I								0		
		PRG0_IEP1_EDC_SYNC_OUT1	2	O										
		PRG0_PWM1_B2	3	IO								1		
		SPI3_CLK	4	IO								0		
		MCASP2_AXR1	5	IO								0		
		UART2_RXD	6	I								1		
		GPIO1_66	7	IO								0		
Y26	PRG0_PRU1_GPO18	PRG0_PRU1_GPO18	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG0_PRU1_GPI18	1	I								0		
		PRG0_IEP1_EDC_LATCH_IN0	2	I								0		
		PRG0_PWM1_TZ_IN	3	I								0		
		SPI3_D0	4	IO								0		
		MCASP2_AFSX	5	IO								0		
		UART2_CTSn	6	I								1		
		GPIO1_67	7	IO								0		

ADVANCE INFORMATION

表 4-1. Pin Attributes (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE [7]	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABL E [14]	IO Daisy Chain [15]
W26	PRG0_PRU1_GPO19	PRG0_PRU1_GPO19	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG0_PRU1_GPI19	1	I								0		
		PRG0_IEP1_EDC_SYNC_OUT0	2	O										
		PRG0_PWM1_TZ_OUT	3	O										
		SPI3_D1	4	IO								0		
		MCASP2_ACLKX	5	IO								0		
		UART2_RTSn	6	O										
		GPIO1_68	7	IO								0		
AH18	PRG1_MDIO0_MDC	PRG1_MDIO0_MDC	0	O	OFF	7	1.8 V/3.3 V	VDDSHV4	Yes	LVCMOS	PU/PD		0/1	Yes
		SPI1_CS3	1	IO								1		
		PRG2_PWM1_B1	3	IO								1		
		GPIO1_1	7	IO								0		
AD18	PRG1_MDIO0_MDIO	PRG1_MDIO0_MDIO	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV4	Yes	LVCMOS	PU/PD	0	0/1	Yes
		SPI1_CS2	1	IO								1		
		PRG2_PWM1_A1	3	IO								0		
		GPIO1_0	7	IO								0		
AE22	PRG1_PRU0_GPO0	PRG1_PRU0_GPO0	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV4	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG1_PRU0_GPI0	1	I								0		
		PRG1_RGMII1_RD0	2	I								0		
		PRG1_PWM3_A0	3	IO								0		
		GPIO0_56	7	IO								0		
AG24	PRG1_PRU0_GPO1	PRG1_PRU0_GPO1	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV4	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG1_PRU0_GPI1	1	I								0		
		PRG1_RGMII1_RD1	2	I								0		
		PRG1_PWM3_B0	3	IO								1		
		GPIO0_57	7	IO								0		
AF23	PRG1_PRU0_GPO2	PRG1_PRU0_GPO2	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV4	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG1_PRU0_GPI2	1	I								0		
		PRG1_RGMII1_RD2	2	I								0		
		PRG1_PWM2_A0	3	IO								0		
		GPIO0_58	7	IO								0		
AD21	PRG1_PRU0_GPO3	PRG1_PRU0_GPO3	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV4	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG1_PRU0_GPI3	1	I								0		
		PRG1_RGMII1_RD3	2	I								0		
		PRG1_PWM3_A2	3	IO								0		
		GPIO0_59	7	IO								0		

表 4-1. Pin Attributes (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE [7]	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABL E [14]	IO Daisy Chain [15]
AG23	PRG1_PRU0_GPO4	PRG1_PRU0_GPO4	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV4	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG1_PRU0_GPI4	1	I								0		
		PRG1_RGMII1_RX_CTL	2	I								0		
		PRG1_PWM2_B0	3	IO								1		
		GPIO0_60	7	IO								0		
AF27	PRG1_PRU0_GPO5	PRG1_PRU0_GPO5	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV4	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG1_PRU0_GPI5	1	I								0		
		PRG1_PWM3_B2	3	IO								1		
		GPIO0_61	7	IO								0		
AF22	PRG1_PRU0_GPO6	PRG1_PRU0_GPO6	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV4	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG1_PRU0_GPI6	1	I								0		
		PRG1_RGMII1_RXC	2	I								0		
		PRG1_PWM3_A1	3	IO								0		
		GPIO0_62	7	IO								0		
AG27	PRG1_PRU0_GPO7	PRG1_PRU0_GPO7	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV4	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG1_PRU0_GPI7	1	I								0		
		PRG1_IEP0_EDC_LATCH_IN1	2	I								0		
		PRG1_PWM3_B1	3	IO								1		
		GPIO0_63	7	IO								0		
AF28	PRG1_PRU0_GPO8	PRG1_PRU0_GPO8	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV4	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG1_PRU0_GPI8	1	I								0		
		PRG1_PWM2_A1	3	IO								0		
		GPIO0_64	7	IO								0		
AF26	PRG1_PRU0_GPO9	PRG1_PRU0_GPO9	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV4	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG1_PRU0_GPI9	1	I								0		
		PRG1_UART0_CTSn	2	I								1		
		PRG1_PWM3_TZ_IN	3	I								0		
		SPI2_CS1	4	IO								1		
		PRG1_IEP0_EDIO_DATA_IN_OUT28	6	IO								0		
		GPIO0_65	7	IO								0		
AH25	PRG1_PRU0_GPO10	PRG1_PRU0_GPO10	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV4	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG1_PRU0_GPI10	1	I								0		
		PRG1_UART0_RTSn	2	O										
		PRG1_PWM2_B1	3	IO								1		
		SPI2_CS2	4	IO								1		
		PRG1_IEP0_EDIO_DATA_IN_OUT29	6	IO								0		
		GPIO0_66	7	IO								0		

表 4-1. Pin Attributes (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE [7]	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABL E [14]	IO Daisy Chain [15]
AF21	PRG1_PRU0_GPO11	PRG1_PRU0_GPO11	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV4	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG1_PRU0_GPI11	1	I								0		
		PRG1_RGMII1_TX_CTL	2	O										
		PRG1_PWM3_TZ_OUT	3	O										
		GPIO0_67	7	IO								0		
AH20	PRG1_PRU0_GPO12	PRG1_PRU0_GPO12	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV4	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG1_PRU0_GPI12	1	I								0		
		PRG1_RGMII1_TD0	2	O										
		PRG1_PWM0_A0	3	IO								0		
		GPIO0_68	7	IO								0		
AH21	PRG1_PRU0_GPO13	PRG1_PRU0_GPO13	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV4	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG1_PRU0_GPI13	1	I								0		
		PRG1_RGMII1_TD1	2	O										
		PRG1_PWM0_B0	3	IO								1		
		GPIO0_69	7	IO								0		
AG20	PRG1_PRU0_GPO14	PRG1_PRU0_GPO14	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV4	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG1_PRU0_GPI14	1	I								0		
		PRG1_RGMII1_TD2	2	O										
		PRG1_PWM0_A1	3	IO								0		
		GPIO0_70	7	IO								0		
AD19	PRG1_PRU0_GPO15	PRG1_PRU0_GPO15	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV4	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG1_PRU0_GPI15	1	I								0		
		PRG1_RGMII1_TD3	2	O										
		PRG1_PWM0_B1	3	IO								1		
		GPIO0_71	7	IO								0		
AD20	PRG1_PRU0_GPO16	PRG1_PRU0_GPO16	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV4	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG1_PRU0_GPI16	1	I								0		
		PRG1_RGMII1_TXC	2	IO								0		
		PRG1_PWM0_A2	3	IO								0		
		GPIO0_72	7	IO								0		
AH26	PRG1_PRU0_GPO17	PRG1_PRU0_GPO17	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV4	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG1_PRU0_GPI17	1	I								0		
		PRG1_IEP0_EDC_SYNC_OUT1	2	O										
		PRG1_PWM0_B2	3	IO								1		
		GPIO0_73	7	IO								0		

表 4-1. Pin Attributes (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE [7]	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABL E [14]	IO Daisy Chain [15]
AG25	PRG1_PRU0_GPO18	PRG1_PRU0_GPO18	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV4	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG1_PRU0_GPI18	1	I								0		
		PRG1_IEP0_EDC_LATCH_IN0	2	I								0		
		PRG1_PWM0_TZ_IN	3	I								0		
		GPIO0_74	7	IO								0		
AG26	PRG1_PRU0_GPO19	PRG1_PRU0_GPO19	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV4	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG1_PRU0_GPI19	1	I								0		
		PRG1_IEP0_EDC_SYNC_OUT0	2	O										
		PRG1_PWM0_TZ_OUT	3	O										
		GPIO0_75	7	IO								0		
AH24	PRG1_PRU1_GPO0	PRG1_PRU1_GPO0	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV4	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG1_PRU1_GPI0	1	I								0		
		PRG1_RGMII2_RD0	2	I								0		
		GPIO0_76	7	IO								0		
AH23	PRG1_PRU1_GPO1	PRG1_PRU1_GPO1	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV4	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG1_PRU1_GPI1	1	I								0		
		PRG1_RGMII2_RD1	2	I								0		
		GPIO0_77	7	IO								0		
AG21	PRG1_PRU1_GPO2	PRG1_PRU1_GPO2	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV4	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG1_PRU1_GPI2	1	I								0		
		PRG1_RGMII2_RD2	2	I								0		
		PRG1_PWM2_A2	3	IO								0		
		GPIO0_78	7	IO								0		
AH22	PRG1_PRU1_GPO3	PRG1_PRU1_GPO3	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV4	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG1_PRU1_GPI3	1	I								0		
		PRG1_RGMII2_RD3	2	I								0		
		EQEP1_A	4	I								0		
		GPIO0_79	7	IO								0		
AE21	PRG1_PRU1_GPO4	PRG1_PRU1_GPO4	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV4	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG1_PRU1_GPI4	1	I								0		
		PRG1_RGMII2_RX_CTL	2	I								0		
		PRG1_PWM2_B2	3	IO								1		
		EQEP1_B	4	I								0		
		GPIO0_80	7	IO								0		

表 4-1. Pin Attributes (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE [7]	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABL E [14]	IO Daisy Chain [15]
AC22	PRG1_PRU1_GPO5	PRG1_PRU1_GPO5	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV4	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG1_PRU1_GPI5	1	I								0		
		EQEP1_S	4	IO								0		
		GPIO0_81	7	IO								0		
AG22	PRG1_PRU1_GPO6	PRG1_PRU1_GPO6	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV4	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG1_PRU1_GPI6	1	I								0		
		PRG1_RGMII2_RXC	2	I								0		
		GPIO0_82	7	IO								0		
AD23	PRG1_PRU1_GPO7	PRG1_PRU1_GPO7	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV4	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG1_PRU1_GPI7	1	I								0		
		PRG1_IEP1_EDC_LATCH_IN1	2	I								0		
		SPI2_CS0	4	IO								1		
		UART1_TXD	6	O										
		GPIO0_83	7	IO								0		
AE24	PRG1_PRU1_GPO8	PRG1_PRU1_GPO8	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV4	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG1_PRU1_GPI8	1	I								0		
		PRG1_PWM2_TZ_OUT	3	O										
		GPIO0_84	7	IO								0		
AF25	PRG1_PRU1_GPO9	PRG1_PRU1_GPO9	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV4	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG1_PRU1_GPI9	1	I								0		
		PRG1_UART0_RXD	2	I								1		
		PRG1_IEP0_EDIO_DATA_IN_OUT30	6	IO								0		
		GPIO0_85	7	IO								0		
AF24	PRG1_PRU1_GPO10	PRG1_PRU1_GPO10	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV4	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG1_PRU1_GPI10	1	I								0		
		PRG1_UART0_TXD	2	O										
		PRG1_PWM2_TZ_IN	3	I								0		
		SPI2_CS3	4	IO								1		
		PRG1_IEP0_EDIO_DATA_IN_OUT31	6	IO								0		
		GPIO0_86	7	IO								0		
AC20	PRG1_PRU1_GPO11	PRG1_PRU1_GPO11	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV4	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG1_PRU1_GPI11	1	I								0		
		PRG1_RGMII2_TX_CTL	2	O										
		EQEP1_I	4	IO								0		
		GPIO0_87	7	IO								0		

表 4-1. Pin Attributes (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE [7]	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABL E [14]	IO Daisy Chain [15]
AE20	PRG1_PRU1_GPO12	PRG1_PRU1_GPO12	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV4	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG1_PRU1_GPI12	1	I								0		
		PRG1_RGMII2_TD0	2	O										
		PRG1_PWM1_A0	3	IO								0		
		GPIO0_88	7	IO								0		
AF19	PRG1_PRU1_GPO13	PRG1_PRU1_GPO13	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV4	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG1_PRU1_GPI13	1	I								0		
		PRG1_RGMII2_TD1	2	O										
		PRG1_PWM1_B0	3	IO								1		
		GPIO0_89	7	IO								0		
AH19	PRG1_PRU1_GPO14	PRG1_PRU1_GPO14	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV4	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG1_PRU1_GPI14	1	I								0		
		PRG1_RGMII2_TD2	2	O										
		PRG1_PWM1_A1	3	IO								0		
		GPIO0_90	7	IO								0		
AG19	PRG1_PRU1_GPO15	PRG1_PRU1_GPO15	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV4	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG1_PRU1_GPI15	1	I								0		
		PRG1_RGMII2_TD3	2	O										
		PRG1_PWM1_B1	3	IO								1		
		GPIO0_91	7	IO								0		
AE19	PRG1_PRU1_GPO16	PRG1_PRU1_GPO16	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV4	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG1_PRU1_GPI16	1	I								0		
		PRG1_RGMII2_TXC	2	IO								0		
		PRG1_PWM1_A2	3	IO								0		
		GPIO0_92	7	IO								0		
AE23	PRG1_PRU1_GPO17	PRG1_PRU1_GPO17	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV4	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG1_PRU1_GPI17	1	I								0		
		PRG1_IEP1_EDC_SYNC_OUT1	2	O										
		PRG1_PWM1_B2	3	IO								1		
		SPI2_CLK	4	IO								0		
		PRG1_ECAP0_SYNC_OUT	5	O										
		UART1_RXD	6	I								1		
		GPIO0_93	7	IO								0		

表 4-1. Pin Attributes (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE [7]	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABL E [14]	IO Daisy Chain [15]
AD22	PRG1_PRU1_GPO18	PRG1_PRU1_GPO18	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV4	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG1_PRU1_GPI18	1	I								0		
		PRG1_IEP1_EDC_LATCH_IN0	2	I								0		
		PRG1_PWM1_TZ_IN	3	I								0		
		SPI2_D0	4	IO								0		
		PRG1_ECAP0_SYNC_IN	5	I								0		
		UART1_CTSn	6	I								1		
		GPIO0_94	7	IO								0		
AC21	PRG1_PRU1_GPO19	PRG1_PRU1_GPO19	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV4	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG1_PRU1_GPI19	1	I								0		
		PRG1_IEP1_EDC_SYNC_OUT0	2	O										
		PRG1_PWM1_TZ_OUT	3	O										
		SPI2_D1	4	IO								0		
		PRG1_ECAP0_IN_APWM_OUT	5	IO								0		
		UART1_RTSn	6	O										
		GPIO0_95	7	IO								0		
AF18	PRG2_PRU0_GPO0	PRG2_PRU0_GPO0	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV5	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG2_PRU0_GPI0	1	I								0		
		PRG2_RGMII1_RD0	2	I								0		
		GPMC0_A25	3	OZ										
		TRC_CLK	4	O										
		EHRPWM0_SYNCI	5	I								0		
		PRG2_PWM3_A0	6	IO								0		
		GPIO0_30	7	IO								0		
AE18	PRG2_PRU0_GPO1	PRG2_PRU0_GPO1	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV5	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG2_PRU0_GPI1	1	I								0		
		PRG2_RGMII1_RD1	2	I								0		
		GPMC0_A24	3	OZ										
		TRC_CTL	4	O										
		EHRPWM0_SYNCO	5	O										
		SYNC2_OUT	6	O										
		GPIO0_31	7	IO								0		

表 4-1. Pin Attributes (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE [7]	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABLE [14]	IO Daisy Chain [15]
AH17	PRG2_PRU0_GPO2	PRG2_PRU0_GPO2	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV5	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG2_PRU0_GPI2	1	I								0		
		PRG2_RGMII1_RD2	2	I								0		
		GPMC0_A23	3	OZ										
		TRC_DATA0	4	O										
		EHRPWM_TZn_IN0	5	I								0		
		SYNC3_OUT	6	O										
		GPIO0_32	7	IO								0		
AG18	PRG2_PRU0_GPO3	PRG2_PRU0_GPO3	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV5	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG2_PRU0_GPI3	1	I								0		
		PRG2_RGMII1_RD3	2	I								0		
		GPMC0_A22	3	OZ										
		TRC_DATA1	4	O										
		EHRPWM0_A	5	IO								0		
		PRG2_PWM3_B0	6	IO								1		
		GPIO0_33	7	IO								0		
AG17	PRG2_PRU0_GPO4	PRG2_PRU0_GPO4	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV5	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG2_PRU0_GPI4	1	I								0		
		PRG2_RGMII1_RX_CTL	2	I								0		
		GPMC0_A21	3	OZ										
		TRC_DATA2	4	O										
		EHRPWM0_B	5	IO								0		
		PRG2_PWM0_A0	6	IO								0		
		GPIO0_34	7	IO								0		
AF17	PRG2_PRU0_GPO5	PRG2_PRU0_GPO5	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV5	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG2_PRU0_GPI5	1	I								0		
		PRG2_RGMII1_RXC	2	I								0		
		GPMC0_A20	3	OZ										
		TRC_DATA3	4	O										
		EHRPWM1_A	5	IO								0		
		PRG2_PWM3_A1	6	IO								0		
		GPIO0_35	7	IO								0		

表 4-1. Pin Attributes (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE [7]	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABL E [14]	IO Daisy Chain [15]
AE17	PRG2_PRU0_GPO6	PRG2_PRU0_GPO6	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV5	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG2_PRU0_GPI6	1	I								0		
		PRG2_RGMII1_TX_CTL	2	O										
		GPMC0_A19	3	OZ										
		TRC_DATA4	4	O										
		EHRPWM1_B	5	IO								0		
		PRG2_PWM3_B1	6	IO								1		
		GPIO0_36	7	IO								0		
AC19	PRG2_PRU0_GPO7	PRG2_PRU0_GPO7	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV5	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG2_PRU0_GPI7	1	I								0		
		PRG2_MDIO0_MDIO	2	IO								0		
		GPMC0_A18	3	OZ										
		TRC_DATA5	4	O										
		EHRPWM_TZn_IN1	5	I								0		
		EHRPWM_SOC_A	6	O										
		GPIO0_37	7	IO								0		
AH16	PRG2_PRU0_GPO8	PRG2_PRU0_GPO8	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV5	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG2_PRU0_GPI8	1	I								0		
		PRG2_RGMII1_TD0	2	O										
		GPMC0_A17	3	OZ										
		TRC_DATA6	4	O										
		EHRPWM2_A	5	IO								0		
		PRG2_PWM0_B0	6	IO								1		
		GPIO0_38	7	IO								0		
AG16	PRG2_PRU0_GPO9	PRG2_PRU0_GPO9	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV5	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG2_PRU0_GPI9	1	I								0		
		PRG2_RGMII1_TD1	2	O										
		GPMC0_A16	3	OZ										
		TRC_DATA7	4	O										
		EHRPWM2_B	5	IO								0		
		GPIO0_39	7	IO								0		

表 4-1. Pin Attributes (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE [7]	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABL E [14]	IO Daisy Chain [15]
AF16	PRG2_PRU0_GPO10	PRG2_PRU0_GPO10	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV5	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG2_PRU0_GPI10	1	I								0		
		PRG2_RGMII1_TD2	2	O										
		GPMC0_A15	3	OZ										
		TRC_DATA8	4	O										
		EHRPWM_TZn_IN2	5	I								0		
		EHRPWM_SOCB	6	O										
		GPIO0_40	7	IO								0		
AE16	PRG2_PRU0_GPO11	PRG2_PRU0_GPO11	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV5	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG2_PRU0_GPI11	1	I								0		
		PRG2_RGMII1_TD3	2	O										
		GPMC0_A14	3	OZ										
		TRC_DATA9	4	O										
		PRG2_ECAP0_IN_APWM_OUT	6	IO								0		
		GPIO0_41	7	IO								0		
AD16	PRG2_PRU0_GPO16	PRG2_PRU0_GPO16	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV5	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG2_PRU0_GPI16	1	I								0		
		PRG2_RGMII1_TXC	2	IO								0		
		GPMC0_A13	3	OZ										
		TRC_DATA10	4	O										
		PRG2_PWM0_A1	6	IO								0		
		GPIO0_42	7	IO								0		
AH15	PRG2_PRU1_GPO0	PRG2_PRU1_GPO0	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV5	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG2_PRU1_GPI0	1	I								0		
		PRG2_RGMII2_RD0	2	I								0		
		GPMC0_A12	3	OZ										
		TRC_DATA11	4	O										
		EHRPWM3_A	5	IO								0		
		PRG2_PWM3_A2	6	IO								0		
		GPIO0_43	7	IO								0		

表 4-1. Pin Attributes (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE [7]	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABL E [14]	IO Daisy Chain [15]
AC16	PRG2_PRU1_GPO1	PRG2_PRU1_GPO1	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV5	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG2_PRU1_GPI1	1	I								0		
		PRG2_RGMII2_RD1	2	I								0		
		GPMC0_A11	3	OZ										
		TRC_DATA12	4	O										
		EHRPWM3_B	5	IO								0		
		PRG2_PWM3_B2	6	IO								1		
		GPIO0_44	7	IO								0		
AD17	PRG2_PRU1_GPO2	PRG2_PRU1_GPO2	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV5	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG2_PRU1_GPI2	1	I								0		
		PRG2_RGMII2_RD2	2	I								0		
		GPMC0_A10	3	OZ										
		TRC_DATA13	4	O										
		EHRPWM3_SYNCI	5	I								0		
		PRG2_PWM0_B1	6	IO								1		
		GPIO0_45	7	IO								0		
AH14	PRG2_PRU1_GPO3	PRG2_PRU1_GPO3	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV5	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG2_PRU1_GPI3	1	I								0		
		PRG2_RGMII2_RD3	2	I								0		
		GPMC0_A9	3	OZ										
		TRC_DATA14	4	O										
		EHRPWM3_SYNCO	5	O										
		GPIO0_46	7	IO								0		
AG14	PRG2_PRU1_GPO4	PRG2_PRU1_GPO4	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV5	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG2_PRU1_GPI4	1	I								0		
		PRG2_RGMII2_RX_CTL	2	I								0		
		GPMC0_A8	3	OZ										
		TRC_DATA15	4	O										
		EHRPWM_TZn_IN3	5	I								0		
		PRG2_ECAP0_SYNC_OUT	6	O										
		GPIO0_47	7	IO								0		

表 4-1. Pin Attributes (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE [7]	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABL E [14]	IO Daisy Chain [15]
AG15	PRG2_PRU1_GPO5	PRG2_PRU1_GPO5	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV5	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG2_PRU1_GPI5	1	I								0		
		PRG2_RGMII2_RXC	2	I								0		
		GPMC0_A7	3	OZ										
		TRC_DATA16	4	O										
		EHRPWM4_A	5	IO								0		
		GPIO0_48	7	IO								0		
AC17	PRG2_PRU1_GPO6	PRG2_PRU1_GPO6	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV5	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG2_PRU1_GPI6	1	I								0		
		PRG2_RGMII2_TX_CTL	2	O										
		GPMC0_A6	3	OZ										
		TRC_DATA17	4	O										
		EHRPWM4_B	5	IO								0		
		GPIO0_49	7	IO								0		
AE15	PRG2_PRU1_GPO7	PRG2_PRU1_GPO7	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV5	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG2_PRU1_GPI7	1	I								0		
		PRG2_MDIO0_MDC	2	O										
		GPMC0_A5	3	OZ										
		TRC_DATA18	4	O										
		EHRPWM_TZn_IN4	5	I								0		
		PRG2_PWM3_TZ_IN	6	I								0		
		GPIO0_50	7	IO								0		
AD15	PRG2_PRU1_GPO8	PRG2_PRU1_GPO8	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV5	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG2_PRU1_GPI8	1	I								0		
		PRG2_RGMII2_TD0	2	O										
		GPMC0_A4	3	OZ										
		TRC_DATA19	4	O										
		EHRPWM5_A	5	IO								0		
		PRG2_PWM0_A2	6	IO								0		
		GPIO0_51	7	IO								0		

表 4-1. Pin Attributes (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE [7]	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABL E [14]	IO Daisy Chain [15]
AF14	PRG2_PRU1_GPO9	PRG2_PRU1_GPO9	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV5	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG2_PRU1_GPI9	1	I								0		
		PRG2_RGMII2_TD1	2	O										
		GPMC0_A3	3	OZ										
		TRC_DATA20	4	O										
		EHRPWM5_B	5	IO								0		
		PRG2_PWM3_TZ_OUT	6	O										
		GPIO0_52	7	IO								0		
AC15	PRG2_PRU1_GPO10	PRG2_PRU1_GPO10	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV5	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG2_PRU1_GPI10	1	I								0		
		PRG2_RGMII2_TD2	2	O										
		GPMC0_A2	3	OZ										
		TRC_DATA21	4	O										
		EHRPWM_TZn_IN5	5	I								0		
		PRG2_PWM0_B2	6	IO								1		
		GPIO0_53	7	IO								0		
AD14	PRG2_PRU1_GPO11	PRG2_PRU1_GPO11	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV5	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG2_PRU1_GPI11	1	I								0		
		PRG2_RGMII2_TD3	2	O										
		GPMC0_A1	3	OZ										
		TRC_DATA22	4	O										
		PRG2_ECAP0_SYNC_IN	6	I								0		
		GPIO0_54	7	IO								0		
AE14	PRG2_PRU1_GPO16	PRG2_PRU1_GPO16	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV5	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG2_PRU1_GPI16	1	I								0		
		PRG2_RGMII2_TXC	2	IO								0		
		GPMC0_A0	3	OZ										
		TRC_DATA23	4	O										
		PRG2_PWM1_TZ_OUT	6	O										
		GPIO0_55	7	IO								0		
AF9	REFCLK0N	REFCLK0N		O	OFF		1.8 V	VDDA_1P8_SE RDES0		LJCB CLK				No
AF10	REFCLK0P	REFCLK0P		O	OFF		1.8 V	VDDA_1P8_SE RDES0		LJCB CLK				No
AE8	REFCLK1N	REFCLK1N		O	OFF		1.8 V	VDDA_1P8_SE RDES0		LJCB CLK				No
AE9	REFCLK1P	REFCLK1P		O	OFF		1.8 V	VDDA_1P8_SE RDES0		LJCB CLK				No
D19	RESETSTATz	RESETSTATz	0	O	OFF	0	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD		0/0	Yes

表 4-1. Pin Attributes (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE [7]	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABLE [14]	IO Daisy Chain [15]
F17	RESETz	RESETz	0	I	PU	0	1.8 V/3.3 V	VDDSHV0	Yes	LVC MOS	PU/PD		1/1	Yes
AG5	SERDES0_REFCLKN	SERDES0_REFCLKN		I	OFF	0	1.8 V	VDDA_1P8_SE RDES0		SERDES0				No
AG6	SERDES0_REFCLKP	SERDES0_REFCLKP		I	OFF	0	1.8 V	VDDA_1P8_SE RDES0		SERDES0				No
AC9	SERDES0_REFRES	SERDES0_REFRES		A		0	1.8 V	VDDA_1P8_SE RDES0		SERDES0				No
AH3	SERDES0_RXN	SERDES0_RXN		I	OFF	0	1.8 V	VDDA_1P8_SE RDES0		SERDES0				No
AG2	SERDES0_RXP	SERDES0_RXP		I	OFF	0	1.8 V	VDDA_1P8_SE RDES0		SERDES0				No
AH4	SERDES0_TXN	SERDES0_TXN		O	OFF	0	1.8 V	VDDA_1P8_SE RDES0		SERDES0				No
AG3	SERDES0_TXP	SERDES0_TXP		O	OFF	0	1.8 V	VDDA_1P8_SE RDES0		SERDES0				No
AH6	SERDES1_REFCLKN	SERDES1_REFCLKN		I	OFF	0	1.8 V	VDDA_1P8_SE RDES0		SERDES1				No
AH7	SERDES1_REFCLKP	SERDES1_REFCLKP		I	OFF	0	1.8 V	VDDA_1P8_SE RDES0		SERDES1				No
AC14	SERDES1_REFRES	SERDES1_REFRES		A		0	1.8 V	VDDA_1P8_SE RDES0		SERDES1				No
AG9	SERDES1_RXN	SERDES1_RXN		I	OFF	0	1.8 V	VDDA_1P8_SE RDES0		SERDES1				No
AH10	SERDES1_RXP	SERDES1_RXP		I	OFF	0	1.8 V	VDDA_1P8_SE RDES0		SERDES1				No
AH9	SERDES1_TXN	SERDES1_TXN		O	OFF	0	1.8 V	VDDA_1P8_SE RDES0		SERDES1				No
AG8	SERDES1_TXP	SERDES1_TXP		O	OFF	0	1.8 V	VDDA_1P8_SE RDES0		SERDES1				No
E20	SOC_SAFETY_ERRORn	SOC_SAFETY_ERRORn	0	IO	PD	0	1.8 V/3.3 V	VDDSHV0	Yes	LVC MOS	PU/PD		1/0	Yes
AH13	SPI0_CLK	SPI0_CLK	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV1	Yes	LVC MOS	PU/PD	0	0/1	Yes
		GPIO1_17	7	IO								0		
AH12	SPI1_CLK	SPI1_CLK	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV1	Yes	LVC MOS	PU/PD	0	0/1	Yes
		PRG2_IEP0_EDC_SYNC_OUT0	3	O										
		PRG2_UART0_RTSn	4	O										
		GPIO1_22	7	IO								0		
AG13	SPI0_CS0	SPI0_CS0	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV1	Yes	LVC MOS	PU/PD	1	0/1	Yes
		GPIO1_15	7	IO								0		

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表 4-1. Pin Attributes (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE [7]	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABL E [14]	IO Daisy Chain [15]
AF13	SPI0_CS1	SPI0_CS1	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD	1	0/1	Yes
		CPTS0_TS_COMP	1	O										
		I2C3_SCL	2	IOD								1		
		PRG1_IEP0_EDIO_OUTVALID	6	O										
		GPIO1_16	7	IO								0		
AE13	SPI0_D0	SPI0_D0	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD	0	0/1	Yes
		GPIO1_18	7	IO								0		
AD13	SPI0_D1	SPI0_D1	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD	0	0/1	Yes
		GPIO1_19	7	IO								0		
AD12	SPI1_CS0	SPI1_CS0	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD	1	0/1	Yes
		PRG2_IEP0_EDC_LATCH_IN0	3	I								0		
		PRG2_UART0_CTSn	4	I								1		
		PRG0_IEP0_EDIO_OUTVALID	6	O										
		GPIO1_20	7	IO								0		
AG12	SPI1_CS1	SPI1_CS1	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD	1	0/1	Yes
		CPTS0_TS_SYNC	1	O										
		I2C3_SDA	2	IOD								1		
		GPIO1_21	7	IO								0		
AE12	SPI1_D0	SPI1_D0	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG2_IEP0_EDC_LATCH_IN1	3	I								0		
		PRG2_UART0_RXD	4	I								1		
		GPIO1_23	7	IO								0		
AF12	SPI1_D1	SPI1_D1	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD	0	0/1	Yes
		PRG2_IEP0_EDC_SYNC_OUT1	3	O										
		PRG2_UART0_TXD	4	O										
		GPIO1_24	7	IO								0		
AA4	TCK	TCK	0	I	PU	0	1.8 V/3.3 V	VDDSHV0_WKU P	Yes	LVCMOS	PU/PD		1/1	Yes
C20	TDI	TDI	0	I	PU	0	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD		1/1	Yes
A20	TDO	TDO	0	OZ	PU	0	1.8 V/3.3 V	VDDSHV0		LVCMOS	PU/PD		0/0	Yes
W6	TEMP_DIODE_P	TEMP_DIODE_P		A			1.8 V			Power				No
B22	TIMER_IO0	TIMER_IO0	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD	0	0/1	Yes
		SYSCLKOUT0	2	O										
		GPIO1_88	7	IO								0		
C23	TIMER_IO1	TIMER_IO1	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD	0	0/1	Yes
		OBSCLK0	2	O										
		GPIO1_89	7	IO								0		

表 4-1. Pin Attributes (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE [7]	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABL E [14]	IO Daisy Chain [15]
A21	TMS	TMS	0	I	PU	0	1.8 V/3.3 V	VDDSHV0	Yes	LVC MOS	PU/PD		1/1	Yes
AA3	TRSTn	TRSTn	0	I	PD	0	1.8 V/3.3 V	VDDSHV0_WKU P	Yes	LVC MOS	PU/PD		1/1	Yes
AG11	UART0_CTSn	UART0_CTSn	0	I	OFF	7	1.8 V/3.3 V	VDDSHV1	Yes	LVC MOS	PU/PD	1	0/1	Yes
		TIMER_IO4	1	IO								0		
		SPI0_CS2	2	IO								1		
		GPIO1_27	7	IO								0		
AD11	UART0_RTSn	UART0_RTSn	0	O	OFF	7	1.8 V/3.3 V	VDDSHV1	Yes	LVC MOS	PU/PD		0/1	Yes
		TIMER_IO5	1	IO								0		
		SPI0_CS3	2	IO								1		
		GPIO1_28	7	IO								0		
AF11	UART0_RXD	UART0_RXD	0	I	OFF	7	1.8 V/3.3 V	VDDSHV1	Yes	LVC MOS	PU/PD	1	0/1	Yes
		GPIO1_25	7	IO								0		
AE11	UART0_TXD	UART0_TXD	0	O	OFF	7	1.8 V/3.3 V	VDDSHV1	Yes	LVC MOS	PU/PD		0/1	Yes
		GPIO1_26	7	IO								0		
AE2	USB0_DM	USB0_DM		IO	OFF		3.3 V	VDDA_3P3_US B		USBHS				No
AF1	USB0_DP	USB0_DP		IO	OFF		3.3 V	VDDA_3P3_US B		USBHS				No
AD9	USB0_DRVVBUS	USB0_DRVVBUS	0	O	PD	0	1.8 V/3.3 V	VDDSHV8	Yes	LVC MOS	PU/PD		0/0	Yes
		GPIO1_71	7	IO								0		
AF7	USB0_ID	USB0_ID		A			3.3 V	VDDA_3P3_US B		USBHS				No
AE7	USB0_VBUS	USB0_VBUS		A				VDDA_3P3_US B		USBHS				No
AD2	USB1_DM	USB1_DM		IO	OFF		3.3 V	VDDA_3P3_US B		USBHS				No
AE1	USB1_DP	USB1_DP		IO	OFF		3.3 V	VDDA_3P3_US B		USBHS				No
AC8	USB1_DRVVBUS	USB1_DRVVBUS	0	O	PD	0	1.8 V/3.3 V	VDDSHV8	Yes	LVC MOS	PU/PD		0/0	Yes
		GPIO1_72	7	IO								0		
AF5	USB1_ID	USB1_ID		A			3.3 V	VDDA_3P3_US B		USBHS				No
AF6	USB1_VBUS	USB1_VBUS		A				VDDA_3P3_US B		USBHS				No
AB6	VDDA_1P8_MON_WKUP	VDDA_1P8_MON_WKUP		A			1.8 V	VDDA_POR_W KUP		Analog				No
G17	VDDA_1P8_SDIO	VDDA_1P8_SDIO		PWR										
L20, M21	VDDA_1P8_CSI0	VDDA_1P8_CSI0		PWR										
AC6	VDDA_1P8_MON0	VDDA_1P8_MON0		A			1.8 V	VDDA_POR_W KUP		Analog				No

表 4-1. Pin Attributes (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE [7]	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABL E [14]	IO Daisy Chain [15]
L22	VDDA_1P8_OLDIO	VDDA_1P8_OLDIO		PWR										
AA14, AB13, AB15	VDDA_1P8_SERDES0	VDDA_1P8_SERDES0		PWR										
AB9	VDDA_3P3_IOLDO_WKUP	VDDA_3P3_IOLDO_WKUP		PWR										
U6	VDDA_3P3_MON_WKUP	VDDA_3P3_MON_WKUP		A			1.8 V	VDDA_POR_W KUP		Analog				No
H17	VDDA_3P3_SDIO	VDDA_3P3_SDIO		PWR										
AC12	VDDA_3P3_USB	VDDA_3P3_USB		PWR										
G18	VDDA_3P3_IOLDO0	VDDA_3P3_IOLDO0		PWR										
AA21	VDDA_3P3_IOLDO1	VDDA_3P3_IOLDO1		PWR										
AC10	VDDA_3P3_MON0	VDDA_3P3_MON0		A			1.8 V	VDDA_POR_W KUP		Analog				No
M7, M9	VDDA_ADC_MCU	VDDA_ADC_MCU		PWR										
AB8	VDDA_LDO_WKUP	VDDA_LDO_WKUP		PWR										
U12	VDDA_MCU	VDDA_MCU		PWR										
H15	VDDA_PLL0_DDR	VDDA_PLL0_DDR		PWR										
H11	VDDA_PLL1_DDR	VDDA_PLL1_DDR		PWR										
Y17	VDDA_PLL_CORE	VDDA_PLL_CORE		PWR										
L21	VDDA_PLL_DSS	VDDA_PLL_DSS		PWR										
L12	VDDA_PLL_MPU0	VDDA_PLL_MPU0		PWR										
K15	VDDA_PLL_MPU1	VDDA_PLL_MPU1		PWR										
AB7	VDDA_PLL_PER0	VDDA_PLL_PER0		PWR										
Y9	VDDA_POR_WKUP	VDDA_POR_WKUP		PWR										
M19	VDDA_SRAM_CORE0	VDDA_SRAM_CORE0		PWR										
V16	VDDA_SRAM_CORE1	VDDA_SRAM_CORE1		PWR										
K7	VDDA_SRAM_MPU0	VDDA_SRAM_MPU0		PWR										
L18	VDDA_SRAM_MPU1	VDDA_SRAM_MPU1		PWR										
AC11	VDDA_VSYS_MON	VDDA_VSYS_MON		A			1.8 V	VDDA_POR_W KUP		Analog				No
AA9	VDDA_WKUP	VDDA_WKUP		PWR										
G12	VDDS0	VDDS0		PWR										
V8	VDDS0_WKUP	VDDS0_WKUP		PWR										
AA16	VDDS1	VDDS1		PWR										
T9	VDDS1_WKUP	VDDS1_WKUP		PWR										
P20	VDDS2	VDDS2		PWR										
N8	VDDS2_WKUP	VDDS2_WKUP		PWR										
T20	VDDS3	VDDS3		PWR										
Y20	VDDS4	VDDS4		PWR										
AC18	VDDS5	VDDS5		PWR										

表 4-1. Pin Attributes (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE [7]	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABL E [14]	IO Daisy Chain [15]
F20	VDDS6	VDDS6		PWR										
K20	VDDS7	VDDS7		PWR										
AA10	VDDS8	VDDS8		PWR										
G15, H16	VDDSHV0	VDDSHV0		PWR										
U8, V7, W8, Y7	VDDSHV0_WKUP	VDDSHV0_WKUP		PWR										
AA18, AB17	VDDSHV1	VDDSHV1		PWR										
R6, R8, T7	VDDSHV1_WKUP	VDDSHV1_WKUP		PWR										
N20, N22, P21, R20, R22	VDDSHV2	VDDSHV2		PWR										
N6, P7, P9	VDDSHV2_WKUP	VDDSHV2_WKUP		PWR										
T21, U20, U22, V21, V23	VDDSHV3	VDDSHV3		PWR										
AA22, W20, W22, Y21, Y23	VDDSHV4	VDDSHV4		PWR										
AA20, AB19, AB21, AB23	VDDSHV5	VDDSHV5		PWR										
G20, H19, H21	VDDSHV6	VDDSHV6		PWR										
J20, J22, K21	VDDSHV7	VDDSHV7		PWR										
AB11	VDDSHV8	VDDSHV8		PWR										
G10, G14, G8, H13, H7, H9	VDDS_DDR	VDDS_DDR		PWR										
J16	VDDS_OSC1	VDDS_OSC1		PWR										
AA12, J10, J12, J14, J19, J8, K13, L14, L19, M13, N14, P13, P15, P19, R14, R16, R18, T13, T15, T17, T19, U14, U16, U18, V13, V15, V19, W14, W18, Y11, Y13, Y15	VDD_CORE	VDD_CORE		PWR										
G22	VDD_DLL_MMC0	VDD_DLL_MMC0		PWR										
H23	VDD_DLL_MMC1	VDD_DLL_MMC1		PWR										
N10, P11, R10, R12, T11	VDD_MCU	VDD_MCU		PWR										
K11, K9, L10, L8, M11	VDD_MPU0	VDD_MPU0		PWR										
K16, K18, L17, M16, M18, N17	VDD_MPU1	VDD_MPU1		PWR										
V11, W10, W12	VDD_WKUP0	VDD_WKUP0		PWR										
M22	VDD_WKUP1	VDD_WKUP1		PWR										
F21	VPP_CORE	VPP_CORE		PWR	OFF		1.8 V			Power				No

表 4-1. Pin Attributes (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE [7]	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABL E [14]	IO Daisy Chain [15]
T6	VPP_MCU	VPP_MCU		PWR	OFF		1.8 V			Power				No
A1, A2, A28, AA11, AA13, AA15, AA17, AA19, AA23, AA26, AA7, AB10, AB12, AB14, AB16, AB18, AB20, AB22, AD4, AE10, AE25, AE5, AF15, AF2, AF20, AF8, AG1, AG10, AG28, AG4, AG7, AH1, AH11, AH2, AH27, AH28, AH5, AH8, B12, B15, B20, B6, B9, D22, E26, E28, E4, F14, F19, F22, F25, F27, F3, G11, G13, G16, G2, G21, G23, G7, G9, H1, H10, H12, H14, H20, H22, H24, H26, H28, H6, H8, J11, J13, J15, J18, J21, J23, J25, J27, J7, J9, K1, K10, K12, K14, K17, K19, K22, K23, K6, K8, L11, L13, L16, L23, L24, L26, L28, L3, L7, L9, M10, M15, M17, M20, M8, N11, N13, N16, N19, N21, N7, N9, P10, P12, P14, P16, P18, P22, P6, P8, R11, R13, R15, R17, R19, R21, R7, R9, T10, T12, T14, T16, T18, T22, T26, T8, U11, U13, U15, U17, U19, U21, U3, U7, U9, V10, V12, V14, V18, V20, V22, V6, W11, W13, W15, W17, W19, W21, W23, W7, W9, Y12, Y14, Y16, Y18, Y22, Y6, Y8	VSS	VSS		GND										
AF4	WKUP_GPIO0_0	WKUP_GPIO0_0	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV0_WKU P	Yes	LVCMOS	PU/PD	0	1/1	Yes
		MCU_SPI1_CLK	1	IO								0		
		WKUP_GPIO0_0	7	IO								0		
		MCU_BOOTMODE00	Bootstrap	I								0		

表 4-1. Pin Attributes (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE [7]	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABLE [14]	IO Daisy Chain [15]
AF3	WKUP_GPIO0_1	WKUP_GPIO0_1	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV0_WKU P	Yes	LVCMOS	PU/PD	0	1/1	Yes
		MCU_SPI1_D0	1	IO								0		
		WKUP_GPIO0_1	7	IO								0		
		MCU_BOOTMODE01	Bootstrap	I								0		
AE3	WKUP_GPIO0_2	WKUP_GPIO0_2	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV0_WKU P	Yes	LVCMOS	PU/PD	0	1/1	Yes
		MCU_SPI1_D1	1	IO								0		
		WKUP_GPIO0_2	7	IO								0		
		MCU_BOOTMODE02	Bootstrap	I								0		
AD1	WKUP_GPIO0_3	WKUP_GPIO0_3	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV0_WKU P	Yes	LVCMOS	PU/PD	0	1/1	Yes
		MCU_SPI1_CS0	1	IO								1		
		WKUP_GPIO0_3	7	IO								0		
		MCU_BOOTMODE03	Bootstrap	I								0		
AC3	WKUP_GPIO0_4	WKUP_GPIO0_4	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV0_WKU P	Yes	LVCMOS	PU/PD	0	1/1	Yes
		MCU_MCAN1_TX	1	O										
		MCU_SPI0_CS3	2	IO								1		
		MCU_ADC_EXT_TRIGGER0	3	I								0		
		WKUP_GPIO0_4	7	IO								0		
		MCU_BOOTMODE04	Bootstrap	I								0		
AD3	WKUP_GPIO0_5	WKUP_GPIO0_5	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV0_WKU P	Yes	LVCMOS	PU/PD	0	0/1	Yes
		MCU_MCAN1_RX	1	I								1		
		MCU_SPI1_CS3	2	IO								1		
		MCU_ADC_EXT_TRIGGER1	3	I								0		
		WKUP_GPIO0_5	7	IO								0		
AC2	WKUP_GPIO0_6	WKUP_GPIO0_6	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV0_WKU P	Yes	LVCMOS	PU/PD	0	0/1	Yes
		WKUP_UART0_CTSn	1	I								1		
		MCU_CPTS0_HW1TSPUSH	2	I								0		
		WKUP_GPIO0_6	7	IO								0		
AC1	WKUP_GPIO0_7	WKUP_GPIO0_7	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV0_WKU P	Yes	LVCMOS	PU/PD	0	0/1	Yes
		WKUP_UART0_RTSn	1	O										
		MCU_CPTS0_HW2TSPUSH	2	I								0		
		WKUP_GPIO0_7	7	IO								0		
AC5	WKUP_GPIO0_8	WKUP_GPIO0_8	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV0_WKU P	Yes	LVCMOS	PU/PD	0	1/1	Yes
		MCU_CPTS0_TS_SYNC	2	O										
		WKUP_GPIO0_8	7	IO								0		
		MCU_BOOTMODE08	Bootstrap	I								0		

表 4-1. Pin Attributes (continued)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE [7]	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABL E [14]	IO Daisy Chain [15]
AB4	WKUP_GPIO0_9	WKUP_GPIO0_9	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV0_WKU P	Yes	LVCMOS	PU/PD	0	1/1	Yes
		MCU_CPTS0_TS_COMP	2	O										
		WKUP_GPIO0_9	7	IO								0		
		MCU_BOOTMODE09	Bootstrap	I								0		
AB3	WKUP_GPIO0_10	WKUP_GPIO0_10	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV0_WKU P	Yes	LVCMOS	PU/PD	0	0/1	Yes
		MCU_EXT_REFCLK0	1	I								0		
		MCU_CPTS0_RFT_CLK	4	I								0		
		MCU_SYSCLKOUT0	5	O										
		WKUP_GPIO0_10	7	IO								0		
AB2	WKUP_GPIO0_11	WKUP_GPIO0_11	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV0_WKU P	Yes	LVCMOS	PU/PD	0	0/1	Yes
		MCU_OBSCCLK0	1	O										
		MCU_TIMER_IO1	4	IO								0		
		MCU_CLKOUT0	6	O										
		WKUP_GPIO0_11	7	IO								0		
AC7	WKUP_I2C0_SCL	WKUP_I2C0_SCL	0	IOD	OFF	0	1.8 V/3.3 V	VDDSHV0_WKU P	Yes	I2C OPEN DRAIN		1	1/0	Yes
AD6	WKUP_I2C0_SDA	WKUP_I2C0_SDA	0	IOD	OFF	0	1.8 V/3.3 V	VDDSHV0_WKU P	Yes	I2C OPEN DRAIN		1	1/0	Yes
AE4	WKUP_LFOSC0_XI	WKUP_LFOSC0_XI		I	OFF		1.8 V	VDDA_WKUP		Analog				No
AC4	WKUP_LFOSC0_XO	WKUP_LFOSC0_XO		O	OFF		1.8 V	VDDA_WKUP		Analog				No
AD5	WKUP_OSC0_XI	WKUP_OSC0_XI		I	OFF		1.8 V	VDDA_WKUP		Analog				No
AE6	WKUP_OSC0_XO	WKUP_OSC0_XO		O	OFF		1.8 V	VDDA_WKUP		Analog				No
AB1	WKUP_UART0_RXD	WKUP_UART0_RXD	0	I	OFF	7	1.8 V/3.3 V	VDDSHV0_WKU P	Yes	LVCMOS	PU/PD	1	0/1	Yes
		WKUP_GPIO0_52	7	IO								0		
AB5	WKUP_UART0_TXD	WKUP_UART0_TXD	0	O	OFF	7	1.8 V/3.3 V	VDDSHV0_WKU P	Yes	LVCMOS	PU/PD	1	0/1	Yes
		WKUP_GPIO0_53	7	IO								0		

The following list describes the table column headers:

1. **BALL NUMBER:** Ball numbers on the bottom side associated with each signal on the bottom.
2. **BALL NAME:** Mechanical name from package device (name is taken from muxmode 0).
3. **SIGNAL NAME:** Names of signals multiplexed on each ball (also notice that the name of the ball is the signal name in muxmode 0).

注: 表 4-1, *Pin Attributes*, does not take into account the subsystem multiplexing signals.
Subsystem multiplexing signals are described in 4.3, *Signal Descriptions*.

4. **MUXMODE:** Multiplexing mode number:
 - a. MUXMODE 0 is the primary muxmode. The primary muxmode is not necessarily the default muxmode.

注: The default muxmode is the mode at the release of the reset; also see the BALL
RESET REL. MUXMODE column.

- b. MUXMODE 1 through 7 are possible muxmodes for alternate functions. On each pin, some muxmodes are effectively used for alternate functions, while some muxmodes are not used. Only MUXMODE values which correspond to defined functions should be used.
 - c. Bootstrap are Special Configuration Pins, latched on rising edge of PORn / RESETFULLn. These are not programable MUXMODE.
 - d. An empty box means Not Applicable.
5. **TYPE:** This column describes functionality of the pin when configured for the given mux mode. It does not represent all capabilities of the pin, and as such, there may be other mux mode configurations where these pins operate as a push-pull driver:
 - I = Input
 - O = Output
 - IO = Input or Output
 - IOD = Open drain terminal - Input or Output
 - IOZ = Input, Output or Three-state terminal
 - OZ = Output or Three-state terminal
 - A = Analog
 - PWR = Power
 - GND = Ground
 - CAP = LDO Capacitor.
6. **BALL RESET STATE:** The state of the terminal at power-on reset:
 - DRIVE 0 (OFF): The buffer drives V_{OL} (pulldown or pullup resistor not activated).
 - DRIVE 1 (OFF): The buffer drives V_{OH} (pulldown or pullup resistor not activated).
 - OFF: High-impedance
 - PD: High-impedance with an active pulldown resistor
 - PU: High-impedance with an active pullup resistor
 - An empty box means Not Applicable.

For more information on the CORE_PWRON_RET_RST reset signal and its reset sources, see chapter *Device Configuration* in the device TRM.

7. **BALL RESET REL. MUXMODE:** This muxmode is automatically configured at the release of the rstoutn signal.
An empty box means Not Applicable.
8. **I/O VOLTAGE VALUE:** This column describes the IO voltage value (the corresponding power supply).
An empty box means Not Applicable.
9. **POWER:** The voltage supply that powers the terminal IO buffers.
An empty box means Not Applicable.
10. **HYS:** Indicates if the input buffer has hysteresis:
 - Yes: With hysteresis

- No: Without hysteresis
An empty box means No.

For more information, see the hysteresis values in [5.6, Electrical Characteristics](#).

11. **BUFFER TYPE:** This column describes the associated output buffer type

An empty box means Not Applicable.

For drive strength of the associated output buffer, refer to [5.6, Electrical Characteristics](#).

12. **PULL UP/DOWN TYPE:** indicates the presence of an internal pullup or pulldown resistor. Pullup and pulldown resistors can be enabled or disabled via software.

- PU: Internal pullup
- PD: Internal pulldown
- PU/PD: Internal pullup and pulldown
- An empty box means No pull.

13. **DSIS:** The deselected input state (DSIS) indicates the state driven on the peripheral input (logic "0", logic "1", or "PIN" level) when the peripheral pin function is not selected by any of the PINCTLx registers.

- 0: Logic 0 driven on the input signal port of the peripheral.
- 1: Logic 1 driven on the input signal port of the peripheral.
- An empty box means Not Applicable.

14. **RXACTIVE / TXDISABLE:** This column indicates the default value of the RXACTIVE / TXDISABLE bits in the PADCONFIG register.

- RXACTIVE: 0 = receiver disabled, 1 = receiver enabled.
- TXDISABLE: 0 = driver enabled, 1 = driver disabled.
- An empty box means Not Applicable.

15. **IO Daisy Chain:** This column indicates which pins can be included in the daisy chain during low power modes.

注: Configuring two pins to the same input signal is not supported as it can yield unexpected results. This can be easily prevented with the proper software configuration (HiZ mode is not an input signal).

注: When a pad is set into a multiplexing mode which is not defined by pin multiplexing, that pad's behavior is undefined. This should be avoided.

4.3 Signal Descriptions

Many signals are available on multiple pins, according to the software configuration of the pin multiplexing options.

The following list describes the column headers:

- (1) **SIGNAL NAME:** The name of the signal passing through the pin.

注: In 表 4-1 and 表 4-75 are not described the subsystem multiplexing signals.

- (2) **DESCRIPTION:** Description of the signal

- (3) **PIN TYPE:** This column describes functionality of the pin when configured for the given mux mode. It does not represent all capabilities of the pin, and as such, there may be other mux mode configurations where these pins operate as a push-pull driver:

- I = Input
- O = Output
- IO = Input or Output
- IOD = Open drain terminal - Input or Output
- IOZ = Input, Output or Three-state terminal
- OZ = Output or Three-state terminal
- A = Analog
- PWR = Power
- GND = Ground
- CAP = LDO Capacitor

- (4) **BALL:** Associated balls bottom

For more information on the I/O cell configurations, see section *Pad Configuration Registers* in the device TRM.

4.3.1 ADC

4.3.1.1 MCU Domain

表 4-2. ADC Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
MCU_ADC_EXT_TRIGGER0	ADC Trigger Input	I	AC3
MCU_ADC_EXT_TRIGGER1	ADC Trigger Input	I	AD3

表 4-3. ADC0 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
MCU_ADC0_REFN	ADC Reference Input (negative)	A	K2
MCU_ADC0_REFP	ADC Reference Input (positive)	A	K3
MCU_ADC0_AIN0	ADC Analog Input 0	A	K5
MCU_ADC0_AIN1	ADC Analog Input 1	A	J3
MCU_ADC0_AIN2	ADC Analog Input 2	A	J1
MCU_ADC0_AIN3	ADC Analog Input 3	A	J5
MCU_ADC0_AIN4	ADC Analog Input 4	A	K4
MCU_ADC0_AIN5	ADC Analog Input 5	A	J4
MCU_ADC0_AIN6	ADC Analog Input 6	A	J2
MCU_ADC0_AIN7	ADC Analog Input 7	A	J6

表 4-4. ADC1 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
MCU_ADC1_REFN	ADC Reference Input (negative)	A	H3
MCU_ADC1_REFP	ADC Reference Input (positive)	A	H2
MCU_ADC1_AIN0	ADC Analog Input 0	A	F4
MCU_ADC1_AIN1	ADC Analog Input 1	A	G6
MCU_ADC1_AIN2	ADC Analog Input 2	A	G4
MCU_ADC1_AIN3	ADC Analog Input 3	A	H5
MCU_ADC1_AIN4	ADC Analog Input 4	A	F5
MCU_ADC1_AIN5	ADC Analog Input 5	A	G5
MCU_ADC1_AIN6	ADC Analog Input 6	A	G3
MCU_ADC1_AIN7	ADC Analog Input 7	A	H4

4.3.2 CAL

4.3.2.1 MAIN Domain

表 4-5. CSI0 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
CSI0_RXN0	CSI Differential Receive Input (negative)	I	G28
CSI0_RXN1	CSI Differential Receive Input (negative)	I	H27
CSI0_RXN2	CSI Differential Receive Input (negative)	I	F26
CSI0_RXN3	CSI Differential Receive Input (negative)	I	H25
CSI0_RXN4 ⁽¹⁾	CSI Differential Receive Input (negative)	I	G24
CSI0_RXP0	CSI Differential Receive Input (positive)	I	F28
CSI0_RXP1	CSI Differential Receive Input (positive)	I	G27
CSI0_RXP2	CSI Differential Receive Input (positive)	I	G26
CSI0_RXP3	CSI Differential Receive Input (positive)	I	G25
CSI0_RXP4 ⁽¹⁾	CSI Differential Receive Input (positive)	I	F24

(1) Line 4 (position 5) supports only data. For more information, see section *Camera Adapter Layer (CAL) Subsystem* in the device TRM.

表 4-6. VIN0 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
VIN0_HD	Video Input Horizontal Sync	I	P23
VIN0_PCLK	Video Input Pixel Clock	I	R28
VIN0_VD	Video Input Vertical Sync	I	R23
VIN0_DATA0	Video Input Data 0	I	N23
VIN0_DATA1	Video Input Data 1	I	M26
VIN0_DATA2	Video Input Data 2	I	P28
VIN0_DATA3	Video Input Data 3	I	P27
VIN0_DATA4	Video Input Data 4	I	N26
VIN0_DATA5	Video Input Data 5	I	N25
VIN0_DATA6	Video Input Data 6	I	P24
VIN0_DATA7	Video Input Data 7	I	R27
VIN0_DATA8	Video Input Data 8	I	T24
VIN0_DATA9	Video Input Data 9	I	T23
VIN0_DATA10	Video Input Data 10	I	R25

表 4-6. VIN0 Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
VIN0_DATA11	Video Input Data 11	I	T27
VIN0_DATA12	Video Input Data 12	I	M27
VIN0_DATA13	Video Input Data 13	I	M23
VIN0_DATA14	Video Input Data 14	I	M28
VIN0_DATA15	Video Input Data 15	I	M24

4.3.3 CPSW2G

4.3.3.1 MCU Domain

表 4-7. CPSW2G0 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
MCU_CPTS0_RFT_CLK	CPTS Reference Clock	I	AB3
MCU_CPTS0_TS_COMP	CPTS Time Stamp Counter Compare	O	AB4
MCU_CPTS0_TS_SYNC	CPTS Time Stamp Counter Bit	O	AC5
MCU_CPTS0_HW1TSPUSH	CPTS Hardware Time Stamp Push 1	I	AC2
MCU_CPTS0_HW2TSPUSH	CPTS Hardware Time Stamp Push 2	I	AC1
MCU_MDIO0_MDC	MDIO Clock	O	L1
MCU_MDIO0_MDIO	MDIO Data	IO	L4
MCU_RGMII1_RXC	RGMII Receive Clock	I	M1
MCU_RGMII1_RX_CTL	RGMII Receive Control	I	N5
MCU_RGMII1_TXC	RGMII Transmit Clock	IO	N1
MCU_RGMII1_TX_CTL	RGMII Transmit Control	O	N4
MCU_RGMII1_RD0	RGMII Receive Data 0	I	L6
MCU_RGMII1_RD1	RGMII Receive Data 1	I	M6
MCU_RGMII1_RD2	RGMII Receive Data 2	I	L5
MCU_RGMII1_RD3	RGMII Receive Data 3	I	L2
MCU_RGMII1_TD0	RGMII Transmit Data 0	O	M5
MCU_RGMII1_TD1	RGMII Transmit Data 1	O	M4
MCU_RGMII1_TD2	RGMII Transmit Data 2	O	M3
MCU_RGMII1_TD3	RGMII Transmit Data 3	O	M2
MCU_RMII1_CR_S_DV	RMII Carrier Sense / Data Valid	I	N4
MCU_RMII1_REF_CLK	RMII Reference Clock	I	M1
MCU_RMII1_RX_ER	RMII Receive Data Error	I	N5
MCU_RMII1_TX_EN	RMII Transmit Enable	O	N1
MCU_RMII1_RXD0	RMII Receive Data 0	I	L6
MCU_RMII1_RXD1	RMII Receive Data 1	I	M6
MCU_RMII1_TXD0	RMII Transmit Data 0	O	M5
MCU_RMII1_TXD1	RMII Transmit Data 1	O	M4

4.3.4 DDRSS**4.3.4.1 MAIN Domain****表 4-8. DDRSS0 Signal Descriptions**

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
DDR_AC0	DDRSS Address and Command Bus	IO	A10
DDR_AC1	DDRSS Address and Command Bus	IO	D9
DDR_AC2	DDRSS Address and Command Bus	IO	C9
DDR_AC3	DDRSS Address and Command Bus	IO	E9
DDR_AC4	DDRSS Address and Command Bus	IO	A9
DDR_AC5	DDRSS Address and Command Bus	IO	E8
DDR_AC6	DDRSS Address and Command Bus	IO	F8
DDR_AC7	DDRSS Address and Command Bus	IO	C7
DDR_AC8	DDRSS Address and Command Bus	IO	C8
DDR_AC9	DDRSS Address and Command Bus	IO	D7
DDR_AC10	DDRSS Address and Command Bus	IO	E7
DDR_AC11	DDRSS Address and Command Bus	IO	A6
DDR_AC12	DDRSS Address and Command Bus	IO	F7
DDR_AC13	DDRSS Address and Command Bus	IO	D6
DDR_AC14	DDRSS Address and Command Bus	IO	C6
DDR_AC15	DDRSS Address and Command Bus	IO	F6
DDR_AC16	DDRSS Address and Command Bus	IO	E6
DDR_AC17	DDRSS Address and Command Bus	IO	E5
DDR_AC18	DDRSS Address and Command Bus	IO	D8
DDR_AC19	DDRSS Address and Command Bus	IO	D10
DDR_AC20	DDRSS Address and Command Bus	IO	E10
DDR_AC21	DDRSS Address and Command Bus	IO	C10
DDR_AC22	DDRSS Address and Command Bus	IO	F11
DDR_AC23	DDRSS Address and Command Bus	IO	B10
DDR_AC24	DDRSS Address and Command Bus	IO	D11
DDR_AC25	DDRSS Address and Command Bus	IO	B11
DDR_AC26	DDRSS Address and Command Bus	IO	C11
DDR_AC27	DDRSS Address and Command Bus	IO	E11
DDR_AC28	DDRSS Address and Command Bus	IO	E12
DDR_AC29	DDRSS Address and Command Bus	IO	D12
DDR_ALERTn	DDRSS Parity Error	IO	D5
DDR_CK0N	DDRSS Differential Clock (negative)	IO	B8
DDR_CK0P	DDRSS Differential Clock (positive)	IO	A8
DDR_CK1N	DDRSS Differential Clock (negative)	IO	B7
DDR_CK1P	DDRSS Differential Clock (positive)	IO	A7
DDR_DM0	DDRSS Data Mask	IO	E1
DDR_DM1	DDRSS Data Mask	IO	C5
DDR_DM2	DDRSS Data Mask	IO	D14
DDR_DM3	DDRSS Data Mask	IO	B17
DDR_DQ0	DDRSS Data	IO	A3
DDR_DQ1	DDRSS Data	IO	B2
DDR_DQ2	DDRSS Data	IO	C2
DDR_DQ3	DDRSS Data	IO	D2

表 4-8. DDRSS0 Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
DDR_DQ4	DDRSS Data	IO	E2
DDR_DQ5	DDRSS Data	IO	G1
DDR_DQ6	DDRSS Data	IO	F2
DDR_DQ7	DDRSS Data	IO	F1
DDR_DQ8	DDRSS Data	IO	E3
DDR_DQ9	DDRSS Data	IO	C3
DDR_DQ10	DDRSS Data	IO	D3
DDR_DQ11	DDRSS Data	IO	B3
DDR_DQ12	DDRSS Data	IO	D4
DDR_DQ13	DDRSS Data	IO	C4
DDR_DQ14	DDRSS Data	IO	B4
DDR_DQ15	DDRSS Data	IO	B5
DDR_DQ16	DDRSS Data	IO	E13
DDR_DQ17	DDRSS Data	IO	C14
DDR_DQ18	DDRSS Data	IO	B14
DDR_DQ19	DDRSS Data	IO	A14
DDR_DQ20	DDRSS Data	IO	E14
DDR_DQ21	DDRSS Data	IO	B13
DDR_DQ22	DDRSS Data	IO	C13
DDR_DQ23	DDRSS Data	IO	D13
DDR_DQ24	DDRSS Data	IO	D15
DDR_DQ25	DDRSS Data	IO	C15
DDR_DQ26	DDRSS Data	IO	E16
DDR_DQ27	DDRSS Data	IO	E15
DDR_DQ28	DDRSS Data	IO	D16
DDR_DQ29	DDRSS Data	IO	B16
DDR_DQ30	DDRSS Data	IO	C16
DDR_DQ31	DDRSS Data	IO	A17
DDR_DQS0N	DDRSS Complimentary Data Strobe	IO	C1
DDR_DQS0P	DDRSS Data Strobe	IO	D1
DDR_DQS1N	DDRSS Complimentary Data Strobe	IO	A4
DDR_DQS1P	DDRSS Data Strobe	IO	A5
DDR_DQS2N	DDRSS Complimentary Data Strobe	IO	A12
DDR_DQS2P	DDRSS Data Strobe	IO	A13
DDR_DQS3N	DDRSS Complimentary Data Strobe	IO	A16
DDR_DQS3P	DDRSS Data Strobe	IO	A15
DDR_ECC_D0	DDRSS ECC Data	IO	B19
DDR_ECC_D1	DDRSS ECC Data	IO	B18
DDR_ECC_D2	DDRSS ECC Data	IO	C18
DDR_ECC_D3	DDRSS ECC Data	IO	D18
DDR_ECC_D4	DDRSS ECC Data	IO	E18
DDR_ECC_D5	DDRSS ECC Data	IO	E17
DDR_ECC_D6	DDRSS ECC Data	IO	D17
DDR_ECC_DM	DDRSS ECC Data Mask	IO	C17
DDR_ECC_DQSN	DDRSS ECC Complimentary Data Strobe	IO	A18
DDR_ECC_DQSP	DDRSS ECC Data Strobe	IO	A19
DDR_FS_RESETn	DDRSS Fail-safe Reset	IO	F16

表 4-8. DDRSS0 Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
DDR_RESETh	DDRSS Reset	IO	A11
DDR_VREF0	DDRSS I/O Voltage Reference ⁽¹⁾	A	F12
DDR_VREF_ZQ	DDRSS I/O Voltage Reference for ZQ calibration	A	F15
DDR_VTP	DDRSS Calibration Resistor ⁽²⁾	A	F13

(1) This pin is intended for observation purpose only. No external voltage should be applied to this pin.

(2) An external 240Ω ±1% resistor must be connected between this pin and VSS. No external voltage should be applied to this pin.

4.3.4.2 DDRSS Mapping

表 4-9 presents DDRSS interface signal mapping per device memory type.

表 4-9. DDRSS Signal Mapping

SIGNAL NAME [1]	MEMORY TYPE			PIN TYPE [3]	BALL [4]
	DDR3L ⁽²⁾	DDR4 ⁽²⁾	LPDDR4 ⁽¹⁾		
DDR_AC0	A0	A0	CA0_A	IO	A10
DDR_AC1	A1	A1	CA1_A	IO	D9
DDR_AC2	A2	A2	CA2_A	IO	C9
DDR_AC3	A3	A3	CA3_A	IO	E9
DDR_AC4	A4	A4	CA4_A	IO	A9
DDR_AC5	A5	A5	CA5_A	IO	E8
DDR_AC6	A6	A6	CA0_B	IO	F8
DDR_AC7	A7	A7	CA1_B	IO	C7
DDR_AC8	A8	A8	CA2_B	IO	C8
DDR_AC9	A9	A9	CA3_B	IO	D7
DDR_AC10	A10	A10	CA4_B	IO	E7
DDR_AC11	A11	A11	CA5_B	IO	A6
DDR_AC12	A12	A12	CS0_B	IO	F7
DDR_AC13	A13	A13	CKE0_B	IO	D6
DDR_AC14	A14	A14/WE_n	CS1_B	IO	C6
DDR_AC15	A15	A15/CAS_n	CKE1_B	IO	F6
DDR_AC16	WE_n	A16/RAS_n		IO	E6
DDR_AC17	CAS_n	A17		IO	E5
DDR_AC18	RAS_n	ACT_n		IO	D8
DDR_AC19	BA0	BA0		IO	D10
DDR_AC20	BA1	BA1		IO	E10
DDR_AC21	BA2	BG0		IO	C10
DDR_AC22		BG1		IO	F11
DDR_AC23		PAR		IO	B10
DDR_AC24	CS0_n	CS0_n	CS0_A	IO	D11
DDR_AC25	ODT0	ODT0		IO	B11
DDR_AC26	CKE0	CKE0	CKE0_A	IO	C11
DDR_AC27	CS1_n	CS1_n	CS1_A	IO	E11
DDR_AC28	ODT1	ODT1		IO	E12
DDR_AC29	CKE1	CKE1	CKE1_A	IO	D12
DDR_ALERTn		ALERT_n		IO	D5
DDR_CK0P	CK0	CK0_t	CK_t_A	IO	A8
DDR_CK0N	CK0_n	CK0_c	CK_c_A	IO	B8

表 4-9. DDRSS Signal Mapping (continued)

SIGNAL NAME [1]	MEMORY TYPE			PIN TYPE [3]	BALL [4]
	DDR3L ⁽²⁾	DDR4 ⁽²⁾	LPDDR4 ⁽¹⁾		
DDR_CK1P	CK1	CK1_t	CK_t_B	IO	A7
DDR_CK1N	CK1_n	CK1_c	CK_c_B	IO	B7
DDR_DQ0	DQ0	DQ0	DQ0	IO	A3
DDR_DQ1	DQ1	DQ1	DQ1	IO	B2
DDR_DQ2	DQ2	DQ2	DQ2	IO	C2
DDR_DQ3	DQ3	DQ3	DQ3	IO	D2
DDR_DQ4	DQ4	DQ4	DQ4	IO	E2
DDR_DQ5	DQ5	DQ5	DQ5	IO	G1
DDR_DQ6	DQ6	DQ6	DQ6	IO	F2
DDR_DQ7	DQ7	DQ7	DQ7	IO	F1
DDR_DM0	DM0	DM0_n	DMI0	IO	E1
DDR_DQ8	DQ8	DQ8	DQ8	IO	E3
DDR_DQ9	DQ9	DQ9	DQ9	IO	C3
DDR_DQ10	DQ10	DQ10	DQ10	IO	D3
DDR_DQ11	DQ11	DQ11	DQ11	IO	B3
DDR_DQ12	DQ12	DQ12	DQ12	IO	D4
DDR_DQ13	DQ13	DQ13	DQ13	IO	C4
DDR_DQ14	DQ14	DQ14	DQ14	IO	B4
DDR_DQ15	DQ15	DQ15	DQ15	IO	B5
DDR_DM1	DM1	DM1_n	DMI1	IO	C5
DDR_DQ16	DQ16	DQ16	DQ16	IO	E13
DDR_DQ17	DQ17	DQ17	DQ17	IO	C14
DDR_DQ18	DQ18	DQ18	DQ18	IO	B14
DDR_DQ19	DQ19	DQ19	DQ19	IO	A14
DDR_DQ20	DQ20	DQ20	DQ20	IO	E14
DDR_DQ21	DQ21	DQ21	DQ21	IO	B13
DDR_DQ22	DQ22	DQ22	DQ22	IO	C13
DDR_DQ23	DQ23	DQ23	DQ23	IO	D13
DDR_DM2	DM2	DM2_n	DMI2	IO	D14
DDR_DQ24	DQ24	DQ24	DQ24	IO	D15
DDR_DQ25	DQ25	DQ25	DQ25	IO	C15
DDR_DQ26	DQ26	DQ26	DQ26	IO	E16
DDR_DQ27	DQ27	DQ27	DQ27	IO	E15
DDR_DQ28	DQ28	DQ28	DQ28	IO	D16
DDR_DQ29	DQ29	DQ29	DQ29	IO	B16
DDR_DQ30	DQ30	DQ30	DQ30	IO	C16
DDR_DQ31	DQ31	DQ31	DQ31	IO	A17
DDR_DM3	DM3	DM3_n	DMI3	IO	B17
DDR_ECC_D0	DQ32	DQ32	DQ32	IO	B19
DDR_ECC_D1	DQ33	DQ33	DQ33	IO	B18
DDR_ECC_D2	DQ34	DQ34	DQ34	IO	C18
DDR_ECC_D3	DQ35	DQ35	DQ35	IO	D18
DDR_ECC_D4	DQ36	DQ36	DQ36	IO	E18
DDR_ECC_D5	DQ37	DQ37	DQ37	IO	E17
DDR_ECC_D6	DQ38	DQ38	DQ38	IO	D17
DDR_ECC_DM	DM4	DM4_n	DM4	IO	C17

表 4-9. DDRSS Signal Mapping (continued)

SIGNAL NAME [1]	MEMORY TYPE			PIN TYPE [3]	BALL [4]
	DDR3L ⁽²⁾	DDR4 ⁽²⁾	LPDDR4 ⁽¹⁾		
DDR_DQS0P	DQS0	DQS0_t	DQS0	IO	D1
DDR_DQS0N	DQS0_n	DQS0_c	DQS0_n	IO	C1
DDR_DQS1P	DQS1	DQS1_t	DQS1	IO	A5
DDR_DQS1N	DQS1_n	DQS1_c	DQS1_n	IO	A4
DDR_DQS2P	DQS2	DQS2_t	DQS2	IO	A13
DDR_DQS2N	DQS2_n	DQS2_c	DQS2_n	IO	A12
DDR_DQS3P	DQS3	DQS3_t	DQS3	IO	A15
DDR_DQS3N	DQS3_n	DQS3_c	DQS3_n	IO	A16
DDR_ECC_DQSP	DQS4	DQS4_t	DQS4	IO	A19
DDR_ECC_DQSN	DQS4_n	DQS4_c	DQS4_n	IO	A18
DDR_FS_RESETh	FS_RESET_n	FS_RESET_n	FS_RESET_n	IO	F16
DDR_RESETh	RESET_n	RESET_n	RESET_n	IO	A11
DDR_VREF0	VREF0	VREF0	VREF0	A	F12
DDR_VREF_ZQ	VREF_ZQ	VREF_ZQ	VREF_ZQ	A	F15
DDR_VTP	VTP	VTP	VTP	A	F13

(1) This device cannot support two independent channels.

(2) Only single rank is supported for DDR3L and DDR4.

4.3.5 DMTIMER

4.3.5.1 MAIN Domain

表 4-10. DMTIMER Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
TIMER_IO0	Timer Inputs and Outputs (not tied to single timer instance)	IO	B22
TIMER_IO1	Timer Inputs and Outputs (not tied to single timer instance)	IO	C23
TIMER_IO2	Timer Inputs and Outputs (not tied to single timer instance)	IO	P23
TIMER_IO3	Timer Inputs and Outputs (not tied to single timer instance)	IO	R23
TIMER_IO4	Timer Inputs and Outputs (not tied to single timer instance)	IO	AG11
TIMER_IO5	Timer Inputs and Outputs (not tied to single timer instance)	IO	AD11
TIMER_IO6	Timer Inputs and Outputs (not tied to single timer instance)	IO	T24
TIMER_IO7	Timer Inputs and Outputs (not tied to single timer instance)	IO	T23

4.3.5.2 MCU Domain

表 4-11. DMTIMER Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
MCU_TIMER_IO0	Timer Inputs and Outputs (not tied to single timer instance)	IO	N3
MCU_TIMER_IO1	Timer Inputs and Outputs (not tied to single timer instance)	IO	AB2

4.3.6 DSS

4.3.6.1 MAIN Domain

表 4-12. DSS0 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
VOUT1_DE	Video Output Data Enable	O	T23
VOUT1_EXTCLKIN	Video Output External Pixel Clock Input	I	R25
VOUT1_HSYNC	Video Output Horizontal Sync	O	T24
VOUT1_PCLK	Video Output Pixel Clock Output	O	R24
VOUT1_VSYNC	Video Output Vertical Sync	O	T25
VOUT1_DATA0	Video Output Data 0	O	M27
VOUT1_DATA1	Video Output Data 1	O	M23
VOUT1_DATA2	Video Output Data 2	O	M28
VOUT1_DATA3	Video Output Data 3	O	M24
VOUT1_DATA4	Video Output Data 4	O	N24
VOUT1_DATA5	Video Output Data 5	O	N27
VOUT1_DATA6	Video Output Data 6	O	N28
VOUT1_DATA7	Video Output Data 7	O	M25
VOUT1_DATA8	Video Output Data 8	O	N23
VOUT1_DATA9	Video Output Data 9	O	M26
VOUT1_DATA10	Video Output Data 10	O	P28
VOUT1_DATA11	Video Output Data 11	O	P27
VOUT1_DATA12	Video Output Data 12	O	N26
VOUT1_DATA13	Video Output Data 13	O	N25
VOUT1_DATA14	Video Output Data 14	O	P24
VOUT1_DATA15	Video Output Data 15	O	R27
VOUT1_DATA16	Video Output Data 16	O	R28
VOUT1_DATA17	Video Output Data 17	O	P25
VOUT1_DATA18	Video Output Data 18	O	P26
VOUT1_DATA19	Video Output Data 19	O	U28
VOUT1_DATA20	Video Output Data 20	O	T28
VOUT1_DATA21	Video Output Data 21	O	P23
VOUT1_DATA22	Video Output Data 22	O	R26
VOUT1_DATA23	Video Output Data 23	O	R23

ADVANCE INFORMATION

4.3.7 ECAP

4.3.7.1 MAIN Domain

表 4-13. ECAP0 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
ECAP0_IN_APWM_OUT	Enhanced Capture (ECAP) Input or Auxiliary PWM (APWM) Output	IO	D21

4.3.8 EHRPWM

4.3.8.1 MAIN Domain

表 4-14. EHRPWM Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
EHRPWM_SOCA	EHRPWM Start of Conversion A	O	AC19
EHRPWM_SOCB	EHRPWM Start of Conversion B	O	AF16
EHRPWM_TZn_IN0	EHRPWM Trip Zone Input 0 (active low)	I	AH17
EHRPWM_TZn_IN1	EHRPWM Trip Zone Input 1 (active low)	I	AC19
EHRPWM_TZn_IN2	EHRPWM Trip Zone Input 2 (active low)	I	AF16
EHRPWM_TZn_IN3	EHRPWM Trip Zone Input 3 (active low)	I	AG14
EHRPWM_TZn_IN4	EHRPWM Trip Zone Input 4 (active low)	I	AE15
EHRPWM_TZn_IN5	EHRPWM Trip Zone Input 5 (active low)	I	AC15

表 4-15. EHRPWM0 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
EHRPWM0_A	EHRPWM Output A	IO	AG18
EHRPWM0_B	EHRPWM Output B	IO	AG17
EHRPWM0_SYNCI	Sync Input to EHRPWM module from an external pin	I	AF18
EHRPWM0_SYNCO	Sync Output to EHRPWM module to an external pin	O	AE18

表 4-16. EHRPWM1 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
EHRPWM1_A	EHRPWM Output A	IO	AF17
EHRPWM1_B	EHRPWM Output B	IO	AE17

表 4-17. EHRPWM2 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
EHRPWM2_A	EHRPWM Output A	IO	AH16
EHRPWM2_B	EHRPWM Output B	IO	AG16

表 4-18. EHRPWM3 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
EHRPWM3_A	EHRPWM Output A	IO	AH15
EHRPWM3_B	EHRPWM Output B	IO	AC16
EHRPWM3_SYNCI	Sync Input to EHRPWM module from an external pin	I	AD17
EHRPWM3_SYNCO	Sync Output to EHRPWM module to an external pin	O	AH14

表 4-19. EHRPWM4 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
EHRPWM4_A	EHRPWM Output A	IO	AG15
EHRPWM4_B	EHRPWM Output B	IO	AC17

表 4-20. EHRPWM5 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
EHRPWM5_A	EHRPWM Output A	IO	AD15
EHRPWM5_B	EHRPWM Output B	IO	AF14

4.3.9 EQEP

4.3.9.1 MAIN Domain

表 4-21. EQEP0 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
EQEP0_A	EQEP Quadrature Input A	I	AB26
EQEP0_B	EQEP Quadrature Input B	I	AA25
EQEP0_I	EQEP Index	IO	AA28
EQEP0_S	EQEP Strobe	IO	U23

表 4-22. EQEP1 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
EQEP1_A	EQEP Quadrature Input A	I	AH22
EQEP1_B	EQEP Quadrature Input B	I	AE21
EQEP1_I	EQEP Index	IO	AC20
EQEP1_S	EQEP Strobe	IO	AC22

表 4-23. EQEP2 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
EQEP2_A	EQEP Quadrature Input A	I	D25
EQEP2_B	EQEP Quadrature Input B	I	B26
EQEP2_I	EQEP Index	IO	A24
EQEP2_S	EQEP Strobe	IO	E24

4.3.10 GPIO

4.3.10.1 MAIN Domain

表 4-24. GPIO0 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
GPIO0_0	General Purpose Input/Output	IO	M27
GPIO0_1	General Purpose Input/Output	IO	M23
GPIO0_2	General Purpose Input/Output	IO	M28
GPIO0_3	General Purpose Input/Output	IO	M24
GPIO0_4	General Purpose Input/Output	IO	N24
GPIO0_5	General Purpose Input/Output	IO	N27
GPIO0_6	General Purpose Input/Output	IO	N28
GPIO0_7	General Purpose Input/Output	IO	M25
GPIO0_8	General Purpose Input/Output	IO	N23
GPIO0_9	General Purpose Input/Output	IO	M26

表 4-24. GPIO0 Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
GPIO0_10	General Purpose Input/Output	IO	P28
GPIO0_11	General Purpose Input/Output	IO	P27
GPIO0_12	General Purpose Input/Output	IO	N26
GPIO0_13	General Purpose Input/Output	IO	N25
GPIO0_14	General Purpose Input/Output	IO	P24
GPIO0_15	General Purpose Input/Output	IO	R27
GPIO0_16	General Purpose Input/Output	IO	R28
GPIO0_17	General Purpose Input/Output	IO	P25
GPIO0_18	General Purpose Input/Output	IO	P26
GPIO0_19	General Purpose Input/Output	IO	U28
GPIO0_20	General Purpose Input/Output	IO	T28
GPIO0_21	General Purpose Input/Output	IO	P23
GPIO0_22	General Purpose Input/Output	IO	R26
GPIO0_23	General Purpose Input/Output	IO	R23
GPIO0_24	General Purpose Input/Output	IO	T25
GPIO0_25	General Purpose Input/Output	IO	T24
GPIO0_26	General Purpose Input/Output	IO	R24
GPIO0_27	General Purpose Input/Output	IO	T23
GPIO0_28	General Purpose Input/Output	IO	R25
GPIO0_29	General Purpose Input/Output	IO	T27
GPIO0_30	General Purpose Input/Output	IO	AF18
GPIO0_31	General Purpose Input/Output	IO	AE18
GPIO0_32	General Purpose Input/Output	IO	AH17
GPIO0_33	General Purpose Input/Output	IO	AG18
GPIO0_34	General Purpose Input/Output	IO	AG17
GPIO0_35	General Purpose Input/Output	IO	AF17
GPIO0_36	General Purpose Input/Output	IO	AE17
GPIO0_37	General Purpose Input/Output	IO	AC19
GPIO0_38	General Purpose Input/Output	IO	AH16
GPIO0_39	General Purpose Input/Output	IO	AG16
GPIO0_40	General Purpose Input/Output	IO	AF16
GPIO0_41	General Purpose Input/Output	IO	AE16
GPIO0_42	General Purpose Input/Output	IO	AD16
GPIO0_43	General Purpose Input/Output	IO	AH15
GPIO0_44	General Purpose Input/Output	IO	AC16
GPIO0_45	General Purpose Input/Output	IO	AD17
GPIO0_46	General Purpose Input/Output	IO	AH14
GPIO0_47	General Purpose Input/Output	IO	AG14
GPIO0_48	General Purpose Input/Output	IO	AG15
GPIO0_49	General Purpose Input/Output	IO	AC17
GPIO0_50	General Purpose Input/Output	IO	AE15
GPIO0_51	General Purpose Input/Output	IO	AD15
GPIO0_52	General Purpose Input/Output	IO	AF14
GPIO0_53	General Purpose Input/Output	IO	AC15
GPIO0_54	General Purpose Input/Output	IO	AD14
GPIO0_55	General Purpose Input/Output	IO	AE14
GPIO0_56	General Purpose Input/Output	IO	AE22

表 4-24. GPIO0 Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
GPIO0_57	General Purpose Input/Output	IO	AG24
GPIO0_58	General Purpose Input/Output	IO	AF23
GPIO0_59	General Purpose Input/Output	IO	AD21
GPIO0_60	General Purpose Input/Output	IO	AG23
GPIO0_61	General Purpose Input/Output	IO	AF27
GPIO0_62	General Purpose Input/Output	IO	AF22
GPIO0_63	General Purpose Input/Output	IO	AG27
GPIO0_64	General Purpose Input/Output	IO	AF28
GPIO0_65	General Purpose Input/Output	IO	AF26
GPIO0_66	General Purpose Input/Output	IO	AH25
GPIO0_67	General Purpose Input/Output	IO	AF21
GPIO0_68	General Purpose Input/Output	IO	AH20
GPIO0_69	General Purpose Input/Output	IO	AH21
GPIO0_70	General Purpose Input/Output	IO	AG20
GPIO0_71	General Purpose Input/Output	IO	AD19
GPIO0_72	General Purpose Input/Output	IO	AD20
GPIO0_73	General Purpose Input/Output	IO	AH26
GPIO0_74	General Purpose Input/Output	IO	AG25
GPIO0_75	General Purpose Input/Output	IO	AG26
GPIO0_76	General Purpose Input/Output	IO	AH24
GPIO0_77	General Purpose Input/Output	IO	AH23
GPIO0_78	General Purpose Input/Output	IO	AG21
GPIO0_79	General Purpose Input/Output	IO	AH22
GPIO0_80	General Purpose Input/Output	IO	AE21
GPIO0_81	General Purpose Input/Output	IO	AC22
GPIO0_82	General Purpose Input/Output	IO	AG22
GPIO0_83	General Purpose Input/Output	IO	AD23
GPIO0_84	General Purpose Input/Output	IO	AE24
GPIO0_85	General Purpose Input/Output	IO	AF25
GPIO0_86	General Purpose Input/Output	IO	AF24
GPIO0_87	General Purpose Input/Output	IO	AC20
GPIO0_88	General Purpose Input/Output	IO	AE20
GPIO0_89	General Purpose Input/Output	IO	AF19
GPIO0_90	General Purpose Input/Output	IO	AH19
GPIO0_91	General Purpose Input/Output	IO	AG19
GPIO0_92	General Purpose Input/Output	IO	AE19
GPIO0_93	General Purpose Input/Output	IO	AE23
GPIO0_94	General Purpose Input/Output	IO	AD22
GPIO0_95	General Purpose Input/Output	IO	AC21

表 4-25. GPIO1 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	ACD [4]
GPIO1_0	General Purpose Input/Output	IO	AD18
GPIO1_1	General Purpose Input/Output	IO	AH18
GPIO1_2	General Purpose Input/Output	IO	D25
GPIO1_3	General Purpose Input/Output	IO	B26
GPIO1_4	General Purpose Input/Output	IO	A24
GPIO1_5	General Purpose Input/Output	IO	E24
GPIO1_6	General Purpose Input/Output	IO	A25
GPIO1_7	General Purpose Input/Output	IO	C26
GPIO1_8	General Purpose Input/Output	IO	E25
GPIO1_9	General Purpose Input/Output	IO	A26
GPIO1_10	General Purpose Input/Output	O	B25
GPIO1_11	General Purpose Input/Output	IO	B27
GPIO1_12	General Purpose Input/Output	I	C25
GPIO1_13	General Purpose Input/Output	IO ⁽¹⁾	A23
GPIO1_14	General Purpose Input/Output	IO ⁽¹⁾	B23
GPIO1_15	General Purpose Input/Output	IO	AG13
GPIO1_16	General Purpose Input/Output	IO	AF13
GPIO1_17	General Purpose Input/Output	IO	AH13
GPIO1_18	General Purpose Input/Output	IO	AE13
GPIO1_19	General Purpose Input/Output	IO	AD13
GPIO1_20	General Purpose Input/Output	IO	AD12
GPIO1_21	General Purpose Input/Output	IO	AG12
GPIO1_22	General Purpose Input/Output	IO	AH12
GPIO1_23	General Purpose Input/Output	IO	AE12
GPIO1_24	General Purpose Input/Output	IO	AF12
GPIO1_25	General Purpose Input/Output	IO	AF11
GPIO1_26	General Purpose Input/Output	IO	AE11
GPIO1_27	General Purpose Input/Output	IO	AG11
GPIO1_28	General Purpose Input/Output	IO	AD11
GPIO1_29	General Purpose Input/Output	IO	V24
GPIO1_30	General Purpose Input/Output	IO	W25
GPIO1_31	General Purpose Input/Output	IO	W24
GPIO1_32	General Purpose Input/Output	IO	AA27
GPIO1_33	General Purpose Input/Output	IO	Y24
GPIO1_34	General Purpose Input/Output	IO	V28
GPIO1_35	General Purpose Input/Output	IO	Y25
GPIO1_36	General Purpose Input/Output	IO	U27
GPIO1_37	General Purpose Input/Output	IO	V27
GPIO1_38	General Purpose Input/Output	IO	V26
GPIO1_39	General Purpose Input/Output	IO	U25
GPIO1_40	General Purpose Input/Output	IO	AB25
GPIO1_41	General Purpose Input/Output	IO	AD27
GPIO1_42	General Purpose Input/Output	IO	AC26
GPIO1_43	General Purpose Input/Output	IO	AD26
GPIO1_44	General Purpose Input/Output	IO	AA24
GPIO1_45	General Purpose Input/Output	IO	AD28

表 4-25. GPIO1 Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	ACD [4]
GPIO1_46	General Purpose Input/Output	IO	U26
GPIO1_47	General Purpose Input/Output	IO	V25
GPIO1_48	General Purpose Input/Output	IO	U24
GPIO1_49	General Purpose Input/Output	IO	AB28
GPIO1_50	General Purpose Input/Output	IO	AC28
GPIO1_51	General Purpose Input/Output	IO	AC27
GPIO1_52	General Purpose Input/Output	IO	AB26
GPIO1_53	General Purpose Input/Output	IO	AA25
GPIO1_54	General Purpose Input/Output	IO	U23
GPIO1_55	General Purpose Input/Output	IO	AB27
GPIO1_56	General Purpose Input/Output	IO	W28
GPIO1_57	General Purpose Input/Output	IO	W27
GPIO1_58	General Purpose Input/Output	IO	Y28
GPIO1_59	General Purpose Input/Output	IO	AA28
GPIO1_60	General Purpose Input/Output	IO	AB24
GPIO1_61	General Purpose Input/Output	IO	AC25
GPIO1_62	General Purpose Input/Output	IO	AD25
GPIO1_63	General Purpose Input/Output	IO	AD24
GPIO1_64	General Purpose Input/Output	IO	AE27
GPIO1_65	General Purpose Input/Output	IO	AC24
GPIO1_66	General Purpose Input/Output	IO	Y27
GPIO1_67	General Purpose Input/Output	IO	Y26
GPIO1_68	General Purpose Input/Output	IO	W26
GPIO1_69	General Purpose Input/Output	IO	AE26
GPIO1_70	General Purpose Input/Output	IO	AE28
GPIO1_71	General Purpose Input/Output	IO	AD9
GPIO1_72	General Purpose Input/Output	IO	AC8
GPIO1_73	General Purpose Input/Output	IO	D27
GPIO1_74	General Purpose Input/Output	IO	D26
GPIO1_75	General Purpose Input/Output	IO	E27
GPIO1_76	General Purpose Input/Output	IO	D28
GPIO1_77	General Purpose Input/Output	O	C27
GPIO1_78	General Purpose Input/Output	IO	C28
GPIO1_79	General Purpose Input/Output	IO ⁽¹⁾	B24
GPIO1_80	General Purpose Input/Output	IO ⁽¹⁾	C24
GPIO1_86	General Purpose Input/Output	IO	D21
GPIO1_87	General Purpose Input/Output	IO	A22
GPIO1_88	General Purpose Input/Output	IO	B22
GPIO1_89	General Purpose Input/Output	IO	C23

(1) When OSC1 is being used with an external crystal, this pin must only be used as an input. The output functionality must be disabled.

4.3.10.2 WKUP Domain

表 4-26. GPIO0 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
WKUP_GPIO0_0	General Purpose Input/Output	IO	AF4
WKUP_GPIO0_1	General Purpose Input/Output	IO	AF3
WKUP_GPIO0_2	General Purpose Input/Output	IO	AE3
WKUP_GPIO0_3	General Purpose Input/Output	IO	AD1
WKUP_GPIO0_4	General Purpose Input/Output	IO	AC3
WKUP_GPIO0_5	General Purpose Input/Output	IO	AD3
WKUP_GPIO0_6	General Purpose Input/Output	IO	AC2
WKUP_GPIO0_7	General Purpose Input/Output	IO	AC1
WKUP_GPIO0_8	General Purpose Input/Output	IO	AC5
WKUP_GPIO0_9	General Purpose Input/Output	IO	AB4
WKUP_GPIO0_10	General Purpose Input/Output	IO	AB3
WKUP_GPIO0_11	General Purpose Input/Output	IO	AB2
WKUP_GPIO0_12	General Purpose Input/Output	IO	V1
WKUP_GPIO0_13	General Purpose Input/Output	IO	U1
WKUP_GPIO0_14	General Purpose Input/Output	IO	U2
WKUP_GPIO0_15	General Purpose Input/Output	IO	U4
WKUP_GPIO0_16	General Purpose Input/Output	IO	U5
WKUP_GPIO0_17	General Purpose Input/Output	IO	T2
WKUP_GPIO0_18	General Purpose Input/Output	IO	T3
WKUP_GPIO0_19	General Purpose Input/Output	IO	T4
WKUP_GPIO0_20	General Purpose Input/Output	IO	T5
WKUP_GPIO0_21	General Purpose Input/Output	IO	R2
WKUP_GPIO0_22	General Purpose Input/Output	IO	R3
WKUP_GPIO0_23	General Purpose Input/Output	IO	R4
WKUP_GPIO0_24	General Purpose Input/Output	IO	R5
WKUP_GPIO0_25	General Purpose Input/Output	IO	T1
WKUP_GPIO0_26	General Purpose Input/Output	IO	R1
WKUP_GPIO0_27	General Purpose Input/Output	IO	P2
WKUP_GPIO0_28	General Purpose Input/Output	IO	P3
WKUP_GPIO0_29	General Purpose Input/Output	IO	P4
WKUP_GPIO0_30	General Purpose Input/Output	IO	P5
WKUP_GPIO0_31	General Purpose Input/Output	IO	P1
WKUP_GPIO0_32	General Purpose Input/Output	IO	N2
WKUP_GPIO0_33	General Purpose Input/Output	IO	N3
WKUP_GPIO0_34	General Purpose Input/Output	IO	N4
WKUP_GPIO0_35	General Purpose Input/Output	IO	N5
WKUP_GPIO0_36	General Purpose Input/Output	IO	M2
WKUP_GPIO0_37	General Purpose Input/Output	IO	M3
WKUP_GPIO0_38	General Purpose Input/Output	IO	M4
WKUP_GPIO0_39	General Purpose Input/Output	IO	M5
WKUP_GPIO0_40	General Purpose Input/Output	IO	N1
WKUP_GPIO0_41	General Purpose Input/Output	IO	M1
WKUP_GPIO0_42	General Purpose Input/Output	IO	L2
WKUP_GPIO0_43	General Purpose Input/Output	IO	L5
WKUP_GPIO0_44	General Purpose Input/Output	IO	M6

表 4-26. GPIO0 Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
WKUP_GPIO0_45	General Purpose Input/Output	IO	L6
WKUP_GPIO0_46	General Purpose Input/Output	IO	L4
WKUP_GPIO0_47	General Purpose Input/Output	IO	L1
WKUP_GPIO0_48	General Purpose Input/Output	IO	Y1
WKUP_GPIO0_49	General Purpose Input/Output	IO	Y3
WKUP_GPIO0_50	General Purpose Input/Output	IO	Y2
WKUP_GPIO0_51	General Purpose Input/Output	IO	Y4
WKUP_GPIO0_52	General Purpose Input/Output	IO	AB1
WKUP_GPIO0_53	General Purpose Input/Output	IO	AB5
WKUP_GPIO0_54	General Purpose Input/Output	IO	W1
WKUP_GPIO0_55	General Purpose Input/Output	IO	W2

4.3.11 GPMC

4.3.11.1 MAIN Domain

表 4-27. GPMC0 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
GPMC0_ADVn_ALE	GPMC Address Valid (active low) or Address Latch Enable	O	P25
GPMC0_CLK	GPMC Clock Output	IO	R28
GPMC0_DIR	GPMC Data Bus Signal Direction Control	O	T24
GPMC0_OEn_REn	GPMC Output Enable (active low) or Read Enable (active low)	O	P26
GPMC0_WEn	GPMC Write Enable (active low)	O	U28
GPMC0_WPn	GPMC Flash Write Protect (active low)	O	T25
GPMC0_A0	GPMC Address 0 Output. Only used to effectively address 8-bit data non-multiplexed memories	OZ	AE14
GPMC0_A1	GPMC address 1 Output in A/D non-multiplexed mode and Address 17 in A/D multiplexed mode	OZ	AD14
GPMC0_A2	GPMC address 2 Output in A/D non-multiplexed mode and Address 18 in A/D multiplexed mode	OZ	AC15
GPMC0_A3	GPMC address 3 Output in A/D non-multiplexed mode and Address 19 in A/D multiplexed mode	OZ	AF14
GPMC0_A4	GPMC address 4 Output in A/D non-multiplexed mode and Address 20 in A/D multiplexed mode	OZ	AD15
GPMC0_A5	GPMC address 5 Output in A/D non-multiplexed mode and Address 21 in A/D multiplexed mode	OZ	AE15
GPMC0_A6	GPMC address 6 Output in A/D non-multiplexed mode and Address 22 in A/D multiplexed mode	OZ	AC17
GPMC0_A7	GPMC address 7 Output in A/D non-multiplexed mode and Address 23 in A/D multiplexed mode	OZ	AG15
GPMC0_A8	GPMC address 8 Output in A/D non-multiplexed mode and Address 24 in A/D multiplexed mode	OZ	AG14
GPMC0_A9	GPMC address 9 Output in A/D non-multiplexed mode and Address 25 in A/D multiplexed mode	OZ	AH14
GPMC0_A10	GPMC address 10 Output in A/D non-multiplexed mode and Address 26 in A/D multiplexed mode	OZ	AD17
GPMC0_A11	GPMC address 11 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	OZ	AC16

表 4-27. GPMC0 Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
GPMC0_A12	GPMC address 12 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	OZ	AH15
GPMC0_A13	GPMC address 13 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	OZ	AD16
GPMC0_A14	GPMC address 14 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	OZ	AE16
GPMC0_A15	GPMC address 15 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	OZ	AF16
GPMC0_A16	GPMC address 16 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	OZ	AG16
GPMC0_A17	GPMC address 17 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	OZ	AH16
GPMC0_A18	GPMC address 18 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	OZ	AC19
GPMC0_A19	GPMC address 19 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	OZ	AE17
GPMC0_A20	GPMC address 20 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	OZ	AF17
GPMC0_A21	GPMC address 21 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	OZ	AG17
GPMC0_A22	GPMC address 22 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	OZ	AG18
GPMC0_A23	GPMC address 23 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	OZ	AH17
GPMC0_A24	GPMC address 24 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	OZ	AE18
GPMC0_A25	GPMC address 25 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	OZ	AF18
GPMC0_A26	GPMC address 26 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	OZ	T27
GPMC0_A27	GPMC address 27 in A/D non-multiplexed mode and Address 27 in A/D multiplexed mode	OZ	R25
GPMC0_AD0	GPMC Data 0 Input/Output in A/D non-multiplexed mode and additionally Address 1 Output in A/D multiplexed mode	IO	M27
GPMC0_AD1	GPMC Data 1 Input/Output in A/D non-multiplexed mode and additionally Address 2 Output in A/D multiplexed mode	IO	M23
GPMC0_AD2	GPMC Data 2 Input/Output in A/D non-multiplexed mode and additionally Address 3 Output in A/D multiplexed mode	IO	M28
GPMC0_AD3	GPMC Data 3 Input/Output in A/D non-multiplexed mode and additionally Address 4 Output in A/D multiplexed mode	IO	M24
GPMC0_AD4	GPMC Data 4 Input/Output in A/D non-multiplexed mode and additionally Address 5 Output in A/D multiplexed mode	IO	N24
GPMC0_AD5	GPMC Data 5 Input/Output in A/D non-multiplexed mode and additionally Address 6 Output in A/D multiplexed mode	IO	N27
GPMC0_AD6	GPMC Data 6 Input/Output in A/D non-multiplexed mode and additionally Address 7 Output in A/D multiplexed mode	IO	N28
GPMC0_AD7	GPMC Data 7 Input/Output in A/D non-multiplexed mode and additionally Address 8 Output in A/D multiplexed mode	IO	M25

表 4-27. GPMC0 Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
GPMC0_AD8	GPMC Data 8 Input/Output in A/D non-multiplexed mode and additionally Address 9 Output in A/D multiplexed mode	IO	N23
GPMC0_AD9	GPMC Data 9 Input/Output in A/D non-multiplexed mode and additionally Address 10 Output in A/D multiplexed mode	IO	M26
GPMC0_AD10	GPMC Data 10 Input/Output in A/D non-multiplexed mode and additionally Address 11 Output in A/D multiplexed mode	IO	P28
GPMC0_AD11	GPMC Data 11 Input/Output in A/D non-multiplexed mode and additionally Address 12 Output in A/D multiplexed mode	IO	P27
GPMC0_AD12	GPMC Data 12 Input/Output in A/D non-multiplexed mode and additionally Address 13 Output in A/D multiplexed mode	IO	N26
GPMC0_AD13	GPMC Data 13 Input/Output in A/D non-multiplexed mode and additionally Address 14 Output in A/D multiplexed mode	IO	N25
GPMC0_AD14	GPMC Data 14 Input/Output in A/D non-multiplexed mode and additionally Address 15 Output in A/D multiplexed mode	IO	P24
GPMC0_AD15	GPMC Data 15 Input/Output in A/D non-multiplexed mode and additionally Address 16 Output in A/D multiplexed mode	IO	R27
GPMC0_BE0n_CLE	GPMC Lower-Byte Enable (active low) or Command Latch Enable	O	T28
GPMC0_BE1n	GPMC Upper-Byte Enable (active low)	O	P23
GPMC0_CSn0	GPMC Chip Select 0 (active low)	O	R24
GPMC0_CSn1	GPMC Chip Select 1 (active low)	O	T23
GPMC0_CSn2	GPMC Chip Select 2 (active low)	O	R25
GPMC0_CSn3	GPMC Chip Select 3 (active low)	O	T27
GPMC0_WAIT0	GPMC External Indication of Wait	I	R26
GPMC0_WAIT1	GPMC External Indication of Wait	I	R23

4.3.12 HYPERBUS

4.3.12.1 MCU Domain

表 4-28. HYPERBUS0 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
MCU_HYPERBUS0_CK	Hyperbus Differential Clock (positive)	O	V1
MCU_HYPERBUS0_CKn	Hyperbus Differential Clock (negative)	O	U1
MCU_HYPERBUS0_INTn	Hyperbus Interrupt (active low)	I	P2
MCU_HYPERBUS0_RESETn	Hyperbus Reset (active low) Output	O	R5
MCU_HYPERBUS0_RESETOn	Hyperbus Reset Status Indicator (active low) from Hyperbus Memory	I	R1
MCU_HYPERBUS0_RWDS	Hyperbus Read-Write Data Strobe	IO	U2
MCU_HYPERBUS0_WPn	Hyperbus Write Protect (Not in use)	O	N3
MCU_HYPERBUS0_CSn0	Hyperbus Chip Select 0	O	R4
MCU_HYPERBUS0_CSn1	Hyperbus Chip Select 1	O	N3
MCU_HYPERBUS0_DQ0	Hyperbus Data 0	IO	U4
MCU_HYPERBUS0_DQ1	Hyperbus Data 1	IO	U5

表 4-28. HYPERBUS0 Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
MCU_HYPERBUS0_DQ2	Hyperbus Data 2	IO	T2
MCU_HYPERBUS0_DQ3	Hyperbus Data 3	IO	T3
MCU_HYPERBUS0_DQ4	Hyperbus Data 4	IO	T4
MCU_HYPERBUS0_DQ5	Hyperbus Data 5	IO	T5
MCU_HYPERBUS0_DQ6	Hyperbus Data 6	IO	R2
MCU_HYPERBUS0_DQ7	Hyperbus Data 7	IO	R3

4.3.13 I2C**4.3.13.1 MAIN Domain**

表 4-29. I2C0 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
I2C0_SCL	I2C Clock	IOD	D20
I2C0_SDA	I2C Data	IOD	C21

表 4-30. I2C1 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
I2C1_SCL	I2C Clock	IOD	B21
I2C1_SDA	I2C Data	IOD	E21

表 4-31. I2C2 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
I2C2_SCL	I2C Clock	IOD	T27
I2C2_SDA	I2C Data	IOD	R25

表 4-32. I2C3 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
I2C3_SCL	I2C Clock	IOD	AF13
I2C3_SDA	I2C Data	IOD	AG12

4.3.13.2 MCU Domain

表 4-33. I2C0 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
MCU_I2C0_SCL	I2C Clock	IOD	AD8
MCU_I2C0_SDA	I2C Data	IOD	AD7

4.3.13.3 WKUP Domain

表 4-34. I2C0 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
WKUP_I2C0_SCL	I2C Clock	IOD	AC7
WKUP_I2C0_SDA	I2C Data	IOD	AD6

4.3.14 MCAN

4.3.14.1 MCU Domain

表 4-35. MCAN0 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
MCU_MCAN0_RX	MCAN Receive Data	I	W2
MCU_MCAN0_TX	MCAN Transmit Data	O	W1

表 4-36. MCAN1 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
MCU_MCAN1_RX	MCAN Receive Data	I	AD3
MCU_MCAN1_TX	MCAN Transmit Data	O	AC3

4.3.15 MCASP

4.3.15.1 MAIN Domain

表 4-37. MCASP0 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
MCASP0_ACLKR	MCASP Receive Bit Clock	IO	W24
MCASP0_ACLKX	MCASP Transmit Bit Clock	IO	V24
MCASP0_AFSR	MCASP Receive Frame Sync	IO	AA27
MCASP0_AFSX	MCASP Transmit Frame Sync	IO	W25
MCASP0_AHCLKR	MCASP Receive Master Clock	IO	AA25
MCASP0_AHCLKX	MCASP Transmit Master Clock	IO	U23
MCASP0_AXR0	MCASP Serial Data (Input/Output)	IO	Y24
MCASP0_AXR1	MCASP Serial Data (Input/Output)	IO	V28
MCASP0_AXR2	MCASP Serial Data (Input/Output)	IO	Y25
MCASP0_AXR3	MCASP Serial Data (Input/Output)	IO	U27
MCASP0_AXR4	MCASP Serial Data (Input/Output)	IO	V27
MCASP0_AXR5	MCASP Serial Data (Input/Output)	IO	V26
MCASP0_AXR6	MCASP Serial Data (Input/Output)	IO	U25
MCASP0_AXR7	MCASP Serial Data (Input/Output)	IO	AB25
MCASP0_AXR8	MCASP Serial Data (Input/Output)	IO	AD27
MCASP0_AXR9	MCASP Serial Data (Input/Output)	IO	AC26
MCASP0_AXR10	MCASP Serial Data (Input/Output)	IO	AD26
MCASP0_AXR11	MCASP Serial Data (Input/Output)	IO	AA24
MCASP0_AXR12	MCASP Serial Data (Input/Output)	IO	AD28
MCASP0_AXR13	MCASP Serial Data (Input/Output)	IO	U26

表 4-37. MCASP0 Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
MCASP0_AXR14	MCASP Serial Data (Input/Output)	IO	V25
MCASP0_AXR15	MCASP Serial Data (Input/Output)	IO	U24

表 4-38. MCASP1 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
MCASP1_ACLKR	MCASP Receive Bit Clock	IO	AC27
MCASP1_ACLKX	MCASP Transmit Bit Clock	IO	AB28
MCASP1_AFSR	MCASP Receive Frame Sync	IO	AB26
MCASP1_AFSX	MCASP Transmit Frame Sync	IO	AC28
MCASP1_AHCLKR	MCASP Receive Master Clock	IO	AD28
MCASP1_AHCLKX	MCASP Transmit Master Clock	IO	U26
MCASP1_AXR0	MCASP Serial Data (Input/Output)	IO	AA25
MCASP1_AXR1	MCASP Serial Data (Input/Output)	IO	U23
MCASP1_AXR2	MCASP Serial Data (Input/Output)	IO	AB27
MCASP1_AXR3	MCASP Serial Data (Input/Output)	IO	W28
MCASP1_AXR4	MCASP Serial Data (Input/Output)	IO	W27
MCASP1_AXR5	MCASP Serial Data (Input/Output)	IO	Y28
MCASP1_AXR6	MCASP Serial Data (Input/Output)	IO	AA28
MCASP1_AXR7	MCASP Serial Data (Input/Output)	IO	AB24
MCASP1_AXR8	MCASP Serial Data (Input/Output)	IO	AC25
MCASP1_AXR9	MCASP Serial Data (Input/Output)	IO	AD25

表 4-39. MCASP2 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
MCASP2_ACLKR	MCASP Receive Bit Clock	IO	AE27
MCASP2_ACLKX	MCASP Transmit Bit Clock	IO	W26
MCASP2_AFSR	MCASP Receive Frame Sync	IO	AD24
MCASP2_AFSX	MCASP Transmit Frame Sync	IO	Y26
MCASP2_AHCLKR	MCASP Receive Master Clock	IO	V25
MCASP2_AHCLKX	MCASP Transmit Master Clock	IO	U24
MCASP2_AXR0	MCASP Serial Data (Input/Output)	IO	AC24
MCASP2_AXR1	MCASP Serial Data (Input/Output)	IO	Y27
MCASP2_AXR2	MCASP Serial Data (Input/Output)	IO	AE26
MCASP2_AXR3	MCASP Serial Data (Input/Output)	IO	AE28

4.3.16 MCSPI

4.3.16.1 MAIN Domain

表 4-40. MCSPI0 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
SPI0_CLK	SPI Clock	IO	AH13
SPI0_CS0	SPI Chip Select 0	IO	AG13
SPI0_CS1	SPI Chip Select 1	IO	AF13

表 4-40. MCSPI0 Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
SPI0_CS2	SPI Chip Select 2	IO	AG11
SPI0_CS3	SPI Chip Select 3	IO	AD11
SPI0_D0	SPI Data 0	IO	AE13
SPI0_D1	SPI Data 1	IO	AD13

表 4-41. MCSPI1 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
SPI1_CLK	SPI Clock	IO	AH12
SPI1_CS0	SPI Chip Select 0	IO	AD12
SPI1_CS1	SPI Chip Select 1	IO	AG12
SPI1_CS2	SPI Chip Select 2	IO	AD18
SPI1_CS3	SPI Chip Select 3	IO	AH18
SPI1_D0	SPI Data 0	IO	AE12
SPI1_D1	SPI Data 1	IO	AF12

表 4-42. MCSPI2 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
SPI2_CLK	SPI Clock	IO	AE23
SPI2_CS0	SPI Chip Select 0	IO	AD23
SPI2_CS1	SPI Chip Select 1	IO	AF26
SPI2_CS2	SPI Chip Select 2	IO	AH25
SPI2_CS3	SPI Chip Select 3	IO	AF24
SPI2_D0	SPI Data 0	IO	AD22
SPI2_D1	SPI Data 1	IO	AC21

表 4-43. MCSPI3 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
SPI3_CLK	SPI Clock	IO	Y27
SPI3_CS0	SPI Chip Select 0	IO	W28
SPI3_CS1	SPI Chip Select 1	IO	V26
SPI3_CS2	SPI Chip Select 2	IO	U25
SPI3_CS3	SPI Chip Select 3	IO	Y28
SPI3_D0	SPI Data 0	IO	Y26
SPI3_D1	SPI Data 1	IO	W26

4.3.16.2 MCU Domain

表 4-44. MCSPI0 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
MCU_SPI0_CLK	SPI Clock	IO	Y1
MCU_SPI0_CS0	SPI Chip Select 0	IO	Y4
MCU_SPI0_CS1	SPI Chip Select 1	IO	P1
MCU_SPI0_CS2	SPI Chip Select 2	IO	N3

表 4-44. MCSPI0 Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
MCU_SPI0_CS3	SPI Chip Select 3	IO	AC3
MCU_SPI0_D0	SPI Data 0	IO	Y3
MCU_SPI0_D1	SPI Data 1	IO	Y2

表 4-45. MCSPI1 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
MCU_SPI1_CLK	SPI Clock	IO	AF4
MCU_SPI1_CS0	SPI Chip Select 0	IO	AD1
MCU_SPI1_CS1	SPI Chip Select 1	IO	P4
MCU_SPI1_CS2	SPI Chip Select 2	IO	P5
MCU_SPI1_CS3	SPI Chip Select 3	IO	AD3
MCU_SPI1_D0	SPI Data 0	IO	AF3
MCU_SPI1_D1	SPI Data 1	IO	AE3

4.3.17 MMC

4.3.17.1 MAIN Domain

表 4-46. MMC0 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
MMC0_CALPAD ⁽¹⁾	MMC/SD Calibration Resistor	A	D24
MMC0_CLK ⁽²⁾⁽³⁾	MMC/SD Clock	O	B25
MMC0_CMD ⁽²⁾	MMC/SD Command	IO	B27
MMC0_DS	MMC Data Strobe	I	C25
MMC0_SDCD	SD Card Detect	I	A23
MMC0_SDWP	SD Write Protect	I	B23
MMC0_DAT0 ⁽²⁾	MMC/SD Data	IO	A26
MMC0_DAT1 ⁽²⁾	MMC/SD Data	IO	E25
MMC0_DAT2 ⁽²⁾	MMC/SD Data	IO	C26
MMC0_DAT3 ⁽²⁾	MMC/SD Data	IO	A25
MMC0_DAT4 ⁽²⁾	MMC/SD Data	IO	E24
MMC0_DAT5 ⁽²⁾	MMC/SD Data	IO	A24
MMC0_DAT6 ⁽²⁾	MMC/SD Data	IO	B26
MMC0_DAT7 ⁽²⁾	MMC/SD Data	IO	D25

(1) An external 10kΩ ±1% resistor must be connected between this pin and VSS. No external voltage should be applied to this pin.

(2) When MMCSD0 or MMCSD1 is used, any non-MMC signal function multiplexed with the respective pins are not available. This is due to the MMC having an internal IO multiplexer which is controlled by MMCSD0/1_SS_PHY_CTRL_1_REG[31] IOMUX_ENABLE. This internal IO multiplexer is primary for the signal functions associated with MMCSD pins, and the PADCONFIG's MUXMODE is secondary. Additionally, the internal IO multiplexer affects all of the MMCSD0 or MMCSD1 pins, regardless of configured data bus width. Therefore, when MMCSD0/1_SS_PHY_CTRL_1_REG[31] IOMUX_ENABLE = 0, the respective MMCSD pins are configured for eMMC/SD functionality, regardless of the PADCONFIG [MUXMODE] setting.

(3) This output signal is also used as a retiming input. It is also recommended to place a 33 Ω resistor in series (close to the processor) to avoid signal reflections.

表 4-47. MMC1 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
MMC1_CALPAD ⁽¹⁾	MMC/SD Calibration Resistor	A	F23
MMC1_CLK ⁽²⁾⁽³⁾	MMC/SD Clock	O	C27
MMC1_CMD ⁽²⁾	MMC/SD Command	IO	C28
MMC1_SDCD	SD Card Detect	I	B24
MMC1_SDWP	SD Write Protect	I	C24
MMC1_DAT0 ⁽²⁾	MMC/SD Data	IO	D28
MMC1_DAT1 ⁽²⁾	MMC/SD Data	IO	E27
MMC1_DAT2 ⁽²⁾	MMC/SD Data	IO	D26
MMC1_DAT3 ⁽²⁾	MMC/SD Data	IO	D27

(1) An external 10kΩ ±1% resistor must be connected between this pin and VSS. No external voltage should be applied to this pin.

(2) When MMCSD0 or MMCSD1 is used, any non-MMC signal function multiplexed with the respective pins are not available. This is due to the MMC having an internal IO multiplexer which is controlled by MMCSD0/1_SS_PHY_CTRL_1_REG[31] IOMUX_ENABLE. This internal IO multiplexer is primary for the signal functions associated with MMCSD pins, and the PADCONFIG's MUXMODE is secondary. Additionally, the internal IO multiplexer affects all of the MMCSD0 or MMCSD1 pins, regardless of configured data bus width. Therefore, when MMCSD0/1_SS_PHY_CTRL_1_REG[31] IOMUX_ENABLE = 0, the respective MMCSD pins are configured for eMMC/SD functionality, regardless of the PADCONFIG [MUXMODE] setting.

(3) This output signal is also used as a retiming input. It is also recommended to place a 33 Ω resistor in series (close to the processor) to avoid signal reflections.

4.3.18 CPTS

4.3.18.1 MAIN Domain

表 4-48. CPTS0 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
CPTS0_RFT_CLK	CPTS Reference Clock	I	D21
CPTS0_TS_COMP	CPTS Time Stamp Counter Compare	O	AF13
CPTS0_TS_SYNC	CPTS Time Stamp Counter Bit	O	AG12
CPTS0_HW1TSPUSH	CPTS Hardware Time Stamp Push 1	I	B21
CPTS0_HW2TSPUSH	CPTS Hardware Time Stamp Push 2	I	E21

4.3.19 OLDI

4.3.19.1 MAIN Domain

表 4-49. OLDI0 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
OLDI0_CLKN	OLDI Differential Clock (negative)	IO	L25
OLDI0_CLKP	OLDI Differential Clock (positive)	IO	K25
OLDI0_A0N	OLDI Differential Data (negative)	IO	J28
OLDI0_A0P	OLDI Differential Data (positive)	IO	K28
OLDI0_A1N	OLDI Differential Data (negative)	IO	L27
OLDI0_A1P	OLDI Differential Data (positive)	IO	K27
OLDI0_A2N	OLDI Differential Data (negative)	IO	K24
OLDI0_A2P	OLDI Differential Data (positive)	IO	J24
OLDI0_A3N	OLDI Differential Data (negative)	IO	J26
OLDI0_A3P	OLDI Differential Data (positive)	IO	K26

4.3.20 OSPI

4.3.20.1 MCU Domain

表 4-50. OSPI0 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
MCU_OSPI0_CLK	OSPI Clock	O	V1
MCU_OSPI0_DQS	OSPI Data Strobe (DQS) or Loopback Clock Input	I	U2
MCU_OSPI0_LBCLKO	OSPI Loopback Clock Output	IO	U1
MCU_OSPI0_CSn0	OSPI Chip Select 0 (active low)	O	R4
MCU_OSPI0_CSn1	OSPI Chip Select 1 (active low)	O	R5
MCU_OSPI0_CSn2	OSPI Chip Select 2 (active low)	O	R1
MCU_OSPI0_CSn3	OSPI Chip Select 3 (active low)	O	P2
MCU_OSPI0_D0	OSPI Data 0	IO	U4
MCU_OSPI0_D1	OSPI Data 1	IO	U5
MCU_OSPI0_D2	OSPI Data 2	IO	T2
MCU_OSPI0_D3	OSPI Data 3	IO	T3
MCU_OSPI0_D4	OSPI Data 4	IO	T4
MCU_OSPI0_D5	OSPI Data 5	IO	T5
MCU_OSPI0_D6	OSPI Data 6	IO	R2
MCU_OSPI0_D7	OSPI Data 7	IO	R3

表 4-51. OSPI1 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
MCU_OSPI1_CLK	OSPI Clock	O	T1
MCU_OSPI1_DQS	OSPI Data Strobe (DQS) or Loopback Clock Input	I	P2
MCU_OSPI1_LBCLKO	OSPI Loopback Clock Output	IO	R1
MCU_OSPI1_CSn0	OSPI Chip Select 0 (active low)	O	N2
MCU_OSPI1_CSn1	OSPI Chip Select 1 (active low)	O	N3
MCU_OSPI1_D0	OSPI Data 0	IO	P3
MCU_OSPI1_D1	OSPI Data 1	IO	P4
MCU_OSPI1_D2	OSPI Data 2	IO	P5
MCU_OSPI1_D3	OSPI Data 3	IO	P1

4.3.21 PRU_ICSSG

4.3.21.1 MAIN Domain

注: The PRU_ICSSG contains a second layer of multiplexing to enable additional functionality on the PRU GPO and GPI signals. This internal wrapper multiplexing is described in the PRU_ICSSG chapter in the device TRM.

表 4-52. PRU_ICSSG0 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
PRG0_ECAP0_IN_APWM_OUT	PRU_ICSSG Enhanced Capture (ECAP) Input or Auxiliary PWM (APWM) Output	IO	V25
PRG0_ECAP0_SYNC_IN	PRU_ICSSG ECAP Sync Input	I	U27
PRG0_ECAP0_SYNC_OUT	PRU_ICSSG ECAP Sync Output	O	U26
PRG0_IEP0_EDIO_OUTVALID	PRU_ICSSG Industrial Ethernet Digital I/O Outvalid	O	AD12
PRG0_IEP0_EDC_LATCH_IN0	PRU_ICSSG Industrial Ethernet Distributed Clock Latch Input	I	V25
PRG0_IEP0_EDC_LATCH_IN1	PRU_ICSSG Industrial Ethernet Distributed Clock Latch Input	I	U27
PRG0_IEP0_EDC_SYNC_OUT0	PRU_ICSSG Industrial Ethernet Distributed Clock Sync Output	O	U24
PRG0_IEP0_EDC_SYNC_OUT1	PRU_ICSSG Industrial Ethernet Distributed Clock Sync Output	O	U26
PRG0_IEP0_EDIO_DATA_IN_OUT28	PRU_ICSSG Industrial Ethernet Digital I/O Data Input/Output	IO	V26
PRG0_IEP0_EDIO_DATA_IN_OUT29	PRU_ICSSG Industrial Ethernet Digital I/O Data Input/Output	IO	U25
PRG0_IEP0_EDIO_DATA_IN_OUT30	PRU_ICSSG Industrial Ethernet Digital I/O Data Input/Output	IO	Y28
PRG0_IEP0_EDIO_DATA_IN_OUT31	PRU_ICSSG Industrial Ethernet Digital I/O Data Input/Output	IO	AA28
PRG0_IEP1_EDC_LATCH_IN0	PRU_ICSSG Industrial Ethernet Distributed Clock Latch Input	I	Y26
PRG0_IEP1_EDC_LATCH_IN1	PRU_ICSSG Industrial Ethernet Distributed Clock Latch Input	I	W28
PRG0_IEP1_EDC_SYNC_OUT0	PRU_ICSSG Industrial Ethernet Distributed Clock Sync Output	O	W26
PRG0_IEP1_EDC_SYNC_OUT1	PRU_ICSSG Industrial Ethernet Distributed Clock Sync Output	O	Y27
PRG0_MDIO0_MDC	PRU_ICSSG MDIO Clock	O	AE28
PRG0_MDIO0_MDIO	PRU_ICSSG MDIO Data	IO	AE26
PRG0_PRU0_GPI0	PRU_ICSSG PRU Data Input	I	V24
PRG0_PRU0_GPI1	PRU_ICSSG PRU Data Input	I	W25
PRG0_PRU0_GPI2	PRU_ICSSG PRU Data Input	I	W24
PRG0_PRU0_GPI3	PRU_ICSSG PRU Data Input	I	AA27
PRG0_PRU0_GPI4	PRU_ICSSG PRU Data Input	I	Y24
PRG0_PRU0_GPI5	PRU_ICSSG PRU Data Input	I	V28
PRG0_PRU0_GPI6	PRU_ICSSG PRU Data Input	I	Y25
PRG0_PRU0_GPI7	PRU_ICSSG PRU Data Input	I	U27
PRG0_PRU0_GPI8	PRU_ICSSG PRU Data Input	I	V27
PRG0_PRU0_GPI9	PRU_ICSSG PRU Data Input	I	V26
PRG0_PRU0_GPI10	PRU_ICSSG PRU Data Input	I	U25
PRG0_PRU0_GPI11	PRU_ICSSG PRU Data Input	I	AB25

表 4-52. PRU_ICSSG0 Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
PRG0_PRU0_GPI12	PRU_ICSSG PRU Data Input	I	AD27
PRG0_PRU0_GPI13	PRU_ICSSG PRU Data Input	I	AC26
PRG0_PRU0_GPI14	PRU_ICSSG PRU Data Input	I	AD26
PRG0_PRU0_GPI15	PRU_ICSSG PRU Data Input	I	AA24
PRG0_PRU0_GPI16	PRU_ICSSG PRU Data Input	I	AD28
PRG0_PRU0_GPI17	PRU_ICSSG PRU Data Input	I	U26
PRG0_PRU0_GPI18	PRU_ICSSG PRU Data Input	I	V25
PRG0_PRU0_GPI19	PRU_ICSSG PRU Data Input	I	U24
PRG0_PRU0_GPO0	PRU_ICSSG PRU Data Output	IO	V24
PRG0_PRU0_GPO1	PRU_ICSSG PRU Data Output	IO	W25
PRG0_PRU0_GPO2	PRU_ICSSG PRU Data Output	IO	W24
PRG0_PRU0_GPO3	PRU_ICSSG PRU Data Output	IO	AA27
PRG0_PRU0_GPO4	PRU_ICSSG PRU Data Output	IO	Y24
PRG0_PRU0_GPO5	PRU_ICSSG PRU Data Output	IO	V28
PRG0_PRU0_GPO6	PRU_ICSSG PRU Data Output	IO	Y25
PRG0_PRU0_GPO7	PRU_ICSSG PRU Data Output	IO	U27
PRG0_PRU0_GPO8	PRU_ICSSG PRU Data Output	IO	V27
PRG0_PRU0_GPO9	PRU_ICSSG PRU Data Output	IO	V26
PRG0_PRU0_GPO10	PRU_ICSSG PRU Data Output	IO	U25
PRG0_PRU0_GPO11	PRU_ICSSG PRU Data Output	IO	AB25
PRG0_PRU0_GPO12	PRU_ICSSG PRU Data Output	IO	AD27
PRG0_PRU0_GPO13	PRU_ICSSG PRU Data Output	IO	AC26
PRG0_PRU0_GPO14	PRU_ICSSG PRU Data Output	IO	AD26
PRG0_PRU0_GPO15	PRU_ICSSG PRU Data Output	IO	AA24
PRG0_PRU0_GPO16	PRU_ICSSG PRU Data Output	IO	AD28
PRG0_PRU0_GPO17	PRU_ICSSG PRU Data Output	IO	U26
PRG0_PRU0_GPO18	PRU_ICSSG PRU Data Output	IO	V25
PRG0_PRU0_GPO19	PRU_ICSSG PRU Data Output	IO	U24
PRG0_PRU1_GPI0	PRU_ICSSG PRU Data Input	I	AB28
PRG0_PRU1_GPI1	PRU_ICSSG PRU Data Input	I	AC28
PRG0_PRU1_GPI2	PRU_ICSSG PRU Data Input	I	AC27
PRG0_PRU1_GPI3	PRU_ICSSG PRU Data Input	I	AB26
PRG0_PRU1_GPI4	PRU_ICSSG PRU Data Input	I	AA25
PRG0_PRU1_GPI5	PRU_ICSSG PRU Data Input	I	U23
PRG0_PRU1_GPI6	PRU_ICSSG PRU Data Input	I	AB27
PRG0_PRU1_GPI7	PRU_ICSSG PRU Data Input	I	W28
PRG0_PRU1_GPI8	PRU_ICSSG PRU Data Input	I	W27
PRG0_PRU1_GPI9	PRU_ICSSG PRU Data Input	I	Y28
PRG0_PRU1_GPI10	PRU_ICSSG PRU Data Input	I	AA28
PRG0_PRU1_GPI11	PRU_ICSSG PRU Data Input	I	AB24
PRG0_PRU1_GPI12	PRU_ICSSG PRU Data Input	I	AC25
PRG0_PRU1_GPI13	PRU_ICSSG PRU Data Input	I	AD25
PRG0_PRU1_GPI14	PRU_ICSSG PRU Data Input	I	AD24
PRG0_PRU1_GPI15	PRU_ICSSG PRU Data Input	I	AE27
PRG0_PRU1_GPI16	PRU_ICSSG PRU Data Input	I	AC24
PRG0_PRU1_GPI17	PRU_ICSSG PRU Data Input	I	Y27
PRG0_PRU1_GPI18	PRU_ICSSG PRU Data Input	I	Y26

表 4-52. PRU_ICSSG0 Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
PRG0_PRU1_GPI19	PRU_ICSSG PRU Data Input	I	W26
PRG0_PRU1_GPO0	PRU_ICSSG PRU Data Output	IO	AB28
PRG0_PRU1_GPO1	PRU_ICSSG PRU Data Output	IO	AC28
PRG0_PRU1_GPO2	PRU_ICSSG PRU Data Output	IO	AC27
PRG0_PRU1_GPO3	PRU_ICSSG PRU Data Output	IO	AB26
PRG0_PRU1_GPO4	PRU_ICSSG PRU Data Output	IO	AA25
PRG0_PRU1_GPO5	PRU_ICSSG PRU Data Output	IO	U23
PRG0_PRU1_GPO6	PRU_ICSSG PRU Data Output	IO	AB27
PRG0_PRU1_GPO7	PRU_ICSSG PRU Data Output	IO	W28
PRG0_PRU1_GPO8	PRU_ICSSG PRU Data Output	IO	W27
PRG0_PRU1_GPO9	PRU_ICSSG PRU Data Output	IO	Y28
PRG0_PRU1_GPO10	PRU_ICSSG PRU Data Output	IO	AA28
PRG0_PRU1_GPO11	PRU_ICSSG PRU Data Output	IO	AB24
PRG0_PRU1_GPO12	PRU_ICSSG PRU Data Output	IO	AC25
PRG0_PRU1_GPO13	PRU_ICSSG PRU Data Output	IO	AD25
PRG0_PRU1_GPO14	PRU_ICSSG PRU Data Output	IO	AD24
PRG0_PRU1_GPO15	PRU_ICSSG PRU Data Output	IO	AE27
PRG0_PRU1_GPO16	PRU_ICSSG PRU Data Output	IO	AC24
PRG0_PRU1_GPO17	PRU_ICSSG PRU Data Output	IO	Y27
PRG0_PRU1_GPO18	PRU_ICSSG PRU Data Output	IO	Y26
PRG0_PRU1_GPO19	PRU_ICSSG PRU Data Output	IO	W26
PRG0_PWM0_TZ_IN	PRU_ICSSG PWM Trip Zone Input	I	V25
PRG0_PWM0_TZ_OUT	PRU_ICSSG PWM Trip Zone Output	O	U24
PRG0_PWM1_TZ_IN	PRU_ICSSG PWM Trip Zone Input	I	Y26
PRG0_PWM1_TZ_OUT	PRU_ICSSG PWM Trip Zone Output	O	W26
PRG0_PWM2_TZ_IN	PRU_ICSSG PWM Trip Zone Input	I	AA28
PRG0_PWM2_TZ_OUT	PRU_ICSSG PWM Trip Zone Output	O	W27
PRG0_PWM3_TZ_IN	PRU_ICSSG PWM Trip Zone Input	I	V26
PRG0_PWM3_TZ_OUT	PRU_ICSSG PWM Trip Zone Output	O	AB25
PRG0_PWM0_A0	PRU_ICSSG PWM Output A	IO	AD27
PRG0_PWM0_A1	PRU_ICSSG PWM Output A	IO	AD26
PRG0_PWM0_A2	PRU_ICSSG PWM Output A	IO	AD28
PRG0_PWM0_B0	PRU_ICSSG PWM Output B	IO	AC26
PRG0_PWM0_B1	PRU_ICSSG PWM Output B	IO	AA24
PRG0_PWM0_B2	PRU_ICSSG PWM Output B	IO	U26
PRG0_PWM1_A0	PRU_ICSSG PWM Output A	IO	AC25
PRG0_PWM1_A1	PRU_ICSSG PWM Output A	IO	AD24
PRG0_PWM1_A2	PRU_ICSSG PWM Output A	IO	AC24
PRG0_PWM1_B0	PRU_ICSSG PWM Output B	IO	AD25
PRG0_PWM1_B1	PRU_ICSSG PWM Output B	IO	AE27
PRG0_PWM1_B2	PRU_ICSSG PWM Output B	IO	Y27
PRG0_PWM2_A0	PRU_ICSSG PWM Output A	IO	W24
PRG0_PWM2_A1	PRU_ICSSG PWM Output A	IO	V27
PRG0_PWM2_A2	PRU_ICSSG PWM Output A	IO	AC27
PRG0_PWM2_B0	PRU_ICSSG PWM Output B	IO	Y24
PRG0_PWM2_B1	PRU_ICSSG PWM Output B	IO	U25
PRG0_PWM2_B2	PRU_ICSSG PWM Output B	IO	AA25

表 4-52. PRU_ICSSG0 Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
PRG0_PWM3_A0	PRU_ICSSG PWM Output A	IO	V24
PRG0_PWM3_A1	PRU_ICSSG PWM Output A	IO	Y25
PRG0_PWM3_A2	PRU_ICSSG PWM Output A	IO	AA27
PRG0_PWM3_B0	PRU_ICSSG PWM Output B	IO	W25
PRG0_PWM3_B1	PRU_ICSSG PWM Output B	IO	U27
PRG0_PWM3_B2	PRU_ICSSG PWM Output B	IO	V28
PRG0_RGMII1_RXC	PRU_ICSSG RGMII Receive Clock	I	Y25
PRG0_RGMII1_RX_CTL	PRU_ICSSG RGMII Receive Control	I	Y24
PRG0_RGMII1_TXC	PRU_ICSSG RGMII Transmit Clock	IO	AD28
PRG0_RGMII1_TX_CTL	PRU_ICSSG RGMII Transmit Control	O	AB25
PRG0_RGMII2_RXC	PRU_ICSSG RGMII Receive Clock	I	AB27
PRG0_RGMII2_RX_CTL	PRU_ICSSG RGMII Receive Control	I	AA25
PRG0_RGMII2_TXC	PRU_ICSSG RGMII Transmit Clock	IO	AC24
PRG0_RGMII2_TX_CTL	PRU_ICSSG RGMII Transmit Control	O	AB24
PRG0_RGMII1_RD0	PRU_ICSSG RGMII Receive Data	I	V24
PRG0_RGMII1_RD1	PRU_ICSSG RGMII Receive Data	I	W25
PRG0_RGMII1_RD2	PRU_ICSSG RGMII Receive Data	I	W24
PRG0_RGMII1_RD3	PRU_ICSSG RGMII Receive Data	I	AA27
PRG0_RGMII1_TD0	PRU_ICSSG RGMII Transmit Data	O	AD27
PRG0_RGMII1_TD1	PRU_ICSSG RGMII Transmit Data	O	AC26
PRG0_RGMII1_TD2	PRU_ICSSG RGMII Transmit Data	O	AD26
PRG0_RGMII1_TD3	PRU_ICSSG RGMII Transmit Data	O	AA24
PRG0_RGMII2_RD0	PRU_ICSSG RGMII Receive Data	I	AB28
PRG0_RGMII2_RD1	PRU_ICSSG RGMII Receive Data	I	AC28
PRG0_RGMII2_RD2	PRU_ICSSG RGMII Receive Data	I	AC27
PRG0_RGMII2_RD3	PRU_ICSSG RGMII Receive Data	I	AB26
PRG0_RGMII2_TD0	PRU_ICSSG RGMII Transmit Data	O	AC25
PRG0_RGMII2_TD1	PRU_ICSSG RGMII Transmit Data	O	AD25
PRG0_RGMII2_TD2	PRU_ICSSG RGMII Transmit Data	O	AD24
PRG0_RGMII2_TD3	PRU_ICSSG RGMII Transmit Data	O	AE27
PRG0_UART0_CTSn	PRU_ICSSG UART Clear to Send (active low)	I	V26
PRG0_UART0_RTSn	PRU_ICSSG UART Request to Send (active low)	O	U25
PRG0_UART0_RXD	PRU_ICSSG UART Receive Data	I	Y28
PRG0_UART0_TXD	PRU_ICSSG UART Transmit Data	O	AA28

表 4-53. PRU_ICSSG1 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
PRG1_ECAPH0_IN_APWM_OUT	PRU_ICSSG Enhanced Capture (ECAP) Input or Auxiliary PWM (APWM) Output	IO	AC21
PRG1_ECAPH0_SYNC_IN	PRU_ICSSG ECAP Sync Input	I	AD22
PRG1_ECAPH0_SYNC_OUT	PRU_ICSSG ECAP Sync Output	O	AE23
PRG1_IEP0_EDIO_OUTVALID	PRU_ICSSG Industrial Ethernet Digital I/O Outvalid	O	AF13
PRG1_IEP0_EDC_LATCH_IN0	PRU_ICSSG Industrial Ethernet Distributed Clock Latch Input	I	AG25
PRG1_IEP0_EDC_LATCH_IN1	PRU_ICSSG Industrial Ethernet Distributed Clock Latch Input	I	AG27

表 4-53. PRU_ICSSG1 Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
PRG1_IEP0_EDC_SYNC_OUT0	PRU_ICSSG Industrial Ethernet Distributed Clock Sync Output	O	AG26
PRG1_IEP0_EDC_SYNC_OUT1	PRU_ICSSG Industrial Ethernet Distributed Clock Sync Output	O	AH26
PRG1_IEP0_EDIO_DATA_IN_OUT28	PRU_ICSSG Industrial Ethernet Digital I/O Data Input/Output	IO	AF26
PRG1_IEP0_EDIO_DATA_IN_OUT29	PRU_ICSSG Industrial Ethernet Digital I/O Data Input/Output	IO	AH25
PRG1_IEP0_EDIO_DATA_IN_OUT30	PRU_ICSSG Industrial Ethernet Digital I/O Data Input/Output	IO	AF25
PRG1_IEP0_EDIO_DATA_IN_OUT31	PRU_ICSSG Industrial Ethernet Digital I/O Data Input/Output	IO	AF24
PRG1_IEP1_EDC_LATCH_IN0	PRU_ICSSG Industrial Ethernet Distributed Clock Latch Input	I	AD22
PRG1_IEP1_EDC_LATCH_IN1	PRU_ICSSG Industrial Ethernet Distributed Clock Latch Input	I	AD23
PRG1_IEP1_EDC_SYNC_OUT0	PRU_ICSSG Industrial Ethernet Distributed Clock Sync Output	O	AC21
PRG1_IEP1_EDC_SYNC_OUT1	PRU_ICSSG Industrial Ethernet Distributed Clock Sync Output	O	AE23
PRG1_MDIO0_MDC	PRU_ICSSG MDIO Clock	O	AH18
PRG1_MDIO0_MDIO	PRU_ICSSG MDIO Data	IO	AD18
PRG1_PRU0_GPI0	PRU_ICSSG PRU Data Input	I	AE22
PRG1_PRU0_GPI1	PRU_ICSSG PRU Data Input	I	AG24
PRG1_PRU0_GPI2	PRU_ICSSG PRU Data Input	I	AF23
PRG1_PRU0_GPI3	PRU_ICSSG PRU Data Input	I	AD21
PRG1_PRU0_GPI4	PRU_ICSSG PRU Data Input	I	AG23
PRG1_PRU0_GPI5	PRU_ICSSG PRU Data Input	I	AF27
PRG1_PRU0_GPI6	PRU_ICSSG PRU Data Input	I	AF22
PRG1_PRU0_GPI7	PRU_ICSSG PRU Data Input	I	AG27
PRG1_PRU0_GPI8	PRU_ICSSG PRU Data Input	I	AF28
PRG1_PRU0_GPI9	PRU_ICSSG PRU Data Input	I	AF26
PRG1_PRU0_GPI10	PRU_ICSSG PRU Data Input	I	AH25
PRG1_PRU0_GPI11	PRU_ICSSG PRU Data Input	I	AF21
PRG1_PRU0_GPI12	PRU_ICSSG PRU Data Input	I	AH20
PRG1_PRU0_GPI13	PRU_ICSSG PRU Data Input	I	AH21
PRG1_PRU0_GPI14	PRU_ICSSG PRU Data Input	I	AG20
PRG1_PRU0_GPI15	PRU_ICSSG PRU Data Input	I	AD19
PRG1_PRU0_GPI16	PRU_ICSSG PRU Data Input	I	AD20
PRG1_PRU0_GPI17	PRU_ICSSG PRU Data Input	I	AH26
PRG1_PRU0_GPI18	PRU_ICSSG PRU Data Input	I	AG25
PRG1_PRU0_GPI19	PRU_ICSSG PRU Data Input	I	AG26
PRG1_PRU0_GPO0	PRU_ICSSG PRU Data Output	IO	AE22
PRG1_PRU0_GPO1	PRU_ICSSG PRU Data Output	IO	AG24
PRG1_PRU0_GPO2	PRU_ICSSG PRU Data Output	IO	AF23
PRG1_PRU0_GPO3	PRU_ICSSG PRU Data Output	IO	AD21
PRG1_PRU0_GPO4	PRU_ICSSG PRU Data Output	IO	AG23
PRG1_PRU0_GPO5	PRU_ICSSG PRU Data Output	IO	AF27
PRG1_PRU0_GPO6	PRU_ICSSG PRU Data Output	IO	AF22
PRG1_PRU0_GPO7	PRU_ICSSG PRU Data Output	IO	AG27

表 4-53. PRU_ICSSG1 Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
PRG1_PRU0_GPO8	PRU_ICSSG PRU Data Output	IO	AF28
PRG1_PRU0_GPO9	PRU_ICSSG PRU Data Output	IO	AF26
PRG1_PRU0_GPO10	PRU_ICSSG PRU Data Output	IO	AH25
PRG1_PRU0_GPO11	PRU_ICSSG PRU Data Output	IO	AF21
PRG1_PRU0_GPO12	PRU_ICSSG PRU Data Output	IO	AH20
PRG1_PRU0_GPO13	PRU_ICSSG PRU Data Output	IO	AH21
PRG1_PRU0_GPO14	PRU_ICSSG PRU Data Output	IO	AG20
PRG1_PRU0_GPO15	PRU_ICSSG PRU Data Output	IO	AD19
PRG1_PRU0_GPO16	PRU_ICSSG PRU Data Output	IO	AD20
PRG1_PRU0_GPO17	PRU_ICSSG PRU Data Output	IO	AH26
PRG1_PRU0_GPO18	PRU_ICSSG PRU Data Output	IO	AG25
PRG1_PRU0_GPO19	PRU_ICSSG PRU Data Output	IO	AG26
PRG1_PRU1_GPI0	PRU_ICSSG PRU Data Input	I	AH24
PRG1_PRU1_GPI1	PRU_ICSSG PRU Data Input	I	AH23
PRG1_PRU1_GPI2	PRU_ICSSG PRU Data Input	I	AG21
PRG1_PRU1_GPI3	PRU_ICSSG PRU Data Input	I	AH22
PRG1_PRU1_GPI4	PRU_ICSSG PRU Data Input	I	AE21
PRG1_PRU1_GPI5	PRU_ICSSG PRU Data Input	I	AC22
PRG1_PRU1_GPI6	PRU_ICSSG PRU Data Input	I	AG22
PRG1_PRU1_GPI7	PRU_ICSSG PRU Data Input	I	AD23
PRG1_PRU1_GPI8	PRU_ICSSG PRU Data Input	I	AE24
PRG1_PRU1_GPI9	PRU_ICSSG PRU Data Input	I	AF25
PRG1_PRU1_GPI10	PRU_ICSSG PRU Data Input	I	AF24
PRG1_PRU1_GPI11	PRU_ICSSG PRU Data Input	I	AC20
PRG1_PRU1_GPI12	PRU_ICSSG PRU Data Input	I	AE20
PRG1_PRU1_GPI13	PRU_ICSSG PRU Data Input	I	AF19
PRG1_PRU1_GPI14	PRU_ICSSG PRU Data Input	I	AH19
PRG1_PRU1_GPI15	PRU_ICSSG PRU Data Input	I	AG19
PRG1_PRU1_GPI16	PRU_ICSSG PRU Data Input	I	AE19
PRG1_PRU1_GPI17	PRU_ICSSG PRU Data Input	I	AE23
PRG1_PRU1_GPI18	PRU_ICSSG PRU Data Input	I	AD22
PRG1_PRU1_GPI19	PRU_ICSSG PRU Data Input	I	AC21
PRG1_PRU1_GPO0	PRU_ICSSG PRU Data Output	IO	AH24
PRG1_PRU1_GPO1	PRU_ICSSG PRU Data Output	IO	AH23
PRG1_PRU1_GPO2	PRU_ICSSG PRU Data Output	IO	AG21
PRG1_PRU1_GPO3	PRU_ICSSG PRU Data Output	IO	AH22
PRG1_PRU1_GPO4	PRU_ICSSG PRU Data Output	IO	AE21
PRG1_PRU1_GPO5	PRU_ICSSG PRU Data Output	IO	AC22
PRG1_PRU1_GPO6	PRU_ICSSG PRU Data Output	IO	AG22
PRG1_PRU1_GPO7	PRU_ICSSG PRU Data Output	IO	AD23
PRG1_PRU1_GPO8	PRU_ICSSG PRU Data Output	IO	AE24
PRG1_PRU1_GPO9	PRU_ICSSG PRU Data Output	IO	AF25
PRG1_PRU1_GPO10	PRU_ICSSG PRU Data Output	IO	AF24
PRG1_PRU1_GPO11	PRU_ICSSG PRU Data Output	IO	AC20
PRG1_PRU1_GPO12	PRU_ICSSG PRU Data Output	IO	AE20
PRG1_PRU1_GPO13	PRU_ICSSG PRU Data Output	IO	AF19
PRG1_PRU1_GPO14	PRU_ICSSG PRU Data Output	IO	AH19

表 4-53. PRU_ICSSG1 Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
PRG1_PRU1_GPO15	PRU_ICSSG PRU Data Output	IO	AG19
PRG1_PRU1_GPO16	PRU_ICSSG PRU Data Output	IO	AE19
PRG1_PRU1_GPO17	PRU_ICSSG PRU Data Output	IO	AE23
PRG1_PRU1_GPO18	PRU_ICSSG PRU Data Output	IO	AD22
PRG1_PRU1_GPO19	PRU_ICSSG PRU Data Output	IO	AC21
PRG1_PWM0_TZ_IN	PRU_ICSSG PWM Trip Zone Input	I	AG25
PRG1_PWM0_TZ_OUT	PRU_ICSSG PWM Trip Zone Output	O	AG26
PRG1_PWM1_TZ_IN	PRU_ICSSG PWM Trip Zone Input	I	AD22
PRG1_PWM1_TZ_OUT	PRU_ICSSG PWM Trip Zone Output	O	AC21
PRG1_PWM2_TZ_IN	PRU_ICSSG PWM Trip Zone Input	I	AF24
PRG1_PWM2_TZ_OUT	PRU_ICSSG PWM Trip Zone Output	O	AE24
PRG1_PWM3_TZ_IN	PRU_ICSSG PWM Trip Zone Input	I	AF26
PRG1_PWM3_TZ_OUT	PRU_ICSSG PWM Trip Zone Output	O	AF21
PRG1_PWM0_A0	PRU_ICSSG PWM Output A	IO	AH20
PRG1_PWM0_A1	PRU_ICSSG PWM Output A	IO	AG20
PRG1_PWM0_A2	PRU_ICSSG PWM Output A	IO	AD20
PRG1_PWM0_B0	PRU_ICSSG PWM Output B	IO	AH21
PRG1_PWM0_B1	PRU_ICSSG PWM Output B	IO	AD19
PRG1_PWM0_B2	PRU_ICSSG PWM Output B	IO	AH26
PRG1_PWM1_A0	PRU_ICSSG PWM Output A	IO	AE20
PRG1_PWM1_A1	PRU_ICSSG PWM Output A	IO	AH19
PRG1_PWM1_A2	PRU_ICSSG PWM Output A	IO	AE19
PRG1_PWM1_B0	PRU_ICSSG PWM Output B	IO	AF19
PRG1_PWM1_B1	PRU_ICSSG PWM Output B	IO	AG19
PRG1_PWM1_B2	PRU_ICSSG PWM Output B	IO	AE23
PRG1_PWM2_A0	PRU_ICSSG PWM Output A	IO	AF23
PRG1_PWM2_A1	PRU_ICSSG PWM Output A	IO	AF28
PRG1_PWM2_A2	PRU_ICSSG PWM Output A	IO	AG21
PRG1_PWM2_B0	PRU_ICSSG PWM Output B	IO	AG23
PRG1_PWM2_B1	PRU_ICSSG PWM Output B	IO	AH25
PRG1_PWM2_B2	PRU_ICSSG PWM Output B	IO	AE21
PRG1_PWM3_A0	PRU_ICSSG PWM Output A	IO	AE22
PRG1_PWM3_A1	PRU_ICSSG PWM Output A	IO	AF22
PRG1_PWM3_A2	PRU_ICSSG PWM Output A	IO	AD21
PRG1_PWM3_B0	PRU_ICSSG PWM Output B	IO	AG24
PRG1_PWM3_B1	PRU_ICSSG PWM Output B	IO	AG27
PRG1_PWM3_B2	PRU_ICSSG PWM Output B	IO	AF27
PRG1_RGMII1_RXC	PRU_ICSSG RGMII Receive Clock	I	AF22
PRG1_RGMII1_RX_CTL	PRU_ICSSG RGMII Receive Control	I	AG23
PRG1_RGMII1_TXC	PRU_ICSSG RGMII Transmit Clock	IO	AD20
PRG1_RGMII1_TX_CTL	PRU_ICSSG RGMII Transmit Control	O	AF21
PRG1_RGMII2_RXC	PRU_ICSSG RGMII Receive Clock	I	AG22
PRG1_RGMII2_RX_CTL	PRU_ICSSG RGMII Receive Control	I	AE21
PRG1_RGMII2_TXC	PRU_ICSSG RGMII Transmit Clock	IO	AE19
PRG1_RGMII2_TX_CTL	PRU_ICSSG RGMII Transmit Control	O	AC20
PRG1_RGMII1_RD0	PRU_ICSSG RGMII Receive Data	I	AE22
PRG1_RGMII1_RD1	PRU_ICSSG RGMII Receive Data	I	AG24

表 4-53. PRU_ICSSG1 Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
PRG1_RGMII1_RD2	PRU_ICSSG RGMII Receive Data	I	AF23
PRG1_RGMII1_RD3	PRU_ICSSG RGMII Receive Data	I	AD21
PRG1_RGMII1_TD0	PRU_ICSSG RGMII Transmit Data	O	AH20
PRG1_RGMII1_TD1	PRU_ICSSG RGMII Transmit Data	O	AH21
PRG1_RGMII1_TD2	PRU_ICSSG RGMII Transmit Data	O	AG20
PRG1_RGMII1_TD3	PRU_ICSSG RGMII Transmit Data	O	AD19
PRG1_RGMII2_RD0	PRU_ICSSG RGMII Receive Data	I	AH24
PRG1_RGMII2_RD1	PRU_ICSSG RGMII Receive Data	I	AH23
PRG1_RGMII2_RD2	PRU_ICSSG RGMII Receive Data	I	AG21
PRG1_RGMII2_RD3	PRU_ICSSG RGMII Receive Data	I	AH22
PRG1_RGMII2_TD0	PRU_ICSSG RGMII Transmit Data	O	AE20
PRG1_RGMII2_TD1	PRU_ICSSG RGMII Transmit Data	O	AF19
PRG1_RGMII2_TD2	PRU_ICSSG RGMII Transmit Data	O	AH19
PRG1_RGMII2_TD3	PRU_ICSSG RGMII Transmit Data	O	AG19
PRG1_UART0_CTSn	PRU_ICSSG UART Clear to Send (active low)	I	AF26
PRG1_UART0_RTSn	PRU_ICSSG UART Request to Send (active low)	O	AH25
PRG1_UART0_RXD	PRU_ICSSG UART Receive Data	I	AF25
PRG1_UART0_TXD	PRU_ICSSG UART Transmit Data	O	AF24

表 4-54. PRU_ICSSG2 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
PRG2_ECAP0_IN_APWM_OUT	PRU_ICSSG Enhanced Capture (ECAP) Input or Auxiliary PWM (APWM) Output	IO	AE16
PRG2_ECAP0_SYNC_IN	PRU_ICSSG ECAP Sync Input	I	AD14
PRG2_ECAP0_SYNC_OUT	PRU_ICSSG ECAP Sync Output	O	AG14
PRG2_IEP0_EDIO_OUTVALID	PRU_ICSSG Industrial Ethernet Digital I/O Outvalid	O ⁽¹⁾	A23
PRG2_IEP0_EDC_LATCH_IN0	PRU_ICSSG Industrial Ethernet Distributed Clock Latch Input	I	AD12
PRG2_IEP0_EDC_LATCH_IN1	PRU_ICSSG Industrial Ethernet Distributed Clock Latch Input	I	AE12
PRG2_IEP0_EDC_SYNC_OUT0	PRU_ICSSG Industrial Ethernet Distributed Clock Sync Output	O	AH12
PRG2_IEP0_EDC_SYNC_OUT1	PRU_ICSSG Industrial Ethernet Distributed Clock Sync Output	O	AF12
PRG2_IEP0_EDIO_DATA_IN_OUT28	PRU_ICSSG Industrial Ethernet Digital I/O Data Input/Output	IO	R23
PRG2_IEP0_EDIO_DATA_IN_OUT29	PRU_ICSSG Industrial Ethernet Digital I/O Data Input/Output	IO	T24
PRG2_IEP0_EDIO_DATA_IN_OUT30	PRU_ICSSG Industrial Ethernet Digital I/O Data Input/Output	IO	R25
PRG2_IEP0_EDIO_DATA_IN_OUT31	PRU_ICSSG Industrial Ethernet Digital I/O Data Input/Output	IO	T27
PRG2_IEP1_EDC_LATCH_IN0	PRU_ICSSG Industrial Ethernet Distributed Clock Latch Input	I	R23
PRG2_IEP1_EDC_LATCH_IN1	PRU_ICSSG Industrial Ethernet Distributed Clock Latch Input	I	R25
PRG2_IEP1_EDC_SYNC_OUT0	PRU_ICSSG Industrial Ethernet Distributed Clock Sync Output	O	T24
PRG2_IEP1_EDC_SYNC_OUT1	PRU_ICSSG Industrial Ethernet Distributed Clock Sync Output	O	T27

表 4-54. PRU_ICSSG2 Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
PRG2_MDIO0_MDC	PRU_ICSSG MDIO Clock	O	AE15
PRG2_MDIO0_MDIO	PRU_ICSSG MDIO Data	IO	AC19
PRG2_PRU0_GPI0	PRU_ICSSG PRU Data Input	I	AF18
PRG2_PRU0_GPI1	PRU_ICSSG PRU Data Input	I	AE18
PRG2_PRU0_GPI2	PRU_ICSSG PRU Data Input	I	AH17
PRG2_PRU0_GPI3	PRU_ICSSG PRU Data Input	I	AG18
PRG2_PRU0_GPI4	PRU_ICSSG PRU Data Input	I	AG17
PRG2_PRU0_GPI5	PRU_ICSSG PRU Data Input	I	AF17
PRG2_PRU0_GPI6	PRU_ICSSG PRU Data Input	I	AE17
PRG2_PRU0_GPI7	PRU_ICSSG PRU Data Input	I	AC19
PRG2_PRU0_GPI8	PRU_ICSSG PRU Data Input	I	AH16
PRG2_PRU0_GPI9	PRU_ICSSG PRU Data Input	I	AG16
PRG2_PRU0_GPI10	PRU_ICSSG PRU Data Input	I	AF16
PRG2_PRU0_GPI11	PRU_ICSSG PRU Data Input	I	AE16
PRG2_PRU0_GPI12	PRU_ICSSG PRU Data Input	I	N23
PRG2_PRU0_GPI13	PRU_ICSSG PRU Data Input	I	M26
PRG2_PRU0_GPI14	PRU_ICSSG PRU Data Input	I	P28
PRG2_PRU0_GPI15	PRU_ICSSG PRU Data Input	I	P27
PRG2_PRU0_GPI16	PRU_ICSSG PRU Data Input	I	AD16
PRG2_PRU0_GPI17	PRU_ICSSG PRU Data Input	I	P23
PRG2_PRU0_GPO0	PRU_ICSSG PRU Data Output	IO	AF18
PRG2_PRU0_GPO1	PRU_ICSSG PRU Data Output	IO	AE18
PRG2_PRU0_GPO2	PRU_ICSSG PRU Data Output	IO	AH17
PRG2_PRU0_GPO3	PRU_ICSSG PRU Data Output	IO	AG18
PRG2_PRU0_GPO4	PRU_ICSSG PRU Data Output	IO	AG17
PRG2_PRU0_GPO5	PRU_ICSSG PRU Data Output	IO	AF17
PRG2_PRU0_GPO6	PRU_ICSSG PRU Data Output	IO	AE17
PRG2_PRU0_GPO7	PRU_ICSSG PRU Data Output	IO	AC19
PRG2_PRU0_GPO8	PRU_ICSSG PRU Data Output	IO	AH16
PRG2_PRU0_GPO9	PRU_ICSSG PRU Data Output	IO	AG16
PRG2_PRU0_GPO10	PRU_ICSSG PRU Data Output	IO	AF16
PRG2_PRU0_GPO11	PRU_ICSSG PRU Data Output	IO	AE16
PRG2_PRU0_GPO12	PRU_ICSSG PRU Data Output	IO	N23
PRG2_PRU0_GPO13	PRU_ICSSG PRU Data Output	IO	M26
PRG2_PRU0_GPO14	PRU_ICSSG PRU Data Output	IO	P28
PRG2_PRU0_GPO15	PRU_ICSSG PRU Data Output	IO	P27
PRG2_PRU0_GPO16	PRU_ICSSG PRU Data Output	IO	AD16
PRG2_PRU0_GPO17	PRU_ICSSG PRU Data Output	IO	P23
PRG2_PRU1_GPI0	PRU_ICSSG PRU Data Input	I	AH15
PRG2_PRU1_GPI1	PRU_ICSSG PRU Data Input	I	AC16
PRG2_PRU1_GPI2	PRU_ICSSG PRU Data Input	I	AD17
PRG2_PRU1_GPI3	PRU_ICSSG PRU Data Input	I	AH14
PRG2_PRU1_GPI4	PRU_ICSSG PRU Data Input	I	AG14
PRG2_PRU1_GPI5	PRU_ICSSG PRU Data Input	I	AG15
PRG2_PRU1_GPI6	PRU_ICSSG PRU Data Input	I	AC17
PRG2_PRU1_GPI7	PRU_ICSSG PRU Data Input	I	AE15
PRG2_PRU1_GPI8	PRU_ICSSG PRU Data Input	I	AD15

表 4-54. PRU_ICSSG2 Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
PRG2_PRU1_GPI9	PRU_ICSSG PRU Data Input	I	AF14
PRG2_PRU1_GPI10	PRU_ICSSG PRU Data Input	I	AC15
PRG2_PRU1_GPI11	PRU_ICSSG PRU Data Input	I	AD14
PRG2_PRU1_GPI12	PRU_ICSSG PRU Data Input	I	N26
PRG2_PRU1_GPI13	PRU_ICSSG PRU Data Input	I	N25
PRG2_PRU1_GPI14	PRU_ICSSG PRU Data Input	I	P24
PRG2_PRU1_GPI15	PRU_ICSSG PRU Data Input	I	R27
PRG2_PRU1_GPI16	PRU_ICSSG PRU Data Input	I	AE14
PRG2_PRU1_GPI17	PRU_ICSSG PRU Data Input	I	T23
PRG2_PRU1_GPO0	PRU_ICSSG PRU Data Output	IO	AH15
PRG2_PRU1_GPO1	PRU_ICSSG PRU Data Output	IO	AC16
PRG2_PRU1_GPO2	PRU_ICSSG PRU Data Output	IO	AD17
PRG2_PRU1_GPO3	PRU_ICSSG PRU Data Output	IO	AH14
PRG2_PRU1_GPO4	PRU_ICSSG PRU Data Output	IO	AG14
PRG2_PRU1_GPO5	PRU_ICSSG PRU Data Output	IO	AG15
PRG2_PRU1_GPO6	PRU_ICSSG PRU Data Output	IO	AC17
PRG2_PRU1_GPO7	PRU_ICSSG PRU Data Output	IO	AE15
PRG2_PRU1_GPO8	PRU_ICSSG PRU Data Output	IO	AD15
PRG2_PRU1_GPO9	PRU_ICSSG PRU Data Output	IO	AF14
PRG2_PRU1_GPO10	PRU_ICSSG PRU Data Output	IO	AC15
PRG2_PRU1_GPO11	PRU_ICSSG PRU Data Output	IO	AD14
PRG2_PRU1_GPO12	PRU_ICSSG PRU Data Output	IO	N26
PRG2_PRU1_GPO13	PRU_ICSSG PRU Data Output	IO	N25
PRG2_PRU1_GPO14	PRU_ICSSG PRU Data Output	IO	P24
PRG2_PRU1_GPO15	PRU_ICSSG PRU Data Output	IO	R27
PRG2_PRU1_GPO16	PRU_ICSSG PRU Data Output	IO	AE14
PRG2_PRU1_GPO17	PRU_ICSSG PRU Data Output	IO	T23
PRG2_PWM0_TZ_IN	PRU_ICSSG PWM Trip Zone Input	I	P28
PRG2_PWM0_TZ_OUT	PRU_ICSSG PWM Trip Zone Output	O	P24
PRG2_PWM1_TZ_IN	PRU_ICSSG PWM Trip Zone Input	I	F18
PRG2_PWM1_TZ_OUT	PRU_ICSSG PWM Trip Zone Output	O	AE14
PRG2_PWM2_TZ_IN	PRU_ICSSG PWM Trip Zone Input	I	P23
PRG2_PWM2_TZ_OUT	PRU_ICSSG PWM Trip Zone Output	O	T23
PRG2_PWM3_TZ_IN	PRU_ICSSG PWM Trip Zone Input	I	AE15
PRG2_PWM3_TZ_OUT	PRU_ICSSG PWM Trip Zone Output	O	AF14
PRG2_PWM0_A0	PRU_ICSSG PWM Output A	IO	AG17
PRG2_PWM0_A1	PRU_ICSSG PWM Output A	IO	AD16
PRG2_PWM0_A2	PRU_ICSSG PWM Output A	IO	AD15
PRG2_PWM0_B0	PRU_ICSSG PWM Output B	IO	AH16
PRG2_PWM0_B1	PRU_ICSSG PWM Output B	IO	AD17
PRG2_PWM0_B2	PRU_ICSSG PWM Output B	IO	AC15
PRG2_PWM1_A0	PRU_ICSSG PWM Output A	IO	R23
PRG2_PWM1_A1	PRU_ICSSG PWM Output A	IO	AD18
PRG2_PWM1_A2	PRU_ICSSG PWM Output A	IO	AE26
PRG2_PWM1_B0	PRU_ICSSG PWM Output B	IO	T24
PRG2_PWM1_B1	PRU_ICSSG PWM Output B	IO	AH18
PRG2_PWM1_B2	PRU_ICSSG PWM Output B	IO	AE28

表 4-54. PRU_ICSSG2 Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
PRG2_PWM2_A0	PRU_ICSSG PWM Output A	IO	N23
PRG2_PWM2_A1	PRU_ICSSG PWM Output A	IO	P27
PRG2_PWM2_A2	PRU_ICSSG PWM Output A	IO	N25
PRG2_PWM2_B0	PRU_ICSSG PWM Output B	IO	M26
PRG2_PWM2_B1	PRU_ICSSG PWM Output B	IO	N26
PRG2_PWM2_B2	PRU_ICSSG PWM Output B	IO	R27
PRG2_PWM3_A0	PRU_ICSSG PWM Output A	IO	AF18
PRG2_PWM3_A1	PRU_ICSSG PWM Output A	IO	AF17
PRG2_PWM3_A2	PRU_ICSSG PWM Output A	IO	AH15
PRG2_PWM3_B0	PRU_ICSSG PWM Output B	IO	AG18
PRG2_PWM3_B1	PRU_ICSSG PWM Output B	IO	AE17
PRG2_PWM3_B2	PRU_ICSSG PWM Output B	IO	AC16
PRG2_RGMII1_RXC	PRU_ICSSG RGMII Receive Clock	I	AF17
PRG2_RGMII1_RX_CTL	PRU_ICSSG RGMII Receive Control	I	AG17
PRG2_RGMII1_TXC	PRU_ICSSG RGMII Transmit Clock	IO	AD16
PRG2_RGMII1_TX_CTL	PRU_ICSSG RGMII Transmit Control	O	AE17
PRG2_RGMII2_RXC	PRU_ICSSG RGMII Receive Clock	I	AG15
PRG2_RGMII2_RX_CTL	PRU_ICSSG RGMII Receive Control	I	AG14
PRG2_RGMII2_TXC	PRU_ICSSG RGMII Transmit Clock	IO	AE14
PRG2_RGMII2_TX_CTL	PRU_ICSSG RGMII Transmit Control	O	AC17
PRG2_RGMII1_RD0	PRU_ICSSG RGMII Receive Data	I	AF18
PRG2_RGMII1_RD1	PRU_ICSSG RGMII Receive Data	I	AE18
PRG2_RGMII1_RD2	PRU_ICSSG RGMII Receive Data	I	AH17
PRG2_RGMII1_RD3	PRU_ICSSG RGMII Receive Data	I	AG18
PRG2_RGMII1_TD0	PRU_ICSSG RGMII Transmit Data	O	AH16
PRG2_RGMII1_TD1	PRU_ICSSG RGMII Transmit Data	O	AG16
PRG2_RGMII1_TD2	PRU_ICSSG RGMII Transmit Data	O	AF16
PRG2_RGMII1_TD3	PRU_ICSSG RGMII Transmit Data	O	AE16
PRG2_RGMII2_RD0	PRU_ICSSG RGMII Receive Data	I	AH15
PRG2_RGMII2_RD1	PRU_ICSSG RGMII Receive Data	I	AC16
PRG2_RGMII2_RD2	PRU_ICSSG RGMII Receive Data	I	AD17
PRG2_RGMII2_RD3	PRU_ICSSG RGMII Receive Data	I	AH14
PRG2_RGMII2_TD0	PRU_ICSSG RGMII Transmit Data	O	AD15
PRG2_RGMII2_TD1	PRU_ICSSG RGMII Transmit Data	O	AF14
PRG2_RGMII2_TD2	PRU_ICSSG RGMII Transmit Data	O	AC15
PRG2_RGMII2_TD3	PRU_ICSSG RGMII Transmit Data	O	AD14
PRG2_UART0_CTSn	PRU_ICSSG UART Clear to Send (active low)	I	AD12
PRG2_UART0_RTSn	PRU_ICSSG UART Request to Send (active low)	O	AH12
PRG2_UART0_RXD	PRU_ICSSG UART Receive Data	I	AE12
PRG2_UART0_TXD	PRU_ICSSG UART Transmit Data	O	AF12

(1) When OSC1 is being used with an external crystal, this signal is unavailable. The output functionality must be disabled.

4.3.22 SERDES

4.3.22.1 MAIN Domain

表 4-55. SERDES0 Signal Descriptions⁽¹⁾

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
SERDES0_REFCLKN	SERDES Clock Input (negative)	I	AG5
SERDES0_REFCLKP	SERDES Clock Input (positive)	I	AG6
SERDES0_REFRES	SERDES Reference Resistor ⁽²⁾	A	AC9
SERDES0_RXN	SERDES Differential Receive Data (negative)	I	AH3
SERDES0_RXP	SERDES Differential Receive Data (positive)	I	AG2
SERDES0_TXN	SERDES Differential Transmit Data (negative)	O	AH4
SERDES0_TXP	SERDES Differential Transmit Data (positive)	O	AG3

(1) The functionality of these pins is controlled by CTRLMMR_SERDES0_CTRL[1:0] LANE_FUNC_SEL. 0x0 = USB3, 0x1 = PCIe0 Lane0, 0x2 = ICSS2 SGMII Lane0.

(2) The required resistor value is 3kΩ ±1%.

表 4-56. SERDES1 Signal Descriptions⁽¹⁾

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
SERDES1_REFCLKN	SERDES Clock Input (negative)	I	AH6
SERDES1_REFCLKP	SERDES Clock Input (positive)	I	AH7
SERDES1_REFRES	SERDES Reference Resistor ⁽²⁾	A	AC14
SERDES1_RXN	SERDES Differential Receive Data (negative)	I	AG9
SERDES1_RXP	SERDES Differential Receive Data (positive)	I	AH10
SERDES1_TXN	SERDES Differential Transmit Data (negative)	O	AH9
SERDES1_TXP	SERDES Differential Transmit Data (positive)	O	AG8

(1) The functionality of these pins is controlled by CTRLMMR_SERDES1_CTRL[1:0] LANE_FUNC_SEL. 0x0 = PCIe1 Lane0, 0x1 = PCIe0 Lane1, 0x2 = ICSS2 SGMII Lane1.

(2) The required resistor value is 3kΩ ±1%.

4.3.23 UART

4.3.23.1 MAIN Domain

表 4-57. UART0 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
UART0_CTSn	UART Clear to Send (active low)	I	AG11
UART0_DCDn	UART Data Carrier Detect (active low)	I	D25
UART0_DSRn	UART Data Set Ready (active low)	I	B26
UART0_DTRn	UART Data Terminal Ready (active low)	O	A24
UART0_RIN	UART Ring Indicator	I	E24
UART0_RTSn	UART Request to Send (active low)	O	AD11
UART0_RXD	UART Receive Data	I	AF11
UART0_TXD	UART Transmit Data	O	AE11

表 4-58. UART1 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
UART1_CTSn	UART Clear to Send (active low)	I	AD22
UART1_RTSn	UART Request to Send (active low)	O	AC21
UART1_RXD	UART Receive Data	I	AE23
UART1_TXD	UART Transmit Data	O	AD23

表 4-59. UART2 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
UART2_CTSn	UART Clear to Send (active low)	I	Y26
UART2_RTSn	UART Request to Send (active low)	O	W26
UART2_RXD	UART Receive Data	I	Y27
UART2_TXD	UART Transmit Data	O	W28

4.3.23.2 MCU Domain

表 4-60. UART0 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
MCU_UART0_CTSn	UART Clear to Send (active low)	I	P1
MCU_UART0_RTSn	UART Request to Send (active low)	O	N3
MCU_UART0_RXD	UART Receive Data	I	P4
MCU_UART0_TXD	UART Transmit Data	O	P5

4.3.23.3 WKUP Domain

表 4-61. UART0 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
WKUP_UART0_CTSn	UART Clear to Send (active low)	I	AC2
WKUP_UART0_RTSn	UART Request to Send (active low)	O	AC1
WKUP_UART0_RXD	UART Receive Data	I	AB1
WKUP_UART0_TXD	UART Transmit Data	O	AB5

4.3.24 USB

4.3.24.1 MAIN Domain

表 4-62. USB0 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
USB0_DM	USB 2.0 Differential Data (negative)	IO	AE2
USB0_DP	USB 2.0 Differential Data (positive)	IO	AF1
USB0_DRVVBUS	USB VBUS control output (active high)	O	AD9
USB0_ID	USB 2.0 Dual-Role Device Role Select	A	AF7
USB0_VBUS ⁽¹⁾	USB Level-shifted VBUS Input	A	AE7

- (1) An external resistor divider is required to limit the voltage applied to the device pin. For more information, see [7.4, USB Design Guidelines](#).

表 4-63. USB1 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
USB1_DM	USB 2.0 Differential Data (negative)	IO	AD2
USB1_DP	USB 2.0 Differential Data (positive)	IO	AE1
USB1_DRVVBUS	USB VBUS control output (active high)	O	AC8
USB1_ID	USB 2.0 Dual-Role Device Role Select	A	AF5
USB1_VBUS ⁽¹⁾	USB Level-shifted VBUS Input	A	AF6

- (1) An external resistor divider is required to limit the voltage applied to the device pin. For more information, see [7.4, USB Design Guidelines](#).

4.3.25 Emulation and Debug

4.3.25.1 MAIN Domain

表 4-64. Emulation and Debug 0 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
EMU0	Emulation Control 0	IO	AA2
EMU1	Emulation Control 1	IO	AA1
TCK	JTAG Test Clock Input	I	AA4
TDI	JTAG Test Data Input	I	C20
TDO	JTAG Test Data Output	OZ	A20
TMS	JTAG Test Mode Select Input	I	A21
TRSTn	JTAG Reset	I	AA3
TRC_CLK	Trace Clock	O	AF18
TRC_CTL	Trace Control	O	AE18
TRC_DATA0	Trace Data 0	O	AH17
TRC_DATA1	Trace Data 1	O	AG18
TRC_DATA2	Trace Data 2	O	AG17
TRC_DATA3	Trace Data 3	O	AF17
TRC_DATA4	Trace Data 4	O	AE17
TRC_DATA5	Trace Data 5	O	AC19
TRC_DATA6	Trace Data 6	O	AH16
TRC_DATA7	Trace Data 7	O	AG16
TRC_DATA8	Trace Data 8	O	AF16
TRC_DATA9	Trace Data 9	O	AE16
TRC_DATA10	Trace Data 10	O	AD16
TRC_DATA11	Trace Data 11	O	AH15
TRC_DATA12	Trace Data 12	O	AC16
TRC_DATA13	Trace Data 13	O	AD17
TRC_DATA14	Trace Data 14	O	AH14
TRC_DATA15	Trace Data 15	O	AG14
TRC_DATA16	Trace Data 16	O	AG15
TRC_DATA17	Trace Data 17	O	AC17
TRC_DATA18	Trace Data 18	O	AE15
TRC_DATA19	Trace Data 19	O	AD15
TRC_DATA20	Trace Data 20	O	AF14

表 4-64. Emulation and Debug 0 Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
TRC_DATA21	Trace Data 21	O	AC15
TRC_DATA22	Trace Data 22	O	AD14
TRC_DATA23	Trace Data 23	O	AE14

4.3.26 System and Miscellaneous

4.3.26.1 Boot Mode Configuration

4.3.26.1.1 MAIN Domain

表 4-65. Sysboot Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
BOOTMODE00	Bootmode pin 00	I	M27
BOOTMODE01	Bootmode pin 01	I	M23
BOOTMODE02	Bootmode pin 02	I	M28
BOOTMODE03	Bootmode pin 03	I	M24
BOOTMODE04	Bootmode pin 04	I	N24
BOOTMODE05	Bootmode pin 05	I	N27
BOOTMODE06	Bootmode pin 06	I	N28
BOOTMODE07	Bootmode pin 07	I	M25
BOOTMODE08	Bootmode pin 08	I	N23
BOOTMODE09	Bootmode pin 09	I	M26
BOOTMODE10	Bootmode pin 10	I	P28
BOOTMODE11	Bootmode pin 11	I	P27
BOOTMODE12	Bootmode pin 12	I	N26
BOOTMODE13	Bootmode pin 13	I	N25
BOOTMODE14	Bootmode pin 14	I	P24
BOOTMODE15	Bootmode pin 15	I	R27
BOOTMODE16	Bootmode pin 16	I	P25
BOOTMODE17	Bootmode pin 17	I	P26
BOOTMODE18	Bootmode pin 18	I	U28

4.3.26.1.2 MCU Domain

表 4-66. Sysboot Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
MCU_BOOTMODE00	Bootmode pin 00	I	AF4
MCU_BOOTMODE01	Bootmode pin 01	I	AF3
MCU_BOOTMODE02	Bootmode pin 02	I	AE3
MCU_BOOTMODE03 ⁽¹⁾	Bootmode pin 03	I	AD1
MCU_BOOTMODE04 ⁽¹⁾	Bootmode pin 04	I	AC3
MCU_BOOTMODE05 ⁽¹⁾	Bootmode pin 05	I	Y2
MCU_BOOTMODE06 ⁽¹⁾	Bootmode pin 06	I	Y1
MCU_BOOTMODE07 ⁽¹⁾	Bootmode pin 07	I	Y3
MCU_BOOTMODE08 ⁽¹⁾	Bootmode pin 08	I	AC5
MCU_BOOTMODE09	Bootmode pin 09	I	AB4

- (1) These signals must be connected to VSS through a separate external pull resistor to ensure these balls are held to a valid logic low level.

4.3.26.2 Clock

4.3.26.2.1 MAIN Domain

表 4-67. Clock1 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
OSC1_XI	High frequency oscillator input	I	C22
OSC1_XO	High frequency oscillator output	O	E22

4.3.26.2.2 WKUP Domain

表 4-68. Clock0 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
WKUP_LFOSC0_XI	Low frequency (32.768 KHz) oscillator input	I	AE4
WKUP_LFOSC0_XO	Low frequency (32.768 KHz) oscillator output	O	AC4
WKUP_OSC0_XI	High frequency oscillator input	I	AD5
WKUP_OSC0_XO	High frequency oscillator output	O	AE6

4.3.26.3 System

4.3.26.3.1 MAIN Domain

表 4-69. System0 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
EXT_REFCLK1	External clock input to Main Domain, routed to Timer clock muxes as one of the selectable input clock sources for Timer/WDT modules, or as reference clock to MAIN_PLL2 (PER1 PLL)	I	A22
NMIIn	External Interrupt	I	F18
OBSCLK0	Observation clock output for test and debug purposes only	O	C23
PORz	Main Domain cold reset	I	E19
PORz_OUT	Main Domain POR status output	O	C19
REFCLK0N	SERDES Differential Clock Output (negative)	O	AF9
REFCLK0P	SERDES Differential Clock Output (positive)	O	AF10
REFCLK1N	SERDES Differential Clock Output (negative)	O	AE8
REFCLK1P	SERDES Differential Clock Output (positive)	O	AE9
RESETSTATz	Main Domain warm reset status output	O	D19
RESETz	Main Domain warm reset	I	F17
SOC_SAFETY_ERRORn	Error signal output from Main Domain ESM	IO	E20
SYNC0_OUT	CPTS Time Stamp Generator Bit 0	O	D21
SYNC1_OUT	CPTS Time Stamp Generator Bit 1	O	A22
SYNC2_OUT	CPTS Time Stamp Generator Bit 2	O	AE18
SYNC3_OUT	CPTS Time Stamp Generator Bit 3	O	AH17
SYSCLKOUT0	SYSCLK0 output from Main PLL controller (divided by 4) for test and debug purposes only	O	B22

4.3.26.3.2 WKUP Domain

表 4-70. System0 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
MCU_BYP_POR	MCU Bypass reset circuitry input. 0 = Internal POR is used, 1 = External MCU_PORz signal is used.	I	V5
MCU_CLKOUT0	Reference clock output for Ethernet PHYs (50MHz or 25MHz)	O	AB2
MCU_EXT_REFCLK0	External system clock input	I	AB3
MCU_OBSCLK0	Observation clock output for test and debug purposes only	O	AB2
MCU_PORz	MCU Domain cold reset	I	W5
MCU_PORz_OUT	MCU Domain POR status output	O	V2
MCU_RESETSTATz	MCU Domain warm reset status output	O	V3
MCU_RESETz	MCU Domain warm reset	I	W4
MCU_SAFETY_ERRORn	Error signal output from MCU Domain ESM	IO	W3
MCU_SYSCLKOUT0	MCU Domain system clock output (divided by 4) for test and debug purposes only	O	AB3
PMIC_POWER_EN0	Power enable output for MAIN Domain supplies	O	Y5
PMIC_POWER_EN1	Power enable output for MAIN Domain supplies	O	AA5

4.3.26.4 Miscellaneous

4.3.26.4.1 WKUP Domain

表 4-71. Miscellaneous0 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
TEMP_DIODE_P	Temperature Sensor Diode	A	W6

4.3.26.5 EFUSE

4.3.26.5.1 MAIN Domain

表 4-72. EFUSE0 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
VPP_CORE ⁽¹⁾	Programming voltage for MAIN Domain efuses	PWR	F21

(1) This signal is valid only for High-Security devices. For more details, see 5.7, VPP Specification for One-Time Programmable (OTP) eFUSES. For General Purpose devices do not connect any signal, test point, or board trace to this signal.

4.3.26.5.2 MCU Domain

表 4-73. EFUSE0 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
VPP_MCU ⁽¹⁾	Programming voltage for MCU Domain efuses	PWR	T6

(1) This signal is valid only for High-Security devices. For more details, see [5.7, VPP Specification for One-Time Programmable \(OTP\) eFUSEs](#). For General Purpose devices do not connect any signal, test point, or board trace to this signal.

4.3.27 Power Supply

表 4-74. Power Supply Signal Description

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
CAP_VDDAR_CORE0 ⁽¹⁾	External capacitor connection for CORE SRAM LDOs	CAP	P17
CAP_VDDAR_CORE1 ⁽¹⁾	External capacitor connection for CORE SRAM LDOs	CAP	V17
CAP_VDDAR_CORE2 ⁽¹⁾	External capacitor connection for CORE SRAM LDOs	CAP	W16
CAP_VDDAR_CORE3 ⁽¹⁾	External capacitor connection for MSMC SRAM LDOs	CAP	M14
CAP_VDDAR_CORE4 ⁽¹⁾	External capacitor connection for MSMC SRAM LDOs	CAP	L15
CAP_VDDAR_MCU ⁽¹⁾	External capacitor connection for MCU SRAM LDO	CAP	U10
CAP_VDDAR_MPU0_0 ⁽¹⁾	External capacitor connection for MPU SRAM LDOs	CAP	M12
CAP_VDDAR_MPU0_1 ⁽¹⁾	External capacitor connection for MPU SRAM LDOs	CAP	N12
CAP_VDDAR_MPU1_0 ⁽¹⁾	External capacitor connection for MPU SRAM LDOs	CAP	N18
CAP_VDDAR_MPU1_1 ⁽¹⁾	External capacitor connection for MPU SRAM LDOs	CAP	N15
CAP_VDDAR_WKUP ⁽¹⁾	External capacitor connection for WKUP SRAM LDO	CAP	Y10
CAP_VDDA_1P8_IOLDO_WKUP ⁽¹⁾	External capacitor connection for IO Bias LDO in WKUP domain	CAP	AA8
CAP_VDDA_1P8_SDIO ⁽²⁾	External capacitor connection for SDIO LDO	CAP	J17
CAP_VDDA_1P8_IOLDO0 ⁽¹⁾	External capacitor connection for IO Bias LDO	CAP	G19
CAP_VDDA_1P8_IOLDO1 ⁽¹⁾	External capacitor connection for IO Bias LDO	CAP	Y19
CAP_VDDSHV_SDIO ⁽³⁾	External capacitor connection for SDIO LDO	CAP	H18
CAP_VDD_WKUP ⁽¹⁾	External capacitor connection for WKUP LDO	CAP	V9
VDDA_1P8_MON_WKUP	Supply monitor in WKUP domain	A	AB6
VDDA_1P8_SDIO	SDIO LDO analog power supply	PWR	G17
VDDA_1P8_CSI0	CSI PHY analog power supply	PWR	L20, M21
VDDA_1P8_MON0	Supply monitor in MAIN domain	A	AC6
VDDA_1P8_OLDI0	OLDI analog power supply	PWR	L22
VDDA_1P8_SERDES0	SERDES0/1 (USB, PCIE) analog power supply	PWR	AA14, AB13, AB15
VDDA_3P3_IOLDO_WKUP	WKUP IO Bias LDO analog power supply	PWR	AB9
VDDA_3P3_MON_WKUP	Supply monitor in WKUP domain	A	U6
VDDA_3P3_SDIO	SDIO LDO analog power supply	PWR	H17
VDDA_3P3_USB	USB analog power supply	PWR	AC12
VDDA_3P3_IOLDO0	IO Bias LDO analog power supply	PWR	G18
VDDA_3P3_IOLDO1	IO Bias LDO analog power supply	PWR	AA21
VDDA_3P3_MON0	Supply monitor in MAIN domain	A	AC10
VDDA_ADC_MCU	ADC0, ADC1 analog power supply	PWR	M7, M9
VDDA_LDO_WKUP	WKUP LDO analog power supply	PWR	AB8
VDDA_MCU	MCU SRAM LDO, MCU DPLL, CPSW DPLL analog power supply	PWR	U12
VDDA_PLL0_DDR	DDR DPLL analog power supply	PWR	H15
VDDA_PLL1_DDR	DDR De-skew DPLL analog power supply	PWR	H11
VDDA_PLL_CORE	CORE DPLL, PER1 DPLL analog power supply	PWR	Y17
VDDA_PLL_DSS	DSS DPLL analog power supply	PWR	L21
VDDA_PLL_MPU0	MPU0 DPLL analog power supply	PWR	L12
VDDA_PLL_MPU1	MPU1 DPLL analog power supply	PWR	K15
VDDA_PLL_PER0	PER0 DPLL analog power supply	PWR	AB7
VDDA_POR_WKUP ⁽⁵⁾	WKUP POR/POK analog power supply	PWR	Y9

表 4-74. Power Supply Signal Description (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
VDDA_SRAM_CORE0	CORE SRAM LDOs analog power supply	PWR	M19
VDDA_SRAM_CORE1	CORE SRAM LDOs analog power supply	PWR	V16
VDDA_SRAM_MPU0	MPU SRAM LDOs analog power supply	PWR	K7
VDDA_SRAM_MPU1	MPU SRAM LDOs analog power supply	PWR	L18
VDDA_VSYS_MON ⁽⁶⁾	Supply monitor for system	A	AC11
VDDA_WKUP	WKUP High/Low Frequency Oscillator (WKUP_LFOSC0 / WKUP_OSC0), SRAM LDO analog power supply	PWR	AA9
VDDS0	IO bias supply for VDDSHV0	PWR	G12
VDDS0_WKUP	IO bias supply for VDDSHV0_WKUP	PWR	V8
VDDS1	IO bias supply for VDDSHV1	PWR	AA16
VDDS1_WKUP	IO bias supply for VDDSHV1_WKUP	PWR	T9
VDDS2	IO bias supply for VDDSHV2	PWR	P20
VDDS2_WKUP	IO bias supply for VDDSHV2_WKUP	PWR	N8
VDDS3	IO bias supply for VDDSHV3	PWR	T20
VDDS4	IO bias supply for VDDSHV4	PWR	Y20
VDDS5	IO bias supply for VDDSHV5	PWR	AC18
VDDS6	IO bias supply for VDDSHV6	PWR	F20
VDDS7	IO bias supply for VDDSHV7	PWR	K20
VDDS8	IO bias supply for VDDSHV8	PWR	AA10
VDDSHV0	Dual-voltage IO domain power supply	PWR	G15, H16
VDDSHV0_WKUP	Dual-voltage IO domain power supply	PWR	U8, V7, W8, Y7
VDDSHV1	Dual-voltage IO domain power supply	PWR	AA18, AB17
VDDSHV1_WKUP	Dual-voltage IO domain power supply	PWR	R6, R8, T7
VDDSHV2	Dual-voltage IO domain power supply	PWR	N20, N22, P21, R20, R22
VDDSHV2_WKUP	Dual-voltage IO domain power supply	PWR	N6, P7, P9
VDDSHV3	Dual-voltage IO domain power supply	PWR	T21, U20, U22, V21, V23
VDDSHV4	Dual-voltage IO domain power supply	PWR	AA22, W20, W22, Y21, Y23
VDDSHV5	Dual-voltage IO domain power supply	PWR	AA20, AB19, AB21, AB23
VDDSHV6	Dual-voltage IO domain power supply	PWR	G20, H19, H21
VDDSHV7	Dual-voltage IO domain power supply	PWR	J20, J22, K21
VDDSHV8	Dual-voltage IO domain power supply	PWR	AB11
VDDS_DDR	DDR IO domain power supply	PWR	G10, G14, G8, H13, H7, H9
VDDS_OSC1	MAIN High Frequency Oscillator (OSC1) analog power supply	PWR	J16
VDD_CORE	CORE voltage domain supply	PWR	AA12, J10, J12, J14, J19, J8, K13, L14, L19, M13, N14, P13, P15, P19, R14, R16, R18, T13, T15, T17, T19, U14, U16, U18, V13, V15, V19, W14, W18, Y11, Y13, Y15
VDD_DLL_MMC0	MMC0 PHY DLL voltage supply	PWR	G22
VDD_DLL_MMC1	MMC1 PHY DLL voltage supply	PWR	H23
VDD_MCU	MCU voltage domain supply	PWR	N10, P11, R10, R12, T11

表 4-74. Power Supply Signal Description (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
VDD_MPU0	MPU0 voltage domain supply	PWR	K11, K9, L10, L8, M11
VDD_MPU1	MPU1 voltage domain supply	PWR	K16, K18, L17, M16, M18, N17
VDD_WKUP0 ⁽⁴⁾	WKUP voltage domain supply	PWR	V11, W10, W12
VDD_WKUP1 ⁽⁴⁾	WKUP voltage domain supply	PWR	M22
VSS	Ground	GND	A1, A2, A28, AA11, AA13, AA15, AA17, AA19, AA23, AA26, AA7, AB10, AB12, AB14, AB16, AB18, AB20, AB22, AD4, AE10, AE25, AE5, AF15, AF2, AF20, AF8, AG1, AG10, AG28, AG4, AG7, AH1, AH11, AH2, AH27, AH28, AH5, AH8, B12, B15, B20, B6, B9, D22, E26, E28, E4, F14, F19, F22, F25, F27, F3, G11, G13, G16, G2, G21, G23, G7, G9, H1, H10, H12, H14, H20, H22, H24, H26, H28, H6, H8, J11, J13, J15, J18, J21, J23, J25, J27, J7, J9, K1, K10, K12, K14, K17, K19, K22, K23, K6, K8, L11, L13, L16, L23, L24, L26, L28, L3, L7, L9, M10, M15, M17, M20, M8, N11, N13, N16, N19, N21, N7, N9, P10, P12, P14, P16, P18, P22, P6, P8, R11, R13, R15, R17, R19, R21, R7, R9, T10, T12, T14, T16, T18, T22, T26, T8, U11, U13, U15, U17, U19, U21, U3, U7, U9, V10, V12, V14, V18, V20, V22, V6, W11, W13, W15, W17, W19, W21, W23, W7, W9, Y12, Y14, Y16, Y18, Y22, Y6, Y8

- (1) This pin must always be connected via a 1-μF capacitor to VSS.
- (2) The net connecting CAP_VDDA_1P8_SDIO and VDDA_1P8_SDIO to VDDSD6 or VDDSD7 must be connected to a 3.3-μF decoupling capacitor. VDDA_1P8_SDIO, CAP_VDDA_1P8_SDIO, CAP_VDDSHV_SDIO, and VDDA_3P3_SDIO must be connected to VSS, when SDIO_LDO is not used with either MMC0 or MMC1.
- (3) When CAP_VDDSHV_SDIO is connected to VDDSHV6 or VDDSHV7, the entire net which connects these pins should not exceed TBD-μF of decoupling capacitance. When SDIO LDO is not used, this pin should be left unconnected.
- (4) These power rails should be connected together on the board level.
- (5) VDDA_POR_WKUP is preferred to be connected to CAP_VDDA_1P8_IOLDO_WKUP when using internal POR feature.
- (6) The VDDA_VSYS_MON pin provides a way to monitor the system power supply and is not fail-safe, unless implemented with the appropriate resistor voltage divider source. For more information, see [7.5, System Power Supply Monitor Design Guidelines](#).

4.4 Pin Multiplexing

表 4-75 describes the device pin multiplexing associated with pins.

注: Many device pins support multiple signal functions. Some signal functions are selected via a single layer of multiplexers associated with pins. Other signal functions are selected via two or more layers of multiplexers, where one layer is associated with the pins and other layers are associated with peripheral logic functions.

表 4-75, *Pin Multiplexing* only describes signal multiplexing at the pins. For more information, related to signal multiplexing at the pins, see section *Pad Configuration Registers* in the device TRM. Refer to the respective peripheral chapter in the device TRM for information associated with peripheral signal multiplexing.

注: When a pad is set into a pin multiplexing mode which is not defined, that pad's behavior is undefined. This should be avoided.

注: 表 4-75, *Pin Multiplexing* does not include SerDes signal functions. For more information, see section *Serializer/Deserializer (SerDes)* in the device TRM.

注: The PRU_ICSSG contains a second layer of multiplexing to enable additional functionality on the PRU GPO and GPI signals. This internal wrapper multiplexing is described in the PRU_ICSSG chapter in the device TRM.

For more information on the I/O cell configurations, see section *Pad Configuration Registers* in the device TRM.

表 4-75. Pin Multiplexing

ADDRESS	REGISTER NAME	BALL NUMBER	MUXMODE[7:0] SETTINGS								Bootstrap
			0	1	2	3	4	5	6	7	
0x0011C000	SOC_PADCONFIG_0	M27	GPMC0_AD0	VOUT1_DATA0	VIN0_DATA12					GPIO0_0	BOOTMODE00
0x0011C004	SOC_PADCONFIG_1	M23	GPMC0_AD1	VOUT1_DATA1	VIN0_DATA13					GPIO0_1	BOOTMODE01
0x0011C008	SOC_PADCONFIG_2	M28	GPMC0_AD2	VOUT1_DATA2	VIN0_DATA14					GPIO0_2	BOOTMODE02
0x0011C00C	SOC_PADCONFIG_3	M24	GPMC0_AD3	VOUT1_DATA3	VIN0_DATA15					GPIO0_3	BOOTMODE03
0x0011C010	SOC_PADCONFIG_4	N24	GPMC0_AD4	VOUT1_DATA4						GPIO0_4	BOOTMODE04
0x0011C014	SOC_PADCONFIG_5	N27	GPMC0_AD5	VOUT1_DATA5						GPIO0_5	BOOTMODE05
0x0011C018	SOC_PADCONFIG_6	N28	GPMC0_AD6	VOUT1_DATA6						GPIO0_6	BOOTMODE06
0x0011C01C	SOC_PADCONFIG_7	M25	GPMC0_AD7	VOUT1_DATA7						GPIO0_7	BOOTMODE07
0x0011C020	SOC_PADCONFIG_8	N23	GPMC0_AD8	VOUT1_DATA8	VIN0_DATA0	PRG2_PRU0_GPO12	PRG2_PRU0_GPI12	PRG2_PWM2_A0		GPIO0_8	BOOTMODE08
0x0011C024	SOC_PADCONFIG_9	M26	GPMC0_AD9	VOUT1_DATA9	VIN0_DATA1	PRG2_PRU0_GPO13	PRG2_PRU0_GPI13	PRG2_PWM2_B0		GPIO0_9	BOOTMODE09

表 4-75. Pin Multiplexing (continued)

ADDRESS	REGISTER NAME	BALL NUMBER	MUXMODE[7:0] SETTINGS								
			0	1	2	3	4	5	6	7	Bootstrap
0x0011C028	SOC_PADCONFIG_10	P28	GPMC0_AD10	VOUT1_DATA10	VIN0_DATA2	PRG2_PRU0_GPO14	PRG2_PRU0_GPI14		PRG2_PWM0_TZ_IN	GPIO0_10	BOOTMODE10
0x0011C02C	SOC_PADCONFIG_11	P27	GPMC0_AD11	VOUT1_DATA11	VIN0_DATA3	PRG2_PRU0_GPO15	PRG2_PRU0_GPI15	PRG2_PWM2_A1		GPIO0_11	BOOTMODE11
0x0011C030	SOC_PADCONFIG_12	N26	GPMC0_AD12	VOUT1_DATA12	VIN0_DATA4	PRG2_PRU1_GPO12	PRG2_PRU1_GPI12	PRG2_PWM2_B1		GPIO0_12	BOOTMODE12
0x0011C034	SOC_PADCONFIG_13	N25	GPMC0_AD13	VOUT1_DATA13	VIN0_DATA5	PRG2_PRU1_GPO13	PRG2_PRU1_GPI13	PRG2_PWM2_A2		GPIO0_13	BOOTMODE13
0x0011C038	SOC_PADCONFIG_14	P24	GPMC0_AD14	VOUT1_DATA14	VIN0_DATA6	PRG2_PRU1_GPO14	PRG2_PRU1_GPI14		PRG2_PWM0_TZ_OUT	GPIO0_14	BOOTMODE14
0x0011C03C	SOC_PADCONFIG_15	R27	GPMC0_AD15	VOUT1_DATA15	VIN0_DATA7	PRG2_PRU1_GPO15	PRG2_PRU1_GPI15	PRG2_PWM2_B2		GPIO0_15	BOOTMODE15
0x0011C040	SOC_PADCONFIG_16	R28	GPMC0_CLK	VOUT1_DATA16	VIN0_PCLK					GPIO0_16	
0x0011C044	SOC_PADCONFIG_17	P25	GPMC0_ADVn_ALE	VOUT1_DATA17						GPIO0_17	BOOTMODE16
0x0011C048	SOC_PADCONFIG_18	P26	GPMC0_OEn_REn	VOUT1_DATA18						GPIO0_18	BOOTMODE17
0x0011C04C	SOC_PADCONFIG_19	U28	GPMC0_WEn	VOUT1_DATA19						GPIO0_19	BOOTMODE18
0x0011C050	SOC_PADCONFIG_20	T28	GPMC0_BE0n_CLE	VOUT1_DATA20						GPIO0_20	
0x0011C054	SOC_PADCONFIG_21	P23	GPMC0_BE1n	VOUT1_DATA21	VIN0_HD	PRG2_PRU0_GPO17	PRG2_PRU0_GPI17	TIMER_IO2	PRG2_PWM2_TZ_IN	GPIO0_21	
0x0011C058	SOC_PADCONFIG_22	R26	GPMC0_WAIT0	VOUT1_DATA22						GPIO0_22	
0x0011C05C	SOC_PADCONFIG_23	R23	GPMC0_WAIT1	VOUT1_DATA23	VIN0_VD	PRG2_PWM1_A0	PRG2_IEP1_EDC_LATCH_IN0	TIMER_IO3	PRG2_IEP0_EDIO_DATA_IN_OUT28	GPIO0_23	
0x0011C060	SOC_PADCONFIG_24	T25	GPMC0_WPn	VOUT1_VSYNC						GPIO0_24	
0x0011C064	SOC_PADCONFIG_25	T24	GPMC0_DIR	VOUT1_HSYNC	VIN0_DATA8	PRG2_PWM1_B0	PRG2_IEP1_EDC_SYNC_OUT0	TIMER_IO6	PRG2_IEP0_EDIO_DATA_IN_OUT29	GPIO0_25	
0x0011C068	SOC_PADCONFIG_26	R24	GPMC0_CSn0	VOUT1_PCLK						GPIO0_26	
0x0011C06C	SOC_PADCONFIG_27	T23	GPMC0_CSn1	VOUT1_DE	VIN0_DATA9	PRG2_PRU1_GPO17	PRG2_PRU1_GPI17	TIMER_IO7	PRG2_PWM2_TZ_OUT	GPIO0_27	
0x0011C070	SOC_PADCONFIG_28	R25	GPMC0_CSn2	VOUT1_EXTCLKIN	VIN0_DATA10	GPMC0_A27	PRG2_IEP1_EDC_LATCH_IN1	I2C2_SDA	PRG2_IEP0_EDIO_DATA_IN_OUT30	GPIO0_28	
0x0011C074	SOC_PADCONFIG_29	T27	GPMC0_CSn3		VIN0_DATA11	GPMC0_A26	PRG2_IEP1_EDC_SYNC_OUT1	I2C2_SCL	PRG2_IEP0_EDIO_DATA_IN_OUT31	GPIO0_29	
0x0011C078	SOC_PADCONFIG_30	AF18	PRG2_PRU0_GPO0	PRG2_PRU0_GPI0	PRG2_RGMII1_RD0	GPMC0_A25	TRC_CLK	EHRPWM0_SYNCI	PRG2_PWM3_A0	GPIO0_30	
0x0011C07C	SOC_PADCONFIG_31	AE18	PRG2_PRU0_GPO1	PRG2_PRU0_GPI1	PRG2_RGMII1_RD1	GPMC0_A24	TRC_CTL	EHRPWM0_SYNCO	SYNC2_OUT	GPIO0_31	
0x0011C080	SOC_PADCONFIG_32	AH17	PRG2_PRU0_GPO2	PRG2_PRU0_GPI2	PRG2_RGMII1_RD2	GPMC0_A23	TRC_DATA0	EHRPWM_TZn_IN0	SYNC3_OUT	GPIO0_32	
0x0011C084	SOC_PADCONFIG_33	AG18	PRG2_PRU0_GPO3	PRG2_PRU0_GPI3	PRG2_RGMII1_RD3	GPMC0_A22	TRC_DATA1	EHRPWM0_A	PRG2_PWM3_B0	GPIO0_33	
0x0011C088	SOC_PADCONFIG_34	AG17	PRG2_PRU0_GPO4	PRG2_PRU0_GPI4	PRG2_RGMII1_RX_CTL	GPMC0_A21	TRC_DATA2	EHRPWM0_B	PRG2_PWM0_A0	GPIO0_34	
0x0011C08C	SOC_PADCONFIG_35	AF17	PRG2_PRU0_GPO5	PRG2_PRU0_GPI5	PRG2_RGMII1_RXC	GPMC0_A20	TRC_DATA3	EHRPWM1_A	PRG2_PWM3_A1	GPIO0_35	

表 4-75. Pin Multiplexing (continued)

ADDRESS	REGISTER NAME	BALL NUMBER	MUXMODE[7:0] SETTINGS								Bootstrap
			0	1	2	3	4	5	6	7	
0x0011C090	SOC_PADCONFIG_36	AE17	PRG2_PRU0_GPO6	PRG2_PRU0_GPI6	PRG2_RGMII1_TX_CTL	GPMC0_A19	TRC_DATA4	EHRPWM1_B	PRG2_PWM3_B1	GPI00_36	
0x0011C094	SOC_PADCONFIG_37	AC19	PRG2_PRU0_GPO7	PRG2_PRU0_GPI7	PRG2_MDIO0_MDI0	GPMC0_A18	TRC_DATA5	EHRPWM_TZn_IN1	EHRPWM_SOC_A	GPI00_37	
0x0011C098	SOC_PADCONFIG_38	AH16	PRG2_PRU0_GPO8	PRG2_PRU0_GPI8	PRG2_RGMII1_TD0	GPMC0_A17	TRC_DATA6	EHRPWM2_A	PRG2_PWM0_B0	GPI00_38	
0x0011C09C	SOC_PADCONFIG_39	AG16	PRG2_PRU0_GPO9	PRG2_PRU0_GPI9	PRG2_RGMII1_TD1	GPMC0_A16	TRC_DATA7	EHRPWM2_B		GPI00_39	
0x0011C0A0	SOC_PADCONFIG_40	AF16	PRG2_PRU0_GPO10	PRG2_PRU0_GPI10	PRG2_RGMII1_TD2	GPMC0_A15	TRC_DATA8	EHRPWM_TZn_IN2	EHRPWM_SOC_B	GPI00_40	
0x0011C0A4	SOC_PADCONFIG_41	AE16	PRG2_PRU0_GPO11	PRG2_PRU0_GPI11	PRG2_RGMII1_TD3	GPMC0_A14	TRC_DATA9		PRG2_ECAP0_IN_APWM_OUT	GPI00_41	
0x0011C0A8	SOC_PADCONFIG_42	AD16	PRG2_PRU0_GPO16	PRG2_PRU0_GPI16	PRG2_RGMII1_TX_C	GPMC0_A13	TRC_DATA10		PRG2_PWM0_A1	GPI00_42	
0x0011C0AC	SOC_PADCONFIG_43	AH15	PRG2_PRU1_GPO0	PRG2_PRU1_GPI0	PRG2_RGMII2_RD0	GPMC0_A12	TRC_DATA11	EHRPWM3_A	PRG2_PWM3_A2	GPI00_43	
0x0011C0B0	SOC_PADCONFIG_44	AC16	PRG2_PRU1_GPO1	PRG2_PRU1_GPI1	PRG2_RGMII2_RD1	GPMC0_A11	TRC_DATA12	EHRPWM3_B	PRG2_PWM3_B2	GPI00_44	
0x0011C0B4	SOC_PADCONFIG_45	AD17	PRG2_PRU1_GPO2	PRG2_PRU1_GPI2	PRG2_RGMII2_RD2	GPMC0_A10	TRC_DATA13	EHRPWM3_SYNCI	PRG2_PWM0_B1	GPI00_45	
0x0011C0B8	SOC_PADCONFIG_46	AH14	PRG2_PRU1_GPO3	PRG2_PRU1_GPI3	PRG2_RGMII2_RD3	GPMC0_A9	TRC_DATA14	EHRPWM3_SYNC_O		GPI00_46	
0x0011C0BC	SOC_PADCONFIG_47	AG14	PRG2_PRU1_GPO4	PRG2_PRU1_GPI4	PRG2_RGMII2_RX_CTL	GPMC0_A8	TRC_DATA15	EHRPWM_TZn_IN3	PRG2_ECAP0_SYNC_OUT	GPI00_47	
0x0011C0C0	SOC_PADCONFIG_48	AG15	PRG2_PRU1_GPO5	PRG2_PRU1_GPI5	PRG2_RGMII2_RX_C	GPMC0_A7	TRC_DATA16	EHRPWM4_A		GPI00_48	
0x0011C0C4	SOC_PADCONFIG_49	AC17	PRG2_PRU1_GPO6	PRG2_PRU1_GPI6	PRG2_RGMII2_TX_CTL	GPMC0_A6	TRC_DATA17	EHRPWM4_B		GPI00_49	
0x0011C0C8	SOC_PADCONFIG_50	AE15	PRG2_PRU1_GPO7	PRG2_PRU1_GPI7	PRG2_MDIO0_MD_C	GPMC0_A5	TRC_DATA18	EHRPWM_TZn_IN4	PRG2_PWM3_TZ_IN	GPI00_50	
0x0011C0CC	SOC_PADCONFIG_51	AD15	PRG2_PRU1_GPO8	PRG2_PRU1_GPI8	PRG2_RGMII2_TD0	GPMC0_A4	TRC_DATA19	EHRPWM5_A	PRG2_PWM0_A2	GPI00_51	
0x0011C0D0	SOC_PADCONFIG_52	AF14	PRG2_PRU1_GPO9	PRG2_PRU1_GPI9	PRG2_RGMII2_TD1	GPMC0_A3	TRC_DATA20	EHRPWM5_B	PRG2_PWM3_TZ_OUT	GPI00_52	
0x0011C0D4	SOC_PADCONFIG_53	AC15	PRG2_PRU1_GPO10	PRG2_PRU1_GPI10	PRG2_RGMII2_TD2	GPMC0_A2	TRC_DATA21	EHRPWM_TZn_IN5	PRG2_PWM0_B2	GPI00_53	
0x0011C0D8	SOC_PADCONFIG_54	AD14	PRG2_PRU1_GPO11	PRG2_PRU1_GPI11	PRG2_RGMII2_TD3	GPMC0_A1	TRC_DATA22		PRG2_ECAP0_SYNC_IN	GPI00_54	
0x0011C0DC	SOC_PADCONFIG_55	AE14	PRG2_PRU1_GPO16	PRG2_PRU1_GPI16	PRG2_RGMII2_TX_C	GPMC0_A0	TRC_DATA23		PRG2_PWM1_TZ_OUT	GPI00_55	
0x0011C0E0	SOC_PADCONFIG_56	AE22	PRG1_PRU0_GPO0	PRG1_PRU0_GPI0	PRG1_RGMII1_RD0	PRG1_PWM3_A0				GPI00_56	
0x0011C0E4	SOC_PADCONFIG_57	AG24	PRG1_PRU0_GPO1	PRG1_PRU0_GPI1	PRG1_RGMII1_RD1	PRG1_PWM3_B0				GPI00_57	
0x0011C0E8	SOC_PADCONFIG_58	AF23	PRG1_PRU0_GPO2	PRG1_PRU0_GPI2	PRG1_RGMII1_RD2	PRG1_PWM2_A0				GPI00_58	
0x0011C0EC	SOC_PADCONFIG_59	AD21	PRG1_PRU0_GPO3	PRG1_PRU0_GPI3	PRG1_RGMII1_RD3	PRG1_PWM3_A2				GPI00_59	

表 4-75. Pin Multiplexing (continued)

ADDRESS	REGISTER NAME	BALL NUMBER	MUXMODE[7:0] SETTINGS								
			0	1	2	3	4	5	6	7	Bootstrap
0x0011C0F0	SOC_PADCONFIG_60	AG23	PRG1_PRU0_GPO4	PRG1_PRU0_GPI4	PRG1_RGMII1_RX_CTL	PRG1_PWM2_B0				GPIO0_60	
0x0011C0F4	SOC_PADCONFIG_61	AF27	PRG1_PRU0_GPO5	PRG1_PRU0_GPI5		PRG1_PWM3_B2				GPIO0_61	
0x0011C0F8	SOC_PADCONFIG_62	AF22	PRG1_PRU0_GPO6	PRG1_PRU0_GPI6	PRG1_RGMII1_RX_C	PRG1_PWM3_A1				GPIO0_62	
0x0011C0FC	SOC_PADCONFIG_63	AG27	PRG1_PRU0_GPO7	PRG1_PRU0_GPI7	PRG1_IEP0_EDC_LATCH_IN1	PRG1_PWM3_B1				GPIO0_63	
0x0011C100	SOC_PADCONFIG_64	AF28	PRG1_PRU0_GPO8	PRG1_PRU0_GPI8		PRG1_PWM2_A1				GPIO0_64	
0x0011C104	SOC_PADCONFIG_65	AF26	PRG1_PRU0_GPO9	PRG1_PRU0_GPI9	PRG1_UART0_CT_Sn	PRG1_PWM3_TZ_I_N	SPI2_CS1		PRG1_IEP0_EDIO_DATA_IN_OUT28	GPIO0_65	
0x0011C108	SOC_PADCONFIG_66	AH25	PRG1_PRU0_GPO10	PRG1_PRU0_GPI10	PRG1_UART0_RT_Sn	PRG1_PWM2_B1	SPI2_CS2		PRG1_IEP0_EDIO_DATA_IN_OUT29	GPIO0_66	
0x0011C10C	SOC_PADCONFIG_67	AF21	PRG1_PRU0_GPO11	PRG1_PRU0_GPI11	PRG1_RGMII1_TX_CTL	PRG1_PWM3_TZ_OUT				GPIO0_67	
0x0011C110	SOC_PADCONFIG_68	AH20	PRG1_PRU0_GPO12	PRG1_PRU0_GPI12	PRG1_RGMII1_TD0	PRG1_PWM0_A0				GPIO0_68	
0x0011C114	SOC_PADCONFIG_69	AH21	PRG1_PRU0_GPO13	PRG1_PRU0_GPI13	PRG1_RGMII1_TD1	PRG1_PWM0_B0				GPIO0_69	
0x0011C118	SOC_PADCONFIG_70	AG20	PRG1_PRU0_GPO14	PRG1_PRU0_GPI14	PRG1_RGMII1_TD2	PRG1_PWM0_A1				GPIO0_70	
0x0011C11C	SOC_PADCONFIG_71	AD19	PRG1_PRU0_GPO15	PRG1_PRU0_GPI15	PRG1_RGMII1_TD3	PRG1_PWM0_B1				GPIO0_71	
0x0011C120	SOC_PADCONFIG_72	AD20	PRG1_PRU0_GPO16	PRG1_PRU0_GPI16	PRG1_RGMII1_TX_C	PRG1_PWM0_A2				GPIO0_72	
0x0011C124	SOC_PADCONFIG_73	AH26	PRG1_PRU0_GPO17	PRG1_PRU0_GPI17	PRG1_IEP0_EDC_SYNC_OUT1	PRG1_PWM0_B2				GPIO0_73	
0x0011C128	SOC_PADCONFIG_74	AG25	PRG1_PRU0_GPO18	PRG1_PRU0_GPI18	PRG1_IEP0_EDC_LATCH_IN0	PRG1_PWM0_TZ_I_N				GPIO0_74	
0x0011C12C	SOC_PADCONFIG_75	AG26	PRG1_PRU0_GPO19	PRG1_PRU0_GPI19	PRG1_IEP0_EDC_SYNC_OUT0	PRG1_PWM0_TZ_OUT				GPIO0_75	
0x0011C130	SOC_PADCONFIG_76	AH24	PRG1_PRU1_GPO0	PRG1_PRU1_GPI0	PRG1_RGMII2_RD0					GPIO0_76	
0x0011C134	SOC_PADCONFIG_77	AH23	PRG1_PRU1_GPO1	PRG1_PRU1_GPI1	PRG1_RGMII2_RD1					GPIO0_77	
0x0011C138	SOC_PADCONFIG_78	AG21	PRG1_PRU1_GPO2	PRG1_PRU1_GPI2	PRG1_RGMII2_RD2	PRG1_PWM2_A2				GPIO0_78	
0x0011C13C	SOC_PADCONFIG_79	AH22	PRG1_PRU1_GPO3	PRG1_PRU1_GPI3	PRG1_RGMII2_RD3		EQEP1_A			GPIO0_79	
0x0011C140	SOC_PADCONFIG_80	AE21	PRG1_PRU1_GPO4	PRG1_PRU1_GPI4	PRG1_RGMII2_RX_CTL	PRG1_PWM2_B2	EQEP1_B			GPIO0_80	
0x0011C144	SOC_PADCONFIG_81	AC22	PRG1_PRU1_GPO5	PRG1_PRU1_GPI5			EQEP1_S			GPIO0_81	
0x0011C148	SOC_PADCONFIG_82	AG22	PRG1_PRU1_GPO6	PRG1_PRU1_GPI6	PRG1_RGMII2_RX_C					GPIO0_82	
0x0011C14C	SOC_PADCONFIG_83	AD23	PRG1_PRU1_GPO7	PRG1_PRU1_GPI7	PRG1_IEP1_EDC_LATCH_IN1		SPI2_CS0		UART1_TXD	GPIO0_83	

表 4-75. Pin Multiplexing (continued)

ADDRESS	REGISTER NAME	BALL NUMBER	MUXMODE[7:0] SETTINGS								
			0	1	2	3	4	5	6	7	Bootstrap
0x0011C150	SOC_PADCONFIG_84	AE24	PRG1_PRU1_GPO8	PRG1_PRU1_GPI8		PRG1_PWM2_TZ_OUT				GPIO0_84	
0x0011C154	SOC_PADCONFIG_85	AF25	PRG1_PRU1_GPO9	PRG1_PRU1_GPI9	PRG1_UART0_RXD				PRG1_IEP0_EDIO_DATA_IN_OUT30	GPIO0_85	
0x0011C158	SOC_PADCONFIG_86	AF24	PRG1_PRU1_GPO10	PRG1_PRU1_GPI10	PRG1_UART0_TXD	PRG1_PWM2_TZ_IN	SPI2_CS3		PRG1_IEP0_EDIO_DATA_IN_OUT31	GPIO0_86	
0x0011C15C	SOC_PADCONFIG_87	AC20	PRG1_PRU1_GPO11	PRG1_PRU1_GPI11	PRG1_RGMII2_TX_CTL		EQEP1_I			GPIO0_87	
0x0011C160	SOC_PADCONFIG_88	AE20	PRG1_PRU1_GPO12	PRG1_PRU1_GPI12	PRG1_RGMII2_TD0	PRG1_PWM1_A0				GPIO0_88	
0x0011C164	SOC_PADCONFIG_89	AF19	PRG1_PRU1_GPO13	PRG1_PRU1_GPI13	PRG1_RGMII2_TD1	PRG1_PWM1_B0				GPIO0_89	
0x0011C168	SOC_PADCONFIG_90	AH19	PRG1_PRU1_GPO14	PRG1_PRU1_GPI14	PRG1_RGMII2_TD2	PRG1_PWM1_A1				GPIO0_90	
0x0011C16C	SOC_PADCONFIG_91	AG19	PRG1_PRU1_GPO15	PRG1_PRU1_GPI15	PRG1_RGMII2_TD3	PRG1_PWM1_B1				GPIO0_91	
0x0011C170	SOC_PADCONFIG_92	AE19	PRG1_PRU1_GPO16	PRG1_PRU1_GPI16	PRG1_RGMII2_TXC	PRG1_PWM1_A2				GPIO0_92	
0x0011C174	SOC_PADCONFIG_93	AE23	PRG1_PRU1_GPO17	PRG1_PRU1_GPI17	PRG1_IEP1_EDC_SYNC_OUT1	PRG1_PWM1_B2	SPI2_CLK	PRG1_ECAP0_SYNC_OUT	UART1_RXD	GPIO0_93	
0x0011C178	SOC_PADCONFIG_94	AD22	PRG1_PRU1_GPO18	PRG1_PRU1_GPI18	PRG1_IEP1_EDC_LATCH_IN0	PRG1_PWM1_TZ_IN	SPI2_D0	PRG1_ECAP0_SYNC_IN	UART1_CTSn	GPIO0_94	
0x0011C17C	SOC_PADCONFIG_95	AC21	PRG1_PRU1_GPO19	PRG1_PRU1_GPI19	PRG1_IEP1_EDC_SYNC_OUT0	PRG1_PWM1_TZ_OUT	SPI2_D1	PRG1_ECAP0_IN_APWM_OUT	UART1_RTSn	GPIO0_95	
0x0011C180	SOC_PADCONFIG_96	AD18	PRG1_MDIO0_MDI0	SPI1_CS2		PRG2_PWM1_A1				GPIO1_0	
0x0011C184	SOC_PADCONFIG_97	AH18	PRG1_MDIO0_MD0C	SPI1_CS3		PRG2_PWM1_B1				GPIO1_1	
0x0011C188	SOC_PADCONFIG_98	D25	MMC0_DAT7	UART0_DCDn				EQEP2_A		GPIO1_2	
0x0011C18C	SOC_PADCONFIG_99	B26	MMC0_DAT6	UART0_DSRn				EQEP2_B		GPIO1_3	
0x0011C190	SOC_PADCONFIG_100	A24	MMC0_DAT5	UART0_DTRn				EQEP2_I		GPIO1_4	
0x0011C194	SOC_PADCONFIG_101	E24	MMC0_DAT4	UART0_RIN				EQEP2_S		GPIO1_5	
0x0011C198	SOC_PADCONFIG_102	A25	MMC0_DAT3							GPIO1_6	
0x0011C19C	SOC_PADCONFIG_103	C26	MMC0_DAT2							GPIO1_7	
0x0011C1A0	SOC_PADCONFIG_104	E25	MMC0_DAT1							GPIO1_8	
0x0011C1A4	SOC_PADCONFIG_105	A26	MMC0_DAT0							GPIO1_9	
0x0011C1A8	SOC_PADCONFIG_106	B25	MMC0_CLK							GPIO1_10	
0x0011C1AC	SOC_PADCONFIG_107	B27	MMC0_CMD							GPIO1_11	
0x0011C1B0	SOC_PADCONFIG_108	C25	MMC0_DS							GPIO1_12	
0x0011C1B4	SOC_PADCONFIG_109	A23	MMC0_SDCD						PRG2_IEP0_EDIO_OUTVALID	GPIO1_13	
0x0011C1B8	SOC_PADCONFIG_110	B23	MMC0_SDWP							GPIO1_14	
0x0011C1BC	SOC_PADCONFIG_111	AG13	SPI0_CS0							GPIO1_15	
0x0011C1C0	SOC_PADCONFIG_112	AF13	SPI0_CS1	CPTS0_TS_COMP	I2C3_SCL				PRG1_IEP0_EDIO_OUTVALID	GPIO1_16	

表 4-75. Pin Multiplexing (continued)

ADDRESS	REGISTER NAME	BALL NUMBER	MUXMODE[7:0] SETTINGS								Bootstrap
			0	1	2	3	4	5	6	7	
0x0011C1C4	SOC_PADCONFIG_113	AH13	SPI0_CLK							GPIO1_17	
0x0011C1C8	SOC_PADCONFIG_114	AE13	SPI0_D0							GPIO1_18	
0x0011C1CC	SOC_PADCONFIG_115	AD13	SPI0_D1							GPIO1_19	
0x0011C1D0	SOC_PADCONFIG_116	AD12	SPI1_CS0			PRG2_IEP0_EDC_LATCH_IN0	PRG2_UART0_CT Sn		PRG0_IEP0_EDIO_OUTVALID	GPIO1_20	
0x0011C1D4	SOC_PADCONFIG_117	AG12	SPI1_CS1	CPTS0_TS_SYNC	I2C3_SDA					GPIO1_21	
0x0011C1D8	SOC_PADCONFIG_118	AH12	SPI1_CLK			PRG2_IEP0_EDC_SYNC_OUT0	PRG2_UART0_RT Sn			GPIO1_22	
0x0011C1DC	SOC_PADCONFIG_119	AE12	SPI1_D0			PRG2_IEP0_EDC_LATCH_IN1	PRG2_UART0_RX D			GPIO1_23	
0x0011C1E0	SOC_PADCONFIG_120	AF12	SPI1_D1			PRG2_IEP0_EDC_SYNC_OUT1	PRG2_UART0_TX D			GPIO1_24	
0x0011C1E4	SOC_PADCONFIG_121	AF11	UART0_RXD							GPIO1_25	
0x0011C1E8	SOC_PADCONFIG_122	AE11	UART0_TXD							GPIO1_26	
0x0011C1EC	SOC_PADCONFIG_123	AG11	UART0_CTSn	TIMER_IO4	SPI0_CS2					GPIO1_27	
0x0011C1F0	SOC_PADCONFIG_124	AD11	UART0_RTSn	TIMER_IO5	SPI0_CS3					GPIO1_28	
0x0011C1F4	SOC_PADCONFIG_125	V24	PRG0_PRU0_GPO 0	PRG0_PRU0_GPI0	PRG0_RGMII1_RD 0	PRG0_PWM3_A0		MCASP0_ACLKX		GPIO1_29	
0x0011C1F8	SOC_PADCONFIG_126	W25	PRG0_PRU0_GPO 1	PRG0_PRU0_GPI1	PRG0_RGMII1_RD 1	PRG0_PWM3_B0		MCASP0_AFSX		GPIO1_30	
0x0011C1FC	SOC_PADCONFIG_127	W24	PRG0_PRU0_GPO 2	PRG0_PRU0_GPI2	PRG0_RGMII1_RD 2	PRG0_PWM2_A0		MCASP0_ACLKR		GPIO1_31	
0x0011C200	SOC_PADCONFIG_128	AA27	PRG0_PRU0_GPO 3	PRG0_PRU0_GPI3	PRG0_RGMII1_RD 3	PRG0_PWM3_A2		MCASP0_AFSR		GPIO1_32	
0x0011C204	SOC_PADCONFIG_129	Y24	PRG0_PRU0_GPO 4	PRG0_PRU0_GPI4	PRG0_RGMII1_RX_CTL	PRG0_PWM2_B0		MCASP0_AXR0		GPIO1_33	
0x0011C208	SOC_PADCONFIG_130	V28	PRG0_PRU0_GPO 5	PRG0_PRU0_GPI5		PRG0_PWM3_B2		MCASP0_AXR1		GPIO1_34	
0x0011C20C	SOC_PADCONFIG_131	Y25	PRG0_PRU0_GPO 6	PRG0_PRU0_GPI6	PRG0_RGMII1_RX C	PRG0_PWM3_A1		MCASP0_AXR2		GPIO1_35	
0x0011C210	SOC_PADCONFIG_132	U27	PRG0_PRU0_GPO 7	PRG0_PRU0_GPI7	PRG0_IEP0_EDC_LATCH_IN1	PRG0_PWM3_B1	PRG0_ECAP0_SY NC_IN	MCASP0_AXR3		GPIO1_36	
0x0011C214	SOC_PADCONFIG_133	V27	PRG0_PRU0_GPO 8	PRG0_PRU0_GPI8		PRG0_PWM2_A1		MCASP0_AXR4		GPIO1_37	
0x0011C218	SOC_PADCONFIG_134	V26	PRG0_PRU0_GPO 9	PRG0_PRU0_GPI9	PRG0_UART0_CT Sn	PRG0_PWM3_TZ_I N	SPI3_CS1	MCASP0_AXR5	PRG0_IEP0_EDIO_DATA_IN_OUT28	GPIO1_38	
0x0011C21C	SOC_PADCONFIG_135	U25	PRG0_PRU0_GPO 10	PRG0_PRU0_GPI10	PRG0_UART0_RT Sn	PRG0_PWM2_B1	SPI3_CS2	MCASP0_AXR6	PRG0_IEP0_EDIO_DATA_IN_OUT29	GPIO1_39	
0x0011C220	SOC_PADCONFIG_136	AB25	PRG0_PRU0_GPO 11	PRG0_PRU0_GPI11	PRG0_RGMII1_TX_CTL	PRG0_PWM3_TZ_OUT		MCASP0_AXR7		GPIO1_40	
0x0011C224	SOC_PADCONFIG_137	AD27	PRG0_PRU0_GPO 12	PRG0_PRU0_GPI12	PRG0_RGMII1_TD 0	PRG0_PWM0_A0		MCASP0_AXR8		GPIO1_41	
0x0011C228	SOC_PADCONFIG_138	AC26	PRG0_PRU0_GPO 13	PRG0_PRU0_GPI13	PRG0_RGMII1_TD 1	PRG0_PWM0_B0		MCASP0_AXR9		GPIO1_42	
0x0011C22C	SOC_PADCONFIG_139	AD26	PRG0_PRU0_GPO 14	PRG0_PRU0_GPI14	PRG0_RGMII1_TD 2	PRG0_PWM0_A1		MCASP0_AXR10		GPIO1_43	

表 4-75. Pin Multiplexing (continued)

ADDRESS	REGISTER NAME	BALL NUMBER	MUXMODE[7:0] SETTINGS								
			0	1	2	3	4	5	6	7	Bootstrap
0x0011C230	SOC_PADCONFIG_140	AA24	PRG0_PRU0_GPO15	PRG0_PRU0_GPI15	PRG0_RGMII1_TD3	PRG0_PWM0_B1		MCASP0_AXR11		GPIO1_44	
0x0011C234	SOC_PADCONFIG_141	AD28	PRG0_PRU0_GPO16	PRG0_PRU0_GPI16	PRG0_RGMII1_TXC	PRG0_PWM0_A2		MCASP0_AXR12	MCASP1_AHCLKR	GPIO1_45	
0x0011C238	SOC_PADCONFIG_142	U26	PRG0_PRU0_GPO17	PRG0_PRU0_GPI17	PRG0_IEP0_EDC_SYNC_OUT1	PRG0_PWM0_B2	PRG0_ECAP0_SYNC_OUT	MCASP0_AXR13	MCASP1_AHCLKX	GPIO1_46	
0x0011C23C	SOC_PADCONFIG_143	V25	PRG0_PRU0_GPO18	PRG0_PRU0_GPI18	PRG0_IEP0_EDC_LATCH_IN0	PRG0_PWM0_TZ_IN	PRG0_ECAP0_IN_APWM_OUT	MCASP0_AXR14	MCASP2_AHCLKR	GPIO1_47	
0x0011C240	SOC_PADCONFIG_144	U24	PRG0_PRU0_GPO19	PRG0_PRU0_GPI19	PRG0_IEP0_EDC_SYNC_OUT0	PRG0_PWM0_TZ_OUT		MCASP0_AXR15	MCASP2_AHCLKX	GPIO1_48	
0x0011C244	SOC_PADCONFIG_145	AB28	PRG0_PRU1_GPO0	PRG0_PRU1_GPI0	PRG0_RGMII2_RD0			MCASP1_ACLKX		GPIO1_49	
0x0011C248	SOC_PADCONFIG_146	AC28	PRG0_PRU1_GPO1	PRG0_PRU1_GPI1	PRG0_RGMII2_RD1			MCASP1_AFSX		GPIO1_50	
0x0011C24C	SOC_PADCONFIG_147	AC27	PRG0_PRU1_GPO2	PRG0_PRU1_GPI2	PRG0_RGMII2_RD2	PRG0_PWM2_A2		MCASP1_ACLKR		GPIO1_51	
0x0011C250	SOC_PADCONFIG_148	AB26	PRG0_PRU1_GPO3	PRG0_PRU1_GPI3	PRG0_RGMII2_RD3		EQEP0_A	MCASP1_AFSR		GPIO1_52	
0x0011C254	SOC_PADCONFIG_149	AA25	PRG0_PRU1_GPO4	PRG0_PRU1_GPI4	PRG0_RGMII2_RX_CTL	PRG0_PWM2_B2	EQEP0_B	MCASP1_AXR0	MCASP0_AHCLKR	GPIO1_53	
0x0011C258	SOC_PADCONFIG_150	U23	PRG0_PRU1_GPO5	PRG0_PRU1_GPI5			EQEP0_S	MCASP1_AXR1	MCASP0_AHCLKX	GPIO1_54	
0x0011C25C	SOC_PADCONFIG_151	AB27	PRG0_PRU1_GPO6	PRG0_PRU1_GPI6	PRG0_RGMII2_RXC			MCASP1_AXR2		GPIO1_55	
0x0011C260	SOC_PADCONFIG_152	W28	PRG0_PRU1_GPO7	PRG0_PRU1_GPI7	PRG0_IEP1_EDC_LATCH_IN1		SPI3_CS0	MCASP1_AXR3	UART2_TXD	GPIO1_56	
0x0011C264	SOC_PADCONFIG_153	W27	PRG0_PRU1_GPO8	PRG0_PRU1_GPI8		PRG0_PWM2_TZ_OUT		MCASP1_AXR4		GPIO1_57	
0x0011C268	SOC_PADCONFIG_154	Y28	PRG0_PRU1_GPO9	PRG0_PRU1_GPI9	PRG0_UART0_RXD		SPI3_CS3	MCASP1_AXR5	PRG0_IEP0_EDIO_DATA_IN_OUT30	GPIO1_58	
0x0011C26C	SOC_PADCONFIG_155	AA28	PRG0_PRU1_GPO10	PRG0_PRU1_GPI10	PRG0_UART0_TXD	PRG0_PWM2_TZ_IN	EQEP0_I	MCASP1_AXR6	PRG0_IEP0_EDIO_DATA_IN_OUT31	GPIO1_59	
0x0011C270	SOC_PADCONFIG_156	AB24	PRG0_PRU1_GPO11	PRG0_PRU1_GPI11	PRG0_RGMII2_TX_CTL			MCASP1_AXR7		GPIO1_60	
0x0011C274	SOC_PADCONFIG_157	AC25	PRG0_PRU1_GPO12	PRG0_PRU1_GPI12	PRG0_RGMII2_TD0	PRG0_PWM1_A0		MCASP1_AXR8		GPIO1_61	
0x0011C278	SOC_PADCONFIG_158	AD25	PRG0_PRU1_GPO13	PRG0_PRU1_GPI13	PRG0_RGMII2_TD1	PRG0_PWM1_B0		MCASP1_AXR9		GPIO1_62	
0x0011C27C	SOC_PADCONFIG_159	AD24	PRG0_PRU1_GPO14	PRG0_PRU1_GPI14	PRG0_RGMII2_TD2	PRG0_PWM1_A1		MCASP2_AFSR		GPIO1_63	
0x0011C280	SOC_PADCONFIG_160	AE27	PRG0_PRU1_GPO15	PRG0_PRU1_GPI15	PRG0_RGMII2_TD3	PRG0_PWM1_B1		MCASP2_ACLKR		GPIO1_64	
0x0011C284	SOC_PADCONFIG_161	AC24	PRG0_PRU1_GPO16	PRG0_PRU1_GPI16	PRG0_RGMII2_TXC	PRG0_PWM1_A2		MCASP2_AXR0		GPIO1_65	
0x0011C288	SOC_PADCONFIG_162	Y27	PRG0_PRU1_GPO17	PRG0_PRU1_GPI17	PRG0_IEP1_EDC_SYNC_OUT1	PRG0_PWM1_B2	SPI3_CLK	MCASP2_AXR1	UART2_RXD	GPIO1_66	
0x0011C28C	SOC_PADCONFIG_163	Y26	PRG0_PRU1_GPO18	PRG0_PRU1_GPI18	PRG0_IEP1_EDC_LATCH_IN0	PRG0_PWM1_TZ_IN	SPI3_D0	MCASP2_AFSX	UART2_CTSn	GPIO1_67	

表 4-75. Pin Multiplexing (continued)

ADDRESS	REGISTER NAME	BALL NUMBER	MUXMODE[7:0] SETTINGS								Bootstrap
			0	1	2	3	4	5	6	7	
0x0011C290	SOC_PADCONFIG_164	W26	PRG0_PRU1_GPO19	PRG0_PRU1_GPI19	PRG0_IEP1_EDC_SYNC_OUT0	PRG0_PWM1_TZ_OUT	SPI3_D1	MCASP2_ACLKX	UART2_RTSn	GPIO1_68	
0x0011C294	SOC_PADCONFIG_165	AE26	PRG0_MDIO0_MDI0			PRG2_PWM1_A2		MCASP2_AXR2		GPIO1_69	
0x0011C298	SOC_PADCONFIG_166	AE28	PRG0_MDIO0_MD0C			PRG2_PWM1_B2		MCASP2_AXR3		GPIO1_70	
0x0011C29C	SOC_PADCONFIG_167	F18	NMIIn						PRG2_PWM1_TZ_IN		
0x0011C2A0	SOC_PADCONFIG_168	F17	RESETz								
0x0011C2A4	SOC_PADCONFIG_169	D19	RESETSTATz								
0x0011C2A8	SOC_PADCONFIG_170	C19	PORz_OUT								
0x0011C2AC	SOC_PADCONFIG_171	E20	SOC_SAFETY_ERORn								
0x0011C2B0	SOC_PADCONFIG_172	C20	TDI								
0x0011C2B4	SOC_PADCONFIG_173	A20	TDO								
0x0011C2B8	SOC_PADCONFIG_174	A21	TMS								
0x0011C2BC	SOC_PADCONFIG_175	AD9	USB0_DRVVBUS							GPIO1_71	
0x0011C2C0	SOC_PADCONFIG_176	AC8	USB1_DRVVBUS							GPIO1_72	
0x0011C2C4	SOC_PADCONFIG_177	D27	MMC1_DAT3							GPIO1_73	
0x0011C2C8	SOC_PADCONFIG_178	D26	MMC1_DAT2							GPIO1_74	
0x0011C2CC	SOC_PADCONFIG_179	E27	MMC1_DAT1							GPIO1_75	
0x0011C2D0	SOC_PADCONFIG_180	D28	MMC1_DAT0							GPIO1_76	
0x0011C2D4	SOC_PADCONFIG_181	C27	MMC1_CLK							GPIO1_77	
0x0011C2D8	SOC_PADCONFIG_182	C28	MMC1_CMD							GPIO1_78	
0x0011C2DC	SOC_PADCONFIG_183	B24	MMC1_SDCD							GPIO1_79	
0x0011C2E0	SOC_PADCONFIG_184	C24	MMC1_SDWP							GPIO1_80	
0x0011C2E8	SOC_PADCONFIG_186	D20	I2C0_SCL								
0x0011C2EC	SOC_PADCONFIG_187	C21	I2C0_SDA								
0x0011C2F0	SOC_PADCONFIG_188	B21	I2C1_SCL	CPTS0_HW1TSPUSH							
0x0011C2F4	SOC_PADCONFIG_189	E21	I2C1_SDA	CPTS0_HW2TSPUSH							
0x0011C2F8	SOC_PADCONFIG_190	D21	ECAP0_IN_APWM_OUT	SYNC0_OUT	CPTS0_RFT_CLK					GPIO1_86	
0x0011C2FC	SOC_PADCONFIG_191	A22	EXT_REFCLK1	SYNC1_OUT						GPIO1_87	
0x0011C300	SOC_PADCONFIG_192	B22	TIMER_IO0		SYSCLKOUT0					GPIO1_88	
0x0011C304	SOC_PADCONFIG_193	C23	TIMER_IO1		OBSClk0					GPIO1_89	
0x0011C308	SOC_PADCONFIG_194	E19	PORz								
0x4301C000	WKUP_PADCONFIG_0	V1	MCU_OSPIO_CLK	MCU_HYPERBUS0_CK						WKUP_GPIO0_12	
0x4301C004	WKUP_PADCONFIG_1	U1	MCU_OSPIO_LBCLKO	MCU_HYPERBUS0_CKn						WKUP_GPIO0_13	

表 4-75. Pin Multiplexing (continued)

ADDRESS	REGISTER NAME	BALL NUMBER	MUXMODE[7:0] SETTINGS								Bootstrap
			0	1	2	3	4	5	6	7	
0x4301C008	WKUP_PADCONFIG_2	U2	MCU_OSPI0_DQS	MCU_HYPERBUS0_RWDS						WKUP_GPIO0_14	
0x4301C00C	WKUP_PADCONFIG_3	U4	MCU_OSPI0_D0	MCU_HYPERBUS0_DQ0						WKUP_GPIO0_15	
0x4301C010	WKUP_PADCONFIG_4	U5	MCU_OSPI0_D1	MCU_HYPERBUS0_DQ1						WKUP_GPIO0_16	
0x4301C014	WKUP_PADCONFIG_5	T2	MCU_OSPI0_D2	MCU_HYPERBUS0_DQ2						WKUP_GPIO0_17	
0x4301C018	WKUP_PADCONFIG_6	T3	MCU_OSPI0_D3	MCU_HYPERBUS0_DQ3						WKUP_GPIO0_18	
0x4301C01C	WKUP_PADCONFIG_7	T4	MCU_OSPI0_D4	MCU_HYPERBUS0_DQ4						WKUP_GPIO0_19	
0x4301C020	WKUP_PADCONFIG_8	T5	MCU_OSPI0_D5	MCU_HYPERBUS0_DQ5						WKUP_GPIO0_20	
0x4301C024	WKUP_PADCONFIG_9	R2	MCU_OSPI0_D6	MCU_HYPERBUS0_DQ6						WKUP_GPIO0_21	
0x4301C028	WKUP_PADCONFIG_10	R3	MCU_OSPI0_D7	MCU_HYPERBUS0_DQ7						WKUP_GPIO0_22	
0x4301C02C	WKUP_PADCONFIG_11	R4	MCU_OSPI0_CSn0	MCU_HYPERBUS0_CSn0						WKUP_GPIO0_23	
0x4301C030	WKUP_PADCONFIG_12	R5	MCU_OSPI0_CSn1	MCU_HYPERBUS0_RESETh						WKUP_GPIO0_24	
0x4301C034	WKUP_PADCONFIG_13	T1	MCU_OSPI1_CLK							WKUP_GPIO0_25	
0x4301C038	WKUP_PADCONFIG_14	R1	MCU_OSPI1_LBCL_KO	MCU_OSPI0_CSn2	MCU_HYPERBUS0_RESETh					WKUP_GPIO0_26	
0x4301C03C	WKUP_PADCONFIG_15	P2	MCU_OSPI1_DQS	MCU_OSPI0_CSn3	MCU_HYPERBUS0_INTn					WKUP_GPIO0_27	
0x4301C040	WKUP_PADCONFIG_16	P3	MCU_OSPI1_D0							WKUP_GPIO0_28	
0x4301C044	WKUP_PADCONFIG_17	P4	MCU_OSPI1_D1				MCU_UART0_RXD	MCU_SPI1_CS1		WKUP_GPIO0_29	
0x4301C048	WKUP_PADCONFIG_18	P5	MCU_OSPI1_D2				MCU_UART0_TXD	MCU_SPI1_CS2		WKUP_GPIO0_30	
0x4301C04C	WKUP_PADCONFIG_19	P1	MCU_OSPI1_D3				MCU_UART0_CTSn	MCU_SPI0_CS1		WKUP_GPIO0_31	
0x4301C050	WKUP_PADCONFIG_20	N2	MCU_OSPI1_CSn0							WKUP_GPIO0_32	
0x4301C054	WKUP_PADCONFIG_21	N3	MCU_OSPI1_CSn1	MCU_HYPERBUS0_WPn	MCU_TIMER_IO0	MCU_HYPERBUS0_CSn1	MCU_UART0_RTSn	MCU_SPI0_CS2		WKUP_GPIO0_33	
0x4301C058	WKUP_PADCONFIG_22	N4	MCU_RGMII1_TX_CTL	MCU_RMII1_CRS_DV						WKUP_GPIO0_34	
0x4301C05C	WKUP_PADCONFIG_23	N5	MCU_RGMII1_RX_CTL	MCU_RMII1_RX_ER						WKUP_GPIO0_35	
0x4301C060	WKUP_PADCONFIG_24	M2	MCU_RGMII1_TD3							WKUP_GPIO0_36	
0x4301C064	WKUP_PADCONFIG_25	M3	MCU_RGMII1_TD2							WKUP_GPIO0_37	
0x4301C068	WKUP_PADCONFIG_26	M4	MCU_RGMII1_TD1	MCU_RMII1_TXD1						WKUP_GPIO0_38	
0x4301C06C	WKUP_PADCONFIG_27	M5	MCU_RGMII1_TD0	MCU_RMII1_TXD0						WKUP_GPIO0_39	
0x4301C070	WKUP_PADCONFIG_28	N1	MCU_RGMII1_TXC_N	MCU_RMII1_TX_EN						WKUP_GPIO0_40	

表 4-75. Pin Multiplexing (continued)

ADDRESS	REGISTER NAME	BALL NUMBER	MUXMODE[7:0] SETTINGS								Bootstrap
			0	1	2	3	4	5	6	7	
0x4301C074	WKUP_PADCONFIG_29	M1	MCU_RGMII1_RXC	MCU_RMII1_REF_CLK						WKUP_GPIO0_41	
0x4301C078	WKUP_PADCONFIG_30	L2	MCU_RGMII1_RD3							WKUP_GPIO0_42	
0x4301C07C	WKUP_PADCONFIG_31	L5	MCU_RGMII1_RD2							WKUP_GPIO0_43	
0x4301C080	WKUP_PADCONFIG_32	M6	MCU_RGMII1_RD1	MCU_RMII1_RXD1						WKUP_GPIO0_44	
0x4301C084	WKUP_PADCONFIG_33	L6	MCU_RGMII1_RD0	MCU_RMII1_RXD0						WKUP_GPIO0_45	
0x4301C088	WKUP_PADCONFIG_34	L4	MCU_MDIO0_MDI_O							WKUP_GPIO0_46	
0x4301C08C	WKUP_PADCONFIG_35	L1	MCU_MDIO0_MDC							WKUP_GPIO0_47	
0x4301C090	WKUP_PADCONFIG_36	Y1	MCU_SPI0_CLK							WKUP_GPIO0_48	MCU_BOOTMODE 06
0x4301C094	WKUP_PADCONFIG_37	Y3	MCU_SPI0_D0							WKUP_GPIO0_49	MCU_BOOTMODE 07
0x4301C098	WKUP_PADCONFIG_38	Y2	MCU_SPI0_D1							WKUP_GPIO0_50	MCU_BOOTMODE 05
0x4301C09C	WKUP_PADCONFIG_39	Y4	MCU_SPI0_CS0							WKUP_GPIO0_51	
0x4301C0A0	WKUP_PADCONFIG_40	AB1	WKUP_UART0_RXD							WKUP_GPIO0_52	
0x4301C0A4	WKUP_PADCONFIG_41	AB5	WKUP_UART0_TXD							WKUP_GPIO0_53	
0x4301C0A8	WKUP_PADCONFIG_42	W1	MCU_MCAN0_TX							WKUP_GPIO0_54	
0x4301C0AC	WKUP_PADCONFIG_43	W2	MCU_MCAN0_RX							WKUP_GPIO0_55	
0x4301C0B0	WKUP_PADCONFIG_44	AF4	WKUP_GPIO0_0	MCU_SPI1_CLK						WKUP_GPIO0_0	MCU_BOOTMODE 00
0x4301C0B4	WKUP_PADCONFIG_45	AF3	WKUP_GPIO0_1	MCU_SPI1_D0						WKUP_GPIO0_1	MCU_BOOTMODE 01
0x4301C0B8	WKUP_PADCONFIG_46	AE3	WKUP_GPIO0_2	MCU_SPI1_D1						WKUP_GPIO0_2	MCU_BOOTMODE 02
0x4301C0BC	WKUP_PADCONFIG_47	AD1	WKUP_GPIO0_3	MCU_SPI1_CS0						WKUP_GPIO0_3	MCU_BOOTMODE 03
0x4301C0C0	WKUP_PADCONFIG_48	AC3	WKUP_GPIO0_4	MCU_MCAN1_TX	MCU_SPI0_CS3	MCU_ADC_EXT_T_RIGGER0				WKUP_GPIO0_4	MCU_BOOTMODE 04
0x4301C0C4	WKUP_PADCONFIG_49	AD3	WKUP_GPIO0_5	MCU_MCAN1_RX	MCU_SPI1_CS3	MCU_ADC_EXT_T_RIGGER1				WKUP_GPIO0_5	
0x4301C0C8	WKUP_PADCONFIG_50	AC2	WKUP_GPIO0_6	WKUP_UART0_CTSn	MCU_CPTS0_HW1_TSPUSH					WKUP_GPIO0_6	
0x4301C0CC	WKUP_PADCONFIG_51	AC1	WKUP_GPIO0_7	WKUP_UART0_RTSn	MCU_CPTS0_HW2_TSPUSH					WKUP_GPIO0_7	
0x4301C0D0	WKUP_PADCONFIG_52	AC5	WKUP_GPIO0_8		MCU_CPTS0_TS_SYNC					WKUP_GPIO0_8	MCU_BOOTMODE 08
0x4301C0D4	WKUP_PADCONFIG_53	AB4	WKUP_GPIO0_9		MCU_CPTS0_TS_COMP					WKUP_GPIO0_9	MCU_BOOTMODE 09
0x4301C0D8	WKUP_PADCONFIG_54	AB3	WKUP_GPIO0_10	MCU_EXT_REFCLK0			MCU_CPTS0_RFT_CLK	MCU_SYSCLKOUT0		WKUP_GPIO0_10	
0x4301C0DC	WKUP_PADCONFIG_55	AB2	WKUP_GPIO0_11	MCU_OBCLK0			MCU_TIMER_IO1		MCU_CLKOUT0	WKUP_GPIO0_11	

表 4-75. Pin Multiplexing (continued)

ADDRESS	REGISTER NAME	BALL NUMBER	MUXMODE[7:0] SETTINGS								Bootstrap
			0	1	2	3	4	5	6	7	
0x4301C0E0	WKUP_PADCONFIG_56	AC7	WKUP_I2C0_SCL								
0x4301C0E4	WKUP_PADCONFIG_57	AD6	WKUP_I2C0_SDA								
0x4301C0E8	WKUP_PADCONFIG_58	AD8	MCU_I2C0_SCL								
0x4301C0EC	WKUP_PADCONFIG_59	AD7	MCU_I2C0_SDA								
0x4301C0F0	WKUP_PADCONFIG_60	AA5	PMIC_POWER_EN 1								
0x4301C0F4	WKUP_PADCONFIG_61	W3	MCU_SAFETY_ER RORn								
0x4301C0F8	WKUP_PADCONFIG_62	W4	MCU_RESETz								
0x4301C0FC	WKUP_PADCONFIG_63	V3	MCU_RESETSTAT z								
0x4301C100	WKUP_PADCONFIG_64	V2	MCU_PORz_OUT								
0x4301C104	WKUP_PADCONFIG_65	AA4	TCK								
0x4301C108	WKUP_PADCONFIG_66	AA3	TRSTn								
0x4301C10C	WKUP_PADCONFIG_67	AA2	EMU0								
0x4301C110	WKUP_PADCONFIG_68	AA1	EMU1								
0x4301C114	WKUP_PADCONFIG_69	Y5	PMIC_POWER_EN 0								

4.5 Connections for Unused Pins

This section describes the Unused/Reserved balls connection requirements.

注: All power balls must be supplied with the voltages specified in [Section 5.4, Recommended Operating Conditions](#), unless otherwise specified in [4.3, Signal Descriptions](#).

表 4-76. Unused Balls Specific Connection Requirements

BALL NUMBER	BALL NAME	CONNECTION REQUIREMENTS
C22	OSC1_XI	Each of these balls must be connected to VSS through a separate external pull resistor to ensure these balls are held to a valid logic low level if unused.
AE4	WKUP_LFOSC0_XI	
AA3	TRSTn	
K2	MCU_ADC0_REFN	
K3	MCU_ADC0_REFP	
V5	MCU_BYP_POR	
H2	MCU_ADC1_REFP	
H3	MCU_ADC1_REFN	
K5	MCU_ADC0_AIN0	
J3	MCU_ADC0_AIN1	
J1	MCU_ADC0_AIN2	
J5	MCU_ADC0_AIN3	
K4	MCU_ADC0_AIN4	
J4	MCU_ADC0_AIN5	
J2	MCU_ADC0_AIN6	
J6	MCU_ADC0_AIN7	
F4	MCU_ADC1_AIN0	
G6	MCU_ADC1_AIN1	
G4	MCU_ADC1_AIN2	
H5	MCU_ADC1_AIN3	
F5	MCU_ADC1_AIN4	
G5	MCU_ADC1_AIN5	
G3	MCU_ADC1_AIN6	
H4	MCU_ADC1_AIN7	
F17	RESETz	Each of these balls must be connected to the corresponding power supply through a separate external pull resistor to ensure these balls are held to a valid logic high level if unused. ⁽¹⁾
W4	MCU_RESETz	
W5	MCU_PORz	
E19	PORz	
AA4	TCK	
A21	TMS	
AC7	WKUP_I2C0_SCL	
AD6	WKUP_I2C0_SDA	
AD7	MCU_I2C0_SDA	
AD8	MCU_I2C0_SCL	
F18	NMIIn	
C20	TDI	
A20	TDO	
AA1	EMU1	
AA2	EMU0	

表 4-76. Unused Balls Specific Connection Requirements (continued)

BALL NUMBER	BALL NAME	CONNECTION REQUIREMENTS
F21	VPP_CORE	This ball must be left unconnected if unused.
T6	VPP_MCU	
F23	MMC1_CALPAD	
D24	MMC0_CALPAD	

(1) To determine which power supply is associated with any IO refer to 表 4-1, *Pin Attributes*.

表 4-77. Reserved Balls Specific Connection Requirements

BALLS	CONNECTION REQUIREMENTS
AA6 (RSV2), B1 (RSV3), AC23 (RSV4), C12 (RSV5), F9 (RSV6), F10 (RSV7), AD10 (RSV8), AC13 (RSV9), B28 (RSV10), A27 (RSV11), D23 (RSV12), E23 (RSV13)	These balls must be left unconnected.
V4 (RSV1)	These balls must be connected to VSS through a separate external pull resistor to ensure these balls are held to a valid logic low level.

注: All other unused signal balls **with** a Pad Configuration Register can be left unconnected with their multiplexing mode set to GPIO input and internal pulldown resistor enabled.

Unused balls are defined as those which only connect to a PCB solder pad. This is the only use case where internal pull resistors are allowed as the only source/sink to hold a valid logic level.

Any balls connected to a via, test point, or PCB trace are considered used and must not depend on the internal pull resistor to hold a valid logic level.

Internal pull resistors are weak and may not source enough current to maintain a valid logic level for some operating conditions. This may be the case when connected to components with leakage to the opposite logic level, or when external noise sources couple to signal traces attached to balls which are only pulled to a valid logic level by the internal resistor. Therefore, external pull resistors may be required to hold a valid logic level on balls with external connections.

If balls are allowed to float between valid logic levels, the input buffer may enter a high-current state which could damage the IO cell.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾⁽²⁾

PARAMETERS		MIN	MAX	UNIT
VDD_CORE	Supply voltage range for CORE domain	-0.3	1.5	V
VDD_MCU	Supply voltage range for R5F MCU domain	-0.3	1.5	V
VDD_MPU0	Supply voltage range for A53 MPU0 domain	-0.3	1.5	V
VDD_MPU1	Supply voltage range for A53 MPU1 domain	-0.3	1.5	V
VDD_WKUP0	Supply voltage range for WKUP domain	-0.3	1.5	V
VDD_WKUP1	Supply voltage range for WKUP domain	-0.3	1.5	V
VDD_DLL_MMC0	Supply voltage range for MMC0 DLL	-0.3	1.5	V
VDD_DLL_MMC1	Supply voltage range for MMC1 DLL	-0.3	1.5	V
VDDA_1P8_CSI0	Supply voltage range for CSI PHY, Analog, 1.8 V	-0.3	2	V
VDDA_1P8_OLDI0	Supply voltage range for OLDI, Analog, 1.8 V	-0.3	2	V
VDDA_1P8_SDIO	Supply voltage range for SDIO LDO, Analog, 1.8 V	-0.3	2	V
VDDA_1P8_SERDES0	Supply voltage range for USB, PCIE, Analog, 1.8 V	-0.3	2	V
VDDA_3P3_IOLDO_WKUP	Supply voltage range for WKUP IO Bias LDO, Analog, 3.3 V	-0.3	3.8	V
VDDA_3P3_IOLDO0	Supply voltage range for IO Bias LDO, Analog 3.3 V	-0.3	3.8	V
VDDA_3P3_IOLDO1	Supply voltage range for IO Bias LDO, Analog 3.3 V	-0.3	3.8	V
VDDA_3P3_SDIO	Supply voltage range for SDIO LDO, Analog, 3.3 V	-0.3	3.8	V
VDDA_3P3_USB	Supply voltage range for USBPHY, Analog, 3.3 V	-0.3	3.8	V
VDDA_ADC_MCU	Supply voltage range for ADC0, ADC1, Analog	-0.3	2	V
VDDA_PLL0_DDR	Supply voltage range for DDR DPLL, Analog	-0.3	2	V
VDDA_PLL1_DDR	Supply voltage range for DDR De-skew DPLL, Analog	-0.3	2	V
VDDA_LDO_WKUP	Supply voltage range for WKUP LDO, Analog	-0.3	2	V
VDDA_MCU	Supply voltage range for MCU SRAM LDO, MCU DPLL, CPSW DPLL, Analog	-0.3	2	V
VDDA_PLL_CORE	Supply voltage range for CORE DPLL, PER1 DPLL, Analog	-0.3	2	V
VDDA_PLL_DSS	Supply voltage range for DSS DPLL, Analog	-0.3	2	V
VDDA_PLL_MPU0	Supply voltage range for MPU0 DPLL, Analog	-0.3	2	V
VDDA_PLL_MPU1	Supply voltage range for MPU1 DPLL, Analog	-0.3	2	V
VDDA_PLL_PER0	Supply voltage range for PER0 DPLL, Analog	-0.3	2	V
VDDA_POR_WKUP	Supply voltage range for WKUP POR, Analog	-0.3	2	V
VDDA_SRAM_CORE0	Supply voltage range for CORE SRAM LDOs, Analog	-0.3	2	V
VDDA_SRAM_CORE1	Supply voltage range for CORE SRAM LDOs, Analog	-0.3	2	V
VDDA_SRAM_MPU0	Supply voltage range for MPU SRAM LDOs, Analog	-0.3	2	V
VDDA_SRAM_MPU1	Supply voltage range for MPU SRAM LDOs, Analog	-0.3	2	V
VDDA_WKUP	Supply voltage range for WKUP OSC, SRAM LDO, Analog	-0.3	2	V
VDDS_DDR	Supply voltage range for DDR IO domain	-0.3	2	V
VDDS_OSC1	Supply voltage range for CORE HFOSC, Analog	-0.3	2	V
VDDS0	Supply voltage range for VDDSHV0 IO bias	-0.3	2	V
VDDS0_WKUP	Supply voltage range for VDDSHV0_WKUP IO bias	-0.3	2	V
VDDS1	Supply voltage range for VDDSHV1 IO bias	-0.3	2	V
VDDS1_WKUP	Supply voltage range for VDDSHV1_WKUP IO bias	-0.3	2	V
VDDS2	Supply voltage range for VDDSHV2 IO bias	-0.3	2	V
VDDS2_WKUP	Supply voltage range for VDDSHV2_WKUP IO bias	-0.3	2	V

Absolute Maximum Ratings (continued)over operating free-air temperature range (unless otherwise noted) ⁽¹⁾⁽²⁾

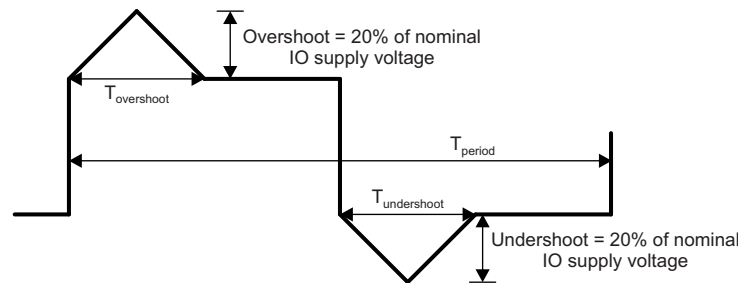
PARAMETERS			MIN	MAX	UNIT
VDDS3	Supply voltage range for VDDSHV3 IO bias		-0.3	2	V
VDDS4	Supply voltage range for VDDSHV4 IO bias		-0.3	2	V
VDDS5	Supply voltage range for VDDSHV5 IO bias		-0.3	2	V
VDDS6	Supply voltage range for VDDSHV6 IO bias		-0.3	2	V
VDDS7	Supply voltage range for VDDSHV7 IO bias		-0.3	2	V
VDDS8	Supply voltage range for VDDSHV8 IO bias		-0.3	2	V
VDDSHV0	Supply voltage range for dual-voltage IO domain	1.8 V	-0.3	2	V
		3.3 V	-0.3	3.8	V
VDDSHV0_WKUP	Supply voltage range for dual-voltage IO domain	1.8 V	-0.3	2	V
		3.3 V	-0.3	3.8	V
VDDSHV1	Supply voltage range for dual-voltage IO domain	1.8 V	-0.3	2	V
		3.3 V	-0.3	3.8	V
VDDSHV1_WKUP	Supply voltage range for dual-voltage IO domain	1.8 V	-0.3	2	V
		3.3 V	-0.3	3.8	V
VDDSHV2	Supply voltage range for dual-voltage IO domain	1.8 V	-0.3	2	V
		3.3 V	-0.3	3.8	V
VDDSHV2_WKUP	Supply voltage range for dual-voltage IO domain	1.8 V	-0.3	2	V
		3.3 V	-0.3	3.8	V
VDDSHV3	Supply voltage range for dual-voltage IO domain	1.8 V	-0.3	2	V
		3.3 V	-0.3	3.8	V
VDDSHV4	Supply voltage range for dual-voltage IO domain	1.8 V	-0.3	2	V
		3.3 V	-0.3	3.8	V
VDDSHV5	Supply voltage range for dual-voltage IO domain	1.8 V	-0.3	2	V
		3.3 V	-0.3	3.8	V
VDDSHV6	Supply voltage range for dual-voltage IO domain	1.8 V	-0.3	2	V
		3.3 V	-0.3	3.8	V
VDDSHV7	Supply voltage range for dual-voltage IO domain	1.8 V	-0.3	2	V
		3.3 V	-0.3	3.8	V
VDDSHV8	Supply voltage range for dual-voltage IO domain	1.8 V	-0.3	2	V
		3.3 V	-0.3	3.8	V
VDDA_VSYS_MON	Supply monitor for system		-0.3	2	V
VPP_CORE	Supply voltage range for CORE EFUSE domain		TBD	TBD	V
VPP_MCU	Supply voltage range for MCU EFUSE domain		TBD	TBD	V
USB0_VBUS	Voltage range for USB VBUS comparator input		TBD	TBD	V
USB1_VBUS	Voltage range for USB VBUS comparator input		TBD	TBD	V
Steady State Max. Voltage at all fail-safe IO pins	I2C0_SCL, I2C0_SDA, I2C1_SCL, I2C1_SDA, NMIn, VDDA_3P3_MON_WKUP, VDDA_3P3_MON0		-0.3	3.8	V
	VDDA_1P8_MON_WKUP, VDDA_1P8_MON0		-0.3	2	V
	DDR_FS_RESETh		TBD	TBD	V
Steady State Max. Voltage at all other IO pins ⁽³⁾	VDDA_VSYS_MON ⁽⁴⁾		-0.3	VDDA_POR_WKUP + 0.3	V
	All other IO pins		-0.3	IO supply voltage + 0.3	V
Transient Overshoot and Undershoot specification at IO pin	20% of IO supply voltage for up to 20% of signal period (see Figure 5-1, IO Transient Voltage Ranges)		0.2 × VDD ⁽⁶⁾		V
Latch-up Performance ⁽⁵⁾	Class II (105°C)		TBD	TBD	mA
	Class II (125°C)		TBD	TBD	mA
T _{STG} ⁽⁷⁾	Storage temperature		-55	+150	°C

Absolute Maximum Ratings (continued)

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾⁽²⁾

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under [Section 5.4, Recommended Operating Conditions](#) is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to their associated VSS or VSSA_x, unless otherwise noted.
- (3) This parameter applies to all IO pins which are not fail-safe and the requirement applies to all values of IO supply voltage. For example, if the voltage applied to a specific IO supply is 0 volts the valid input voltage range for any IO powered by that supply will be –0.3 to +0.3 volts. Special attention should be applied anytime peripheral devices are not powered from the same power sources used to power the respective IO supply. It is important the attached peripheral never sources a voltage outside the valid input voltage range, including power supply ramp-up and ramp-down sequences.
- (4) The VDDA_VSYS_MON pin provides a way to monitor the system power supply and is not fail-safe, unless implemented with the appropriate resistor voltage divider source. For more information, see [7.5, System Power Supply Monitor Design Guidelines](#).
- (5) For current pulse injection:
Pins stressed per JEDEC JESD78D (Class II) and passed with specified I/O pin injection current and clamp voltage of 1.5 times maximum recommended I/O voltage and negative 0.5 times maximum recommended I/O voltage.
For overvoltage performance:
Supplies stressed per JEDEC JESD78D (Class II) and passed specified voltage injection.
- (6) VDD is the voltage on the corresponding power-supply pin(s) for the IO.
- (7) For tape and reel the storage temperature range is [–10°C; +50°C] with a maximum relative humidity of 70%. TI recommends returning to ambient room temperature before usage.

Fail-safe IO terminals are designed such they do not have dependencies on the respective IO power supply voltage. This allows external voltage sources to be connected to these IO terminals when the respective IO power supplies are turned off. The I2C0_SCL, I2C0_SDA, I2C1_SCL, I2C1_SDA, DDR_FS_RESETn, NMIn, VDDA_1P8_MON_WKUP, VDDA_1P8_MON0, VDDA_3P3_MON_WKUP, and VDDA_3P3_MON0 are the only fail-safe IO terminals. All other IO terminals are not fail-safe and the voltage applied to them should be limited to the value defined by the Steady State Max. Voltage at all IO pins parameter in [Section 5.1, Absolute Maximum Ratings](#).



$$(1) \quad T_{\text{overshoot}} + T_{\text{undershoot}} < 20\% \text{ of } T_{\text{period}}$$

图 5-1. IO Transient Voltage Ranges

5.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	TBD
		Charged-device model (CDM), per JEDEC specification ANSI/ESDA/JEDEC JS-002 ⁽²⁾	TBD

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Power-On-Hour (POH) Limits⁽¹⁾⁽²⁾⁽³⁾

OPERATING CONDITION	COMMERCIAL TEMPERATURE RANGE		EXTENDED TEMPERATURE RANGE	
OPP	JUNCTION TEMPERATURE (T _J)	LIFETIME (POH)	JUNCTION TEMP (T _J)	LIFETIME (POH)
OPP_NOM	0°C to 90°C	100k	-40°C to 105°C	100k
OPP_OD		100k		100k
OPP_TURBO		TBD		TBD

(1) This information is provided solely for your convenience and does not extend or modify the warranty provided under TI's standard terms and conditions for TI semiconductor products.

(2) Unless specified in the table above, all voltage domains and operating conditions are supported in the device at the noted temperatures.

(3) POH is a function of voltage, temperature and time. Usage at higher voltages and temperatures will result in a reduction in POH.

5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

SUPPLY NAME	DESCRIPTION		MIN ⁽¹⁾	NOM	MAX ⁽¹⁾	UNIT
VDD_CORE ⁽³⁾	CORE voltage domain supply		0.95	1	1.05	V
VDD_MCU ⁽³⁾	MCU voltage domain supply		0.95	1	1.05	V
VDD_MPU0 ⁽³⁾	MPU0 voltage domain supply	OPP_NOM	0.95	1	1.05	V
		OPP_OD	1.05	1.1	1.15	V
		OPP_TURBO	1.16	1.22	1.28	V
VDD_MPU1 ⁽³⁾	MPU1 voltage domain supply	OPP_NOM	0.95	1	1.05	V
		OPP_OD	1.05	1.1	1.15	V
		OPP_TURBO	1.16	1.22	1.28	V
VDD_WKUP0	WKUP voltage domain supply		0.95	1	1.05	V
VDD_WKUP1	WKUP voltage domain supply		0.95	1	1.05	V
VDD_DLL_MMC0	MMC0 PHY DLL voltage supply		0.95	1	1.05	V
	Maximum peak-to-peak supply noise				TBD	mV _{PPmax}
VDD_DLL_MMC1	MMC1 PHY DLL voltage supply		0.95	1	1.05	V
	Maximum peak-to-peak supply noise				TBD	mV _{PPmax}
VDDA_1P8_CSI0	CSI PHY analog power supply		1.71	1.8	1.89	V
VDDA_1P8_SDIO	SDIO LDO analog power supply		1.71	1.8	1.89	V
VDDA_1P8_OLDI0	OLDI analog power supply		1.71	1.8	1.89	V
VDDA_1P8_SERDES0	SERDES0/1 (USB, PCIE, SGMII) analog power supply		1.71	1.8	1.89	V
VDDA_3P3_IOLDO_WKUP	WKUP IO Bias LDO analog power supply		3.14	3.3	3.46	V
VDDA_3P3_IOLDO0	IO Bias LDO analog power supply		3.14	3.3	3.46	V
VDDA_3P3_IOLDO1	IO Bias LDO analog power supply		3.14	3.3	3.46	V
VDDA_3P3_SDIO	SDIO LDO analog power supply		3.14	3.3	3.46	V
VDDA_3P3_USB	USB analog power supply		3.14	3.3	3.46	V
VDDA_1P8_MON_WKUP	1.8V supply monitor in WKUP domain		1.71	1.8	1.89	V
VDDA_1P8_MON0	1.8V supply monitor in MAIN domain		1.71	1.8	1.89	V
VDDA_3P3_MON_WKUP	3.3V supply monitor in WKUP domain		3.14	3.3	3.46	V
VDDA_3P3_MON0	3.3V supply monitor in MAIN domain		3.14	3.3	3.46	V
VDDA_VSYS_MON	Supply monitor for system		0	see ⁽⁶⁾	1	V
VDDA_ADC_MCU	ADC0, ADC1 analog power supply		1.71	1.8	1.89	V
VDDA_LDO_WKUP	WKUP LDO analog power supply		1.71	1.8	1.89	V
VDDA_MCU	MCU SRAM LDO, MCU DPLL, CPSW DPLL analog power supply		1.71	1.8	1.89	V
VDDA_PLL_CORE	CORE DPLL, PER1 DPLL analog power supply		1.71	1.8	1.89	V
	Maximum peak-to-peak supply noise				50	mV _{PPmax}

Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

SUPPLY NAME	DESCRIPTION	MIN ⁽¹⁾	NOM	MAX ⁽¹⁾	UNIT	
VDDA_PLL0_DDR	DDR DPLL analog power supply	1.71	1.8	1.89	V	
	Maximum peak-to-peak supply noise			50	mV _{PPmax}	
VDDA_PLL1_DDR	DDR De-skew DPLL analog power supply	1.71	1.8	1.89	V	
	Maximum peak-to-peak supply noise			50	mV _{PPmax}	
VDDA_PLL_DSS	DSS DPLL analog power supply	1.71	1.8	1.89	V	
	Maximum peak-to-peak supply noise			50	mV _{PPmax}	
VDDA_PLL_MPU0	MPU0 DPLL analog power supply	1.71	1.8	1.89	V	
	Maximum peak-to-peak supply noise			50	mV _{PPmax}	
VDDA_PLL_MPU1	MPU1 DPLL analog power supply	1.71	1.8	1.89	V	
	Maximum peak-to-peak supply noise			50	mV _{PPmax}	
VDDA_PLL_PER0	PER0 DPLL analog power supply	1.71	1.8	1.89	V	
	Maximum peak-to-peak supply noise			50	mV _{PPmax}	
VDDA_POR_WKUP	WKUP POR/POK analog power supply	1.71	1.8	1.89	V	
VDDA_SRAM_CORE0	CORE SRAM LDOs analog power supply	1.71	1.8	1.89	V	
VDDA_SRAM_CORE1	CORE SRAM LDOs analog power supply	1.71	1.8	1.89	V	
VDDA_SRAM_MPU0	MPU SRAM LDOs analog power supply	1.71	1.8	1.89	V	
VDDA_SRAM_MPU1	MPU SRAM LDOs analog power supply	1.71	1.8	1.89	V	
VDDA_WKUP	WKUP High/Low Frequency Oscillator (WKUP_LFOSC0 / WKUP_OSC0), SRAM LDO analog power supply	1.71	1.8	1.89	V	
VDDS_DDR ⁽⁴⁾	DDR IO domain power supply (DDR3L)	1.28	1.35	1.42	V	
	DDR IO domain power supply (DDR4)	1.14	1.2	1.26	V	
	DDR IO domain power supply (LPDDR4)	1.05	1.1	1.15	V	
VDDS_OSC1	MAIN High Frequency Oscillator (OSC1) analog power supply	1.71	1.8	1.89	V	
VDDS0	IO bias supply for VDDSHV0	1.71	1.8	1.89	V	
VDDS0_WKUP	IO bias supply for VDDSHV0_WKUP	1.71	1.8	1.89	V	
VDDS1	IO bias supply for VDDSHV1	1.71	1.8	1.89	V	
VDDS1_WKUP	IO bias supply for VDDSHV1_WKUP	1.71	1.8	1.89	V	
VDDS2	IO bias supply for VDDSHV2	1.71	1.8	1.89	V	
VDDS2_WKUP	IO bias supply for VDDSHV2_WKUP	1.71	1.8	1.89	V	
VDDS3	IO bias supply for VDDSHV3	1.71	1.8	1.89	V	
VDDS4	IO bias supply for VDDSHV4	1.71	1.8	1.89	V	
VDDS5	IO bias supply for VDDSHV5	1.71	1.8	1.89	V	
VDDS6	IO bias supply for VDDSHV6	1.71	1.8	1.89	V	
VDDS7	IO bias supply for VDDSHV7	1.71	1.8	1.89	V	
VDDS8	IO bias supply for VDDSHV8	1.71	1.8	1.89	V	
VDDSHV0	Dual-voltage IO domain power supply	1.8-V operation	1.71	1.8	1.89	V
		3.3-V operation	3.14	3.3	3.46	V
VDDSHV0_WKUP	Dual-voltage IO domain power supply	1.8-V operation	1.71	1.8	1.89	V
		3.3-V operation	3.14	3.3	3.46	V
VDDSHV1	Dual-voltage IO domain power supply	1.8-V operation	1.71	1.8	1.89	V
		3.3-V operation	3.14	3.3	3.46	V
VDDSHV1_WKUP	Dual-voltage IO domain power supply	1.8-V operation	1.71	1.8	1.89	V
		3.3-V operation	3.14	3.3	3.46	V
VDDSHV2	Dual-voltage IO domain power supply	1.8-V operation	1.71	1.8	1.89	V
		3.3-V operation	3.14	3.3	3.46	V

Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

SUPPLY NAME	DESCRIPTION		MIN ⁽¹⁾	NOM	MAX ⁽¹⁾	UNIT
VDDSHV2_WKUP	Dual-voltage IO domain power supply	1.8-V operation	1.71	1.8	1.89	V
		3.3-V operation	3.14	3.3	3.46	V
VDDSHV3	Dual-voltage IO domain power supply	1.8-V operation	1.71	1.8	1.89	V
		3.3-V operation	3.14	3.3	3.46	V
VDDSHV4	Dual-voltage IO domain power supply	1.8-V operation	1.71	1.8	1.89	V
		3.3-V operation	3.14	3.3	3.46	V
VDDSHV5	Dual-voltage IO domain power supply	1.8-V operation	1.71	1.8	1.89	V
		3.3-V operation	3.14	3.3	3.46	V
VDDSHV6	Dual-voltage IO domain power supply	1.8-V operation	1.71	1.8	1.89	V
		3.3-V operation	3.14	3.3	3.46	V
VDDSHV7	Dual-voltage IO domain power supply	1.8-V operation	1.71	1.8	1.89	V
		3.3-V operation	3.14	3.3	3.46	V
VDDSHV8	Dual-voltage IO domain power supply	1.8-V operation	1.71	1.8	1.89	V
		3.3-V operation	3.14	3.3	3.46	V
USB0_VBUS	Voltage range for USB VBUS comparator input		0	TBD	TBD	V
USB1_VBUS	Voltage range for USB VBUS comparator input		0	TBD	TBD	V
USB0_ID	Voltage range for the USB ID input		see ⁽⁵⁾			V
USB1_ID	Voltage range for the USB ID input		see ⁽⁵⁾			V
VSS	Ground		0			V
T _J	Operating junction temperature range	Extended	-40		105	°C
		Commercial	0		90	°C

- (1) The voltage at the device ball must never be below the MIN voltage or above the MAX voltage for any amount of time. This requirement includes dynamic voltage events such as AC ripple, voltage transients, voltage dips, and so forth.
- (2) Refer to [Section 5.3, Power-On-Hour \(POH\) Limits](#) for limitations.
- (3) This value is without AVS. The AVS Voltages are device-dependent, voltage domain-dependent, and OPP-dependent. They must be read from the VTM_DEVINFO_VDn. For information about VTM_DEVINFO_VDn Registers address, please refer to section *Voltage and Thermal Manager (VTM)* in the device TRM. The power supply should be adjustable over the following ranges for each required OPP:
 - OPP_NOM: TBD
 - OPP_OD: TBD
 - OPP_TURBO: TBD
 The AVS Voltages will be within the above specified ranges.
- (4) VDDSD_DDR is required to still be powered with either DDR3L, DDR4, or LPDDR4 voltage ranges, even if DDR interface is unused.
- (5) This terminal is connected to analog circuits in the respective USB PHY. The circuit sources a known current while measuring the voltage to determine if the terminal is connected to VSS with a resistance less than 10 Ω or greater than 100 kΩ. The terminal should be connected to ground for USB host operation or open-circuit for USB peripheral operation, and should never be connected to any external voltage source.
- (6) The VDDA_VSYS_MON pin provides a way to monitor the system power supply and is not fail-safe, unless implemented with the appropriate resistor voltage divider source. For more information, see [7.5, System Power Supply Monitor Design Guidelines](#).

5.5 Operating Performance Points

This section describes the operating conditions of the device. This section also contains the description of each operating performance point for processor clocks and device core clocks.

注: The OPP voltage and frequency values may change following the silicon characterization result.

表 5-1 describes the maximum supported frequency per speed grade for the device.

表 5-1. Speed Grade Maximum Frequency⁽¹⁾

DEVICE SPEED	MAXIMUM FREQUENCY (MHz)							
	MPU	MCU	DMSC	GPU	CBASS0	ICSSG	DDR3L/DDR4	LPDDR4
AM6548xxX	1100	400	200	450	250	250	800 (DDR-1600)	667 (DDR-1333)
AM6528xxX	1100	400	200	450	250	250	800 (DDR-1600)	667 (DDR-1333)
AM6546xxX	1100	400	200	N/A	250	250	800 (DDR-1600)	667 (DDR-1333)
AM6526xxX	1100	400	200	N/A	250	250	800 (DDR-1600)	667 (DDR-1333)
AM6527xxX	1100	400	200	N/A	250	250	800 (DDR-1600)	667 (DDR-1333)

(1) N/A stands for Not Applicable.

5.5.1 Core Clock Specifications

表 5-2 describes the standard processor clocks speed characteristics vs OPP of the device.

表 5-2. Supported OPP vs Max Frequency⁽¹⁾⁽²⁾

DESCRIPTION	OPP_NOM	OPP_OD	OPP_TURBO
	MAXIMUM FREQUENCY (MHz)	MAXIMUM FREQUENCY (MHz)	MAXIMUM FREQUENCY (MHz)
VD_CORE			
GPU	450	N/A	N/A
DDR3L/DDR4	800 (DDR-1600)	N/A	N/A
LPDDR4	667 (DDR-1333)	N/A	N/A
CBASS0	250	N/A	N/A
ICSSG	250	N/A	N/A
VD_MPU0			
MPU0	800	1000	1100
VD_MPU1			
MPU1	800	1000	1100
VD_MCU			
MCU	400	N/A	N/A
VD_WKUP			
DMSC	200	N/A	N/A

(1) N/A stands for Not Applicable.

(2) Maximum supported frequency is limited according to the 表 5-1, Speed Grade Maximum Frequency.

5.6 Electrical Characteristics

注: The interfaces or signals described in 表 5-3 through 表 5-9 correspond to the interfaces or signals available in multiplexing mode 0 (Primary Function).

All interfaces or signals multiplexed on the balls described in these tables have the same DC electrical characteristics, unless multiplexing involves a PHY and GPIO combination, in which case different DC electrical characteristics are specified for the different multiplexing modes (Functions).

表 5-3. I2C OPEN DRAIN DC Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
BALL NAMES in Mode 0: WKUP_I2C0_SCL / WKUP_I2C0_SDA / MCU_I2C0_SCL / MCU_I2C0_SDA					
BALL NUMBERS: AC7 / AD6 / AD7 / AD8					
I2C STANDARD MODE / FAST MODE - VDDSHV0_WKUP = 1.8 V					
V _{IH}	High-level input threshold	0.7 × VDDSHV0_WKUP			V
V _{IL}	Low-level input threshold	0.3 × VDDSHV0_WKUP			V
V _{HYS}	Hysteresis	0.1 × VDDSHV0_WKUP			V
I _{IN}	Input leakage current. This value represents the maximum current flowing in or out of the pin while the output driver is disabled and the input is swept from VSS to VDD.	12			μA
I _{OZ}	Total leakage current through the driver/receiver combination, which may include an internal pull-up or pull-down. This value represents the maximum current flowing in or out of the pin while the output driver is disabled, the pull-up or pull-down is inhibited, and the input is swept from VSS to VDD.	12			μA
V _{OL}	Low-level output voltage at 3-mA sink current	0.2 × VDDSHV0_WKUP			V
I2C STANDARD MODE / FAST MODE - VDDSHV0_WKUP = 3.3 V					
V _{IH}	High-level input voltage	0.7 × VDDSHV0_WKUP			V
V _{IL}	Low-level input voltage	0.3 × VDDSHV0_WKUP			V
V _{HYS}	Hysteresis	0.05 × VDDSHV0_WKUP			V
I _{IN}	Input leakage current. This value represents the maximum current flowing in or out of the pin while the output driver is disabled and the input is swept from VSS to VDD.	80			μA
I _{OZ}	Total leakage current through the driver/receiver combination, which may include an internal pull-up or pull-down. This value represents the maximum current flowing in or out of the pin while the output driver is disabled, the pull-up or pull-down is inhibited, and the input is swept from VSS to VDD.	80			μA
V _{OL}	Low-level output voltage at 3-mA sink current	0.4			V

表 5-4. Analog OSC Buffers DC Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER	MIN	TYP	MAX	UNIT
BALL NAMES: OSC1_XI / WKUP_OSC0_XI				

表 5-4. Analog OSC Buffers DC Electrical Characteristics (continued)

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
BALL NUMBERS: C22 / AD5					
HIGH FREQUENCY OSCILLATOR					
V _{IH}	High-level input voltage	0.65 × VDD _S ⁽¹⁾			V
V _{IL}	Low-level input voltage	0.35 × VDD _S ⁽¹⁾			V
BALL NAMES: WKUP_LFOSC0_XI					
BALL NUMBERS: AE4					
LOW FREQUENCY OSCILLATOR					
V _{IH}	High-level input voltage	0.65 × VDDA_WKUP			V
V _{IL}	Low-level input voltage	0.35 × VDDA_WKUP			V

(1) VDD_S stands for corresponding power supply. For WKUP_OSC0_XI, the corresponding power supply is VDDA_WKUP. For OSC1_XI, the corresponding power supply is VDD_S_OSC1.

表 5-5. UHS-I MMC (8-bit PHY) Buffers DC Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	NOM	MAX	UNIT
BALL NAMES in Mode 0: MMC0_CLK / MMC0_CMD / MMC0_DS / MMC0_DAT[7:0] / MMC1_CLK / MMC1_CMD / MMC1_DAT[3:0] / MMC0_CALPAD / MMC1_CALPAD					
BALL NUMBERS: A24 / A25 / A26 / B25 / B26 / B27 / C25 / C26 / C27 / C28 / D24 / D25 / D26 / D27 / D28 / E24 / E25 / E27 / F23					
V _{IH}	Input High-Level Voltage	0.65 × VDD _S ⁽¹⁾			V
V _{IL}	Input Low-Level Voltage	0.35 × VDD _S ⁽¹⁾			V
V _{OH}	Output High-Level Threshold	0.75 × VDD _S ⁽¹⁾			V
V _{OL}	Output Low-Level Threshold	0.125 × VDD _S ⁽¹⁾			V
I _{IN}	Input Leakage Current	10			μA

(1) VDD_S stands for corresponding power supply (that is VDDSHV6 or VDDSHV7). For more information on the power supply name and the corresponding ball, see 表 4-1, POWER [9] column.

表 5-6. Analog ADC DC Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
BALL NAMES in Mode 0: MCU_ADC0_AIN[7:0] / MCU_ADC0_REFP/N / MCU_ADC1_AIN[7:0] / MCU_ADC1_REFP/N						
BALL NUMBERS: F4 / F5 / G3 / G4 / G5 / G6 / H2 / H3 / H4 / H5 / J1 / J2 / J3 / J4 / J5 / J6 / K2 / K3 / K4 / K5						
Analog Input						
V _{MCU_ADC0/1_REFP}	MCU_ADC0/1_REFP		(0.5 x VDDA_ADC_MCU) + 0.25	VDDA_ADC_MCU		V
V _{MCU_ADC0/1_REFN}	MCU_ADC0/1_REFN		0	(0.5 x VDDA_ADC_MCU) - 0.25		V
V _{MCU_ADC0/1_REFP + MCU_ADC0/1_REFN}	MCU_ADC0/1_REFP + MCU_ADC0/1_REFN		VDDA_ADC_MCU			V
V _{MCU_ADC0/1_AIN[7:0]}	Full-scale Input Range		MCU_ADC0/1_REFN	MCU_ADC0/1_REFP		V
DNL	Differential Non-Linearity	MCU_ADC0/1_REFP = VDDA_MCU_ADC0/1, MCU_ADC0/1_REFN = VSS	-1	0.5	TBD	LSB
INL	Integral Non-Linearity	MCU_ADC0/1_REFP = VDDA_MCU_ADC0/1, MCU_ADC0/1_REFN = VSS		±1	±2	LSB
LSB _{GAIN-ERROR}	Gain Error	MCU_ADC0/1_REFP = VDDA_MCU_ADC0/1, MCU_ADC0/1_REFN = VSS		±2		LSB
LSB _{OFFSET-ERROR}	Offset Error	MCU_ADC0/1_REFP = VDDA_MCU_ADC0/1, MCU_ADC0/1_REFN = VSS		±2		LSB
C _{IN}	Input Sampling Capacitance			5.5		pF
SNR	Signal-to-Noise Ratio	Input Signal: 200 kHz sine wave at -0.5 dB Full Scale, MCU_ADC0/1_REFP = VDDA_MCU_ADC0/1, MCU_ADC0/1_REFN = VSS		70		dB
THD	Total Harmonic Distortion	Input Signal: 200 kHz sine wave at -0.5 dB Full Scale, MCU_ADC0/1_REFP = VDDA_MCU_ADC0/1, MCU_ADC0/1_REFN = VSS		75		dB
SFDR	Spurious Free Dynamic Range	Input Signal: 200 kHz sine wave at -0.5 dB Full Scale, MCU_ADC0/1_REFP = VDDA_MCU_ADC0/1, MCU_ADC0/1_REFN = VSS		80		dB

表 5-6. Analog ADC DC Electrical Characteristics (continued)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SNR _(PLUS)	Signal-to-Noise Plus Distortion	Input Signal: 200 kHz sine wave at -0.5 dB Full Scale, MCU_ADC0/1_REFP = VDDA_MCU_ADC0/1, MCU_ADC0/1_REFN = VSS		69		dB
R _{static} (MCU_ADC0/1_REFP, MCU_ADC0/1_REFN)	Static Input Impedance of MCU_ADC0/1_REFP relative to MCU_ADC0/1_REFN			2.2		kΩ
R _{dynamic} (MCU_ADC0/1_REFP, MCU_ADC0/1_REFN)	Dynamic Input Impedance of MCU_ADC0/1_REFP relative to MCU_ADC0/1_REFN			$[1/((65.97 \times 10^{-12}) \times f_{\text{SMPL_CLK}})]^{(1)}$		Ω
R _{MCU_ADC0/1_AIN[0:7]}	Input Impedance of MCU_ADC0/1_AIN[7:0]	f = input frequency		$[1/((65.97 \times 10^{-12}) \times f_{\text{SMPL_CLK}})]$		Ω
I _{IN}	Input Leakage	MCU_ADC0/1_AIN[7:0] = VSS			-126	μA
		MCU_ADC0/1_AIN[7:0] = VDDA_MCU_ADC0/1			572	μA
Sampling Dynamics						
F _{SMPL_CLK}	SMPL_CLK Frequency		TBD		60	MHz
t _C	Conversion Time			13		ADC0/1 SMPL_CLK Cycles
t _{ACQ}	Acquisition time		2		257	ADC0/1 SMPL_CLK Cycles
T _R	Sampling Rate	ADC0/1 SMPL_CLK = 60 MHz			4	MSPS
CCISO	Channel to Channel Isolation			100		dB

(1) The MCU_ADC0/1_REFP and MCU_ADC0/1_REFN source impedance should be $\leq 1/10 \times (R_{\text{dynamic}}(\text{MCU_ADC0/1_REFP}, \text{MCU_ADC0/1_REFN}))$. For example, for a 60 MHz clock, this source should be $\leq 25 \Omega$ on each reference input.

表 5-7. DPHY CSI2 Buffers DC Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	NOM	MAX	UNIT
BALL NAMES in Mode 0: CSIO_RXN0 / CSIO_RXN3 / CSIO_RXN4 / CSIO_RXP0 / CSIO_RXP3 / CSIO_RXP4 / CSIO_RXN1 / CSIO_RXN2 / CSIO_RXP1 / CSIO_RXP2					
BALL NUMBERS: F24 / F26 / F28 / G24 / G25 / G26 / G27 / G28 / H25 / H27					
Low-Power Receiver (LP-RX)					
V _{IH}	High-level input voltage	880			mV
V _{IL}	Low-level input voltage			550	mV
V _{HYS}	Hysteresis	25			mV
Ultra-Low Power Receiver (ULP-RX)					
V _{ITH}	High-level input voltage	880			mV
V _{ITL-ULPM}	Low-level input voltage			300	mV
V _{HYS}	Hysteresis	25			mV
High Speed Receiver (HS-RX)					
V _{IDTH}	Differential input high threshold	70			mV
V _{IDTL}	Differential input low threshold			-70	mV
V _{IDMAX}	Maximum differential input voltage			270	mV
V _{ILHS}	Single-ended input low voltage	-40			mV
V _{IHHS}	Single-ended input high voltage			460	mV
V _{CMRXDC}	Common-mode voltage	70		330	mV

表 5-8. OLDI LVDS Buffers DC Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
1.8-V MODE						
BALL NAMES in Mode 0: OLDIO_A0P/N / OLDIO_A1P/N / OLDIO_A2P/N / OLDIO_A3P/N / OLDIO_CLKP/N						
BALL NUMBERS: J24 / J26 / J28 / K24 / K25 / K26 / K27 / K28 / L25 / L27						
OLDI LVDS TRANSMITTER						
V _{OH}	High Level Output Voltage	Differential Load =100Ω		1.3	1.6	V
V _{OL}	Low Level Output Voltage		0.9	1.01		V
V _{CM}	Common Mode Voltage (OLDI)		1.125	1.25	1.375	V
	Common Mode Voltage (sub-LVDS)			0.9		V
ΔV _{CM}	Difference in Common Mode Output Voltage, between high/low steady-states				35	mV
V _{OD}	Differential Output Voltage		250	380	450	mV
	Reduced Differential Output Voltage		100	200	300	mV
ΔV _{OD}	Difference in Differential Output Voltage, between high/low steady states				50	mV
I _{OS}	Output Short Circuit Current	PAD/PADN=0, Differential Load =100Ω			-5	mA
I _{OZ}	Output Tri-State Current	PAD/PADN = 0/VDD ⁽¹⁾	-10	4	40	μA

(1) VDD_S stands for corresponding power supply. For more information on the power supply name and the corresponding ball, see 表 4-1, POWER [9] column.

表 5-9. LVCMOS Buffers DC Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER	SPECIFIC BALL	MIN	TYP	MAX	UNIT
BALL NAMES: ALL LVCMOS IOs as defined in 表 4-1, Pin Attributes					
BALL NUMBERS: ALL LVCMOS IOs as defined in 表 4-1, Pin Attributes					

表 5-9. LVCMOS Buffers DC Electrical Characteristics (continued)

over recommended operating conditions (unless otherwise noted)

PARAMETER		SPECIFIC BALL	MIN	TYP	MAX	UNIT
1.8-V MODE						
V _{IH}	Input high-level threshold	TCK (AA4)	0.60 * VDD _S ⁽¹⁾			V
		All other I/Os	0.65 * VDD _S ⁽¹⁾			
V _{IL}	Input low-level threshold	TCK (AA4)			0.30 * VDD _S ⁽¹⁾	V
		All other I/Os			0.35 * VDD _S ⁽¹⁾	
V _{HYS}	Input hysteresis voltage	TCK (AA4)	400			mV
		PORz (E19), MCU_PORz (W5), MCU_BYP_POR (V5)	50			
		All other I/Os	100			
V _{OH}	Output high-level threshold	I _{OH} = 100μA	VDD _S ⁽¹⁾ -0.1			V
		I _{OH} = 2mA	VDD _S ⁽¹⁾ -0.2			
		I _{OH} = 4mA	VDD _S ⁽¹⁾ -0.3			
		I _{OH} = 6mA	VDD _S ⁽¹⁾ -0.4			
V _{OL}	Output low-level threshold	I _{OL} = 100μA			0.1	V
		I _{OL} = 2mA			0.2	
		I _{OL} = 4mA			0.3	
		I _{OL} = 6mA			0.4	
I _{IN}	Input leakage current, pull-up or pull-down inhibited				11.5	μA
		Input leakage current, pull-down enabled, V _I = VDD _S ⁽¹⁾	65	96	153	
		Input leakage current, pull-up enabled, V _I = VSS	64	97	154	
I _{OZ}	Total leakage current through the driver/receiver combination, which may include an internal pull-up or pull-down. This value represents the maximum current flowing in or out of the pin while the output driver is disabled, the pull-up or pull-down is inhibited, and the input is swept from VSS to VDD.				11.5	μA
3.3-V MODE						
V _{IH}	Input high-level threshold	TCK (AA4)	2			V
		All other I/Os	2			
V _{IL}	Input low-level threshold	TCK (AA4)			0.8	V
		All other I/Os			0.8	
V _{HYS}	Input hysteresis voltage	TCK (AA4)	400			mV
		PORz (E19), MCU_PORz (W5), MCU_BYP_POR (V5)	50			
		All other I/Os	100			
V _{OH}	Output high-level threshold	I _{OH} = 100μA	VDD _S ⁽¹⁾ -0.1			V
		I _{OH} = 2mA	VDD _S ⁽¹⁾ -0.2			
		I _{OH} = 4mA	VDD _S ⁽¹⁾ -0.3			
		I _{OH} = 6mA	VDD _S ⁽¹⁾ -0.45			

表 5-9. LVCMOS Buffers DC Electrical Characteristics (continued)

over recommended operating conditions (unless otherwise noted)

PARAMETER		SPECIFIC BALL	MIN	TYP	MAX	UNIT
V _{OL}	Output low-level threshold	I _{OL} = 100μA			0.1	V
		I _{OL} = 2mA			0.2	
		I _{OL} = 4mA			0.3	
		I _{OL} = 6mA			0.45	
I _{IN}	Input leakage current, pull-up or pull-down inhibited				64	μA
	Input leakage current, pull-down enabled, V _I = V _{DD} ⁽¹⁾		67	100.7	198	
	Input leakage current, pull-up enabled, V _I = V _{SS}		63	100.3	160	
I _{OZ}	Total leakage current through the driver/receiver combination, which may include an internal pull-up or pull-down. This value represents the maximum current flowing in or out of the pin while the output driver is disabled, the pull-up or pull-down is inhibited, and the input is swept from V _{SS} to V _{DD} .				64	μA

(1) V_{DD} stands for corresponding power supply. For more information on the power supply name and the corresponding ball, see 表 4-1, POWER [9] column.

表 5-10. LVCMOS-FS Buffers DC Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BALL NAMES in Mode 0: I2C0_SCL / I2C0_SDA / I2C1_SCL / I2C1_SDA / NMIn						
BALL NUMBERS: D20 / C21 / B21 / E21 / F18						
1.8-V MODE						
V _{IH}	High-level input threshold		1.21			V
V _{IL}	Low-level input threshold				0.55	V
V _{OH}	High-level output threshold	I _{OH} = 1 mA	V _{DDSHV0} - 0.45			V
V _{OL}	Low-level output threshold	I _{OL} = 1 mA			0.45	V
I _{IN}	Input leakage current. This value represents the maximum current flowing in or out of the pin while the output driver is disabled and the input is swept from V _{SS} to V _{DD} .	V _I = V _{DDSHV0}			6	μA
		V _I = V _{SS}			2.6	μA
I _{OZ}	Total leakage current through the driver/receiver combination, which may include an internal pull-up or pull-down. This value represents the maximum current flowing in or out of the pin while the output driver is disabled, the pull-up or pull-down is inhibited, and the input is swept from V _{SS} to V _{DD} .				6	μA
3.3-V MODE						
V _{IH}	High-level input threshold		1.21			V
V _{IL}	Low-level input threshold				0.55	V
V _{OH}	High-level output threshold	I _{OH} = 100 μA	V _{DDSHV0} - 0.2			V
V _{OL}	Low-level output threshold	I _{OL} = 100 μA			0.2	V
I _{IN}	Input leakage current. This value represents the maximum current flowing in or out of the pin while the output driver is disabled and the input is swept from V _{SS} to V _{DD} .	V _I = V _{DDSHV0}			45	μA
		V _I = V _{SS}			1	μA

表 5-10. LVCMOS-FS Buffers DC Electrical Characteristics (continued)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{OZ}	Total leakage current through the driver/receiver combination, which may include an internal pull-up or pull-down. This value represents the maximum current flowing in or out of the pin while the output driver is disabled, the pull-up or pull-down is inhibited, and the input is swept from VSS to VDD.				45	μA

5.6.1 USBHS Buffers DC Electrical Characteristics

注: USB0 and USB1 Electrical Characteristics are compliant with Universal Serial Bus Revision 2.0 Specification dated April 27, 2000 including ECNs and Errata as applicable.

5.6.2 SERDES Buffers DC Electrical Characteristics

注: The PCIe interfaces are compliant with the electrical parameters specified in PCI Express® Base Specification Revision 3.1.

注: USB0 instance is compliant with the USB3.1 SuperSpeed Transmitter and Receiver Normative Electrical Parameters as defined in the Universal Serial Bus 3.1 Specification, Revision 1.0, July 26, 2013.

5.7 VPP Specifications for One-Time Programmable (OTP) eFuses

This section specifies the operating conditions required for programming the OTP eFuses and is applicable only for High-Security Devices.

表 5-11. Recommended Operating Conditions for OTP eFuse Programming⁽²⁾

over operating free-air temperature range (unless otherwise noted)

PARAMETER	DESCRIPTION	MIN	NOM	MAX	UNIT
VDD_MCU	Supply voltage range for the core domain during OTP operation; OPP NOM (BOOT)	See Section 5.4			V
VPP_CORE	Supply voltage range for the eFuse ROM domain during normal operation	NC			V
	Supply voltage range for the eFuse ROM domain during OTP programming ⁽¹⁾	NC			V
VPP_MCU	Supply voltage range for the eFuse ROM domain during normal operation	NC			V
	Supply voltage range for the eFuse ROM domain during OTP programming ⁽¹⁾	1.71	1.8	1.89	V
I _(VPP_MCU)		100			mA
T _j	Temperature (junction)	0	25	85	°C

(1) Supply voltage range includes DC errors and peak-to-peak noise. TI power management solutions [TLV70718](#) from the TLV707x family meet the supply voltage range needed for VPP_MCU.

(2) NC stands for No Connect.

5.7.1 Hardware Requirements

The following hardware requirements must be met when programming keys in the OTP eFuses:

- The VPP_MCU power supply must be disabled when not programming OTP registers.
- The VPP_MCU power supply must be ramped up after the proper device power-up sequence (for more details, see [Section 5.9.2, Power Supply Sequencing](#)).

5.7.2 Programming Sequence

Programming sequence for OTP eFuses:

- Power on the board per the power-up sequencing. No voltage should be applied on the VPP_MCU terminal during power up and normal operation.
- Load the OTP write software required to program the eFuse (contact your local TI representative for the OTP software package).
- Apply the voltage on the VPP_MCU terminal according to the specification in [表 5-11](#).
- Run the software that programs the OTP registers.
- After validating the content of the OTP registers, remove the voltage from the VPP_MCU terminal.

5.7.3 Impact to Your Hardware Warranty

You accept that e-Fusing the TI Devices with security keys permanently alters them. You acknowledge that the e-Fuse can fail, for example, due to incorrect or aborted program sequence or if you omit a sequence step. Further the TI Device may fail to secure boot if the error code correction check fails for the Production Keys or if the image is not signed and optionally encrypted with the current active Production Keys. These types of situations will render the TI Device inoperable and TI will be unable to confirm whether the TI Devices conformed to their specifications prior to the attempted e-Fuse.

CONSEQUENTLY, TI WILL HAVE NO LIABILITY (WARRANTY OR OTHERWISE) FOR ANY TI DEVICES THAT HAVE BEEN e-FUSED WITH SECURITY KEYS.

5.8 Thermal Resistance Characteristics

This section provides the thermal resistance characteristics used on this device.

For reliability and operability concerns, the maximum junction temperature of the Device has to be at or below the T_J value identified in [Section 5.4, Recommended Operating Conditions](#).

表 5-12. Thermal Resistance Characteristics

It is recommended to perform thermal simulations at the system level with the worst case device power consumption.

NO.	NAME	DESCRIPTION	ACD °C/W ^{(1) (3)}	AIR FLOW (m/s) ⁽²⁾
T1	$R_{\theta JC}$	Junction-to-case	0.2	N/A
T2	$R_{\theta JB}$	Junction-to-board	3.1	N/A
T3	$R_{\theta JA}$	Junction-to-free air	12.8	0
T4		Junction-to-moving air	7.4	1
T5			6.5	2
T6			6	3
T7	Ψ_{JT}	Junction-to-package top	0.1	0
T8			0.1	1
T9			0.1	2
T10			0.1	3
T11	Ψ_{JB}	Junction-to-board	2.9	0
T12			2.4	1
T13			2.3	2
T14			2.3	3

(1) These values are based on a JEDEC defined 2S2P system (with the exception of the Theta JC [$R_{\theta JC}$] value, which is based on a JEDEC defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:

- JESD51-2, *Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions - Forced Convection (Moving Air)*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Packages*

(2) m/s = meters per second.

(3) °C/W = degrees Celsius per watt.

5.9 Timing and Switching Characteristics

NOTE

The Timing Requirements and Switching Characteristics values may change following the silicon characterization result.

NOTE

The default SLEWRATE settings in each pad configuration register must be used to ensure timings, unless specific instructions are given otherwise.

5.9.1 Timing Parameters and Information

The timing parameter symbols used in [Section 5.9](#) are created in accordance with JEDEC Standard 100. To shorten the symbols, some pin names and other related terminologies have been abbreviated in [Table 5-13](#):

Table 5-13. Timing Parameters Subscripts

SYMBOL	PARAMETER
c	Cycle time (period)
d	Delay time
dis	Disable time
en	Enable time
h	Hold time
su	Setup time
START	Start bit
t	Transition time
v	Valid time
w	Pulse duration (width)
X	Unknown, changing, or don't care level
F	Fall time
H	High
L	Low
R	Rise time
V	Valid
IV	Invalid
AE	Active Edge
FE	First Edge
LE	Last Edge
Z	High impedance

5.9.2 Power Supply Sequencing

This section describes the power-up sequence required to ensure proper device operation. The power supply names described in this section comprise a superset of a family of compatible devices. Some members of this family will not include a subset of these power supplies and their associated device modules.

NOTE

All timing requirements and switching characteristics in [Section 5.9.3](#) should be strictly followed unless otherwise specified.

5.9.2.1 Power Supply Slew Rate Requirement

To maintain the safe operating range of the internal ESD protection devices, TI recommends limiting the maximum slew rate of supplies to be less than $1.0E + 5$ V/s. For instance, as shown in [Figure 5-2](#), TI recommends having the supply ramp slew for a 1.8-V supply of more than $18\ \mu\text{s}$.

[Figure 5-2](#) describes the Power Supply Slew Rate Requirement of the device.

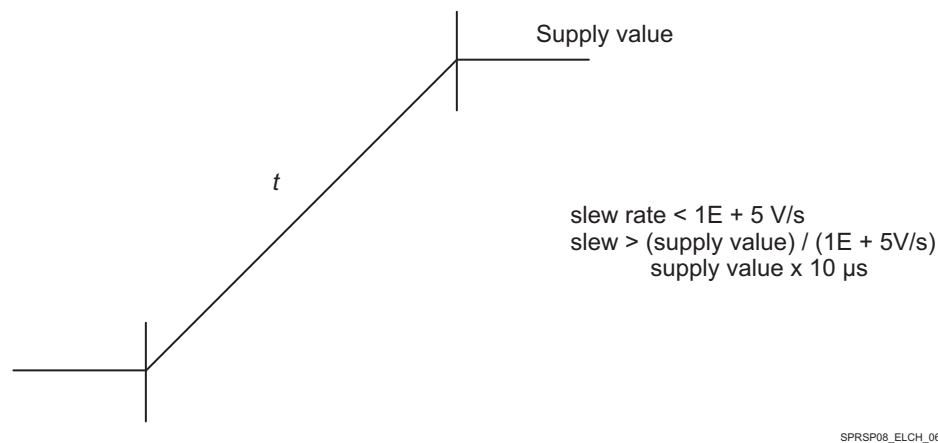


Figure 5-2. Power Supply Slew and Slew Rate

5.9.2.2 Power-Up Sequencing

[Figure 5-3](#) describes the Power-Up Sequencing using On Chip Power-on-reset (POR) of the device.

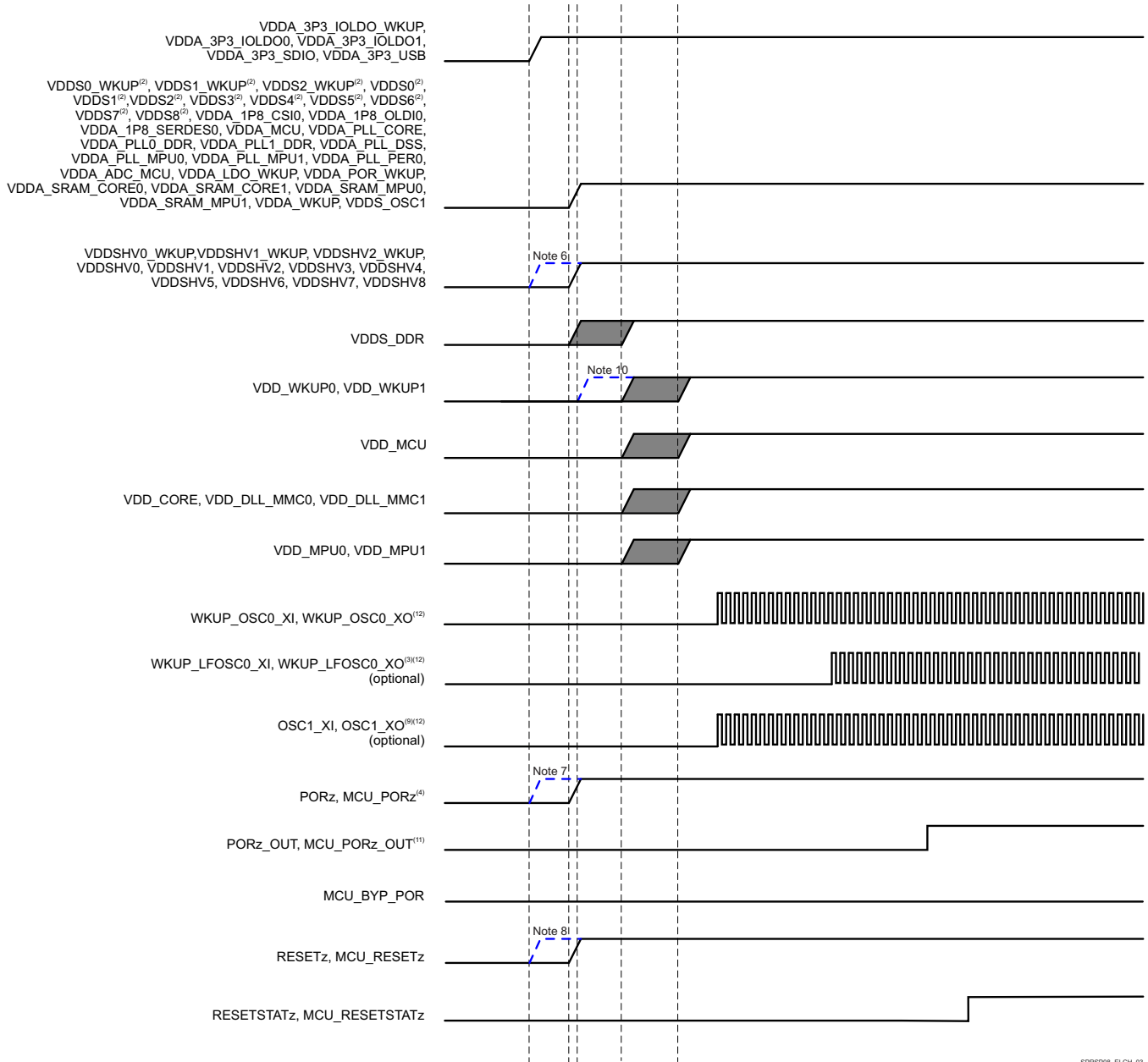


Figure 5-3. Power-Up Sequencing using On Chip Power-on-reset (POR)

- (1) Grey shaded areas are windows where it is valid to ramp the voltage rail.
- (2) The VDDS[2:0]_WKUP, VDDS[8:0] are sourced from the same 1.8 V VDDSHV[2:0]_WKUP, VDDSHV[8:0] supply. If VDDSHV[2:0]_WKUP, VDDSHV[8:0] is configured as 3.3 V, VDDS[2:0]_WKUP, VDDS[8:0] should be sourced from the internal IO bias LDO.
- (3) WKUP_LFOSC0 crystal clock source is enabled by default. For the oscillator start-up time, see [Table 5-18, WKUP_OSC0 Switching Characteristics – Crystal Mode](#). For more information about WKUP_LFOSC0 clock source configuration, refer to device TRM.
- (4) PORz should be pulled to VDDSHV0. MCU_PORz should be pulled to VDDSHV0_WKUP.
- (5) Blue dashed lines are not valid windows but show alternate ramp possibilities based on the associated note.
- (6) If any of the VDDSHV[0-8], VDDSHV[2:0]_WKUP rails are used as 3.3 V only, then these rails must be ramped-up with the 3.3 V power supplies.
- (7) If any of the PORz, MCU_PORz signals are configured at 3.3 V only, then these signals must be ramped-up at the same time with the 3.3 V power supplies.
- (8) If any of the RESETz, MCU_RESETz signals are configured at 3.3 V only, then these signals must be ramped-up at the same time with the 3.3 V power supplies.

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- (9) OSC1 crystal clock sources is enabled by default. For the oscillator start-up time, see [Table 5-22, OSC1 Switching Characteristics – Crystal Mode](#). For more information about OSC1 clock source configuration, refer to device TRM.
- (10) If WKUP LDO is used to power the WKUP domain, connect CAP_VDD_WKUP pin to VDD_WKUP0/1 pin. VDD_WKUP0/1 will start ramping after VDDA_LDO_WKUP reaches a certain threshold. If WKUP LDO is bypassed, connect VDD_WKUP0/1 with VDD_MCU.
- (11) PORz_OUT and MCU_PORz_OUT should be pulled down.
- (12) Refer to the Clock Specifications section for the oscillator start-up time.

Figure 5-4 describes the Power-Up Sequencing using External Power-on-reset (POR), bypassing on-chip POR circuit of the device.

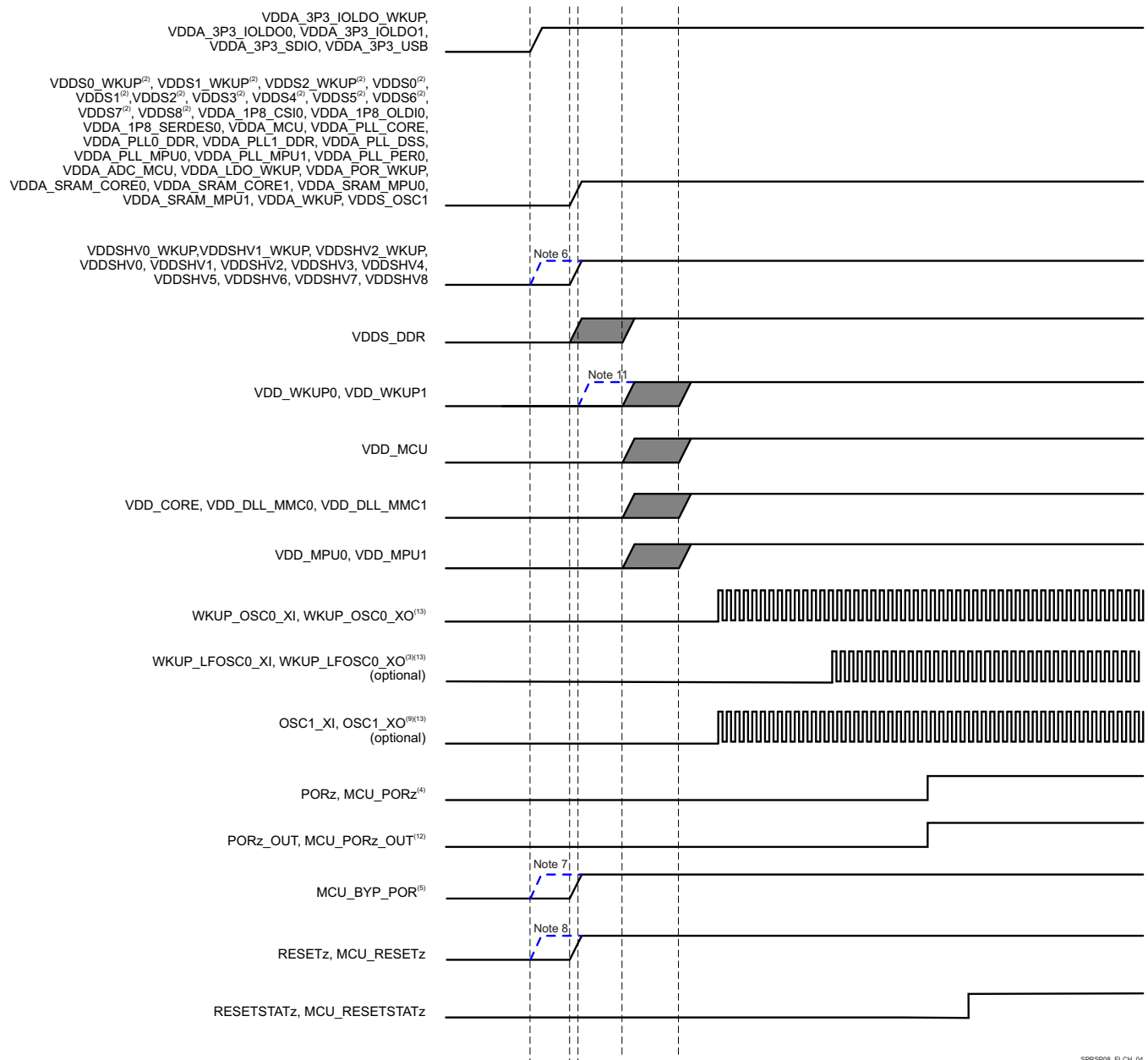


Figure 5-4. Power-Up Sequencing using External Power-on-reset (POR), bypassing on-chip POR circuit

- (1) Grey shaded areas are windows where it is valid to ramp the voltage rail.
- (2) The VDDSD[2:0]_WKUP, VDDSD[8:0] are sourced from the same 1.8 V VDDSHV[2:0]_WKUP, VDDSHV[8:0] supply. If VDDSHV[2:0]_WKUP, VDDSHV[8:0] is configured as 3.3 V, VDDSD[2:0]_WKUP, VDDSD[8:0] should be sourced from the internal IO bias LDO.
- (3) WKUP_LFOSC0 crystal clock source is enabled by default. For the oscillator start-up time, see [Table 5-18, WKUP_OSC0 Switching](#)

Characteristics – Crystal Mode. For more information about WKUP_LFOSC0 clock source configuration, refer to device TRM.

- (4) PORz should be pulled to VDDSHV0. MCU_PORz should be pulled to VDDSHV0_WKUP.
- (5) MCU_BYP_POR should be pulled to VDDSHV0_WKUP.
- (6) If any of the VDDSHV[0-8] rails are used as 3.3 V only, then these rails must be ramped-up with the 3.3 V power supplies.
- (7) If MCU_BYP_POR is configured at 3.3 V only, then this signal must be ramped-up at the same time with the 3.3 V power supplies.
- (8) If any of the RESETz, MCU_RESETz signals are configured at 3.3 V only, then these signals must be ramped-up at the same time with the 3.3 V power supplies.
- (9) OSC1 crystal clock sources is enabled by default. For the oscillator start-up time, see [Table 5-22, OSC1 Switching Characteristics – Crystal Mode](#). For more information about OSC1 clock source configuration, refer to device TRM.
- (10) Blue dashed lines are not valid windows but show alternate ramp possibilities based on the associated note.
- (11) If WKUP LDO is used to power the WKUP domain, connect CAP_VDD_WKUP pin to VDD_WKUP0/1 pin. VDD_WKUP0/1 will start ramping after VDDA_LDO_WKUP reaches a certain threshold. If WKUP LDO is bypassed, connect VDD_WKUP0/1 with VDD_MCU.
- (12) PORz_OUT and MCU_PORz_OUT should be pulled down.
- (13) Refer to the Clock Specifications section for the oscillator start-up time.

5.9.2.3 Power-Down Sequencing

A typical power down sequence is to have the Power-on-Reset asserted, clock shut down, and ramp down all the power supplies sequentially in the exact reverse order of the power-up sequencing. In other words, the power supply that has been ramped up first should be the last one that is ramped down.

For AM654x/AM652x, there are no specific power-down sequencing requirements, except for asserting Power-on-Reset before ramping down the rails while bypassing internal POR.

5.9.3 Reset Timing

5.9.3.1 Reset Electrical Data/Timing

For more details about features and additional description information on the subsystem multiplexing signals, see the corresponding sections within [4.3, Signal Descriptions](#) and [6, Detailed Description](#).

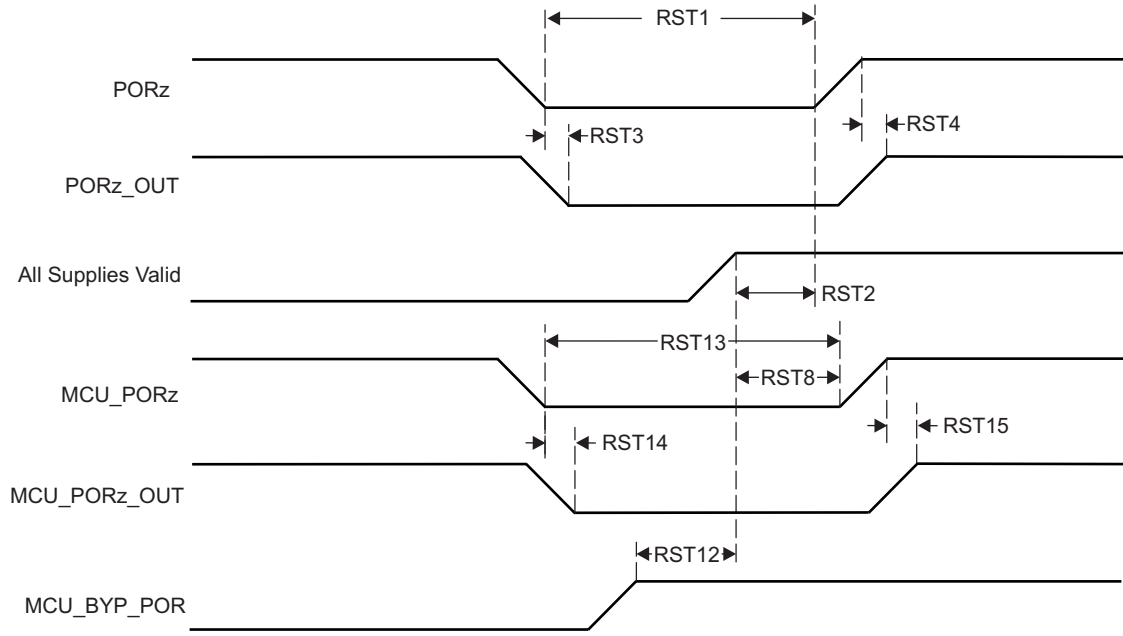
[Table 5-14](#), [Table 5-15](#), [Figure 5-5](#), and [Figure 5-6](#) present the reset timing requirements and switching characteristics.

Table 5-14. Reset Timing Requirements

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PORz Pin					
RST1	$t_{w(PORzL)}$	Pulse Width minimum, PORz low	2000		ns
RST2	$t_{h(SUPPLIES\ VALID - PORz)}$	Hold time, PORz active (low) after all supplies valid	2000000		ns
RESETz Pin					
RST5	$t_{w(RESETzL)}$	Pulse Width minimum, RESETz low	400		ns
MCU_PORz Pin					
RST13	$t_{w(MCU_PORzL)}$	Pulse Width minimum, MCU_PORz	2000		ns
RST8	$t_{h(SUPPLIES\ VALID - MCU_PORz)}$	Hold time, MCU_PORz active (low) after all supplies valid	2000000		ns
MCU_RESETz Pin					
RST9	$t_{w(MCU_RESETzL)}$	Pulse Width minimum, MCU_RESETz	400		ns
MCU_BYP_POR Pin					
RST12	$t_{su(MCU_BYP_POR-MCU_PORz)}$	Setup time, MCU_BYP_POR active (high) before all supplies are valid	1000000		ns

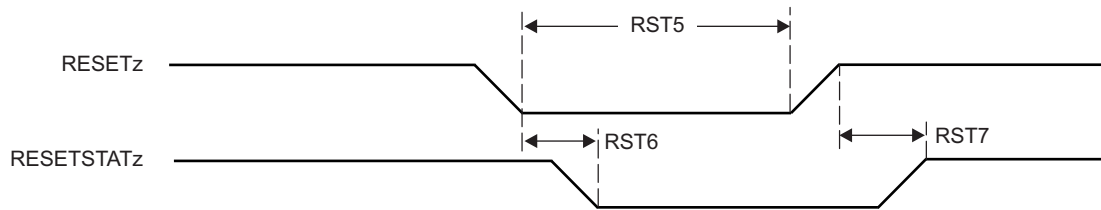
Table 5-15. Reset Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PORz Pin					
RST3	$t_d(PORz-PORz_OUT\ low)$	Delay time, PORz active (low) to PORz_OUT active (low)	0		ns
RST4	$t_d(PORz-PORz_OUT\ high)$	Delay time, PORz inactive (high) to PORz_OUT inactive (high)	0		ns
RESETz Pin					
RST6	$t_d(RESETz-RESETSTATz\ low)$	Delay time, RESETz active (low) to RESETSTATz active (low)	4106		ns
RST7	$t_d(RESETz-RESETSTATz\ high)$	Delay time, RESETz inactive (high) to RESETSTATz inactive (high)	380000		ns
MCU_RESETSTATz Pin					
RST10	$t_d(MCU_RESETz-MCU_RESETSTATz\ low)$	Delay time, MCU_RESETz active (low) to MCU_RESETSTATz active (low)	4106		ns
RST11	$t_d(MCU_RESETz-MCU_RESETSTATz\ high)$	Delay time, MCU_RESETz inactive (high) to MCU_RESETSTATz inactive (high)	289000		ns
MCU_PORz Pin					
RST14	$t_d(MCU_PORz-MCU_PORz_OUT\ low)$	Delay time, MCU_PORz active (low) to MCU_PORz_OUT active (low)	0		ns
RST15	$t_d(MCU_PORz-MCU_PORz_OUT\ high)$	Delay time, MCU_PORz inactive (high) to MCU_PORz_OUT inactive (high)	0		ns



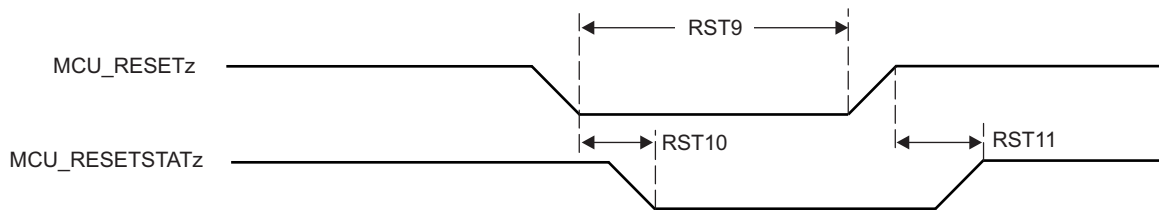
SPRSP08_PORz_Reset_Timing

Figure 5-5. PORz Reset Timing



SPRSP08_RESETz_Timing

Figure 5-6. RESETz and RESETSTATz Timing



SPRSP08_MCU_RESETz_Timing

Figure 5-7. MCU_RESETz and MCU_RESETSTATz Timing

Table 5-16 and Figure 5-8 present the boot configuration timing requirements.

Table 5-16. Boot Configuration Timing Requirements

NO.	PARAMETER		MIN	MAX	UNIT
BC1	$t_{su}(BOOTMODE-PORz)$	Setup time, All Bootmode pins active to PORz inactive (high)	2000		ns
BC2	$t_h(PORz - BOOTMODE)$	Hold time, All Bootmode pins active after PORz inactive (high)	0		ns
BC3	$t_{su}(MCU_BOOTMODE-MCU_PORz)$	Setup time, All Bootmode pins active to MCU_PORz inactive (high)	2000		ns

Table 5-16. Boot Configuration Timing Requirements (continued)

NO.	PARAMETER		MIN	MAX	UNIT
BC4	$t_{h(MCU_PORz - MCU_BOOTMODE)}$	Hold time, All Bootmode pins active after MCU_PORz inactive (high)	0		ns

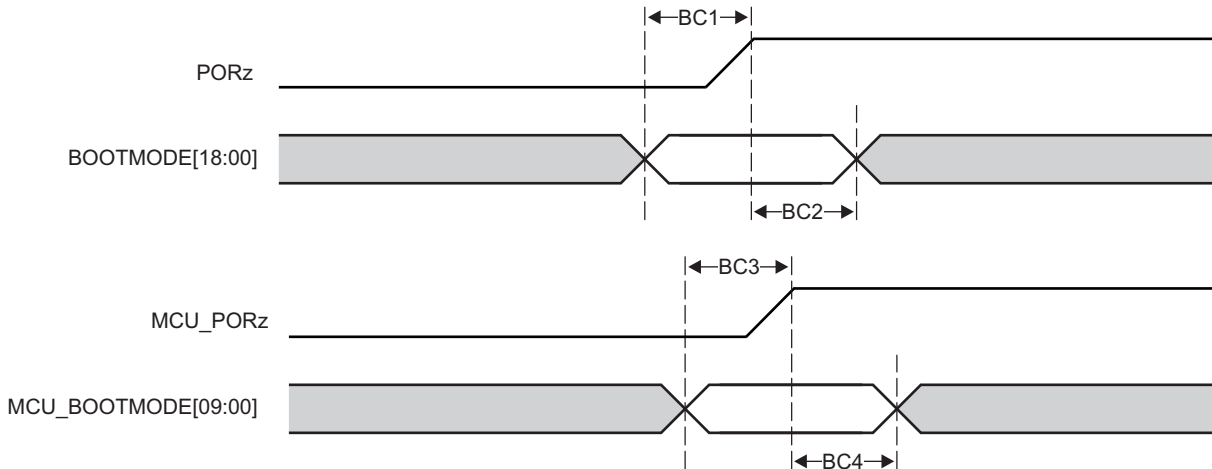


Figure 5-8. Boot Configuration Timing

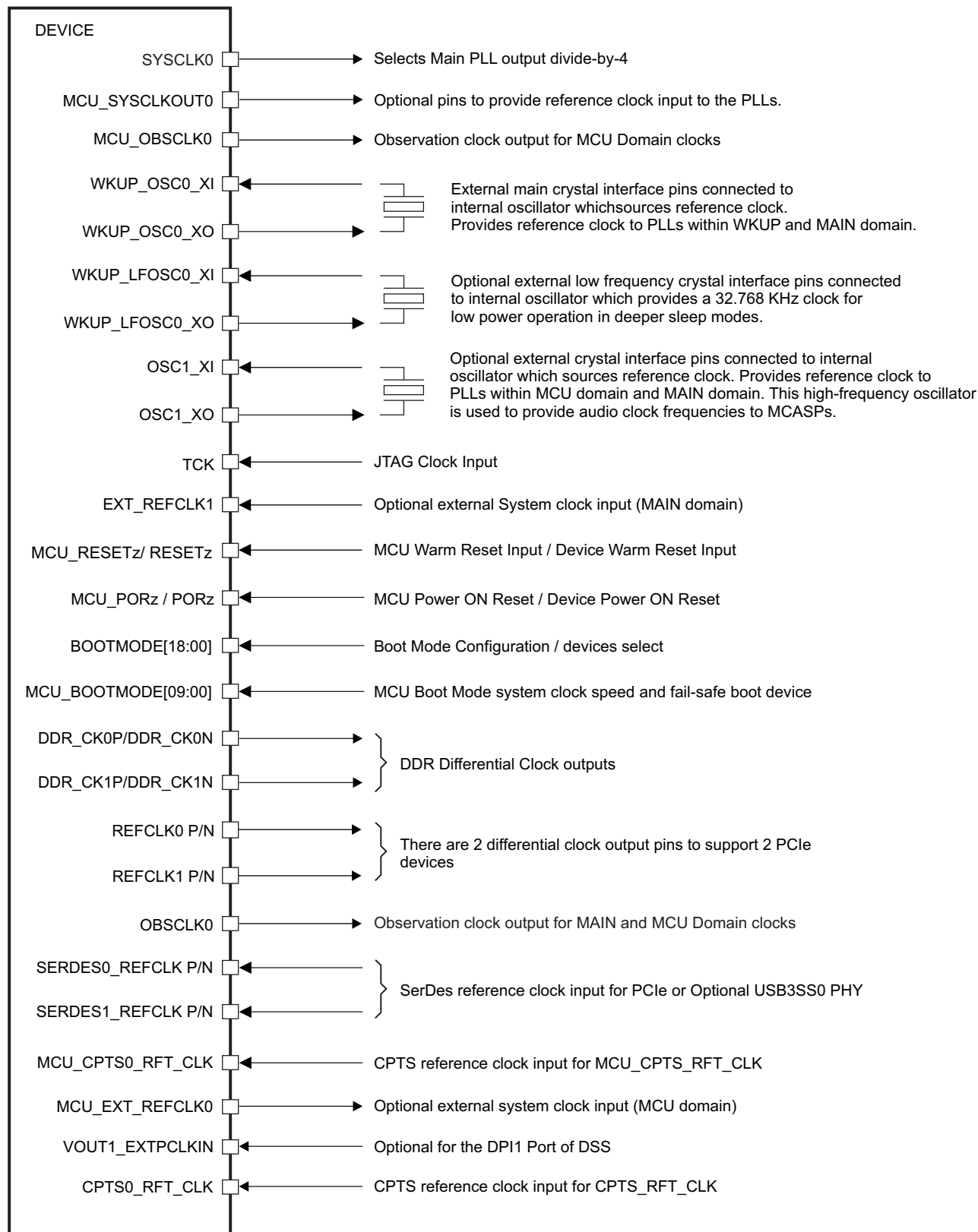
5.9.4 Clock Specifications

5.9.4.1 Input Clocks / Oscillators

Various external clock inputs are needed to drive the device. Summary of these input clock signals are:

- OSC1_XO/OSC1_XI — External main crystal interface pins connected to internal oscillator which sources reference clock and provides reference clock to PLLs within MAIN domain. Also, for audio applications, high-frequency oscillator 0 is used to provide audio clock frequencies to MCASPs.
- WKUP_OSC0_XO/WKUP_OSC0_XI — External main crystal interface pins connected to internal oscillator which sources reference clock and provides reference clock to PLLs within MCU domain and MAIN domain.
- WKUP_LFOSC_XO/WKUP_LFOSC_XI — External main crystal interface pins connected to internal oscillator which sources reference clock provides a clock for low power operation in deeper sleep modes.
- MCU_EXT_REFCLK0 — Optional external system clock input (MCU domain).
- EXT_REFCLK1— Optional external System clock input (MAIN domain). Optionally PLL2 (PER1) and MCASP can be sourced by EXT_REFCLK1 (sourced externally).
- SERDES0_REFCLK P/N and SERDES1_REFCLK P/N — SerDes reference clock for PCIe or Optional USB3.0 PHY.
- MCU_CPTS0_RFT_CLK — CPTS reference clock inputs for MCU_CPTS0_RFT_CLK.
- CPTS_RFT0_CLK — CPTS reference clock inputs for CPTS0_RFT_CLK.
- VOUT1_EXTPLCKIN — Optional for the DPI1 Port of DSS.
- REFCLK0 P/N and REFCLK1 P/N — There are 2 differential clock output pins to support 2 PCIe devices.

Figure 5-9 shows the external input clock sources to peripherals.



SPRSP08_CLOCK_01

Figure 5-9. Input Clocks Interface

For more information about Input clock interfaces, see section *Clocking* in the device TRM.

5.9.4.1.1 WKUP_OSC0 Internal Oscillator Clock Source

Figure 5-10 shows the recommended crystal circuit. It is recommended that preproduction printed-circuit board (PCB) designs include the two optional resistors R_{bias} and R_d in case they are required for proper oscillator operation when combined with production crystal circuit components. In most cases, R_{bias} is not required and R_d is a 0-Ω resistor. These resistors may be removed from production PCB designs after evaluating oscillator performance with production crystal circuit components installed on preproduction PCBs.

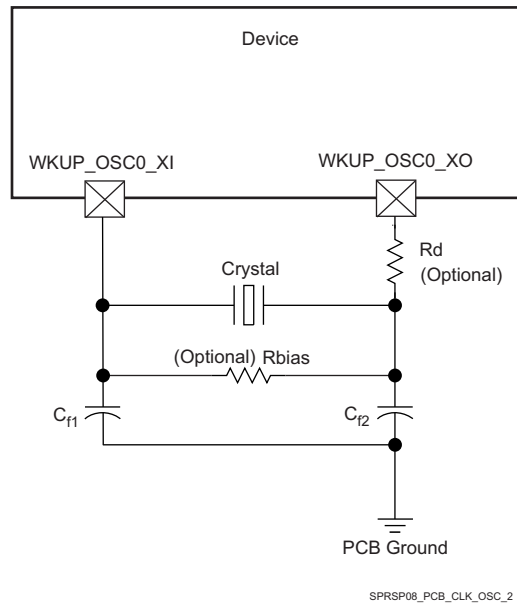


Figure 5-10. WKUP_OSC0 Crystal Implementation

NOTE

The load capacitors, C_{f1} and C_{f2} in Figure 5-11, should be chosen such that the below equation is satisfied. C_L in the equation is the load specified by the crystal manufacturer. All discrete components used to implement the oscillator circuit should be placed as close as possible to the associated oscillator WKUP_OSC0_XI, WKUP_OSC0_XO, and VSS pins.

$$C_L = \frac{C_{f1} C_{f2}}{(C_{f1} + C_{f2})}$$

SPRSP08_CLOCK_03

Figure 5-11. Load Capacitance Equation

The crystal must be in the fundamental mode of operation and parallel resonant. Table 5-17 summarizes the required electrical constraints.

Table 5-17. WKUP_OSC0 Crystal Electrical Characteristics

NAME	DESCRIPTION			MIN	TYP	MAX	UNIT	
f _p	Parallel resonance crystal frequency			19.2, 20, 24, 25, 26, 27			MHz	
C _{f1}	C _{f1} load capacitance for crystal parallel resonance with C _{f1} = C _{f2}			12			24	pF
C _{f2}	C _{f2} load capacitance for crystal parallel resonance with C _{f1} = C _{f2}			12			24	pF
ESR(C _{f1} ,C _{f2})	Crystal ESR			100			Ω	
C _O	Crystal shunt capacitance	ESR = 30 Ω ESR = 40 Ω	19.2 MHz, 20 MHz, 24 MHz, 25 MHz, 26 MHz, 27 MHz	7			pF	
			19.2 MHz, 20 MHz	7			pF	
		ESR = 50 Ω	24 MHz, 25 MHz, 26 MHz, 27 MHz	5			pF	
			19.2 MHz, 20 MHz	7			pF	
		ESR = 60 Ω	24 MHz, 25 MHz, 26 MHz, 27 MHz	Not Supported			-	
			19.2 MHz, 20 MHz	5			pF	
		ESR = 80 Ω	24 MHz, 25 MHz, 26 MHz, 27 MHz	Not Supported			-	
			19.2 MHz, 20 MHz	3			pF	
ESR = 100 Ω	24 MHz, 25 MHz, 26 MHz, 27 MHz	Not Supported			-			
	L _M			Crystal motional inductance for f _p = 20 MHz			10.16	mH
C _M			Crystal motional capacitance			3.42	fF	
f _{J(WKUP_OSC0_XI)}	Frequency accuracy, WKUP_OSC0_XI		Ethernet RGMII and RMII not used	±100			ppm	
			Ethernet RGMII and RMII using derived clock	±50				

When selecting a crystal, the system design must consider the temperature and aging characteristics of a based on the worst case environment and expected life expectancy of the system.

Table 5-18 details the switching characteristics of the oscillator and the requirements of the input clock.

Table 5-18. WKUP_OSC0 Switching Characteristics – Crystal Mode

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
f_p	Oscillation frequency	19.2, 20, 24, 25, 26, 27			MHz
t_{SX}	Start-up time	$2^{(1)}$			ms

- (1) In order to meet the start-up time defined in this table, the crystal needs to be selected according to the following equation:

$$T_{su} = K \cdot L_m / (R_o - ESR) + \Delta t$$

where L_m is crystal motional inductance, R_o is the negative resistance of amplifier, ESR is the crystal Effective series resistance and K is a constant which represents the initial conditions. Δt is the time amplifier takes to reach its bias point after power down is released.

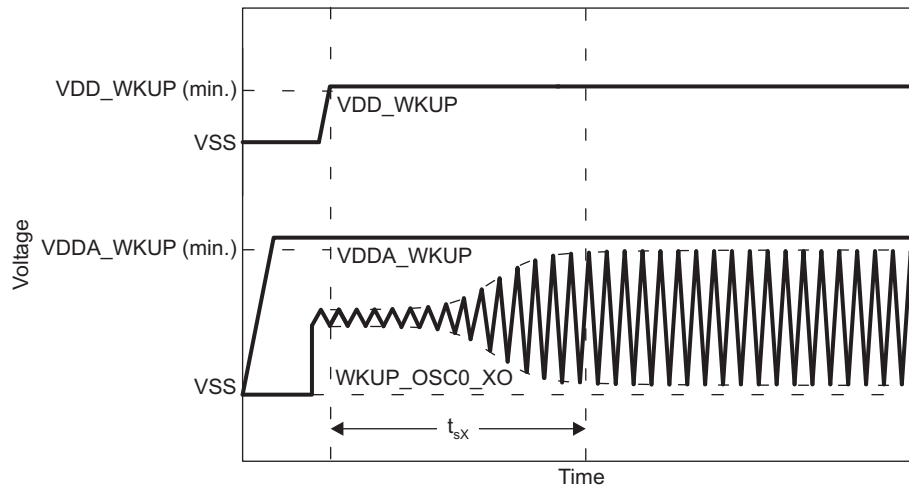


Figure 5-12. WKUP_OSC0 Start-up Time

5.9.4.1.2 WKUP_OSC0 LVCMOS Digital Clock Source

Figure 5-13 shows the recommended oscillator connections when WKUP_OSC0 is connected to an LVCMOS square-wave digital clock source. The 1.8-V LVCMOS-Compatible clock source is connected to the WKUP_OSC0_XI pin. In this mode of operation, the WKUP_OSC0_XO pin is left unconnected and should not be used to source any external components.

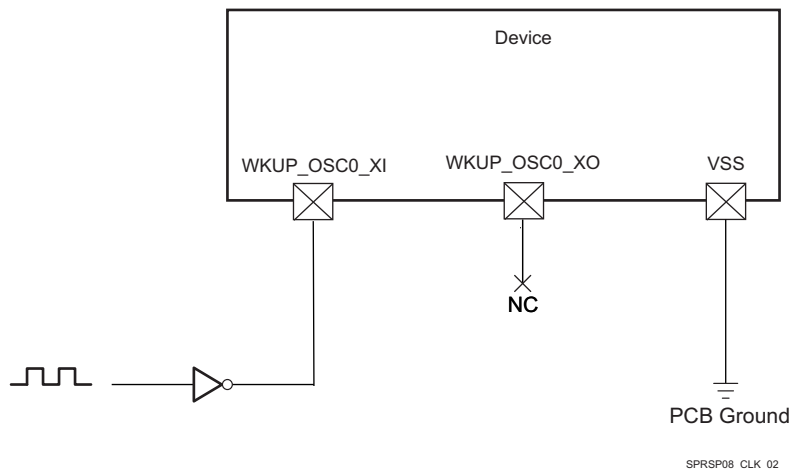


Figure 5-13. 1.8-V LVCMOS-Compatible Clock Input

Table 5-19 summarizes the WKUP_OSC0 input clock electrical characteristics

Table 5-19. WKUP_OSC0 Switching Characteristics – Crystal Mode

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
f	Frequency		19.2, 20, 24, 25, 26, 27		MHz
C _{IN}	Input capacitance	2.184	2.384	2.584	pF
I _{IN}	Input current (3.3V mode)	4	6	10	μA

Table 5-20 details the WKUP_OSC0 input clock timing requirements.

Table 5-20. WKUP_OSC0 Input Clock Timing Requirements

NAME	DESCRIPTION		MIN	TYP	MAX	UNIT
CK0	1 / $t_c(\text{WKUP_OSC0_XI})$	Frequency, WKUP_OSC0_XI	19.2, 20, 24, 25, 26, 27			MHz
CK1	$t_w(\text{WKUP_OSC0_XI})$	Pulse duration, WKUP_OSC0_XI low or high	$0.45 \times t_c(\text{WKUP_OSC0_XI})$		$0.55 \times t_c(\text{WKUP_OSC0_XI})$	ns
	$t_j(\text{WKUP_OSC0_XI})$	Period jitter, WKUP_OSC0_XI			$0.01 \times t_c(\text{WKUP_OSC0_XI})$	ns
	$t_R(\text{WKUP_OSC0_XI})$	Rise time, WKUP_OSC0_XI			5	ns
	$t_F(\text{WKUP_OSC0_XI})$	Fall time, WKUP_OSC0_XI			5	ns
	$t_j(\text{WKUP_OSC0_XI})$	Frequency accuracy, WKUP_OSC0_XI	Ethernet RGMII and RMII not used		±100	ppm
			Ethernet RGMII and RMII using derived clock		±50	

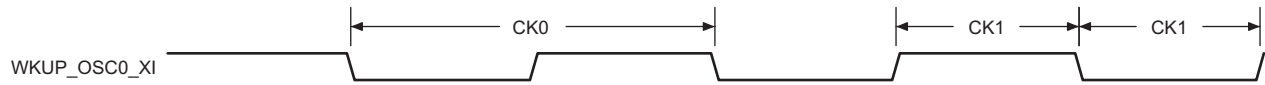


Figure 5-14. WKUP_OSC0_XI Input Clock

5.9.4.1.3 Auxiliary OSC1 Internal Oscillator Clock Source

Figure 5-15 shows the recommended crystal circuit. It is recommended that preproduction printed-circuit board (PCB) designs include the two optional resistors R_{bias} and R_d in case they are required for proper oscillator operation when combined with production crystal circuit components. In most cases, R_{bias} is not required and R_d is a 0-Ω resistor. These resistors may be removed from production PCB designs after evaluating oscillator performance with production crystal circuit components installed on preproduction PCBs.

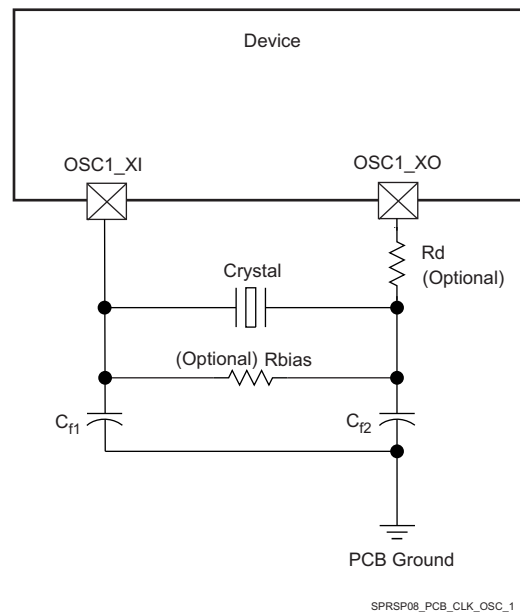


Figure 5-15. OSC1 Crystal Implementation

NOTE

The load capacitors, C_{f1} and C_{f2} in [Figure 5-16](#), should be chosen such that the below equation is satisfied. C_L in the equation is the load specified by the crystal manufacturer. All discrete components used to implement the oscillator circuit should be placed as close as possible to the associated oscillator OSC1_XI, OSC1_XO, and VSS pins.

$$C_L = \frac{C_{f1} C_{f2}}{(C_{f1} + C_{f2})}$$

SPR002, CLOCK_01

Figure 5-16. Load Capacitance Equation

The crystal must be in the fundamental mode of operation and parallel resonant. [Table 5-21](#) summarizes the required electrical constraints.

Table 5-21. OSC1 Crystal Electrical Characteristics

NAME	DESCRIPTION		MIN	TYP	MAX	UNIT
f_p	Parallel resonance crystal frequency		19.2, 20, 24, 25, 26, 27			MHz
C_{f1}	C_{f1} load capacitance for crystal parallel resonance with $C_{f1} = C_{f2}$		12			pF
C_{f2}	C_{f2} load capacitance for crystal parallel resonance with $C_{f1} = C_{f2}$		12			pF
ESR(C_{f1}, C_{f2})	Crystal ESR		100			Ω
C_O	Crystal shunt capacitance	ESR = 30 Ω ESR = 40 Ω	19.2 MHz, 20 MHz, 24 MHz, 25 MHz, 26 MHz, 27 MHz		7	pF
		ESR = 50 Ω	19.2 MHz, 20 MHz		7	pF
			24 MHz, 25 MHz, 26 MHz, 27 MHz		5	pF
		ESR = 60 Ω	19.2 MHz, 20 MHz		7	pF
			24 MHz, 25 MHz, 26 MHz, 27 MHz		Not Supported	-
		ESR = 80 Ω	19.2 MHz, 20 MHz		5	pF
			24 MHz, 25 MHz, 26 MHz, 27 MHz		Not Supported	-
$f_{f(OSC1_XI)}$	Frequency accuracy, OSC1_XI	Ethernet RGMII and RMII not used			± 100	ppm
		Ethernet RGMII and RMII using derived clock			± 50	
L_M	Crystal motional inductance for $f_p = 20$ MHz		10.16			mH
C_M	Crystal motional capacitance		3.42			fF

When selecting a crystal, the system design must consider the temperature and aging characteristics of a based on the worst case environment and expected life expectancy of the system.

[Table 5-22](#) details the switching characteristics of the oscillator and the requirements of the input clock.

Table 5-22. OSC1 Switching Characteristics – Crystal Mode

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
f_p	Oscillation frequency	19.2, 20, 24, 25, 26, 27			MHz
t_{sX}	Start-up time	2 ⁽¹⁾			ms

- (1) In order to meet the start-up time defined in this table, the crystal needs to be selected according to the following equation:

$$T_{su} = K \cdot L_m / (R_o - ESR) + \Delta t$$

where L_m is crystal motional inductance, R_o is the negative resistance of amplifier, ESR is the crystal Effective series resistance and K is a constant which represents the initial conditions. Δt is the time amplifier takes to reach its bias point after power down is released.

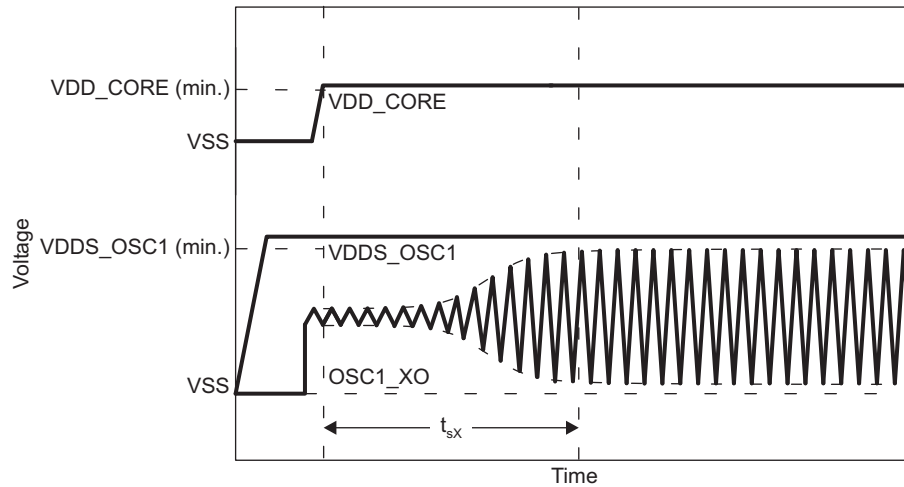


Figure 5-17. OSC1 Start-up Time

5.9.4.1.4 Auxiliary OSC1 LVCMOS Digital Clock Source

Figure 5-18 shows the recommended oscillator connections when OSC1 is connected to an LVCMOS square-wave digital clock source. The 1.8-V LVCMOS-Compatible clock source is connected to the OSC1_XI pin. In this mode of operation, the OSC1_XO pin is left unconnected and should not be used to source any external components.

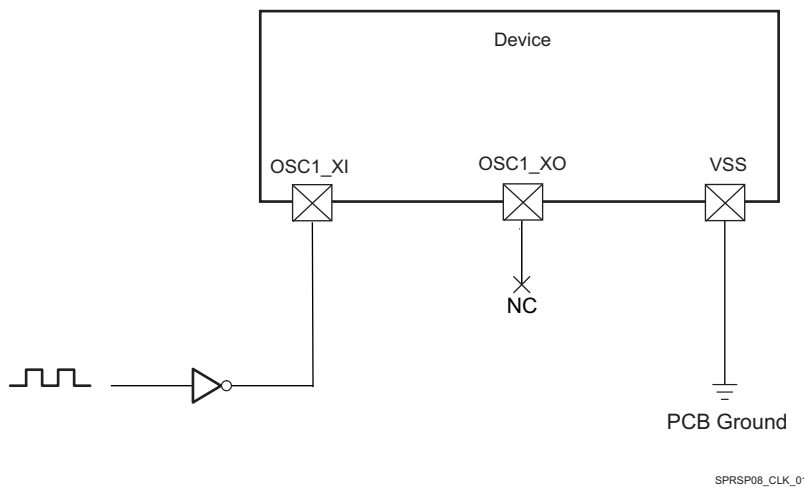


Figure 5-18. 1.8-V LVCMOS-Compatible Clock Input

Table 5-23 summarizes the OSC1 input clock electrical characteristics.

Table 5-23. OSC1 Switching Characteristics – Crystal Mode

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
f	Frequency		19.2, 20, 24, 25, 26, 27		MHz
C _{IN}	Input capacitance	2.184	2.384	2.584	pF
I _{IN}	Input current (3.3V mode)	4	6	10	μA

Table 5-24 details the OSC1 input clock timing requirements.

Table 5-24. OSC1 Input Clock Timing Requirements

NAME	DESCRIPTION		MIN	TYP	MAX	UNIT
CK0	$1 / t_{c(OSC1_XI)}$	Frequency, OSC1_XI	19.2, 20, 24, 25, 26, 27			MHz
CK1	$t_{w(OSC1_XI)}$	Pulse duration, OSC1_XI low or high	$0.45 \times t_{c(OSC1_XI)}$		$0.55 \times t_{c(OSC1_XI)}$	ns
	$t_{j(OSC1_XI)}$	Period jitter, OSC1_XI			$0.01 \times t_{c(OSC1_XI)}$	ns
	$t_{R(OSC1_XI)}$	Rise time, OSC1_XI			5	ns
	$t_{F(OSC1_XI)}$	Fall time, OSC1_XI			5	ns
	$t_{j(OSC1_XI)}$	Frequency accuracy, OSC1_XI	Ethernet RGMII and RMII not used		± 100	ppm
			Ethernet RGMII and RMII using derived clock		± 50	

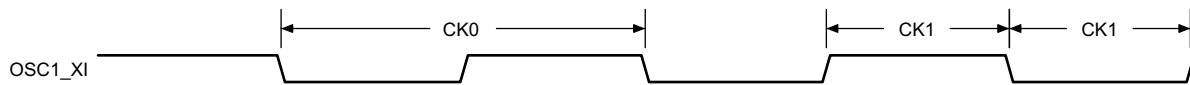


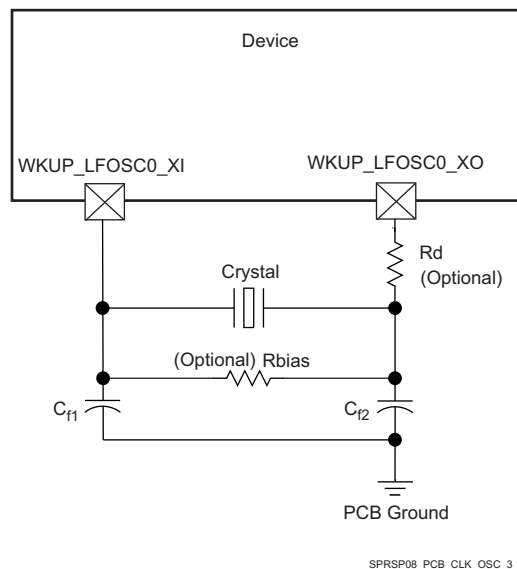
Figure 5-19. OSC1_XI Input Clock

5.9.4.1.5 Auxiliary OSC1 Not Used

For more Information see 4.5, *Connections for Unused Pins*.

5.9.4.1.6 WKUP_LFOSC0 Internal Oscillator Clock Source

Figure 5-20 shows the recommended crystal circuit. It is recommended that preproduction printed-circuit board (PCB) designs include the two optional resistors R_{bias} and R_d in case they are required for proper oscillator operation when combined with production crystal circuit components. In most cases, R_{bias} is not required and R_d is a 0 ohm resistor. These resistors may be removed from production PCB designs after evaluating oscillator performance with production crystal circuit components installed on preproduction PCBs.



SPRSP08_PCB_CLK_OSC_3

Figure 5-20. WKUP_LFOSC0 Crystal Implementation

NOTE

The load capacitors, C_{f1} and C_{f2} in [Figure 5-21](#), should be chosen such that the below equation is satisfied. C_L in the equation is the load specified by the crystal manufacturer. All discrete components used to implement the oscillator circuit should be placed as close as possible to the associated oscillator WKUP_LFOSC0_XI, WKUP_LFOSC0_XO, and VSS pins.

$$C_L = \frac{C_{f1} C_{f2}}{(C_{f1} + C_{f2})}$$

SPRSH02, CLOCK_03

Figure 5-21. Load Capacitance Equation

The crystal must be in the fundamental mode of operation and parallel resonant. [Table 5-25](#) summarizes the required electrical constraints

Table 5-25. WKUP_LFOSC0 Crystal Electrical Characteristics

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
f_p	Parallel resonance crystal frequency		32768		Hz
C_{f1}	C_{f1} load capacitance for crystal parallel resonance with $C_{f1} = C_{f2}$	12		24	pF
C_{f2}	C_{f2} load capacitance for crystal parallel resonance with $C_{f1} = C_{f2}$	12		24	pF
C_{shunt}	Shunt capacitance			TBD	pF
ESR	Crystal effective series resistance			TBD	kΩ

When selecting a crystal, the system design must consider the temperature and aging characteristics of a based on the worst case environment and expected life expectancy of the system.

[Table 5-26](#) details the switching characteristics of the oscillator and the requirements of the input clock.

Table 5-26. WKUP_LFOSC0 Switching Characteristics – Crystal Mode

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
f_{xtal}	Oscillation frequency		32768		Hz
t_{sx}	Start-up time			(1)	s

- (1) In order to meet the start-up time defined in this table, the crystal needs to be selected according to the following equation:

$$T_{SU} = K * L_m / (R_O - ESR) + \Delta t$$

where L_m is crystal motional inductance, R_O is the negative resistance of amplifier, ESR is the crystal Effective series resistance and K is a constant which represents the initial conditions. Δt is the time amplifier takes to reach its bias point after power down is released.

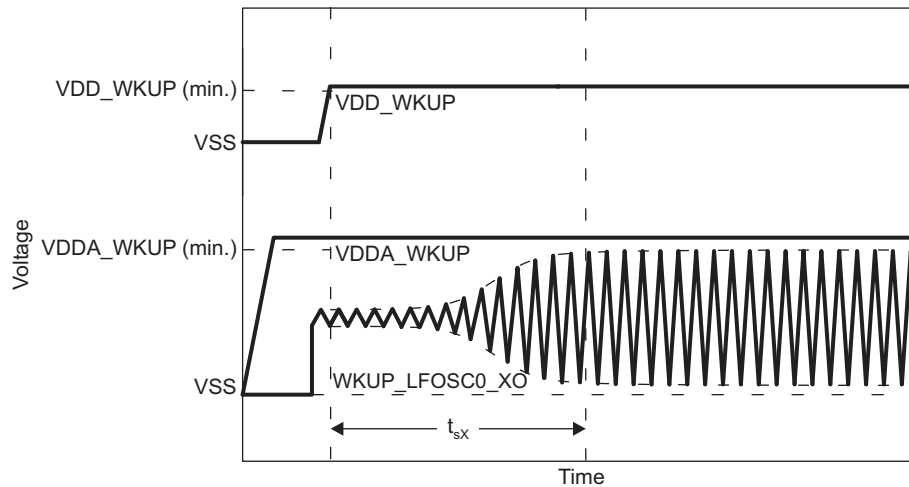


Figure 5-22. WKUP_LFOSC0 Start-up Time

5.9.4.1.7 WKUP_LFOSC0 Not Used

For more Information see [4.5, Connections for Unused Pins](#).

5.9.4.2 Output Clocks

The device provides several system clock outputs. Summary of these output clocks are as follows:

- **MCU_SYSCCLKOUT0**
 - SYSCCLK0 of WKUP_PLLCTRL0 is divided by 4 and then sent out of the device as a LVCMOS clock signal (MCU_SYSCCLKOUT0). This signal can be used to test if the main chip clock is functioning or not.
- **MCU_OBSCLK0**
 - On the clock output MCU_OBSCLK0, oscillators and PLLs clocks can be observed for tests and debug.
- **SYSCCLKOUT0**
 - SYSCCLK0 from the MAIN_PLL controller is divided by 4 and then sent out of the device as a LVCMOS clock signal (SYSCCLKOUT0). This signal can be used to test if the main chip clock is functioning or not.
- **OBSCLK0**
 - On the clock output OBSCLK0, oscillators and PLLs clocks can be observed for tests and debug.

5.9.4.3 PLLs

Power is supplied to the PLL by internal regulators that derive power from the off-chip power-supply.

There are total nine Phase Locked Loops (PLLs) in the device:

- MCU_PLL0 (MCU PLL) with WKUP_PLL_CTRL0: The MCU PLL — which is used to drive the switch fabrics, accelerators, and a majority of the peripheral clocks — requires a PLL controller to manage the various clock divisions, gating, and synchronization in WKUP domain and MCU domain.
- MCU_PLL1 (CPSW PLL): The MCU_PLL1, which is used to drive the CPSW.
- PLL0 (MAIN PLL) with PLL_CTRL0: The Main PLL — which is used to drive the switch fabrics, accelerators, and a majority of the peripheral clocks — requires a PLL controller to manage the various clock divisions, gating, and synchronization in MAIN domain.
- PLL1 (PER0 PLL): The PER0 PLL, which is used to drive the Peripherals in MAIN Domain.
- PLL2 (PER1 PLL): The PER1 PLL, which is used to drive the PRU_ICSSG.
- PLL3 (DDR PLL): The DDR PLL is used to drive the DDR PHY for the DDRSS.
- PLL4 (DSS PLL): The DSS PLL, which is used to drive the Display Subsystem.
- PLL6 (ARM0 PLL): The ARM0 PLL, which is used to drive the ARM0.
- PLL7 (ARM1 PLL): The ARM1 PLL, which is used to drive the ARM1.

Most of the Device is driven by the output from the main PLL except the following items:

- Arm subsystem has its own dedicated PLL.
- MCU subsystem has its own dedicated PLL
- EMIF DDR subsystem has its own dedicated PLL to drive DDR PHY and DDRSS.
- PRU_ICSSG has clocks sourced from several PLLs:
 - PER0 PLL to generate UART clock,
 - PER1 PLL to generate Core clock,
 - MAIN PLL to generate Industrial Ethernet Peripheral clock,
 - CPSW PLL to generate Ethernet clocks.
- DSS has its own dedicated PLL, to generate Pixel Clock.
- PCIESS require separate reference clocks to drive SERDES PHYs.

NOTE

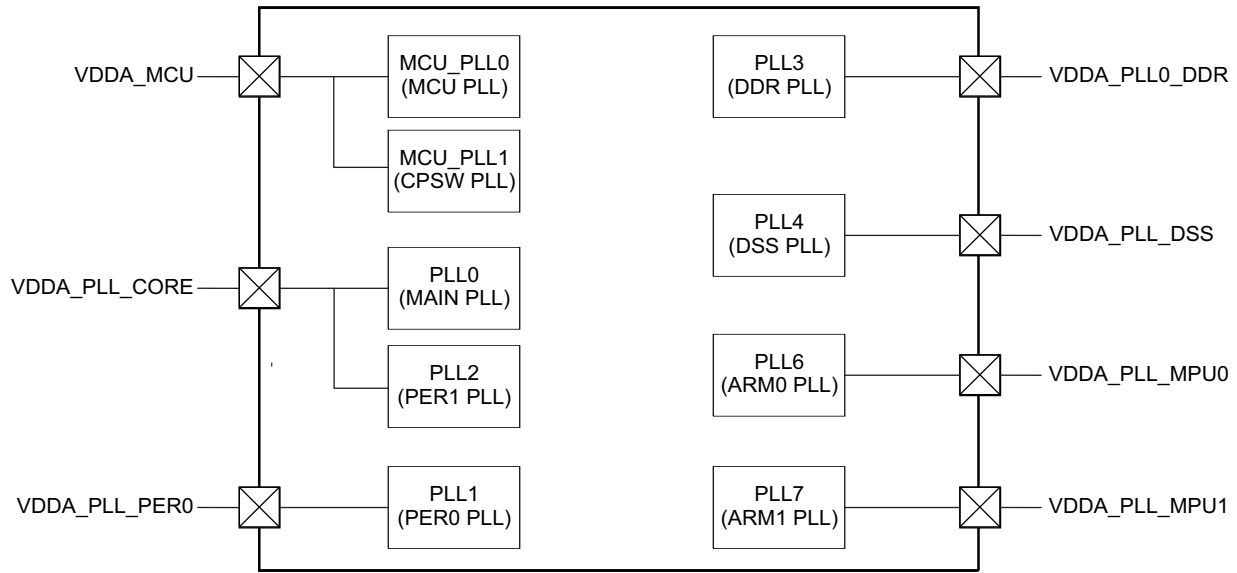
For more information, see:

- *Device Configuration / Clocking / PLLs* section of the device TRM
- *Peripherals / Display Subsystem Overview* section of the device TRM
- *Programmable Real-Time Unit Subsystem and Industrial Communication Subsystem - Gigabit (PRU_ICSSG)* section of the device TRM

NOTE

The input reference clock (OSC1_XI/OSC1_XO) are specified and the lock time is ensured by the PLL controller, as documented in the *Device Configuration* chapter of the device TRM.

Figure 5-23 shows the power supply connectivity implemented in the device.



SPRSP08_PLL_PWR_01

Figure 5-23. PLL Power Supply Connectivity

5.9.4.4 Recommended Clock and Control Signal Transition Behavior

All clocks and strobe signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner. Monotonic transitions are more easily ensured with faster switching signals. Slower input transitions are more susceptible to glitches due to noise, and special care must be taken for slow input clocks.

5.9.4.5 Interface Clock Specifications

5.9.4.5.1 Interface Clock Terminology

The interface clock is used at the system level to sequence the data and to control transfers accordingly with the interface protocol.

5.9.4.5.2 Interface Clock Frequency

The two interface clock characteristics are:

- The maximum clock frequency
- The maximum operating frequency

The interface clock frequency documented here is the maximum clock frequency, which corresponds to the maximum frequency programmable on this output clock. This frequency defines the maximum limit supported by the Device IC and does not take into account any system consideration (PCB, peripherals).

The system designer must take into account these system considerations and the Device IC timing characteristics to properly define the maximum operating frequency that corresponds to the maximum frequency supported to transfer the data on this interface.

5.9.5 Peripherals

5.9.5.1 VIN

表 5-27, 图 5-24, and 图 5-25 present timing requirements for LVDSRX interface.

表 5-27. Timing Requirements for LVDSRX ⁽¹⁾

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
V1	$t_c(\text{PCLK})$	Cycle time, VIN0_PCLK	5.76 ⁽¹⁾		ns
V2	$t_w(\text{PCLKH})$	Pulse duration, VIN0_PCLK high	$0.45 \times P$ ⁽²⁾		ns
V3	$t_w(\text{PCLKL})$	Pulse duration, VIN0_PCLK low	$0.45 \times P$ ⁽²⁾		ns
V4	$t_{su}(\text{PCLK-CTL/DATA})$	Input setup time, control (VIN0_HD, VIN0_VD) and data (VIN0_DATA[15:0]) valid to VIN0_PCLK transition	2.38		ns
V5	$t_h(\text{CTL/DAT-PCLK})$	Input hold time, control (VIN0_HD, VIN0_VD) valid to VIN0_PCLK transition	-0.05		ns

(1) For maximum frequency of 165 MHz

(2) P = VIN0_PCLK period

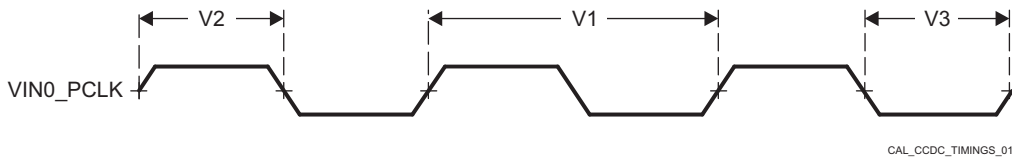


图 5-24. LVDSRX Input Clock Signal

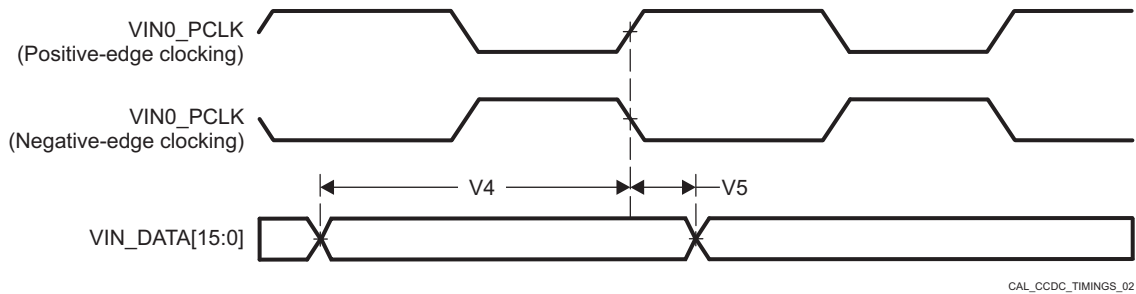


图 5-25. LVDSRX Input Timings

5.9.5.2 CPSW2G

For more details about features and additional description information on the device Gigabit Ethernet MAC, see the corresponding sections within 4.3, *Signal Descriptions* and 6, *Detailed Description*.

5.9.5.2.1 CPSW2G MDIO Interface Timings

表 5-28, 表 5-29, and 图 5-26 present timing requirements for MDIO.

表 5-28. Timing Requirements for MDIO Input

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
MDIO1	$t_{su}(\text{MDIO_MDC})$	Setup time, MDIO_DATA valid before MDIO_CLK high	90		ns
MDIO2	$t_h(\text{MDIO_MDC})$	Hold time, MDIO_DATA valid after MDIO_CLK high	0		ns

表 5-29. Switching Characteristics Over Recommended Operating Conditions for MDIO Output

NO.	PARAMETER		MIN	MAX	UNIT
MDIO3	$t_{c(MDC)}$	Cycle time, MDIO_CLK	400		ns
MDIO4	$t_{w(MDCH)}$	Pulse Duration, MDIO_CLK high	160		ns
MDIO5	$t_{w(MDCL)}$	Pulse Duration, MDIO_CLK low	160		ns
MDIO6	$t_{t(MDC)}$	Transition time, MDIO_CLK		5	ns
MDIO7	$t_{d(MDC_MDIO)}$	Delay time, MDIO_CLK low to MDIO_DATA valid	-150	150	ns

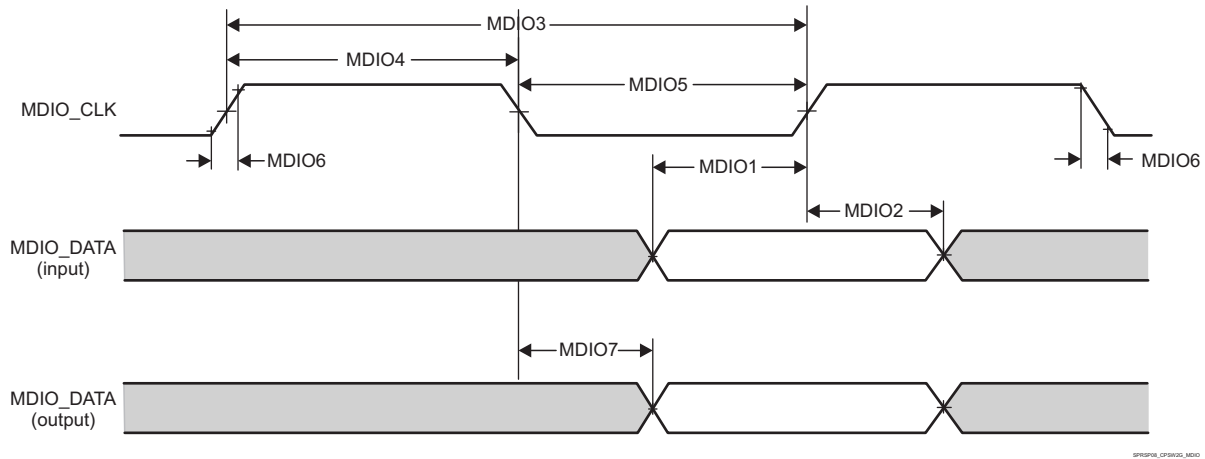


图 5-26. CPSW2G MDIO Diagrams Receive and Transmit

5.9.5.2.2 CPSW2G RMII Timings

表 5-30, 表 5-31, 图 5-27, and 图 5-28 present timing requirements for CPSW2G RMII receive.

表 5-30. Timing Requirements for RMII[x]_REFCLK - RMII Mode

NO.	PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
RMII1	$t_{c(REF_CLK)}$	Cycle time, REF_CLK	19.999		20.001	ns
RMII2	$t_{w(REF_CLKH)}$	Pulse Duration, REF_CLK High	7		13	ns
RMII3	$t_{w(REF_CLKL)}$	Pulse Duration, REF_CLK Low	7		13	ns

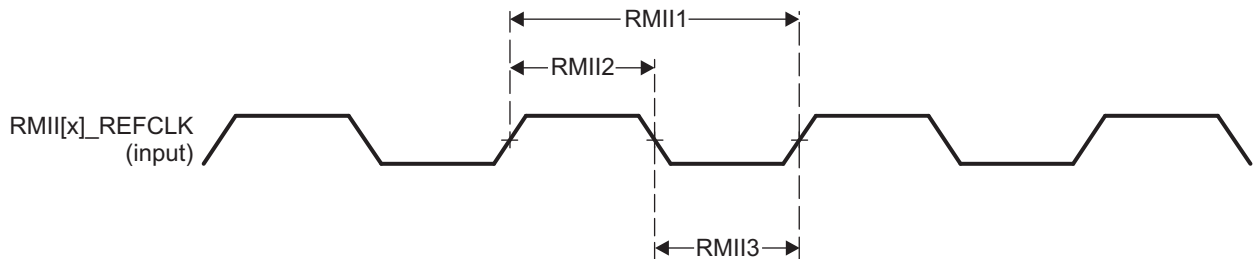


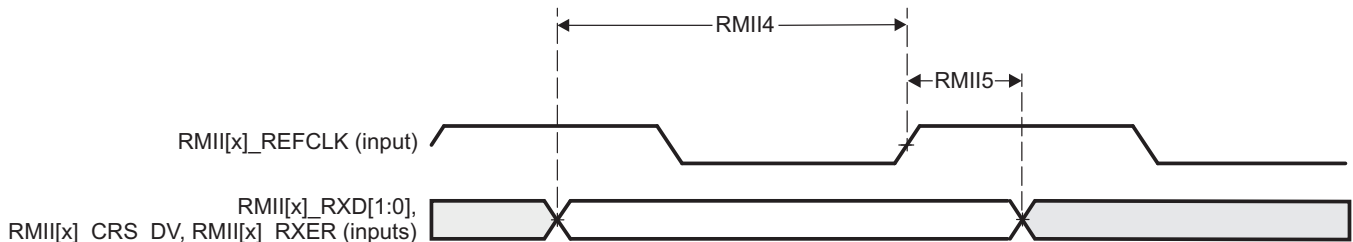
图 5-27. RMII[x]_REFCLK Timing - RMII Mode

表 5-31. Timing Requirements for RMII[x]_RXD[1:0], RMII[x]_CRS_DV, and RMII[x]_RXER - RMII Mode

NO.	PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
RMII4	$t_{su(RXD_REF_CLK)}$	Setup time, RXD[1:0] valid before REF_CLK	4			ns
	$t_{su(CRS_DV_REF_CLK)}$	Setup time, CRS_DV valid before REF_CLK	4			ns
	$t_{su(RX_ER_REF_CLK)}$	Setup time, RX_ER valid before REF_CLK	4			ns

表 5-31. Timing Requirements for RMII[x]_RXD[1:0], RMII[x]_CRS_DV, and RMII[x]_RXER - RMII Mode (continued)

NO.	PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
RMII5	$t_{h(REF_CLK-RXD)}$	Hold time RXD[1:0] valid after REF_CLK	2			ns
	$t_{h(REF_CLK-CRS_DV)}$	Hold time, CRS_DV valid after REF_CLK	2			ns
	$t_{h(REF_CLK-RX_ER)}$	Hold time, RX_ER valid after REF_CLK	2			ns



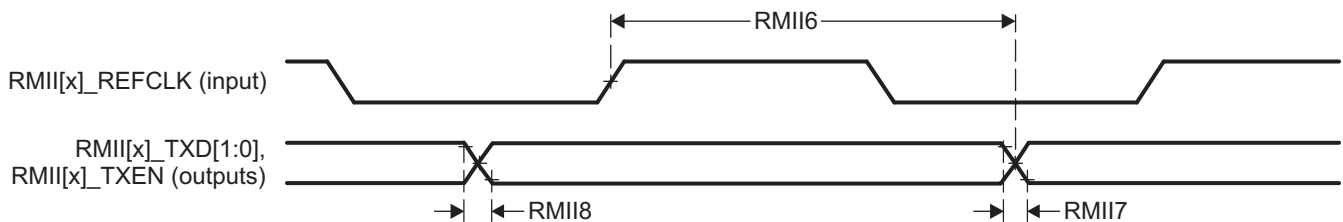
SPRSP08_CPSW2G_RMII RX

图 5-28. RMII[x]_RXD[1:0], RMII[x]_CRS_DV, RMII[x]_RXER Timing - RMII Mode

表 5-32, and 图 5-29 present switching characteristics for CPSW2G RMII Transmit.

表 5-32. Switching Characteristics for RMII[x]_TXD[1:0], and RMII[x]_TXEN - RMII Mode

NO.	PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
RMII6	$t_{d(REF_CLK-TXD)}$	Delay time, REF_CLK High to TXD[1:0] valid	2		13	ns
	$t_{d(REF_CLK-TXEN)}$	Delay time, REF_CLK to TXEN valid	2		13	ns
RMII7	$t_r(TXD)$	Rise Time, TXD Outputs	1		5	ns
	$t_r(TX_EN)$	Rise Time, TX_EN Output	1		5	ns
RMII8	$t_f(TXD)$	Fall Time, TXD Outputs	1		5	ns
	$t_f(TX_EN)$	Fall Time, TX_EN Output	1		5	ns



SPRSP08_CPSW2G_RMII TX

图 5-29. RMII[x]_TXD[1:0], RMII[x]_TXEN Timing - RMII Mode

5.9.5.2.3 CPSW2G RGMII Timings

表 5-33, 表 5-34, and 图 5-30 present timing requirements for receive RGMII operation.

表 5-33. Timing Requirements for RGMII[x]_RCLK - RGMII Mode

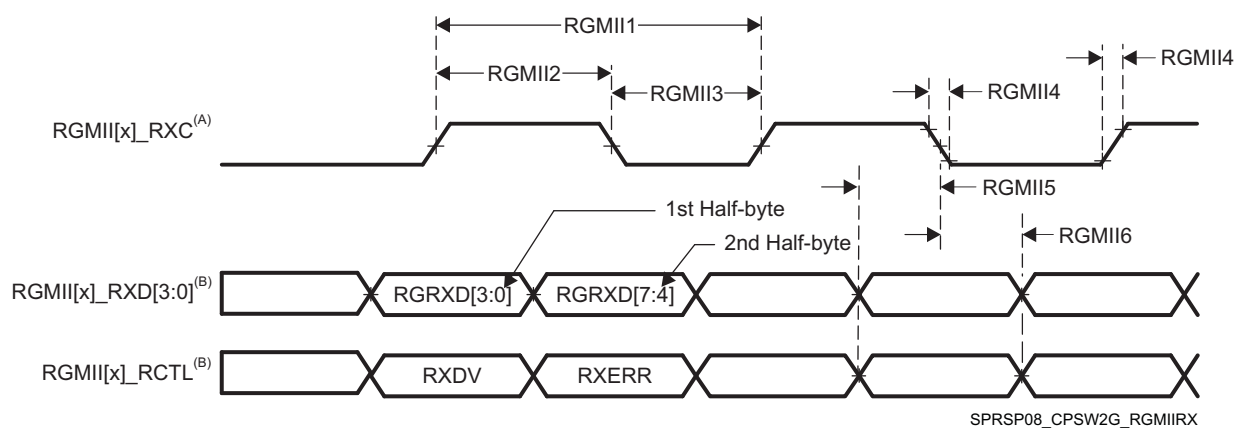
NO.	PARAMETER	DESCRIPTION	MODE	MIN	TYP	MAX	UNIT
RGMII1	$t_c(RXC)$	Cycle time, RXC	10Mbps	360		440	ns
			100Mbps	36		44	ns
			1000Mbps	7.2		8.8	ns

表 5-33. Timing Requirements for RGMII[x]_RCLK - RGMII Mode (continued)

NO.	PARAMETER	DESCRIPTION	MODE	MIN	TYP	MAX	UNIT
RGMII2	$t_{w(RXCH)}$	Pulse duration, RXC high	10Mbps	160		240	ns
			100Mbps	16		24	ns
			1000Mbps	3.6		4.4	ns
RGMII3	$t_{w(RXCL)}$	Pulse duration, RXC low	10Mbps	160		240	ns
			100Mbps	16		24	ns
			1000Mbps	3.6		4.4	ns
RGMII4	$t_l(RXC)$	Transition time, RXC	10Mbps			0.75	ns
			100Mbps			0.75	ns
			1000Mbps			0.75	ns

表 5-34. Timing Requirements for RGMII[x]_RD[3:0], and RGMII[x]_RCTL - RGMII Mode

NO.	PARAMETER	DESCRIPTION	MODE	MIN	TYP	MAX	UNIT
RGMII5	$t_{su(RD-RXC)}$	Setup time, RD[3:0] valid before RXC high/low	10Mbps	1			ns
			100Mbps	1			ns
			1000Mbps	1			ns
	$t_{su(RX_CTL-RXC)}$	Setup time, RX_CTL valid before RXC high/low	10Mbps	1			ns
			100Mbps	1			ns
			1000Mbps	1			ns
RGMII6	$t_h(RXC-RD)$	Hold time, RD[3:0] valid after RXC high/low	10Mbps	1			ns
			100Mbps	1			ns
			1000Mbps	1			ns
	$t_h(RXC-RX_CTL)$	Hold time, RX_CTL valid after RXC high/low	10Mbps	1			ns
			100Mbps	1			ns
			1000Mbps	1			ns
RGMII7	$t_l(RD)$	Transition time, RD	10Mbps			0.75	ns
			100Mbps			0.75	ns
			1000Mbps			0.75	ns
	$t_l(RX_CTL)$	Transition time, RX_CTL	10Mbps			0.75	ns
			100Mbps			0.75	ns
			1000Mbps			0.75	ns



- A. RGMII_RXC must be externally delayed relative to the data and control pins.
- B. Data and control information is received using both edges of the clocks. RGMII_RXD[3:0] carries data bits 3-0 on the rising edge of RGMII_RXC and data bits 7-4 on the falling edge of RGMII_RXC. Similarly, RGMII_RXCTL carries RXDV on rising edge of RGMII_RXC and RXERR on falling edge of RGMII_RXC.

图 5-30. CPSW2G Receive Interface Timing, RGMII operation

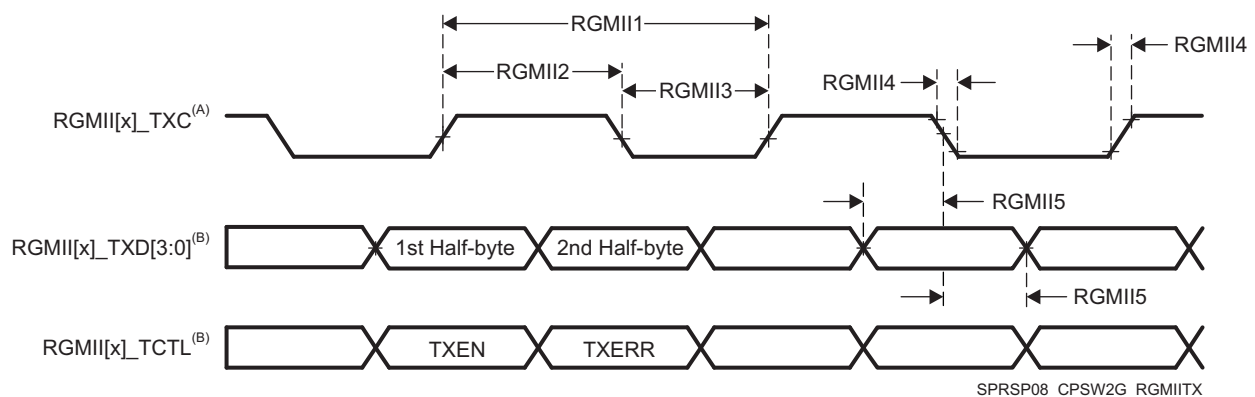
表 5-35, 表 5-36, and 图 5-31 present switching characteristics for transmit - RGMII for 10 Mbps, 100 Mbps, and 1000 Mbps.

表 5-35. Switching Characteristics for RGMII[x]_TCLK - RGMII Mode

NO.	PARAMETER	DESCRIPTION	MODE	MIN	TYP	MAX	UNIT
RGMII1	$t_{c(TXC)}$	Cycle time, TXC	10Mbps	360		440	ns
			100Mbps	36		44	ns
			1000Mbps	7.2		8.8	ns
RGMII2	$t_{w(TXCH)}$	Pulse duration, TXC high	10Mbps	160		240	ns
			100Mbps	16		24	ns
			1000Mbps	3.6		4.4	ns
RGMII3	$t_{w(TXCL)}$	Pulse duration, TXC low	10Mbps	160		240	ns
			100Mbps	16		24	ns
			1000Mbps	3.6		4.4	ns
RGMII4	$t_{t(TXC)}$	Transition time, TXC	10Mbps			0.75	ns
			100Mbps			0.75	ns
			1000Mbps			0.75	ns

表 5-36. Switching Characteristics for RGMII[x]_TD[3:0], and RGMII[x]_TCTL - RGMII Mode

NO.	PARAMETER	DESCRIPTION	MODE	MIN	TYP	MAX	UNIT
RGMII5	$t_{sk(TD-TXC)}$	TD to TXC output skew	10Mbps	TBD		TBD	ns
			100Mbps	TBD		TBD	ns
			1000Mbps	TBD		TBD	ns
	$t_{sk(TX_CTL-TXC)}$	TX_CTL to TXC output skew	10Mbps	TBD		TBD	ns
			100Mbps	TBD		TBD	ns
			1000Mbps	TBD		TBD	ns
RGMII6	$t_{t(TD)}$	Transition time, TD	10Mbps			0.75	ns
			100Mbps			0.75	ns
			1000Mbps			0.75	ns
	$t_{t(TX_CTL)}$	Transition time, TX_CTL	10Mbps			0.75	ns
			100Mbps			0.75	ns
			1000Mbps			0.75	ns



- A. TXC is delayed internally before being driven to the RGMII[x]_TxC pin. This internal delay is always enabled.
- B. Data and control information is received using both edges of the clocks. RGMII_TXD[3:0] carries data bits 3-0 on the rising edge of RGMII_TXC and data bits 7-4 on the falling edge of RGMII_TXC. Similarly, RGMII_TXCTL carries TXDV on rising edge of RGMII_TXC and RTXERR on falling edge of RGMII_TXC.

图 5-31. CPSW2G Transmit Interface Timing RGMII Mode

For more information, see section *Gigabit Ethernet MAC (MCU_CPSW0)* in the device TRM.

5.9.5.3 CSI2

注

For more information, see section *Camera Adapter Layer (CAL) Subsystem* in the device TRM.

The camera adaptation layer (CAL) is a very flexible subsystem that enables connection to multiple cameras supporting MIPI CSI-2 over D-PHY serial interface, a LVDS serial interface, and a traditional parallel interface.

The device includes one instantiation of CAL Subsystem named CALSS0, with a single companion CAMERARX0 instance.

- CSI2 Port is compliant with MIPI CSI-2 protocol with four data lanes.

5.9.5.4 DDRSS

For more details about features and additional description information on the device DDR3L, DDR4, and LPDDR4 Memory Interfaces, see the corresponding sections within [4.3, Signal Descriptions](#) and [6, Detailed Description](#).

The device has dedicated interfaces to DDR3L, DDR4, and LPDDR4 SDRAM. It supports JEDEC JESD79-3-1, JESD79-4B, and JESD209-4B standards compliant DDR3L, DDR4, and LPDDR4 SDRAM devices with the following features:

- 16-bit or 32-bit data path to external SDRAM memory
- Memory device capacity: Up to 32 GB address space available over one chip select

[表 5-37](#) and [図 5-32](#) present switching characteristics for DDRSS.

表 5-37. Switching Characteristics for DDRSS

NO.	PARAMETER	DDR TYPE	MODE	MIN	MAX	UNIT
1	$t_{c(DDR_CKP/DDR_CKN)}$	DDR3L		1.25	3.3	ns
		DDR4		1.25	1.6	
		LPDDR4	DDR PHY PLL: DDRPHY_PLLCR0[31] = 0	1.5	3.003	

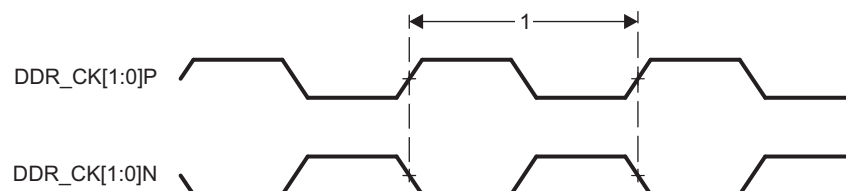


図 5-32. DDRSS Memory Interface Clock Timing

For more information, see section *DDR Subsystem (DDRSS)* in the device TRM.

5.9.5.5 DSS

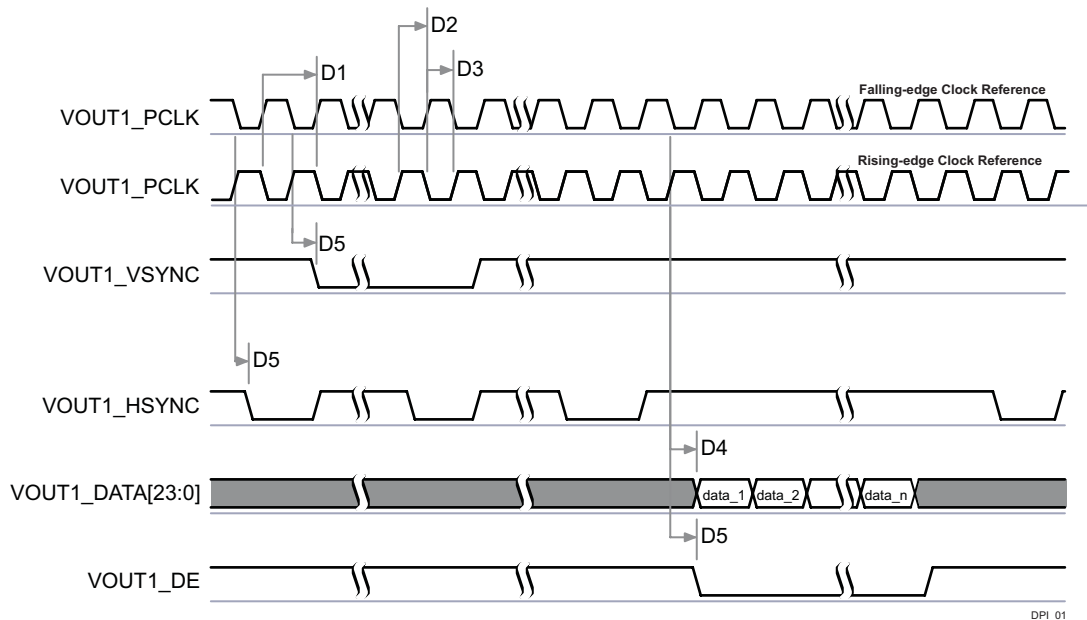
For more details about features and additional description information on the device Display Subsystem – Video Output Ports, see the corresponding sections within [4.3, Signal Descriptions](#) and [6, Detailed Description](#).

表 5-38, 表 5-39, 图 5-33 和 图 5-34 assume testing over the recommended operating conditions and electrical characteristic conditions.

表 5-38. DPI Video Output Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
D1	$t_c(\text{VOUT1_PCLK})$	Cycle time, VOUT1_PCLK	6.06		ns
D2	$t_w(\text{VOUT1_PCLKL})$	Pulse duration, VOUT1_PCLK low	$0.45 \times P^{(1)}$		ns
D3	$t_w(\text{VOUT1_PCLKH})$	Pulse duration, VOUT1_PCLK high	$0.45 \times P^{(1)}$		ns
D4	$t_d(\text{VOUT1_PCLK-VOUT_DATA})$	Delay time, VOUT1_PCLK to VOUT1_DATA[23:0]	-0.68	1.78	ns
D5	$t_d(\text{VOUT1_PCLK-VOUT_CTRL})$	Delay time, VOUT1_PCLK to VOUT1_VSYNC, VOUT1_HSYNC, VOUT1_DE	-0.68	1.78	ns

(1) P = output VOUT1_PCLK period in ns.



- (1) The configuration of assertion of the data can be programmed on the falling or rising edge of the pixel clock.
- (2) The polarity and the pulse width of VOUT1_HSYNC and VOUT1_VSYNC are programmable, refer to section *Display Subsystem (DSS)* in the device TRM.
- (3) The VOUT1_PCLK frequency can be configured, refer to section *Display Subsystem (DSS)* in the device TRM..

图 5-33. DPI Video Output ⁽¹⁾⁽²⁾⁽³⁾

表 5-39. DPI External Pixel Clock Input Timing Requirements

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
D6	$t_c(\text{VOUT1_EXTCLKIN})$	Cycle time, VOUT1_EXTCLKIN	6.06		ns
D7	$t_w(\text{VOUT1_EXTCLKIN})$	Pulse duration, VOUT1_EXTCLKIN low	$0.45 \times P^{(1)}$		ns
D8	$t_w(\text{VOUT1_EXTCLKIN})$	Pulse duration, VOUT1_EXTCLKIN high	$0.45 \times P^{(1)}$		ns

(1) P = output VOUT1_PCLK period in ns.

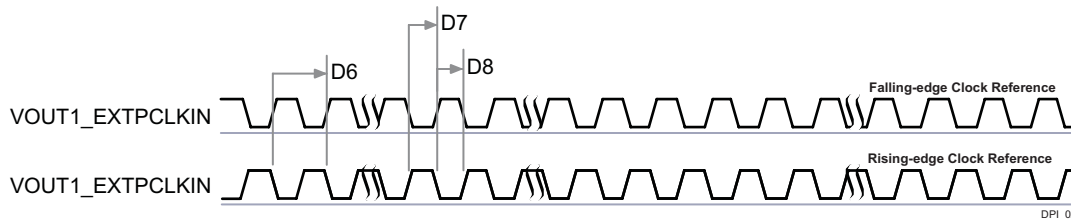


图 5-34. DPI External Pixel Clock Input

For more information, see section *Display Subsystem (DSS)* in the device TRM.

5.9.5.6 eCAP

The supported features by the device eCAP are:

- 32-bit time base counter
- 4-event time-stamp registers (each 32 bits)
- Independent edge polarity selection for up to four sequenced time-stamp capture events
- Interrupt capabilities on any of the four capture events
- Input capture signal pre-scaling (from 1 to 16)
- Support of different capture modes (single shot capture, continuous mode capture, absolute timestamp capture or difference mode time-stamp capture)

表 5-40 and 表 5-41 present timing and switching characteristics for eCAP (see 图 5-35 and 图 5-36).

表 5-40. Timing Requirements for eCAP

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
CAP1	$t_w(\text{CAP})$	Pulse duration, capture input (asynchronous)	$3 + 2P^{(1)}$		ns

(1) P = sysclk

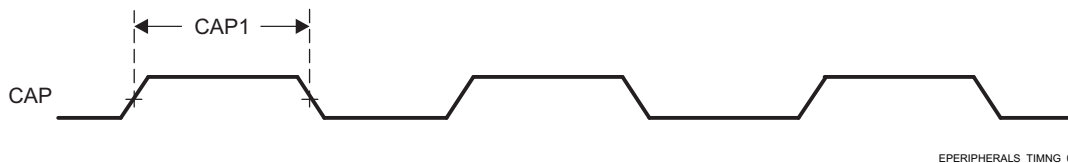


图 5-35. eCAP Input Timings

表 5-41. Switching Characteristics for eCAP

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
CAP2	$t_w(\text{APWM})$	Pulse duration, APWMx output high/low	$-3 + 2P^{(1)}$		ns

(1) P = sysclk


 **5-36. eCAP Output Timings**

For more information, see section *Enhanced Capture (ECAP) Module* in the device TRM.

5.9.5.7 eHRPWM

The supported features by the device eHRPWM are:

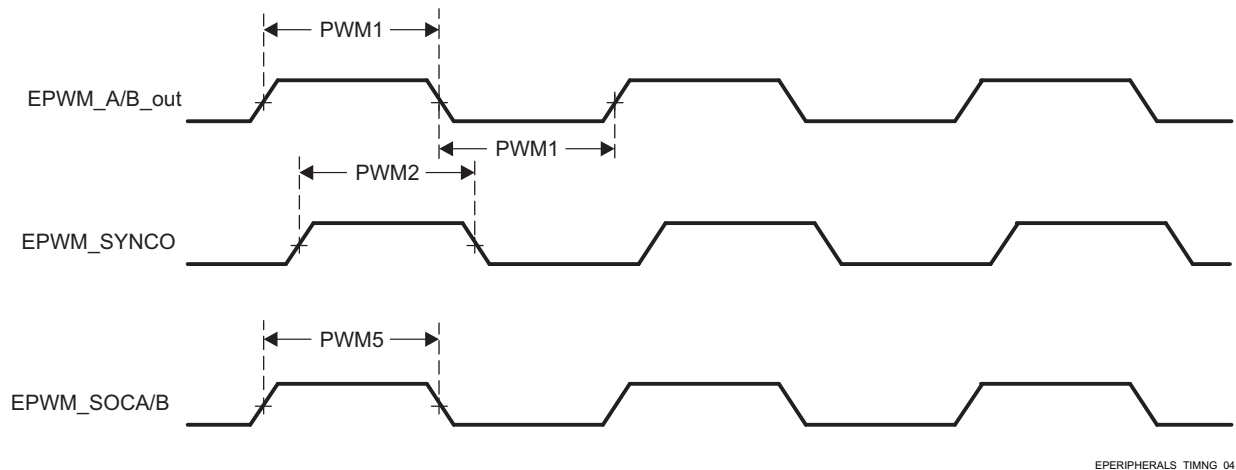
- Dedicated 16-bit time-base counter with period and frequency control
- Two independent PWM outputs which can be used in different configurations (with single-edge operation, with dual-edge symmetric operation or one independent PWM output with dual-edge asymmetric operation)
- Asynchronous override control of PWM signals during fault conditions
- Programmable phase-control support for lag or lead operation relative to other EPWM modules
- Dead-band generation with independent rising and falling edge delay control
- Programmable trip zone allocation of both latched and un-latched fault conditions
- Events enabling to trigger both CPU interrupts and start of ADC conversions

表 5-42, 表 5-43 and present timing and switching characteristics for eHRPWM (see  5-37,  5-38,  5-39, and  5-40).

表 5-42. Timing Requirements for eHRPWM

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PWM1	$t_w(\text{PWM})$	Pulse duration, PWM output high/low	$-3 + 1P^{(1)}$		ns
PWM2	$t_w(\text{SYNCO})$	Pulse duration, Sync output	$-3 + 1P^{(1)}$		ns
PWM3	$t_d(\text{TZ-PWM})$	Delay time, trip input active to PWM forced high/low		11	ns
PWM4	$t_d(\text{TZ-PWMZ})$	Delay time, trip input active to PWM Hi-Z		11	ns
PWM5	$t_w(\text{SOC})$	Pulse duration, SOC output (asynchronous)	$-3 + 1P^{(1)}$		ns

(1) P = sysclk


 **5-37. ePWM_A/B_out, ePWM_SYNCO, and ePWM_SOC/A/B Input Timings**

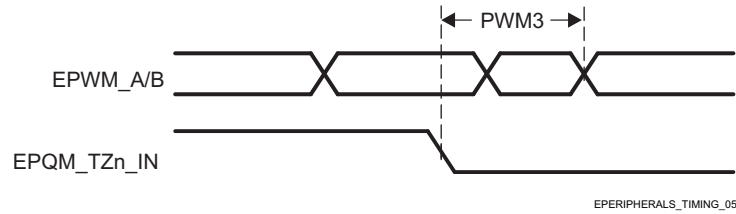


图 5-38. ePWM_A/B and ePWM_TZn_IN Forced High/Low Input Timings

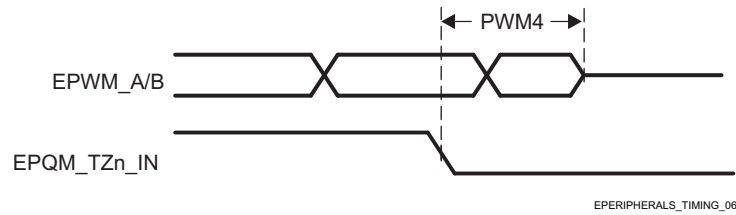


图 5-39. ePWM_A/B and ePWM_TZn_IN Hi-Z Input Timings

表 5-43. Switching Characteristics for eHRPWM

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PWM6	$t_{w(SYNCIN)}$	Pulse duration, Sync input (asynchronous)	$3 + 2P^{(1)}$		ns
PWM7	$t_{w(TZ)}$	Pulse duration, TZx input low (asynchronous)	$3 + 3P^{(1)}$		ns

(1) P = sysclk

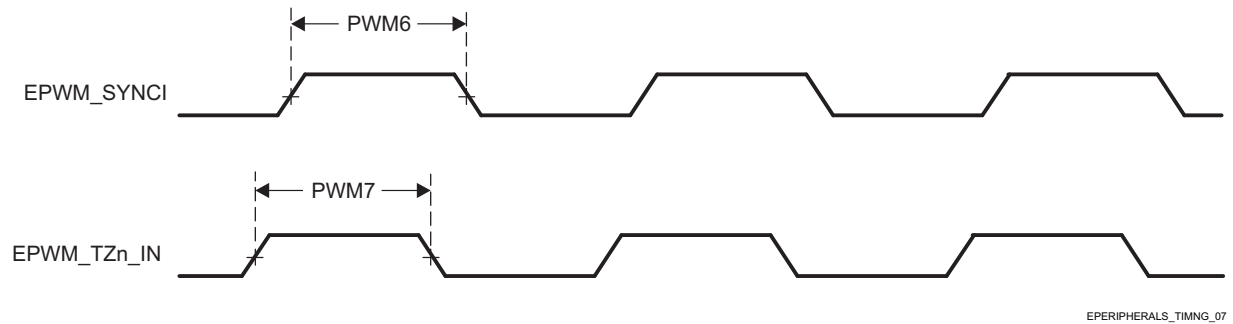


图 5-40. ePWM_SYNCI and ePWM_TZn_IN Output Timings

For more information, see section *Enhanced Pulse Width Modulation (EPWM) Module* in the device TRM.

5.9.5.8 eQEP

The supported features by the device eQEP are:

- Input Synchronization
- Three Stage/Six Stage Digital Noise Filter
- Quadrature Decoder Unit
- Position Counter and Control unit for position measurement
- Quadrature Edge Capture unit for low speed measurement
- Unit Time base for speed/frequency measurement
- Watchdog Timer for detecting stalls

表 5-44 和 表 5-45 present Timing Requirements and Switching Characteristics for eQEP (see 图 5-41).

表 5-44. Timing Requirements for eQEP

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
QEP1	$t_{w(QEP)}$	Pulse duration, QEP input	$3 + 2P^{(1)}$		ns
QEP2	$t_{w(QEPIH)}$	Pulse duration, QEP Index input high	$3 + 2P^{(1)}$		ns
QEP3	$t_{w(QEPI L)}$	Pulse duration, QEP Index input low	$3 + 2P^{(1)}$		ns
QEP4	$t_{w(QEPSH)}$	Pulse duration, QEP Strobe high	$3 + 2P^{(1)}$		ns
QEP5	$t_{w(QEPSL)}$	Pulse duration, QEP Strobe low	$3 + 2P^{(1)}$		ns

(1) P = sysclk

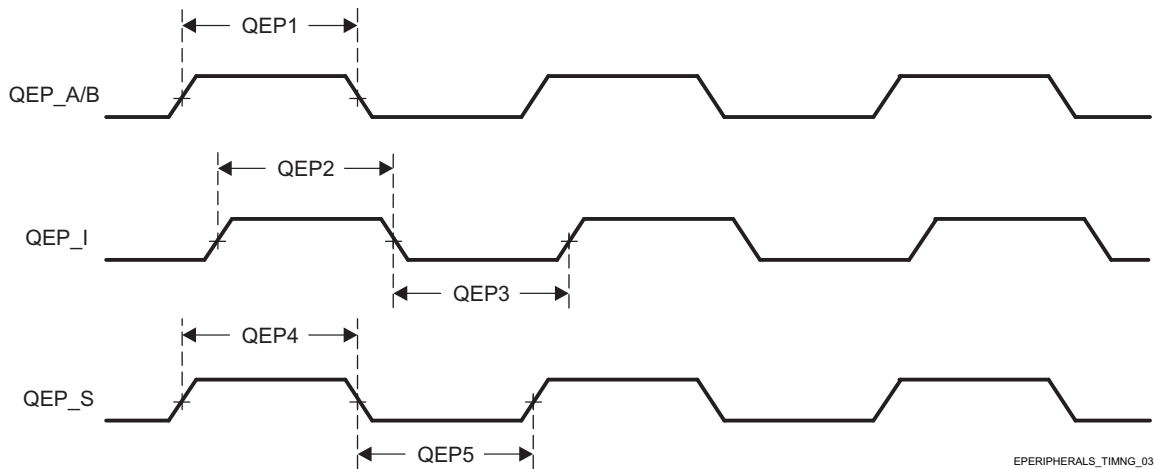


图 5-41. eQEP Input Timings

表 5-45. Switching Characteristics for eQEP

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
QEP6	$t_{d(QEP-CNTR)}$	Delay time, external clock to counter increment		24	ns

For more information, see section *Enhanced Quadrature Encoder Pulse (EQEP) Module* in the device TRM.

5.9.5.9 GPIO

The device has three instances of GPIO144 modules. The GPIO pins are grouped into banks (16 pins per bank), which means that each GPIO module provides up to 144 dedicated general-purpose pins with input and output capabilities; thus, the general-purpose interface supports up to 432 (3 instances × (9 banks × 16 pins)) pins. Since WKUP_GPIO0_[56:143], GPIO0_[96:143], and GPIO1_[90:143] are reserved in this Device, general purpose interface supports up to 242 pins.

For more details about features and additional description information on the device General-Purpose Interface, see the corresponding sections within [4.3, Signal Descriptions](#) and [6, Detailed Description](#).

注

The general-purpose input/output i (i = 0 to 1) is also referred to as GPIOi.

表 5-46 和 表 5-47 present timings and switching characteristics of the GPIO Interface.

表 5-46. GPIO Timing Requirements

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
GP2	$t_{w(GPIO_IN)}$	Minimum Input Pulse Width	$3.6 + 2P^{(1)}$		ns

(1) P = functional clock period in ns.

表 5-47. GPIO Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
GP1	$t_{w(GPIO_OUT)}$	Minimum Output Pulse Width	-4.6 + 0.975P ⁽¹⁾		ns

(1) P = functional clock period in ns.

For more information, see section *General-Purpose Interface (GPIO)* in the device TRM.

5.9.5.10 GPMC

For more details about features and additional description information on the device General-Purpose Memory Controller, see the corresponding sections within [4.3, Signal Descriptions](#) and [6, Detailed Description](#).

5.9.5.10.1 GPMC and NOR Flash—Synchronous Mode

[表 5-48](#) and [表 5-49](#) assume testing over the recommended operating conditions and electrical characteristic conditions below (see [图 5-42](#) through [图 5-46](#)).

表 5-48. GPMC and NOR Flash Timing Requirements—Synchronous Mode

NO.	PARAMETER	DESCRIPTION	MODE ⁽³⁾	MIN	MAX	UNIT
F12	$t_{su(dV-clkH)}$	Setup time, input data GPMC_AD[15:0] valid before output clock GPMC_CLK high	div_by_1_mode; GPMC_FCLK_MUX_100; TIMEPARAGRANULARITY_X1	0.59		ns
			not_div_by_1_mode; GPMC_FCLK_MUX_100; TIMEPARAGRANULARITY_X1	0.34		ns
F13	$t_{h(clkH-dV)}$	Hold time, input data GPMC_AD[15:0] valid after output clock GPMC_CLK high	div_by_1_mode; GPMC_FCLK_MUX_100; TIMEPARAGRANULARITY_X1	1.78		ns
			not_div_by_1_mode; GPMC_FCLK_MUX_100; TIMEPARAGRANULARITY_X1	1.78		ns
F21	$t_{su(waitV-clkH)}$	Setup time, input wait GPMC_WAIT[x] valid before output clock GPMC_CLK high ⁽¹⁾	div_by_1_mode; GPMC_FCLK_MUX_100; TIMEPARAGRANULARITY_X1	0.59		ns
			not_div_by_1_mode; GPMC_FCLK_MUX_100; TIMEPARAGRANULARITY_X1	0.34		ns
F22	$t_{h(clkH-waitV)}$	Hold time, input wait GPMC_WAIT[x] valid after output clock GPMC_CLK high ⁽¹⁾	div_by_1_mode; GPMC_FCLK_MUX_100; TIMEPARAGRANULARITY_X1	1.78		ns
			not_div_by_1_mode; GPMC_FCLK_MUX_100; TIMEPARAGRANULARITY_X1	1.78		ns

(1) In GPMC_WAIT[x], x is equal to 0 or 1.

(2) Wait monitoring support is limited to a WaitMonitoringTime value > 0. For a full description of wait monitoring feature, see section *General-Purpose Memory Controller (GPMC)* in the device TRM.

(3) For div_by_1_mode:

- GPMC_CONFIG1_i Register: GPMCFCLKDIVIDER = 0h:
- GPMC_CLK frequency = GPMC_FCLK frequency

For not_div_by_1_mode:

- GPMC_CONFIG1_i Register: GPMCFCLKDIVIDER = 1h to 3h:
- GPMC_CLK frequency = GPMC_FCLK frequency / (2 to 4)

For GPMC_FCLK_MUX_100:

- gpmc_fclk_sel[1:0] = 01 = PER1_PLL_CLKOUT / 3 = 300 / 3 = 100MHz

For TIMEPARAGRANULARITY_X1:

- GPMC_CONFIG1_i Register: TIMEPARAGRANULARITY = 0h = x1 latencies (affecting RD/WRCYCLETIME, RD/WRACCESSTIME, PAGEBURSTACCESSTIME, CSONTIME, CSRD/WROFFTIME, ADVONTIME, ADVRD/WROFFTIME, OEONTIME, OEOFFTIME, WEONTIME, WEOFFTIME, CYCLE2CYCLEDELAY, BUSTURNAROUND, TIMEOUTSTARTVALUE, WRDATAONADMUXBUS)

表 5-49. GPMC and NOR Flash Switching Characteristics—Synchronous Mode⁽²⁾

NO.	PARAMETER	DESCRIPTION	MODE ⁽²⁰⁾	MIN	MAX	UNIT
F0	1 / tc(clk)	Period, output clock GPMC_CLK ⁽¹⁸⁾	div_by_1_mode; GPMC_FCLK_MUX_100; TIMEPARAGRANULARITY_X1	10		ns
F1	t _w (clkH)	Typical pulse duration, output clock GPMC_CLK high	div_by_1_mode; GPMC_FCLK_MUX_100; TIMEPARAGRANULARITY_X1	-0.3+0.475*P ⁽¹⁵⁾		ns
F1	t _w (clkL)	Typical pulse duration, output clock GPMC_CLK low	div_by_1_mode; GPMC_FCLK_MUX_100; TIMEPARAGRANULARITY_X1	-0.3+0.475*P ⁽¹⁵⁾		ns
	t _{dc} (clk)	Duty cycle error, output clock GPMC_CLK	div_by_1_mode; GPMC_FCLK_MUX_100; TIMEPARAGRANULARITY_X1	-500	500	ps
	t _j (clk)	Jitter standard deviation, output clock GPMC_CLK ⁽¹⁹⁾	div_by_1_mode; GPMC_FCLK_MUX_100; TIMEPARAGRANULARITY_X1		33.33	ps
	t _R (clk)	Rise time, output clock GPMC_CLK	div_by_1_mode; GPMC_FCLK_MUX_100; TIMEPARAGRANULARITY_X1		2	ns
	t _F (clk)	Fall time, output clock GPMC_CLK	div_by_1_mode; GPMC_FCLK_MUX_100; TIMEPARAGRANULARITY_X1		2	ns
	t _R (do)	Rise time, output data GPMC_AD[15:0]	div_by_1_mode; GPMC_FCLK_MUX_100; TIMEPARAGRANULARITY_X1		2	ns
	t _F (do)	Fall time, output data GPMC_AD[15:0]	div_by_1_mode; GPMC_FCLK_MUX_100; TIMEPARAGRANULARITY_X1		2	ns
F2	t _d (clkH-csnV)	Delay time, output clock GPMC_CLK rising edge to output chip select GPMC_CS[n] transition ⁽¹⁴⁾	div_by_1_mode; GPMC_FCLK_MUX_100; TIMEPARAGRANULARITY_X1; no extra_delay	-2.2+F ⁽⁶⁾	4.5+F ⁽⁶⁾	ns
F3	t _d (clkH-csnIV)	Delay time, output clock GPMC_CLK rising edge to output chip select GPMC_CS[n] invalid ⁽¹⁴⁾	div_by_1_mode; GPMC_FCLK_MUX_100; TIMEPARAGRANULARITY_X1; no extra_delay	-2.2+E ⁽⁵⁾	4.5+E ⁽⁵⁾	ns
F4	t _d (aV-clk)	Delay time, output address GPMC_A[27:1] valid to output clock GPMC_CLK first edge	div_by_1_mode; GPMC_FCLK_MUX_100; TIMEPARAGRANULARITY_X1	-2.3+B ⁽²⁾	4.5+B ⁽²⁾	ns
F5	t _d (clkH-aIV)	Delay time, output clock GPMC_CLK rising edge to output address GPMC_A[27:1] invalid	div_by_1_mode; GPMC_FCLK_MUX_100; TIMEPARAGRANULARITY_X1	-2.3	4.5	ns
F6	t _d (be[x]nV-clk)	Delay time, output lower byte enable and command latch enable GPMC_BE0n_CLE, output upper byte enable GPMC_BE1n valid to output clock GPMC_CLK first edge	div_by_1_mode; GPMC_FCLK_MUX_100; TIMEPARAGRANULARITY_X1	-2.3+B ⁽²⁾	1.9+B ⁽²⁾	ns
F7	t _d (clkH-be[x]nIV)	Delay time, output clock GPMC_CLK rising edge to output lower byte enable and command latch enable GPMC_BE0n_CLE, output upper byte enable GPMC_BE1n invalid ⁽¹¹⁾	div_by_1_mode; GPMC_FCLK_MUX_100; TIMEPARAGRANULARITY_X1	-2.3+D ⁽⁴⁾	1.9+D ⁽⁴⁾	ns
F7	t _d (clkL-be[x]nIV)	Delay time, GPMC_CLK falling edge to GPMC_BE0n_CLE, GPMC_BE1n invalid ⁽¹²⁾	div_by_1_mode; GPMC_FCLK_MUX_100; TIMEPARAGRANULARITY_X1	-2.3+D ⁽⁴⁾	1.9+D ⁽⁴⁾	ns
F7	t _d (clkL-be[x]nIV)	Delay time, GPMC_CLK falling edge to GPMC_BE0n_CLE, GPMC_BE1n invalid ⁽¹³⁾	div_by_1_mode; GPMC_FCLK_MUX_100; TIMEPARAGRANULARITY_X1	-2.3+D ⁽⁴⁾	1.9+D ⁽⁴⁾	ns

表 5-49. GPMC and NOR Flash Switching Characteristics—Synchronous Mode⁽²⁾ (continued)

NO.	PARAMETER	DESCRIPTION	MODE ⁽²⁰⁾	MIN	MAX	UNIT
F8	$t_{d(\text{clkH-advn})}$	Delay time, output clock GPMC_CLK rising edge to output address valid and address latch enable GPMC_ADVn_ALE transition	div_by_1_mode; GPMC_FCLK_MUX_100; TIMEPARAGRANULARITY_X1; no extra_delay	-2.3+G ⁽⁷⁾	4.5+G ⁽⁷⁾	ns
F9	$t_{d(\text{clkH-advnIV})}$	Delay time, output clock GPMC_CLK rising edge to output address valid and address latch enable GPMC_ADVn_ALE invalid	div_by_1_mode; GPMC_FCLK_MUX_100; TIMEPARAGRANULARITY_X1; no extra_delay	-2.3+D ⁽⁴⁾	4.5+D ⁽⁴⁾	ns
F10	$t_{d(\text{clkH-oen})}$	Delay time, output clock GPMC_CLK rising edge to output enable GPMC_OEn_REn transition	div_by_1_mode; GPMC_FCLK_MUX_100; TIMEPARAGRANULARITY_X1; no extra_delay	-2.3H ⁽⁸⁾	3.5+H ⁽⁸⁾	ns
F11	$t_{d(\text{clkH-oenIV})}$	Delay time, output clock GPMC_CLK rising edge to output enable GPMC_OEn_REn invalid	div_by_1_mode; GPMC_FCLK_MUX_100; TIMEPARAGRANULARITY_X1; no extra_delay	-2.3+E ⁽⁸⁾	3.5+E ⁽⁸⁾	ns
F14	$t_{d(\text{clkH-wen})}$	Delay time, output clock GPMC_CLK rising edge to output write enable GPMC_WEn transition	div_by_1_mode; GPMC_FCLK_MUX_100; TIMEPARAGRANULARITY_X1; no extra_delay	-2.3+I ⁽⁹⁾	4.5+I ⁽⁹⁾	ns
F15	$t_{d(\text{clkH-do})}$	Delay time, output clock GPMC_CLK rising edge to output data GPMC_AD[15:0] transition ⁽¹¹⁾	div_by_1_mode; GPMC_FCLK_MUX_100; TIMEPARAGRANULARITY_X1	-2.3+J ⁽¹⁰⁾	2.7+J ⁽¹⁰⁾	ns
F15	$t_{d(\text{clkL-do})}$	Delay time, GPMC_CLK falling edge to GPMC_AD[15:0] data bus transition ⁽¹²⁾	div_by_1_mode; GPMC_FCLK_MUX_100; TIMEPARAGRANULARITY_X1	-2.3+J ⁽¹⁰⁾	2.7+J ⁽¹⁰⁾	ns
F15	$t_{d(\text{clkL-do})}$	Delay time, GPMC_CLK falling edge to GPMC_AD[15:0] data bus transition ⁽¹³⁾	div_by_1_mode; GPMC_FCLK_MUX_100; TIMEPARAGRANULARITY_X1	-2.3+J ⁽¹⁰⁾	2.7+J ⁽¹⁰⁾	ns
F17	$t_{d(\text{clkH-be[x]n})}$	Delay time, output clock GPMC_CLK rising edge to output lower byte enable and command latch enable GPMC_BE0n_CLE transition ⁽¹¹⁾	div_by_1_mode; GPMC_FCLK_MUX_100; TIMEPARAGRANULARITY_X1	-2.3+J ⁽¹⁰⁾	1.9+J ⁽¹⁰⁾	ns
F17	$t_{d(\text{clkL-be[x]n})}$	Delay time, GPMC_CLK falling edge to GPMC_BE0n_CLE, GPMC_BE1n transition ⁽¹²⁾	div_by_1_mode; GPMC_FCLK_MUX_100; TIMEPARAGRANULARITY_X1	-2.3+J ⁽¹⁰⁾	1.9+J ⁽¹⁰⁾	ns
F17	$t_{d(\text{clkL-be[x]n})}$	Delay time, GPMC_CLK falling edge to GPMC_BE0n_CLE, GPMC_BE1n transition ⁽¹³⁾	div_by_1_mode; GPMC_FCLK_MUX_100; TIMEPARAGRANULARITY_X1	-2.3+J ⁽¹⁰⁾	1.9+J ⁽¹⁰⁾	ns
F18	$t_w(\text{csnV})$	Pulse duration, output chip select GPMC_CS[n] low ⁽¹⁴⁾	Read	A ⁽¹⁾		ns
			Write	A ⁽¹⁾		ns
F19	$t_w(\text{be[x]nV})$	Pulse duration, output lower byte enable and command latch enable GPMC_BE0n_CLE, output upper byte enable GPMC_BE1n low	Read	C ⁽³⁾		ns
			Write	C ⁽³⁾		ns
F20	$t_w(\text{advnV})$	Pulse duration, output address valid and address latch enable GPMC_ADVn_ALE low	Read	K ⁽¹⁶⁾		ns
			Write	K ⁽¹⁶⁾		ns

(1) For single read: $A = (\text{CSRdOffTime} - \text{CSOnTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC_FCLK}^{(17)}$
For burst read: $A = (\text{CSRdOffTime} - \text{CSOnTime} + (n - 1) \times \text{PageBurstAccessTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC_FCLK}^{(17)}$
For burst write: $A = (\text{CSWrOffTime} - \text{CSOnTime} + (n - 1) \times \text{PageBurstAccessTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC_FCLK}^{(17)}$
With n being the page burst access number.

(2) $B = \text{ClkActivationTime} \times \text{GPMC_FCLK}^{(17)}$

(3) For single read: $C = \text{RdCycleTime} \times (\text{TimeParaGranularity} + 1) \times \text{GPMC_FCLK}^{(17)}$
For burst read: $C = (\text{RdCycleTime} + (n - 1) \times \text{PageBurstAccessTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC_FCLK}^{(17)}$
For burst write: $C = (\text{WrCycleTime} + (n - 1) \times \text{PageBurstAccessTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC_FCLK}^{(17)}$
With n being the page burst access number.

(4) For single read: $D = (\text{RdCycleTime} - \text{AccessTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC_FCLK}^{(17)}$
For burst read: $D = (\text{RdCycleTime} - \text{AccessTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC_FCLK}^{(17)}$
For burst write: $D = (\text{WrCycleTime} - \text{AccessTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC_FCLK}^{(17)}$

(5) For single read: $E = (\text{CSRdOffTime} - \text{AccessTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC_FCLK}^{(17)}$
For burst read: $E = (\text{CSRdOffTime} - \text{AccessTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC_FCLK}^{(17)}$
For burst write: $E = (\text{CSWrOffTime} - \text{AccessTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC_FCLK}^{(17)}$

(6) For cs_n falling edge (CS activated):

- Case GpmcFCLKDivider = 0:
 - $F = 0.5 \times \text{CSEExtraDelay} \times \text{GPMC_FCLK}^{(17)}$
- Case GpmcFCLKDivider = 1:
 - $F = 0.5 \times \text{CSEExtraDelay} \times \text{GPMC_FCLK}^{(17)}$ if (ClkActivationTime and CSOnTime are odd) or (ClkActivationTime and CSOnTime are even)
 - $F = (1 + 0.5 \times \text{CSEExtraDelay}) \times \text{GPMC_FCLK}^{(17)}$ otherwise
- Case GpmcFCLKDivider = 2:
 - $F = 0.5 \times \text{CSEExtraDelay} \times \text{GPMC_FCLK}^{(17)}$ if ((CSOnTime - ClkActivationTime) is a multiple of 3)
 - $F = (1 + 0.5 \times \text{CSEExtraDelay}) \times \text{GPMC_FCLK}^{(17)}$ if ((CSOnTime - ClkActivationTime - 1) is a multiple of 3)
 - $F = (2 + 0.5 \times \text{CSEExtraDelay}) \times \text{GPMC_FCLK}^{(17)}$ if ((CSOnTime - ClkActivationTime - 2) is a multiple of 3)

(7) For ADV falling edge (ADV activated):

- Case GpmcFCLKDivider = 0:
 - $G = 0.5 \times \text{ADVExtraDelay} \times \text{GPMC_FCLK}^{(17)}$
- Case GpmcFCLKDivider = 1:
 - $G = 0.5 \times \text{ADVExtraDelay} \times \text{GPMC_FCLK}^{(17)}$ if (ClkActivationTime and ADVOnTime are odd) or (ClkActivationTime and ADVOnTime are even)
 - $G = (1 + 0.5 \times \text{ADVExtraDelay}) \times \text{GPMC_FCLK}^{(17)}$ otherwise
- Case GpmcFCLKDivider = 2:
 - $G = 0.5 \times \text{ADVExtraDelay} \times \text{GPMC_FCLK}^{(17)}$ if ((ADVOnTime - ClkActivationTime) is a multiple of 3)
 - $G = (1 + 0.5 \times \text{ADVExtraDelay}) \times \text{GPMC_FCLK}^{(17)}$ if ((ADVOnTime - ClkActivationTime - 1) is a multiple of 3)
 - $G = (2 + 0.5 \times \text{ADVExtraDelay}) \times \text{GPMC_FCLK}^{(17)}$ if ((ADVOnTime - ClkActivationTime - 2) is a multiple of 3)

For ADV rising edge (ADV deactivated) in Reading mode:

- Case GpmcFCLKDivider = 0:
 - $G = 0.5 \times \text{ADVExtraDelay} \times \text{GPMC_FCLK}^{(17)}$
- Case GpmcFCLKDivider = 1:
 - $G = 0.5 \times \text{ADVExtraDelay} \times \text{GPMC_FCLK}^{(17)}$ if (ClkActivationTime and ADVrDOffTime are odd) or (ClkActivationTime and ADVrDOffTime are even)
 - $G = (1 + 0.5 \times \text{ADVExtraDelay}) \times \text{GPMC_FCLK}^{(17)}$ otherwise
- Case GpmcFCLKDivider = 2:
 - $G = 0.5 \times \text{ADVExtraDelay} \times \text{GPMC_FCLK}^{(17)}$ if ((ADVrDOffTime - ClkActivationTime) is a multiple of 3)
 - $G = (1 + 0.5 \times \text{ADVExtraDelay}) \times \text{GPMC_FCLK}^{(17)}$ if ((ADVrDOffTime - ClkActivationTime - 1) is a multiple of 3)
 - $G = (2 + 0.5 \times \text{ADVExtraDelay}) \times \text{GPMC_FCLK}^{(17)}$ if ((ADVrDOffTime - ClkActivationTime - 2) is a multiple of 3)

For ADV rising edge (ADV deactivated) in Writing mode:

- Case GpmcFCLKDivider = 0:
 - $G = 0.5 \times \text{ADVExtraDelay} \times \text{GPMC_FCLK}^{(17)}$
- Case GpmcFCLKDivider = 1:
 - $G = 0.5 \times \text{ADVExtraDelay} \times \text{GPMC_FCLK}^{(17)}$ if (ClkActivationTime and ADVwROffTime are odd) or (ClkActivationTime and ADVwROffTime are even)
 - $G = (1 + 0.5 \times \text{ADVExtraDelay}) \times \text{GPMC_FCLK}^{(17)}$ otherwise
- Case GpmcFCLKDivider = 2:
 - $G = 0.5 \times \text{ADVExtraDelay} \times \text{GPMC_FCLK}^{(17)}$ if ((ADVwROffTime - ClkActivationTime) is a multiple of 3)
 - $G = (1 + 0.5 \times \text{ADVExtraDelay}) \times \text{GPMC_FCLK}^{(17)}$ if ((ADVwROffTime - ClkActivationTime - 1) is a multiple of 3)
 - $G = (2 + 0.5 \times \text{ADVExtraDelay}) \times \text{GPMC_FCLK}^{(17)}$ if ((ADVwROffTime - ClkActivationTime - 2) is a multiple of 3)

(8) For OE falling edge (OE activated) and IO DIR rising edge (Data Bus input direction):

- Case GpmcFCLKDivider = 0:
 - $H = 0.5 \times \text{OEEExtraDelay} \times \text{GPMC_FCLK}^{(17)}$
- Case GpmcFCLKDivider = 1:
 - $H = 0.5 \times \text{OEEExtraDelay} \times \text{GPMC_FCLK}^{(17)}$ if (ClkActivationTime and OEOnTime are odd) or (ClkActivationTime and OEOnTime are even)
 - $H = (1 + 0.5 \times \text{OEEExtraDelay}) \times \text{GPMC_FCLK}^{(17)}$ otherwise
- Case GpmcFCLKDivider = 2:
 - $H = 0.5 \times \text{OEEExtraDelay} \times \text{GPMC_FCLK}^{(17)}$ if ((OEOnTime - ClkActivationTime) is a multiple of 3)
 - $H = (1 + 0.5 \times \text{OEEExtraDelay}) \times \text{GPMC_FCLK}^{(17)}$ if ((OEOnTime - ClkActivationTime - 1) is a multiple of 3)
 - $H = (2 + 0.5 \times \text{OEEExtraDelay}) \times \text{GPMC_FCLK}^{(17)}$ if ((OEOnTime - ClkActivationTime - 2) is a multiple of 3)

For OE rising edge (OE deactivated):

- Case GpmcFCLKDivider = 0:
 - $H = 0.5 \times \text{OEEExtraDelay} \times \text{GPMC_FCLK}^{(17)}$
- Case GpmcFCLKDivider = 1:
 - $H = 0.5 \times \text{OEEExtraDelay} \times \text{GPMC_FCLK}^{(17)}$ if (ClkActivationTime and OEOffTime are odd) or (ClkActivationTime and OEOffTime are even)
 - $H = (1 + 0.5 \times \text{OEEExtraDelay}) \times \text{GPMC_FCLK}^{(17)}$ otherwise
- Case GpmcFCLKDivider = 2:
 - $H = 0.5 \times \text{OEEExtraDelay} \times \text{GPMC_FCLK}^{(17)}$ if ((OEOffTime - ClkActivationTime) is a multiple of 3)
 - $H = (1 + 0.5 \times \text{OEEExtraDelay}) \times \text{GPMC_FCLK}^{(17)}$ if ((OEOffTime - ClkActivationTime - 1) is a multiple of 3)
 - $H = (2 + 0.5 \times \text{OEEExtraDelay}) \times \text{GPMC_FCLK}^{(17)}$ if ((OEOffTime - ClkActivationTime - 2) is a multiple of 3)

(9) For WE falling edge (WE activated):

- Case GpmcFCLKDivider = 0:
 - $I = 0.5 \times WEEExtraDelay \times GPMC_FCLK^{(17)}$
- Case GpmcFCLKDivider = 1:
 - $I = 0.5 \times WEEExtraDelay \times GPMC_FCLK^{(17)}$ if (ClkActivationTime and WEOntime are odd) or (ClkActivationTime and WEOntime are even)
 - $I = (1 + 0.5 \times WEEExtraDelay) \times GPMC_FCLK^{(17)}$ otherwise
- Case GpmcFCLKDivider = 2:
 - $I = 0.5 \times WEEExtraDelay \times GPMC_FCLK^{(17)}$ if ((WEOntime - ClkActivationTime) is a multiple of 3)
 - $I = (1 + 0.5 \times WEEExtraDelay) \times GPMC_FCLK^{(17)}$ if ((WEOntime - ClkActivationTime - 1) is a multiple of 3)
 - $I = (2 + 0.5 \times WEEExtraDelay) \times GPMC_FCLK^{(17)}$ if ((WEOntime - ClkActivationTime - 2) is a multiple of 3)

For WE rising edge (WE deactivated):

- Case GpmcFCLKDivider = 0:
 - $I = 0.5 \times WEEExtraDelay \times GPMC_FCLK^{(17)}$
- Case GpmcFCLKDivider = 1:
 - $I = 0.5 \times WEEExtraDelay \times GPMC_FCLK^{(17)}$ if (ClkActivationTime and WEOffTime are odd) or (ClkActivationTime and WEOffTime are even)
 - $I = (1 + 0.5 \times WEEExtraDelay) \times GPMC_FCLK^{(17)}$ otherwise
- Case GpmcFCLKDivider = 2:
 - $I = 0.5 \times WEEExtraDelay \times GPMC_FCLK^{(17)}$ if ((WEOffTime - ClkActivationTime) is a multiple of 3)
 - $I = (1 + 0.5 \times WEEExtraDelay) \times GPMC_FCLK^{(17)}$ if ((WEOffTime - ClkActivationTime - 1) is a multiple of 3)
 - $I = (2 + 0.5 \times WEEExtraDelay) \times GPMC_FCLK^{(17)}$ if ((WEOffTime - ClkActivationTime - 2) is a multiple of 3)

(10) $J = GPMC_FCLK^{(17)}$

(11) First transfer only for CLK DIV 1 mode.

(12) Half cycle; for all data after initial transfer for CLK DIV 1 mode.

(13) Half cycle of GPMC_CLK_OUT; for all data for modes other than CLK DIV 1 mode. GPMC_CLK_OUT divide down from GPMC_FCLK.

(14) In GPMC_CS[n], x is equal to 0, 1, 2 or 3. In GPMC_WAIT[x], x is equal to 0 or 1.

(15) $P = GPMC_CLK$ period in ns

(16) For read: $K = (ADVrdOffTime - ADVOnTime) \times (TimeParaGranularity + 1) \times GPMC_FCLK^{(17)}$
For write: $K = (ADVwrOffTime - ADVOnTime) \times (TimeParaGranularity + 1) \times GPMC_FCLK^{(17)}$

(17) GPMC_FCLK is general-purpose memory controller internal functional clock period in ns.

(18) Related to the GPMC_CLK output clock maximum and minimum frequencies programmable in the GPMC module by setting the GPMC_CONFIG1_CSx configuration register bit field GpmcFCLKDivider.

(19) The jitter probability density can be approximated by a Gaussian function.

(20) For div_by_1_mode:

- GPMC_CONFIG1_i Register: GPMCFCLKDIVIDER = 0h:
- GPMC_CLK frequency = GPMC_FCLK frequency

For GPMC_FCLK_MUX_100:

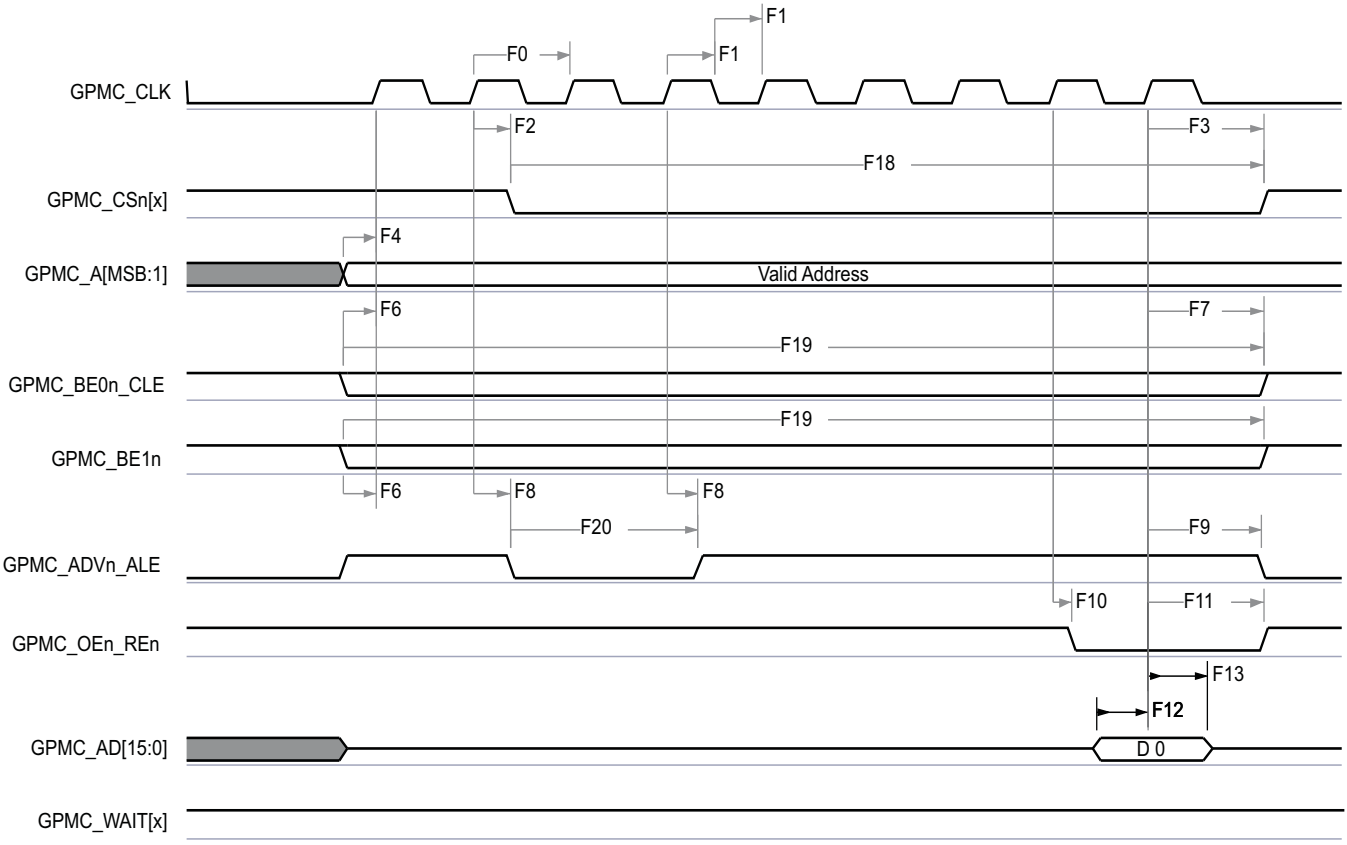
- gpmc_fclk_sel[1:0] = 01 = PER1_PLL_CLKOUT / 3 = 300 / 3 = 100MHz

For TIMEPARAGRANULARITY_X1:

- GPMC_CONFIG1_i Register: TIMEPARAGRANULARITY = 0h = x1 latencies (affecting RD/WRCYCLETIME, RD/WRACCESSTIME, PAGEBURSTACCESSTIME, CSONTIME, CSRD/WROFFTIME, ADVONTIME, ADVRD/WROFFTIME, OEONTIME, OEOFFTIME, WEONTIME, WEOFFTIME, CYCLE2CYCLEDELAY, BUSTURNAROUND, TIMEOUTSTARTVALUE, WRDATAONADMUXBUS)

For no extra_delay:

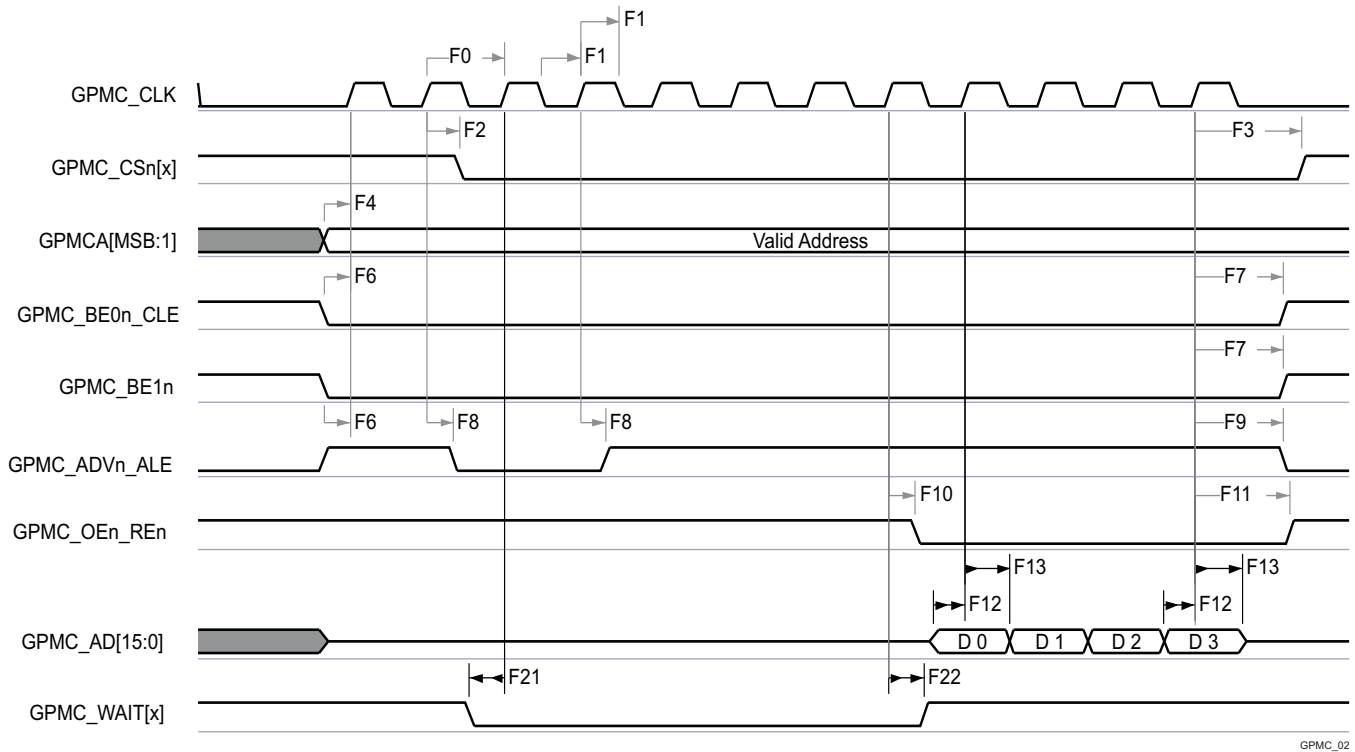
- GPMC_CONFIG2_i Register : CSEXTRADELAY = 0h = CS i Timing control signal is not delayed
- GPMC_CONFIG4_i Register : WEEEXTRADELAY = 0h = nWE timing control signal is not delayed
- GPMC_CONFIG4_i Register : OEEXTRADELAY = 0h = nOE timing control signal is not delayed
- GPMC_CONFIG3_i Register: ADVEXTRADELAY = 0h = nADV timing control signal is not delayed



GPMC_01

- A. In GPMC_CS[n], x is equal to 0, 1, 2 or 3.
B. In GPMC_WAIT[x], x is equal to 0 or 1.

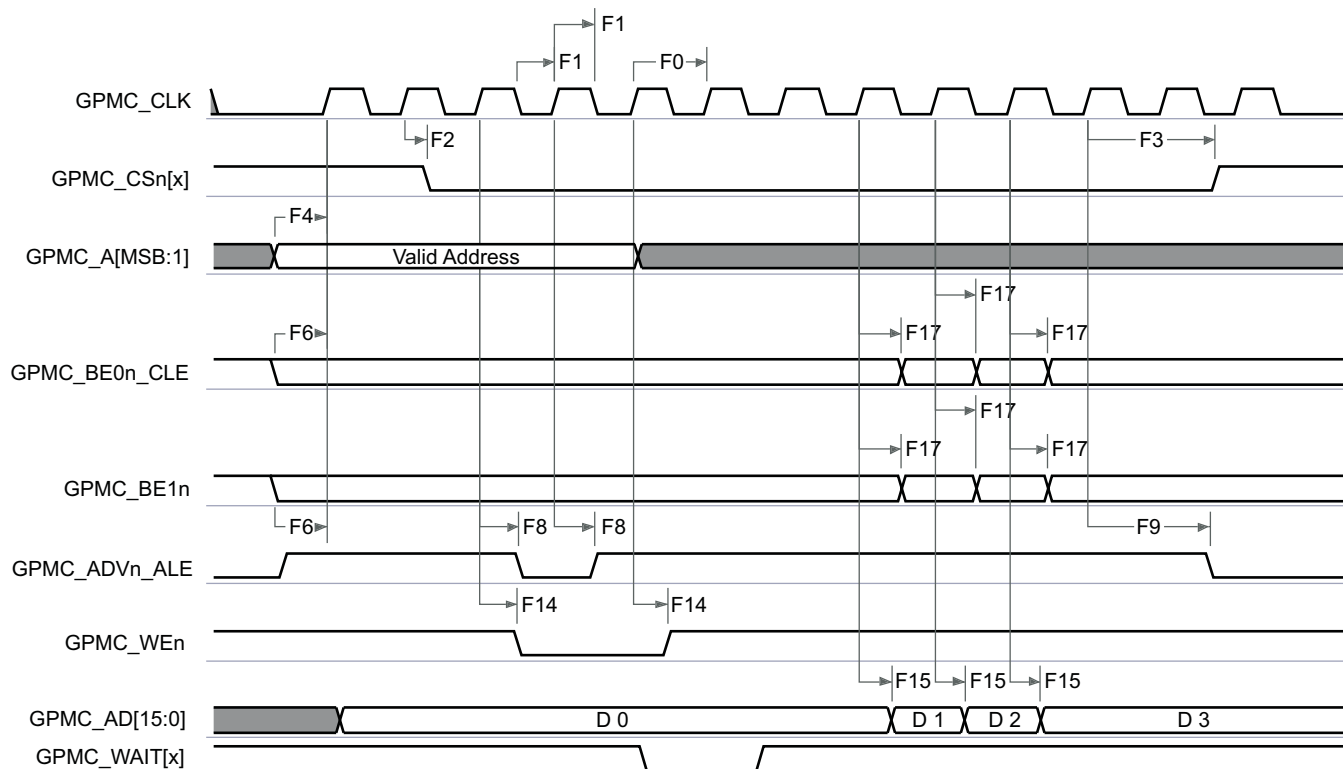
5-42. GPMC and NOR Flash—Synchronous Single Read—(GpmcFCLKDivider = 0)



- A. In GPMC_CS[x], x is equal to 0, 1, 2 or 3.
B. In GPMC_WAIT[x], x is equal to 0 or 1.

图 5-43. GPMC and NOR Flash—Synchronous Burst Read—4x16-bit (GpmcFCLKDivider = 0)

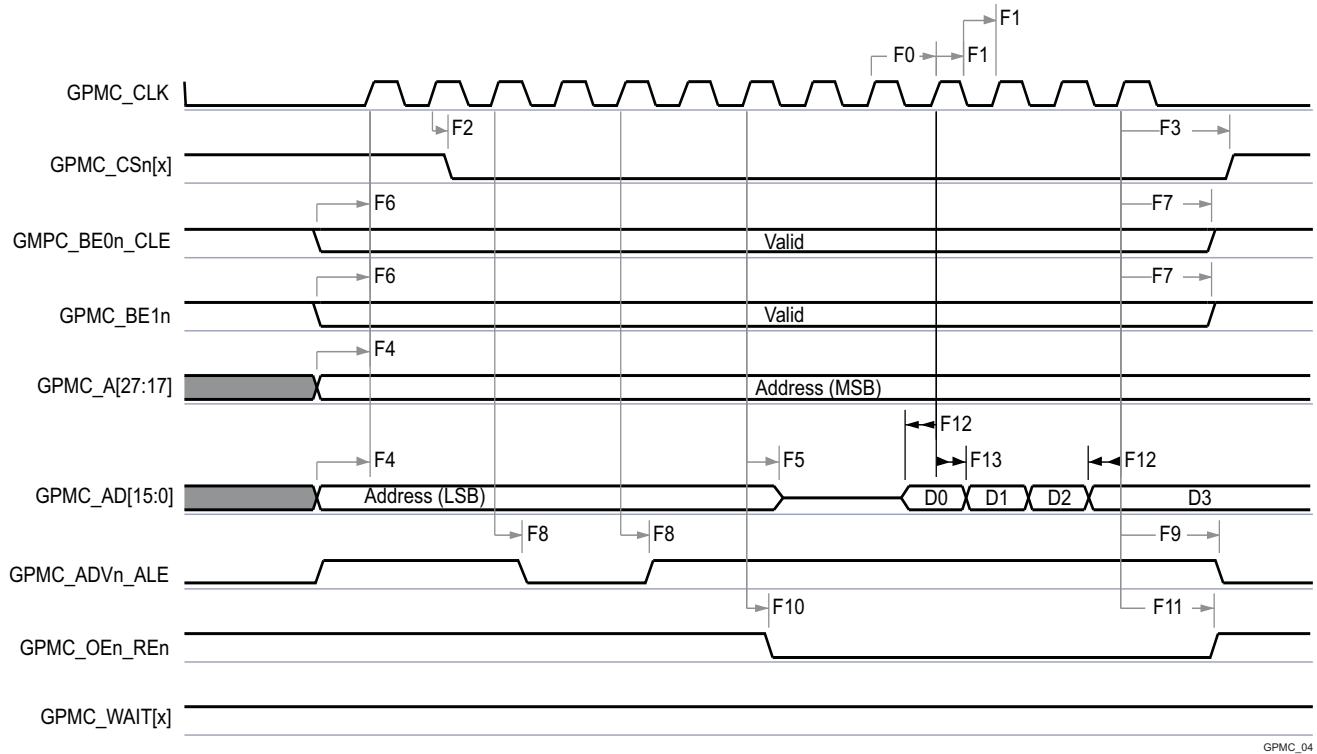
GPMC_02



GPMC_03

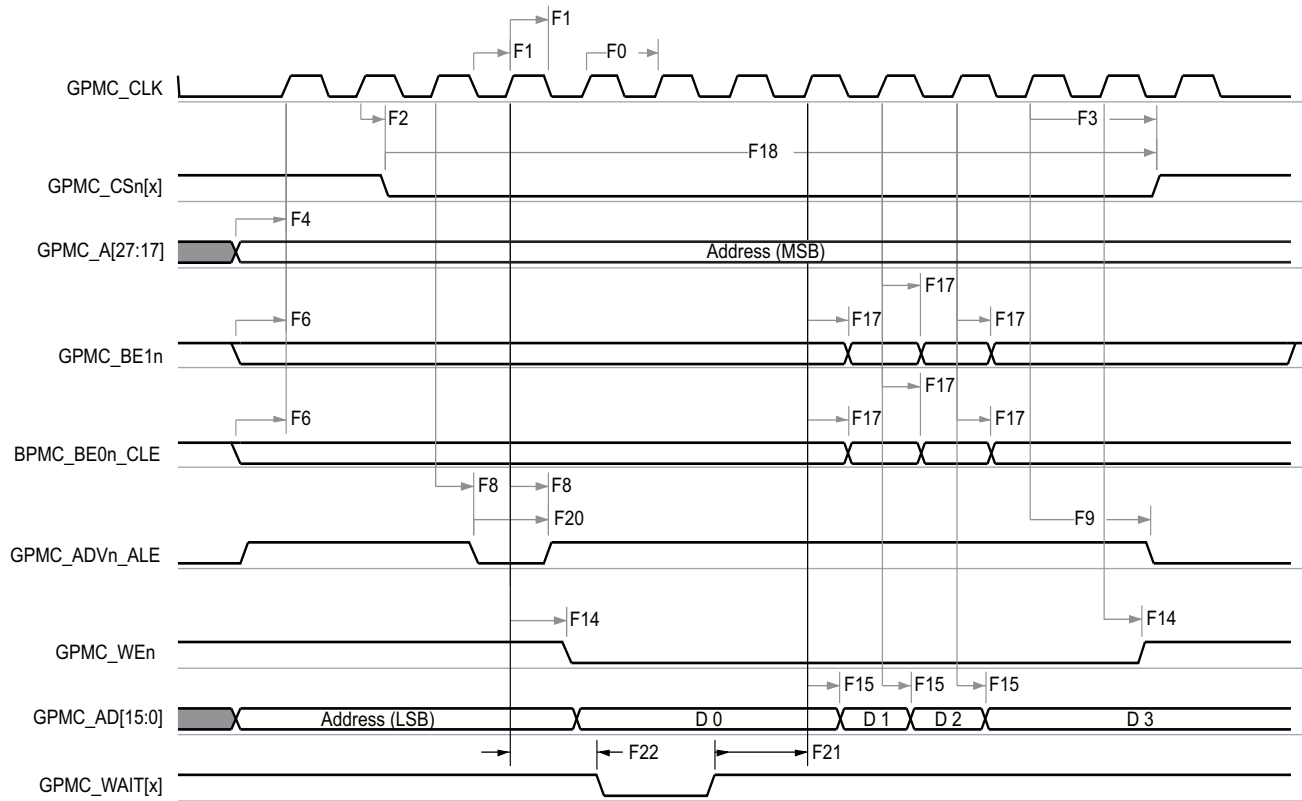
- A. In GPMC_CSn[x], x is equal to 0, 1, 2 or 3.
- B. In GPMC_WAIT[x], x is equal to 0 or 1.

图 5-44. GPMC and NOR Flash—Synchronous Burst Write—(GpmcFCLKDivider > 0)



- A. In GPMC_CS[n], x is equal to 0, 1, 2 or 3.
B. In GPMC_WAIT[x], x is equal to 0 or 1.

5-45. GPMC and Multiplexed NOR Flash—Synchronous Burst Read



GPMC_05

- A. In GPMC_CS[n], x is equal to 0, 1, 2 or 3.
B. In GPMC_WAIT[x], x is equal to 0 or 1.

图 5-46. GPMC and Multiplexed NOR Flash—Synchronous Burst Write

5.9.5.10.2 GPMC and NOR Flash—Asynchronous Mode

表 5-50 和 表 5-51 假设测试 over 的 recommended operating conditions 和 electrical characteristic conditions below (see 图 5-47 through 图 5-52).

表 5-50. GPMC and NOR Flash Timing Requirements—Asynchronous Mode

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
FA5 ⁽¹⁾	$t_{acc(d)}$	Data access time	div_by_1_mode; GPMC_FCLK_MUX_133; TIMEPARAGRANULARITY_X1		H ⁽⁵⁾	ns
FA20 ⁽²⁾	$t_{acc1-pgmode(d)}$	Page mode successive data access time	div_by_1_mode; GPMC_FCLK_MUX_133; TIMEPARAGRANULARITY_X1		P ⁽⁴⁾	ns
FA21 ⁽¹⁾	$t_{acc2-pgmode(d)}$	Page mode first data access time	div_by_1_mode; GPMC_FCLK_MUX_133; TIMEPARAGRANULARITY_X1		H ⁽⁵⁾	ns

- (1) The FA5 parameter illustrates the amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data is internally sampled by active functional clock edge. FA5 value must be stored inside the AccessTime register bit field.
- (2) The FA20 parameter illustrates amount of time required to internally sample successive input page data. It is expressed in number of GPMC functional clock cycles. After each access to input page data, next input page data is internally sampled by active functional clock edge after FA20 functional clock cycles. The FA20 value must be stored in the PageBurstAccessTime register bit field.
- (3) The FA21 parameter illustrates amount of time required to internally sample first input page data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA21 functional clock cycles, first input page data is internally sampled by active functional clock edge. FA21 value must be stored inside the AccessTime register bit field.
- (4) $P = \text{PageBurstAccessTime} \times (\text{TimeParaGranularity} + 1) \times \text{GPMC_FCLK}^{(6)}$
- (5) $H = \text{AccessTime} \times (\text{TimeParaGranularity} + 1) \times \text{GPMC_FCLK}^{(6)}$

(6) GPMC_FCLK is general-purpose memory controller internal functional clock period in ns.

(7) For div_by_1_mode:

- GPMC_CONFIG1_i Register: GPMCCLKDIVIDER = 0h:
- GPMC_CLK frequency = GPMC_FCLK frequency

For GPMC_FCLK_MUX_133:

- gpmc_fclk_sel[1:0] = 00 = CPSWHS DIV_CLKOUT3 = 2000/15 = 133.33 MHz

For TIMEPARAGRANULARITY_X1:

- GPMC_CONFIG1_i Register: TIMEPARAGRANULARITY = 0h = x1 latencies (affecting RD/WRCYCLETIME, RD/WRACCESTIME, PAGEBURSTACCESTIME, CSONTIME, CSRD/WROFFTIME, ADVONTIME, ADVRD/WROFFTIME, OEONTIME, OEOFFTIME, WEONTIME, WEOFFTIME, CYCLE2CYCLEDELAY, BUSTURNAROUND, TIMEOUTSTARTVALUE, WRDATAONADMUXBUS)

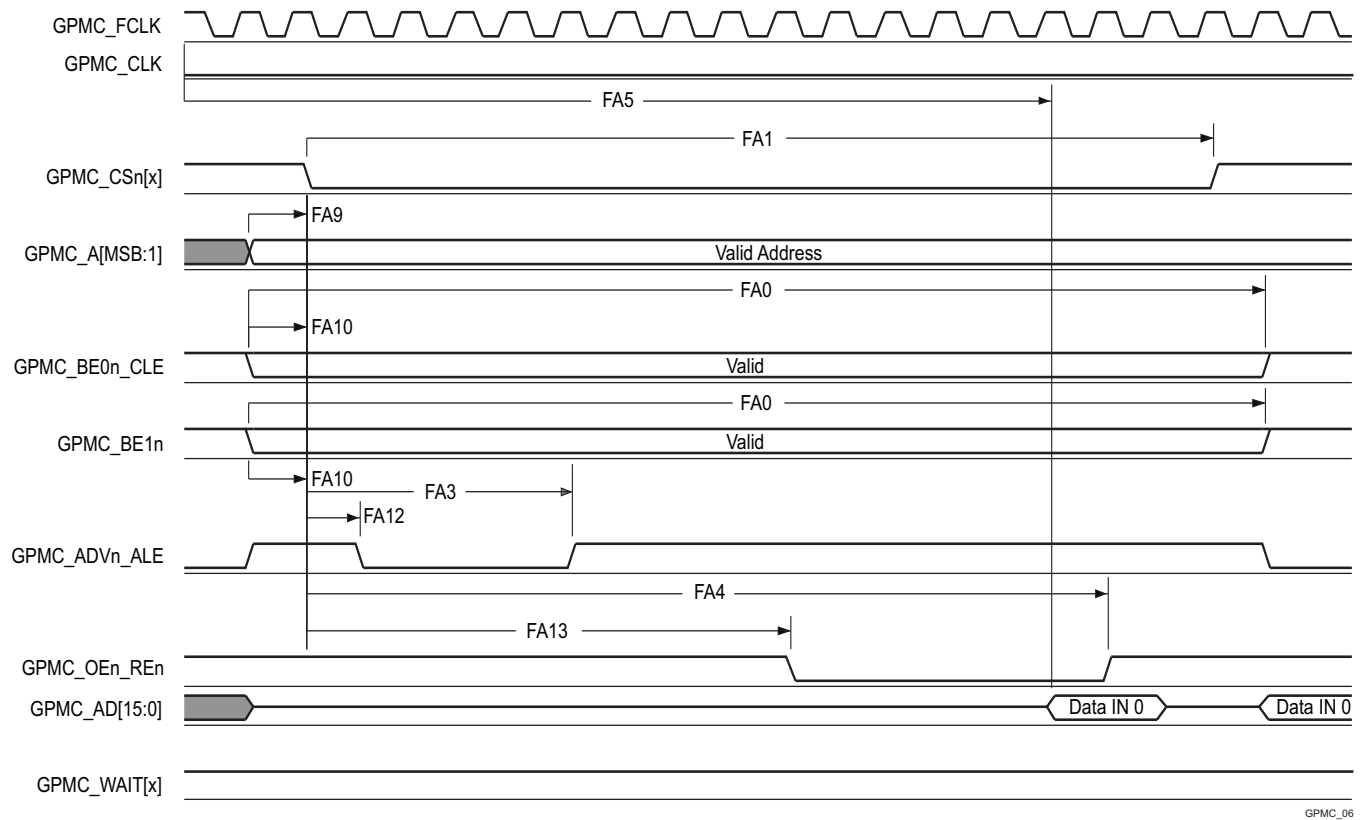
表 5-51. GPMC and NOR Flash Switching Characteristics—Asynchronous Mode

NO.	PARAMETER	DESCRIPTION	MODE ⁽¹⁹⁾	MIN	MAX	UNIT
	$t_{R(d)}$	Rise time, output data GPMC_AD[15:0]	div_by_1_mode; GPMC_FCLK_MUX_133; TIMEPARAGRANULARITY_X1	2		ns
	$t_{F(d)}$	Fall time, output data GPMC_AD[15:0]	div_by_1_mode; GPMC_FCLK_MUX_133; TIMEPARAGRANULARITY_X1	2		ns
FA0	$t_{w(be x nV)}$	Pulse duration, output lower-byte enable and command latch enable GPMC_BE0n_CLE, output upper-byte enable GPMC_BE1n valid time	Read	N ⁽¹²⁾		ns
			Write	N ⁽¹²⁾		
FA1	$t_{w(csnV)}$	Pulse duration, output chip select GPMC_CS[n] ⁽¹³⁾ low	Read	A ⁽¹⁾		ns
			Write	A ⁽¹⁾		
FA3	$t_{d(csnV-advnIV)}$	Delay time, output chip select GPMC_CS[n] ⁽¹³⁾ valid to output address valid and address latch enable GPMC_ADVn_ALE invalid	Read	-2+B ⁽²⁾	2+B ⁽²⁾	ns
			Write	-2+B ⁽²⁾	2+B ⁽²⁾	
FA4	$t_{d(csnV-oenIV)}$	Delay time, output chip select GPMC_CS[n] ⁽¹³⁾ valid to output enable GPMC_OEn_REn invalid (Single read)	div_by_1_mode; GPMC_FCLK_MUX_133; TIMEPARAGRANULARITY_X1	-2+C ⁽³⁾	2+C ⁽³⁾	ns
FA9	$t_{d(aV-csnV)}$	Delay time, output address GPMC_A[27:1] valid to output chip select GPMC_CS[n] ⁽¹³⁾ valid	div_by_1_mode; GPMC_FCLK_MUX_133; TIMEPARAGRANULARITY_X1	-2+J ⁽⁹⁾	2+J ⁽⁹⁾	ns
FA10	$t_{d(be x nV-csnV)}$	Delay time, output lower-byte enable and command latch enable GPMC_BE0n_CLE, output upper-byte enable GPMC_BE1n valid to output chip select GPMC_CS[n] ⁽¹³⁾ valid	div_by_1_mode; GPMC_FCLK_MUX_133; TIMEPARAGRANULARITY_X1	-2+J ⁽⁹⁾	2+J ⁽⁹⁾	ns
FA12	$t_{d(csnV-advnV)}$	Delay time, output chip select GPMC_CS[n] ⁽¹³⁾ valid to output address valid and address latch enable GPMC_ADVn_ALE valid	div_by_1_mode; GPMC_FCLK_MUX_133; TIMEPARAGRANULARITY_X1	-2+K ⁽¹⁰⁾	2+K ⁽¹⁰⁾	ns
FA13	$t_{d(csnV-oenV)}$	Delay time, output chip select GPMC_CS[n] ⁽¹³⁾ valid to output enable GPMC_OEn_REn valid	div_by_1_mode; GPMC_FCLK_MUX_133; TIMEPARAGRANULARITY_X1	-2+L ⁽¹¹⁾	2+L ⁽¹¹⁾	ns
FA16	$t_{w(aIV)}$	Pulse duration output address GPMC_A[26:1] invalid between 2 successive read and write accesses	div_by_1_mode; GPMC_FCLK_MUX_133; TIMEPARAGRANULARITY_X1	G ⁽⁷⁾		ns
FA18	$t_{d(csnV-oenIV)}$	Delay time, output chip select GPMC_CS[n] ⁽¹³⁾ valid to output enable GPMC_OEn_REn invalid (Burst read)	div_by_1_mode; GPMC_FCLK_MUX_133; TIMEPARAGRANULARITY_X1	-2+I ⁽⁸⁾	2+I ⁽⁸⁾	ns
FA20	$t_{w(aV)}$	Pulse duration, output address GPMC_A[27:1] valid - 2nd, 3rd, and 4th accesses	div_by_1_mode; GPMC_FCLK_MUX_133; TIMEPARAGRANULARITY_X1	D ⁽⁴⁾		ns
FA25	$t_{d(csnV-wenV)}$	Delay time, output chip select GPMC_CS[n] ⁽¹³⁾ valid to output write enable GPMC_WEn valid	div_by_1_mode; GPMC_FCLK_MUX_133; TIMEPARAGRANULARITY_X1	-2+E ⁽⁵⁾	2+E ⁽⁵⁾	ns
FA27	$t_{d(csnV-wenIV)}$	Delay time, output chip select GPMC_CS[n] ⁽¹³⁾ valid to output write enable GPMC_WEn invalid	div_by_1_mode; GPMC_FCLK_MUX_133; TIMEPARAGRANULARITY_X1	-2+F ⁽⁶⁾	2+F ⁽⁶⁾	ns

表 5-51. GPMC and NOR Flash Switching Characteristics—Asynchronous Mode (continued)

NO.	PARAMETER	DESCRIPTION	MODE ⁽¹⁵⁾	MIN	MAX	UNIT
FA28	$t_{d(wenV-dv)}$	Delay time, output write enable GPMC_WEn valid to output data GPMC_AD[15:0] valid	div_by_1_mode; GPMC_FCLK_MUX_133; TIMEPARAGRANULARITY_X1		2.8	ns
FA29	$t_{d(dV-csnV)}$	Delay time, output data GPMC_AD[15:0] valid to output chip select GPMC_CSn[x] ⁽¹³⁾ valid	div_by_1_mode; GPMC_FCLK_MUX_133; TIMEPARAGRANULARITY_X1	-2+J ⁽⁹⁾	2+J ⁽⁹⁾	ns
FA37	$t_{d(oenV-alV)}$	Delay time, output enable GPMC_OEn_REn valid to output address GPMC_AD[15:0] phase end	div_by_1_mode; GPMC_FCLK_MUX_133; TIMEPARAGRANULARITY_X1		2.8	ns

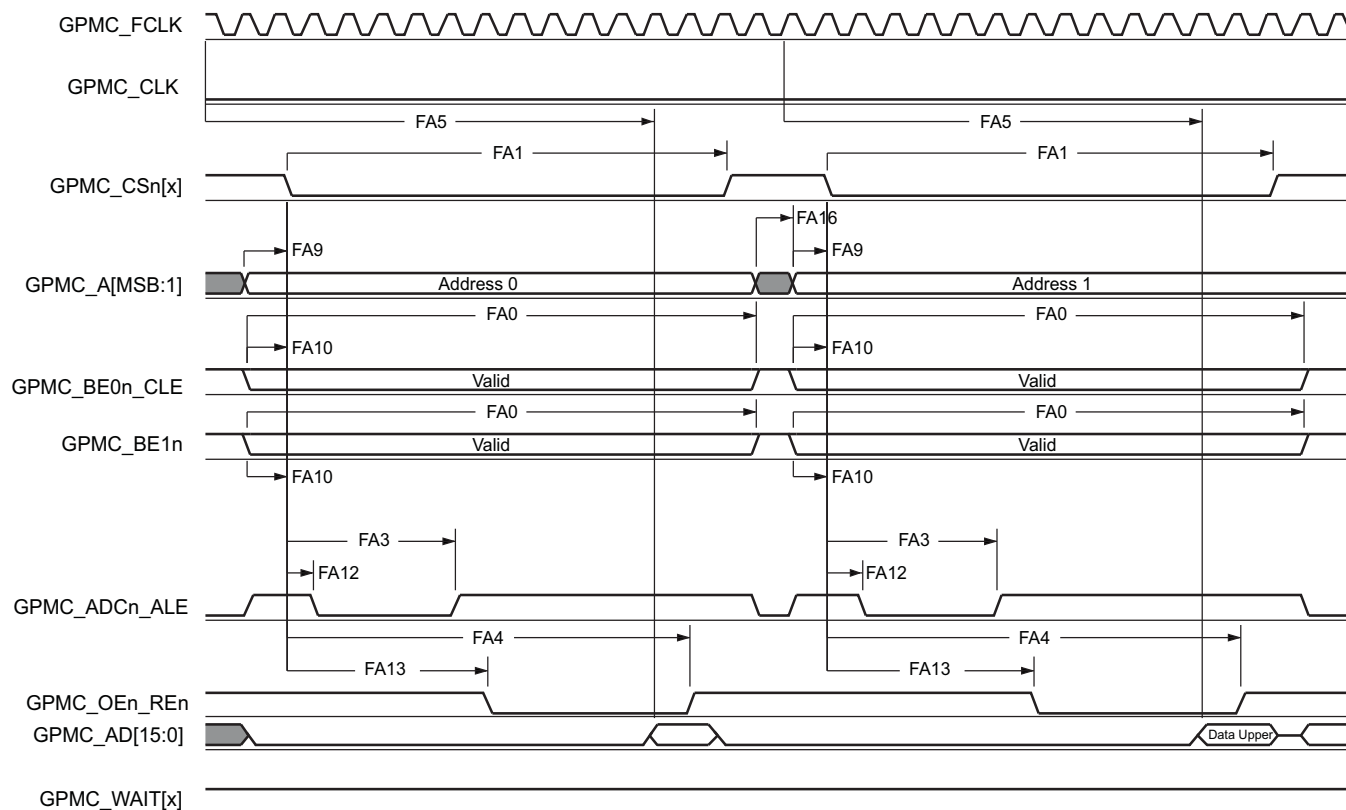
- (1) For single read: $A = (CSRdOffTime - CSOnTime) \times (TimeParaGranularity + 1) \times GPMC_FCLK^{(14)}$
 For single write: $A = (CSWrOffTime - CSOnTime) \times (TimeParaGranularity + 1) \times GPMC_FCLK^{(14)}$
 For burst read: $A = (CSRdOffTime - CSOnTime + (n - 1) \times PageBurstAccessTime) \times (TimeParaGranularity + 1) \times GPMC_FCLK^{(14)}$
 For burst write: $A = (CSWrOffTime - CSOnTime + (n - 1) \times PageBurstAccessTime) \times (TimeParaGranularity + 1) \times GPMC_FCLK^{(14)}$
 with n being the page burst access number
- (2) For reading: $B = ((ADVrOffTime - CSOnTime) \times (TimeParaGranularity + 1) + 0.5 \times (ADVExtraDelay - CSEExtraDelay)) \times GPMC_FCLK^{(14)}$
 For writing: $B = ((ADVWrOffTime - CSOnTime) \times (TimeParaGranularity + 1) + 0.5 \times (ADVExtraDelay - CSEExtraDelay)) \times GPMC_FCLK^{(14)}$
- (3) $C = ((OEOffTime - CSOnTime) \times (TimeParaGranularity + 1) + 0.5 \times (OEExtraDelay - CSEExtraDelay)) \times GPMC_FCLK^{(14)}$
- (4) $D = PageBurstAccessTime \times (TimeParaGranularity + 1) \times GPMC_FCLK^{(14)}$
- (5) $E = ((WEOnTime - CSOnTime) \times (TimeParaGranularity + 1) + 0.5 \times (WEExtraDelay - CSEExtraDelay)) \times GPMC_FCLK^{(14)}$
- (6) $F = ((WEOffTime - CSOnTime) \times (TimeParaGranularity + 1) + 0.5 \times (WEExtraDelay - CSEExtraDelay)) \times GPMC_FCLK^{(14)}$
- (7) $G = Cycle2CycleDelay \times GPMC_FCLK^{(14)}$
- (8) $I = ((OEOffTime + (n - 1) \times PageBurstAccessTime - CSOnTime) \times (TimeParaGranularity + 1) + 0.5 \times (OEExtraDelay - CSEExtraDelay)) \times GPMC_FCLK^{(14)}$
- (9) $J = (CSOnTime \times (TimeParaGranularity + 1) + 0.5 \times CSEExtraDelay) \times GPMC_FCLK^{(14)}$
- (10) $K = ((ADVOnTime - CSOnTime) \times (TimeParaGranularity + 1) + 0.5 \times (ADVExtraDelay - CSEExtraDelay)) \times GPMC_FCLK^{(14)}$
- (11) $L = ((OEOnTime - CSOnTime) \times (TimeParaGranularity + 1) + 0.5 \times (OEExtraDelay - CSEExtraDelay)) \times GPMC_FCLK^{(14)}$
- (12) For single read: $N = RdCycleTime \times (TimeParaGranularity + 1) \times GPMC_FCLK^{(14)}$
 For single write: $N = WrCycleTime \times (TimeParaGranularity + 1) \times GPMC_FCLK^{(14)}$
 For burst read: $N = (RdCycleTime + (n - 1) \times PageBurstAccessTime) \times (TimeParaGranularity + 1) \times GPMC_FCLK^{(14)}$
 For burst write: $N = (WrCycleTime + (n - 1) \times PageBurstAccessTime) \times (TimeParaGranularity + 1) \times GPMC_FCLK^{(14)}$
- (13) In GPMC_CSn[x], x is equal to 0, 1, 2 or 3.
- (14) GPMC_FCLK is general-purpose memory controller internal functional clock period in ns.
- (15) For div_by_1_mode:
- GPMC_CONFIG1_i Register: GPMCFCLKDIVIDER = 0h:
 - GPMC_CLK frequency = GPMC_FCLK frequency
- For GPMC_FCLK_MUX_133:
- gpmc_fclk_sel[1:0] = 00 = CPSWHS DIV_CLKOUT3 = 2000/15 = 133.33 MHz
- For TIMEPARAGRANULARITY_X1:
- GPMC_CONFIG1_i Register: TIMEPARAGRANULARITY = 0h = x1 latencies (affecting RD/WRCYCLETIME, RD/WRACCESTIME, PAGEBURSTACCESTIME, CSONTIME, CSRd/WROFFTIME, ADVONTIME, ADVRD/WROFFTIME, OEONTIME, OEOffTIME, WEONTIME, WEOffTIME, CYCLE2CYCLEDELAY, BUSTURNAROUND, TIMEOUTSTARTVALUE, WRDATAONADMUXBUS)



GPMC_06

- In **GPMC_CS[x]**, x is equal to 0, 1, 2 or 3. In **GPMC_WAIT[x]**, x is equal to 0 or 1.
- FA5** parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after **FA5** functional clock cycles, input data will be internally sampled by active functional clock edge. **FA5** value must be stored inside AccessTime register bits field.
- GPMC_FCLK** is an internal clock (GPMC functional clock) not provided externally.

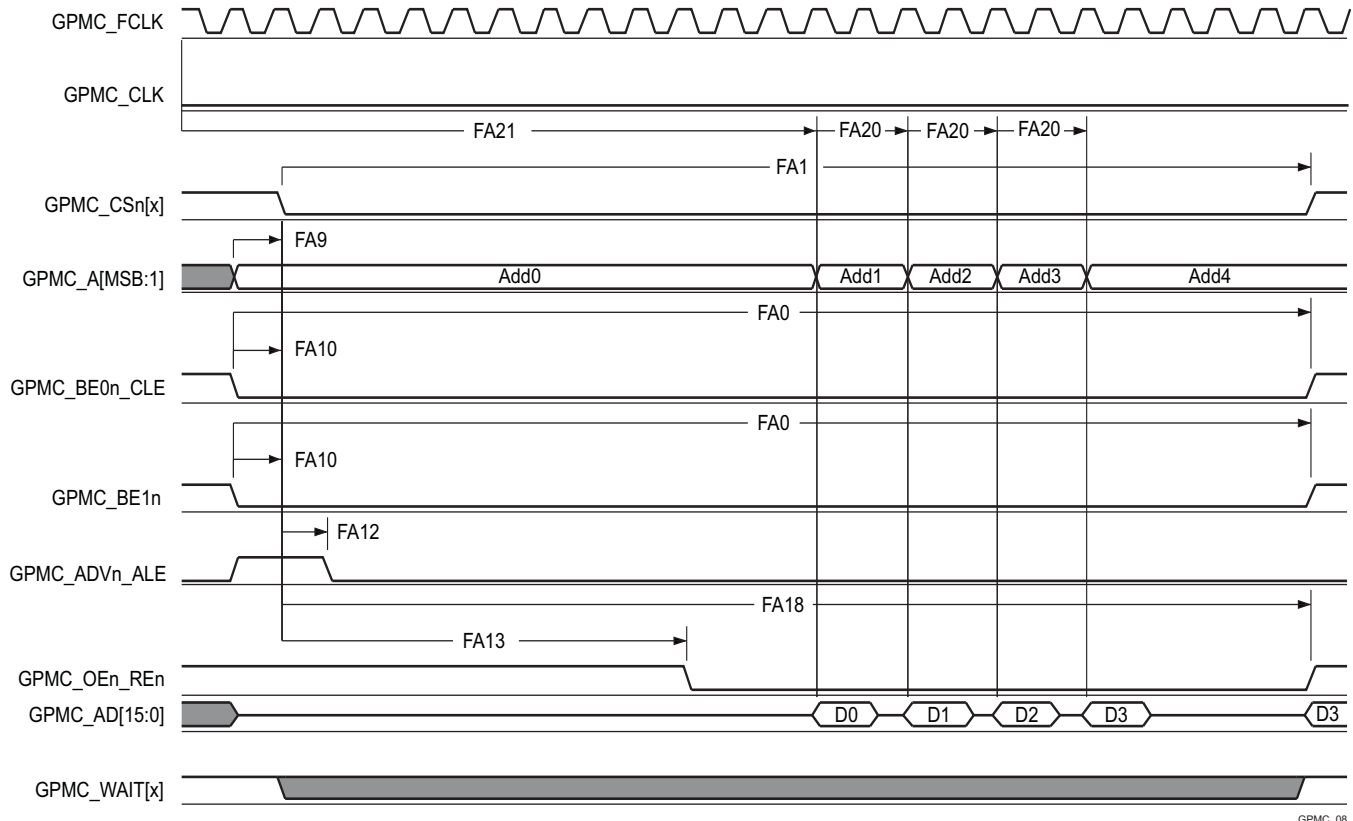
图 5-47. GPMC and NOR Flash—Asynchronous Read—Single Word



GPMC_07

- In GPMC_CS[n], x is equal to 0, 1, 2 or 3. In GPMC_WAIT[x], x is equal to 0 or 1.
- FA5 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data will be internally sampled by active functional clock edge. FA5 value must be stored inside AccessTime register bits field.
- GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.

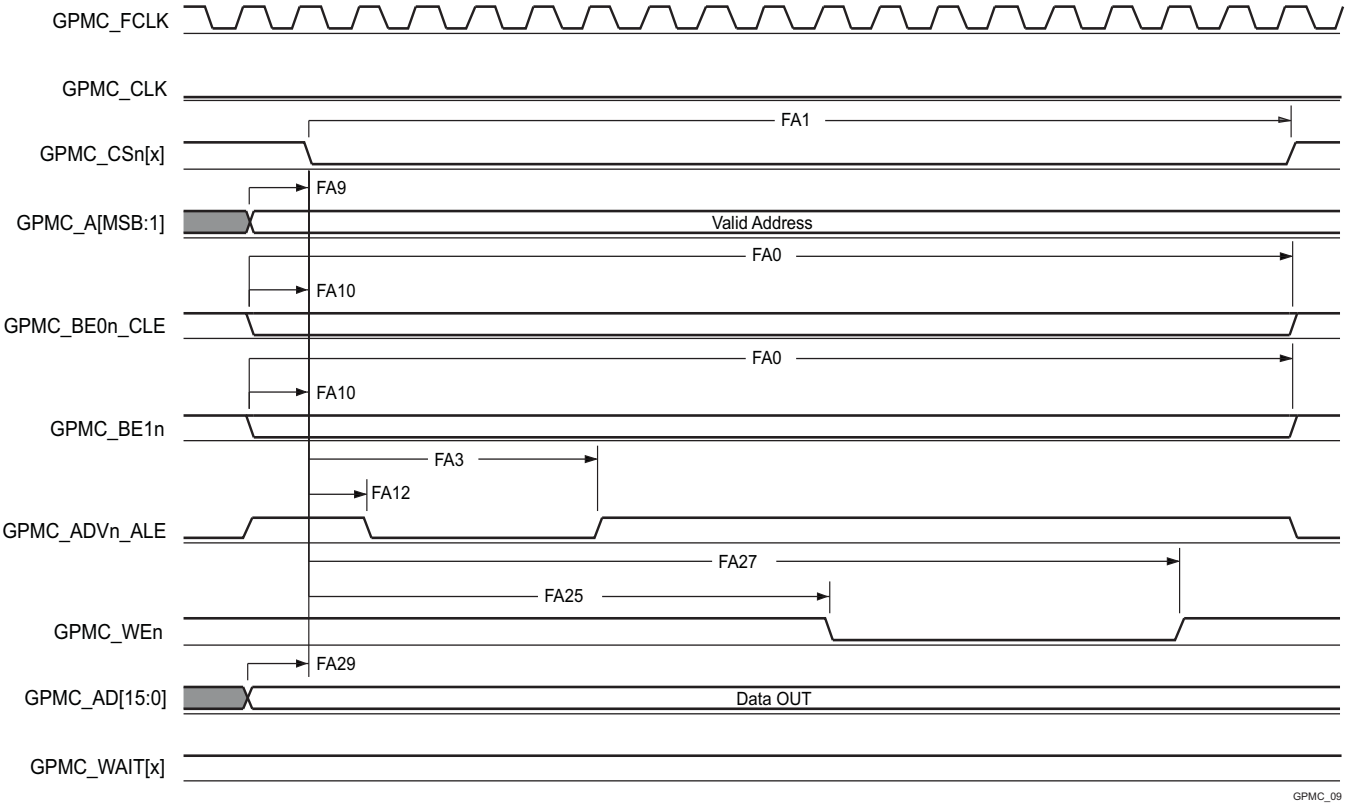
图 5-48. GPMC and NOR Flash—Asynchronous Read—32-Bit



GPMC_08

- In GPMC_CS[n], x is equal to 0, 1, 2 or 3. In GPMC_WAIT[x], x is equal to 0 or 1.
- FA21 parameter illustrates amount of time required to internally sample first input page data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA21 functional clock cycles, first input page data will be internally sampled by active functional clock edge. FA21 calculation must be stored inside AccessTime register bits field.
- FA20 parameter illustrates amount of time required to internally sample successive input page data. It is expressed in number of GPMC functional clock cycles. After each access to input page data, next input page data will be internally sampled by active functional clock edge after FA20 functional clock cycles. FA20 is also the duration of address phases for successive input page data (excluding first input page data). FA20 value must be stored in PageBurstAccessTime register bits field.
- GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.

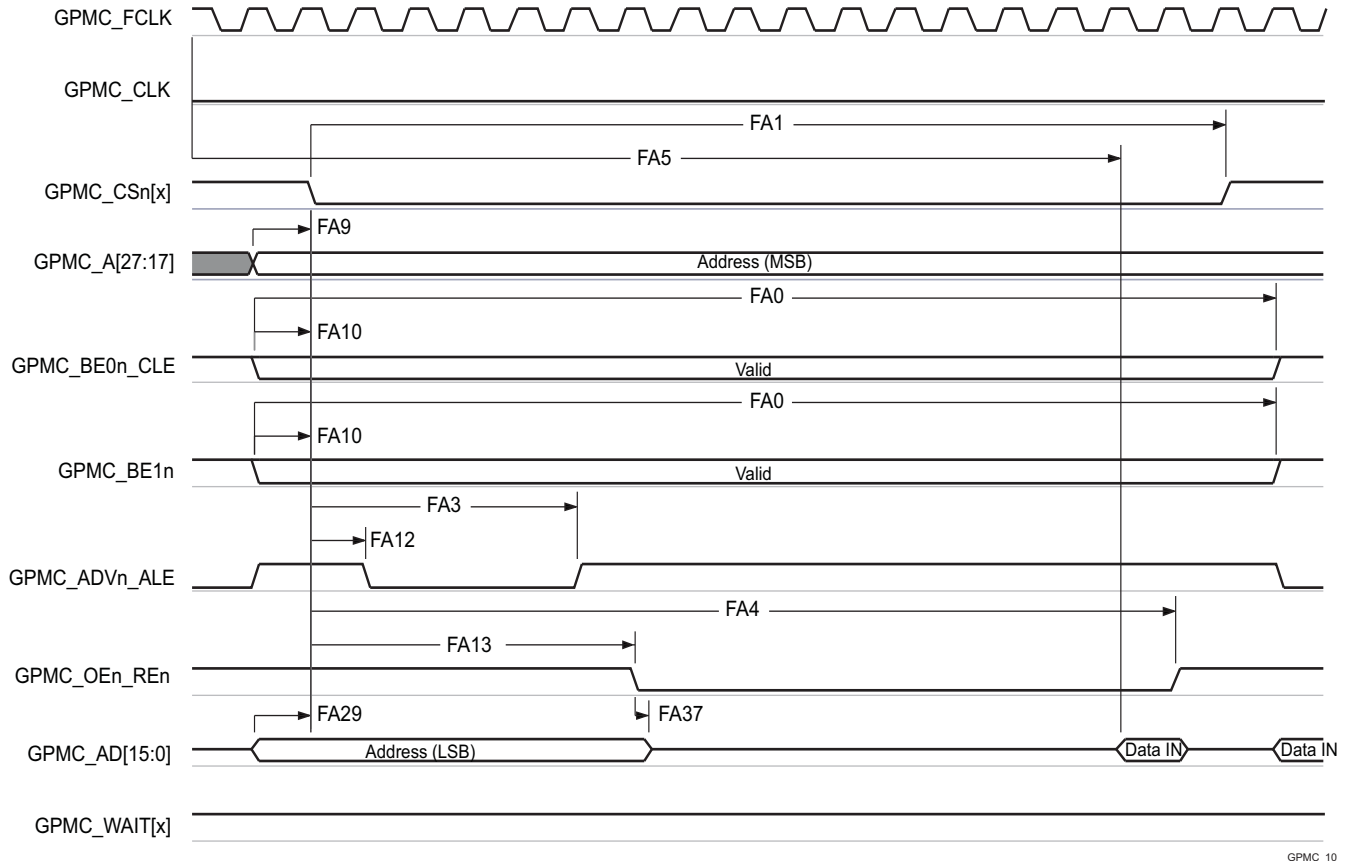
图 5-49. GPMC and NOR Flash—Asynchronous Read—Page Mode 4x16-Bit



A. In GPMC_CS[x], x is equal to 0, 1, 2 or 3. In GPMC_WAIT[x], x is equal to 0 or 1.

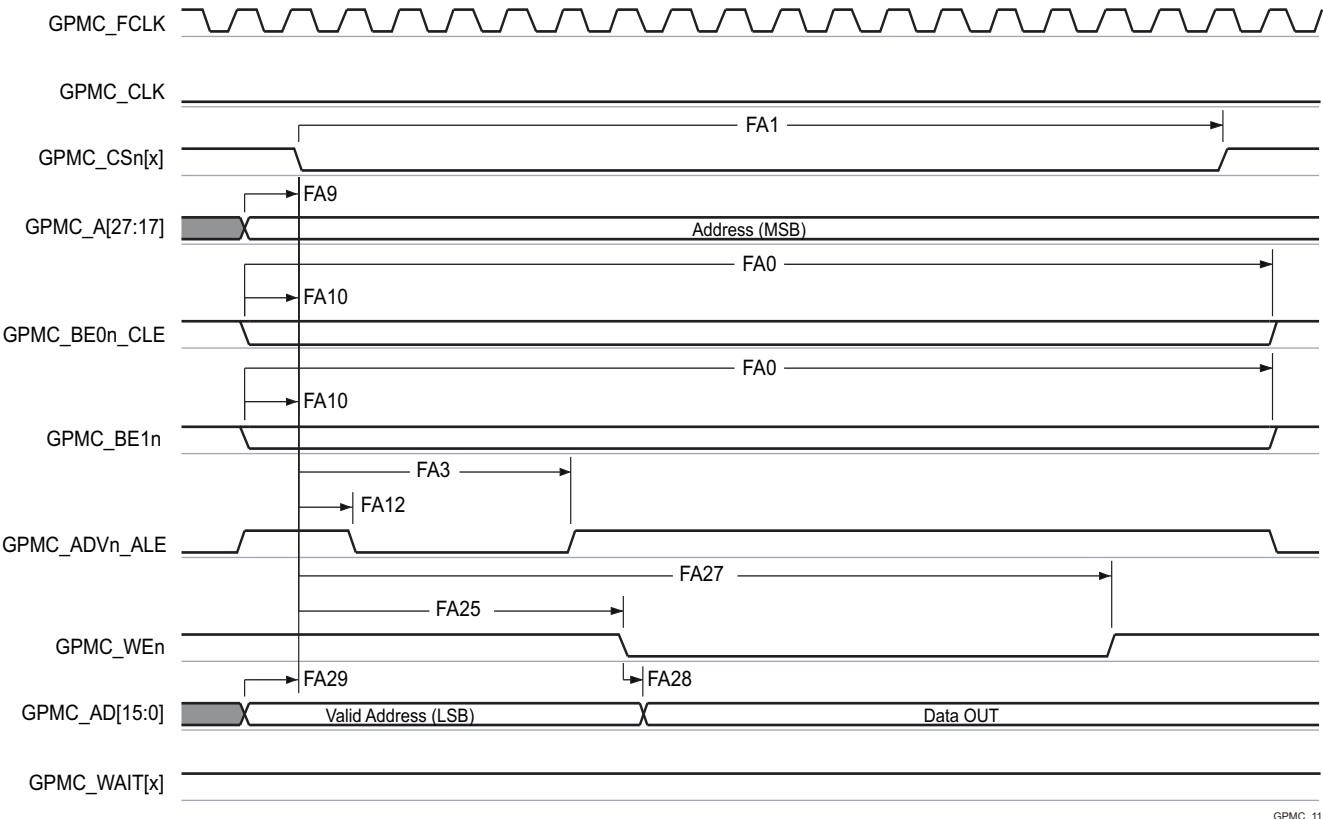
✎ 5-50. GPMC and NOR Flash—Asynchronous Write—Single Word

ADVANCE INFORMATION



- In GPMC_CS[x], x is equal to 0, 1, 2 or 3. In GPMC_WAIT[x], x is equal to 0 or 1.
- FA5 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data will be internally sampled by active functional clock edge. FA5 value must be stored inside AccessTime register bits field.
- GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.

图 5-51. GPMC and Multiplexed NOR Flash—Asynchronous Read—Single Word



A. In GPMC_CS[n], x is equal to 0, 1, 2 or 3. In GPMC_WAIT[x], x is equal to 0 or 1.

✎ 5-52. GPMC and Multiplexed NOR Flash—Asynchronous Write—Single Word

5.9.5.10.3 GPMC and NAND Flash—Asynchronous Mode

表 5-52 和 表 5-53 assume testing over the recommended operating conditions and electrical characteristic conditions below (see 图 5-53 through 图 5-56).

表 5-52. GPMC and NAND Flash Timing Requirements—Asynchronous Mode

NO.	PARAMETER	DESCRIPTION	MODE ⁽⁴⁾	MIN	MAX	UNIT
GNF12 ⁽¹⁾	t _{acc(d)}	Access time, input data GPMC_AD[15:0] ⁽³⁾	div_by_1_mode; GPMC_FCLK_MUX_133; TIMEPARAGRANULARITY_X1		J ⁽²⁾	ns

(1) The GNF12 parameter illustrates the amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of the read cycle and after GNF12 functional clock cycles, input data is internally sampled by the active functional clock edge. The GNF12 value must be stored inside AccessTime register bit field.

(2) J = AccessTime × (TimeParaGranularity + 1) × GPMC_FCLK⁽³⁾

(3) GPMC_FCLK is general-purpose memory controller internal functional clock period in ns.

(4) For div_by_1_mode:

- GPMC_CONFIG1_i Register: GPMCFCLKDIVIDER = 0h;
- GPMC_CLK frequency = GPMC_FCLK frequency

For GPMC_FCLK_MUX_133:

- gpmc_fclk_sel[1:0] = 00 = CPSWHS DIV_CLKOUT3 = 2000/15 = 133.33 MHz

For TIMEPARAGRANULARITY_X1:

- GPMC_CONFIG1_i Register: TIMEPARAGRANULARITY = 0h = x1 latencies (affecting RD/WRCYCLETIME, RD/WRACCESTIME, PAGEBURSTACCESTIME, CSONTIME, CSRD/WROFFTIME, ADVONTIME, ADVRD/WROFFTIME, OEONTIME, OEOFFTIME, WEONTIME, WEOFFTIME, CYCLE2CYCLEDELAY, BUSTURNAROUND, TIMEOUTSTARTVALUE, WRDATAONADMUXBUS)

表 5-53. GPMC and NAND Flash Switching Characteristics—Asynchronous Mode

NO.	PARAMETER	DESCRIPTION	MODE ⁽¹⁵⁾	MIN	MAX	UNIT
	t _{R(d)}	Rise time, output data GPMC_AD[15:0]	div_by_1_mode; GPMC_FCLK_MUX_133; TIMEPARAGRANULARITY_X1		2	ns
	t _{F(d)}	Fall time, output data GPMC_AD[15:0]	div_by_1_mode; GPMC_FCLK_MUX_133; TIMEPARAGRANULARITY_X1		2	ns
GNF0	t _{w(wenV)}	Pulse duration, output write enable GPMC_WEn valid	div_by_1_mode; GPMC_FCLK_MUX_133; TIMEPARAGRANULARITY_X1	A ⁽¹⁾		ns
GNF1	t _{d(csnV-wenV)}	Delay time, output chip select GPMC_CS[n] ⁽¹³⁾ valid to output write enable GPMC_WEn valid	div_by_1_mode; GPMC_FCLK_MUX_133; TIMEPARAGRANULARITY_X1	-2+B ⁽²⁾	2+B ⁽²⁾	ns
GNF2	t _{w(cleH-wenV)}	Delay time, output lower-byte enable and command latch enable GPMC_BE0n_CLE high to output write enable GPMC_WEn valid	div_by_1_mode; GPMC_FCLK_MUX_133; TIMEPARAGRANULARITY_X1	-2+C ⁽³⁾	2+C ⁽³⁾	ns
GNF3	t _{w(wenV-dV)}	Delay time, output data GPMC_AD[15:0] valid to output write enable GPMC_WEn valid	div_by_1_mode; GPMC_FCLK_MUX_133; TIMEPARAGRANULARITY_X1	-2+D ⁽⁴⁾	2.8+D ⁽⁴⁾	ns
GNF4	t _{w(wenIV-dIV)}	Delay time, output write enable GPMC_WEn invalid to output data GPMC_AD[15:0] invalid	div_by_1_mode; GPMC_FCLK_MUX_133; TIMEPARAGRANULARITY_X1	-2+E ⁽⁵⁾	2.8+E ⁽⁵⁾	ns
GNF5	t _{w(wenIV-cleIV)}	Delay time, output write enable GPMC_WEn invalid to output lower-byte enable and command latch enable GPMC_BE0n_CLE invalid	div_by_1_mode; GPMC_FCLK_MUX_133; TIMEPARAGRANULARITY_X1	-2+F ⁽⁶⁾	2+F ⁽⁶⁾	ns
GNF6	t _{w(wenIV-csnIV)}	Delay time, output write enable GPMC_WEn invalid to output chip select GPMC_CS[n] ⁽¹³⁾ invalid	div_by_1_mode; GPMC_FCLK_MUX_133; TIMEPARAGRANULARITY_X1	-2+G ⁽⁷⁾	2+G ⁽⁷⁾	ns
GNF7	t _{w(aleH-wenV)}	Delay time, output address valid and address latch enable GPMC_ADVn_ALE high to output write enable GPMC_WEn valid	div_by_1_mode; GPMC_FCLK_MUX_133; TIMEPARAGRANULARITY_X1	-2+C ⁽³⁾	2+C ⁽³⁾	ns

表 5-53. GPMC and NAND Flash Switching Characteristics—Asynchronous Mode (continued)

NO.	PARAMETER		MODE ⁽¹⁵⁾	MIN	MAX	UNIT
GNF8	$t_{w(wenIV-aleIV)}$	Delay time, output write enable GPMC_WEn invalid to output address valid and address latch enable GPMC_ADVn_ALE invalid	div_by_1_mode; GPMC_FCLK_MUX_133; TIMEPARAGRANULARITY_X1	-2+F ⁽⁶⁾	2+F ⁽⁶⁾	ns
GNF9	$t_{c(wen)}$	Cycle time, write	div_by_1_mode; GPMC_FCLK_MUX_133; TIMEPARAGRANULARITY_X1		H ⁽⁸⁾	ns
GNF10	$t_{d(csnV-oenV)}$	Delay time, output chip select GPMC_CS[n] ⁽¹³⁾ valid to output enable GPMC_OEn_REn valid	div_by_1_mode; GPMC_FCLK_MUX_133; TIMEPARAGRANULARITY_X1	-2+I ⁽⁹⁾	2+I ⁽⁹⁾	ns
GNF13	$t_{w(oenV)}$	Pulse duration, output enable GPMC_OEn_REn valid	div_by_1_mode; GPMC_FCLK_MUX_133; TIMEPARAGRANULARITY_X1		K ⁽¹⁰⁾	ns
GNF14	$t_{c(oen)}$	Cycle time, read	div_by_1_mode; GPMC_FCLK_MUX_133; TIMEPARAGRANULARITY_X1	L ⁽¹¹⁾		ns
GNF15	$t_{w(oenIV-csnIV)}$	Delay time, output enable GPMC_OEn_REn invalid to output chip select GPMC_CS[n] ⁽¹³⁾ invalid	div_by_1_mode; GPMC_FCLK_MUX_133; TIMEPARAGRANULARITY_X1	-2+M ⁽¹²⁾	2+M ⁽¹²⁾	ns

(1) $A = (WEOffTime - WEOnTime) \times (TimeParaGranularity + 1) \times GPMC_FCLK^{(14)}$ (2) $B = ((WEOnTime - CSOnTime) \times (TimeParaGranularity + 1) + 0.5 \times (WEEExtraDelay - CSEExtraDelay)) \times GPMC_FCLK^{(14)}$ (3) $C = ((WEOnTime - ADVOnTime) \times (TimeParaGranularity + 1) + 0.5 \times (WEEExtraDelay - ADVExtraDelay)) \times GPMC_FCLK^{(14)}$ (4) $D = (WEOnTime \times (TimeParaGranularity + 1) + 0.5 \times WEEExtraDelay) \times GPMC_FCLK^{(14)}$ (5) $E = ((WrCycleTime - WEOffTime) \times (TimeParaGranularity + 1) - 0.5 \times WEEExtraDelay) \times GPMC_FCLK^{(14)}$ (6) $F = ((ADVWrOffTime - WEOffTime) \times (TimeParaGranularity + 1) + 0.5 \times (ADVExtraDelay - WEEExtraDelay)) \times GPMC_FCLK^{(14)}$ (7) $G = ((CSWrOffTime - WEOffTime) \times (TimeParaGranularity + 1) + 0.5 \times (CSEExtraDelay - WEEExtraDelay)) \times GPMC_FCLK^{(14)}$ (8) $H = WrCycleTime \times (1 + TimeParaGranularity) \times GPMC_FCLK^{(14)}$ (9) $I = ((OEOnTime - CSOnTime) \times (TimeParaGranularity + 1) + 0.5 \times (OEEExtraDelay - CSEExtraDelay)) \times GPMC_FCLK^{(14)}$ (10) $K = (OEOffTime - OEOnTime) \times (1 + TimeParaGranularity) \times GPMC_FCLK^{(14)}$ (11) $L = RdCycleTime \times (1 + TimeParaGranularity) \times GPMC_FCLK^{(14)}$ (12) $M = ((CSRdOffTime - OEOffTime) \times (TimeParaGranularity + 1) + 0.5 \times (CSEExtraDelay - OEEExtraDelay)) \times GPMC_FCLK^{(14)}$

(13) In GPMC_CS[n], x is equal to 0, 1, 2 or 3.

(14) GPMC_FCLK is general-purpose memory controller internal functional clock period in ns.

(15) For div_by_1_mode:

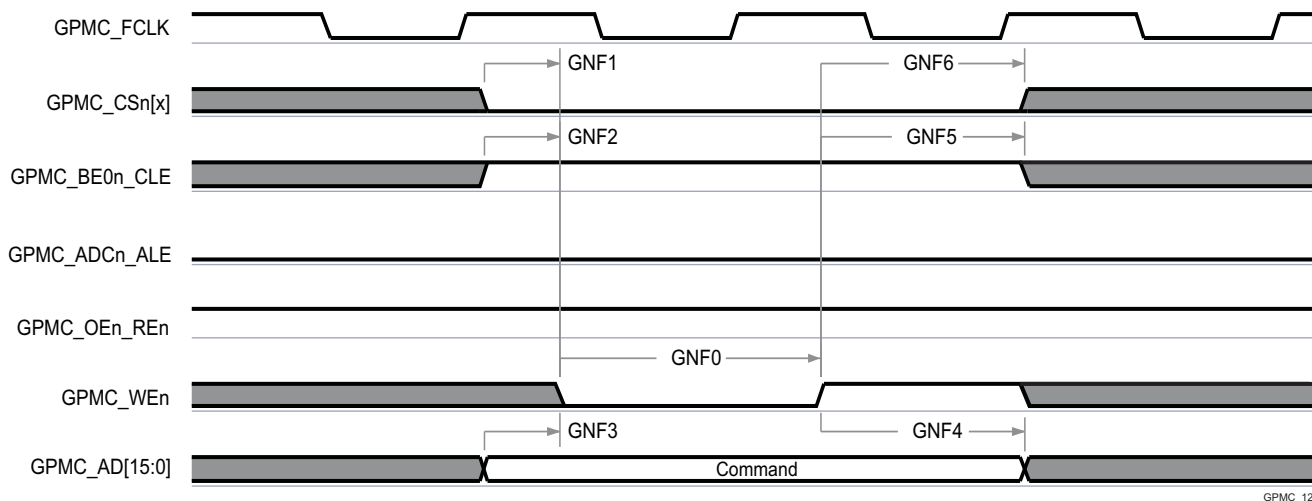
- GPMC_CONFIG1_i Register: GPMCFCLKDIVIDER = 0h:
- GPMC_CLK frequency = GPMC_FCLK frequency

For GPMC_FCLK_MUX_133:

- gpmc_fclk_sel[1:0] = 00 = CPSWHS DIV_CLKOUT3 = 2000/15 = 133.33 MHz

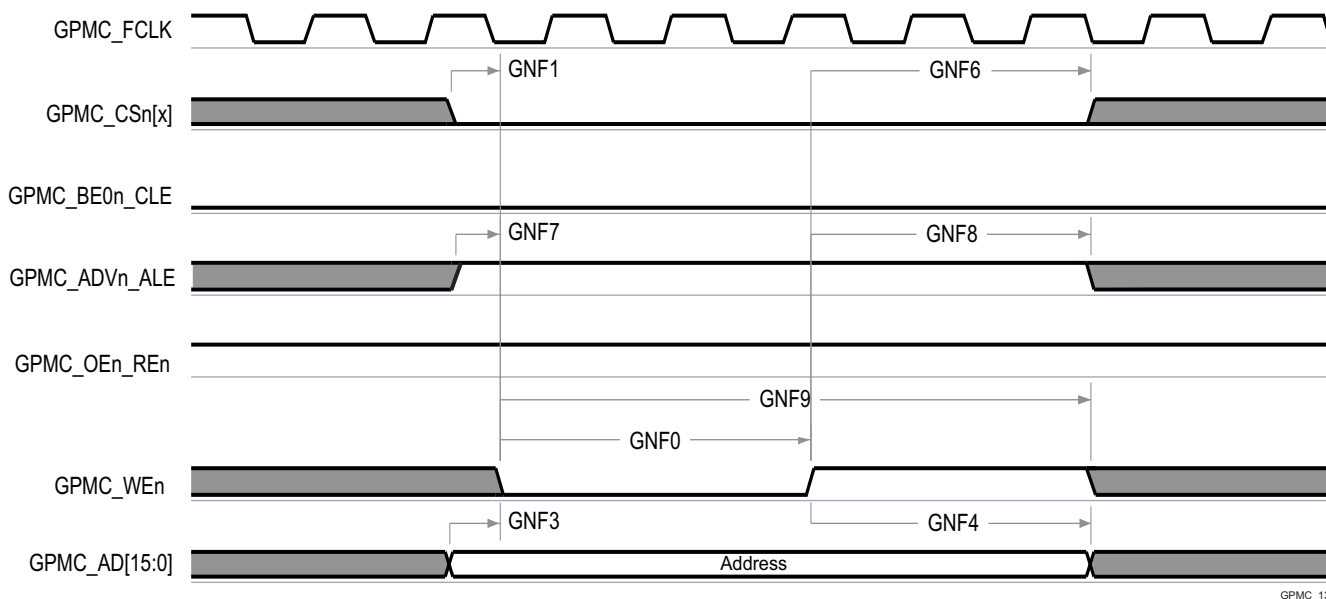
For TIMEPARAGRANULARITY_X1:

- GPMC_CONFIG1_i Register: TIMEPARAGRANULARITY = 0h = x1 latencies (affecting RD/WRCYCLETIME, RD/WRACCESSTIME, PAGEBURSTACCESSTIME, CSONTIME, CSRD/WROFFTIME, ADVONTIME, ADVRD/WROFFTIME, OEONTIME, OEOFFTIME, WEONTIME, WEOFFTIME, CYCLE2CYCLEDELAY, BUSTURNAROUND, TIMEOUTSTARTVALUE, WRDATAONADMUXBUS)



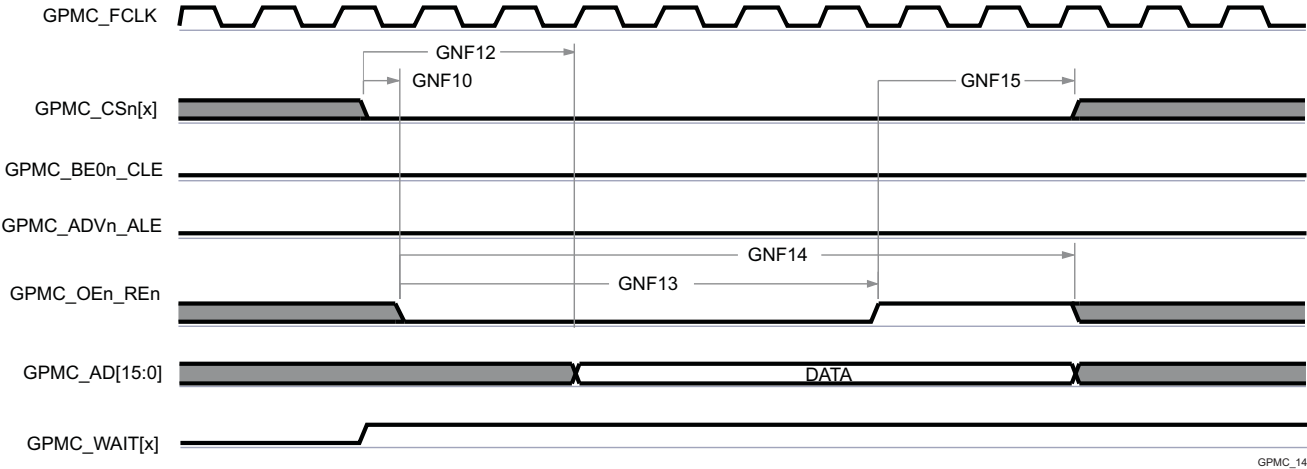
(1) In GPMC_CS[n], x is equal to 0, 1, 2 or 3.

✖ 5-53. GPMC and NAND Flash—Command Latch Cycle



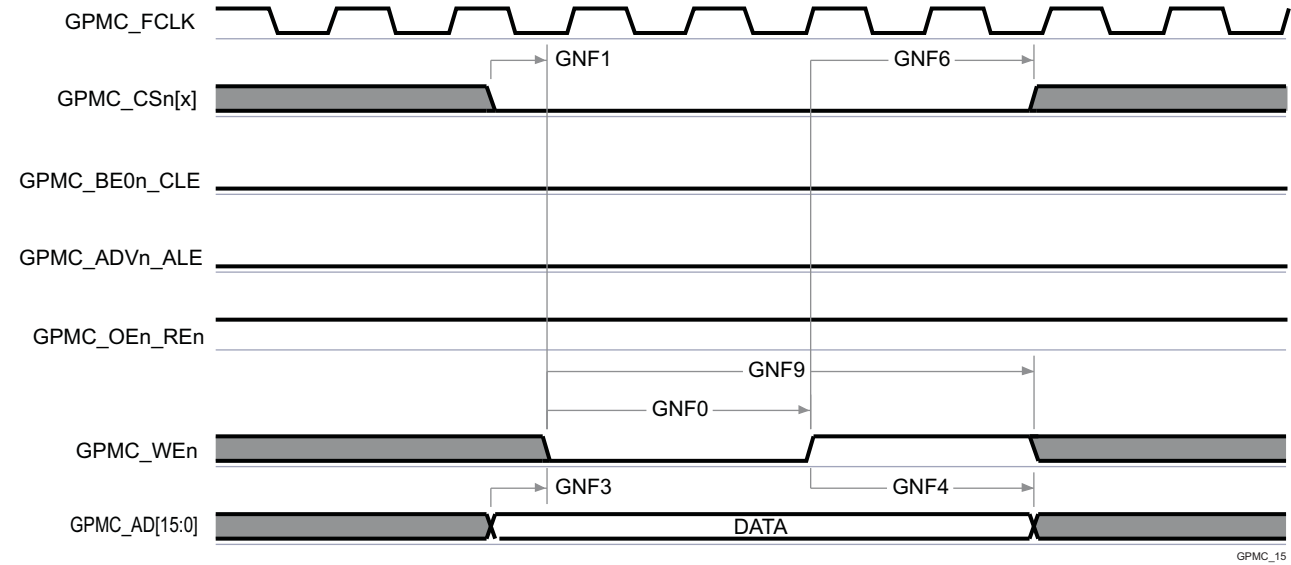
(1) In GPMC_CS[n], x is equal to 0, 1, 2 or 3.

✖ 5-54. GPMC and NAND Flash—Address Latch Cycle



- (1) GNF12 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after GNF12 functional clock cycles, input data will be internally sampled by active functional clock edge. GNF12 value must be stored inside AccessTime register bits field.
- (2) GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.
- (3) In GPMC_CS[n], x is equal to 0, 1, 2 or 3. In GPMC_WAIT[x], x is equal to 0 or 1.

Figure 5-55. GPMC and NAND Flash—Data Read Cycle



- (1) In GPMC_CS[n], x is equal to 0, 1, 2 or 3.

Figure 5-56. GPMC and NAND Flash—Data Write Cycle

For more information, see section *General-Purpose Memory Controller (GPMC)* in the device TRM.

5.9.5.11 HYPERBUS

For more details about features and additional description information on the device Hyperbus, see the corresponding sections within [4.3, Signal Descriptions](#) and [6, Detailed Description](#).

Table 5-54, Table 5-55, and Table 5-56 assume testing over the recommended operating conditions and electrical characteristic conditions (see Figure 5-57, Figure 5-58, and Figure 5-59).

表 5-54. Timing Requirements for HyperBus Initialization

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
D1	$t_{w(RESETn)}$	RESETn Pulse Width	200		ns
D2	$t_{w(csL)}$	Chip Select Pulse Width	1000		ns
D3	$t_{d(RESETnH-csL)}$	Delay time, RESETn inactive to CSn active	200.34		ns
D4	$t_{d(csL-RWDSL)}$	Delay time, CSn active to RWDS falling	115		ns

表 5-55. HyperBus 166 MHz Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
D5	$t_{skn(rwdsX-dV)}$	Input skew, RWDS transitioning to D0:D7 valid	-0.46	0.46	ns
D6	$t_{c(clk/clkn)}$	CLK period, CLK/CLKn	6		ns
D7	$t_{w(clk/clkn)}$	Pulse width, CLK/CLKn	2.7		ns
D8	$t_{w(csIV)}$	Pulse width, CS0 invalid between operations	6		ns
D9	$t_{d(clkH-csL)}$	Delay time, CS0 active to CLK rising/ CLKn falling	-3.41		ns
D10	$t_{d(clkL[LE]-csH)}$	Delay time, last falling CLK/ rising CLKn edge to CS0 inactive	0.66		ns
D11	$t_{d(clkX-rwdsV)}$	Delay time, CLK transition to RWDS valid	1.01	2.02	ns
D12	$t_{d(clkX-d[0:7]V)}$	Delay time, CLK transitioning to D0:7 valid	0.84	2.2	ns

表 5-56. HyperBus 100 MHz Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
LFD5	$t_{skn(rwdsX-dV)}$	Input skew, RWDS transitioning to D0:D7 valid	-0.81	0.81	ns
LFD6	$t_{c(clk)}$	CLK period, CLK	10		ns
LFD7	$t_{w(clk)}$	Pulse width, CLK	4.5		ns
LFD8	$t_{w(csIV)}$	Pulse width, CS0 invalid between operations	10		ns
LFD9	$t_{d(clkH-csL)}$	Delay time, CS0 active to CLK rising	-3.76		ns
LFD10	$t_{d(clkL[LE]-csH)}$	Delay time, last falling CLK edge to CS0 inactive	1.77		ns
LFD11	$t_{d(clkX-rwdsV)}$	Delay time, CLK transition to RWDS valid	2.05	3.24	ns
LFD12	$t_{d(clkX-d[0:7]V)}$	Delay time, CLK transitioning to D0:7 valid	1.87	3.41	ns

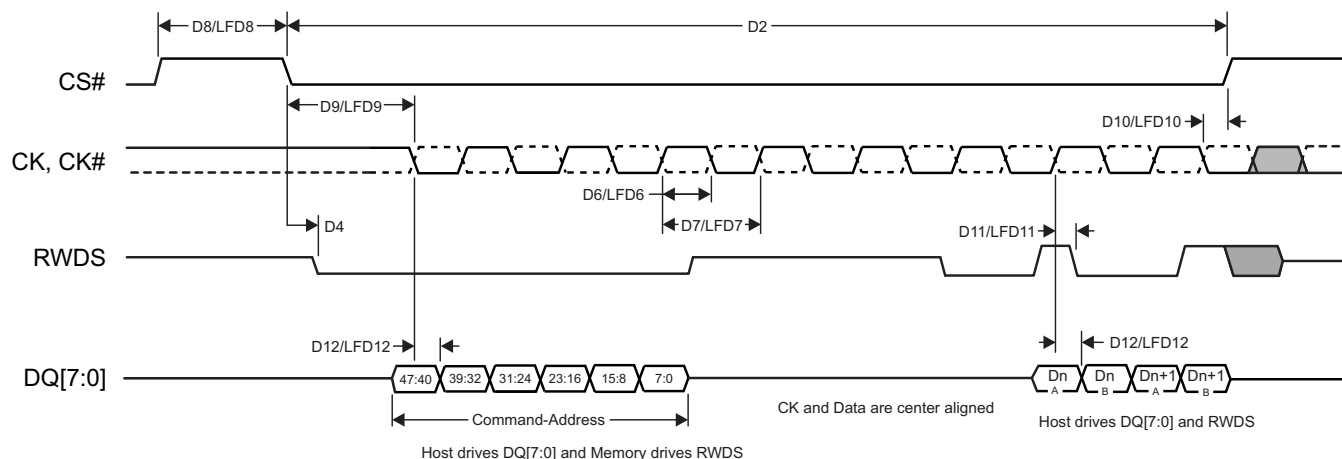
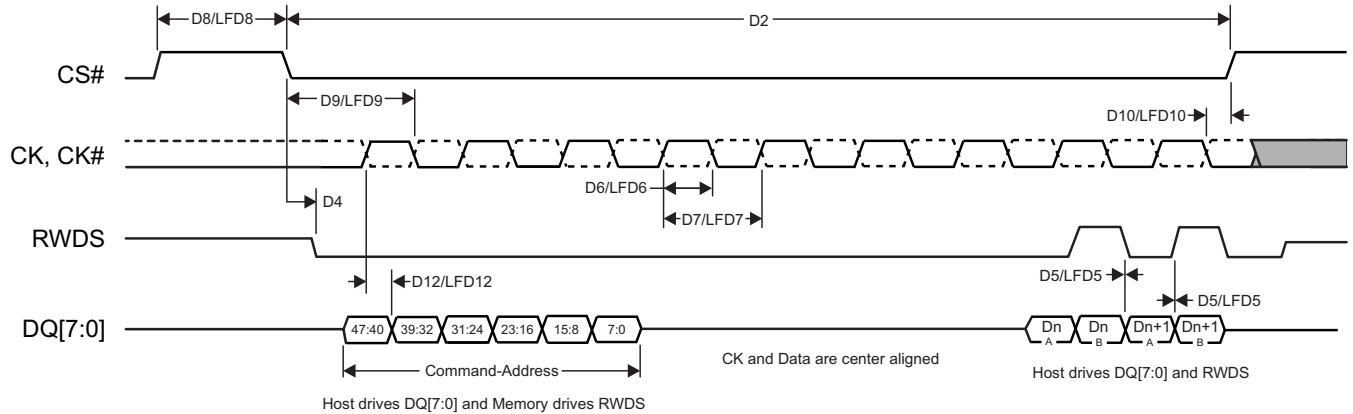


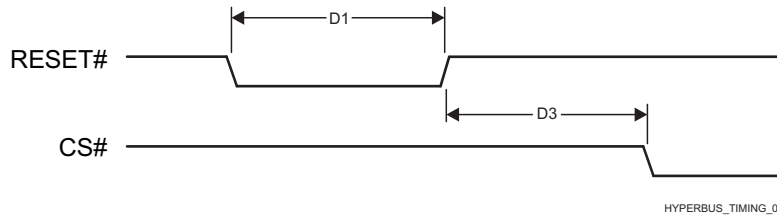
图 5-57. HyperBus Timing Diagrams - Transmitter Mode

HYPERBUS_TIMING_01



HYPERBUS_TIMING_02

图 5-58. HyperBus Timing Diagrams - Receiver Mode



HYPERBUS_TIMING_03

图 5-59. HyperBus Timing Diagrams - Reset

For more information, see section *HyperBus Interface* in the device TRM.

5.9.5.12 I2C

For more details about features and additional description information on the device Inter-Integrated Circuit, see the corresponding sections within 4.3, *Signal Descriptions* and 6, *Detailed Description*.

表 5-57, and 图 5-60 assume testing over the recommended operating conditions and electrical characteristic conditions.

表 5-57. Timing Requirements for I2C Input Timings⁽¹⁾⁽⁶⁾

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
I1	$t_{c(SCL)}$	Cycle time, SCL	Standard	10000		ns
			Fast	2500		ns
I2	$t_{su(SCLH-SDAL)}$	Setup time, SCL high before SDA low (for a repeated START condition)	Standard	4700		ns
			Fast	600		ns
I3	$t_{h(SDAL-SCLL)}$	Hold time, SCL low after SDA low (for a START and a repeated START condition)	Standard	4000		ns
			Fast	900		ns
I4	$t_{w(SCLL)}$	Pulse duration, SCL low	Standard	4700		ns
			Fast	1300		ns
I5	$t_{w(SCLH)}$	Pulse duration, SCL high	Standard	4000		ns
			Fast	600		ns
I6	$t_{su(SDAV-SCLH)}$	Setup time, SDA valid before SCL high	Standard	250		ns
			Fast	100 ⁽²⁾		ns
I7	$t_{h(SCLL-SDAV)}$	Hold time, SDA valid after SCL low	Standard	0 ⁽³⁾	3450 ⁽⁴⁾	ns
			Fast	0 ⁽³⁾	900 ⁽⁴⁾	ns
I8	$t_{w(SDAH)}$	Pulse duration, SDA high between STOP and START conditions	Standard	4700		ns
			Fast	1300		ns

表 5-57. Timing Requirements for I2C Input Timings⁽¹⁾⁽⁶⁾ (continued)

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
I9	$t_{r(SDA)}$	Rise time, SDA	Standard		1000	ns
			Fast	$20 + .1Cb^{(5)}$ (7)	$300^{(3)}$ (7)	ns
I10	$t_{r(SCL)}$	Rise time, SCL	Standard		1000	ns
			Fast	$20 + .1Cb^{(5)}$ (7)	$300^{(3)}$ (7)	ns
I11	$t_{f(SDA)}$	Fall time, SDA	Standard		300	ns
			Fast	$20 + .1Cb^{(5)}$ (7)	$300^{(3)}$ (7)	ns
I12	$t_{f(SCL)}$	Fall time, SCL	Standard		300	ns
			Fast	$20 + .1Cb$	300	ns
I13	$t_{su(SCLH-SDAH)}$	Setup time, SCL high before SDA high (for STOP condition)	Standard	4000		ns
			Fast	600		ns
I14	$t_{w(SP)}$	Pulse duration, spike (must be suppressed)	Standard			ns
			Fast	0	50	ns
I15	t_{skew}	Skew	Standard		1	ns
			Fast		1	ns
I16	Cb	Capacitive load for each bus line	Standard		400	pF
			Fast		400	pF

- (1) The I2C pins SDA and SCL do not feature fail-safe I/O buffers. These pins could potentially draw current when the device is powered down.
- (2) A Fast-mode I2C-bus™ device can be used in a Standard-mode I2C-bus system, but the requirement $t_{su(SDA-SCLH)} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r\max} + t_{su(SDA-SCLH)} = 1000 + 250 = 1250$ ns (according to the Standard-mode I2C-Bus Specification) before the SCL line is released.
- (3) A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
- (4) The maximum $t_{h(SDA-SCLL)}$ has only to be met if the device does not stretch the low period [$t_{w(SCLL)}$] of the SCL signal.
- (5) Cb = total capacitance of one bus line in pF. If mixed with HS-mode devices, faster fall-times are allowed
- (6) Software must properly configure the I2C module registers to achieve the timings shown in this table. See the device TRM for details.
- (7) These timings apply only to MCU_I2C0 and WKUP_I2C0. MAIN_I2C[0:3] use standard LVCMOS buffers to emulate open-drain buffers and their rise/fall times should be referenced in the device IBIS model.

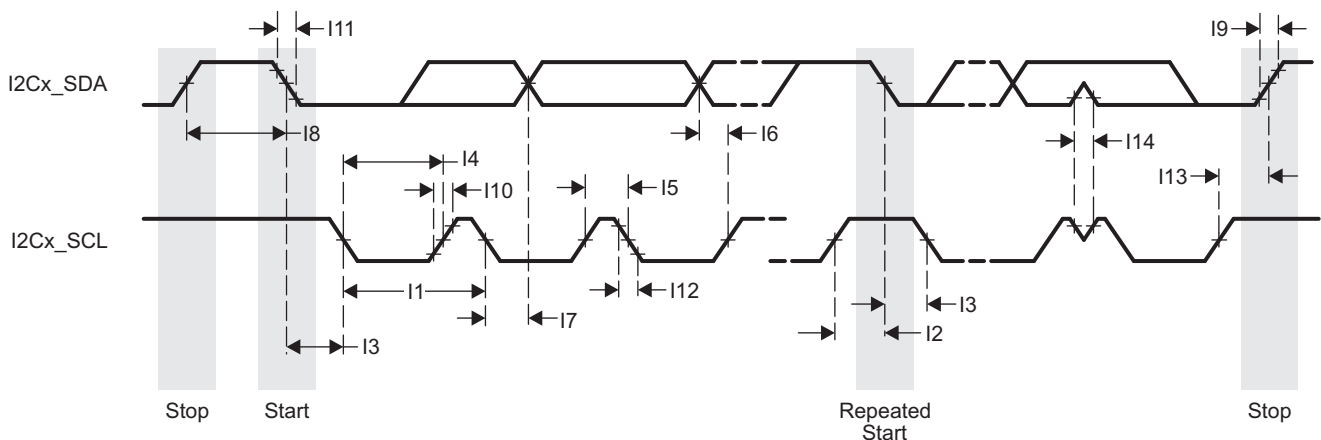


图 5-60. I2C Receive Timing⁽¹⁾

- (1) x in I2Cx_SDA and I2Cx_SCL is 0, 1 or 2.

表 5-58 和 图 5-61 assume testing over the recommended operating conditions and electrical characteristic conditions.

表 5-58. Switching Characteristics Over Recommended Operating Conditions for I2C Output Timings

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
I16	$t_{c(SCL)}$	Cycle time, SCL	Standard	10000		ns
			Fast	2500		ns
I17	$t_{su(SCLH-SDAL)}$	Setup time, SCL high before SDA low (for a repeated START condition)	Standard	4700		ns
			Fast	600		ns
I18	$t_{h(SDAL-SCLL)}$	Hold time, SCL low after SDA low (for a START and a repeated START condition)	Standard	4000		ns
			Fast	900		ns
I19	$t_{w(SCLL)}$	Pulse duration, SCL low	Standard	4700		ns
			Fast	1300		ns
I20	$t_{w(SCLH)}$	Pulse duration, SCL high	Standard	4000		ns
			Fast	600		ns
I21	$t_{su(SDAV-SCLH)}$	Setup time, SDA valid before SCL high	Standard	250		ns
			Fast	100 ⁽²⁾		ns
I22	$t_{h(SCLL-SDAV)}$	Hold time, SDA valid after SCL low	Standard	0 ⁽³⁾	3450 ⁽⁴⁾	ns
			Fast	0 ⁽³⁾	900 ⁽⁴⁾	ns
I23	$t_{w(SDAH)}$	Pulse duration, SDA high between STOP and START conditions	Standard	4700		ns
			Fast	1300		ns
I24	$t_{r(SDA)}$	Rise time, SDA	Standard		1000	ns
			Fast	20+.1Cb ^{(5) (7)}	300 ^{(3) (7)}	ns
I25	$t_{r(SCL)}$	Rise time, SCL	Standard		1000	ns
			Fast	20+.1Cb ^{(5) (7)}	300 ^{(3) (7)}	ns
I26	$t_{f(SDA)}$	Fall time, SDA	Standard		300	ns
			Fast	20+.1Cb ^{(5) (7)}	300 ^{(3) (7)}	ns
I27	$t_{f(SCL)}$	Fall time, SCL	Standard		300	ns
			Fast	20+.1Cb ^{(5) (7)}	300 ^{(3) (7)}	ns
I28	$t_{su(SCLH-SDAH)}$	Setup time, SCL high before SDA high (for STOP condition)	Standard	4000		ns
			Fast	600		ns
I29	t_{skew}	Skew	Standard		3	ns
			Fast		20	ns
I30	C_b	Capacitive load for each bus line	Standard		400	pF
			Fast		400	pF

- (1) The I2C pins SDA and SCL do not feature fail-safe I/O buffers. These pins could potentially draw current when the device is powered down.
- (2) A Fast-mode I2C-bus™ device can be used in a Standard-mode I2C-bus system, but the requirement $t_{su(SDA-SCLH)} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r \max} + t_{su(SDA-SCLH)} = 1000 + 250 = 1250$ ns (according to the Standard-mode I2C-Bus Specification) before the SCL line is released.
- (3) A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
- (4) The maximum $t_{h(SDA-SCLL)}$ has only to be met if the device does not stretch the low period [$t_{w(SCLL)}$] of the SCL signal.
- (5) C_b = total capacitance of one bus line in pF. If mixed with HS-mode devices, faster fall-times are allowed.
- (6) Software must properly configure the I2C module registers to achieve the timings shown in this table. See the device TRM for details.
- (7) These timings apply only to MCU_I2C0 and WKUP_I2C0. MAIN_I2C[0:3] use standard LVCMOS buffers to emulate open-drain buffers and their rise/fall times should be referenced in the device IBIS model.

注

I2C emulation is achieved by configuring the LVCMOS buffers to output HiZ instead of driving high when transmitting logic-1.

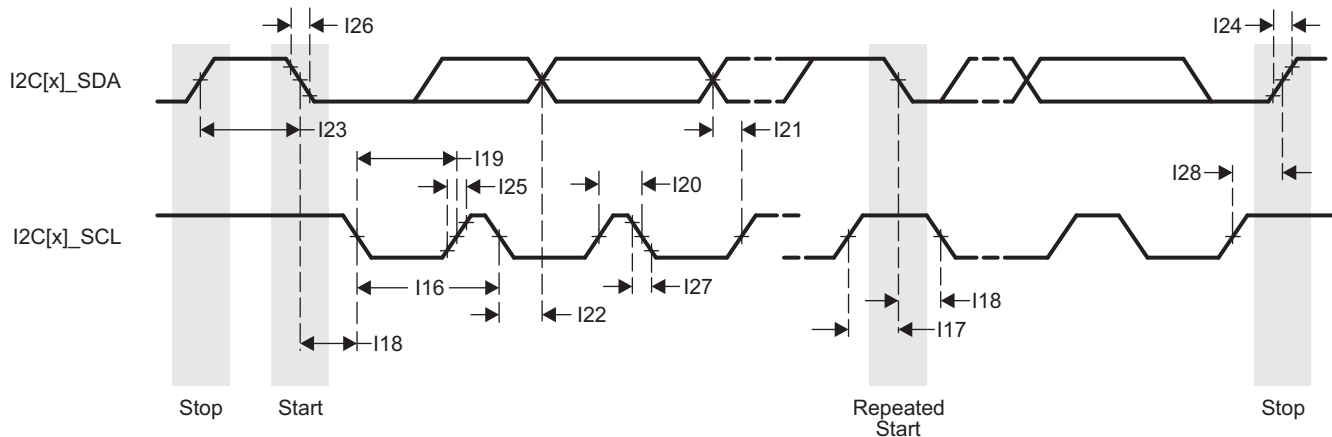


图 5-61. I2C Transmit Timing⁽¹⁾

(1) x in I2Cx_SDA and I2Cx_SCL is 0, 1 or 2.

For more information, see section *Inter-Integrated Circuit (I2C) Interface* in the device TRM.

5.9.5.13 MCAN

For more details about features and additional description information on the device Controller Area Network Interface, see the corresponding sections within 4.3, *Signal Descriptions* and 6, *Detailed Description*.

表 5-59 presents timing parameters for MCANi Interface.

表 5-59. MCAN Register to Pin Timings

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
M1	$t_{p(MCANi_TX)}$	Delay Time Max, Transmit Shift Register to MCANi_TX pin	Normal		10	ns
M2	$t_{p(MCANi_RX)}$	Delay Time Max, MCANi_RX pin to receive shift register	Normal		10	ns

(1) i in MCANi_* = 0 or 1.

For more information, see section *Controller Area Network (MCAN)* in the device TRM.

5.9.5.14 MCASP

For more details about features and additional description information on the device Multichannel Audio Serial Port, see the corresponding sections within 4.3, *Signal Descriptions* and 6, *Detailed Description*.

表 5-60, and 图 5-62 present timing requirements for MCASP0 to MCASP2.

表 5-60. Timing Requirements for MCASP⁽¹⁾

NO.	PARAMETER	DESCRIPTION	Mode	MIN	MAX	UNIT
ASP1	$t_c(AHCLKRX)$	Cycle time, AHCLKR/X		20		ns
ASP2	$t_w(AHCLKRX)$	Pulse duration, AHCLKR/X high or low		0.5P - 2.5 ⁽²⁾		ns
ASP3	$t_c(ACLKRX)$	Cycle time, ACLKR/X		20		ns
ASP4	$t_w(ACLKRX)$	Pulse duration, ACLKR/X high or low		0.5R - 2.5 ⁽³⁾		ns

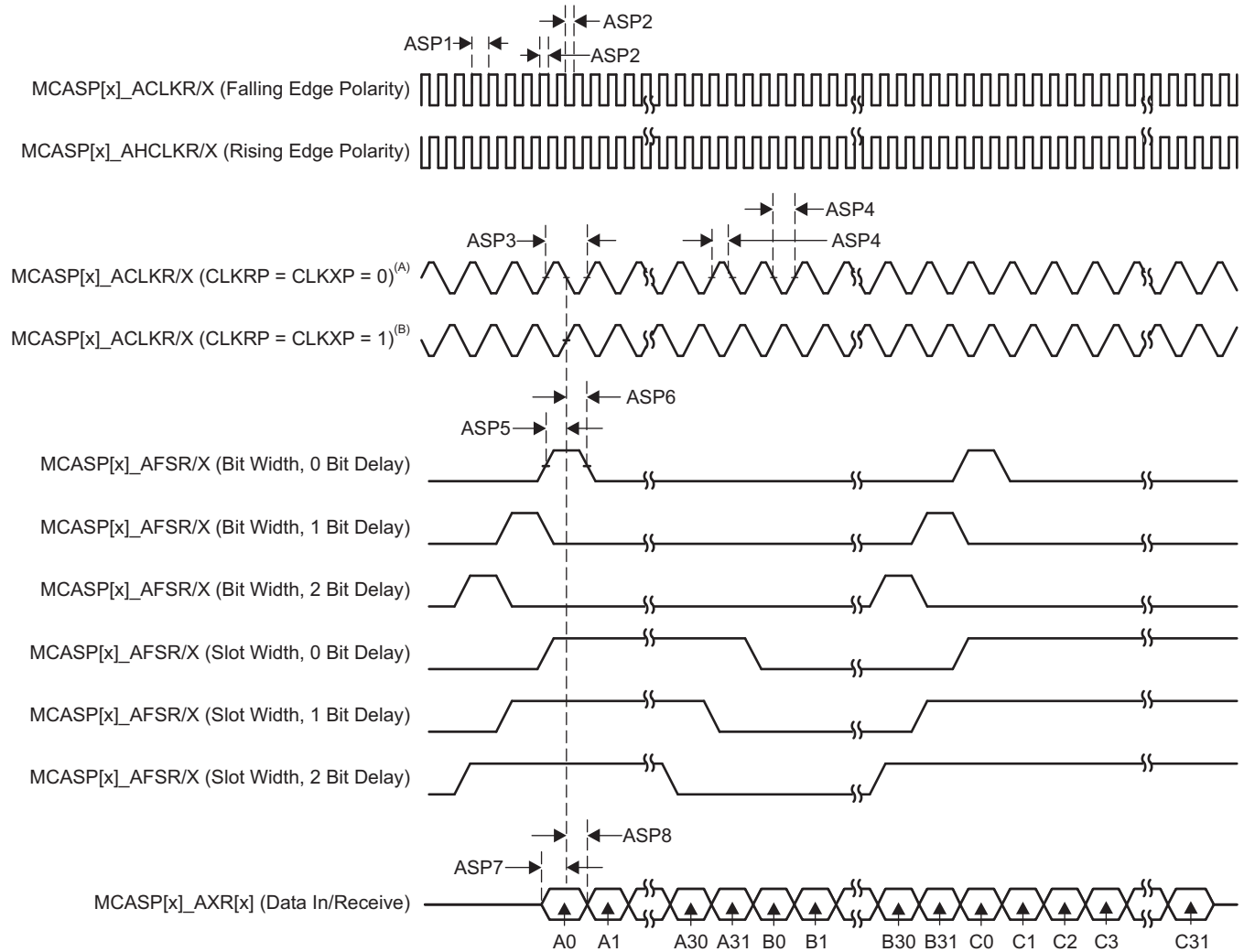
表 5-60. Timing Requirements for MCASP⁽¹⁾ (continued)

NO.	PARAMETER	DESCRIPTION	Mode	MIN	MAX	UNIT
ASP5	$t_{su}(AFSRX-ACLKRX)$	Setup time, AFSR/X input valid before ACLKRX	ACLKRX int	10.995		ns
			ACLKRX ext in/out	4		
ASP6	$t_h(ACLKRX-AFSRX)$	Hold time, AFSR/X input valid after ACLKRX	ACLKRX int	-1		ns
			ACLKRX ext in/out	1.6		
ASP7	$t_{su}(AXR-ACLKRX)$	Setup time, AXR input valid before ACLKRX	ACLKRX int	10.995		ns
			ACLKRX ext in/out	4		
ASP8	$t_h(ACLKRX-AXR)$	Hold time, AXR input valid after ACLKRX	ACLKRX int	-1		ns
			ACLKRX ext in/out	1.6		

- (1) ACLKR internal: ACLKRCTL.CLKRM=1, PDIR.ACLKR = 1
 ACLKR external input: ACLKRCTL.CLKRM=0, PDIR.ACLKR=0
 ACLKR external output: ACLKRCTL.CLKRM=0, PDIR.ACLKR=1
 ACLKX internal: ACLKXCTL.CLKXM=1, PDIR.ACLKX = 1
 ACLKX external input: ACLKXCTL.CLKXM=0, PDIR.ACLKX=0
 ACLKX external output: ACLKXCTL.CLKXM=0, PDIR.ACLKX=1

(2) P = AHCLKRX period in ns.

(3) R = ACLKRX period in ns.



- A. For CLKRP = CLKXP = 0, the MCASP transmitter is configured for rising edge (to shift data out) and the MCASP receiver is configured for falling edge (to shift data in).
- B. For CLKRP = CLKXP = 1, the MCASP transmitter is configured for falling edge (to shift data out) and the MCASP receiver is configured for rising edge (to shift data in).

图 5-62. MCASP Input Timing

(1) x in MCASP[x]_* is 0, 1 or 2

表 5-61 and 図 5-63 present switching characteristics over recommended operating conditions for MCASP0 to MCASP2.

表 5-61. Switching Characteristics Over Recommended Operating Conditions for MCASP⁽¹⁾

NO.	PARAMETER	DESCRIPTION	Mode	MIN	MAX	UNIT
ASP9	$t_c(\text{AHCLKRX})$	Cycle time, AHCLKR/X		20		ns
ASP10	$t_w(\text{AHCLKRX})$	Pulse duration, AHCLKR/X high or low		0.5P - 2.5 ⁽²⁾		ns
ASP11	$t_c(\text{ACLKRX})$	Cycle time, ACLKR/X		20		ns
ASP12	$t_w(\text{ACLKRX})$	Pulse duration, ACLKR/X high or low		0.5R - 2.5 ⁽³⁾		ns
ASP13	$t_d(\text{ACLKRX-AFSRX})$	Delay time, ACLKR/X transmit edge to AFSR/X output valid	ACLKRX int	0	6.5	ns
			ACLKRX ext in/out	2	14	
ASP14	$t_d(\text{ACLKX-AXR})$	Delay time, ACLKX transmit edge to AXR output valid	ACLKRX int	0	6.5	ns
			ACLKRX ext in/out	2	14	
ASP15	$t_{dis}(\text{ACLKX-AXR})$	Disable time, ACLKX transmit edge to AXR output high impedance	ACLKRX int	0	6.5	ns
			ACLKRX ext in/out	2	14	

- (1) ACLKR internal: ACLKRCTL.CLKRM=1, PDIR.ACLKR = 1
 ACLKR external input: ACLKRCTL.CLKRM=0, PDIR.ACLKR=0
 ACLKR external output: ACLKRCTL.CLKRM=0, PDIR.ACLKR=1
 ACLKX internal: ACLKXCTL.CLKXM=1, PDIR.ACLKX = 1
 ACLKX external input: ACLKXCTL.CLKXM=0, PDIR.ACLKX=0
 ACLKX external output: ACLKXCTL.CLKXM=0, PDIR.ACLKX=1

(2) P = AHCLKR/X period in ns.

(3) R = ACLKR/X period in ns.

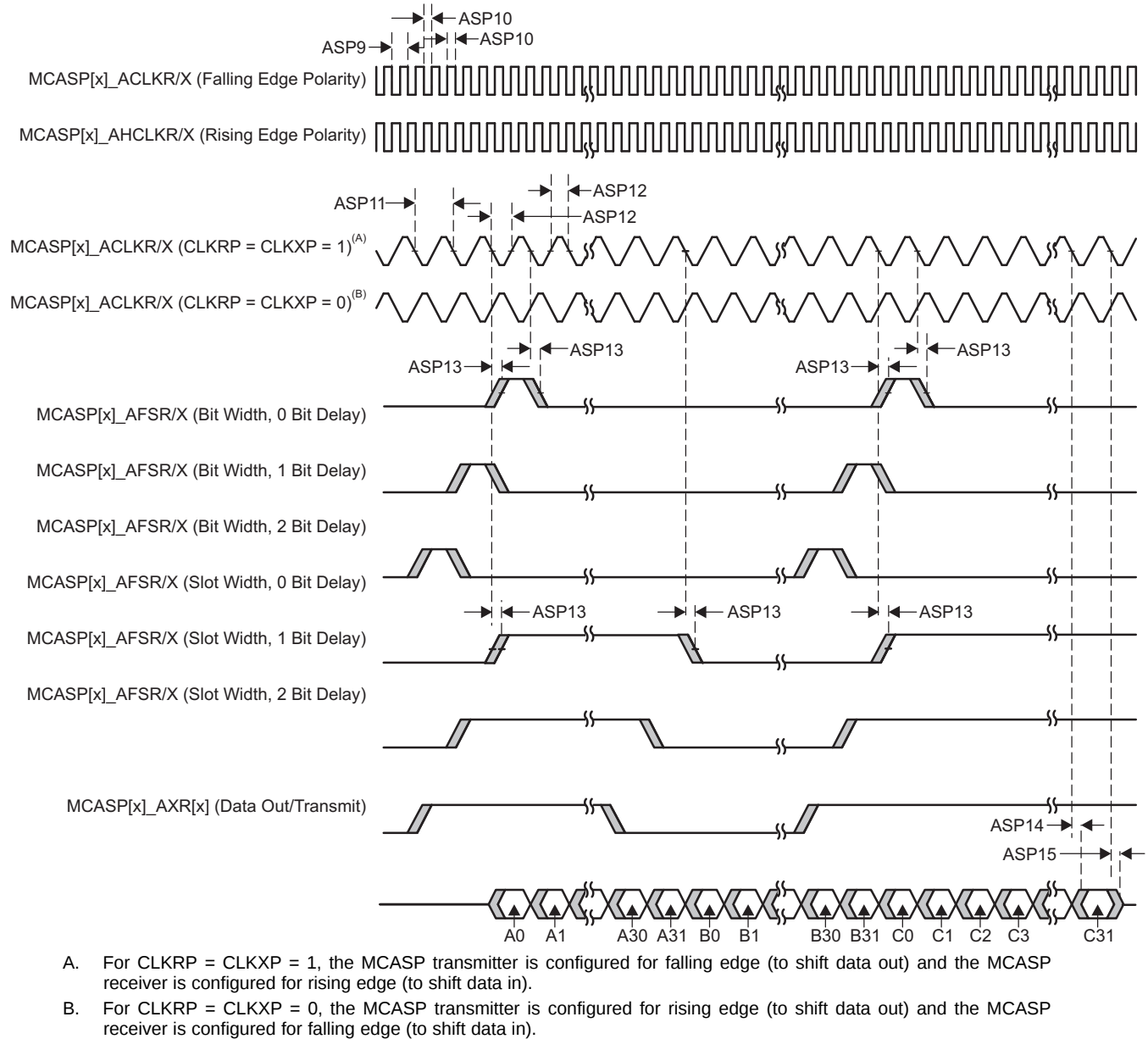


图 5-63. MCASP Output Timing

(1) x in MCASP[x]_* is 0, 1 or 2

For more information, see section *Controller Area Network (MCAN)* in the device TRM.

5.9.5.15 MCSPI

For more details about features and additional description information on the device Serial Port Interface, see the corresponding sections within [4.3, Signal Descriptions](#) and [6, Detailed Description](#).

5.9.5.15.1 SPI—Master Mode

表 5-62, 图 5-64 和 图 5-65 present Timing Requirements for SPI - Master Mode.

表 5-62. Timing Requirements for SPI - Master Mode ⁽¹⁾⁽⁸⁾

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
SM1	$t_{c(SPICLK)}$	Cycle time, SPI_CLK ^{(1) (2)}		20.8 ⁽³⁾		ns
SM2	$t_{w(SPICLK_L)}$	Typical Pulse duration, SPI_CLK low ⁽¹⁾		-1 + 0.5P ⁽⁴⁾		ns
SM3	$t_{w(SPICLK_H)}$	Typical Pulse duration, SPI_CLK high ⁽¹⁾		-1 + 0.5P ⁽⁴⁾		ns
SM4	$t_{su(MISO-SPICLK)}$	Setup time, SPI_D[x] valid before SPI_CLK active edge ⁽¹⁾		2		ns
SM5	$t_{h(SPICLK-MISO)}$	Hold time, SPI_D[x] valid after SPI_CLK active edge ⁽¹⁾		3		ns
SM6	$t_{d(SPICLK-SIMO)}$	Delay time, SPI_CLK active edge to SPI_D[x] transition ⁽¹⁾		-3	2	ns
SM7	$t_{sk(CS-SIMO)}$	Delay time, SPI_CS[x] active to SPI_D[x] transition		5		ns
SM8	$t_{d(SPICLK-CS)}$	Delay time, SPI_CS[x] active to SPI_CLK first edge	Master_PHA0_POL0; Master_PHA0_POL1; ⁽⁵⁾	-4 + B ⁽⁶⁾		ns
			Master_PHA1_POL0; Master_PHA1_POL1; ⁽⁵⁾	-4 + A ⁽⁷⁾		ns
SM9	$t_{d(SPICLK-CS)}$	Delay time, SPI_CLK last edge to SPI_CS[x] inactive	Master_PHA0_POL0; Master_PHA0_POL1; ⁽⁵⁾	-4 + A ⁽⁷⁾		ns
			Master_PHA1_POL0; Master_PHA1_POL1; ⁽⁵⁾	-4 + B ⁽⁶⁾		ns

(1) This timing applies to all configurations regardless of SPI_CLK polarity and which clock edges are being used to drive output data and capture input data

(2) Related to the SPI_CLK maximum frequency

(3) 20 ns cycle time = 50 MHz

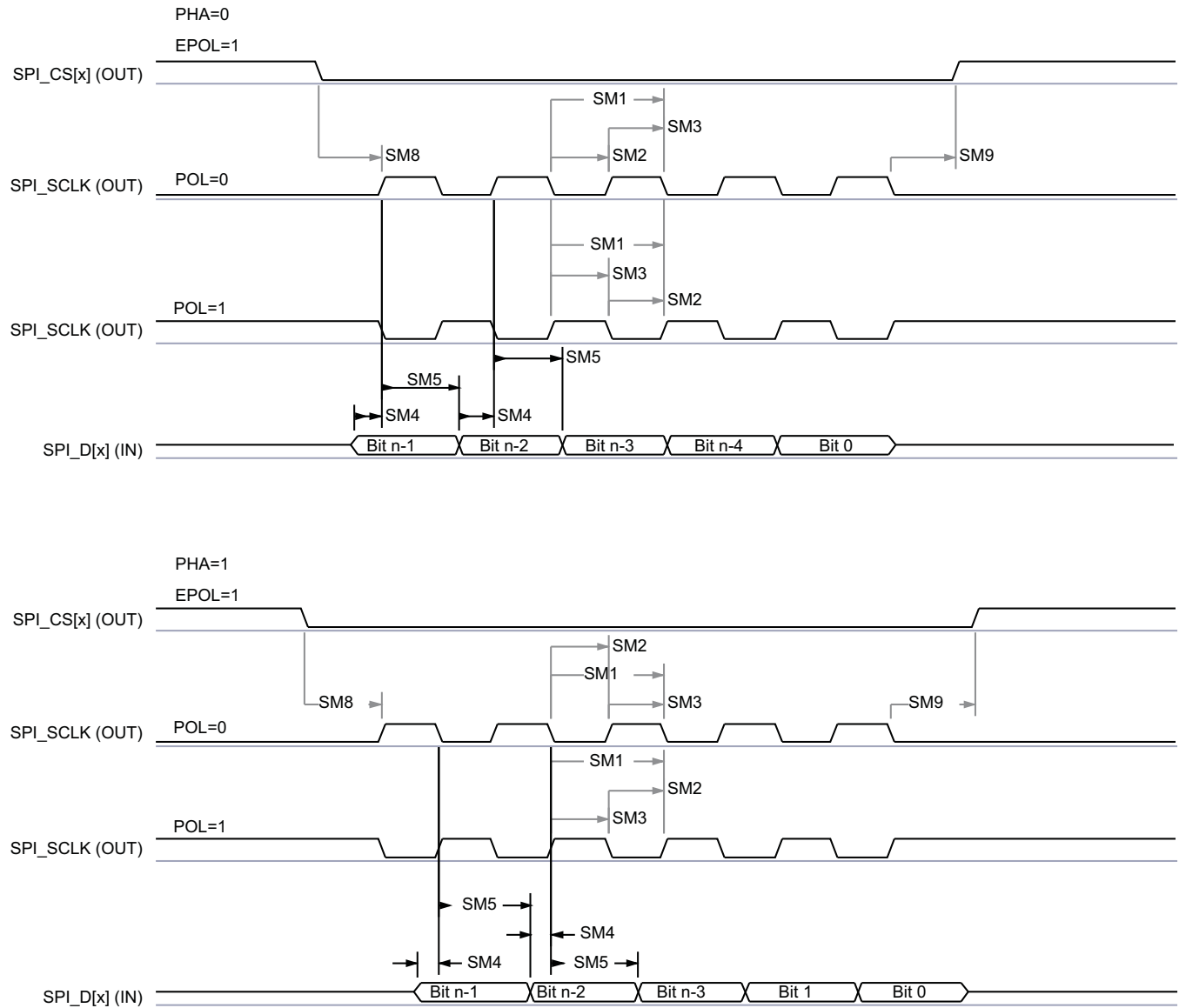
(4) P = SPICLK period

(5) SPI_CLK phase is programmable with the PHA bit of the SPI_CH(i)CONF register

(6) $B = (TCS + .5) * TSPICLKREF$, where TCS is a bit field of the SPI_CH(i)CONF register and Fratio = Even ≥ 2 .

(7) When P = 20.8 ns, $A = (TCS + 1) * TSPICLKREF$, where TCS is a bit field of the SPI_CH(i)CONF register.
When P > 20.8 ns, $A = (TCS + 0.5) * Fratio * TSPICLKREF$, where TCS is a bit field of the SPI_CH(i)CONF register.

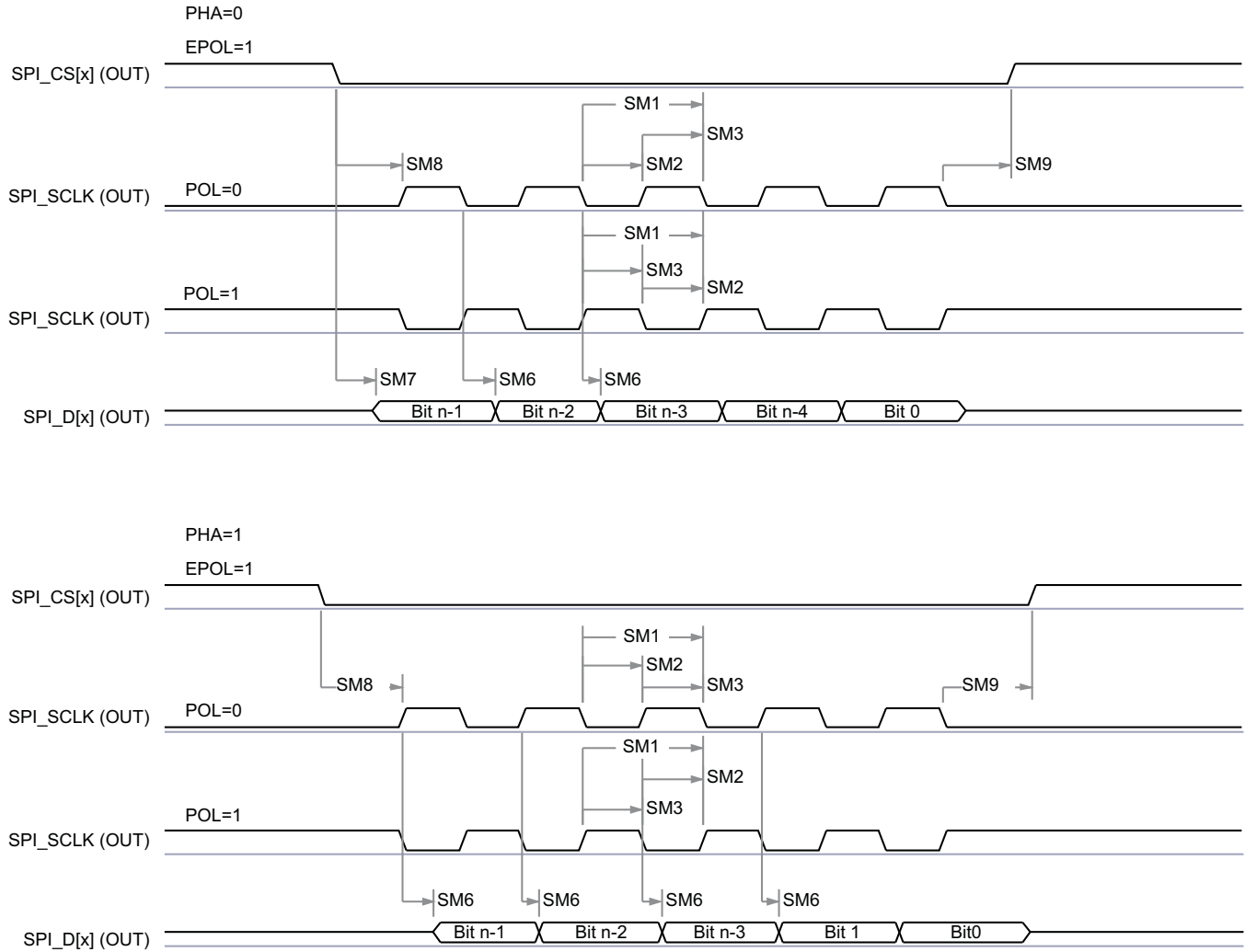
(8) The IO timings provided in this section are applicable for all combinations of signals for SPI1 and SPI2. However, the timings are only valid for SPI3 and SPI4 if signals within a single IOSET are used. The IOSETs are defined in the following tables.



SPRSP08_TIMING_McSPI_02

图 5-64. SPI Master Mode Receive Timing

ADVANCE INFORMATION



SPRS098_TIMING_McSPI_01

 **5-65. SPI Master Mode Transmit Timing**

5.9.5.15.2 MCSPI—Slave Mode

表 5-63, 图 5-66, and 图 5-67 present Timing Requirements for SPI - Slave Mode.

表 5-63. Timing Requirements for SPI - Slave Mode

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
SS1	$t_c(\text{SPICLK})$	Cycle time, SPI_CLK		20.8		ns
SS2	$t_w(\text{SPICLK})$	Typical Pulse duration, SPI_CLK low		0.45P ⁽²⁾		ns
SS3	$t_w(\text{SPICLK})$	Typical Pulse duration, SPI_CLK high		0.45P ⁽²⁾		ns
SS4	$t_{su}(\text{SIMO-SPICLK})$	Setup time, SPI_D[x] valid before SPI_CLK active edge		5		ns
SS5	$t_h(\text{SPICLK-SIMO})$	Hold time, SPI_D[x] valid after SPI_CLK active edge		5		ns
SS6	$t_d(\text{SPICLK-SOMI})$	Delay time, SPI_CLK active edge to mcspi_somi transition		2	5	ns
SS7	$t_{sk}(\text{CS-SOMI})$	Delay time, SPI_CS[x] active edge to mcspi_somi transition		20.95		ns
SS8	$t_{su}(\text{CS-SPICLK})$	Setup time, SPI_CS[x] valid before SPI_CLK first edge		5		ns
SS9	$t_h(\text{SPICLK-CS})$	Hold time, SPI_CS[x] valid after SPI_CLK last edge		5		ns

- (1) This timing applies to all configurations regardless of SPI_CLK polarity and which clock edges are used to drive output data and capture input data.
- (2) P = SPICLK period.
- (3) PHA = 0; SPI_CLK phase is programmable with the PHA bit of the SPI_CH(i)CONF register.

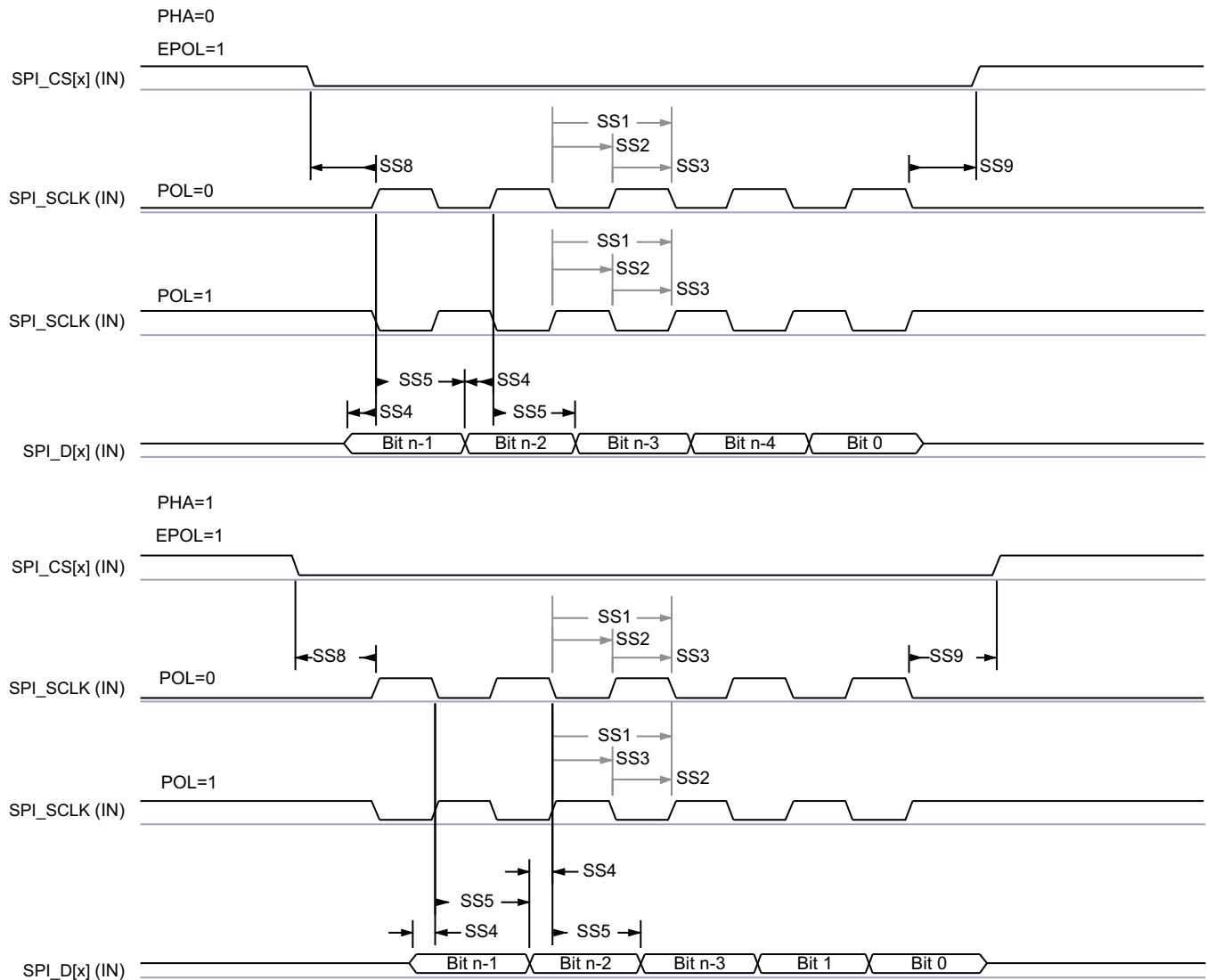
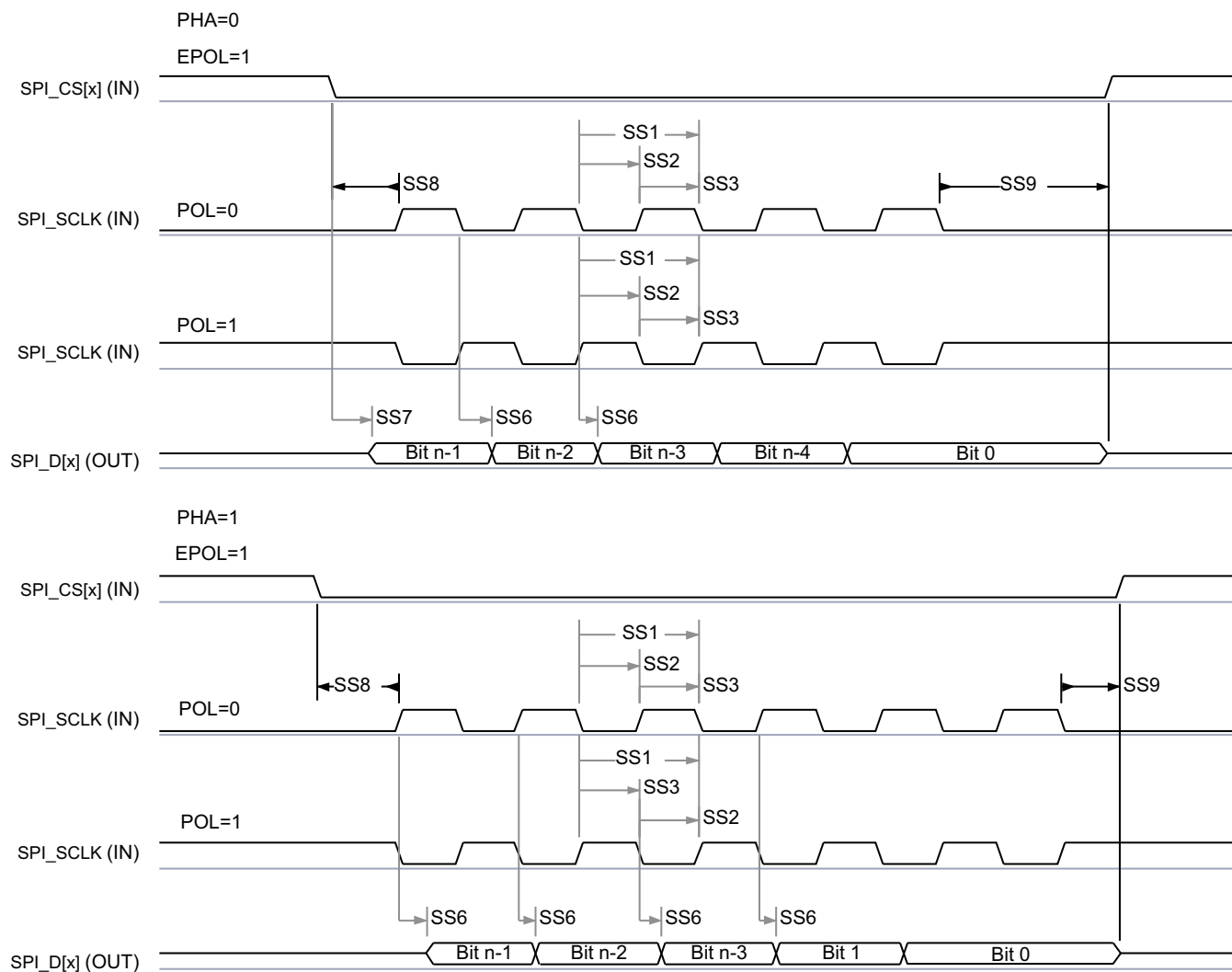


图 5-66. SPI Slave Mode Receive Timing

SPRSP08_TIMING_McSPI_04



SPRS08_TIMING_McSPI_03

5-67. SPI Slave Mode Transmit Timing

For more information, see section *Multichannel Serial Peripheral Interface (MCSPI)* in the device TRM.

5.9.5.16 eMMC/SD/SDIO

注

The I/O Timings provided in this section are valid only when the corresponding DLL Delays are configured for some MMC usage modes, as described in 表 5-76.

注

The MMCi (i = 0 to 1) controller is also referred to as MMCi.

For more details about features and additional description information on the device Multi Media Card, see the corresponding sections within 4.3, *Signal Descriptions* and 6, *Detailed Description*.

5.9.5.16.1 MMCi — eMMC/SD/SDIO Card Interface

MMCi interface is compliant with the SD Standard v3.01 as well as JC64 eMMC standard v4.5 and it supports the following SD Card and eMMC applications:

- Default speed
- High speed
- UHS-I SDR12
- UHS-I SDR25
- UHS-I SDR50
- UHS-I SDR104 / HS200
- UHS-I DDR50

注

For more information, see section *Multimedia Card/Secure Digital (MMC/SD) Interface* in the device TRM.

5.9.5.16.1.1 Default speed Mode

表 5-64 and 表 5-65 present Timing requirements and Switching characteristics for MMCi - Default Speed in receiver and transmitter mode (see 图 5-68 and 图 5-69)

表 5-64. Timing Requirements for MMCi - Default Speed Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
DSSD5	$t_{su}(cmdV-clkH)$	Setup time, MMCi_CMD valid before MMCi_CLK rising clock edge	1.65		ns
DSSD6	$t_h(clkH-cmdV)$	Hold time, MMCi_CMD valid after MMCi_CLK rising clock edge	19.17		ns
DSSD7	$t_{su}(dV-clkH)$	Setup time, MMCi_DAT[j:0] valid before MMCi_CLK rising clock edge	1.65		ns
DSSD8	$t_h(clkH-dV)$	Hold time, MMCi_DAT[j:0] valid after MMCi_CLK rising clock edge	19.17		ns

(1) j in [j:0] is equal to 7 (for MMC0), or 3 (for MMC1).

表 5-65. Switching Characteristics for MMCi - Default Speed Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
DSSD0	$f_{op}(clk)$	Operating frequency, MMCi_CLK		25	MHz
DSSD1	$t_w(clkH)$	Pulse duration, MMCi_CLK high	18.7		ns
DSSD2	$t_w(clkL)$	Pulse duration, MMCi_CLK low	18.7		ns
DSSD3	$t_d(clkL-cmdV)$	Delay time, MMCi_CLK falling clock edge to MMCi_CMD transition	- 13.6	13.6	ns
DSSD4	$t_d(clkL-dV)$	Delay time, MMCi_CLK falling clock edge to MMCi_DAT[j:0] transition	- 13.6	13.6	ns

(1) j in [j:0] is equal to 7 (for MMC0), or 3 (for MMC1).

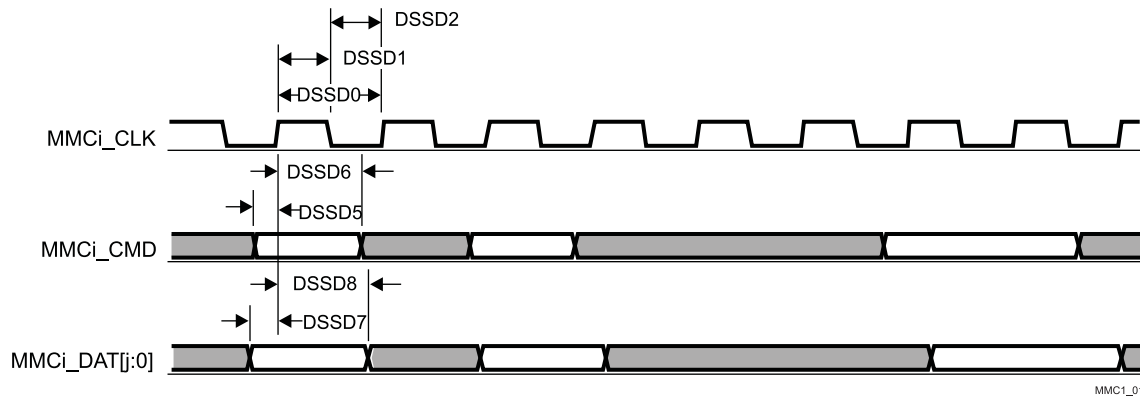


图 5-68. eMMC/SD/SDIO in - Default Speed - Receiver Mode

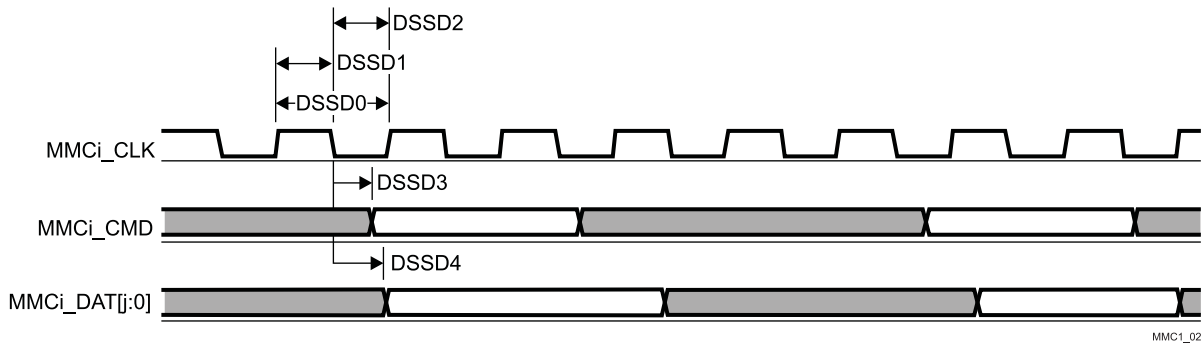


图 5-69. eMMC/SD/SDIO in - Default Speed - Transmitter Mode

5.9.5.16.1.2 High speed Mode

表 5-66 和 表 5-67 呈现 Timing requirements and Switching characteristics for MMCi - High Speed in receiver and transmitter mode (see 图 5-70 and 图 5-71).

表 5-66. Timing Requirements for MMCi - High Speed Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
HSSD3	$t_{su(cmdV-clkH)}$	Setup time, MMCi_CMD valid before MMCi_CLK rising clock edge	2.15		ns
HSSD4	$t_{h(clkH-cmdV)}$	Hold time, MMCi_CMD valid after MMCi_CLK rising clock edge	2.67		ns
HSSD7	$t_{su(dV-clkH)}$	Setup time, MMCi_DAT[j:0] valid before MMCi_CLK rising clock edge	2.15		ns
HSSD8	$t_{h(clkH-dV)}$	Hold time, MMCi_DAT[j:0] valid after MMCi_CLK rising clock edge	2.67		ns

(1) j in [j:0] is equal to 7 (for MMC0), or 3 (for MMC1).

表 5-67. Switching Characteristics for MMCi - High Speed Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
HSSD1	$f_{op(clk)}$	Operating frequency, MMCi_CLK		50	MHz
HSSD2H	$t_{w(clkH)}$	Pulse duration, MMCi_CLK high	9.2		ns
HSSD2L	$t_{w(clkL)}$	Pulse duration, MMCi_CLK low	9.2		ns
HSSD5	$t_{d(clkL-cmdV)}$	Delay time, MMCi_CLK falling clock edge to MMCi_CMD transition	-6.1	3.1	ns
HSSD6	$t_{d(clkL-dV)}$	Delay time, MMCi_CLK falling clock edge to MMCi_DAT[j:0] transition	-6.1	3.1	ns

(1) j in [j:0] is equal to 7 (for MMC0), or 3 (for MMC1).

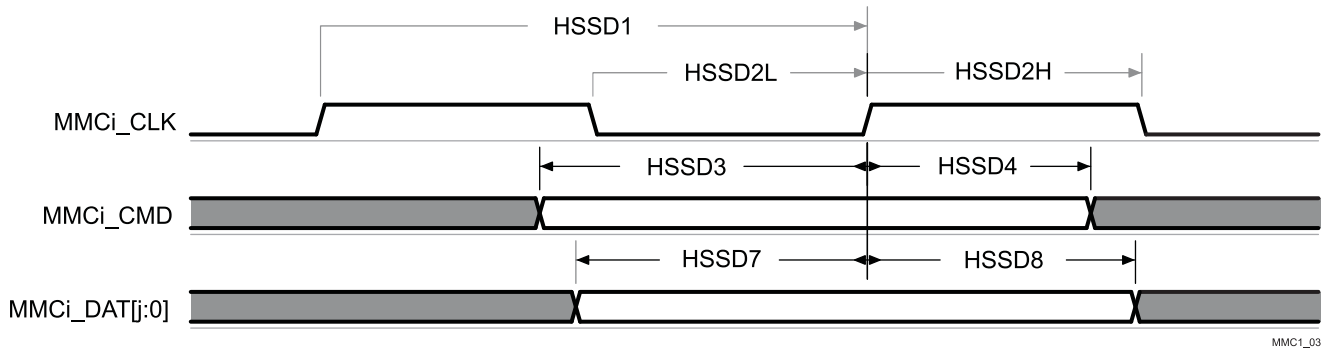


图 5-70. eMMC/SD/SDIO in - High Speed - Receiver Mode

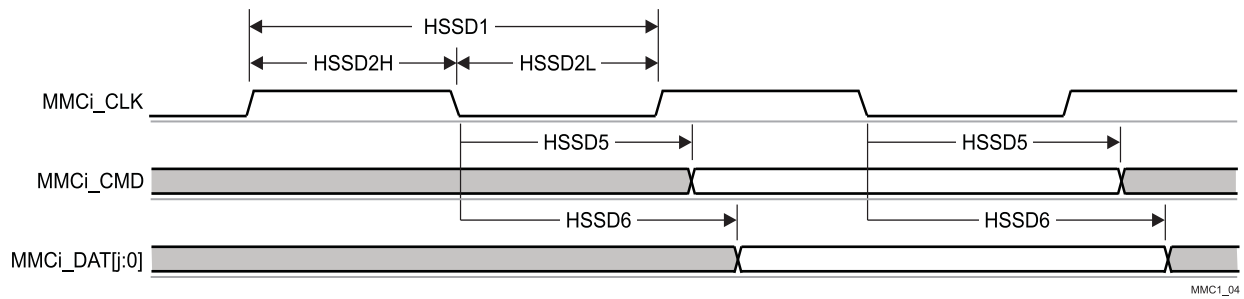


图 5-71. eMMC/SD/SDIO in - High Speed - Transmitter Mode

5.9.5.16.1.3 UHS-I SDR12 Mode

表 5-68 和 表 5-69 呈现 Timing requirements and Switching characteristics for MMCi - SDR12 in receiver and transmitter mode (see 图 5-72 and 图 5-73).

表 5-68. Timing Requirements for MMCi - SDR12 Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SDR125	$t_{su(cmdV-clkH)}$	Setup time, MMCi_CMD valid before MMCi_CLK rising clock edge	9.96		ns
SDR126	$t_{h(clkH-cmdV)}$	Hold time, MMCi_CMD valid after MMCi_CLK rising clock edge	1.67		ns
SDR127	$t_{su(dV-clkH)}$	Setup time, MMCi_DAT[j:0] valid before MMCi_CLK rising clock edge	9.96		ns
SDR128	$t_{h(clkH-dV)}$	Hold time, MMCi_DAT[j:0] valid after MMCi_CLK rising clock edge	1.67		ns

(1) j in [j:0] is equal to 7 (for MMC0), or 3 (for MMC1).

表 5-69. Switching Characteristics for MMCi - SDR12 Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SDR120	$f_{op(clk)}$	Operating frequency, MMCi_CLK		25	MHz
SDR121	$t_{w(clkH)}$	Pulse duration, MMCi_CLK high	18.7		ns
SDR122	$t_{w(clkL)}$	Pulse duration, MMCi_CLK low	18.7		ns
SDR123	$t_{d(clkL-cmdV)}$	Delay time, MMCi_CLK falling clock edge to MMCi_CMD transition	-13.6	13.6	ns
SDR124	$t_{d(clkL-dV)}$	Delay time, MMCi_CLK falling clock edge to MMCi_DAT[j:0] transition	-13.6	13.6	ns

(1) j in [j:0] is equal to 7 (for MMC0), or 3 (for MMC1).

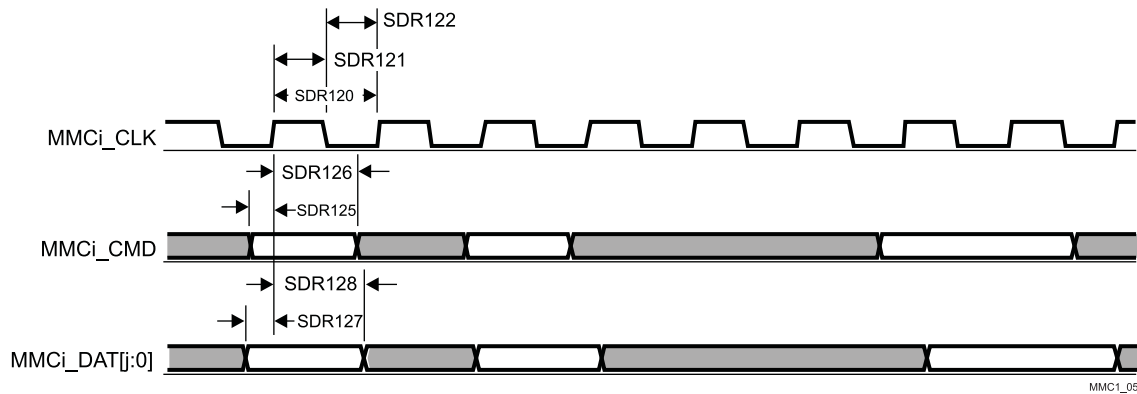


图 5-72. eMMC/SD/SDIO in - High Speed SDR12 - Receiver Mode

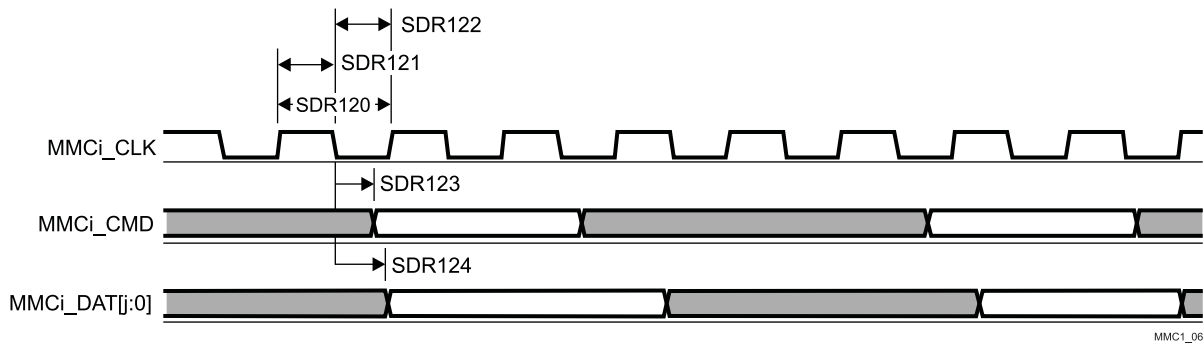


图 5-73. eMMC/SD/SDIO in - High Speed SDR12 - Transmitter Mode

5.9.5.16.1.4 UHS-I SDR25 Mode

表 5-70 和 表 5-71 呈现 Timing requirements and Switching characteristics for MMCi - SDR25 in receiver and transmitter mode (see 图 5-74 and 图 5-75).

表 5-70. Timing Requirements for MMCi - SDR25 Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SDR253	$t_{su(cmdV-clkH)}$	Setup time, MMCi_CMD valid before MMCi_CLK rising clock edge	2.15		ns
SDR254	$t_{h(clkH-cmdV)}$	Hold time, MMCi_CMD valid after MMCi_CLK rising clock edge	1.67		ns
SDR257	$t_{su(dV-clkH)}$	Setup time, MMCi_DAT[j:0] valid before MMCi_CLK rising clock edge	2.15		ns
SDR258	$t_{h(clkH-dV)}$	Hold time, MMCi_DAT[j:0] valid after MMCi_CLK rising clock edge	1.67		ns

(1) j in [j:0] is equal to 7 (for MMC0), or 3 (for MMC1).

表 5-71. Switching Characteristics for MMCi - SDR25 Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SDR251	$f_{op(clk)}$	Operating frequency, MMCi_CLK		50	MHz
SDR252H	$t_{w(clkH)}$	Pulse duration, MMCi_CLK high	9.2		ns
SDR252L	$t_{w(clkL)}$	Pulse duration, MMCi_CLK low	9.2		ns
SDR255	$t_{d(clkL-cmdV)}$	Delay time, MMCi_CLK falling clock edge to MMCi_CMD transition	-6.1	3.1	ns
SDR256	$t_{d(clkL-dV)}$	Delay time, MMCi_CLK falling clock edge to MMCi_DAT[j:0] transition	-6.1	3.1	ns

(1) j in [j:0] is equal to 7 (for MMC0), or 3 (for MMC1).

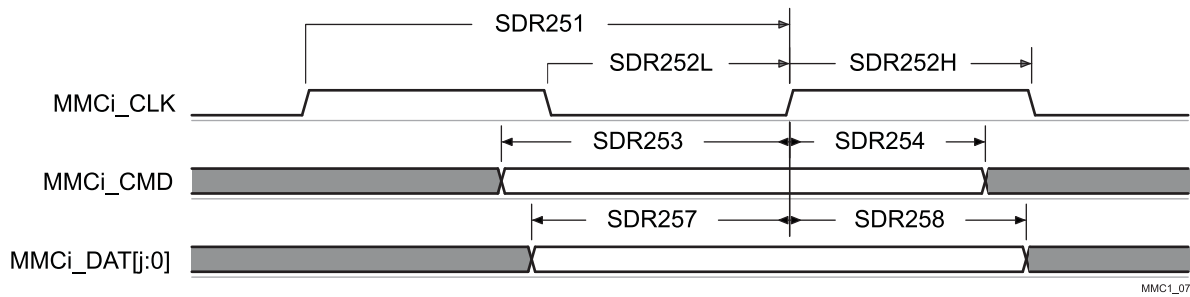


图 5-74. eMMC/SD/SDIO in - High Speed SDR25 - Receiver Mode

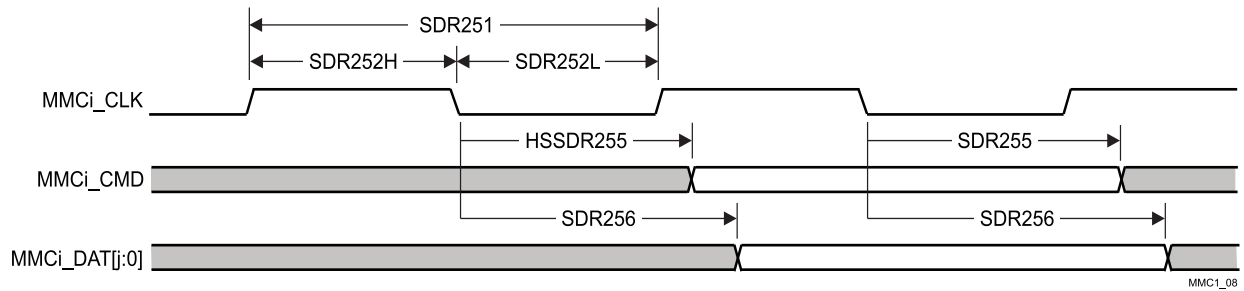


图 5-75. eMMC/SD/SDIO in - High Speed SDR25 - Transmitter Mode

5.9.5.16.1.5 UHS-I SDR50 Mode

and 表 5-72 present Timing requirements and Switching characteristics for MMCi - SDR50 in receiver and transmitter mode (see and 图 5-76).

表 5-72. Switching Characteristics for MMCi - SDR50 Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SDR501	$f_{op}(clk)$	Operating frequency, MMCi_CLK		100	MHz
SDR502H	$t_{w}(clkH)$	Pulse duration, MMCi_CLK high	4.45		ns
SDR502L	$t_{w}(clkL)$	Pulse duration, MMCi_CLK low	4.45		ns
SDR505	$t_{d}(clkL-cmdV)$	Delay time, MMCi_CLK rising clock edge to MMCi_CMD transition	1.2	6.35	ns
SDR506	$t_{d}(clkL-dV)$	Delay time, MMCi_CLK rising clock edge to MMCi_DAT[j:0] transition	1.2	6.35	ns

(1) j in [j:0] is equal to 7 (for MMC0), or 3 (for MMC1).

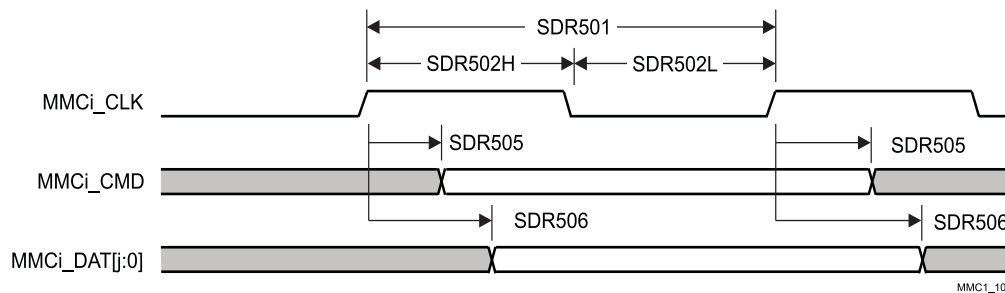


图 5-76. eMMC/SD/SDIO in - High Speed SDR50 - Transmitter Mode

5.9.5.16.1.6 UHS-I SDR104 / HS200 Mode

表 5-73 presents Timing requirements and Switching characteristics for MMCi - SDR104 in receiver and transmitter mode (see and 图 5-77)

表 5-73. Switching Characteristics for MMCi - SDR104 / HS200 Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SDR1041	$f_{op}(clk)$	Operating frequency, MMCi_CLK		200	MHz
SDR1042H	$t_w(clkH)$	Pulse duration, MMCi_CLK high	2.08		ns
SDR1042L	$t_w(clkL)$	Pulse duration, MMCi_CLK low	2.08		ns
SDR1045	$t_d(clk-cmdV)$	Delay time, MMCi_CLK rising clock edge to MMCi_CMD transition	1.12	3.16	ns
SDR1046	$t_d(clk-dV)$	Delay time, MMCi_CLK rising clock edge to MMCi_DAT[j:0] transition	1.12	3.16	ns

(1) j in [j:0] is equal to 7 (for MMC0), or 3 (for MMC1).

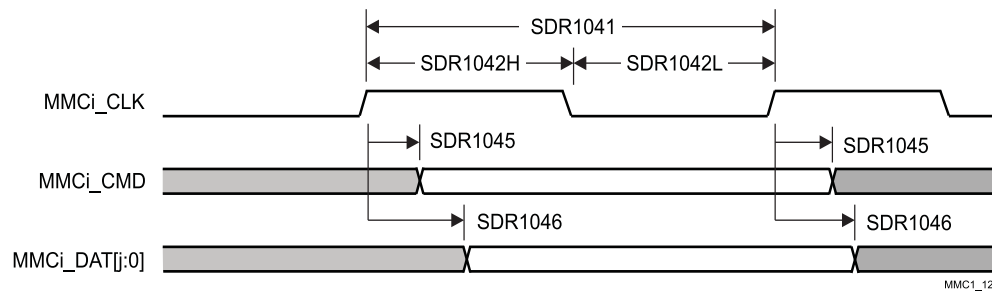


图 5-77. eMMC/SD/SDIO in - High Speed SDR104 / HS200 - Transmitter Mode

5.9.5.16.1.7 UHS-I DDR50 Mode

表 5-74 和 表 5-75 present Timing requirements and Switching characteristics for MMCi - DDR50 in receiver and transmitter mode (see 图 5-78 and 图 5-79).

表 5-74. Timing Requirements for MMCi - DDR50 Mode

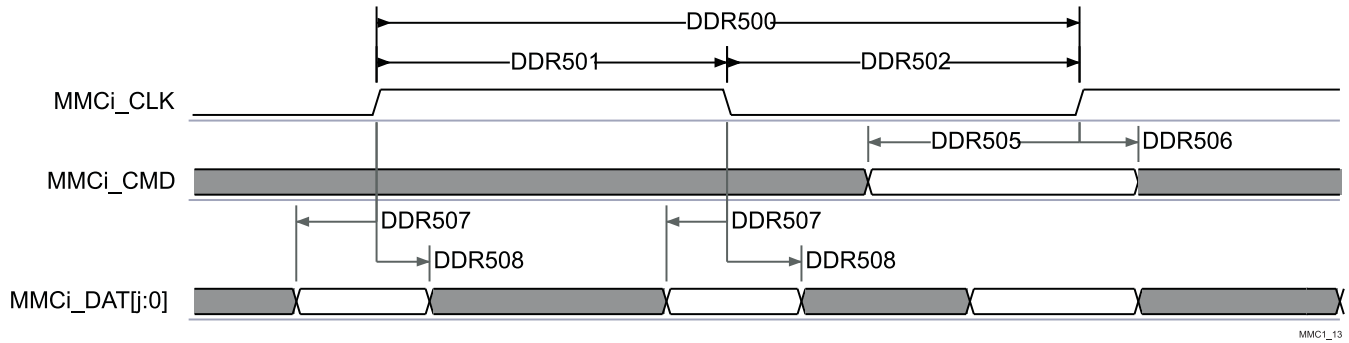
NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
DDR505	$t_{su}(cmdV-clk)$	Setup time, MMCi_CMD valid before MMCi_CLK rising clock edge	3.12		ns
DDR506	$t_h(clk-cmdV)$	Hold time, MMCi_CMD valid after MMCi_CLK rising clock edge	1.91		ns
DDR507	$t_{su}(dV-clk)$	Setup time, MMCi_DAT[j:0] valid before MMCi_CLK transition	-0.18		ns
DDR508	$t_h(clk-dV)$	Hold time, MMCi_DAT[j:0] valid after MMCi_CLK transition	1.67		ns

(1) j in [j:0] is equal to 7 (for MMC0), or 3 (for MMC1).

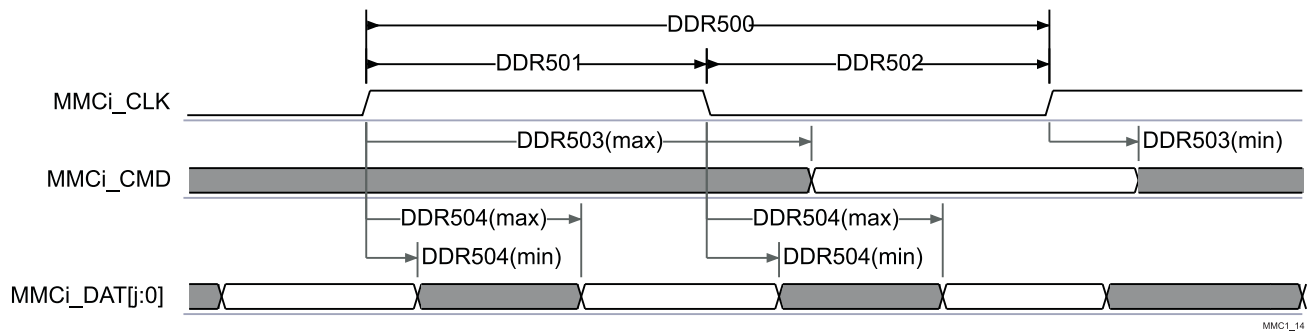
表 5-75. Switching Characteristics for MMCi - DDR50 Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
DDR500	$f_{op}(clk)$	Operating frequency, MMCi_CLK		50	MHz
DDR501	$t_w(clkH)$	Pulse duration, MMCi_CLK high	9.2		ns
DDR502	$t_w(clkL)$	Pulse duration, MMCi_CLK low	9.2		ns
DDR503	$t_d(clk-cmdV)$	Delay time, MMCi_CLK rising clock edge to MMCi_CMD transition	3.4	13.1	ns
DDR504	$t_d(clk-dV)$	Delay time, MMCi_CLK transition to MMCi_DAT[j:0] transition	2.9	6.1	ns

(1) j in [j:0] is equal to 7 (for MMC0), or 3 (for MMC1).



✎ 5-78. eMMC/SD/SDIO - High Speed SD - DDR - Data/Command Receive



✎ 5-79. eMMC/SD/SDIO - High Speed SD - DDR - Data/Command Transmit

表 5-76, shows the required DLL software configuration settings for MMC timing modes.

表 5-76. MMC DLL Delay Mapping for All Timing Modes

MODE	DESCRIPTION	DELAY VALUE MMCSdN_PHY_CTRL_4_REG[15:12] OTAPDLYSEL	DELAY ENABLE MMCSdN_PHY_CTRL_4_REG[20] OTAPDLYENA	DLL REFERENCE FREQUENCY MMCSdN_PHY_CTRL_5_REG[9] SEL100	DLL REFERENCE FREQUENCY MMCSdN_PHY_CTRL_5_REG[9] SEL50	STROBE DELAY MMCSd0_SS_PHY_CTL_RL_4_REG [27:24] STRBSEL
MMC Default Speed	Either 8-bit or 4-bit PHY operating in DS mode	0x0	0x0	0x0	0x0	0x0
MMC High Speed	Either 8-bit or 4-bit PHY operating in HS mode	0x0	0x0	0x0	0x0	0x0
MMC HS-DDR	Either 8-bit or 4-bit PHY operating in HS-DDR mode	0x0	0x0	0x0	0x0	0x0
MMC SDR50	Either 8-bit or 4-bit PHY operating in SDR50	0x8	0x1	0x1	0x0	0x0
MMC0 DDR50	8-bit PHY operating in DDR50 mode	0x5	0x1	0x0	0x1	0x0
MMC1 DDR50	4-bit PHY operating in DDR50 mode	0x4	0x1	0x0	0x1	0x0
MMC SDR104	Either 8-bit or 4-bit PHY operating in SDR104 mode	0x7	0x1	0x0	0x0	0x0
MMC HS200	Either 8-bit or 4-bit PHY operating in HS200 mode	0x5	0x1	0x0	0x0	0x0
MMC HS400	8-bit PHY operating in HS400 mode	0x0	0x1	0x0	0x0	0xF

For more information, see section *Multimedia Card/Secure Digital (MMC/SD) Interface* in the device TRM.

5.9.5.17 NAVSS

表 5-77, 表 5-78, 图 5-80, and 图 5-81 present timing requirement and switching characteristics of the CPTS interface.

表 5-77. Timing Requirements for CPTS Input

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
T1	$t_{w(HWTSPUSH)}$	HWTSPUSH Pulse duration, high	$6 + 12P^{(1)}$		ns
T2	$t_{w(HWTSPUSHL)}$	HWTSPUSH pulse duration, low	$6 + 12P^{(1)}$		ns
T3	$t_{c(RFT_CLK)}$	RFT_CLK cycle time	5	8	ns
T4	$t_{w(RFT_CLKH)}$	RFT_CLK pulse duration, high	$0.45 \times t_{c(RFT_CLK)}$		ns
T5	$t_{w(RFT_CLKL)}$	RFT_CLK pulse duration, low	$0.45 \times t_{c(RFT_CLK)}$		ns

(1) P = functional clock period in ns.

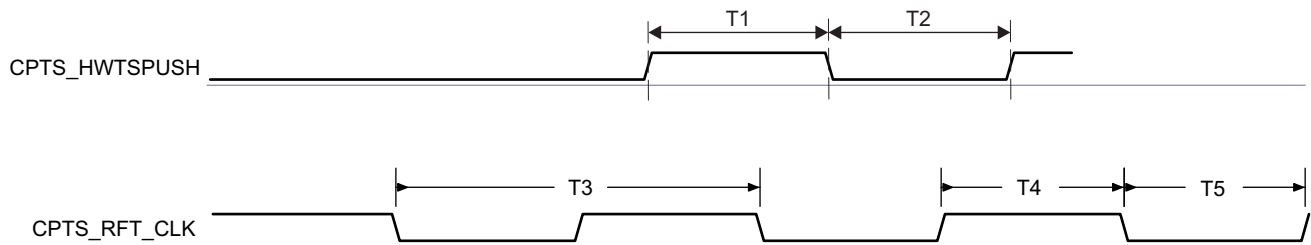


图 5-80. CPTS Input Timing

表 5-78. Switching Characteristics for CPTS Output

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
T6	$t_{w(TS_COMP)}$	NAVSS-CPTS TS_COMP, high	$-6 + 36P^{(1)}$		ns
T7	$t_{w(TS_COMPL)}$	NAVSS-CPTS TS_COMP, low	$-6 + 36P^{(1)}$		ns
T8	$t_{w(TS_COMP)}$	CPSW-CPTS TS_COMP, high	$-6 + 36P^{(1)}$		ns
T9	$t_{w(TS_COMPL)}$	CPSW-CPTS TS_COMP, low	$-6 + 36P^{(1)}$		ns
T10	$t_{w(TS_SYNCH)}$	NAVSS-CPTS TS_SYNC, high	$-6 + 36P^{(1)}$		ns
T11	$t_{w(TS_SYNCL)}$	NAVSS-CPTS TS_SYNC, low	$-6 + 36P^{(1)}$		ns
T12	$t_{w(TS_SYNCH)}$	CPSW-CPTS TS_SYNC, high	$-6 + 36P^{(1)}$		ns
T13	$t_{w(TS_SYNCL)}$	CPSW-CPTS TS_SYNC, low	$-6 + 36P^{(1)}$		ns
T14	$t_{w(SYNC_OUTH)}$	TS_SYNC sourcing SYNCn_OUT, high	$-6 + 36P^{(1)}$		ns
T15	$t_{w(SYNC_OUTL)}$	TS_SYNC sourcing SYNCn_OUT, low	$-6 + 36P^{(1)}$		ns
T16	$t_{w(SYNC_OUTH)}$	GENF sourcing SYNCn_OUT, high	$-6 + 5P^{(1)}$		ns
T17	$t_{w(SYNC_OUTL)}$	GENF sourcing SYNCn_OUT, low	$-6 + 5P^{(1)}$		ns

(1) P = functional clock period in ns.

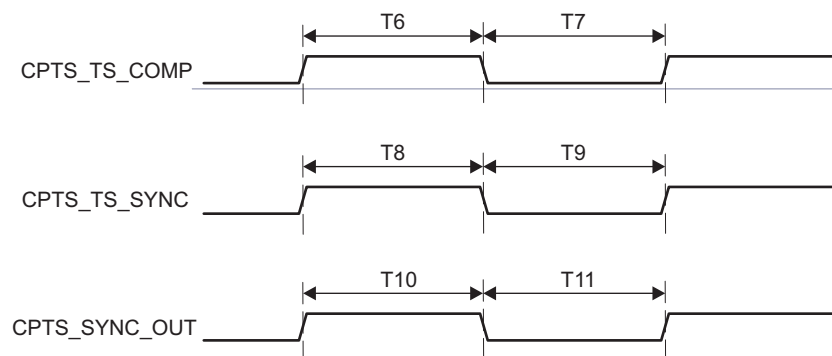


图 5-81. CPTS Output Switching Characteristics

For more information, see section *Navigator Subsystem (NAVSS)* in the device TRM.

5.9.5.18 OSPI

For more details about features and additional description information on the device Octal Serial Peripheral Interface, see the corresponding sections within [4.3, Signal Descriptions](#) and [6, Detailed Description](#).

5.9.5.18.1 OSPI with Data Training

表 5-79. OSPI Switching Characteristics - Data Training

PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
$t_{c(CLK)}$	Cycle time, CLK	DDR, 1.8V	6.02		ns
		DDR, 3.3V	7.52		ns
$t_{c(CLK)}$	Cycle time, CLK	SDR, 1.8V	5.00		ns
		SDR, 3.3V	7.52		ns

5.9.5.18.2 OSPI without Data Training

注

The I/O Timings provided in this section are only applicable when data training is not implemented. Additionally, the I/O Timings are valid only for some OSPI usage modes when the corresponding DLL Delays are configured as described in [表 5-84](#) found in this section.

[表 5-80](#), [表 5-81](#), [図 5-82](#), and [図 5-83](#) present switching characteristics for OSPI DDR and SDR Mode.

表 5-80. OSPI Switching Characteristics - DDR Mode ⁽¹⁾

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
O1	$t_{c(CLK)}$	Cycle time, CLK	1.8V	19		ns
			3.3V	19		ns
O2	$t_{w(CLKL)}$	Pulse duration, CLK low		$-0.3+0.475 \cdot P$ (2)		ns
O3	$t_{w(CLKH)}$	Pulse duration, CLK high		$-0.3+0.475 \cdot P$ (2)		ns
O4	$t_{d(CLK-CSn)}$	Delay time, CLK rising edge to CSn active edge	1.8V, OSPI0 DDR TX; 1.8V, OSPI1 DDR TX	$-7.7-0.475 \cdot P - 0.975 \cdot N \cdot R$ (3) (4) (5)	$0-0.475 \cdot P - 0.975 \cdot N \cdot R$ (3) (4) (5)	ns
			3.3V, OSPI0 DDR TX; 3.3V, OSPI1 DDR TX	$-8-0.475 \cdot P - 0.975 \cdot N \cdot R$ (3) (4) (5)	$0-0.475 \cdot P - 0.975 \cdot N \cdot R$ (3) (4) (5)	ns
O5	$t_{d(CLK-CSn)}$	Delay time, CLK rising edge to CSn inactive edge	1.8V, OSPI0 DDR TX; 1.8V, OSPI1 DDR TX	$-7.7+0.475 \cdot P + 0.975 \cdot N \cdot R$ (3) (4) (5)	$0+0.475 \cdot P + 0.975 \cdot N \cdot R$ (3) (4) (5)	ns
			3.3V, OSPI0 DDR TX; 3.3V, OSPI1 DDR TX	$-8+0.475 \cdot P + 0.975 \cdot N \cdot R$ (3) (4) (5)	$0+0.475 \cdot P + 0.975 \cdot N \cdot R$ (3) (4) (5)	ns
O6	$t_{d(CLK-D)}$	Delay time, CLK active edge to D[i:0] transition	1.8V, OSPI0 DDR TX; 1.8V, OSPI1 DDR TX	-7.7	-1.56	ns
			3.3V, OSPI0 DDR TX; 3.3V, OSPI1 DDR TX	-7.7	-1.56	ns

(1) i in [i:0] = 7 for OSPI0, i in [i:0] = 3 for OSPI1

(2) P = CLK cycle time

(3) P = SCLK period

(4) N = OSPI_DEV_DELAY_REG[D_INIT_FLD]

(5) R = refclk

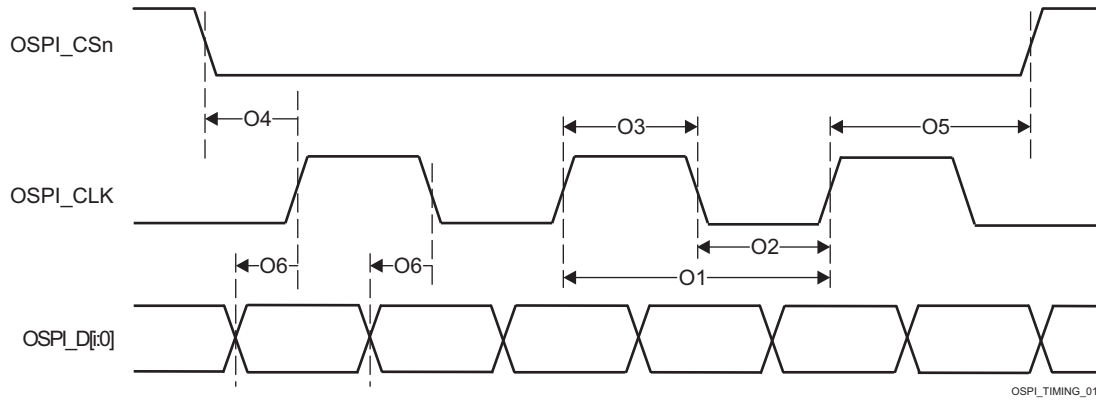


图 5-82. OSPI Switching Characteristics - DDR

表 5-81. OSPI Switching Characteristics - SDR Mode ⁽¹⁾

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
O7	$t_{c(CLK)}$	Cycle time, CLK	1.8V	7		ns
			3.3V	7.52		ns
O8	$t_{w(CLKL)}$	Pulse duration, CLK low		$-0.3+0.475 \cdot P$ (2)		ns
O9	$t_{w(CLKH)}$	Pulse duration, CLK high		$-0.3+0.475 \cdot P$ (2)		ns
O10	$t_d(CLK-CSn)$	Delay time, CLK rising edge to CSn active edge	1.8V	$-1-0.475 \cdot P - 0.975 \cdot N \cdot R$ (3) (4) (5)	$1-0.475 \cdot P - 0.975 \cdot N \cdot R$ (3) (4) (5)	ns
			3.3V	$-1-0.475 \cdot P - 0.975 \cdot N \cdot R$ (3) (4) (5)	$1-0.475 \cdot P - 0.975 \cdot N \cdot R$ (3) (4) (5)	ns
O11	$t_d(CLK-CSn)$	Delay time, CLK rising edge to CSn inactive edge	1.8V	$-1+0.475 \cdot P + 0.975 \cdot N \cdot R$ (3) (4) (5)	$1+0.475 \cdot P + 0.975 \cdot N \cdot R$ (3) (4) (5)	ns
			3.3V	$-1+0.475 \cdot P + 0.975 \cdot N \cdot R$ (3) (4) (5)	$1+0.475 \cdot P + 0.975 \cdot N \cdot R$ (3) (4) (5)	ns
O12	$t_d(CLK-D)$	Delay time, CLK active edge to D[i:0] transition	1.8V	-1.15	1.25	ns
			3.3V	-1.33	1.51	ns

(1) i in [i:0] = 7 for OSPI0, i in [i:0] = 3 for OSPI1

(2) P = CLK cycle time

(3) P = SCLK period

(4) N = OSPI_DEV_DELAY_REG[D_INIT_FLD]

(5) R = refclk

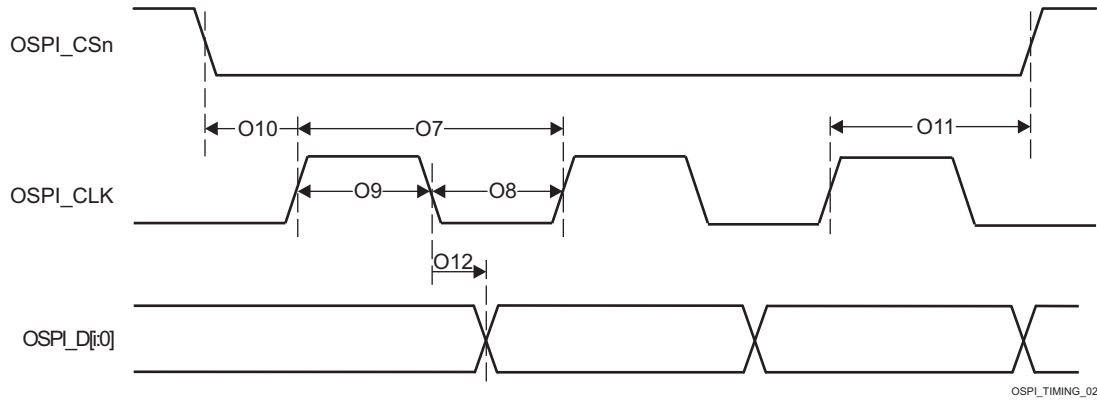


图 5-83. OSPI Switching Characteristics - SDR

表 5-82, 表 5-83, 图 5-84, 图 5-85, 图 5-86, and 图 5-87 presents timing requirements for OSPI DDR and SDR Mode.

表 5-82. OSPI Timing Requirements - DDR Mode ⁽¹⁾

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
O13	$t_{su(D-CLK)}$	Setup time, D[i:0] valid before active CLK edge	1.8V, No Loopback Clock; 1.8V, Internal Pad Loopback Clock	5.23		ns
			3.3V, No Loopback Clock; 3.3V, Internal Pad Loopback Clock	6.19		ns
O14	$t_{h(CLK-D)}$	Hold time, D[i:0] valid after active CLK edge	1.8V, No Loopback Clock; 1.8V, Internal Pad Loopback Clock	1.84		ns
			3.3V, No Loopback Clock; 3.3V, Internal Pad Loopback Clock	2.34		ns
O15	$t_{su(D-LBCLK)}$	Setup time, D[i:0] valid before active LBCLK (DQS) edge	1.8V, External Board Loopback Clock	0.52		ns
			3.3V, External Board Loopback Clock	1.97		ns
O16	$t_{h(LBCLK-D)}$	Hold time, D[i:0] valid after active LBCLK (DQS) edge	1.8V, External Board Loopback Clock	1.8 ⁽²⁾		ns
			3.3V, External Board Loopback Clock	2.2 ⁽²⁾		ns
O17	$t_{su(D-DQS)}$	Setup time, DQS edge to D[i:0] transition	1.8V, OSPI0 DQS; 1.8V, OSPI1 DQS	-0.46		ns
			3.3V, OSPI0 DQS; 3.3V, OSPI1 DQS	-0.66		ns
O18	$t_{h(DQS-D)}$	Hold time, DQS edge to D[i:0] transition	1.8V, OSPI0 DQS; 1.8V, OSPI1 DQS	3.59		ns
			3.3V, OSPI0 DQS; 3.3V, OSPI1 DQS	7.92		ns

- (1) i in $[i:0] = 7$ for OSPI0, i in $[i:0] = 3$ for OSPI1
- (2) This Hold time requirement is larger than the Hold time provided by a typical flash device. Therefore, the trace length between the SoC and flash device must be sufficiently long enough to ensure that the Hold time is met at the SoC. The length of the SoC's external loopback clock (OSPI_LBCLK to OSPI_DQS) may need to be shortened to compensate.

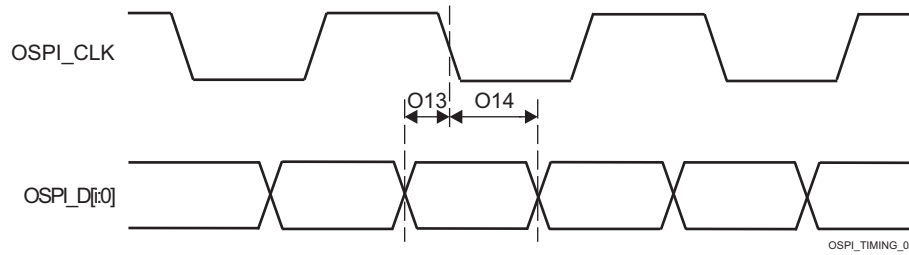


图 5-84. OSPI Timing Requirements - DDR, No Loopback Clock and Internal Pad Loopback Clock

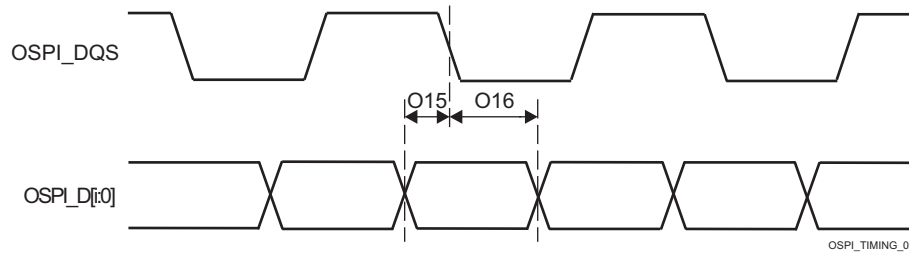


图 5-85. OSPI Timing Requirements - DDR, External Loopback Clock and DQS

表 5-83. OSPI Timing Requirements - SDR Mode ⁽¹⁾

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
O19	$t_{su}(D-CLK)$	Setup time, D[i:0] valid before active CLK edge	1.8V, No Loopback Clock	-2.18		ns
			3.3V, No Loopback Clock	-1.7		ns
O20	$t_h(CLK-D)$	Hold time, D[i:0] valid after active CLK edge	1.8V, No Loopback Clock	7.62		ns
			3.3V, No Loopback Clock	8.1		ns
O21	$t_{su}(D-LBCLK)$	Setup time, D[i:0] valid before active LBCLK input (DQS) edge	1.8V, External Board Loopback Clock	-3.24		ns
			3.3V, External Board Loopback Clock	-2.72		ns
O22	$t_h(LBCLK-D)$	Hold time, D[i:0] valid after active LBCLK input (DQS) edge	1.8V, External Board Loopback Clock	3.81		ns
			3.3V, External Board Loopback Clock	4.33		ns

- (1) i in $[i:0] = 7$ for OSPI0, i in $[i:0] = 3$ for OSPI1

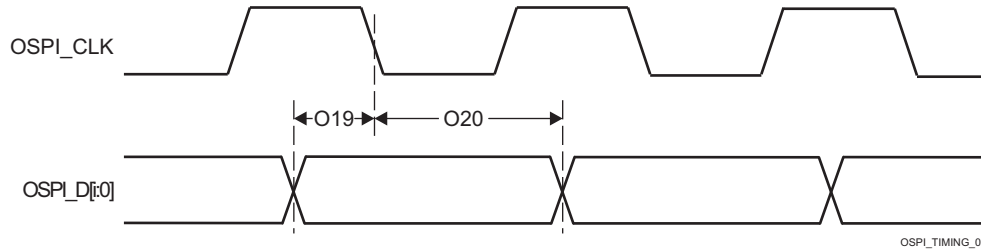


图 5-86. OSPI Timing Requirements - SDR, No Loopback Clock and Internal Pad Loopback Clock

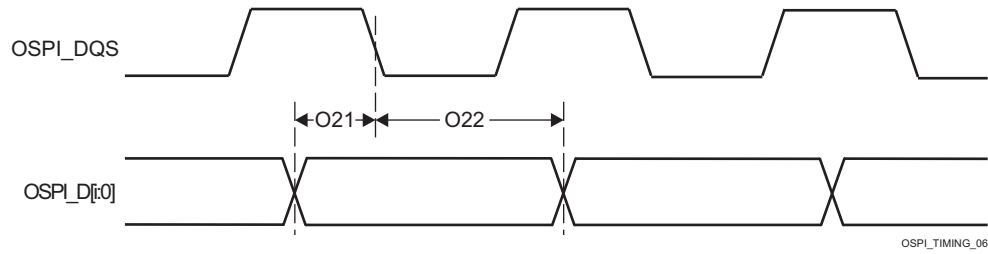


图 5-87. OSPI Timing Requirements - SDR, External Loopback Clock

表 5-84. OSPI DLL Delay Mapping for Timing Modes

MODE	OSPI_PHY_CONFIGURATION_REG BITFIELD	DELAY VALUE
1.8V, OSPI0 DDR TX	PHY_CONFIG_TX_DLL_DELAY_FLD	0x45
1.8V, OSPI1 DDR TX	PHY_CONFIG_TX_DLL_DELAY_FLD	0x4B
3.3V, OSPI0 DDR TX	PHY_CONFIG_TX_DLL_DELAY_FLD	0x46
3.3V, OSPI1 DDR TX	PHY_CONFIG_TX_DLL_DELAY_FLD	0x4C
1.8V, OSPI0 DQS	PHY_CONFIG_RX_DLL_DELAY_FLD	0x14
1.8V, OSPI1 DQS	PHY_CONFIG_RX_DLL_DELAY_FLD	0x16
3.3V, OSPI0 DQS	PHY_CONFIG_RX_DLL_DELAY_FLD	0x3A
3.3V, OSPI1 DQS	PHY_CONFIG_RX_DLL_DELAY_FLD	0x3E
All other modes	PHY_CONFIG_TX_DLL_DELAY_FLD, PHY_CONFIG_RX_DLL_DELAY_FLD	0x0

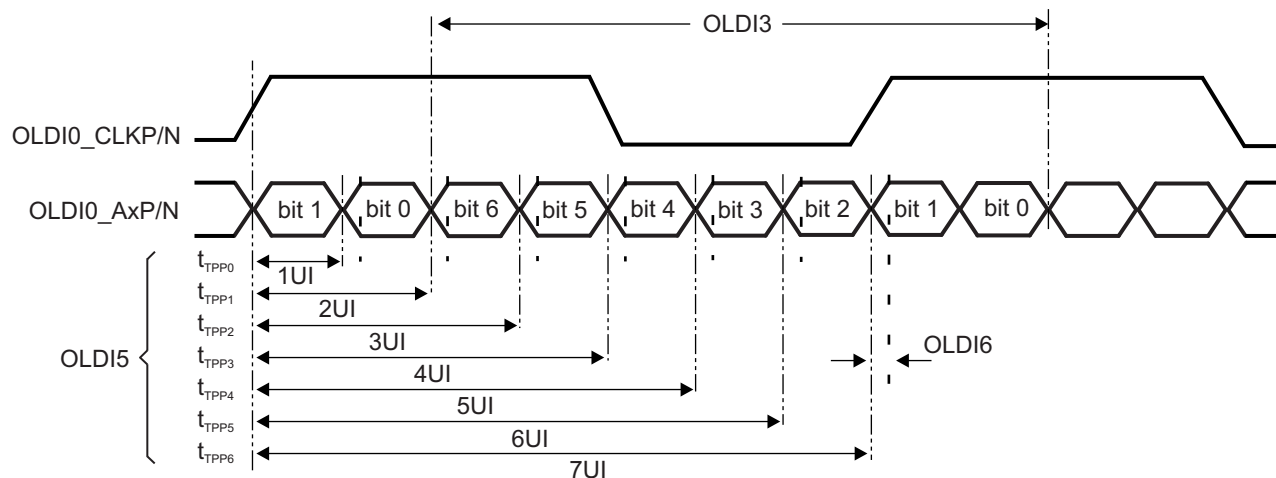
For more information, see section *Octal Serial Peripheral Interface (OSPI)* in the device TRM.

5.9.5.19 OLDI

表 5-85. OLDI Switching Characteristics

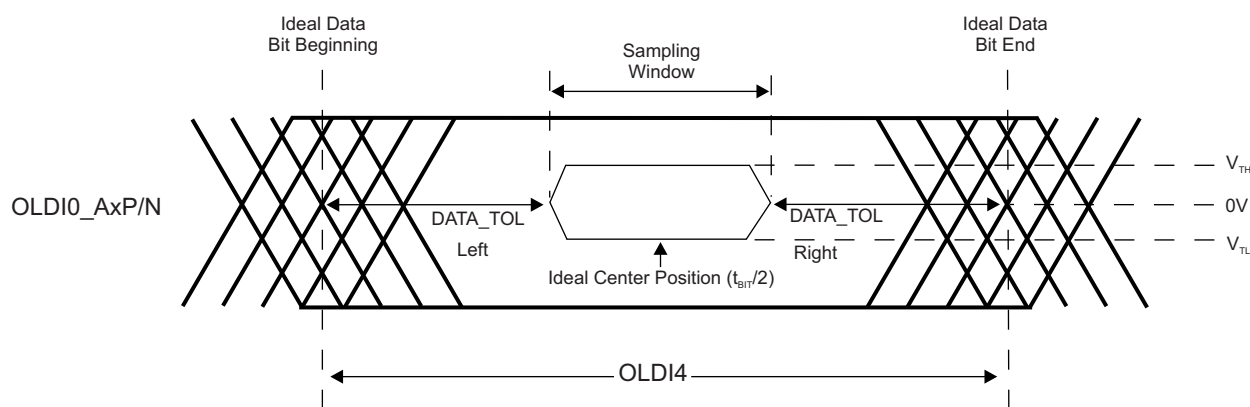
NO.	PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
OLDI1	$t_{l(LHTT)}$	Low-to-high transition time of LVDS differential signals: OLDI0_CLKP/N, OLDI0_AxP/N			0.5	ns
OLDI2	$t_{l(HLTT)}$	High-to-low transition time of LVDS differential signals: OLDI0_CLKP/N, OLDI0_AxP/N			0.5	ns
OLDI3	$t_c(CLK)$	Output pixel clock period (OLDI0_CLKP/N)	6.06		110.01	ns
OLDI4	$t_w(BIT)$	Output bit width (OLDI0_AxP/N)		1		UI
OLDI5	$t_{(TPPx, x=[6:0])}$	Output pulse positions normalized for each bit (OLDI0_AxP/N)		7-1		UI
OLDI6	$\Delta t_{(TPP)}$	Variation of pulse positions for each bit from their normalized center (OLDI0_AxP/N)	-0.06		0.06	UI
OLDI7	$t_{sk(TCCS)}$	Output channel to channel skew (OLDI0_CLKP/N, OLDI0_AxP/N)		110		ps
OLDI8	$t_j(TJCC)$	Output jitter cycle-to-cycle (OLDI0_CLKP/N, OLDI0_AxP/N)	0.028		0.035	UI
OLDI9	$t_j(IJIT)$	Total jitter tolerance (Includes data to clock skew, pulse position variation from normalized edges (OLDI0_AxP/N)			0.25	UI

- (1) x in OLDI0_AxP/N = [3:0]
- (2) UI = $t_{c(CLK)} / 7$



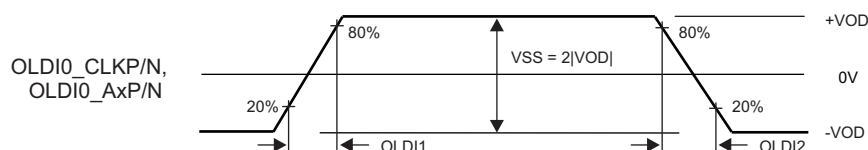
- (1) x in OLDI0_AxP/N = [3:0]

FIG 5-88. OLDI Output Pulse Positions



- (1) OLDI9 = DATA_TOL (Left+Right)
- (2) x in OLDI0_AxP/N = [3:0]

FIG 5-89. OLDI Data Output Jitter



- (1) x in OLDI0_AxP/N = [3:0]

FIG 5-90. LVDS Output Transition Times

For more information, see section *Display Subsystem (DSS)* in the device TRM.

5.9.5.20 PCIE

The PCI-Express Subsystem is compliant with the PCI Express Base Specification, revision 3.1. Refer to the specification for timing details.

For more details about features and additional description information on the device Peripheral Component Interconnect Express, see the corresponding sections within [4.3, Signal Descriptions](#) and [6, Detailed Description](#).

5.9.5.21 PRU_ICSSG

The device has integrated three identical PRU_ICSSG subsystems (PRU_ICSSG0, PRU_ICSSG1 and PRU_ICSSG2). The programmable nature of the PRU cores, along with their access to pins, events and all device resources, provides flexibility in implementing fast real-time responses, specialized data handling operations, custom peripheral interfaces, and in offloading tasks from the other processor cores of the device.

For more details about features and additional description information on the device Programmable Real-Time Unit Subsystem and Industrial Communication Subsystem - Gigabit, see the corresponding sections within [4.3, Signal Descriptions](#) and [6, Detailed Description](#).

注

The PRU_ICSSG_0 and PRU_ICSSG_1 support an internal wrapper multiplexing that expands the device top-level multiplexing. Signal naming in this section must match the internal wrapper multiplexing.

5.9.5.21.1 Programmable Real-Time Unit (PRU_ICSSG PRU)

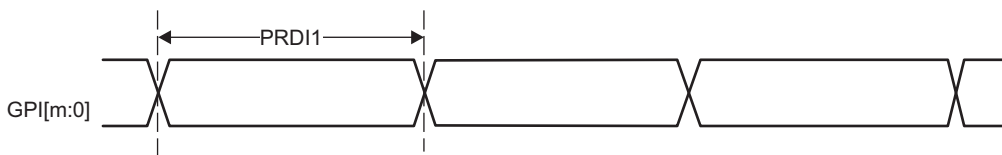
注

The PRU_ICSSG PRU signals have different functionality depending on the mode of operation. The signal naming in this section matches the naming used in the PRU Module Interface section in the device TRM.

5.9.5.21.1.1 PRU_ICSSG PRU Direct Input/Output Mode Electrical Data and Timing

表 5-86. PRU_ICSSG PRU Timing Requirements - Direct Input Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PRDI1	$t_{sk}(\text{PRU_DATAIN})$	PRU_DATAIN skew		2	ns



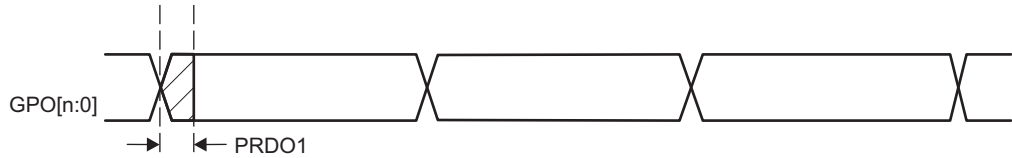
SPRS91X_TIMING_PRU_01

图 5-91. PRU_ICSSG PRU Direct Input Timing

(1) m in GPI[m:0] = 19.

表 5-87. PRU_ICSSG PRU Switching Characteristics - Direct Output Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PRDO1	$t_{sk}(\text{PRU_DATAOUT})$	PRU_DATAOUT skew		4	ns



SPRS91x_TIMING_PRU_02

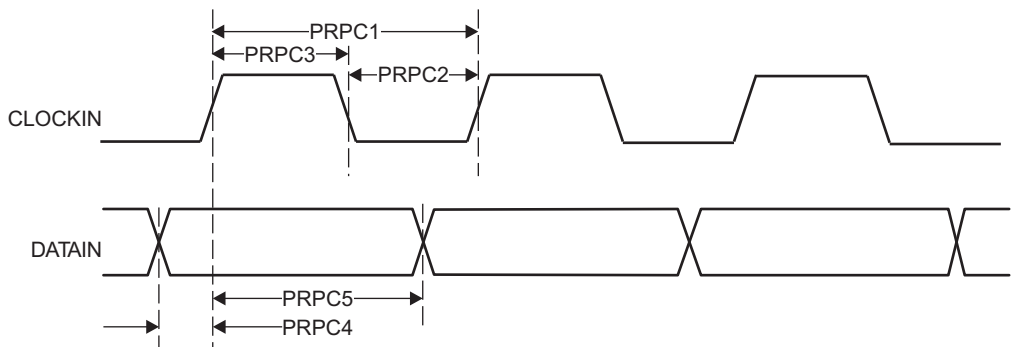
图 5-92. PRU_ICSSG PRU Direct Output Timing

(1) n in GPO[n:0] = 19.

5.9.5.21.1.2 PRU_ICSSG PRU Parallel Capture Mode Electrical Data and Timing

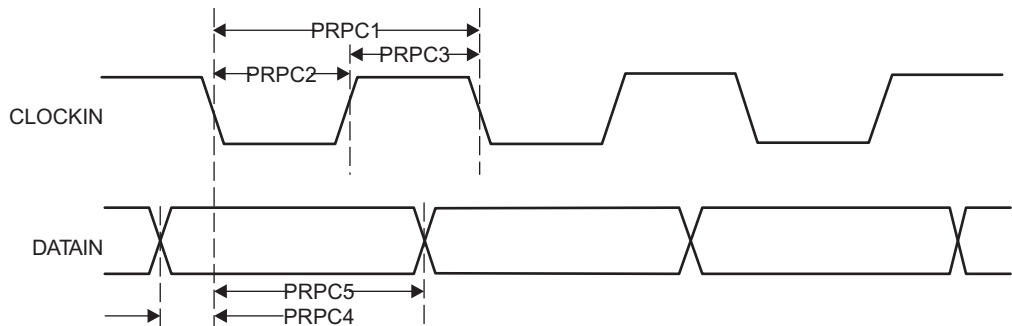
表 5-88. PRU_ICSSG PRU Timing Requirements - Parallel Capture Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PRPC1	$t_{c}(\text{PRU_CLOCK})$	Cycle time, PRU_CLOCK	20		ns
PRPC2	$t_{w}(\text{PRU_CLOCKL})$	Pulse Duration, PRU_CLOCK Low	10		ns
PRPC3	$t_{w}(\text{PRU_CLOCKH})$	Pulse Duration, PRU_CLOCK High	10		ns
PRPC4	$t_{su}(\text{PRU_DATAIN-PRU_CLOCK})$	Setup time, PRU_DATAIN valid before PRU_CLOCK active edge	4		ns
PRPC5	$t_{h}(\text{PRU_CLOCK-PRU_DATAIN})$	Hold time, PRU_DATAIN valid after PRU_CLOCK active edge	0		ns



SPRS91x_TIMING_PRU_03

图 5-93. PRU_ICSSG PRU Parallel Capture Timing – Rising Edge Mode



SPRS91x_TIMING_PRU_04

图 5-94. PRU_ICSSG PRU Parallel Capture Timing – Falling Edge Mode

5.9.5.21.1.3 PRU_ICSSG PRU Shift Mode Electrical Data and Timing

表 5-89. PRU_ICSSG PRU Timing Requirements - Shift In Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PRSI1	$t_w(\text{PRU_DATAINL})$	Pulse Duration, PRU_DATAIN Low	$2+2 \cdot P^{(1)}$		ns
PRSI2	$t_w(\text{PRU_DATAINH})$	Pulse Duration, PRU_DATAIN High	$2+2 \cdot P^{(1)}$		ns

(1) P = Internal shift in clock period, defined by PRU0_GPI_DIV0 and PRU0_GPI_DIV1 bit fields in the GPCFGn register.

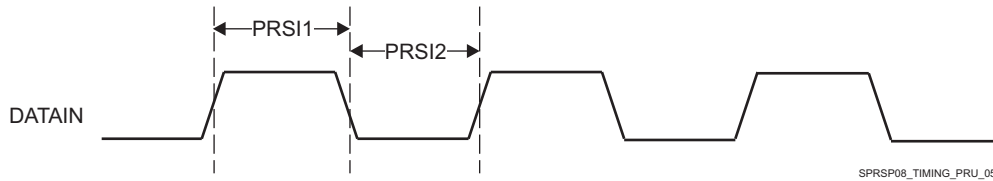


图 5-95. PRU_ICSSG PRU Shift In Timing

表 5-90. PRU_ICSSG PRU Switching Characteristics - Shift Out Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PRSO1	$t_c(\text{PRU_CLKOUT})$	Cycle time, PRU_CLKOUT	10		ns
PRSO2	$t_w(\text{PRU_CLKOUTL})$	Pulse Duration, PRU_CLKOUT Low	$-0.3 + 0.475 \cdot P \cdot Z^{(1)(2)}$		ns
PRSO3	$t_w(\text{PRU_CLKOUTH})$	Pulse Duration, PRU_CLKOUT High	$-0.3 + 0.475 \cdot P \cdot Y^{(1)(3)}$		ns
PRSO4	$t_d(\text{PRU_CLKOUT-PRU_DATAOUT})$	Delay time, PRU_CLKOUT to PRU_DATAOUT Valid	0	3	ns

(1) P = Software programmable shift out clock period, defined by PRU0_GPO_DIV0 and PRU0_GPO_DIV1 bit fields in the GPCFGn register.

(2) The Z parameter is defined as follows: If PRU0_GPI_DIV0 and PRU0_GPI_DIV1 are INTEGERS -or- if PRU0_GPI_DIV0 is a NON-INTEGERS and PRU0_GPI_DIV1 is an EVEN INTEGER then, Z equals $(\text{PRU0_GPI_DIV0} \cdot \text{PRU0_GPI_DIV1})$. If PRU0_GPI_DIV0 is a NON-INTEGERS and PRU0_GPI_DIV1 is an ODD INTEGER then, Z equals $(\text{PRU0_GPI_DIV0} \cdot \text{PRU0_GPI_DIV1} + 0.5)$. If PRU0_GPI_DIV0 is an INTEGER and PRU0_GPI_DIV1 is a NON-INTEGERS then, Z equals $(\text{PRU0_GPI_DIV0} \cdot \text{PRU0_GPI_DIV1} + 0.5 \cdot \text{PRU0_GPI_DIV0})$. If PRU0_GPI_DIV0 and PRU0_GPI_DIV1 are NON-INTEGERS then, Z equals $(\text{PRU0_GPI_DIV0} \cdot \text{PRU0_GPI_DIV1} + 0.25 \cdot \text{PRU0_GPI_DIV0})$.

(3) The Y parameter is defined as follows: If PRU0_GPI_DIV0 and PRU0_GPI_DIV1 are INTEGERS -or- if PRU0_GPI_DIV0 is a NON-INTEGERS and PRU0_GPI_DIV1 is an EVEN INTEGER then, Y equals $(\text{PRU0_GPI_DIV0} \cdot \text{PRU0_GPI_DIV1})$. If PRU0_GPI_DIV0 is a NON-INTEGERS and PRU0_GPI_DIV1 is an ODD INTEGER then, Y equals $(\text{PRU0_GPI_DIV0} \cdot \text{PRU0_GPI_DIV1} - 0.5)$. If PRU0_GPI_DIV0 is an INTEGER and PRU0_GPI_DIV1 is a NON-INTEGERS then, Y equals $(\text{PRU0_GPI_DIV0} \cdot \text{PRU0_GPI_DIV1} - 0.5 \cdot \text{PRU0_GPI_DIV0})$. If PRU0_GPI_DIV0 and PRU0_GPI_DIV1 are NON-INTEGERS then, Y1 equals $(\text{PRU0_GPI_DIV0} \cdot \text{PRU0_GPI_DIV1} - 0.25 \cdot \text{PRU0_GPI_DIV0})$ and Y2 equals $(\text{PRU0_GPI_DIV0} \cdot \text{PRU0_GPI_DIV1} + 0.25 \cdot \text{PRU0_GPI_DIV0})$, where Y1 is the first high pulse and Y2 is the second high pulse.

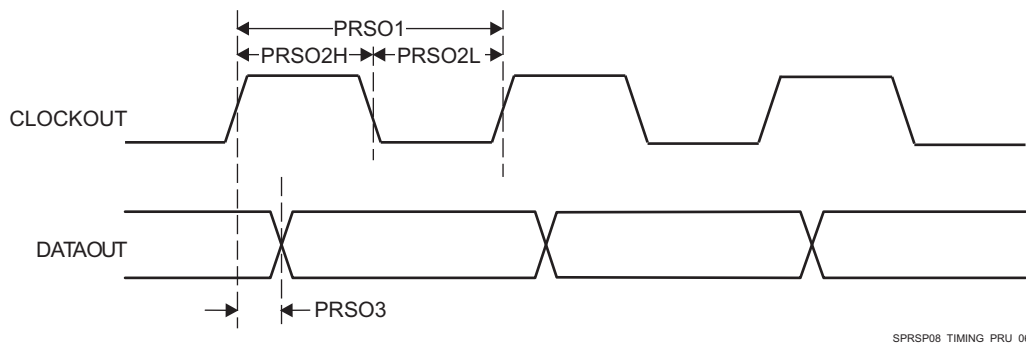


图 5-96. PRU_ICSSG PRU Shift Out Timing

5.9.5.21.1.4 PRU_ICSSG PRU Sigma Delta and Peripheral Interface Modes Electrical Data and Timing

表 5-91. PRU_ICSSG PRU Timing Requirements - Sigma Delta Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PRSD1	$t_{c(SD_CLK)}$	Cycle time, SD_CLK	40		ns
PRSD2L	$t_{w(SD_CLKL)}$	Pulse Duration, SD_CLK Low	20		ns
PRSD2H	$t_{w(SD_CLKH)}$	Pulse Duration, SD_CLK High	20		ns
PRSD3	$t_{su(SD_DATA-SD_CLK)}$	Setup time, SD_DATA valid before SD_CLK active edge	10		ns
PRSD4	$t_{h(SD_CLK-SD_DATA)}$	Hold time, SD_DATA valid before SD_CLK active edge	5		ns

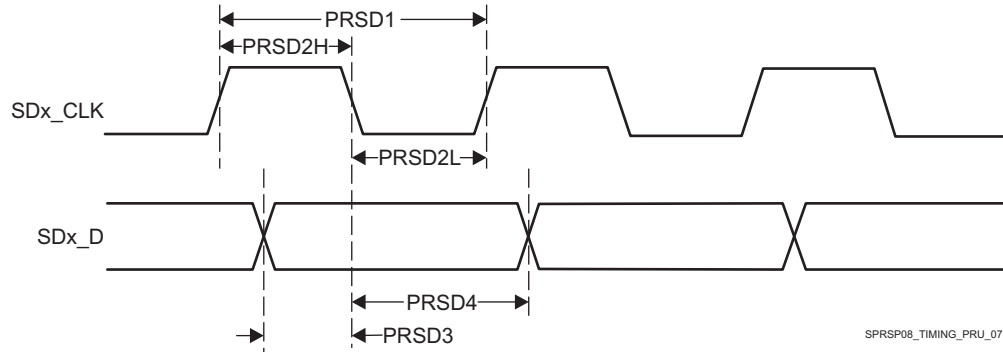


图 5-97. PRU_ICSSG PRU SD_CLK Falling Active Edge

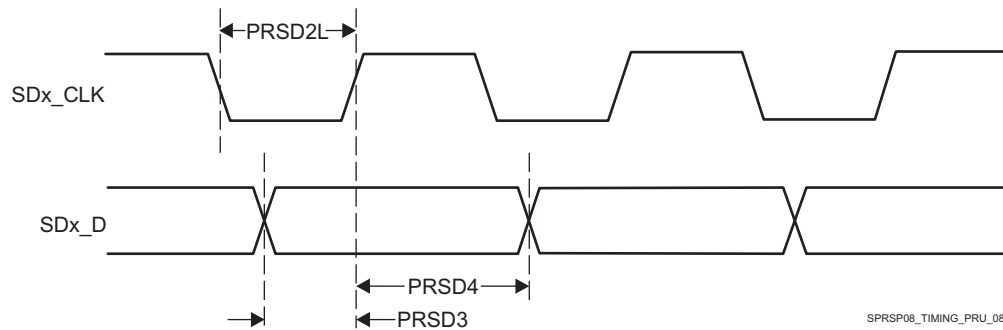


图 5-98. PRU_ICSSG PRU SD_CLK Rising Active Edge

表 5-92. PRU_ICSSG PRU Timing Requirements - Peripheral Interface Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PRPIF1	$t_{w(PIF_DATA_INH)}$	Pulse Duration, PIF_DATA_IN High	$2 + 0.475 \cdot (4 \cdot P)^{(1)}$		ns
PRPIF2	$t_{w(PIF_DATA_INL)}$	Pulse Duration, PIF_DATA_IN Low	$2 + 0.475 \cdot (4 \cdot P)^{(1)}$		ns

(1) $P = 1x$ (or TX) clock period, defined by TX_DIV_FACTOR and TX_DIV_FACTOR_FRAC in the CFG_ED_Pn_TXCFG register.

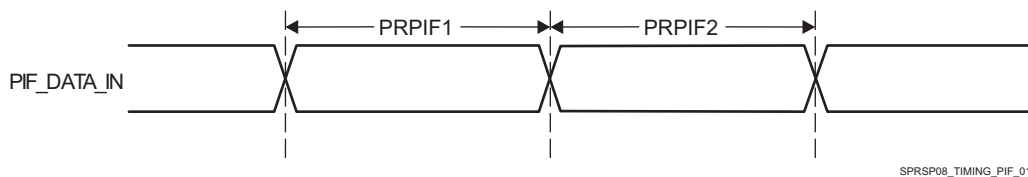


图 5-99. PRU_ICSSG PRU Peripheral Interface Timing

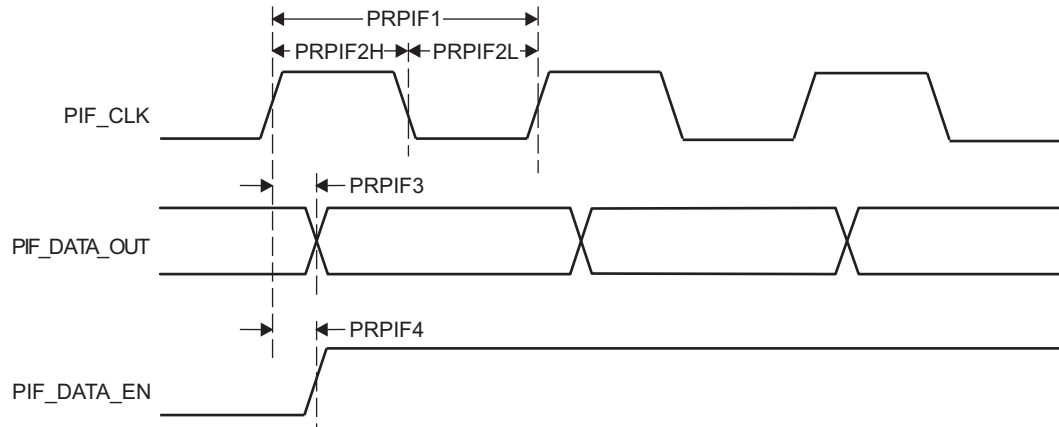
表 5-93. PRU_ICSSG PRU Switching Characteristics - Peripheral Interface Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PRPIF1	$t_{c(PIF_CLK)}$	Cycle time, PIF_CLK	30		ns

表 5-93. PRU_ICSSG PRU Switching Characteristics - Peripheral Interface Mode (continued)

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PRPIF2H	$t_{w(PIF_DATA_INH)}$	Pulse Duration, PIF_CLK High	$0 + 0.475 \cdot P^{(1)}$		ns
PRPIF2L	$t_{w(PIF_DATA_INL)}$	Pulse Duration, PIF_CLK Low	$0 + 0.475 \cdot P^{(1)}$		ns
PRPIF3	$t_d(PIF_CLK-PIF_DATA_OUT)$	Delay time, PIF_CLK fall to PIF_DATA_OUT	-5	5	ns
PRPIF4	$t_d(PIF_CLK-PIF_DATA_EN)$	Delay time, PIF_CLK fall to PIF_DATA_EN	-5	5	ns

(1) $P = 1x$ (or TX) clock period, defined by TX_DIV_FACTOR and TX_DIV_FACTOR_FRAC in the CFG_ED_Pn_TXCFG register.



SPRSP08_TIMING_PIF_02

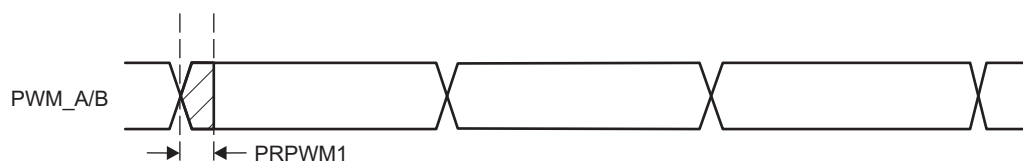
图 5-100. PRU_ICSSG PRU Peripheral Interface Switching Characteristics

5.9.5.21.2 PRU_ICSSG Pulse Width Modulation (PWM)

5.9.5.21.2.1 PRU_ICSSG PWM Electrical Data and Timing

表 5-94. PRU_ICSSG PWM Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PRPWM1	$t_{sk(PWM_A/B)}$	PWM_A/B skew		5	ns



SPRSP08_TIMING_PRU_PWM_01

图 5-101. PRU_ICSSG PRU PWM Timing

5.9.5.21.3 PRU_ICSSG Industrial Ethernet Peripheral (PRU_ICSSG IEP)

5.9.5.21.3.1 PRU_ICSSG IEP Electrical Data and Timing

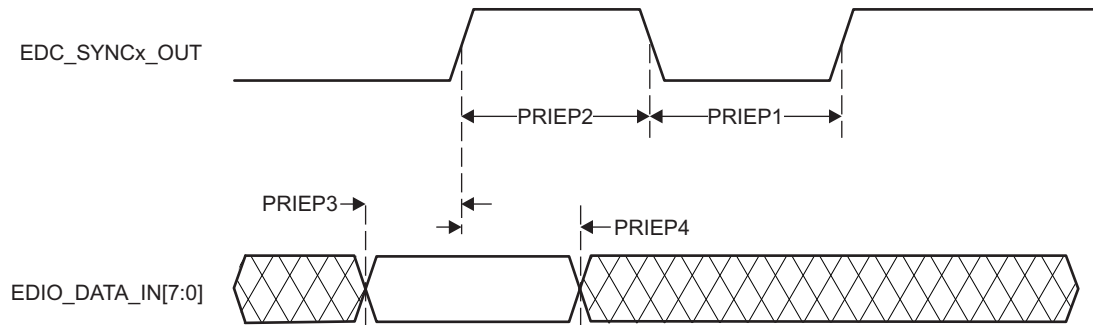
表 5-95. PRU_ICSSG IEP Timing Requirements - Input Validated with SYNCx

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PRIEP1	$t_{w(EDC_SYNCx_OUTL)}$	Pulse Duration, EDC_SYNCx_OUT Low	$-2+20 \cdot P^{(1)}$		ns
PRIEP2	$t_{w(EDC_SYNCx_OUTH)}$	Pulse Duration, EDC_SYNCx_OUT High	$-2+20 \cdot P^{(1)}$		ns

表 5-95. PRU_ICSSG IEP Timing Requirements - Input Validated with SYNCx (continued)

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PRIEP3	$t_{su}(EDIO_DATA_IN-EDC_SYNCx_OUT)$	Setup time, EDIO_DATA_IN valid before EDC_SYNCx_OUT active edge	20		ns
PRIEP4	$t_{h}(EDC_SYNCx_OUT-EDIO_DATA_IN)$	Hold time, EDIO_DATA_IN valid after EDC_SYNCx_OUT active edge	20		ns

(1) P = PRU-ICSS IEP clock source period.



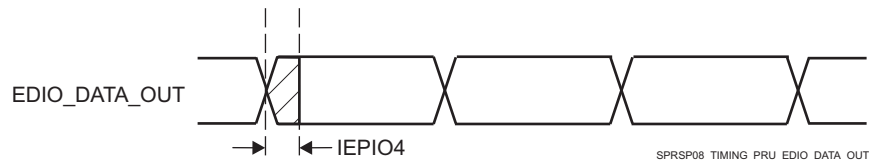
SPRSP08_TIMING_PRU_IEP_01

图 5-102. PRU_ICSSG PRU IEP SYNCx Timing

表 5-96. PRU_ICSSG IEP Timing Requirements - Digital IOs

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
IEPIO1	$t_w(EDIO_OUTVALIDL)$	Pulse Duration, EDIO_OUTVALID Low	$-2+14 \cdot P^{(1)}$		ns
IEPIO2	$t_w(EDIO_OUTVALIDH)$	Pulse Duration, EDIO_OUTVALID High	$-2+32 \cdot P^{(1)}$		ns
IEPIO3	$t_d(EDIO_OUTVALID-EDIO_DATA_OUT)$	Delay time, EDIO_OUTVALID to EDIO_DATA_OUT	0	$0+18 \cdot P^{(1)}$	ns
IEPIO4	$t_{sk}(EDIO_DATA_OUT)$	EDIO_DATA_OUT skew	5		ns

(1) P = PRU-ICSS IEP clock source period.



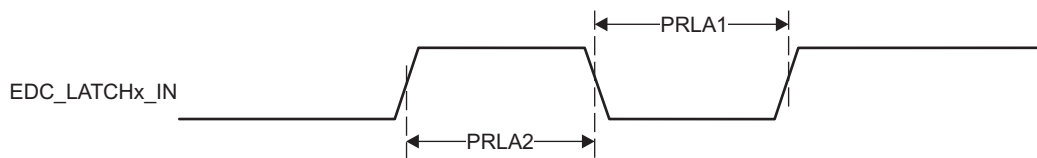
SPRSP08_TIMING_PRU_EDIO_DATA_OUT

图 5-103. PRU_ICSSG PRU IEP Digital IOs Timing

表 5-97. PRU_ICSSG IEP Timing Requirements - LATCHx_IN

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PRLA1	$t_w(EDC_LATCHx_INL)$	Pulse Duration, EDC_LATCHx_IN Low	$2+3 \cdot P^{(1)}$		ns
PRLA2	$t_w(EDC_LATCHx_INH)$	Pulse Duration, EDC_LATCHx_IN High	$2+3 \cdot P^{(1)}$		ns

(1) P = PRU-ICSS IEP clock source period.



SPRSP08_TIMING_PRU_IEP_02

图 5-104. PRU_ICSSG PRU IEP LATCHx_IN Timing

5.9.5.21.4 PRU_ICSSG Universal Asynchronous Receiver Transmitter (PRU-ICSS UART)

5.9.5.21.4.1 PRU_ICSSG UART Electrical Data and Timing

表 5-98. PRU_ICSSG UART Timing Requirements

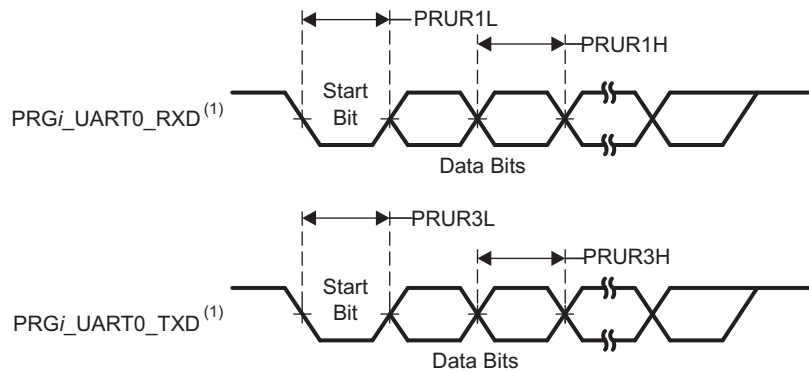
NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PRUR1H	$t_{w(RXH)}$	Pulse Duration, Receive start, stop, data bit High	0+U ⁽¹⁾		ns
PRUR1L	$t_{w(RXL)}$	Pulse Duration, Receive start, stop, data bit Low	-2+U ⁽¹⁾		ns

(1) U = UART baud time = 1/programmed baud rate.

表 5-99. PRU_ICSSG UART Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PRUR2	f(baud)	Maximum programmable baud rate			
PRUR3L	$t_{w(TXH)}$	Pulse Duration, Transmit start, stop, data bit High	0+U ⁽¹⁾		ns
PRUR3H	$t_{w(TXL)}$	Pulse Duration, Transmit start, stop, data bit Low	-2+U ⁽¹⁾		ns

(1) U = UART baud time = 1/programmed baud rate.



(1) i in PRGi_UART0_RXD and PRGi_UART0_TXD = 0, 1 or 2

SPRS91x_TIMING_PRU_UART_01

图 5-105. PRU_ICSSG UART Timing

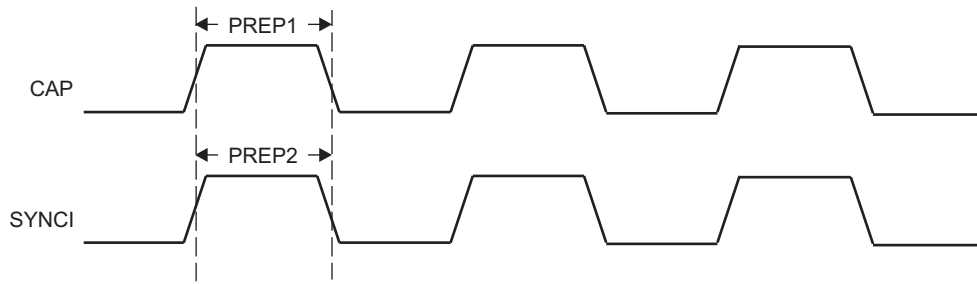
5.9.5.21.5 PRU_ICSSG Enhanced Capture Peripheral (PRU-ICSS ECAP)

5.9.5.21.5.1 PRU_ICSSG ECAP Electrical Data and Timing

表 5-100. PRU_ICSSG ECAP Timing Requirements

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PREP1	$t_{w(CAP)}$	Pulse Duration, Capture input (asynchronous)	2+2*P ⁽¹⁾		ns
PREP2	$t_{w(SYNCI)}$	Pulse Duration, Sync input (asynchronous)	2+2*P ⁽¹⁾		ns

(1) P = core_clk period



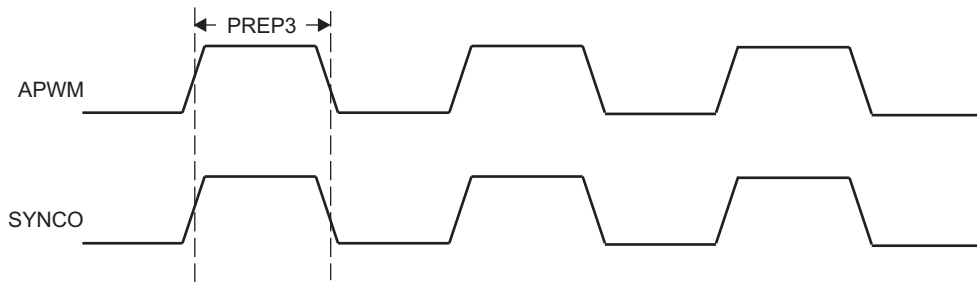
SPRSP08_TIMING_ECAPH_01

图 5-106. PRU_ICSSG ECAP Timing

表 5-101. PRU_ICSSG ECAP Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PREP3	$t_{W(APWM)}$	Pulse Duration, Auxillary PWM (APWM) output	$0+2 \cdot P^{(1)}$		ns
PREP4	$t_{W(SYNCO)}$	Pulse Duration, Sync output (asynchronous)	$0+P^{(1)}$		ns

(1) P = core_clk period



SPRSP08_TIMING_ECAPH_02

图 5-107. PRU_ICSSG ECAP Switching Characteristics

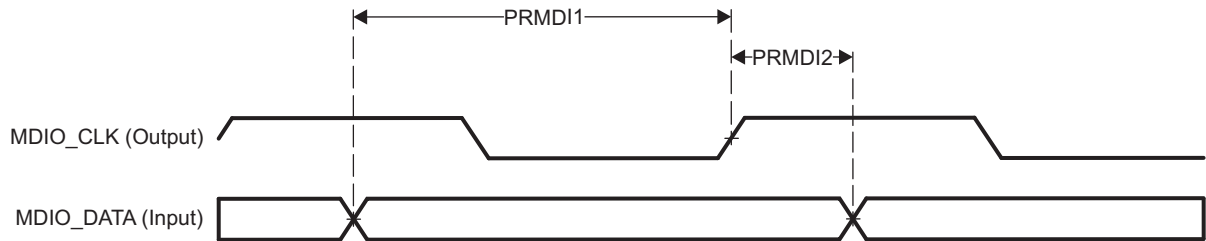
5.9.5.21.6 PRU_ICSSG RGMII, MII_RT, and Switch

5.9.5.21.6.1 PRU_ICSSG MDIO Electrical Data and Timing

表 5-102. PRU_ICSSG MDIO Timing Requirements – MDIO_DATA

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PRMDI1	$t_{su(MDIO-MDC)}$	Setup time, MDIO valid before MDC High	90		ns
PRMDI2	$t_{h(MDC-MDIO)}$	Hold time, MDIO valid from MDC High	0		ns

(1) P = Cycle time

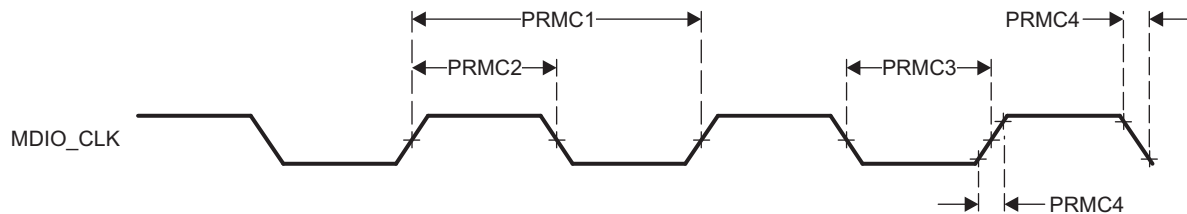


SPRS91x_TIMING_PRU_MII_RT_01

图 5-108. PRU_ICSSG MDIO_DATA Timing – Input Mode

表 5-103. PRU_ICSSG MDIO Switching Characteristics – MDIO_CLK

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PRMC1	$t_{c(MDC)}$	Cycle time, MDC	400		ns
PRMC2	$t_{w(MDCH)}$	Pulse Duration, MDC High	160		ns
PRMC3	$t_{w(MDCL)}$	Pulse Duration, MDC Low	160		ns
PRMC4	$t_{t(MDC)}$	Transition time, MDC		5	ns

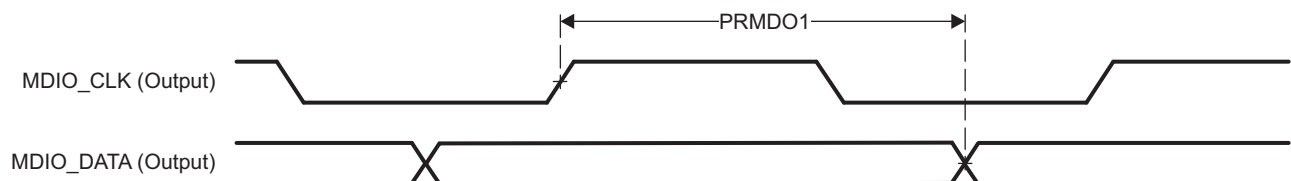


SPRS91x_TIMING_PRU_MII_RT_02

图 5-109. PRU_ICSSG MDIO_CLK Timing

表 5-104. PRU_ICSSG MDIO Switching Characteristics – MDIO_DATA

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PRMDO1	$t_{d(MDC-MDIO)}$	Delay time, MDC High to MDIO valid	10		ns



SPRS91x_TIMING_PRU_MII_RT_03

图 5-110. PRU_ICSSG MDIO_DATA Timing – Output Mode

5.9.5.21.6.2 PRU_ICSSG RGMII Electrical Data and Timing

表 5-105. PRU_ICSSG RGMII Timing Requirements - RGMII_RCLK

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
PRRG1	$t_{c(RXC)}$	Cycle time, RXC	10 Mbps	TBD	TBD	ns
			100 Mbps	TBD	TBD	ns
			1000 Mbps	7.2	8.8	ns
PRRG2	$t_{w(RXCH)}$	Pulse duration, RXC high	10 Mbps	TBD	TBD	ns
			100 Mbps	TBD	TBD	ns
			1000 Mbps	3.6	4.4	ns
PRRG3	$t_{w(RXCL)}$	Pulse duration, RXC low	10 Mbps	TBD	TBD	ns
			100 Mbps	TBD	TBD	ns
			1000 Mbps	3.6	4.4	ns
PRRG4	$t_{l(RXC)}$	Transition time, RXC	10 Mbps		TBD	ns
			100 Mbps		TBD	ns
			1000 Mbps		0.75	ns

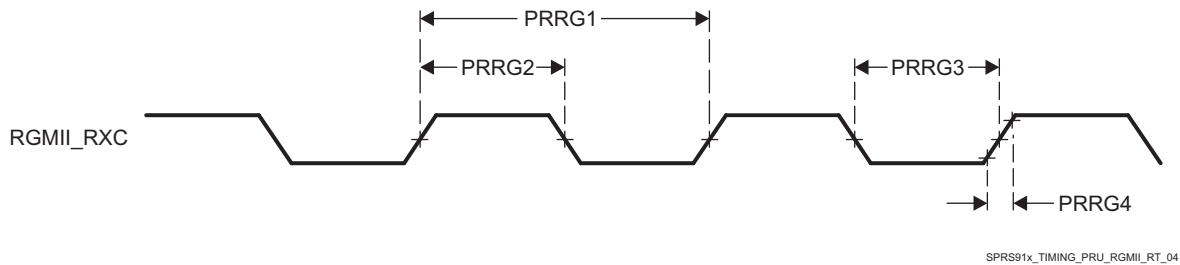
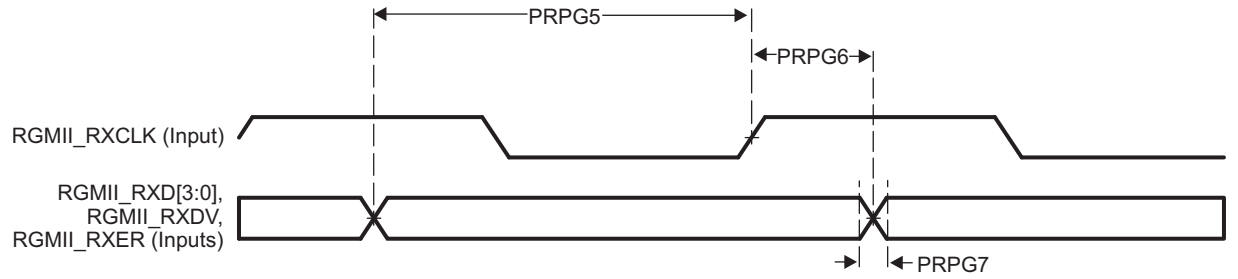


图 5-111. PRU_ICSSG RGMII_RCLK Input Timing

表 5-106. PRU_ICSSG RGMII Timing Requirements - RGMII_RD[3:0] and RGMII_RCTL

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
PRRG5	$t_{su(RD-RXC)}$	Setup time, RD[3:0] valid before RXC high/low	10 Mbps	TBD		ns
			100 Mbps	TBD		ns
			1000 Mbps	1		ns
	$t_{su(RX_CTL-RXC)}$	Setup time, RX_CTL valid before RXC high/low	10 Mbps	TBD		ns
			100 Mbps	TBD		ns
			1000 Mbps	1		ns
PRRG6	$t_{h(RXC-RD)}$	Hold time, RD[3:0] valid after RXC high/low	10 Mbps	TBD		ns
			100 Mbps	TBD		ns
			1000 Mbps	1		ns
	$t_{h(RXC-RX_CTL)}$	Hold time, RX_CTL valid after RXC high/low	10 Mbps	TBD		ns
			100 Mbps	TBD		ns
			1000 Mbps	1		ns
PRRG7	$t_{l(RD)}$	Transition time, RD	10 Mbps		TBD	ns
			100 Mbps		TBD	ns
			1000 Mbps		0.75	ns
	$t_{l(RX_CTL)}$	Transition time, RX_CTL	10 Mbps		TBD	ns
			100 Mbps		TBD	ns
			1000 Mbps		0.75	ns

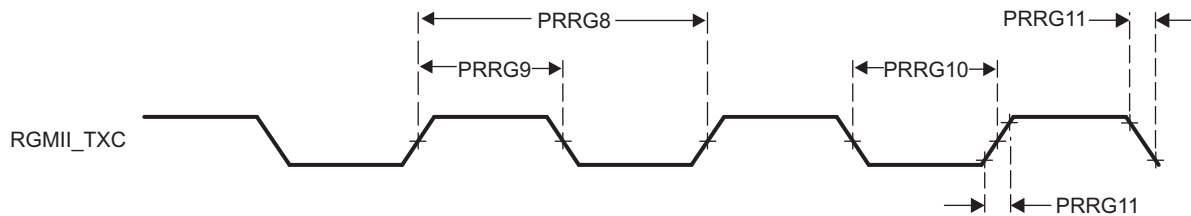


SPRS91x_TIMING_PRU_RGMII_RT_05

图 5-112. PRU_ICSSG RGMII_RD[3:0] and RGMII_RCTL Input Timing

表 5-107. PRU_ICSSG RGMII Switching Characteristics - RGMII_TCLK

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
PRRG8	$t_{c(TXC)}$	Cycle time, TXC	10 Mbps	TBD	TBD	ns
			100 Mbps	TBD	TBD	ns
			1000 Mbps	7.2	8.8	ns
PRRG9	$t_{w(TXCH)}$	Pulse duration, TXC high	10 Mbps	TBD	TBD	ns
			100 Mbps	TBD	TBD	ns
			1000 Mbps	3.6	4.4	ns
PRRG10	$t_{w(TXCL)}$	Pulse duration, TXC low	10 Mbps	TBD	TBD	ns
			100 Mbps	TBD	TBD	ns
			1000 Mbps	3.6	4.4	ns
PRRG11	$t_{l(TXC)}$	Transition time, TXC	10 Mbps		TBD	ns
			100 Mbps		TBD	ns
			1000 Mbps		0.75	ns



SPRS91x_TIMING_PRU_RGMII_RT_06

图 5-113. PRU_ICSSG RGMII_RCLK Output Timing

表 5-108. PRU_ICSSG RGMII Switching Characteristics - RGMII_TD[3:0] and RGMII_TCTL

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
PRRG12	$t_{sk(TD-TXC)}$	TD to TXC output skew	10 Mbps	TBD	TBD	ns
			100 Mbps	TBD	TBD	ns
			1000 Mbps	TBD	TBD	ns
	$t_{sk(TX_CTL-TXC)}$	TX_CTL to TXC output skew	10 Mbps	TBD	TBD	ns
			100 Mbps	TBD	TBD	ns
			1000 Mbps	TBD	TBD	ns

表 5-108. PRU_ICSSG RGMII Switching Characteristics - RGMII_TD[3:0] and RGMII_TCTL (continued)

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
PRRG13	$t_{i(TD)}$	Transition time, TD	10 Mbps		TBD	ns
			100 Mbps		TBD	ns
			1000 Mbps		0.75	ns
	$t_{i(TX_CTL)}$	Transition time, TX_CTL	10 Mbps		TBD	ns
			100 Mbps		TBD	ns
			1000 Mbps		0.75	ns

(1) P = Cycle time

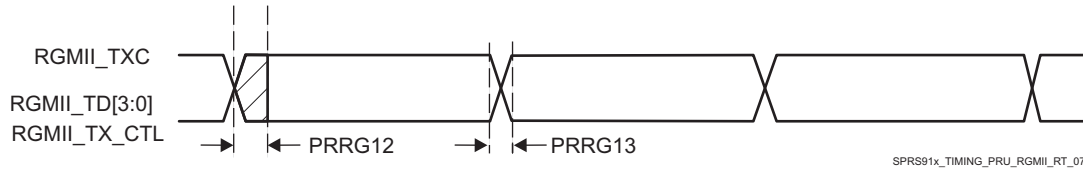


图 5-114. PRU_ICSSG RGMII_RD[3:0] and RGMII_RCTL Output Timing

5.9.5.21.6.3 PRU_ICSSG MII_RT Electrical Data and Timing

注

In order to ensure the MII_G_RT I/O timing values published in the device data sheet, the PRU_ICSSG ICSSGn_CORE_CLK (where n = 0 to 2) core clock must be configured for 200 MHz, 225 MHz, or 250 MHz and the TX_CLK_DELAYn (where n = 0 or 1) bit field in the ICSSG_TXCFG0/1 register must be set to 0h (default value).

表 5-109. PRU_ICSSG MII_RT Timing Requirements – MII_RXCLK

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
PMIR1	$t_{c(RX_CLK)}$	Cycle time, RX_CLK	10 Mbps	399.96	400.04	ns
			100 Mbps	39.996	40.004	ns
PMIR2	$t_{w(RX_CLKH)}$	Pulse Duration, RX_CLK High	10 Mbps	140	260	ns
			100 Mbps	14	26	ns
PMIR3	$t_{w(RX_CLKL)}$	Pulse Duration, RX_CLK Low	10 Mbps	140	260	ns
			100 Mbps	14	26	ns

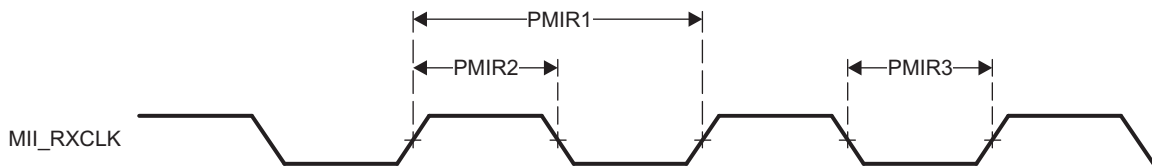


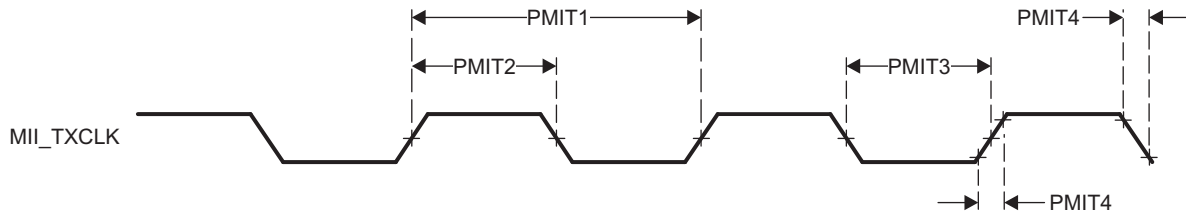
图 5-115. PRU_ICSSG MII_RXCLK Timing

表 5-110. PRU_ICSSG MII_RT Timing Requirements – MII_TXCLK

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
PMIT1	$t_{c(TX_CLK)}$	Cycle time, TX_CLK	10 Mbps	399.96	400.04	ns
			100 Mbps	39.996	40.004	ns

表 5-110. PRU_ICSSG MII_RT Timing Requirements – MII_TXCLK (continued)

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
PMIT2	$t_w(\text{TX_CLKH})$	Pulse Duration, TX_CLK High	10 Mbps	140	260	ns
			100 Mbps	14	26	ns
PMIT3	$t_w(\text{TX_CLKL})$	Pulse Duration, TX_CLK Low	10 Mbps	140	260	ns
			100 Mbps	14	26	ns
PMIT4	$t_t(\text{TX_CLK})$	Transition time, TX_CLK	10 Mbps		5	ns
			100 Mbps		5	ns

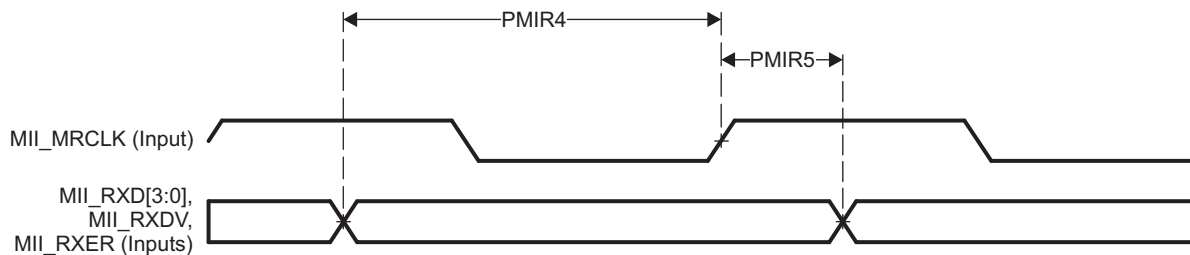


SPRS91x_TIMING_PRU_MII_RT_05

图 5-116. PRU_ICSSG MII_TXCLK Timing

表 5-111. PRU_ICSSG MII_RT Timing Requirements – MII_RXD[3:0], MII_RXDV, and MII_RXER

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
PMIR4	$t_{su}(\text{RXD-RX_CLK})$	Setup time, RXD[3:0] valid before RX_CLK	10 Mbps	8		ns
	$t_{su}(\text{RX_DV-RX_CLK})$	Setup time, RX_DV valid before RX_CLK		8		ns
	$t_{su}(\text{RX_ER-RX_CLK})$	Setup time, RX_ER valid before RX_CLK		8		ns
	$t_{su}(\text{RXD-RX_CLK})$	Setup time, RXD[3:0] valid before RX_CLK	100 Mbps	8		ns
	$t_{su}(\text{RX_DV-RX_CLK})$	Setup time, RX_DV valid before RX_CLK		8		ns
	$t_{su}(\text{RX_ER-RX_CLK})$	Setup time, RX_ER valid before RX_CLK		8		ns
PMIR5	$t_h(\text{RX_CLK-RXD})$	Hold time, RXD[3:0] valid after RX_CLK	10 Mbps	8		ns
	$t_h(\text{RX_CLK-RX_DV})$	Hold time, RX_DV valid after RX_CLK		8		ns
	$t_h(\text{RX_CLK-RX_ER})$	Hold time, RX_ER valid after RX_CLK		8		ns
	$t_h(\text{RX_CLK-RXD})$	Hold time, RXD[3:0] valid after RX_CLK	100 Mbps	8		ns
	$t_h(\text{RX_CLK-RX_DV})$	Hold time, RX_DV valid after RX_CLK		8		ns
	$t_h(\text{RX_CLK-RX_ER})$	Hold time, RX_ER valid after RX_CLK		8		ns

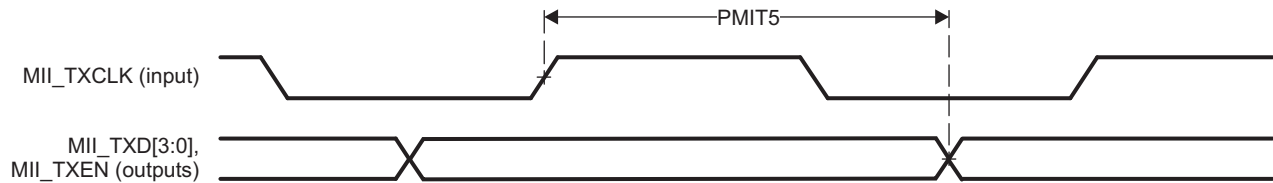


SPRS91x_TIMING_PRU_MII_RT_06

图 5-117. PRU_ICSSG MII_RXD[3:0], MII_RXDV, and MII_RXER Timing

表 5-112. PRU_ICSSG MII_RT Switching Characteristics – MII_TXD[3:0] and MII_TXEN

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
PMIT5	$t_d(\text{TX_CLK-TXD})$	Delay time, TX_CLK High to TXD[3:0] valid	10 Mbps	5	25	ns
	$t_d(\text{TX_CLK-TX_EN})$	Delay time, TX_CLK to TX_EN valid		5	25	ns
	$t_d(\text{TX_CLK-TXD})$	Delay time, TX_CLK High to TXD[3:0] valid	100 Mbps	5	25	ns
	$t_d(\text{TX_CLK-TX_EN})$	Delay time, TX_CLK to TX_EN valid		5	25	ns



SPRS91x_TIMING_PRU_MII_RT_07

图 5-118. PRU_ICSSG MII_TXD[3:0], MII_TXEN Timing

For more information, see section *Programmable Real-Time Unit Subsystem and Industrial Communication Subsystem - Gigabit (PRU_ICSSG)* in the device TRM.

5.9.5.22 Timers

For more details about features and additional description information on the device Timers, see the corresponding sections within [4.3, Signal Descriptions](#) and [6, Detailed Description](#).

[表 5-113](#), [表 5-114](#) and [图 5-119](#) present timings and switching characteristics of the Timers.

表 5-113. Timing Requirements for Timers

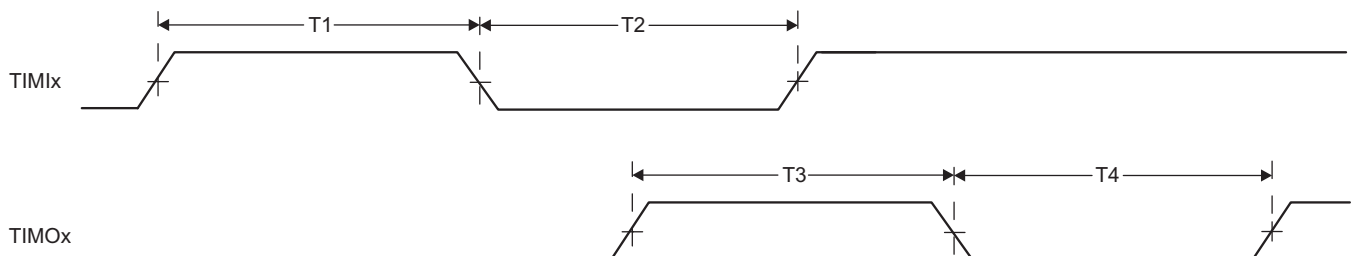
NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
T1	$t_w(\text{TINPH})$	Pulse duration, high	CAPTURE	5 + 4P ⁽¹⁾		ns
T2	$t_w(\text{TINPL})$	Pulse duration, low	CAPTURE	5 + 4P ⁽¹⁾		ns

(1) P = functional clock period in ns.

表 5-114. Switching Characteristics for Timers

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
T3	$t_w(\text{TOUTH})$	Pulse duration, high	PWM	-3 + 4P ⁽¹⁾		ns
T4	$t_w(\text{TOUTL})$	Pulse duration, low	PWM	-3 + 4P ⁽¹⁾		ns

(1) P = functional clock period in ns.



TIMER_01

图 5-119. Timer Timing

For more information, see section *Timers* in the device TRM.

5.9.5.23 UART

For more details about features and additional description information on the device Universal Asynchronous Receiver Transmitter, see the corresponding sections within [4.3, Signal Descriptions](#) and [6, Detailed Description](#).

表 5-115, 表 5-116, and 图 5-120 present Timing Requirements and Switching Characteristics for UART interface.

表 5-115. Timing Requirements for UART

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
4	$t_{w(RX)}$	Pulse width, receive data bit, 15/30 pF high or low		$0.95U^{(1)}$	$1.05U^{(1)}$	ns
5	$t_{w(CTS)}$	Pulse width, receive start bit, 15/30 pF high or low		$0.95U^{(1)}$	$1.05U^{(1)}$	ns
	$t_{d(RTS-TX)}$	Delay time, transmit start bit to transmit data		P ⁽²⁾		ns
	$t_{d(CTS-TX)}$	Delay time, receive start bit to transmit data		P ⁽²⁾		ns

(1) U = UART baud time = 1/Programmed baud rate

(2) P = Clock period of the reference clock (FCLK, usually 48 MHz or 192 MHz)

表 5-116. Switching Characteristics Over Recommended Operating Conditions for UART

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
	$f_{(baud)}$	Maximum programmable baud rate	15 pF		12	MHz
			30 pF		0.115	
2	$t_{w(TX)}$	Pulse width, transmit data bit, 15/30 pF high or low		$U - 2^{(1)}$	$U + 2^{(1)}$	ns
3	$t_{w(RTS)}$	Pulse width, transmit start bit, 15/30 pF high or low		$U - 2^{(1)}$	$U + 2^{(1)}$	ns

(1) U = UART baud time = 1/Programmed baud rate

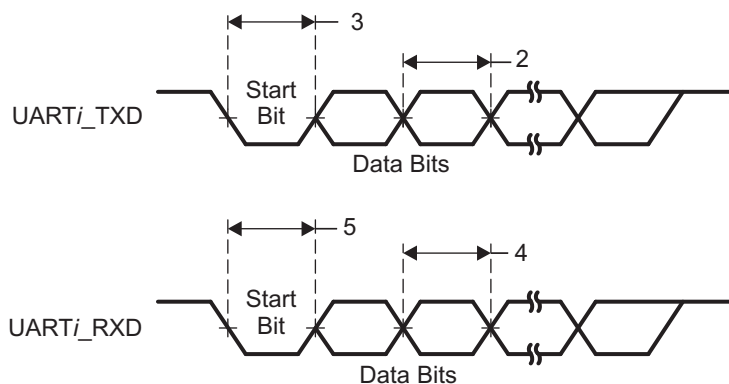


图 5-120. UART Timing

For more information, see section *Universal Asynchronous Receiver/Transmitter (UART)* in the device TRM.

5.9.5.24 USB

The USB 2.0 subsystem is compliant with the Universal Serial Bus (USB) Specification, revision 2.0. Refer to the specification for timing details.

The USB 3.1 GEN1 Dual-Role Device Subsystem is compliant with the Universal Serial Bus (USB) 3.1 Specification, revision 1.0. Refer to the specification for timing details.

For more details about features and additional description information on the device Universal Serial Bus Subsystem (USB), see the corresponding sections within [4.3, Signal Descriptions](#) and [6, Detailed Description](#).

For more information, see section *Universal Serial Bus (USB) Subsystem* in the device TRM.

5.9.6 Emulation and Debug

5.9.6.1 Debug Trace

表 5-117 和 图 5-121 假设测试在推荐的运行条件和电气特性条件下。

表 5-117. Debug Trace Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
DBTR1	$t_c(\text{TRC_CLK})$	Cycle time, TRC_CLK	10.16		ns
DBTR2	$t_w(\text{TRC_CLKH})$	Pulse width, TRC_CLK high	4.33		ns
DBTR3	$t_w(\text{TRC_CLKL})$	Pulse width, TRC_CLK low	4.33		ns
DBTR4	$t_{\text{osu}}(\text{TRC_DATAV-TRC_CLK})$	Output setup time, TRC_DATA valid to TRC_CLK edge	1.27		ns
DBTR5	$t_{\text{oh}}(\text{TRC_CLK-TRC_DATAI})$	Output hold time, TRC_CLK edge to TRC_DATA invalid	1.27		ns
DBTR6	$t_{\text{osu}}(\text{TRC_CTLV-TRC_CLK})$	Output setup time, TRC_CTL valid to TRC_CLK edge	1.27		ns
DBTR7	$t_{\text{oh}}(\text{TRC_CLK-TRC_CTLI})$	Output hold time, TRC_CLK edge to TRC_CTL invalid	1.27		ns
DBTR8	$t_{\text{rx}}(\text{TRC_CLK_DATA_CTL})$	Output rise time, 30% VDD to 70% VDD		0.75	ns
DBTR9	$t_{\text{fx}}(\text{TRC_CLK_DATA_CTL})$	Output fall time, 70% VDD to 30% VDD		0.75	ns

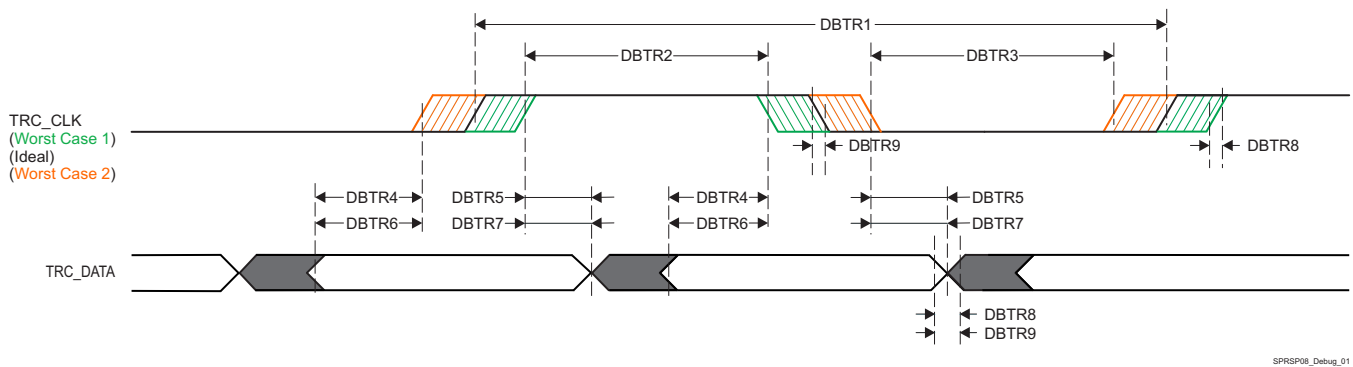


图 5-121. Debug Trace Timing

5.9.6.2 IEEE 1149.1 Standard-Test-Access Port (JTAG)

For more details about features and additional description information on the device IEEE 1149.1 Standard-Test-Access Port, see the corresponding sections within 4.3, *Signal Descriptions* and 6, *Detailed Description*.

5.9.6.2.1 JTAG Electrical Data and Timing

表 5-118, 表 5-119, 和 图 5-122 假设测试在推荐的运行条件和电气特性条件下。

表 5-118. Timing Requirements for IEEE 1149.1 JTAG

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
J1	$t_c(\text{TCK})$	Cycle time minimum, TCK	75		ns
J2	$t_w(\text{TCKH})$	Pulse width minimum, TCK high	30		ns
J3	$t_w(\text{TCKL})$	Pulse width minimum, TCK low	30		ns
J4	$t_{\text{su}}(\text{TDI-TCK})$	Input setup time minimum, TDI valid to TCK high	8		ns
	$t_{\text{su}}(\text{TMS-TCK})$	Input setup time minimum, TMS valid to TCK high	8		ns

表 5-118. Timing Requirements for IEEE 1149.1 JTAG (continued)

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
J5	$t_h(\text{TCK-TDI})$	Input hold time minimum, TDI valid from TCK high	5.2		ns
	$t_h(\text{TCK-TMS})$	Input hold time minimum, TMS valid from TCK high	5.2		ns

表 5-119. Switching Characteristics Over Recommended Operating Conditions for IEEE 1149.1 JTAG

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
J6	$t_d(\text{TCKL-TDOI})$	Delay time minimum, TCK low to TDO invalid	0		ns
J7	$t_d(\text{TCKL-TDOV})$	Delay time maximum, TCK low to TDO valid		27.75	ns

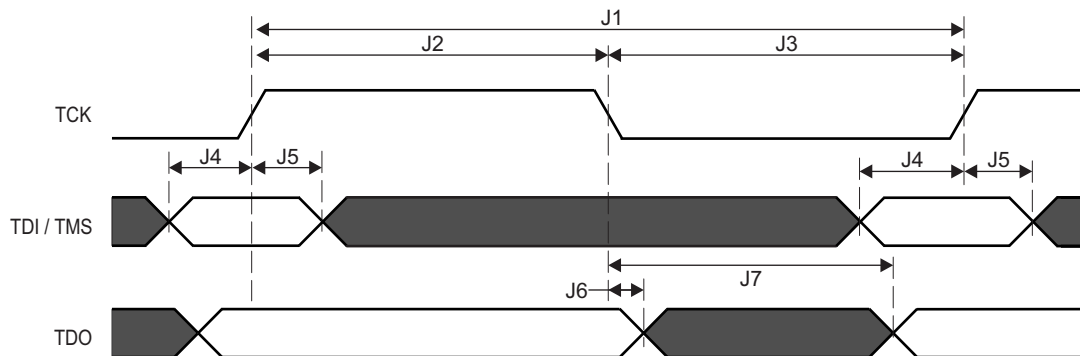


图 5-122. JTAG Test-Port Timing

6 Detailed Description

6.1 Overview

AM654x and AM652x Sitara™ processors are Arm applications processors built to meet the complex processing needs of modern industry 4.0 embedded products.

The AM654x and AM652x devices combine four or two Arm Cortex-A53 cores with a dual Cortex-R5F MCU subsystem which includes features intended to help customers achieve their functional safety goals for their end products and three Gigabit industrial communications subsystems (PRU_ICSSG) to create a SoC capable of high-performance industrial controls with industrial connectivity and processing for functional safety applications. AM65xx is currently undergoing assessment to be certified by TÜV SÜD according to IEC 61508.

The four A53 cores are arranged in two dual-core clusters with shared L2 memory to create two processing channels. Extensive ECC is included on on-chip memory, peripherals, and interconnect for reliability. The SoC as a whole includes features intended to help customers design systems that can achieve their functional safety goals (assessment pending with TÜV SÜD). Cryptographic acceleration and secure boot are available on AM654x and AM652x devices in addition to granular firewalls managed by the DMSC.

Programmability is provided by the quad-core Arm Cortex-A53 RISC CPUs with Neon extension, and the dual Cortex-R5F MCU subsystem is available for general purpose use as two cores or it can be used in lockstep to help meet the needs of functional safety applications. The PRU_ICSSG subsystems can be used to provide up to six ports of industrial Ethernet such as Profinet IRT, TSN, or EtherCAT® (among many others), or they can be used for standard Gigabit Ethernet connectivity.

TI provides a complete set of software and development tools for the Arm cores including Processor SDK Linux, Linux-RT, RTOS, and Android as well as C compilers and a debugging interface for visibility into source code execution. Applicable safety documentation will be made available to assist customers in developing their functional safety related systems.

注

For more information on features, subsystems, and architecture of superset device System on Chip (SoC), see the device TRM.

6.2 Processor Subsystems

6.2.1 Arm Cortex-A53

The SoC implements two Dual-Core Arm Cortex-A53 Subsystems (CC_ARMSS0 and CC_ARMSS1), which are both integrated inside the Compute Cluster (along with the MSMC module). The Cortex-A53 cores are general-purpose processors that can be used for running customer applications.

注

Notes on references used in this document:

- Both Arm Cortex-A53 Subsystems are functionally identical and are referred to as a single subsystem (CC_ARMSS), where appropriate.
- CC_ARMSS is also referred to as Arm CorePac and A53SS.
- Cortex-A53 is often shortened to A53.

The CC_ARMSS is built around the Cortex-A53 MPCore (Arm A53 Cluster), which is provided by Arm and configured by TI. It is based on the symmetric multiprocessor (SMP) architecture, and thus it delivers high performance and optimal power management, debug and emulation capabilities.

The A53 processor is a multi-issue out-of-order superscalar execution engine with integrated L1 Instruction and Data Caches, compatible with Arm®v8-A architecture. It delivers significantly more performance than its predecessors at a higher level of power efficiency.

The Armv8-A architecture brings a number of new features. These include 64-bit data processing, extended virtual addressing and 64-bit general purpose registers. The A53 processor is Arm's first Armv8-A processor aimed at providing power-efficient 64-bit processing. It features an in-order, 8-stage, dual-issue pipeline, and improved integer, Arm® Neon™, Floating-Point Unit (FPU) and memory performance.

The A53 CPU supports two execution states: AArch32 and AArch64. The AArch64 state gives the A53 CPU its ability to execute 64-bit applications, while the AArch32 state allows the processor to execute existing Arm®v7-A applications.

Details on the Compute Cluster module and the interaction between CC_ARMSS(s) and MSMC can be found in the *Compute Cluster* chapter.

The CC_ARMSS supports the following key features:

- Cortex-A53 MPCore (A53 Cluster) features:
 - Dual-core configuration (coherent SMP processors within the cluster)
 - A53 core revision: r0p4
 - Full compliance to Armv8-A architecture
 - AArch32 and AArch64 Execution States
 - AArch32 for full backward compatibility with Armv7
 - AArch64 for 64b support and new architectural features
 - All exception levels EL0-3
 - A32 Instruction Set
 - T32 Instruction Set
 - A64 Instruction Set
 - Neon Advanced SIMD
 - VFPv4 Floating point
 - Hardware virtualization support
 - Armv8 Cryptography Extensions
 - Arm GICv3 architecture
 - In-order pipeline with symmetric dual-issue of most instructions
 - Harvard L1 with system MMU
 - 32KB Instruction (Program) Cache
 - 32KB Data Cache
 - 512KB Shared L2 Cache
 - Snoop Control Unit (SCU) managing the interconnect, arbitration, communication, cache-to-cache and system memory transfers, cache coherence and other capabilities for the processor
 - Generic Timer(s)
 - Arm® CoreSight™ Debug and Trace Architecture
 - Functional safety support
 - Error Correction Code (ECC) protection for:
 - L1 Data Cache (Data RAM)
 - L2 Cache (Data RAM, Tag RAM)
 - L1 SCU Duplicate Tags
 - Parity protection for:
 - L1 Instruction Cache (Data RAM and Tag RAM)
 - L1 Data Cache Tag RAM and Dirty Bits
 - TLB
 - No error protection on branch protection and L2 victim RAM
 - Support for error injection to all supported ECC memory blocks
 - Provided for testing ECC functionality in safety-critical applications (add-on function from TI)
 - Supported by ECC Aggregators at the CC_ARMSS level
- 256-bit wide, synchronous or asynchronous VBUSM.C master interface
 - AXI2VBUSM_MASTER Bridge
 - Sync/Async boot time selectable via pin
 - Cache pre-warming via use of ACP Port
- 64-bit graycoded system input time
- 48-bit graycoded debug input time
- 32-bit VBUSP slave interface for debug (internally converted to APB)
- 32-bit ATB output port for debug/trace
- Interface with Arm GIC-500 Interrupt Controller (SoC level, not part of CC_ARMSS)

- Supports the SoC multi-core cache coherency architecture
- Dedicated MPU clocking (Arm PLLs) for full flexibility in performance trade-offs
- Advanced power management with fine-grained control of individual A53 CPU power domains, coarse-grained cluster-level power management, and low-power standby modes (WFI/WFE modes)
- Dedicated RTI windowed watchdog timer per core
- Support for Little-Endian (LE) at core level

For more information, see section *Compute Cluster Arm Cortex-A53 Subsystem* in the device TRM.

6.2.2 Arm Cortex-R5F

The MCU_ARMSS is a dual-core implementation of the Arm Cortex-R5F processor configured for split/lock operation. It also includes accompanying memories (L1 caches and tightly-coupled memories), standard Arm® CoreSight™ debug and trace architecture, integrated Vectored Interrupt Manager (VIM), ECC Aggregators, and various other modules for protocol conversion and address translation for easy integration into the SoC.

注

The Cortex-R5F processor is a Cortex-R5 processor that includes the optional Floating Point Unit (FPU) extension.

The MCU_ARMSS supports the following features:

- Dual Arm Cortex-R5F CPU configuration
 - Core revision: r1p3
 - Arm®v7-R profile
 - Split/Lock operation
 - Split mode: Two independently operating cores (Asymmetric Multi Processing, no coherence)
 - Lock (lockstep) mode: One main operating core with the other operating in lockstep for safety
 - Boot-time configurable to be in split or lock mode
 - L1 Memory System
 - 16KB Instruction Cache
 - 4x4KB ways
 - SECDED ECC protected per 64 bits
 - 16KB Data Cache
 - 4x4KB ways
 - SECDED ECC protected per 32 bits
 - 64KB Tightly-Coupled Memory (TCM) per CPU
 - SECDED ECC protected per 32 bits
 - Readable/Writable from system
 - Split into A and B banks (with B further splitting into B0 and B1 interleaved banks)
 - 32KB TCMA (ATCM)
 - 16KB TCMB0 (B0TCM)
 - 16KB TCMB1 (B1TCM)
 - Low interrupt latency with restartable instructions
 - Non-Maskable Interrupt (NMI)
 - Full-precision Floating Point (VFPv3)
 - 16-region Memory Protection Unit (MPU)
 - 8 breakpoints
 - 8 watchpoints
 - Dynamic branch prediction with global history buffer and 4-entry return stack
 - CoreSight Debug Access Port (DAP)
 - CoreSight ETM-R5 interface
 - Performance Monitoring Unit (PMU)
- Interfaces
 - 64-bit VBUSM master pair (1 read, 1 write) for L3 memory accesses (per core)
 - 64-bit VBUSM slave for TCM access (per core)
 - Also allows access to cache for debug purposes
 - 32-bit VBUSP master for peripheral access (per core)
 - 32-bit VBUSP slave configuration port (per core)
 - 32-bit VBUSP slave debug port
 - Allows access to all MCU_ARMSS internal debug logic
- Synchronous clock domain crossing on all interfaces
- 32-bit to 48-bit Region-based Address Translation (RAT) on memory access masters
 - 16 regions

- Integrated Vectored Interrupt Manager (VIM)
 - 512 interrupts per core
 - Only interrupts connected to R5F Core 0 are available in lock mode
 - Each interrupt programmable as either IRQ or FIQ
 - Each interrupt has a programmable enable mask
 - Each interrupt has a programmable 4-bit priority
 - Priority interrupt supported
 - Vectored Interrupt Interface
 - Compatible with R5F VIC port
 - Programmable 32-bit vector address per interrupt
 - Address is SECDED error protected
 - Default vector addresses provided on DED
 - Software interrupt generation
- Standard Arm CoreSight debug and trace architecture at the MCU_ARMSS level
 - Cross Triggering: Supported by Cross Trigger Interface (CTI) (per CPU) and Cross Trigger Matrix (CTM) components
 - Processor Trace: Supported by Embedded Trace Macrocell (ETM) (per CPU) and Advanced Trace Bus (ATB) Funnel components
- Integrated ECC Aggregators
 - Support for error injection to all supported ECC memory blocks to test ECC functionality in safety-critical applications (add-on function from TI)
 - One ECC Aggregator per core to cover all RAMs associated with that core
- Boot
 - From ROM or external memory
 - From TCM

The MCU_ARMSS does *not* support the following features in this device:

- ACP port (no coherence)
- AXI peripheral port (PPX/PPV); corresponds to the VBUSM peripheral port at the MCU_ARMSS level
- Bus parity/ECC

For more information, see section *MCU Arm Cortex-R5F Subsystem* in the device TRM.

6.3 Accelerators and Coprocessors

6.3.1 PRU_ICSSG

The Programmable Real-Time Unit Subsystem and Industrial Communication Subsystem (PRU_ICSSG) consists of:

- Two 32-bit load/store RISC CPU cores — Programmable Real-Time Units (PRU0 and PRU1)
- Two auxiliary 32-bit load/store RISC CPU cores — Auxiliary Programmable Real-Time Units (RTU_PRU0 and RTU_PRU1)
- Data RAMs per PRU core
- Instruction RAMs per PRU and per RTU_PRU cores
- Shared RAM
- Peripheral modules: UART0, ECAP0, PWM, IEP0 and IEP1
- Interrupt controller (INTC)

The programmable nature of the PRU cores, along with their access to pins, events and all device resources, provides flexibility in implementing fast real-time responses, specialized data handling operations, custom peripheral interfaces, and in offloading tasks from the other processor cores of the device.

The PRU cores are programmed with a small, deterministic instruction set. Each PRU can operate independently or in coordination with each other and can also work in coordination with the device-level host CPU. This interaction between processors is determined by the nature of the firmware loaded into the PRU's instruction memory.

The device has integrated three identical PRU_ICSSG subsystems (PRU_ICSSG0, PRU_ICSSG1 and PRU_ICSSG2).

The PRU_ICSSG subsystem includes the following main features:

- Asynchronous capture [Serial Capture Unit (SCU)] with EnDat[®] 2.2 protocol and Sigma-Delta demodulation support
- Two 32-bit load/store RISC CPU cores — Programmable Real-Time Units (PRU0 and PRU1), each with:
 - 20 Enhanced General-Purpose Inputs (EGPI) and 20 Enhanced General-Purpose Outputs (EGPO)
 - 12KB program memory per PRU (PRU0_IRAM and PRU1_IRAM) with ECC
 - 4KB Broadside (BS) RAM
 - MAC (Multiplier with optional Accumulation)
 - CRC16/CRC32 HW accelerator
 - Byte Swap, for Little/Big Endian conversion
 - SUM32 Hardware accelerator for UDP checksum
 - Task Manager
 - Support of 128-bit wide PSI-L TX port for streaming access to NAVSS0
 - Broadside (32-bit) connection to MII_G_RTn (where n= 1 or 2), Filter Data Base (FDB), Scratchpad Memory (SPAD), SPINLOCK, XFR2VBUS, and RTU_PRUm (where m= 0 or 1)

- Two auxiliary Real-Time Transfer Units (RTU_PRU0 and RTU_PRU1), each with:
 - 8KB program memory with ECC
 - 16KB Broadside (BS) RAM
 - MAC (Multiplier with optional Accumulation)
 - CRC16/CRC32 HW accelerator
 - Byte Swap, for Little/Big Endian conversion
 - Two instances of SUM32 Hardware accelerator
 - Task Manager
 - XFR2TR, for accelerating the internal memory copy of worklist from TRs (Transfer Requests)
 - Supports 128-bit wide PSI-L RX/TX port for streaming access through NAVSS0
- Scratchpad Memory (SPAD) with 4 banks of 30 x 32-bit registers
- 64KB Shared general purpose memory RAM with ECC (Data RAM2), shared between PRU0 and PRU1
- Two 8KB Data Memories with ECC (Data RAM0 and Data RAM1)
- Two 256-bit VBUSM Master Ports:
 - Separate port for each PRUn/RTU_PRUn (where n = 0 or 1)
 - Optional address translation for PRUn (where n = 0 or 1) transactions to External Host
- 16 Software Events generated by 2 PRUs
- Two Real-Time Ethernet ports (MII_G_RT1 and MII_G_RT2) configurable to connect to each PRUn (where n = 0 or 1) to support multiple industrial communication protocols.
 - Each of the Ethernet ports can be configured as MII/RGMII/SGMII ports
 - **NOTE: SGMII mode is supported only for PRU_ICSSG2 instance**
- Two Industrial Ethernet Peripheral's (IEP0/IEP1) to manage/generate Industrial Ethernet functions such as time stamping.
 - Each of the Industrial Ethernet 64-bit timers support 10 capture and 16 compare events along with slow and fast compensation.
 - Supports up to 4 sets of 3 phased motor control with 12 primary and 12 complimentary programmable PWM outputs.
 - Up to 9 safety events with optional external trip IO per PWM set with hardware glitch filter.
- One MDIO port to control external Ethernet PHY
- One Enhanced Capture Module (ECAPO)
- 16550-compatible UART with a dedicated 192MHz clock to support 12-Mbps PROFIBUS
- Interrupt Controller (INTC)
 - Up to 64 internal events, generated by modules, internal to the PRU_ICSSG
 - Up to 96 external events, generated by the system
 - Supports up to 20 interrupt channels
 - Generation of 20 Host interrupts:
 - 2 Host interrupts to PRU0 and PRU1
 - 2 Host interrupts to RTU_PRU0 and RTU_PRU1
 - 8 Host interrupts, exported from the PRU_ICSSG for signaling the Arm interrupt controllers (pulse and level provided)
 - 8 Host Interrupts for the Task Managers
 - Each system event can be enabled and disabled
 - Each host event can be enabled and disabled
 - Hardware prioritization of events
- One 32-bit VBUSP slave (target) port for memory mapped register and internal memories access
- Flexible power management support
- Integrated 32-bit Interconnect

The following PRU_ICSSG features are not supported:

- Only 4 of the IEP0 (and none of the IEP1) Ethernet Digital Data Input/Output's of each PRU_ICSSG are pinned out
- UART Modem interface is not supported
- **The following features are not supported only for PRU_ICSSG0 and PRU_ICSSG1:**
 - 12 Enhanced General-Purpose Inputs (pr<0/1>_pru0_r31_in[31:20]) are not pinned out
 - 12 Enhanced General-Purpose Outputs (pr<0/1>_pru0_r31_out[31:20]) are not pinned out
 - SGMII mode is not supported on PRU_ICSSG0 and PRU_ICSSG1
- **The following features are not supported only for PRU_ICSSG2:**
 - 14 Enhanced General-Purpose Inputs (pr<2>_pru0_r31_in[31:18]) are not pinned out
 - 14 Enhanced General-Purpose Outputs (pr<2>_pru0_r31_out[31:18]) are not pinned out

For more information, see section *Programmable Real-Time Unit Subsystem and Industrial Communication Subsystem - Gigabit (PRU_ICSSG)* in the device TRM.

6.3.2 GPU

The graphics processing unit (GPU) accelerates 2-dimensional (2D) and 3-dimensional (3D) graphics and compute applications.

The GPU module is a scalable architecture which efficiently processes a number of differing multimedia data types concurrently:

- Pixel Data
- Vertex Data
- General Purpose Processing

The GPU subsystem supports the following features:

- Single-core GPU architecture is consists of:
 - 1 × SGX544-MP1 core
 - Shared system level cache of 64 KB
- Tile-based deferred rendering architecture:
 - Reduces external bandwidth to SDRAM
 - 32×32 pixels tile size
- Universal Scalable Shader Engine (USSE™):
 - Multithreaded engine incorporating vertex and pixel shader functionality
 - Automatic load balancing of vertex and pixel processing tasks
- Present and texture load accelerator (PTLA):
 - Enables to move, rotate, twiddle, and scale texture surfaces
 - Supports RGB, ARGB, YUV4:2:2, and YUV4:2:0 surface formats
 - Supports bilinear upscale, boxcar filter downscale
 - Supports source colorkey
- Fully virtualized memory addressing for operating system (OS) operation in a unified memory architecture:
 - Memory management unit (MMU)
 - Up to 4 GB virtual address space natively supported by graphics core:
 - Address extension to 48-bit provided by RAT function

Graphics Feature Overview:

- Texture support:
 - Cube map
 - Projected textures
 - Non-square textures
- Texture formats:
 - RGBA 8888, 565, 1555, and 1565
 - Monochromatic 8, 16, 16f, 32f, and 32int
 - Dual channel, 8:8, 16:16, and 16f:16f
 - Compressed textures:
 - PVRTC-i 2 bpp
 - PVRTC-i 4 bpp
 - PVRTC-ii 2 bpp
 - PVRTC-ii 4 bpp
 - ETC1
 - DXT 1-5 and BC 4-5
 - Programmable support for YUV formats:
 - Programmable matrix in hardware, coefficients on 12 bits
 - YUV4:2:2, YUV4:2:0, two planes (NV12 or NV21); YUV4:2:0, three planes
- Resolution support:
 - Frame buffer maximum = 4096×4096
 - Texture maximum size = 4096×4096
- Texture filtering:
 - Bilinear, Trilinear, Anisotropic
 - Independent minification and magnification control
- Antialiasing:
 - $4 \times$ multisampling
 - Programmable sample positions

注

TI provides the DXT1-5 and BC4-5 texture compression technology for use only with a Microsoft Windows operating system. A separate license is required for the use of this technology (also referred to as S3 texture compression technology) with any other operating system.

For more information, see section *Graphics Accelerator (GPU)* in the device TRM.

6.4 Other Subsystems

6.4.1 DMSC

Integrated in WKUP domain Device Management and Security Controller (WKUP_DMSC) provides control over the device boot sequencing, device management, power management, and security. With the factory-sealed firmware, DMSC main functions include:

- Device management
- On-chip power management and wake-up control
- Device boot configuration and sequence
- Secure boot setup
- Authentication routines (all modes), including R5F island only boot modes
- Decryption routines
- Firewall control for isolation and Security
- Runtime Security Management and resource allocation
- Arm Cortex-M3 based DMSC acts as system security master and protects critical security assets during run-time. As part of booting on High Security (HS) device, DMSC uses on-chip keys to establish root-of-trust and authenticate images to reinforce trust. DMSC controls the power management of device, hence is responsible to bring device cleanly out of reset and enforce clock and reset rules. DMSC power management functions are critical to bring device to low power modes and sense wakeup events to bring device back to active state. DMSC acts also as main boot processor and as such is the very first subsystem that is brought out of reset after device power-on-reset.

Main components of the DMSC are:

- Arm Cortex-M3 processor core
- 160 KB ROM to allow boot sequence, authentication and provide security service (M3 accessible only)
- Two separate local memory banks for Instruction code (I-code) and Data space (D-code) with single error correction and double error detection
- Firewall enabled 32-bit VBUSP CBASS interconnect
- Interrupt Aggregator with support of up to 80 interrupt inputs to the DMSC
- Four 32-bit Timers
- One RTI/WWDT module capable of issuing warm reset to the SoC
- DMSC control module - contains various control, configuration and status MMRs for power management functions
- Debug and trace related modules
- Security Manager module for device security management, device type control (GP, EMU, HS), emulation control, and key management
- AES engine with 128, 192 and 256-bits support

For more information, see section *WKUP Device Management and Security Controller (DMSC)* in the device TRM.

6.4.2 MSMC

The Multicore Shared Memory Controller (MSMC) forms the heart of the compute cluster (COMPUTE_CLUSTER0) providing high-bandwidth resource access both to and from all of the connected processing elements and the rest of the system. MSMC serves as the data-movement backbone of the compute cluster.

MSMC supports the following features:

- 2MB (2 banks x 1MB) SRAM with ECC:
 - Shared coherent level 2/level 3 memory-mapped SRAM
 - Shared coherent level 3 cache

- 256-bit processor port bus and 40-bit physical address bus
- Coherent unified bi-directional interfaces to connect to processors or device masters
- One infrastructure master interface
- Single external memory master interface
- Supports distributed virtual system
- Supports internal DMA engine – DRU (Data Routing Unit)
 - DMA in/out L2 SRAM, MSMC, DDR and system
 - L2, L3 cache pre-warming and post flushing
- Bandwidth management with starvation bound
- Two-level QoS support for real-time/nonreal-time split
- Security firewall flush support for SRAM/cache and external memory
- Functional safety:
 - SEC/DED protection on all data and tag memories with hardware scrubbing
 - SEC/DED protection on all data pipelines
 - Data memory address hamming protection
 - Coherent interconnect transaction metadata parity protection
- One interconnect messaging interface that supports DMA/prefetch requests to DRU
- Trace and debugging support
- Supports dynamic power up and power down on PDs low power modes, if required by system applications
- Supports dynamic clock gating on all logic units
- Supports low power mode during low-usage processor states

MSMC does not support the following:

- RAM address decode protection
- Direct cache resize changes from one non-zero cache size configuration to another non-zero cache size configuration. In this case software is required to manually transition down to zero cache size configuration first, followed by a second transition from zero cache size configuration to the new non-zero cache size configuration.
- MSMC SRAM or SDRAM traffic during an MSMC cache resize transition. The traffic during this transition has undefined behavior.

For more information, see section *Multicore Shared Memory Controller (MSMC)* in the device TRM.

6.4.3 NAVSS

6.4.3.1 NAVSS0

Main SoC Navigator Subsystem (NAVSS0) consists of DMA/Queue Management components – UDMA and Ring Accelerator (UDMASS), Peripherals (Module subsystem [MODSS]), and a North Bridge (NBSS).

UDMASS – UDMASS is the essential part of the DMA Architecture. UDMASS consists of:

- Unified DMA Controller
- Ring Accelerator
- Packet Streaming Interface (PSI-L)

MODSS – MODSS is a collection of peripherals with different system-level functions, for example, interprocessor communication and time sync, among others. NAVSS0 contains the following modules:

- Mailbox
- Spinlock
- Two Timer Managers (Timer banks)
- Time Stamp Module (CPTS)

- Memory CRC module
- Infrastructure components such as:
 - CBASS
 - Proxies
 - Interrupt aggregators
 - Interrupt router

NBSS – This is a north bridge infrastructure

6.4.3.2 MCU_NAVSS

MCU Navigator Subsystem (MCU NAVSS) has a subset of the modules of the main NAVSS and is instantiated in the MCU domain.

MCU Navigator Subsystem consists of DMA/Queue Management components – UDMA and Ring Accelerator (UDMASS), and Peripherals (Module subsystem [MODSS]).

UDMASS – UDMASS is the essential part of the DMA Architecture. UDMASS consists of:

- Unified DMA Controller
- Ring Accelerator
- Packet Streaming Interface (PSILSS)

MODSS – MODSS is a collection of peripherals with different system-level functions. NAVSS0 contains the following modules:

- Memory CRC module
- Infrastructure components such as CBASS, proxies, interrupt aggregators, and an interrupt router

ECC aggregators – for SEC/DED memory protection.

For more information, see sections *Main Navigator Subsystem (NAVSS)* and *MCU Navigator Subsystem (MCU NAVSS)* in the device TRM.

6.4.4 PDMA Controller

The Peripheral DMA is a simple DMA which has been architected to specifically meet the data transfer needs of peripherals, which perform data transfers using memory mapped registers (MMRs) accessed via a standard non-coherent bus fabric. The PDMA module is located close to one or more peripherals which require an external DMA for data movement and is architected to reduce cost by using VBUSP interfaces and supporting only statically configured Transfer Request (TR) operations.

The PDMA is only responsible for performing the data movement transactions which interact with the peripherals themselves. Data which is read from a given peripheral is packed by a PDMA source channel into a PSI-L data stream which is then sent to a remote peer UDMA-P destination channel which then performs the movement of the data into memory. Likewise, a remote UDMA-P source channel fetches data from memory and transfers it to a peer PDMA destination channel over PSI-L which then performs the writes to the peripheral.

The PDMA architecture is intentionally heterogeneous (UDMA-P + PDMA) to right size the data transfer complexity at each point in the system to match the requirements of whatever is being transferred to or from. Peripherals are typically FIFO based and do not require multi-dimensional transfers beyond their FIFO dimensioning requirements, so the PDMA transfer engines are kept simple with only a few dimensions (typically for sample size and FIFO depth), hardcoded address maps, and simple triggering capabilities.

Multiple source and destination channels are provided within the PDMA which allow multiple simultaneous transfer operations to be ongoing. The DMA controller maintains state information for each of the channels and employs round-robin scheduling between channels in order to share the underlying DMA hardware.

There are five PDMA modules in the device.

6.4.4.1 PDMA Features

6.4.4.1.1 MCU_PDMA0 Features

The MCU domain PDMA0 supports the following features:

- Implements CPPI 5.0 compliant third-party Unified Transfer Controller (UTC)
- Provides 0 memory write access units
- Provides 1 memory read access unit (Read Unit 0):
 - Provides a 32-bit wide VBUSP read-only master interface for peripheral accesses
 - Supports 1 outstanding read
- Supports up to 4 simultaneous source (Rx) channels
- Supports static Transfer Requests (TRs) only
- Provides per-channel buffering:
 - Provides 8x128-bit word deep data FIFO for each source channel
 - Provides 128-bit wide PSI-L compliant data interface to remote UDMA-P and remote peripherals

6.4.4.1.2 MCU_PDMA1 Features

The MCU domain PDMA1 supports the following features:

- Implements CPPI 5.0 compliant third-party Unified Transfer Controller (UTC)
- Provides 1 memory write access unit (Write Unit 0):
 - Provides a 32-bit wide VBUSP write-only master interface for peripheral accesses.
 - Supports 1 outstanding write
- Provides 1 memory read access unit
 - Provides a 32-bit wide VBUSP read-only master interface for peripheral accesses
 - Supports 1 outstanding read
- Supports up to 19 simultaneous destination (Tx) channels
- Supports up to 19 simultaneous source (Rx) channels
- Supports static Transfer Requests (TRs) only
- Supports MCAN special transfer mode
- Provides per-channel buffering:
 - Provides 8x128-bit word deep data FIFO for each destination channel
 - Provides 8x128-bit word deep data FIFO for each source channel
 - Provides 128-bit wide PSI-L compliant data interface to remote UDMA-P and remote peripherals
 - Provides 128-bit wide PSI-L compliant data interface from remote UDMA-P and remote peripherals

6.4.4.1.3 PDMA0 Features

The MAIN domain PDMA0 supports the following features:

- Implements CPPI 5.0 compliant third-party Unified Transfer Controller (UTC)
- Provides 1 memory write access unit (Write Unit 0):
 - Provides a 32-bit wide VBUSP write-only master interface for peripheral accesses
 - Supports 1 outstanding write
- Provides 1 memory read access unit (Read Unit 0):
 - Provides a 32-bit wide VBUSP read-only master interface for peripheral accesses
 - Supports 1 outstanding read
- Supports up to 3 simultaneous destination (Tx) channels
- Supports up to 3 simultaneous source (Rx) channels
- Supports static Transfer Requests (TRs) only

- Provides per-channel buffering:
 - Provides 8x128-bit word deep data FIFO for each destination channel
 - Provides 8x128-bit word deep data FIFO for each source channel
 - Provides 128-bit wide PSI-L compliant data interface to remote UDMA-P and remote peripherals
 - Provides 128-bit wide PSI-L compliant data interface from remote UDMA-P and remote peripherals

6.4.4.1.4 PDMA1 Features

The MAIN domain PDMA1 supports the following features:

- Implements CPPI 5.0 compliant third-party Unified Transfer Controller (UTC)
- Provides 1 memory write access unit (Write Unit 0):
 - Provides a 32-bit wide VBUSP write-only master interface for peripheral accesses
 - Supports 1 outstanding write
- Provides 1 memory read access unit (Read Unit 0):
 - Provides a 32-bit wide VBUSP read-only master interface for peripheral accesses
 - Supports 1 outstanding read
- Supports up to 23 simultaneous destination (Tx) channels
- Supports up to 23 simultaneous source (Rx) channels
- Supports static Transfer Requests (TRs) only
- Provides per-channel buffering:
 - Provides 8x128-bit word deep data FIFO for each destination channel
 - Provides 8x128-bit word deep data FIFO for each source channel
 - Provides 128-bit wide PSI-L compliant data interface to remote UDMA-P and remote peripherals
 - Includes 1 output event transport lane
 - Provides 128-bit wide PSI-L compliant data interface from remote UDMA-P and remote peripherals
- Includes support for converting 16 local events to global events with corresponding mapping registers

6.4.4.1.5 PDMA_DEBUG Features

The Debug PDMA supports the following features:

- Implements CPPI 5.0 compliant third-party Unified Transfer Controller (UTC)
- Provides 0 memory write access units
- Provides 1 memory read access unit (Read Unit 0):
 - Provides a 64-bit wide VBUSP read-only master interface for peripheral accesses
 - Supports 1 outstanding read
- Supports up to 3 simultaneous source (Rx) channels
- Supports static Transfer Requests (TRs) only
- Provides per-channel buffering:
 - Provides 8x128-bit word deep data FIFO for each source channel
 - Provides 128-bit wide PSI-L compliant data interface to remote UDMA-P and remote peripherals

For more information, see section *PDMA Controller* in the device TRM.

6.4.5 Peripherals

6.4.5.1 ADC

The Analog-to-Digital Converter (ADC) module contains a single 12-bit ADC which can be multiplexed to any 1 of 8 analog inputs (channels).

There are total of two ADC modules in the device.

Each ADC module has the following features:

- 4 MSPS rate with a 60 MHz SMPL_CLK
- Functional Safety Debug Mode
- Single-ended or differential input options
- Programmable Finite State Machine (FSM) sequencer that supports the following:
 - Software initiated start of conversion
 - Optional hardware start of conversion (SOC), synchronized to external hardware event
 - Single conversion (one-shot mode)
 - Continuous conversions (continuous mode)
 - Sequence through all enabled steps based on a mask
 - Programmable open delay before executing each step
 - Programmable sampling delay for each step
 - Programmable averaging (16, 8, 4, 2, or 1) of input samples for each step
 - Store data in either of two FIFOs – 256-word × 16-bit
 - Option to encode input (channel) number with data
 - Support for servicing FIFOs via DMA or processor
 - Programmable DMA request event (for each FIFO)
- Support for the following interrupts and status, with masking:
 - Interrupt if AFE fails to return end of conversion (EOC)
 - Interrupt after a sequence of conversions (all non-masked steps)
 - Interrupt for FIFO threshold levels
 - Interrupt if sampled data is out of a programmable range
 - Interrupt for FIFO overflow and underflow conditions
 - Status bit to indicate if ADC is busy converting

ADC Not Supported Features:

- No packing of 16-bit FIFO data onto 32-bit DMA bus
- Big endian
- Support only 32-bit aligned read/write accesses on the MCU_CBASS0/DMA ports

For more information, see section *Analog-to-Digital Converter (ADC)* in the device TRM.

6.4.5.2 CAL

CALSS0 is a very flexible subsystem that enables connection to multiple cameras supporting MIPI CSI-2 over D-PHY serial interface, a LVDS serial interface, and a traditional parallel interface. It also includes an internal write DMA engine connected to VBUSM interface.

The device includes one instantiation of CAL Subsystem named CALSS0, with a single companion CAMERARX0 instance.

The device CALSS provides the following main features:

- Up to 250 MHz processing clock rate
- Interfaces:
 - One PHY Protocol Interfaces (PPI) to shared companion MIPI D-PHY compliant receiver (CAMERARX)
 - Serial Configuration Interface (SCP) to CAMERARX
 - 32-bit slave configuration interface (OCPC) to the system interconnect
 - 128-bit master data interface (OCPO) to the system interconnect and memory
- On-the-fly functional mode: A byte stream received from PPI is interpreted as a MIPI CSI-2 stream. Pixels are extracted and sent to the system memory.

- MIPI CSI-2 low level protocol support:
 - Up to 8 contexts (VCT + DT combinations)
 - Data lane merger
 - Error detection/correction (CRC/ECC)
 - Re-synchronization FIFO
- Up to four [4] independent pixel processing contexts:
 - All primary and secondary MIPI CSI-2 formats supported
 - Extract pixels from byte stream
 - DPCM decompression (4 pixels/cycle for predictor1; 1 pixel/cycle for predictor2)
 - DPCM compression (2 pixels/cycle for predictor1; predictor2 is not supported)
 - Pixel packing into a byte stream (for memory storage)
- Up to eight [8] independent write DMA contexts:
 - Write header, pixel, or attribute data
 - Horizontal cropping
 - Pack data from independent streams into efficient OCP transactions
 - 1D and 2D addressing modes (only INCR bursts)
 - Resynchronize on line boundaries (for TxBuffer overflows)
 - Linear, circular, and sub-sampled addressing modes

CALSS does not support the following features:

- ECC on internal RAMs

For more information, see section *Camera Adapter Layer (CAL) Subsystem* in the device TRM.

6.4.5.3 CPSW2G

The two-port Gigabit Ethernet MAC (MCU_CPSW0) subsystem provides Ethernet packet communication for the device and is configured in a similar manner as a two-port Ethernet switch. MCU_CPSW0 features the Reduced Gigabit Media Independent Interface (RGMI), Reduced Media Independent Interface (RMII), and the Management Data Input/Output (MDIO) interface for physical layer device (PHY) management.

The MCU_CPSW0 subsystem provides the following features:

- One Ethernet port (port 1) with selectable RGMI and RMII interfaces and an internal Communications Port Programming Interface (CPPI) port (port 0)
- Synchronous 10/100/1000 Mbit operation
- Flexible logical FIFO-based packet buffer structure
- Eight priority level Quality Of Service (QOS) support (802.1p)
- Support for Audio/Video Bridging (P802.1Qav/D6.0)
- Support for IEEE 1588 Clock Synchronization (2008 Annex D, Annex E and Annex F)
 - Timestamp module capable of time stamping external timesync events like Pulse-Per-Second and also generating Pulse-Per-Second outputs
 - CPTS module that supports time stamping for IEEE1588 with support for 4 hardware push events and generation of compare output pulses
- DSCP Priority Mapping (IPv4 and IPv6)
- Energy Efficient Ethernet (EEE) support (802.3az)
- Flow Control (802.3x) Support
- Non Blocking switch fabric
- Time Sensitive Network Support
 - IEEE P902.3br/D2.0 Interspersing Express Traffic
 - IEEE 802.1Qbv/D2.2 Enhancements for Scheduled Traffic

- Address Lookup Engine (ALE)
 - Configurable number of addresses plus VLANs
 - Wire rate lookup
 - Host controlled time-based aging and/or auto-aging
 - Spanning tree support
 - L2 address lock and L2 filtering support
 - MAC authentication (802.1x)
 - Receive-based or destination-based Multicast and Broadcast rate limits
 - MAC address blocking
 - Source port locking
 - OUI (Vendor ID) host accept/deny feature
 - Configurable number of classifier/policers
 - VLAN support
 - 802.1Q compliant
 - Auto add port VLAN for untagged frames on ingress
 - Auto VLAN removal on egress and auto pad to minimum frame size
- EtherStats and 802.3Stats Remote network Monitoring (RMON) statistics gathering (per port)
- Ethernet CRC selectable per port
- Ethernet Mac transmit to Ethernet Mac receive Loopback mode (digital loopback) supported
- CPSGMII Loopback Modes (transmit to receive)
- Maximum frame size of 2024 bytes
- Management Data Input/Output (MDIO) module for PHY Management with Clause 45 support
- Programmable interrupt control with selected interrupt pacing
- Host port CPPI Streaming Packet Interface (CPPI_GCLK)
- Flow Control Support (802.3x)
- Digital loopback and FIFO loopback modes supported
- Emulation support
- Full duplex mode supported in 10/100/1000 Mbps. Half-duplex mode supported only in 10/100 Mbps modes only.
- RAM Error Detection and Correction (SECCDED)

The following MCU_CPSW0 features are not supported:

- Maximum frame size of 9600 bytes
- MII/ GMII Mode
- SGMII Mode
- MACSEC
- Synchronous Ethernet
- Software reset
- Ethernet Port Reset Isolation
- Rate-limiting is not supported in half-duplex mode
- Dual VLAN switch operations are not supported
- Gigabit half-duplex mode is not supported (10/100 Mbps half-duplex mode is supported).
- RGMII Internal Delay Mode disabled.

For more information, see section *Gigabit Ethernet MAC (MCU_CPSW0)* in the device TRM.

6.4.5.4 DCC

The Dual Clock Comparator (DCC) is used to determine the accuracy of a clock signal during the time execution of an application. Specifically, the DCC is designed to detect drifts from the expected clock frequency. The desired accuracy can be programmed based on calculation for each application. The DCC measures the frequency of a selectable clock source using another input clock as a reference.

The device has eleven instances of DCC modules.

The DCC uses two independent clock sources to detect when one is out of spec. Each DCC module implements the following features:

- Two independent counter blocks count clock pulses from each clock source
- Each counter block is programmable, however, for proper operation the counters must be programmed with seed values that respect the ratio of the two clock frequencies
- Configurable timebase for error signal
- Error signal generation when one of the clocks is out of spec
- Clock frequency measurement

For more information, see section *Dual Clock Comparator (DCC)* in the device TRM.

6.4.5.5 DDRSS

The DDR subsystem in this device comprises DDR controller, DDR PHY and wrapper logic to integrate these blocks in the device. The DDR subsystem is referred to as DDRSS0 and is used to provide an interface to external SDRAM devices which can be utilized for storing program or data. DDRSS0 is accessed via MSMC, and not directly through the system interconnect.

The DDRSS0 supports:

- Memory Types:
 - DDR3L
 - DDR4
 - LPDDR4
- Memory Bus Features:
 - 39-bit width with ECC (32 bits for data and 7 bits for ECC)
 - 1/2 width (22-bit) mode via software configuration
 - 1/4 width (13-bit) mode via software configuration
 - Up to 2 ranks (LPDDR4 only)
 - SDRAM address range up to 32 GB
- System Bus Interface:
 - 256-bit data width
 - Clock asynchronous to DDR clock
 - Little endian only
 - Address aliasing prevention to block accesses to unpopulated SDRAM region
- Configuration Bus Interface:
 - 32-bit data width
 - Linear incrementing addressing mode
 - 32-bit aligned accesses only
 - Little endian only

- Key Features:
 - Full coherency across all commands
 - Bank interleaving
 - Priority based scheduling
 - Scheduling based on bank openness
 - Class of Service (CoS)
 - Three latency classes supported
 - Programmable counters to tune CoS
 - Read/write scheduling to avoid turn-around time
 - Prioritized refresh scheduling
 - Dynamic change of refresh rate via software for extended temperatures
 - Statistical counters for performance management
- ECC Features:
 - SEC/DED for 32-bit interface (39-bit with ECC)
 - Supported only for DDR3 and DDR4
 - SEC/DED for 16-bit interface (22-bit with ECC)
 - Supported for DDR3, DDR4, and LPDDR4
 - SEC/DED for 8-bit interface (13-bit with ECC)
 - Supported only for DDR3 and DDR4
 - Read-modify-write ECC for sub-word writes
 - ECC address error logging
 - Statistical counters for counting ECC errors
 - Injecting ECC errors during normal operation for validation
 - Automatic ECC scrub operation inside the DDR controller for any read command received which has led to a single-bit error.
 - At any time, only one outstanding ECC scrub operation is allowed inside the DDR controller
- Low Power Features:
 - All power modes defined by JEDEC (clock stop for LPDDR_x, self-refresh, power-down, etc.)
 - Self-refresh entry and exit via software or clock stop req/ack
 - System bus clock stop via clock stop request when controller is idle
 - Automatic idle power saving mode when no or low activity is detected
 - DDR and system bus clock frequency change using self-refresh via software or clock stop request
 - Turning off SoC power after DDR is put into self-refresh (DDR reset and CKE IO retention)
- Functional Safety Features:
 - ECC on data
 - Parity on address and command
 - ECC on internal RAMs

- DDR PHY Features:
 - Partial data macro use for ECC in 39-bit and 22-bit mode
 - Automatic and software controllable DDR-PHY and I/Os initialization and calibration (ZQ)
 - Automatic and software controllable delay line calibrations with voltage and temperature (VT) compensation
 - Automatic and software controllable write levelling with VT compensation
 - Automatic read DQS gating training per rank with VT compensation
 - Automatic and software controllable DQ/DQS eye training per rank
 - Automatic and software controllable read and write data bit deskew
 - Automatic and software controllable Command/Address (CA) levelling with VT compensation for LPDDR4
 - Automatic and software controllable CA bit deskew for LPDDR4
 - Refreshes to SDRAM during leveling and training
 - Any bit in the byte lane as prime bit for write leveling and read trainings
 - No seeding requirement based on board topology for any of the leveling and training algorithms
 - Max channel length of 3 inches with controlled impedance for command and data channels
 - Dynamic/automatic I/O receiver disable when read transfer is not on going
 - Capability of disabling unused data macros and I/Os when not in use

DDRSS0 does not support the following:

- 4-bit wide DDR4 devices
- UDIMMs
- SODIMMs
- RDIMMs
- LRDIMMs
- Address mirroring for DIMMs
- Data bus obfuscation or any other kind of encryption
- Automatic periodic scrubbing of SDRAM for ECC
- 32-bit with ECC (39-bit) for LPDDR4
- 8-bit with ECC (13-bit) for LPDDR4
- 8-bit without ECC for LPDDR4
- Two independent 16-bit channel operation for LPDDR4
- DDR4 DBI mode
- DDR3 SDRAMs
- DDR3U SDRAMs
- LPDDR3 SDRAMs
- LPDDR2 SDRAMs
- LPDDR4X SDRAMs
- Only single rank is supported for DDR3L and DDR4
- Hardware FFC (Fast Frequency Change)
- DDR4 Geardown mode
- Write data CRC for DDR4 when ECC is enabled
- PLL bypass mode for AC and Data macros

For more information, see section *DDR Subsystem (DDRSS)* in the device TRM.

6.4.5.6 DSS

The Display Subsystem (DSS) is a flexible, multi-pipeline subsystem that supports high-resolution display outputs. DSS includes input pipelines providing multi-layer blending with transparency to enable on-the-fly composition. Various pixel processing capabilities are supported, such as color space conversion and scaling, among others. DSS includes a DMA engine, which allows direct access to the frame buffer (device system memory). Display outputs can connect seamlessly to an Open LVDS Display Interface transmitter (OLDITX), or can directly drive device pads as a parallel video output interface.

The device includes one instantiation of DSS named DSS0 (with a single OLDITX0 instance).

DSS includes a Display Controller (DISPC), with the following main features:

- Internal DMA engine:
 - Support for 1D DMA transfers only
 - Support for 48-bit addressable memory space
 - No support for rotation and memory fragmentation
 - Integrated buffers between DMA engine and video pipelines
 - Programmable buffer thresholds
 - Self-refresh using the DMA buffers (outputting data on display only from the DMA buffer)
 - Arbitration between normal/low priority pipelines
 - On-the-fly support for source image flip along X and Y axis (flip/mirror support)
 - Support for up to 4K-pixels wide frame buffer for 8/16/32/64-bit per pixel, if the frame buffer is used without scaling (that is, no upscale/downscale) in the video pipelines
 - Support for up to 2560-pixels wide frame buffer for 8/16-bit per pixel, if scaling is enabled in video pipelines
 - Support for up to 1280-pixels wide frame buffer for 32-bit per pixel, if scaling is enabled in video pipelines
 - Support for up to 640-pixels wide frame buffer for 64-bit per pixel, if scaling is enabled in video pipelines
 - Support for secure access to firewall protected frame buffer in DDR memory
 - Support for MFLAG mechanism to indicate critical fullness of DMA buffer (close to underflow for a video pipeline)

- One Video Pipeline (VID):
 - RGB input source pixel formats support:
 - BITMAP1, BITMAP2, BITMAP4, BITMAP8
 - ARGB16-4444, ABGR16-4444, RGBA16-4444, RGB16-565, BGR16-565, ARGB16-1555, ABGR16-1555
 - RGB16-565/BGR16-565 with a separate A8 plane
 - RGB24-888, BGR24-888
 - ARGB32-8888, ABGR32-8888, BGRA32-8888, RGBA32-8888, ARGB32-2101010, ABGR32-2101010
 - ARGB64-16161616, RGBA64-16161616
 - Additionally, equivalent RGBx, xRGB, xBGR, and BGRx pixel formats defined, considering that A component of RGBA, ARGB, ABGR, BGRA pixel formats is ignored by DSS hardware (for example, ARGB -> xRGB, where A can be ignored by not selecting alpha pixel)
 - Pre-multiplied ARGB/RGBA formats
 - YUV input source pixel formats support:
 - Packed: YUV422-UYVY, YUV422-YUV2
 - 2-plane: YUV420-NV12, YUV420-NV21
 - 8-bit per component support for all YUV formats
 - 10/12-bit per component packed/unpacked source format support for YUV420/422 (internally processed as 8-bit component data)
 - Programmable poly-phase filter (scaler):
 - Independent horizontal and vertical resampling: up-sampling (up to x16), and down-sampling (down to 1/4)
 - Maximum input width supported: 1280 pixels (using 32-bit pixels and 5-tap mode), 2560 pixels (using 16-bit pixels and 5-tap mode), and 2560 pixels (using 32-bit pixels and 3-tap mode)
 - No limitation on the input height
 - Supported input pixel formats: ARGB48-12121212, YUV422-UYVY, YUV422-YUV2, and YUV420-NV12. The alpha channel is rescaled like the R, G and B color components. 16 phases with symmetrical coefficients are implemented.
 - Programmable color space conversion (CSC) from YUV422/YUV420 (after chroma upsampled to YUV444 using the scaler) into ARGB48-12121212
 - Programmable Brightness/Contrast/Hue/Saturation using the CSC block
 - Programmable VC1 range mapping
 - Luma Key generation
 - 256 x 24-bit entries color look-up table (CLUT), used either to convert BITMAP (1, 2, 4, or 8-bit indexed formats) into RGB format, or for RGB to RGB inverse gamma correction

- One Video Lite Pipeline (VIDL1)
 - RGB input source pixel formats support:
 - BITMAP1, BITMAP2, BITMAP4, BITMAP8
 - ARGB16-4444, ABGR16-4444, RGBA16-4444, RGB16-565, BGR16-565, ARGB16-1555, ABGR16-1555
 - RGB16-565/BGR16-565 with a separate A8 plane
 - RGB24-888, BGR24-888
 - ARGB32-8888, ABGR32-8888, BGRA32-8888, RGBA32-8888, ARGB32-2101010, ABGR32-2101010
 - ARGB64-16161616, RGBA64-16161616
 - Additionally, equivalent RGBx, xRGB, xBGR, and BGRx pixel formats defined, considering that A component of RGBA, ARGB, ABGR, BGRA pixel formats is ignored by DSS hardware (for example, ARGB -> xRGB, where A can be ignored by not selecting alpha pixel)
 - Pre-multiplied ARGB/RGBA formats
 - YUV input source pixel formats support:
 - Packed: YUV422-UYVY, YUV422-YUV2
 - 2-plane: YUV420-NV12, YUV420-NV21
 - 8-bit per component support for all YUV formats
 - 10/12-bit per component packed/unpacked source format support for YUV420/422 (internally processed as 8-bit component data)
 - YUV420 to YUV422 chroma upsampling using an average filter
 - YUV422 to YUV444 chroma upsampling using a 4-tap filter based on Catmull-Rom algorithm
 - Programmable color space conversion (CSC) from YUV422/YUV420 into ARGB48-12121212
 - Programmable Brightness/Contrast/Hue/Saturation using the CSC block
 - Programmable VC1 range mapping
 - Luma Key generation
 - 256 x 24-bit entries color look-up table (CLUT), used either to convert BITMAP (1, 2, 4, or 8-bit indexed formats) into RGB format, or for RGB to RGB inverse gamma correction
- Two Overlay Managers (OVR1 and OVR2):
 - Input pixel format: ARGB48-12121212
 - Output pixel format: ARGB48-12121212
 - Transparency color key (source and destination)
 - Programmable background color
 - Alpha blending support: embedded pixel alpha (ARGB and RGBA), global pixel, combination of global pixel and pixel alpha
 - Z-order programmable (full flexibility)
 - Color bar test pattern insertion

- Two Video Port outputs (VP1 and VP2):
 - Up to 24 bits per pixel on the output interface (selection between 12, 16, 18, or 24 bits)
 - Independent programmable timing generator for each VP output to support up to 165 MHz pixel clock frequency for video formats defined in CEA-861-E and VESA-DMT standards (including 1600x1200@60fps or 1920x1200@60fps with reduced blanking)
 - Independent programmable 8-bit gamma correction support on each VP output
 - Fully programmable color space conversion matrix to serve as color phase rotation (CPR) and/or as brightness/contrast/saturation control on the combined output
 - Independent programmable multiple cycles output format on 8/9/12/16-bit time division multiplexed (TDM) interface for each VP output
 - Configurable VP output mode: progressive or interlaced mode
 - Selection between RGB and YUV422 output pixel format (YUV422 only available when a BT mode is enabled)
- Safety Features:
 - Supports up to 4 programmable (position/size) safety check regions on each display output
 - Support for 1 safety check region on each input video pipeline output
 - Support for MISR (Multiple Input Signature Register) on each safety region, used to perform data correctness check and/or freeze frame detection

DSS integrates a single-link Open LVDS Display Interface transmitter (OLDITX) with the following main features:

- Up to 170MHz input pixel data interface support: RGB[23:0], VS, HS, DE. Limited by the maximum data rate provided by the DISPC video port output connected to OLDITX.
- Single (non-duplicate) OLDI output link mode.
- 18-bit or 24-bit output with OLDI mapping modes (three or four LVDS data channels, one clock channel).
- LVDS signaling: Compliant with ANSI/TIA/EIA644-A standard (Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits).
- LVDS transmit throughput performance: WUXGA (1920x1200@60), 162 MHz pixel clock resolution.
- Test support features: Built-in pattern generator; loopback mode.

DSS provides two interfaces to device interconnect:

- One 128-bit master port (with MFLAG support), used by the DISPC DMA engine to read data from device system memory.
- One 32-bit slave port, used for configuration of the memory mapped registers inside DSS.

DISPC does not support the following features:

- Write-back pipeline for memory-to-memory composition
- 2-D tiled buffer access
- On-the-fly rotation
- Compressed data format
- Fragmented frame buffers
- YUV formats (YUV420/YUV422) on the video pipeline inputs and video port outputs (BT.656/BT.1120 modes)

OLDITX does not support the following features:

- Single link duplication mode
- Dual link (master or slave) mode
- DC balanced mode on LVDS output
- Hot plug detection
- EDID/DDC

- Gamma correction
- Internal PLL clock recovery
- Digital display information protection

For more information, see section *Display Subsystem (DSS)* in the device TRM.

6.4.5.7 ECAP

The enhanced Capture (ECAP) module can be used for:

- Sample rate measurements of audio inputs
- Speed measurements of rotating machinery (for example, toothed sprockets sensed via Hall sensors)
- Elapsed time measurements between position sensor pulses
- Period and duty cycle measurements of pulse train signals
- Decoding current or voltage amplitude derived from duty cycle encoded current/voltage sensors.

The ECAP module includes the following features:

- 32-bit time base counter
- 4-event time-stamp registers (each 32 bits)
- Edge polarity selection for up to four sequenced time-stamp capture events
- Interrupt on any of the four events
- Single shot capture of up to four event time-stamps
- Continuous mode capture of time-stamps in a four-deep circular buffer
- Absolute time-stamp capture
- Difference (Delta) mode time-stamp capture
- All above resources dedicated to a single input pin
- When not used in capture mode, the ECAP module can be configured as a single channel PWM output.

For more information, see section *Enhanced Capture (ECAP) Module* in the device TRM.

6.4.5.8 EPWM

An effective PWM peripheral must be able to generate complex pulse width waveforms with minimal CPU overhead or intervention. It needs to be highly programmable and very flexible while being easy to understand and use. The EPWM unit described here addresses these requirements by allocating all needed timing and control resources on a per PWM channel basis. Cross coupling or sharing of resources has been avoided; instead, the EPWM is built up from smaller single channel modules with separate resources and that can operate together as required to form a system. This modular approach results in an orthogonal architecture and provides a more transparent view of the peripheral structure, helping users to understand its operation quickly.

In the further description the letter x within a signal or module name is used to indicate a generic EPWM instance on a device. For example, output signals EPWMxA and EPWMxB refer to the output signals from the EPWMx instance. Thus, EPWM1A and EPWM1B belong to EPWM1, EPWM2A and EPWM2B belong to EPWM2, and so forth.

Additionally, the EPWM integration allows this synchronization scheme to be extended to the capture peripheral modules (ECAP). The number of modules is device-dependent and based on target application needs. Modules can also operate stand-alone.

The device has six instances of EPWM modules.

Each EPWM module supports the following features:

- Dedicated 16-bit time-base counter with period and frequency control

- Two PWM outputs (EPWMxA and EPWMxB) that can be used in the following configurations:
 - Two independent PWM outputs with single-edge operation
 - Two independent PWM outputs with dual-edge symmetric operation
 - One independent PWM output with dual-edge asymmetric operation
- Asynchronous override control of PWM signals through software
- Programmable phase-control support for lag or lead operation relative to other EPWM modules
- Hardware-locked (synchronized) phase relationship on a cycle-by-cycle basis
- Dead-band generation with independent rising and falling edge delay control
- Programmable trip zone allocation of both cycle-by-cycle trip and one-shot trip on fault conditions
- A trip condition can force either high, low, or high-impedance state logic levels at PWM outputs
- Allows events to trigger both CPU interrupts and ADC start of conversions
- Programmable event prescaling minimizes CPU overhead on interrupts
- PWM chopping by high-frequency carrier signal, useful for pulse transformer gate drives
- High-resolution module with programmable delay line
 - Programmable on a per PWM period basis
 - Can be inserted either on the rising edge or falling edge of the PWM pulse or both or not at all.

EHRPWM Not Supported Features:

- EPWM digital comparator modules are not supported

For more information, see section *Enhanced Pulse Width Modulation (EPWM) Module* in the device TRM.

6.4.5.9 ELM

The ELM is used with the GPMC. Syndrome polynomials generated on-the-fly when reading a NAND flash page and stored in GPMC registers are passed to the ELM. A host processor can then correct the data block by flipping the bits to which the ELM error-location outputs point.

When reading from NAND flash memories, some level of error-correction is required. In the case of NAND modules with no internal correction capability, sometimes referred to as *bare NANDs*, the correction process is delegated to the memory controller. ELM can be also used to support parallel NOR flash or NAND flash.

The General-Purpose Memory Controller (GPMC) probes data read from an external NAND flash and uses this to compute checksum-like information, called syndrome polynomials, on a per-block basis. Each syndrome polynomial gives a status of the read operations for a full block, including 512 bytes of data, parity bits, and an optional spare-area data field, with a maximum block size of 1023 bytes. Computation is based on a Bose-Chaudhuri-Hocquenghem (BCH) algorithm. The ELM extracts error addresses from these syndrome polynomials.

Based on the syndrome polynomial value, the ELM can detect errors, compute the number of errors, and give the location of each error bit. The actual data is not required to complete the error-correction algorithm. Errors can be reported anywhere in the NAND flash block, including in the parity bits.

The maximum acceptable number of errors that can be corrected depends on a programmable configuration parameter. 4-, 8-, and 16-bit error-correction levels are supported. The ELM depends on a static and fixed definition of the generator polynomial for each error-correction level that corresponds to the generator polynomials defined in the GPMC (there are three fixed polynomial for the three correction error levels). A larger number of errors than the programmed error-correction level may be detected, but the ELM cannot correct them all. The offending block is then tagged as *uncorrectable* in the associated computation exit status register. If the computation is successful, that is, if the number of errors detected does not exceed the maximum value authorized for the chosen correction capability, the exit status register contains the information on the number of detected errors.

When the error-location process completes, an interrupt is triggered to inform the software that its status can be checked. The number of detected errors and their locations in the NAND block can be retrieved from the module through register accesses.

The ELM has the following features:

- 4, 8, and 16 bits per 512-byte block error-location, based on BCH algorithms
- Eight simultaneous processing contexts
- Page-based and continuous modes
- Interrupt generation on error-location process completion:
 - When the full page has been processed in page mode
 - For each syndrome polynomial in continuous mode.

The following features are not supported on this family of devices:

- Local power management of clock activity

For more information, see section *Error Location Module (ELM)* in the device TRM.

6.4.5.10 ESM

The Error Signaling Module (ESM) aggregates safety-related events and/or errors from throughout the device into one location. It can signal both low and high priority interrupts to a processor to deal with a safety event and/or manipulate an I/O error pin to signal an external hardware that an error has occurred. Therefore an external controller is able to reset the device or keep the system in a safe, known state.

The device has three instances of ESM modules.

Each ESM module implements the following features:

- Up to 1024 error event inputs
 - Implemented in groups of 32 events
 - Level or Pulse inputs (Pulse inputs are triple redundant)
- Selectable low and high priority interrupt error pin prioritization of each error event
- Error pin to signal severe device failure
- Configurable timebase for error signal
- Error forcing capability
- Internal redundant flops on safety critical fields

For more information, see section *Error Signaling Module (ESM)* in the device TRM.

6.4.5.11 EQEP

The Enhanced Quadrature Encoder Pulse (EQEP) peripheral is used for direct interface with a linear or rotary incremental encoder to get position, direction and speed information from a rotating machine for use in high performance motion and position control system. The disk of an incremental encoder is patterned with a single track of slots patterns. These slots create an alternating pattern of dark and light lines. The disk count is defined as the number of dark/light line pairs that occur per revolution (lines per revolution). As a rule, a second track is added to generate a signal that occurs once per revolution (index signal: QEPI), which can be used to indicate an absolute position. Encoder manufacturers identify the index pulse using different terms such as index, marker, home position and zero reference.

To derive direction information, the lines on the disk are read out by two different photo-elements that "look" at the disk pattern with a mechanical shift of 1/4 the pitch of a line pair between them. This shift is realized with a reticle or mask that restricts the view of the photo-element to the desired part of the disk lines. As the disk rotates, the two photo-elements generate signals that are shifted 90 degrees out of phase from each other. These are commonly called the quadrature QEPA and QEPB signals. The clockwise direction for most encoders is defined as the QEPA channel going positive before the QEPB channel and vice versa.

The encoder wheel typically makes one revolution for every revolution of the motor or the wheel may be at a geared rotation ratio with respect to the motor. Therefore, the frequency of the digital signal coming from the QEPA and QEPB outputs varies proportionally with the velocity of the motor. For example, a 2000-line encoder directly coupled to a motor running at 5000 revolutions per minute (rpm) results in a frequency of 166.6 kHz, so by measuring the frequency of either the QEPA or QEPB output, the processor can determine the velocity of the motor.

The EQEP module includes the following features:

- EQEP inputs (A/B/INDEX and STROBE) are available at chip level
- EQEP phase error output is also available.

The following EQEP features are not supported:

- EQEP quadrature outputs (A and B) are not pinned out

For more information, see section *Enhanced Quadrature Encoder Pulse (EQEP) Module* in the device TRM.

6.4.5.12 GPIO

The General-Purpose Input/Output (GPIO) peripheral provides dedicated general-purpose pins that can be configured as either inputs or outputs. When configured as an output, the user can write to an internal register to control the state driven on the output pin. When configured as an input, user can obtain the state of the input by reading the state of an internal register.

In addition, the GPIO peripheral can produce host CPU interrupts and DMA synchronization events in different interrupt/event generation modes.

The device has three instances of GPIO modules. The GPIO pins are grouped into banks (16 pins per bank and 9 banks per module), which means that each GPIO module provides up to 144 dedicated general-purpose pins with input and output capabilities; thus, the general-purpose interface supports up to 432 (3 instances × (9 banks × 16 pins)) pins. Since WKUP_GPIO0_[56:143], GPIO0_[96:143], and GPIO1_[90:143] are reserved in this device, general purpose interface supports up to 242 pins.

Each channel in the GPIO modules has the following features:

- Supports 9 banks of 16 GPIO signals
- Supports up to 9 banks of interrupt capable GPIOs
- Interrupts:
 - Can enable interrupts for each bank of 16 GPIO signals
 - Interrupts can be triggered by rising and/or falling edge, specified for each interrupt capable GPIO signal
- Set/clear functionality:
 - Firmware writes 1 to corresponding bit position(s) to set or to clear GPIO signal(s). This allows multiple firmware processes to toggle GPIO output signals without critical section protection (disable interrupts, program GPIO, re-enable interrupts, to prevent context switching to another process during GPIO programming).
- Separate Input/Output registers:
 - If preferred by firmware, some GPIO output signals can be toggled by direct write to the output register(s) in addition to set/clear.
 - Output register, when read in, reflects output drive status. This, in addition to the input register reflecting pin status, allows wired logic be implemented.

GPIO do not support the following features:

- The following apply to WKUP_GPIO0:
 - WKUP_GPIO0_[56:143] are not pinned out.
 - Interrupts [56:143] are not pinned out.
 - Bank Interrupts [8:4] are not pinned out.

- The following apply to GPIO0:
 - GPIO0_[96:143] are not pinned out.
 - Interrupts [96:143] are not pinned out.
 - Bank Interrupts [8:6] are not pinned out.
- The following apply to GPIO1:
 - GPIO1_[90:143] are not pinned out.
 - Interrupts [90:143] are not pinned out.
 - Bank Interrupts [8:6] are not pinned out.
 - GPI[10] and GPI[77] buffer is input only.
 - Interrupt [10] and [77] buffer is output only.
 - GPO[12] buffer is output only.

For more information, see section *General-Purpose Interface (GPIO)* in the device TRM.

6.4.5.13 GPMC

The General-Purpose Memory Controller is a unified memory controller dedicated for interfacing with external memory devices like:

- Asynchronous SRAM-like memories and application-specific integrated circuit (ASIC) devices
- Asynchronous, synchronous, and page mode (available only in non-multiplexed mode) burst NOR flash devices
- NAND flash
- Pseudo-SRAM devices

The main features of the GPMC are:

- 8- or 16-bit-wide data path to external memory device
- Supports up to 4 chip select regions of programmable size and programmable base addresses in a total address space of 1GB
- Supports on-the-fly error code detection using the Bose-Chaudhuri-Hocquenghem (BCH) (t = 4, 8, or 16) or Hamming code to improve the reliability of NAND with a minimum effect on software (NAND flash with 512-byte page size or greater)
- Fully pipelined operation for optimal memory bandwidth usage
- The clock to the external memory is provided from GPMC_FICLK divided by 1, 2, 3, or 4
- Supports programmable autoclock gating when no access is detected
- Independent and programmable control signal timing parameters for setup and hold time on a per-chip basis. Parameters are set according to the memory device timing parameters with a timing granularity of one GPMC_FICLK clock cycle.
- Flexible internal access time control (wait state) and flexible handshake mode using external WAIT pin monitoring
- Support bus keeping
- Support bus turnaround
- Prefetch and write-posting engine associated with DMA controller at system level to achieve full performance from the NAND device with minimum effect on NOR/SRAM concurrent access
- 32-bit interconnect slave interface which supports non-wrapping and wrapping burst of up to 16x32 bits.

The GPMC supports the following various access types:

- Asynchronous read/write access
- Asynchronous read page access (4, 8, and 16 Word16)
- Synchronous read/write access
- Synchronous read/write burst access without wrap capability (4, 8 and 16 Word16)

- Synchronous read/write burst access with wrap capability (4, 8 and 16 Word16)
- Address-data-multiplexed (AD) access
- Address-address-data (AAD) multiplexed access
- Little-endian access only

The GPMC can communicate with a wide range of external devices:

- External asynchronous or synchronous 8-bit wide memory or device (non burst device)
- External asynchronous or synchronous 16-bit wide memory or device
- External 16-bit non-multiplexed NOR flash device
- External 16-bit address and data multiplexed NOR Flash device
- External 8-bit and 16-bit NAND flash device
- External 16-bit pseudo-SRAM (pSRAM) device

The following features are not supported on this family of devices:

- DMA mode is not supported.
- WAIT[3-2] are not pinned out. All CS regions must use WAIT0 or WAIT1.
- Asynchronous page write mode is not supported.
- Multiple write access in asynchronous mode is not supported.
- Multiple read is not supported in address/data-multiplexed and AAD-multiplexed modes.

For more information, see section *General-Purpose Memory Controller (GPMC)* in the device TRM.

6.4.5.14 HYPERBUS

The HyperBus module is a part of the device Flash Subsystem (FSS).

The HyperBus module is a low pin count memory interface that provides high read/write performance. The HyperBus module connects to HyperBus memory (HyperFlash or HyperRAM) and uses simple HyperBus protocol for read and write transactions.

There is one HyperBus module inside the device. The HyperBus module includes one HyperBus Memory Controller (HBMC).

HyperBus module supports the following features:

- Support for Cypress® HyperFlash and HyperRAM
- Up to 166 MHz maximum memory bus operation for reads
 - Supports up to 166 MHz dual data rate (333 MBps) flash devices for system requiring rapid boot or instant-on displays
 - Supports up to 333 MBps external pseudo-RAM (HyperRAM) for systems
- Low pin count interface with LVCMOS I/O pins (can be muxed with other FSS interfaces (OSPIs))
- Two memory chip selects
- Linear incrementing mode for reads and writes
- Up to 16 outstanding read transactions
- Asynchronous bus clock

HyperBus Not Supported Features:

- Cache-line wrap and fixed address modes for reads or writes
- General Purpose Output register of the HBMC is not used

For more information, see section *HyperBus Interface* in the device TRM.

6.4.5.15 I2C

The device contains six multimaster Inter-Integrated Circuit (I2C) controllers each of which provides an interface between a local host (LH), such as an Arm and any I2C-bus-compatible device that connects via the I2C serial bus. External components attached to the I2C bus can serially transmit and receive up to 8 bits of data to and from the LH device through the 2-wire I2C interface.

Each multimaster I2C module can be configured to act like a slave or master I2C-compatible device.

The WKUP_I2C0 and MCU_I2C0 controllers have dedicated I2C compliant open drain buffers, and support fast mode (up to 400 Kbps). The I2C0, I2C1, I2C2, and I2C3 controllers are multiplexed with standard LVCMOS I/O and connected to emulate open drain. The I2C emulation is achieved by configuring the LVCMOS buffers to output Hi-Z instead of driving high when transmitting logic 1.

The multimaster I2C module has the following features:

- Compliant with Philips I2C-bus specification version 2.1
- Supports a standard mode (up to 100 Kbps) and fast mode (up to 400 Kbps)
- 7-bit and 10-bit device addressing modes
- General call
- Start/Restart/Stop
- Multimaster transmitter/slave receiver mode
- Multimaster receiver/slave transmitter mode
- Built-in FIFO for buffered read or write
 - Programmable size of 8-64 bytes
- Module enable/disable capability
- Programmable multislave channel (responds to four separate addresses)
- Programmable clock generation
- 8-bit-wide data access
- Low power consumption
- Support Auto Idle mechanism
- Support Idle Request/Idle Acknowledge handshake mechanism
- Support for asynchronous wakeup mechanism
- Wide interrupt capability

I2C Not Supported Features:

- Serial Camera Control Bus (SCCB) Protocol
- High-Speed (HS) Mode
- DMA Mode
- Full I2C electrical compliance (only for MAIN domain I2C modules)
- Local power management of clock activity

For more information, see section *Inter-Integrated Circuit (I2C) Interface* in the device TRM.

6.4.5.16 MCAN

The Controller Area Network (CAN) is a serial communications protocol which efficiently supports distributed real-time control. CAN has high immunity to electrical interference. In a CAN network, many short messages are broadcast to the entire network, which provides for data consistency in every node of the system.

The MCAN module supports both classic CAN and CAN FD (CAN with Flexible Data-Rate) specifications. CAN FD feature allows high throughput and increased payload per data frame. The classic CAN and CAN FD devices can coexist on the same network without any conflict.

The device supports two MCAN modules - MCU_MCAN0 and MCU_MCAN1. They connect to the physical layer of the CAN network through external (for the device) transceivers. Each MCAN module supports flexible bit rates greater than 1 Mbps and is compliant to ISO 11898-1:2015.

Each MCAN module implements the following features:

- Conforms with CAN Protocol 2.0 A, B and ISO 11898-1:2015
- Full CAN FD support (up to 64 data bytes)
- SAE J1939 support
- AUTOSAR support (only on DRA80xM family of devices)
- Up to 32 dedicated Transmit Buffers
- Configurable Transmit FIFO, up to 32 elements
- Configurable Transmit Queue, up to 32 elements
- Configurable Transmit Event FIFO, up to 32 elements
- Up to 64 dedicated Receive Buffers
- Two configurable Receive FIFOs, up to 64 elements each
- Up to 128 filter elements
- Internal Loopback mode for self-test
- Maskable interrupts, two interrupt lines
- Two clock domains (CAN clock/Host clock)
- Parity/ECC support - Message RAM single error correction and double error detection (SECEDED) mechanism
- Local power-down and wakeup support
- Timestamp Counter

MCAN subsystems do not support the following features:

- Host bus firewall
- GPIO mode
- Clock calibration
- External (IO) Loopback mode
- Debug DMA
- TX DMA channels [31:3]
- AUTOSAR (on AM65x family of devices)

For more information, see section *Modular Controller Area Network (MCAN)* in the device TRM.

6.4.5.17 MCASP

The MCASP functions as a general-purpose audio serial port are optimized to the requirements of various audio applications. The MCASP module can operate in both transmit and receive modes. The MCASP is useful for time-division multiplexed (TDM) stream, Inter-IC Sound (I2S) protocols reception and transmission as well as for an intercomponent digital audio interface transmission (DIT). The MCASP has the flexibility to gluelessly connect to a Sony/Philips digital interface (S/PDIF) transmit physical layer component.

Although intercomponent digital audio interface reception (DIR) mode (this is, S/PDIF stream receiving) is not natively supported by the MCASP module, a specific TDM mode implementation for the MCASP receivers allows an easy connection to external DIR components (for example, S/PDIF to I2S format converters).

The device has integrated three MCASP modules within:

- MCASP0 supporting up to 16 channels with independent TX/RX clock/sync domain
- MCASP1 supporting up to 10 channels with independent TX/RX clock/sync domain

- MCASP2 supporting up to 4 channels with independent TX/RX clock/sync domain

MCASP module includes the following main features:

- Independent serializer for each AXRx channel of each MCASP module.
- Clock stop request/acknowledge protocol
- A single 32-bit buffer per serializer for transmit and receive operations
- Interconnect interface port for CBASS0
- Two independent clock generator modules for transmit and receive (clocking flexibility allows the MCASP to receive and transmit at different rates. For example, the MCASP can receive data at 48 kHz but output up-sampled data at 96 kHz or 192 kHz)
- Each MCASP module functional clock can be generated:
 - internally (master mode)
 - supplied over MCASP serial interface (slave mode)
 - has a controllable functional clock divide ratio
- Independent transmit and receive modules, each includes:
 - Programmable clock and frame sync generator
 - TDM streams from 2 to 32, and 384 time slots
 - Support for time slot sizes of 8, 12, 16, 20, 24, 28, and 32 bits
 - Data formatter for bit manipulation
- Glueless connection to audio analog-to-digital converters (ADC), digital-to-analog converters (DAC), codec, digital audio interface receiver (DIR), and S/PDIF transmit physical layer components
- Wide variety of I2S and similar bit-stream format
- Integrated digital audio interface transmitter (DIT):
 - S/PDIF, IEC60958-1, AES-3 formats
 - Enhanced channel status/user data RAM
- 384-slot TDM with external digital audio interface receiver (DIR) device
 - For DIR reception, an external DIR receiver integrated circuit should be used with I2S output format and connected to the MCASP receive section
- Support for 2 × DMA requests (one per direction):
 - 1 level-sensitive transmit direct memory access (DMA) request common for all of the MCASP serializers
 - 1 level-sensitive receive direct memory access (DMA) request common for all of the MCASP serializers
 - All transmit DMA requests are mapped to the device DMA controllers
- One transmit interrupt request common for all serializers
- One receive interrupt request common for all serializers
- Each of the Rx and Tx interrupts is propagated to different host processors via the device Interrupts

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Because a serializer receive and transmit channels data is shared on the same MCASP data pin, user can choose to have either Tx or Rx function from a serializer, not both at the same time.

The MCASP module does not support the following features:

- Muting output (AMUTE)
- Muting input (AMUTEIN)

For more information, see section *Multichannel Audio Serial Port (MCASP)* in the device TRM.

6.4.5.18 MCRC

VBUSM CRC controller is a module which is used to perform CRC (Cyclic Redundancy Check) to verify the integrity of a memory system. A signature representing the contents of the memory is obtained when the contents of the memory are read into MCRC Controller. The responsibility of MCRC controller is to calculate the signature for a set of data and then compare the calculated signature value against a pre-determined good signature value. MCRC controller provides four channels to perform CRC calculation on multiple memories in parallel and can be used on any memory system. Channel 1 can also be put into data trace mode, where MCRC controller compresses each data being read through CPU read data bus.

MCRC has the following features:

- Four channels to perform background signature verification on any memory subsystem
- Data compression on 8-, 16-, 32-, and 64-bit data size
- Maximum-length PSA (Parallel Signature Analysis) register constructed based on 64-bit primitive polynomial
- Each channel has a CRC Value Register which contains the pre-determined CRC value
- Use timed base event trigger from timer to initiate DMA data transfer
- Programmable 20-bit pattern counter per channel to count the number of data patterns for compression
- Three modes of operation:
 - Auto
 - Semi-CPU
 - Full-CPU
- For each channel, CRC can be performed either by MCRC Controller or by CPU
- Automatically performs signature verification without CPU intervention in AUTO mode
- Generates interrupt to CPU in Semi-CPU mode to allow CPU to perform signature verification itself
- Generates CRC fail interrupt in AUTO mode if signature verification fails
- Generates Timeout interrupt if CRC is not performed within the time limit
- Generates DMA request per channel to initiate CRC value transfer
- An 128-byte block burst address for the PSA register to DMA without constant mode bus attribute

The following MCRC features are not supported by the module:

- Data trace capability on VBUSM, ITCM and DTCM data buses.

For more information, see section *Memory Cyclic Redundancy Check (MCRC) Controller* in the device TRM.

6.4.5.19 MCSPI

The MCSPI module is a multichannel transmit/receive, master/slave synchronous serial bus.

There are total of eight MCSPI modules in the device.

MCSPi3 and MCSPi4 include internal connectivity to MCSPI modules in the MCU domain, as follows:

- MCSPi3 is connected as a master to MCU_MCSPi1 by default at power-up. MCU_MCSPi1 and MCSPi3 may be optionally mapped to external device pads.
- MCSPi4 is directly connected as a slave to MCU_MCSPi2 by default at power-up. MCSPi4 and MCU_MCSPi2 are not pinned out externally.

The MCSPI modules include the following main features:

- Serial clock with programmable frequency, polarity, and phase for each channel
- Wide selection of MCSPI word lengths, ranging from 4 to 32 bits
- Up to four master channels, or single channel in slave mode

- Master multichannel mode:
 - Full duplex/half duplex
 - Transmit-only/receive-only/transmit-and-receive modes
 - Flexible input/output (I/O) port controls per channel
 - Programmable clock granularity
 - MCSPI configuration per channel. This means, clock definition, polarity enabling and word width
- Single interrupt line for multiple interrupt source events
- Enable the addition of a programmable start-bit for MCSPI transfer per channel (start-bit mode)
- Supports start-bit write command
- Supports start-bit pause and break sequence
- Programmable shift operations (1-32 bits)
- Programmable timing control between chip select and external clock generation
- Built-in FIFO available for a single channel.

The following features are not supported on this family of devices:

- Slave mode wake-up
- Retention during power down
- MCU_MCSPI2 and MCSPI4 are not pinned out
- MCSPI4 master mode is not supported
- Loopback testing is not available for MCSPI4 internal connection to MCU_MCSPI2 because DMA operation is not verified
- In slave mode only channel 0 is used
- Local power management of clock activity.

For more information, see section *Multichannel Serial Peripheral Interface (MCSPI)* in the device TRM.

6.4.5.20 MMC/SD

There are two MMCSD modules inside the device - MMCSD0 and MMCSD1. Each MMCSD module includes one MMCSD Host Controller.

Each controller has the following data bus width:

- MMCSD0 - 8-bit wide data bus
- MMCSD1 - 4-bit wide data bus

The MMCSD Host Controller provides an interface to eMMC 5.1 (embedded MultiMedia Card), SD 4.10 (Secure Digital), and SDIO 4.0 (Secure Digital IO) devices. The MMCSD Host Controller deals with MMC/SD/SDIO protocol at transmission level, data packing, adding cyclic redundancy checks (CRCs), start/end bit insertion, and checking for syntactical correctness.

Each MMCSD Host Controller supports:

- eMMC5.1 Host Specification (JESD84-B51)
- SD Host Controller Standard Specification 4.10
- Integrated DMA controller supporting SD Advanced DMA - ADMA2
- High Voltage eMMC – 3.3 V
- Dual Voltage eMMC – 1.8 V, 3.3 V
- System Bus Interface:
 - 64-bit data width (master interface)
 - 64-bit address
 - Clock asynchronous to MMCSD clock (MMCi_CLK)
 - Little endian only

- Configuration Bus Interface:
 - 32-bit data width (slave interface)
 - Linear incrementing addressing mode
 - 32-bit aligned accesses only
 - Little endian only

MMCSD0 Host Controller:

MultiMedia Card Support:

- eMMC Electrical Standard 5.1 (JESD84-B51)
- Backward compatible with earlier eMMC standards
- Legacy MMC SDR:
 - 3.3 V/1.8 V, 8-bit bus width, 0-25 MHz, 25 MBps
 - 3.3 V/1.8 V, 4-bit bus width, 0-25 MHz, 12.5 MBps
 - 3.3 V/1.8 V, 1-bit bus width, 0-25 MHz, 3.125 MBps
- High Speed SDR:
 - 3.3 V/1.8 V, 8-bit bus width, 0-50 MHz, 50 MBps
 - 3.3 V/1.8 V, 4-bit bus width, 0-50 MHz, 25 MBps
 - 3.3 V/1.8 V, 1-bit bus width, 0-50 MHz, 6.25 MBps
- High Speed DDR:
 - 3.3 V/1.8 V, 8-bit bus width, 0-50 MHz, 100 MBps
 - 3.3 V/1.8 V, 4-bit bus width, 0-50 MHz, 50 MBps
- HS200 SDR:
 - 1.8 V, 0-200 MHz, 8-bit bus width, 200 MBps
 - 1.8 V, 0-200 MHz, 4-bit bus width, 100 MBps

Secure Digital Card Support:

- Backward compatible with earlier SD card specifications
- SD Physical Layer Specification v3.01
- SDIO support
- SDIO Specification v3.00
- High Voltage SD memory card – 3.3 V
- Default Speed mode: 3.3 V signaling, frequency up to 25 MHz, up to 12.5 MBps
- High Speed mode: 3.3 V signaling, frequency up to 50 MHz, up to 25 MBps
- SDR12: UHS-I 1.8 V signaling, frequency up to 25 MHz, up to 12.5 MBps
- SDR25: UHS-I 1.8 V signaling, frequency up to 50 MHz, up to 25 MBps
- SDR50: UHS-I 1.8 V signaling, frequency up to 100 MHz, up to 50 MBps
- SDR104: UHS-I 1.8 V signaling, frequency up to 200 MHz, up to 100 MBps
- DDR50: UHS-I 1.8 V signaling, frequency up to 50 MHz, up to 50 MBps

MMCSD1 Host Controller:

MultiMedia Card Support:

- eMMC Electrical Standard 5.1 (JESD84-B51)
- Backward compatible with earlier eMMC standards
- Legacy MMC SDR:
 - 3.3 V/1.8 V, 4-bit bus width, 0-25 MHz, 12.5 MBps
 - 3.3 V/1.8 V, 1-bit bus width, 0-25 MHz, 3.125 MBps
- High Speed SDR:
 - 3.3 V/1.8 V, 4-bit bus width, 0-50 MHz, 25 MBps
 - 3.3 V/1.8 V, 1-bit bus width, 0-50 MHz, 6.25 MBps
- High Speed DDR:

- 3.3 V/1.8 V, 4-bit bus width, 0-50 MHz, 50 MBps
- HS200 SDR:
 - 1.8 V, 0-200 MHz, 4-bit bus width, 100 MBps

Secure Digital Card Support:

- Backward compatible with earlier SD card specifications
- SD Physical Layer Specification v3.01
- SDIO support
- SDIO Specification v3.00
- High Voltage SD memory card – 3.3 V
- Default Speed mode: 3.3 V signaling, frequency up to 25 MHz, up to 12.5 MBps
- High Speed mode: 3.3 V signaling, frequency up to 50 MHz, up to 25 MBps
- SDR12: UHS-I 1.8 V signaling, frequency up to 25 MHz, up to 12.5 MBps
- SDR25: UHS-I 1.8 V signaling, frequency up to 50 MHz, up to 25 MBps
- SDR50: UHS-I 1.8 V signaling, frequency up to 100 MHz, up to 50 MBps
- SDR104: UHS-I 1.8 V signaling, frequency up to 200 MHz, up to 100 MBps
- DDR50: UHS-I 1.8 V signaling, frequency up to 50 MHz, up to 50 MBps

MMCSD Not Supported Features:

MMCSD0 Host Controller:

- MultiMedia Card:
 - 3.0 V and 1.2 V
 - HS400 DDR: 1.8 V, 0-200 MHz, 8-bit bus width, 400 MBps
- Secure Digital Card
 - UHS II

MMCSD1 Host Controller:

- MultiMedia Card
 - 3.0 V and 1.2 V
 - All 8-bit modes
- Secure Digital Card
 - UHS II

For more information, see section *Multimedia Card/Secure Digital (MMC/SD) Interface* in the device TRM.

6.4.5.21 OSPI

The Octal Serial Peripheral Interface (OSPI™) module is a kind of Serial Peripheral Interface (SPI) module which allows single, dual, quad or octal read and write access to external flash devices.

The OSPI module is used to transfer data, either in a memory mapped direct mode (for example a processor wishing to execute code directly from external flash memory), or in an indirect mode where the module is set-up to silently perform some requested operation, signaling its completion via interrupts or status registers. For indirect operations, data is transferred between system memory and external flash memory via an internal SRAM which is loaded for writes and unloaded for reads by a device master at low latency system speeds. Interrupts or status registers are used to identify the specific times at which this SRAM should be accessed using user programmable configuration registers.

The OSPI modules have the following features:

- Support for single, dual, quad (QSPI mode) or octal (on MCU_FSS0_OSPI0 only) I/O instructions.
- Support dual Quad-SPI mode for fast boot applications.
- Memory mapped 'direct' mode of operation for performing flash data transfers and executing code from flash memory.

- Software triggered 'indirect' mode of operation for performing low latency and non-processor intensive flash data transfers.
- Local SRAM of configurable size to reduce advanced high-performance bus overhead and buffer flash data during indirect transfers.
- Set of software advanced peripheral bus accessible flash control registers to perform any flash command, including data transfers up to 8-bytes at a time.
- Additional addressable memory bank to accommodate more than 8-bytes at a time.
- Support for XIP, sometimes referred to as continuous mode.
- Support for DDR Mode and DTR protocol (including Octal DDR protocol with DQS for Octal-SPI devices)
- Programmable device sizes.
- Programmable write protected regions to block system writes from taking effect.
- Programmable delays between transactions.
- Legacy mode allowing software direct access to low level transmit and receive FIFOs, bypassing the higher layer processes.
- An independent reference clock to decouple bus clock from SPI clock – allows slow system clocks.
- Programmable baud rate generator to generate OSPI clocks.
- Features included to improve high speed read data capture mechanism.
- Option to use adapted clocks or DQS to further improve read data capturing.
- Programmable interrupt generation.
- Up to four external device selects - OSPI and QSPI devices can be mixed:
 - MCU_FSS0_OSPI0 has four chip-selects
 - MCU_FSS0_OSPI1 has two chip-selects.
- Programmable data decoder, enables continuous addressing mode for each of the connected devices and auto-detection of boundaries between devices.
- Support BOOT mode.
- Support for data safety mechanisms:
 - Bidirectional CRC on Multiple-SPI interface.
 - Handling ECC errors for flash devices with embedded correction engine.
- Full integration with PHY module dedicated to more flexible and power efficient transfers.

The following features are not supported on this family of devices:

- OSPI1_D[7-4] are not pinned out.
- OSPI1_SCn[3-2] are not pinned out.
- DMA not supported.
- Pulse events not used.
- In Octal-SPI mode, Mode 1 and 2 are not supported. In Mode 3 DDR is not supported.
- In Quad-SPI mode, Mode 1 and 2 are not supported. In Mode 3 DDR is not supported.

For more information, see section *Octal Serial Peripheral Interface (OSPI)* in the device TRM.

6.4.5.22 PCIE

The Peripheral Component Interconnect Express (PCIe) subsystem is built around a multi-lane dual-mode PCIe controller that provides low pin-count, high reliability, and high-speed data transfers at rates of up to 8.0 Gbps per lane for serial links on backplanes and printed wiring boards.

The device includes two instantiations of PCIe subsystem named PCIE0 and PCIE1.

Each PCIe subsystem supports the following main features:

- Compliant with PCI-Express® Base Specification, Revision 3.1

- One or two-lane configuration with up to 8.0 Gbps/lane (Gen3)
 - PCIe0 used as 2-lane controller, configurable in 1x1 or 1x2 mode
 - PCIe1 used as 1-lane controller configured in 1x1 mode
- Gen3 (8 Gbps 128/130-bit encoding), Gen2 (5 Gbps 8/10-bit encoding), and Gen1 (2.5 Gbps 8/10-bit encoding) with auto-negotiation
- Dynamic PIPE width change when switching between Gen1/2/3 modes
- Root Complex (RC) or End Point (EP) operation modes
- Maximum payload size of 256 bytes
- Maximum remote read request size of 4K bytes
- Ultra-low transmit and receive latency
- Automatic lane reversal as specified in the PCIe specification (transmit and receive)
- Polarity inversion on receive
- One Physical Function (PF)
- Single function in End Point (EP) mode
- Four virtual channels (VC)
- Four traffic classes (TC)
- Automatic credit management
- ECRC generation and checking
- PCI Device Power Management states D0, D1, D3Hot and D3Cold with the exception of D3Cold with Vaux
- PCIe Active State Power Management (ASPM) state L0s and L1 (with exceptions)
- PCIe Link Power Management states, except L2 state
- PCIe Advanced Error Reporting
- PCIe messages for both transmit and receive
- Filtering for Posted, Non-posted, and Completion traffic
- Configurable BAR filtering, I/O filtering, configuration filtering, and completion lookup/timeout
- Access to configuration space registers and external application memory-mapped registers through BAR0 and through configuration access
- Legacy interrupts reception (in RC mode) and generation (in EP mode)
- Custom interrupt generation in RC mode and interrupt reception in EP mode.
- MSI-X generation and reception
- Precision Time Measurement (PTM) in combination with internal Common Platform Time Sync (CPTS) module
- Quality-of-Service (QoS) mechanism by enabling priority or round-robin arbitration on VCs
- Two host bus master interfaces for high and low priority traffic mapped to four virtual channels
- PCIe compliant PHY (PIPE 4.0) interface for connection to a SERDES based PHY

The PCIe subsystems do not support the following features:

- PCIe beacon for in-band wake
- Vendor Messaging
- I/O access in inbound direction in RC or EP mode
- Single-root I/O Virtualization (SR-IOV)
- Address Translation Services (ATS)
- Addressing modes other than incremental for burst transactions. As a result, the PCIe addresses cannot be in cacheable memory space.

For more information, see section *Peripheral Component Interconnect Express (PCIe) Subsystem* in the device TRM.

6.4.5.23 SerDes

SerDes'es goal is to convert device (SoC) parallel data into serialized data that can be output over a high-speed electrical interface. In the opposite direction, SerDes converts high-speed serial data into parallel data that can be processed by the device. To this end, the SerDes contains a variety of functional blocks to handle both the external analog interface as well as the internal digital logic.

Most important building blocks of SerDes are:

- Lanes: The lanes handle all inputs and outputs from the serial interface, and contain the Tx/Rx I/Os, serializer/deserializer, and Clock and Data Recovery (CDR) unit.
- Clock Multiplier Unit (CMU): The CMU handles peripheral and Tx clocking of the SerDes. It consists of an internal PLL and the reference clock input buffers.
- Physical Coding Sub-block (PCS): The PCS is responsible for translating data from/to the parallel interface, as well as data encoding/decoding and symbol alignment.
- WIZ: The WIZ acts as a wrapper for the SerDes, and can both send control signals to and report status signals from the SerDes, and muxes SerDes to peripherals.

The device contains two SerDeses: SERDES0 and SERDES1.

The SERDES module features include:

- Single lane PHY containing:
 - Transmit and Receive I/Os
 - Serializer
 - Deserializer
 - Clock and data recovery (CDR) unit
- Clock Multiplying Unit (CMU)
 - PLLs
 - Master bias
 - Termination calibration
 - Reference clock input buffers
- Physical Coding Sub-block (PCS)
 - 8b/10b encoder/decoder (PCIe 1 and PCIe 2)
 - 128b/130b encoder/decoder (PCIe 3)
 - Symbol alignment
 - Polarity inversion
 - Bit stream reordering
- Physical Media Attachment (PMA) layer
 - Transmit equalization
 - Receive equalization

The SERDES mux (WIZ) module supports the following features:

- Multiplexes device interfaces onto a single SERDES lane (one Tx and one Rx)
- Provides registers to implement SERDES control and status functions and alignment delays
- Clock generator block for providing MAC transmit clock
- Rx comma align block
 - Performs de-stuffing the Rx data stream in the event that the Rx rate is different from the Tx rate
 - Supports comma detection that is not sensitive to false commas using all 8B10B character combinations

For more information, see section *Serializer/Deserializer (SerDes)* in the device TRM.

6.4.5.24 RTI

This section describes the Real Time Interrupt (RTI) modules with Windowed Watchdog Timer (WWDT) functionality for the device.

The Real Time Interrupt module provides timer functionality for operating systems and for benchmarking code. The module incorporates several counters, which define the timebases needed for scheduling in the operating system.

This module is specifically designed to fulfill the requirements for OSEK (“Offene Systeme und deren Schnittstellen für die Elektronik im Kraftfahrzeug”; “Open Systems and the Corresponding Interfaces for Automotive Electronics”) as well as OSEK/Time compliant operating systems.

The timers also provide the ability to benchmark certain areas of code by reading the counter contents at the beginning and the end of the desired code range and calculating the difference between the values.

The RTI modules include the following main features:

- Two independent 64 bit counter blocks (counter block0 or counter block1). Each block consists of
 - One 32 bit up counter
 - One 32 bit free running counter
 - Two capture registers for capturing the prescale and free running counter on a special event.
- Free running counter 0 can be incremented by either the internal prescale counter or by an external event.
- Four configurable compare registers for generating operating system ticks. Each event can be driven by either counter block0 or counter block1.
- Fast enabling/disabling of events.
- Capture events to capture timestamps through recording of timer status.
- Two time-stamp (capture) functions for system or peripheral interrupts, one for each counter block.
- Windowed watchdog timer (WWDT) feature.
- RTI clock input derived from any of the available clock sources, selectable in the System Module
- Optional capability to drive a pulse-width modulated signal out on an interrupt line

The following features are not supported on this family of devices:

- RTI[3-0] are not supported in PG1.0
- Analog and Digital Watchdog (DWD) Timers
- Periodic interrupt / DMA events
- Compare events not used
- Counter operation is not supported and counter overflow interrupts are not used.

For more information, see section *Real Time Interrupt (RTI) Module* in the device TRM.

6.4.5.25 Timers

There are sixteen timer modules in the device.

All timers include specific functions to generate accurate tick interrupts to the operating system.

Each timer can be clocked from several different independent clocks. The selection of clock source is made from registers in the MCU_CTRL_MMR0/CTRL_MMR0.

In the MCU domain the device provides 2 timer pins to be used as MCU Timer Capture inputs or as MCU Timer PWM outputs. In order to provide maximum flexibility, these 2 pins may be used with any of MCU_TIMER0 through MCU_TIMER3 instances. System level muxes are used to control the capture source pin for each MCU_TIMER[3-0] and the MCU_TIMER[3-0] source for each MCU_TIMER_IO[1-0] PWM output.

In the MAIN domain the device provides 8 timer pins to be used as Timer Capture inputs or as Timer PWM outputs. For maximum flexibility, these 8 pins may be used with any of TIMER0 through TIMER11 instances. System level muxes are used to control the capture source pin for each TIMER[11-0] and the TIMER[11-0] source for each TIMER_IO[7-0] PWM output.

Each odd numbered timer instance from each of the domains may be optionally cascaded with the previous even numbered timer instance from the same domain to form up to a 64-bit timer. For example, TIMER1 may be cascaded to TIMER0, MCU_TIMER1 may be cascaded to MCU_TIMER0, etc.

When cascaded, $TIMER_i$ acts as a 32-bit prescaler to $TIMER_{i+1}$, as well as MCU_TIMER_n acts as a 32-bit prescaler to MCU_TIMER_{n+1} . $TIMER_i / MCU_TIMER_n$ must be configured to generate a PWM output edge at the desired rate to increment the $TIMER_{i+1} / MCU_TIMER_{n+1}$ counter.

For more information, see section *Timers* in the device TRM.

6.4.5.26 UART

The UART is a slave peripheral that utilizes the DMA for data transfer or interrupt polling via host CPU. There are five UART modules in the device. All UART modules support IrDA and CIR modes when 48 MHz function clock is used. Each UART can be used for configuration and data exchange with a number of external peripheral devices or interprocessor communication between devices.

The UART include the following features:

- 16C750-compatible
- RS-485 external transceiver auto flow control support
- 64-byte FIFO buffer for receiver and 64-byte FIFO buffer for transmitter
- Programmable interrupt trigger levels for FIFOs
- Programmable sleep mode
- The 48 MHz functional clock is default option and allows baud rates up to 3.6 Mbps
- The 192 MHz functional clock is not default option and allows baud rates up to 12 Mbps, and auto-baud cannot be used
- Auto-baud between 1200 bits/s and 115.2 Kbits/s (only when 48 MHz function clock is used)
- Optional multi-drop transmission
- Configurable time-guard feature
- Configurable data format:
 - Data bit: 5, 6, 7, or 8 bits
 - Parity bit: Even, odd, none
 - Stop-bit: 1, 1.5, 2 bit(s)
- Flow control: Hardware (RTS/CTS) or software (XON/XOFF)
- False start bit detection
- Line break generation and detection
- Fully prioritized interrupt system controls
- Internal test and loopback capabilities
- Modem control functions (CTS, RTS)
- UART0 module in MAIN domain has extended modem control signals (DCD, RI, DTR, DSR)

The IrDA includes the following features:

- Support of IrDA 1.4 slow infrared (SIR), medium infrared (MIR), and fast infrared (FIR) communications:
 - Slow infrared (SIR 115.2 KBAUD), medium infrared (MIR 0.576 MBAUD) and fast infrared (FIR 4.0 MBAUD) operations (very fast infrared (VFIR) is not supported)
 - Frame formatting: addition of variable beginning-of-frame (xBOF) characters and end-of-frame (EOF) characters
 - Uplink/downlink cyclic redundancy check (CRC) generation/detection
 - Asynchronous transparency (automatic insertion of break character)
 - Eight-entry status FIFO (with selectable trigger levels) to monitor frame length and frame errors
 - Framing error, CRC error, illegal symbol (FIR), and abort pattern (SIR, MIR) detection

- IrDA mode when 48 MHz function clock is used

The CIR mode uses a variable pulse-width modulation (PWM) technique (based on multiples of a programmable t period) to encompass the various formats of infrared encoding for remote-control applications. The CIR logic transmits data packets based on a user-definable frame structure and packet content.

The CIR includes the following features to provide CIR support for remote-control applications:

- Transmit and receive mode
- Free data format (supports any remote-control private standards)
- Selectable bit rate
- Configurable carrier frequency
- 1/2, 5/12, 1/3, or 1/4 carrier duty cycle
- CIR mode when 48 MHz function clock is used

UART Not Supported Features:

- Synchronous mode
- ISO7816 mode

For more information, see section *Universal Synchronous/Asynchronous Receiver/Transmitter (UART)* in the device TRM.

6.4.5.27 USB

Similar to earlier versions of USB bus, USB 3.0 is a general-purpose cable bus, supporting data exchange between a host device and a wide range of simultaneously accessible peripherals.

The device supports two USB subsystems, both instantiated in the MAIN system domain:

- USB3SS0 is SuperSpeed (SS) USB 3.0 Dual-Role-Device (DRD) subsystem with integrated SS (USB3.0) PHY and HS/FS/LS (USB2.0) PHY
- USB3SS1 is HighSpeed (HS) USB 2.0 Dual-Role-Device (DRD) subsystem with integrated HS/FS/LS (USB2.0) PHY

The USB subsystem, supports the following USB features:

- General features:
 - Supports Peripheral (aka Device) mode at Superspeed (5 Gbps), Highspeed (480 Mbps), and Fullspeed (12 Mbps)
 - Supports Host mode at Superspeed (5 Gbps), Highspeed (480 Mbps), Fullspeed (12 Mbps), and Lowspeed (1.5 Mbps)
 - Static peripheral operation
 - Static host operation
 - Limited OTG 2.0 functionality in conjunction with an VBUS/ID analog comparator detection circuit and software handshake
 - Host Negotiation Protocol (HNP) support in conjunction with an ID comparator detection circuit and software handshake
 - Accessory Charger Adapter (ACA) support via ID-pin comparator
 - External Buffer Control (EBC) mode for IN (Tx) Endpoints 14 and 15

- Each controller instance contains single xHCI with the following features:
 - Compatible to the xHCI specification (revision 1.1) in Host mode
 - Supports 15 Transmit (TX), 15 Receive (RX) endpoints (EPs), and one EP0 endpoint which is bidirectional
 - Internal DMA controller
 - Interrupt moderation and blocking
 - Supports for all USB transfer modes - Control, Bulk, Interrupt, and Isochronous
 - Supports high bandwidth ISO mode
 - Descriptor caching and data pre-fetching used to improve system performance
 - Dynamic FIFO memory allocation for all endpoints
 - USB power saving states (U0, U1, U2, and U3)
 - Asynchronous wakeup signal for remote wakeup
- Operation flexibility:
 - Uniform programming model for SS, HS, FS, and LS operation
 - Multiple interrupt lines:
 - 16 interrupts associated with 16 programmable Event Rings for multi-core support
 - Interrupt lines for all miscellaneous events
- Functional safety:
 - Internal RAM with ECC
 - Loopback on USB3 PHY (SerDes)
- External requirements:
 - An external charge pump or power switch for VBUS 5-V generation
 - An external circuitry or PMIC to start the battery charging upon Battery Charger (BC) detected event
 - An external reference clock input for USB PHY operation
 - An external high-precision resistor for PHY termination calibration

The following are USB features which are not supported in current device:

- OTG 3.0 functionality
- HSIC (High Speed inter-chip) and SSIC interface
- ULPI Interface for external PHY
- SRP and ADP protocols
- External Buffer Control (EBC) for OUT (Rx) Endpoint
- Hibernation

For more information, see section *Universal Serial Bus (USB) Subsystem* in the device TRM.

6.5 Identification

6.5.1 Revision Identification

For more information about Revision Identification, see section [8.1, Device Nomenclature](#).

6.5.2 Die Identification

The device part number identification data can be read in the CTRLMMR_WKUP_JTAG_DEVICE_ID register.

For more information about Die Identification, see section *Device Identification* in the device TRM.

6.5.3 JTAG Identification

The manufacturer identity, the boundary scan part number, and the silicon revision of the device can be read in the CTRLMMR_WKUP_JTAGID register.

For more information about JTAG Identification, see section *Device Identification* in the device TRM.

6.5.4 ROM Code Identification

The ROM code uses several global memories in the MSRAM that are useful for debugging.

For more information about ROM Code Identification, see section *Global Memory Addresses Used by ROM Code* in the device TRM.

6.6 Boot Modes

6.6.1 Boot Mode List

Boot Mode pins provide means to select the boot mode before the device is powered up.

Boot mode pins can be divided into the following categories:

- **BOOTMODE[03:00]** – Select the requested boot (primary) mode after POR, that is, the peripheral/memory to boot from.
- **BOOTMODE[06:04]** – Select the backup boot mode, that is, the peripheral/memory to boot from, if primary boot device failed.
- **BOOTMODE07** – This is the minimum (MIN) configuration pin. MIN pin allows minimum BOOTMODE pins to be set up, and thus saving DIP switches or pull-ups/pull-downs on the board. A default value, stored in ROM Code, is loaded in place of BOOTMODE[18:8] pin values. See the particular boot mode section for the default values when MIN was selected.
- **BOOTMODE[15:08]** – These pins provide optional configurations for primary boot and are used in conjunction with the boot mode selected. See [6.6.2.2.1, Primary Boot Mode Configuration](#) and the corresponding boot mode section.
- **BOOTMODE[18:16]** – These pins provide optional configurations for the backup boot devices. See [6.6.2.2.2, Backup Boot Mode Configuration](#) and the corresponding boot mode section.
- **MCU_BOOTMODE[02:00]** – Denote system clock frequency (WKUP_HFOSC0) for PLL configuration.
- **MCU_BOOTMODE[04:03]** – These pins are reserved for future use.
- **MCU_BOOTMODE[08:05]** – On safety-enabled devices, these pins enable certain power-on tests (POST).
- **MCU_BOOTMODE09** – Selects which MMCSD port is connected to 1.8-V SDIO LDO.

注

It is user's responsibility to set properly the (MCU_)BOOTMODE pins (via pullups or pulldowns) depending on the desired boot scenario.

System board must provide means to switch (MCU_)BOOTMODE pin settings easily. In a field design, some pins may be hardcoded to 0 or 1 but only after careful evaluation (for example with MIN pin enabled).

For more information about Boot Mode List, see section *Boot Mode Pins* in the device TRM.

6.6.2 Boot Mode Pin Usage

6.6.2.1 MCU_BOOTMODE Pin Mapping

MCU_BOOTMODE pin mapping is shown in [表 6-1, MCU_BOOTMODE Pin Mapping](#).

表 6-1. MCU_BOOTMODE Pin Mapping

9	8	7	6	5	4	3	2	1	0
---	---	---	---	---	---	---	---	---	---

表 6-1. MCU_BOOTMODE Pin Mapping (continued)

1.8V MMC/SD	POST ⁽¹⁾	Reserved ⁽²⁾	Ref Clock
----------------	---------------------	-------------------------	-----------

(1) Only on safety-enabled devices. Refer to device Datasheet for device nomenclature.

(2) Always set to 0s (via pull-downs to VSS)

The ROM Code will configure any PLLs required during the boot process. The ROM Code does not have the ability to select HFOSC1 (in main domain) during initial boot, however the selection can be done through the boot certificate.

The ROM Code has no means to detect the system clock speed, therefore user must set the Ref Clock pins according to the actual clock speed in the design (generated by PMIC, internal or external XTAL oscillator, or other). Ref Clock pins are described in 表 6-2, *PLL Reference Clock Selection*.

表 6-2. PLL Reference Clock Selection

MCU_BOOTMODE PINS			REFERENCE CLOCK (MHz)
2	1	0	
0	0	0	19.2
0	0	1	20
0	1	0	24
0	1	1	25
1	0	0	26
1	0	1	27
1	1	0	Reserved
1	1	1	No PLL configuration (slow speed backup)

On safety-enabled devices, users can select certain POST tests to be performed on power-on. POST tests are executed in hardware, without any ROM code intervention. More than one test can be selected at a time. 表 6-3 shows the POST selection.

表 6-3. POST Selection

MCU_BOOTMODE PINS				POST SELECT
8	7	6	5	
0	0	0	0	POST bypass
X	X	X	1	Enable POST DMSC, MCU LBIST Parallel
X	X	1	X	POST DMSC LBIST Enable
X	1	X	X	POST MCU LBIST Enable
1	X	X	X	POST PBIST Enable

表 6-4. 1.8V LDO Configuration

9	1.8V MMC/SD
0	MMCS0D0 connected to 1.8V LDO
1	MMCS0D1 connected to 1.8V LDO

For more information about MCU_BOOTMODE Pin Mapping, see *MCU_BOOTMODE Pin Mapping* in the device TRM.

6.6.2.2 BOOTMODE Pin Mapping

In normal boot operation the ROM execution is directed through the main boot mode pins. Main boot mode pins are shown in 表 6-5, *BOOTMODE Pin Mapping*.

表 6-5. BOOTMODE Pin Mapping

18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Backup Config			Primary Config								Min	Backup Mode			Primary Mode			

6.6.2.2.1 Primary Boot Mode Configuration

The mapping of primary boot mode configuration pins is shown in 表 6-6, *Primary Boot Mode Configuration*.

表 6-6. Primary Boot Mode Configuration⁽¹⁾

BOOTMODE PINS									BOOT MODE
15	14	13	12	11	10	9	8	3-0	
								0000	Sleep
Pin Cmd		Iclk	Csel		Speed		Addr Width	0001	OSPI
Port	Pin Cmd	Iclk	Csel		Speed		Addr Width	0010	QSPI
			ns	Csel		Speed		0011	Hyperflash
Port	Mode		Csel		Read Cmd	Addr Width		0100	SPI
		Bus Reset		Mode	Speed	Addr		0101	I2C
		Volt	Port	Interface Config			1bit	0110	MMC/SD Card
Clken	Clkf	Interface		Speed	Duplex	Extern conf		0111	Ethernet
					Mode		Port	1000	USB
Port	Dual	Sref						1001	PCIe
								1010	UART
Base	A/D mux		Csel Size		Csel		Bus Width	1100	GPMC NOR
	Port	Alt	Bus Width		Speed		Ack	1101	eMMC

(1) Shaded cells are do not cares and pins can take any value.

6.6.2.2.2 Backup Boot Mode Configuration

The mapping of backup boot mode configuration pins is shown in 表 6-7, *Backup Boot Mode Configuration*.

表 6-7. Backup Boot Mode Configuration⁽¹⁾

BOOTMODE PINS				BACKUP BOOT MODE
18	17	16	6-4	
			000	None
Mode		Port	001	USB
			010	UART
Clkout	Interface		011	Ethernet
Volt	Port	1bit	100	MMC/SD
Port	Addr Width/Cmd		101	SPI
Csel	Speed		110	Hyperflash
Bus Reset	Mode	Addr	111	I2C

(1) Shaded cells are do not cares and pins can take any value.

For more information about BOOTMODE Pin Mapping, see *BOOTMODE Pin Mapping* in the device TRM.

6.6.3 Boot Mode Selection

6.6.3.1 Primary Boot Mode Selection

The primary boot mode is the first mode attempted after reset. 表 6-8, *Primary Boot Mode Selection* lists all possible primary boot modes.

表 6-8. Primary Boot Mode Selection

BOOTMODE PINS				PRIMARY BOOT MODE SELECTED
3	2	1	0	
0	0	0	0	Sleep (No boot – debug mode)
0	0	0	1	OSPI
0	0	1	0	QSPI
0	0	1	1	Hyperflash
0	1	0	0	SPI (on QSPI/OSPI port 0 in legacy SPI mode)
0	1	0	1	I2C
0	1	1	0	MMC/SD card, eMMC boot from UDA or file system
0	1	1	1	Ethernet
1	0	0	0	USB
1	0	0	1	PCIe
1	0	1	0	UART
1	0	1	1	Reserved
1	1	0	0	GPMC NOR
1	1	0	1	eMMC boot from boot partition (with auto-fall back to file system)
1	1	1	0	Reserved (acts as Sleep)
1	1	1	1	Reserved (acts as Sleep)

6.6.3.2 Backup Boot Mode Selection

The backup boot mode is attempted if the primary boot mode fails. Note that if the primary boot device is a flash device the primary boot mode will be re-tried at multiple different flash addresses before falling to the backup boot mode. 表 6-9, *Backup Mode Selection* lists all possible backup boot modes.

表 6-9. Backup Mode Selection

BOOTMODE PINS			BACKUP BOOT MODE SELECTED
6	5	4	
0	0	0	None (no backup boot will be attempted)
0	0	1	USB
0	1	0	UART
0	1	1	Ethernet
1	0	0	MMC/SD
1	0	1	SPI (on OSPI port 0 in legacy SPI mode)
1	1	0	Hyperflash
1	1	1	I2C

6.6.3.3 Min Pin

The *min* (minimal boot config) pin is provided as a way to use minimal pin count to configure boot. When the min pin value is 1, all configuration fields are based on pre-defined default values. In this case, no configuration pins (BOOTMODE[18:8]) need to be driven since their values are ignored.

表 6-10. Min Pin Configuration

BOOTMODE PINS	MINIMAL PIN CONFIGURATION
7	
0	All boot mode pins must be properly set
1	Certain boot mode pins are do not cares. ROM code uses built-in values instead.

For more information about Boot Mode Selection, see *BOOTMODE Pin Mapping* in the device TRM.

7 Applications, Implementation, and Layout

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test design implementation to confirm system functionality.

7.1 DDR Board Design and Layout Guidelines

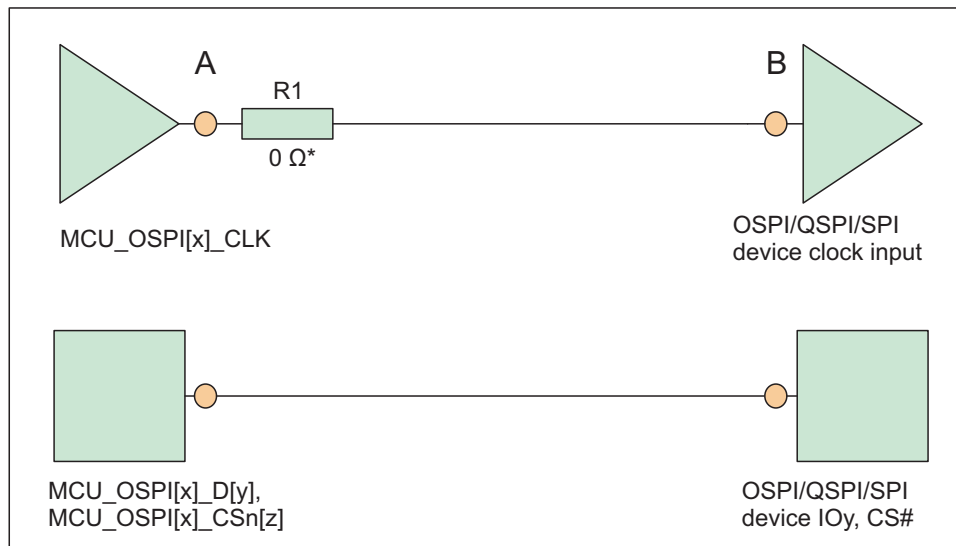
The goal of the [AM65x/DRA80xM DDR Board Design and Layout Guidelines](#) is to make the DDR3L, DDR4, and LPDDR4 system implementation straightforward for all designers. Requirements have been distilled down to a set of layout and routing rules that allow designers to successfully implement a robust design for the topologies that TI supports. TI only supports board designs using DDR3L, DDR4, and LPDDR4 memories that follow the guidelines in this document.

7.2 OSPI Board Design and Layout Guidelines

The following section details the routing guidelines that must be observed when routing the OSPI interfaces.

7.2.1 No Loopback & Internal Pad Loopback

- The MCU_OSPI[x]_CLK output signal must be connected to the CLK pin of the flash device
- The signal propagation delay from the MCU_OSPI[x]_CLK signal to the flash device must be < 450ps (~7cm as stripline or ~8cm as microstrip)
- 50 Ω PCB routing is recommended along with series terminations, as shown in [Figure 7-1](#)
- Propagation delays and matching:
 - A to B < 450ps
 - Matching skew: < 60pS



OSPI_Board_01

*0 Ω resistor (R1), located as close as possible to the MCU_OSPI[x]_CLK pin, is placeholder for fine tuning, if needed

Figure 7-1. OSPI Interface High Level Schematic

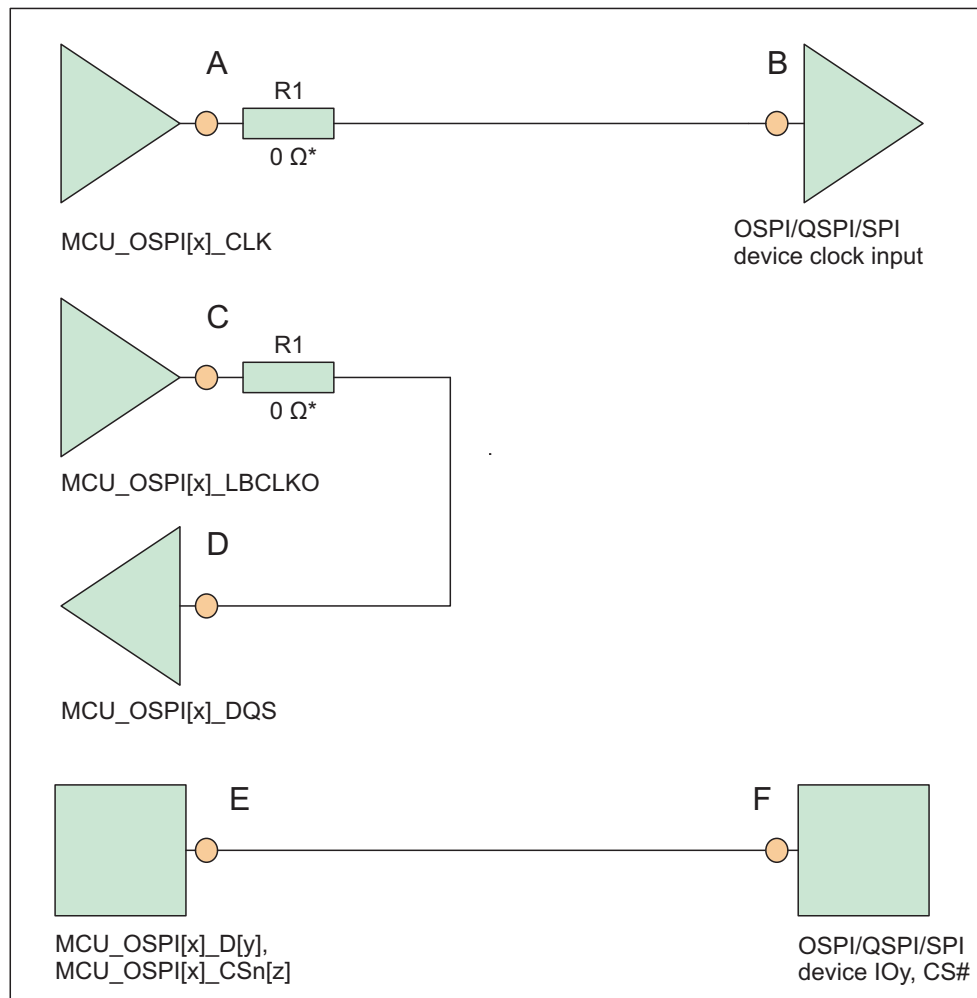
7.2.2 External Board Loopback

- The MCU_OSPI[x]_CLK output signal must be connected to the CLK pin of the flash device
- The MCU_OSPI[x]_LBCLKO output signal must be looped back into the MCU_OSPI[x]_DQS input

- The signal propagation delay from the MCU_OSPI[x]_CLK pin to the flash device CLK input pin (A to B) should be approximately equal to half of the signal propagation delay from the MCU_OSPI[x]_LBCLKO pin to the MCU_OSPI[x]_DQS pin ((C to D)/2). See the note below.
- The signal propagation delay from the MCU_OSPI[x]_CLK pin to the flash device CLK input pin (A to B) must be approximately equal to the signal propagation delay of the control and data signals between the flash device and the SoC device (E to F, or F to E)
- 50 Ω PCB routing is recommended along with series terminations, as shown in 7-2
- Propagation delays and matching:
 - A to B = E to F = (C to D) / 2
 - Matching skew: < 60pS

注

The OSPI Board Loopback Hold time requirement (described in 5.9.5.18, OSPI) is larger than the Hold time provided by a typical flash device. Therefore, the length of MCU_OSPI[x]_LBCLKO pin to the MCU_OSPI[x]_DQS pin (C to D) may need to be shortened to compensate.

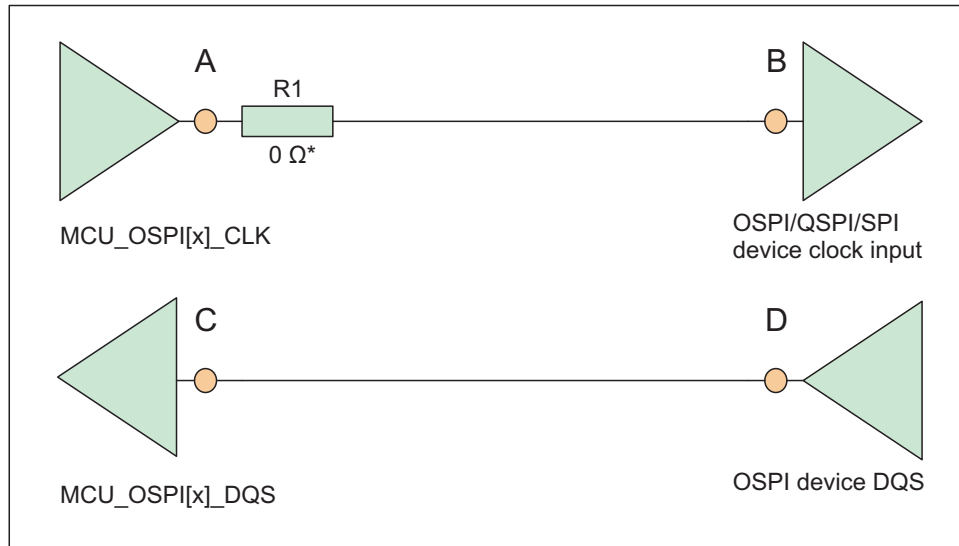


*0 Ω resistor (R1), located as close as possible to the MCU_OSPI[x]_CLK and MCU_OSPI[x]_LBCLKO pins, is placeholder for fine tuning, if needed

7-2. OSPI Interface High Level Schematic

7.2.3 DQS (only available in Octal Flash devices)

- The MCU_OSPI[x]_CLK output signal must be connected to the CLK pin of the flash device
- The DQS pin of the flash devices must be connected to MCU_OSPI[x]_DQS signal
- The signal propagation delay from the MCU_OSPI[x]_CLK pin to the flash device CLK input pin (A to B) should be approximately equal to the signal propagation delay from the MCU_OSPI[x]_DQS pin to the DQS output pin (C to D)
- 50 Ω PCB routing is recommended along with series terminations, as shown in [Figure 7-3](#)
- Propagation delays and matching:
 - A to B = C to D
 - Matching skew: < 60pS



*0 Ω resistor (R1), located as close as possible to the MCU_OSPI[x]_CLK pin, is placeholder for fine tuning, if needed

Figure 7-3. OSPI Interface High Level Schematic

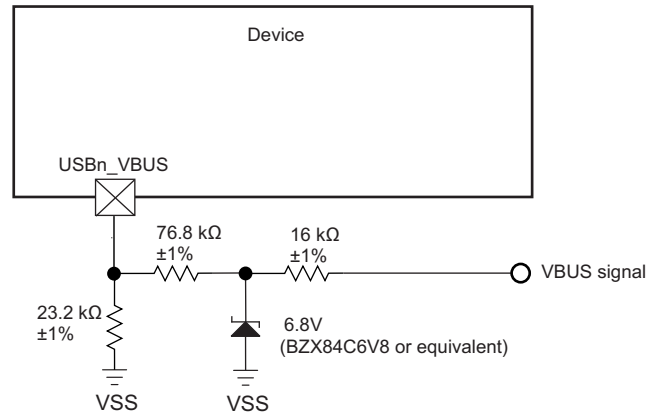
7.3 High Speed Differential Signal Routing Guidance

The [High-Speed Interface Layout Guidelines](#) provides guidance for successful routing of the high speed differential signals. This includes PCB stackup and materials guidance as well as routing skew, length and spacing limits. TI supports *only* designs that follow the board design guidelines contained in the application report.

7.4 USB Design Guidelines

The USB 3.1 specification allows the VBUS voltage to be as high as 5.5 V for normal operation, and as high as 20 V when the Power Delivery addendum is supported. Some automotive applications require a max voltage to be 30 V.

The AM65xx device requires the VBUS signal voltage be scaled down using an external resistor divider (as shown in the [Figure 7-4](#)), which limits the voltage applied to the actual device pin (USB0_VBUS, USB1_VBUS). The tolerance of these external resistors should be equal to or less than 1%, and the leakage current of zener diode at 5 V should be less than 100 nA.



SPRSP08_USB_VBUS_01

FIG 7-4. USB VBUS Detect Voltage Divider / Clamp Circuit⁽¹⁾

(1) USBn_VBUS, where n = 0 or 1.

The USB0_VBUS and USB1_VBUS pins may be considered to be fail-safe because the external circuit in FIG 7-4 limits the input current to the actual device pin in a case where VBUS is applied while the device is powered off.

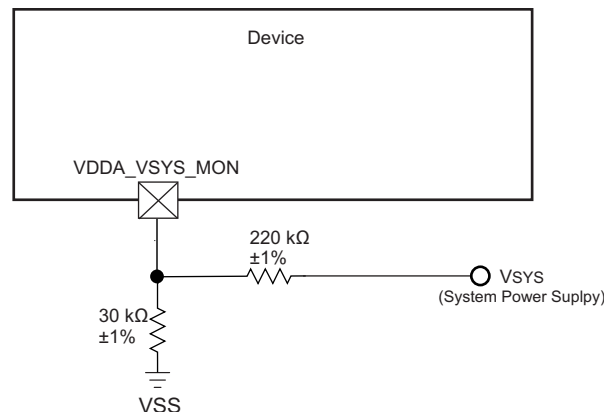
7.5 System Power Supply Monitor Design Guidelines

The VDDA_VSYS_MON pin provides a way to monitor the system power supply and is not fail-safe, unless implemented with the appropriate resistor voltage divider source. This pin should be sourced with a resistor voltage divider that receives its power from the system power supply.

The output of the resistor voltage divider is connected to the VDDA_VSYS_MON pin which has a trigger voltage of $0.5 \text{ V} \pm 5\%$. The resistor voltage divider should be implemented such that it has a reference current in the range of $1 \mu\text{A}$ to $50 \mu\text{A}$, output voltage that never exceeds the maximum value defined in Section 5.1, *Absolute Maximums Ratings*, and output voltage of 0.54 V when the system supply drops to its lowest desired operating voltage.

The recommended output voltage of 0.54 V provides 40 mV of margin that includes 5% for tolerance of the voltage monitor, 1% for tolerance of each resistor, plus 5 mV of potential error introduced by input leakage current. This value ensures the voltage monitor will never trigger before reaching the expected trigger voltage.

FIG 7-5 presents an example, when the system power supply voltage is nominally 5 V and the desired trigger threshold is -10% or 4.5 V .



SPRSP08_VSYS_MON_01

FIG 7-5. System Supply Monitor Voltage Divider Circuit

In this example the voltage divider ratio should be $(4.5 \text{ V} / 0.54 \text{ V}) = 8.33$. This ratio produces a 0.54 V potential on the VDDA_VSYS_MON pin when the system power supply is 4.5 V. In this case, the voltage monitor will trigger in the range of 3.88 V to 4.5 V. Precision 1% resistors with similar thermal coefficient are recommended for implementing the resistor voltage divider.

7.6 MMC Design Guidelines

The MMC peripheral on this device contains an integrated SDIO LDO for handling automatic voltage transitions for SD Interfaces. For details about how to connect the device pins associated with the SDIO LDO, refer to [Figure 7-10](#) through [Figure 7-12](#).

7.7 Power Distribution Network Implementation Guidance

The [Sitara™ Processor Power Distribution Networks: Implementation and Analysis](#) provides guidance for successful implementation of the power distribution network. This includes PCB stackup guidance as well as guidance for optimizing the selection and placement of the decoupling capacitors. TI supports *only* designs that follow the board design guidelines contained in the application report.

7.8 External Capacitors

[Figure 7-6](#) shows an example of the external decoupling capacitor connections.



(1) Refer to [7.8.1, LVCMOS External Capacitor Connections](#) for details about external capacitor connections for VDDSHV[2:0]_WKUP, VDDSHV[8:0], VDDSHV[2:0] WKUP, and VDDSHV[8:0].

- (2) In this Figure, the VDD_WKUP0 and VDD_WKUP1 supplies are sourced through the WKUP LDO, not an external supply.
- (3) Refer to [Figure 7-10](#) through [Figure 7-12](#) for details about external capacitor connections when using the SDIO LDO.

7.8.1 LVC MOS External Capacitor Connections

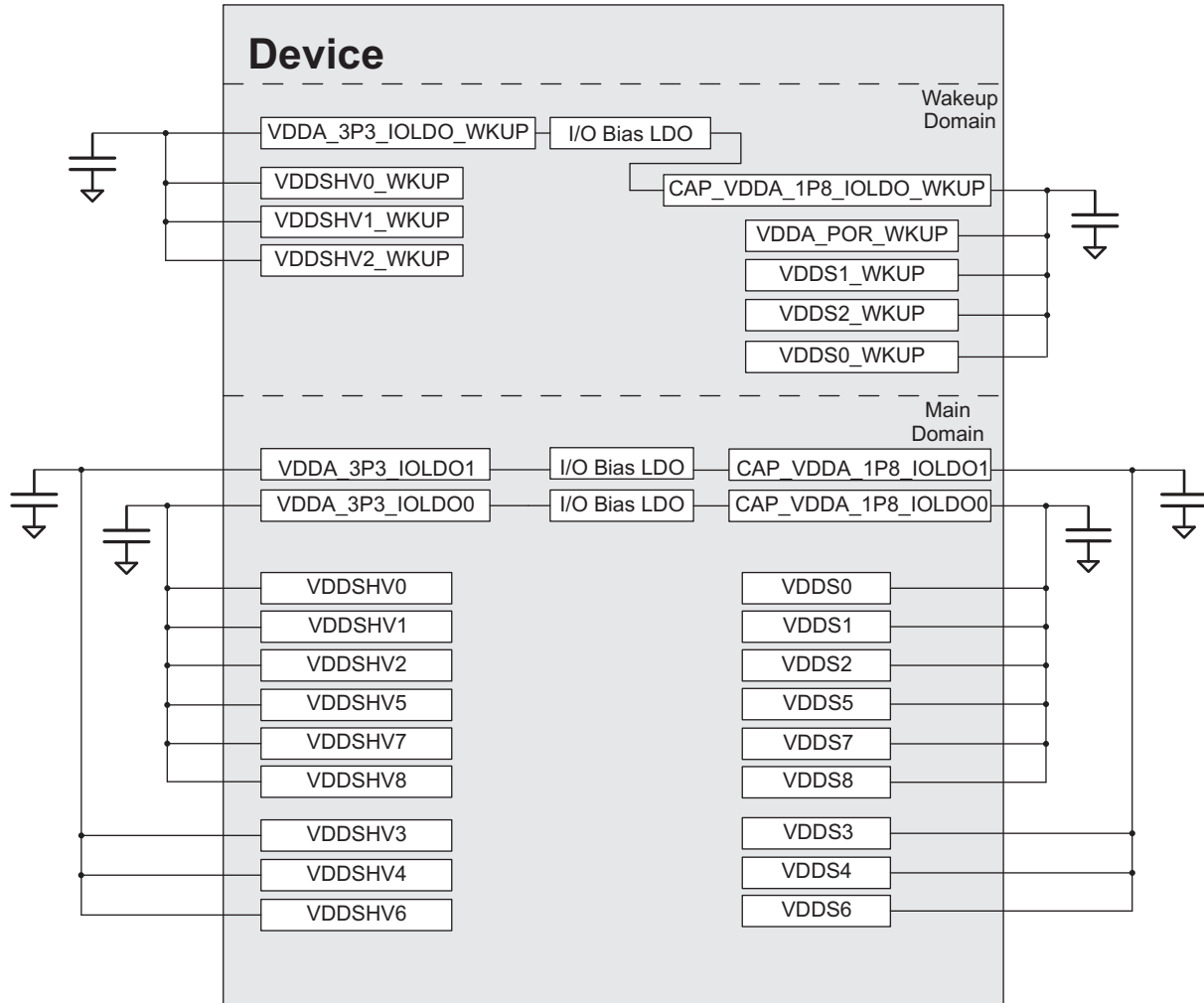
Each VDDSHV[8:0] and VDDSHV[0:2]_WKUP can be configured as 1.8 V or 3.3 V. [Figure 7-7](#) through [Figure 7-12](#) illustrate different system configurations for the dual-voltage I/O supplies.

VDDSHV[8:0] and VDDSHV[2:0]_WKUP are the dual-voltage LVC MOS I/O supplies, while VDDS[8:0] are the dual-voltage LVC MOS I/O bias supplies. If any of the VDDSHV[8:0] or VDDSHV[2:0]_WKUP are configured for 3.3 V operation, the corresponding VDDS[8:0] or VDDS[2:0]_WKUP should be sourced from the internal I/O Bias LDO. When any of the VDDSHV[8:0] or VDDSHV[2:0]_WKUP are configured for 1.8 V operation, both VDDS[8:0] and VDDSHV[8:0] or VDDS[2:0]_WKUP and VDDSHV[2:0]_WKUP should be supplied from the same source.

Two I/O Bias LDOs are integrated on this device to share load current. The recommended load sharing is as follows:

- IOLDO0 : VDDS0, VDDS1, VDDS2, VDDS5, VDDS7, VDDS8
- IOLDO1 : VDDS3, VDDS4, VDDS6

[Figure 7-7](#) shows all VDDSHV[8:0] and VDDSHV[2:0]_WKUP supplies configured for 3.3V operation.



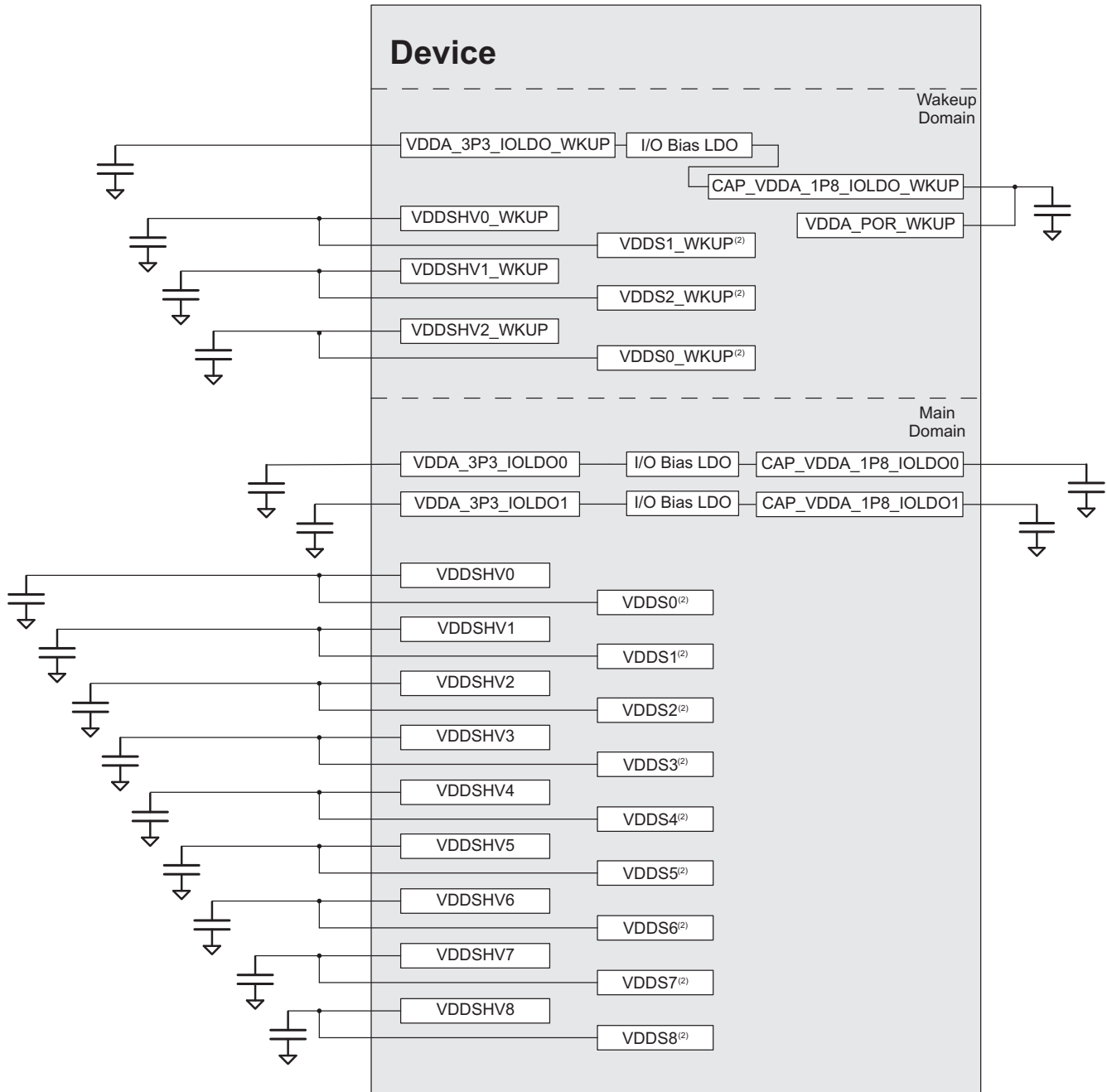
SPRSP08_DECOUPLING_CAPS_01

7-7. All VDDSHV[8:0] and VDDSHV[2:0]_WKUP supplies configured for 3.3 V operation

(1) VDDS6 and VDDS7 can be connected to SDIO LDO in some use cases. See 7-10 through 7-12 for more details.

7-8 shows all VDDSHV[8:0] and VDDSHV[2:0]_WKUP supplies configured for 1.8 V operation.

ADVANCE INFORMATION



SPRSP08_DECOUPLING_CAPS_03

7-8. All VDDSHV[8:0] and VDDSHV[2:0]_WKUP supplies configured for 1.8V operation

- (1) VDDSHV6 and VDDSHV7 can be connected to SDIO LDO in some use cases. See 7-10 through 7-12 for more details.
- (2) When any of the VDDSHV[8:0] or VDDSHV[2:0]_WKUP are configured for 1.8 V operation, the corresponding VDDSHV[8:0] or VDDSHV[2:0]_WKUP must be connected to their respective VDDSHV[8:0] or VDDSHV[2:0]_WKUP power supply.

Figure 7-9 shows a split configuration where VDDSHV[0, 1, 2, 5, 7, 8] and VDDSHV0_WKUP are configured for 3.3 V operation, while VDDSHV[3, 4, 6] and VDDSHV[2:1]_WKUP are configured for 1.8 V operation. Note the colors indicate rails that are tied to the same source.

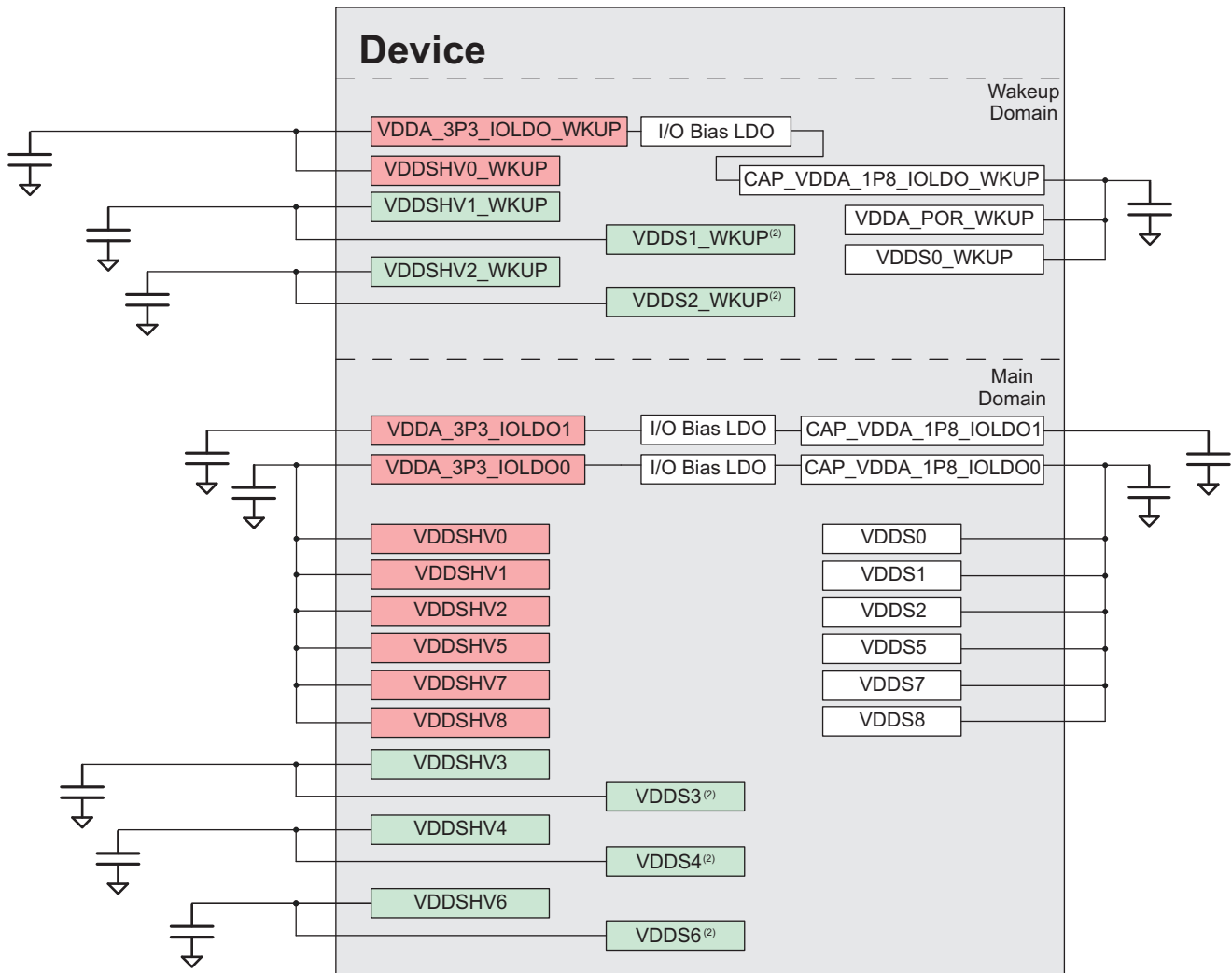
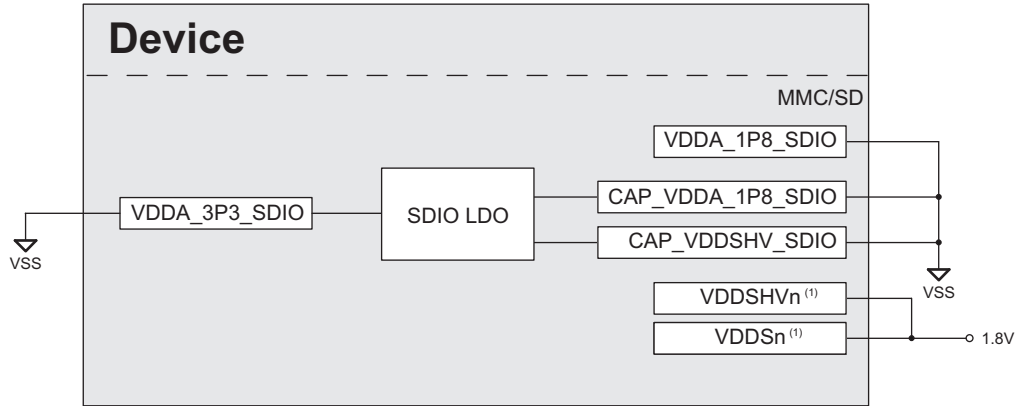


Figure 7-9. VDDSHV[8:0] and VDDSHV[2:0]_WKUP supplies configured for combination of 1.8 V or 3.3 V operation

- (1) VDDS6 and VDDS7 can be connected to SDIO LDO in some use cases. See [Figure 7-10](#) through [Figure 7-12](#) for more details.
- (2) When any of the VDDSHV[8:0] or VDDSHV[2:0]_WKUP are configured for 1.8 V operation, the corresponding VDDS[8:0] or VDDS[2:0] WKUP must be connected to their respective VDDSHV[8:0] or VDDSHV[2:0] WKUP power supply.

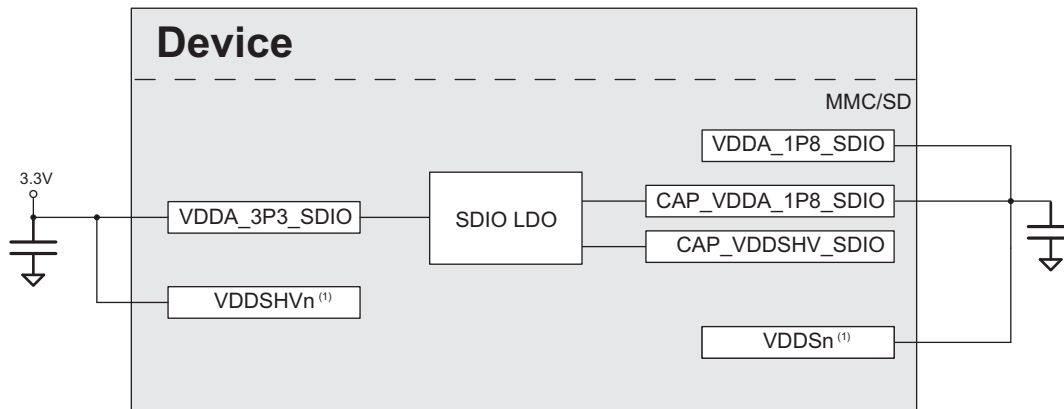
Figure 7-10 through Figure 7-12 illustrate the system configuration when VDDSHV6 or VDDSHV7 is used as the MMC/SD supply.



SPRSP08_DECOUPLING_CAPS_06

Figure 7-10. VDDSHV6 or VDDSHV7 used as the MMC/SD supply for fixed 1.8V IO

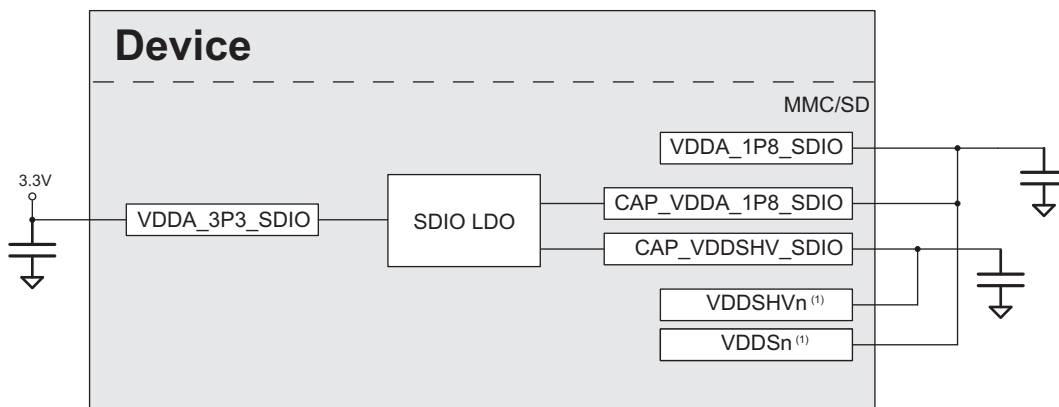
- (1) VDDSHVn and VDDSn, where n = 6 or 7.
- (2) VDDA_1P8_SDIO, CAP_VDDA_1P8_SDIO, CAP_VDDSHV_SDIO, and VDDA_3P3_SDIO must be connected to VSS, when SDIO_LDO is not used with either MMC0 or MMC1.



SPRSP08_DECOUPLING_CAPS_07

Figure 7-11. VDDSHV6 or VDDSHV7 used as the MMC/SD supply for fixed 3.3V IO

- (1) VDDSHVn and VDDSn, where n = 6 or 7.



SPRSP08_DECOUPLING_CAPS_05

Figure 7-12. VDDSHV6 or VDDSHV7 used as the MMC/SD supply for dynamic 3.3V/1.8V IO

- (1) VDDSHVn and VDDSn, where n = 6 or 7.

7.9 Thermal Solution Guidance

The [Thermal Design Guide for DSP and ARM Application Processors](#) provides guidance for successful implementation of a thermal solution for system designs containing this device. This document provides background information on common terms and methods related to thermal solutions. TI only supports designs that follow system design guidelines contained in the application report.

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all microprocessors (MPUs) and support tools. Each device has one of three prefixes: X, P, or null (no prefix) (for example, AM654x). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMDX) through fully qualified production devices and tools (TMDS).

Device development evolutionary flow:

- X** Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.
- P** Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.
- null** Production version of the silicon die that is fully qualified.

Support tool development evolutionary flow:

- TMDX** Development-support product that has not yet completed Texas Instruments internal qualification testing.
- TMDS** Fully-qualified development-support product.

X and P devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

Production devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

For orderable part numbers of AM65xx devices in the ACD package type, see the Package Option Addendum of this document, the TI website (ti.com), or contact your TI sales representative.

8.1.1 Standard Package Symbolization

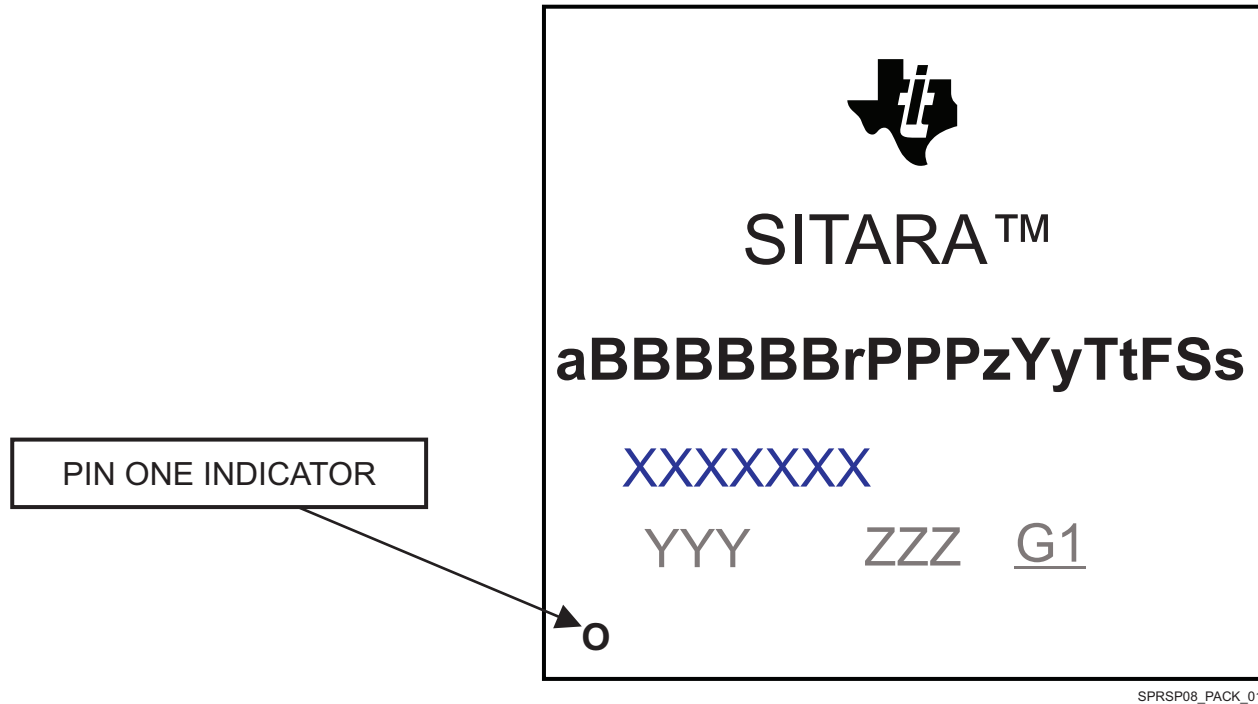


图 8-1. Printed Device Reference

8.1.2 Device Naming Convention

表 8-1. Nomenclature Description

FIELD PARAMETER	FIELD DESCRIPTION	VALUE	DESCRIPTION
a	Device evolution stage	X	Prototype
		P	Preproduction (production test flow, no reliability data)
		BLANK	Production
BBBBBB	Base production part number	AM6548	Quad Core High Tier (See 表 3-1, Device Comparison)
		AM6528	Dual Core High Tier (See 表 3-1, Device Comparison)
		AM6546	Quad Core Low Tier (See 表 3-1, Device Comparison)
		AM6526	Dual Core Low Tier (See 表 3-1, Device Comparison)
		AM6527	Dual Core Low Tier (See 表 3-1, Device Comparison)
r	Device revision	BLANK	SR 1.0
PPP	Package Designator	ACD	ACD FCBGA-N784 (23mm × 23mm) Package
z	Device Speed	X	High speed grade (see 表 5-1, Speed Grade Maximum Frequency)
		OTHER	Alternate speed grade
Yy	Device type	E	All industrial protocols enabled (basic protocols plus EtherCAT slave and POWERLINK slave)
		BLANK	Basic Industrial protocols enabled
Tt	Temperature ⁽²⁾	A	Extended (see Section 5.4, Recommended Operating Conditions)
		BLANK	Commercial (see Section 5.4, Recommended Operating Conditions)
F	Functional Safety	BLANK	No safety features
		F	Safety features enabled including lock-step MCU

表 8-1. Nomenclature Description (continued)

FIELD PARAMETER	FIELD DESCRIPTION	VALUE	DESCRIPTION
Ss	Security Identifier	S1	High-Security device, Secure Boot Supported
		SB	Dummy key High-Security device, Secure Boot Supported
		BLANK	General purpose device
XXXXXXX	Lot Trace Code (LTC)		
YYY	Production Code; For TI use only		
ZZZ	Production Code; For TI use only		
O	Pin one designator		
G1	ECAT—Green package designator		

- (1) To designate the stages in the product development cycle, TI assigns prefixes to the part numbers. These prefixes represent evolutionary stages of product development from engineering prototypes through fully qualified production devices. Prototype devices are shipped against the following disclaimer:
 "This product is still in development and is intended for internal evaluation purposes."
 Notwithstanding any provision to the contrary, TI makes no warranty expressed, implied, or statutory, including any implied warranty of merchantability of fitness for a specific purpose, of this device.
- (2) Applies to device max junction temperature.

注

X6580ACD is a prototype part that is functionally equivalent to XAM6548ACDXEAF.

注

BLANK in the symbol or part number is collapsed so there are no gaps between characters.

8.2 Tools and Software

The following products support development for AM65xx platforms:

Design kits and evaluation modules

AM65x evaluation module The AM65x Evaluation Module provides a platform to quickly start evaluation of Sitara™ Arm® Cortex®-A53 AM65x Processors (AM6548, AM6546, AM6528, AM6527, AM6526) and accelerate development for HMI, networking, patient monitoring, and other industrial applications. It is a development platform based on the quad core Cortex-A53, dual Cortex-R5F processor that is integrated with ample connectivity such as PCIe, USB 3.0/2.0, Gigabit Ethernet, and more.

Development tools

Clock Tree Tool for Sitara, Automotive, Vision Analytics, & Digital Signal Processors The Clock Tree Tool (CTT) for Sitara™ ARM®, Automotive, and Digital Signal Processors is an interactive clock tree configuration software that provides information about the clocks and modules in these TI devices. It allows the user to:

- Visualize the device clock tree
- Interact with clock tree elements and view the effect on PRCM registers
- Interact with the PRCM registers and view the effect on the device clock tree
- View a trace of all the device registers affected by the user interaction with clock tree

Code Composer Studio (CCS) Integrated Development Environment (IDE) for Sitara ARM Processors

Code Composer Studio is an integrated development environment (IDE) that supports TI's Microcontroller and Embedded Processors portfolio. Code Composer Studio comprises a suite of tools used to develop and debug embedded applications. It includes an optimizing C/C++ compiler, source code editor, project build environment, debugger, profiler, and many other features. The intuitive IDE provides a single user interface taking you through each step of the application development flow. Familiar tools and interfaces allow users to get started faster than ever before. Code Composer Studio combines the advantages of the Eclipse software framework with advanced embedded debug capabilities from TI resulting in

a compelling feature-rich development environment for embedded developers.

Pin mux tool The Pin MUX Utility is a software tool which provides a Graphical User Interface for configuring pin multiplexing settings, resolving conflicts and specifying I/O cell characteristics for TI MPUs. Results are output as C header/code files that can be imported into software development kits (SDKs) or used to configure customer's custom software. Version 4 of the Pin Mux utility adds the capability of automatically selecting a mux configuration that satisfies the entered requirements.

Models

AM654x/DRA80xM BSDL Model BSDL Model

AM654x/DRA80xM IBIS File IBIS Model

AM654x/DRA80xM Thermal Models Thermal Model

For a complete listing of development-support tools for the processor platform, visit the Texas Instruments website at ti.com. For information on pricing and availability, contact the nearest TI field sales office or authorized distributor.

8.3 Documentation Support

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

The following documents describe the AM65xx devices.

Technical Reference Manual

AM65x/DRA80xM Processors

Details the integration, the environment, the functional description, and the programming models for each peripheral and subsystem in the AM65xx family of devices.

Errata

AM65x/DRA80xM Processors Silicon Revision 1.0

Describes the known exceptions to the functional specifications for the device.

8.4 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 8-2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
AM6548	Click here	Click here	Click here	Click here	Click here
AM6528	Click here	Click here	Click here	Click here	Click here
AM6546	Click here	Click here	Click here	Click here	Click here
AM6526	Click here	Click here	Click here	Click here	Click here
AM6527	Click here	Click here	Click here	Click here	Click here

8.5 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community The TI engineer-to-engineer (E2E) community was created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

TI Embedded Processors Wiki Established to help developers get started with Embedded Processors

from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

8.6 商標

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8.7 静電気放電に関する注意事項



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8.8 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

9 Mechanical, Packaging, and Orderable Information

9.1 Packaging Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AM6526BACDXA	ACTIVE	FCCSP	ACD	784	60	RoHS & Green	Call TI	Level-3-250C-168 HR	-40 to 105	AM6526BACDXA 900 900 ACD	Samples
AM6526BACDXEAF	ACTIVE	FCCSP	ACD	784	60	RoHS & Green	Call TI	Level-3-250C-168 HR	-40 to 105	AM6526BACDXEAF 900 900 ACD	Samples
AM6528BACDXEA	ACTIVE	FCCSP	ACD	784	60	RoHS & Green	Call TI	Level-3-250C-168 HR	-40 to 105	AM6528BACDXEA 900 900 ACD	Samples
AM6546BACDXA	ACTIVE	FCCSP	ACD	784	60	RoHS & Green	Call TI	Level-3-250C-168 HR	-40 to 105	AM6546BACDXA 900 900 ACD	Samples
AM6548BACDXEAF	ACTIVE	FCCSP	ACD	784	60	RoHS & Green	Call TI	Level-3-250C-168 HR	-40 to 105	AM6548BACDXEAF 900 900 ACD	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

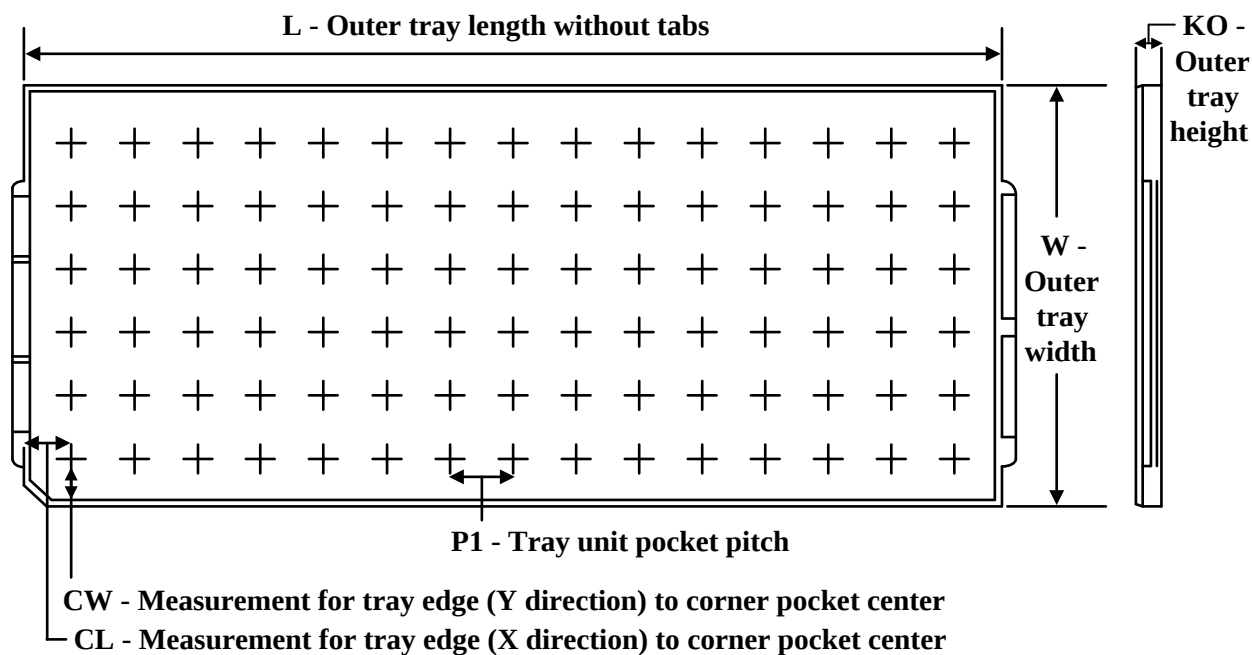
⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

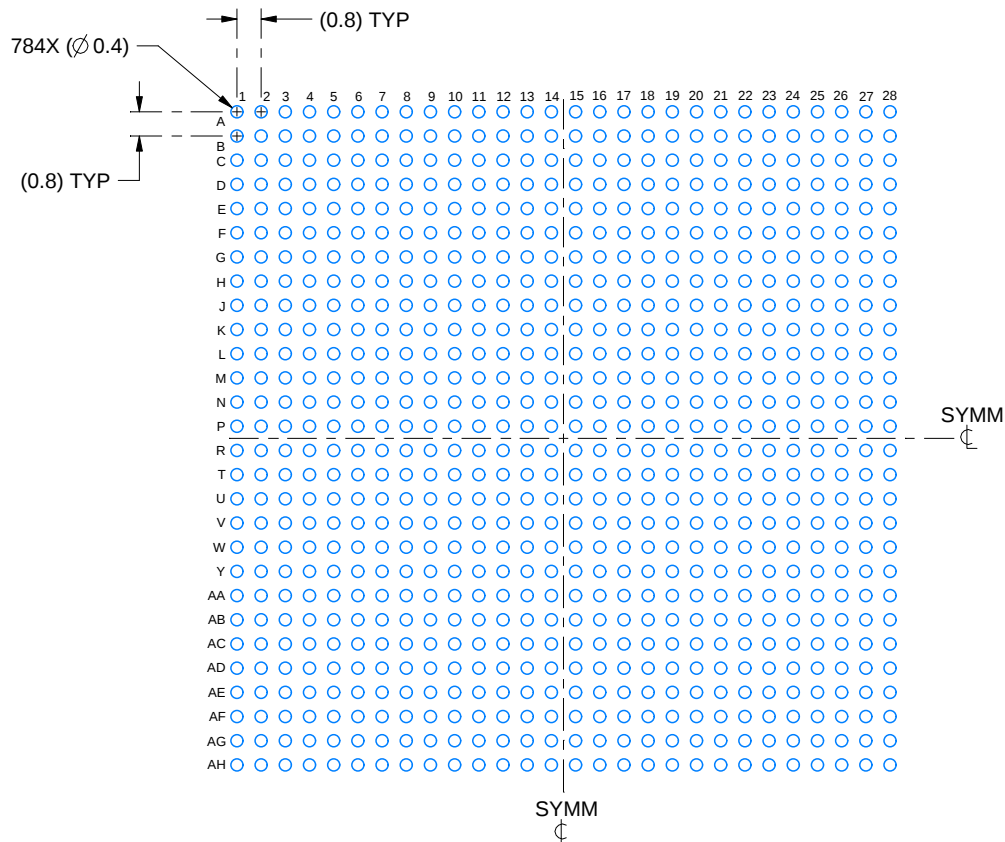
Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (μm)	P1 (mm)	CL (mm)	CW (mm)
AM6526BACDXA	ACD	FCCSP	784	60	5 x 12	150	322.6	135.9	7620	25.5	17.25	16.95
AM6526BACDXEAF	ACD	FCCSP	784	60	5 x 12	150	322.6	135.9	7620	25.5	17.25	16.95
AM6528BACDXEA	ACD	FCCSP	784	60	5 x 12	150	322.6	135.9	7620	25.5	17.25	16.95
AM6546BACDXA	ACD	FCCSP	784	60	5 x 12	150	322.6	135.9	7620	25.5	17.25	16.95
AM6548BACDXEAF	ACD	FCCSP	784	60	5 x 12	150	322.6	135.9	7620	25.5	17.25	16.95

EXAMPLE BOARD LAYOUT

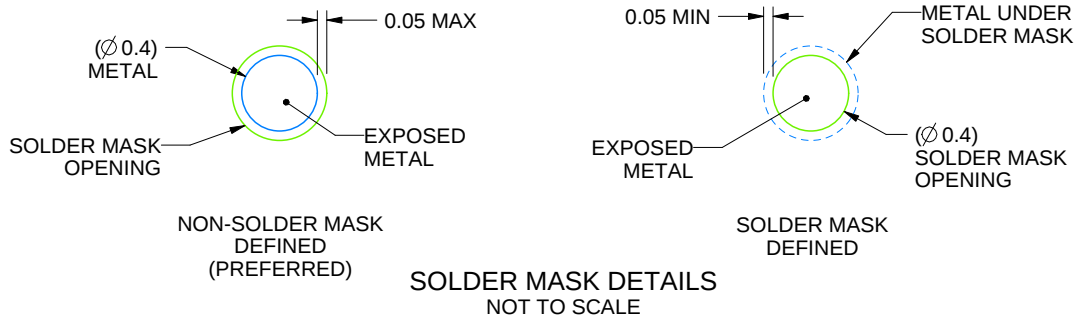
ACD0784A

FCBGA - 1.63 mm max height

BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 4X



4223579/B 01/2019

NOTES: (continued)

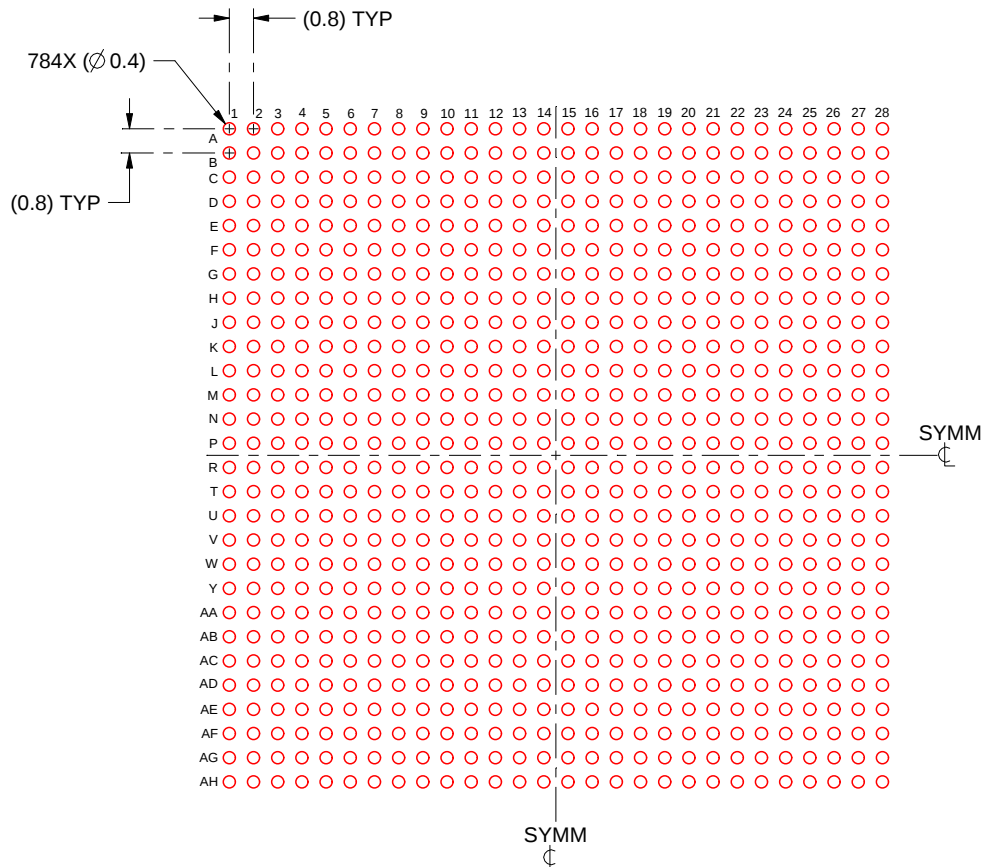
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. See Texas Instruments Literature No. SPRU811 (www.ti.com/lit/spru811).

EXAMPLE STENCIL DESIGN

ACD0784A

FCBGA - 1.63 mm max height

BALL GRID ARRAY



SOLDER PASTE EXAMPLE
 BASED ON 0.15 mm THICK STENCIL
 SCALE: 4X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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