参考資料

TI Designs: TIDA-00893
電源内蔵の絶縁CANのリファレンス・デザイン

概要

このリファレンス・デザインでは、絶縁DC電源を生成し、同時に絶縁CAN通信をサポートする、小型のソリューションを紹介します。この絶縁CANのリファレンス・デザインは、強化されたデジタル・アイソレータと内蔵電源およびCANトランシーバの組み合わせで構成され、放射を低減するよう設計されています。

リソース

TIDA-00893	デザイン・フォルダ
TCAN1042-Q1	プロダクト・フォルダ
ISOW7841	プロダクト・フォルダ

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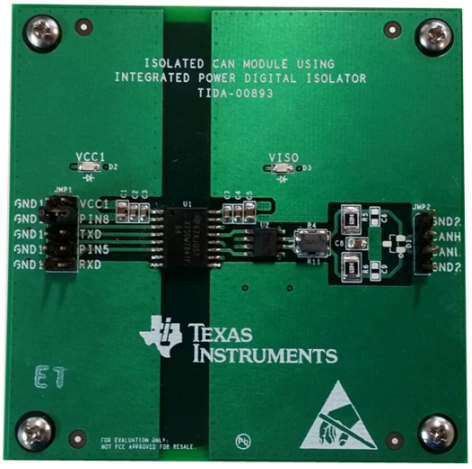
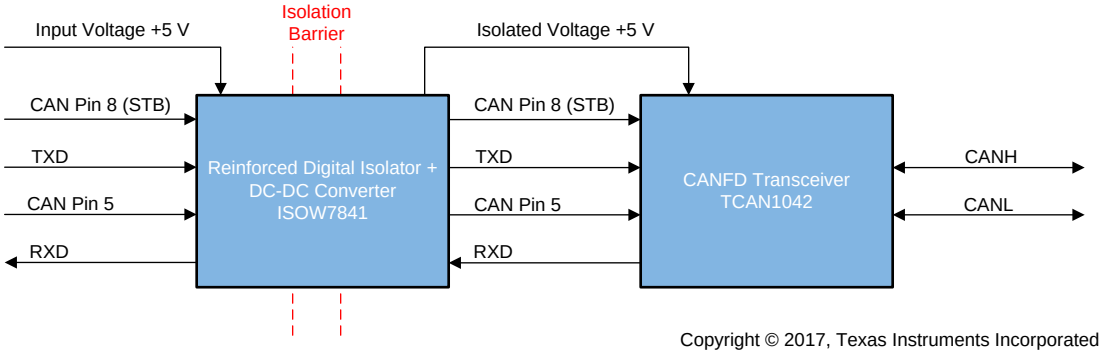


特長

- バリアの両側で±8kV超、同じ側で±16kVのIEC 61000-4-2 ESD保護
- 最適化されたサイズでも±4kV EFTバースト許容
- 業界最先端の同相過渡耐性(CMTI): ±100kV/µs (最小値)
- 単一電源のソリューション
  - サイド2のコンポーネント用に別の電源が不要
  - ISOW7841のV_{ISO}は最大130mAの負荷に電力を供給可能
  - 3Vおよび5VのCANアプリケーションをサポート可能
- 別の変圧器が必要ないため、ソリューションのBOMコストを低減
- 設計の単純化
- 高速なループ遅延
- 他のCANやCAN FDトランシーバに拡張可能
- PCB設計により絶縁バリアにまたがるスティッチング・コンデンサを実装して放射を改善

アプリケーション

- PLC、PAC、DCS通信モジュール
- グリッド通信モジュール
- 産業用オートメーション
- 高電圧システムの通信モジュール



1 System Description

This reference design combines both data and power isolation along with a Controller Area Network (CAN) communication interface to provide a robust, low-cost, small-footprint solution that customers can directly place on their designs. This design combines a high-performance reinforced digital isolator with an integrated high-efficiency, low-emissions DC/DC converter (ISOW7841), and a robust automotive fault protected CAN flexible data rate (CAN FD) transceiver (TCAN1042HG-Q1).

This reference design does not require any additional components to generate the isolated power, making the isolation solution less than a quarter of the size of all existing solutions by using a discrete transformer to generate the required isolated power. This reference design takes a single power supply input between 3 V and 5.5 V and digital signals referred to the input supply level on side 1 of the board. The ISOW7841 generates an isolated power supply using an integrated DC/DC converter, which is used to power the CAN transceiver on side 2 of the board. The side 1 signals are isolated and connected to the CAN transceiver, which converts the single-ended digital signals into the differential CAN format.

PLCs and grid communication systems have been an integral part of factory automation and industrial process control using digital and analog I/O modules to interface to sensors, actuators, and other equipment. Analog inputs for the PLC system include temperature sensors, transmitters, and current and voltage sensors. Examples of common digital inputs include push-buttons, proximity switches, photo sensors, pressure switches, and more that need to be either group isolated or isolated per channel. Because PLCs are expected to work in harsh industrial environments, sensor signals are converted into the digital domain and coupled to the control domain through a digital isolator. Power for the sensors and switches is also isolated from the back plane side with an isolated DC/DC converter. The isolated CAN reference design can significantly reduce the required component mounting area on the PCB and bring down the BOM cost by eliminating the requirement for discrete transformers.

1.1 Key System Specifications

表 1. Key System Specifications

FEATURE	PARAMETER	SPECIFICATION
Input supply	Input voltage	5 V
Isolated output supply	Output voltage	3.3 V or 5 V
	Output current	75 mA (3.3 V_{IN})
		130 mA (5 V_{IN})
Communication	Max data rate	5 Mbps (CAN FD communication)
Isolation	Clearance	> 3 mm
	Surge	4 kV
	Working voltage	300 V_{RMS}
	CMTI	> 100 kV/µs
EMI or EMC	ESD	6 kV (across barrier)
		16 kV (across CAN lines)
	EFT	2 kV (Class A)
	Radiated emissions	CISPR22 (Class B)
	Radiated immunity	10 V/m

2 System Overview

2.1 Block Diagram

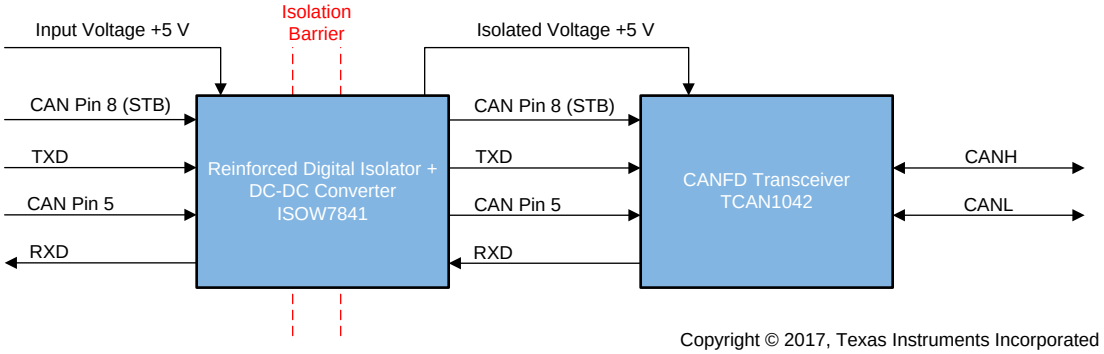


図 1. TIDA-00893 Block Diagram

図 1 shows the high-level block diagram of this reference design, which can be broken down to two main sections: the isolation block (ISOW7841) and the interface block (TCAN1042HG-Q1).

The isolated CAN reference design works on a single input of 3 V to 5.5 V. The integrated power supply can produce an isolated output voltage of 3.3 V (for any input) or 5 V (for VCC1 ≥ 5 V), which can be used to power up the CAN interface block. Most CAN transceivers including the TCAN1042HG-Q1 use a 5-V supply; some CAN transceivers use a 3.3-V supply that can be supported by this reference design. Digital signals from a source such as a microcontroller (MCU) are connected on one side of the board to the ISOW7841 digital isolator, and the differential CAN lines that communicate with the field side of the system are connected to the other.

2.2 Highlighted Products

This reference design features the following devices from Texas Instruments.

2.2.1 ISOW7841

The ISOW7841 is a high-performance, quad-channel, reinforced digital isolator with an integrated, high-efficiency power converter. The integrated DC/DC converter provides up to 650 mW of isolated power at high efficiency, can be configured for various input and output voltage configurations, and eliminates the need for a separate isolated power supply in isolated designs with space constraints.

The ISOW7841 device provides high electromagnetic immunity and low emissions while isolating CMOS or LVCMOS digital signals with an isolation channel that has a logic input and output buffer separated by a silicon dioxide (SiO_2) insulation barrier. Power isolation uses on-chip transformers separated by insulation material that is a thin film polymer. Unwanted noise currents are prevented from entering the data bus, other circuits, or the local ground and interfering with or damaging sensitive circuitry. Through innovative chip design and layout techniques, the electromagnetic compatibility of the ISOW7841 has been significantly enhanced to ease system-level electrostatic discharge (ESD), electrical fast transient (EFT), surge, and emissions standard compliance. The high efficiency of the power converter allows operation at a higher ambient temperature. The ISOW7841 is available in a 16-pin SOIC wide-body (DWE) package.

Key features of the ISOW7841 isolator include the following:

- Integrated, high-efficiency DC/DC converter with on-chip transformer
- Wide input supply range: 3 V to 5.5 V
- Regulated 3.3-V or 5-V output
- Up to 650-mW output power
- 130-mA load current (5 V to 5 V or 5 V to 3.3 V)
- 70-mA load current (3.3 V to 3.3 V)
- Soft start to limit inrush current
- Overload and short-circuit protection
- Thermal shutdown
- Signaling rate up to 100 Mbps
- Low prop-delay: 13 ns typical (5-V supply)
- High CMTI: ±100 kV/µs (min)
- Robust electromagnetic compatibility (EMC):
  - System-level ESD, EFT, and surge immunity
  - Low radiated emissions
- Safety-related certifications:
  - 7071-V_{PK} Reinforced Isolation per DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12
  - 5000-V_{RMS} Isolation for 1 Minute per UL 1577
  - CSA Component Acceptance Notice 5A, IEC 60950-1 and IEC 60601-1 End Equipment Standards
  - CQC Approval per GB4943.1-2011
  - TUV Certification according to EN 60950-1 and EN 61010-1

  - All agency certifications are planned
- Extended temperature range: –40°C to +125°C

2.2.2 TCAN1042HGV-Q1

The TCAN1042HG-Q1 transceiver meets the ISO 11898-2 (2016) high-speed CAN physical layer standard. This transceiver is designed for data rates in excess of 1 Mbps for CAN FD with an enhanced timing margin for higher data rates in long and highly-loaded networks. The TCAN1042 provides many protection features including undervoltage protection (UVLO) on the supply pins, ±70-V bus fault protection, both driver and receiver dominant state timeouts (TXD DTO, RXD DTO), and thermal shutdown protection (TSD). The CANH and CANL bus pins also have robust integrated ESD protection against HBM, CDM, IEC 61000-4-2, and ISO 7637 standards. Without requiring external protection components, the TCAN1042HG-Q1 tolerates ±8-kV IEC 61000-4-2 ESD, ±16-kV HBM ESD, and ±4-kV IEC 6100-4-4 EFT levels.

Key features of the TCAN1042HGV-Q1 transceiver include the following:

- AEC Q100: qualified for automotive applications
- Meets the ISO 11898-2:2016 physical layer update
- Meets the released ISO 11898-2:2007 and ISO 11898-2:2003 physical layer standards
- "Turbo" CAN:
  - Supports 5-Mbps CAN FD
  - Short and symmetrical propagation delay times and fast loop times for enhanced timing margin
  - Higher data rates in loaded CAN networks
- Input and output voltage range supports 3.3-V and 5-V MCUs
- Ideal passive behavior when unpowered:
  - Bus and logic terminals are high impedance (no load)
  - Power-up and power-down glitch free operation on bus and RXD output pins
- Protection features:
  - HBM ESD protection: ±16 kV
  - IEC ESD protection: up to ±15 kV
  - Bus fault protection: ±70 V
  - UVLO on V_{CC} and V_{IO} (V variants only) supply terminals
  - Driver dominant timeout (TXD DTO) with data rates down to 10 kbps
  - Thermal shutdown protection (TSD)
- Receiver common-mode input voltage: ±30 V
- Typical loop delay: 100 ns
- Junction temperatures: –55°C to +150°C

2.3 System Design Theory

2.3.1 Isolation

Noise can seriously affect the integrity of data transfer in most industrial interface systems. Including galvanic isolation in the interface circuit is a proven method for improving the communication performance and protecting the low-voltage (LV) MCU side from the high-voltage (HV) side exposed to stresses like ESD, EFT, and surge.

Ground loops and electrical line surges can cause many forms of radiated and common-mode noise with unwanted current and voltage on the cable bus connecting multiple systems resulting in severe problems. Ground loops occur when there are multiple paths in the system for current to flow to ground. These paths have different impedance and can pick up additional current through electromagnetic induction, creating a potential difference for current to flow and cause bit errors or damage components. Electrical surges can be caused by many sources typically coupled onto long cables through induction. Industrial environments have many sources of surge, such as electric motors that cause rapid changes in the ground potential while operating and force current to flow on system cables to equalize the changing ground potential.

Other HV stress sources include ESD and lightning strikes (surge) that can result in thousands of volts of potential on the line. A remote node may receive a 5-V switching signal superimposed on a HV level with respect to the local ground. These uncontrolled voltages and currents can corrupt the signal and be catastrophic to the device and system, causing damage or destruction of the components connected to the bus and resulting in system failure. CAN systems that connect multiple systems in automotive and industrial environments are especially susceptible to these events.

Isolating the CAN system devices from each of the systems connected to the bus prevents ground loops and electrical surges from destroying circuits. Isolation prevents ground loops because each system and CAN circuit connected to a CAN cable bus has a separate and isolated ground. By referencing each CAN circuit only to one ground, ground loops are eliminated. Isolation also allows the reference voltage levels of the CAN circuit to rise and fall with any surges that appear on the cable line. Isolation allows the circuit voltage reference to move with surges, rather than being clamped to a fixed ground, preventing devices from being damaged or destroyed. To accomplish system isolation, both the CAN signal lines and power supplies must be isolated.

2.3.2 CAN Communication

CAN is an International Standardization Organization (ISO) defined serial communications bus originally developed for the automotive industry to replace complex wiring harnesses with a two-wire bus. The specification calls for high immunity to electrical interference and the ability to self-diagnose and repair data errors. These features have made CAN popular in a variety of industries including building automation, process control automation, elevators, construction equipment, robotics, medical, and manufacturing among many others.

The following key features make CAN ideal for use in industrial and instrumentation applications:

- Established standard and standardized plug-n-play products
- Fault tolerant, very-high short-circuit protection
- Self-diagnosing error repair, every bit checked five times for errors
- Robust interface for harsh electrical environments
- Wide common-mode operating range tolerant of ground potential differences
- Multi-master message broadcast system where all nodes receive all messages

- Message priority identifier with lossless bit-wise arbitration system to ensure the highest priority message is transmitted first and no message is lost

3 Hardware, Testing Requirements, and Test Results

3.1 Hardware

3.1.1 Board Description

図 2 shows the size of the reference design that has been optimized for low radiated emissions with the component mounting area on the board marked in red. Traditional solutions that do not integrate power isolation into the same digital isolation device require transformers, transformer drivers, and rectifiers to isolate the power from one side of the isolation barrier to the other. These additions take up much more space on a PCB than the integrated solution shown with the ISOW7841. The board for this reference design measures 3 by 3 inches, while the component mounting requires less than 0.5 by 2 inches of area. This board has been separated into two sides for isolation. Side 1 is the system side connected to power input VCC1 and GND1 planes. Side 2 is connected to the isolated output voltage (V_{ISO}) and GND2 planes and contains the TCAN1042 transceiver.

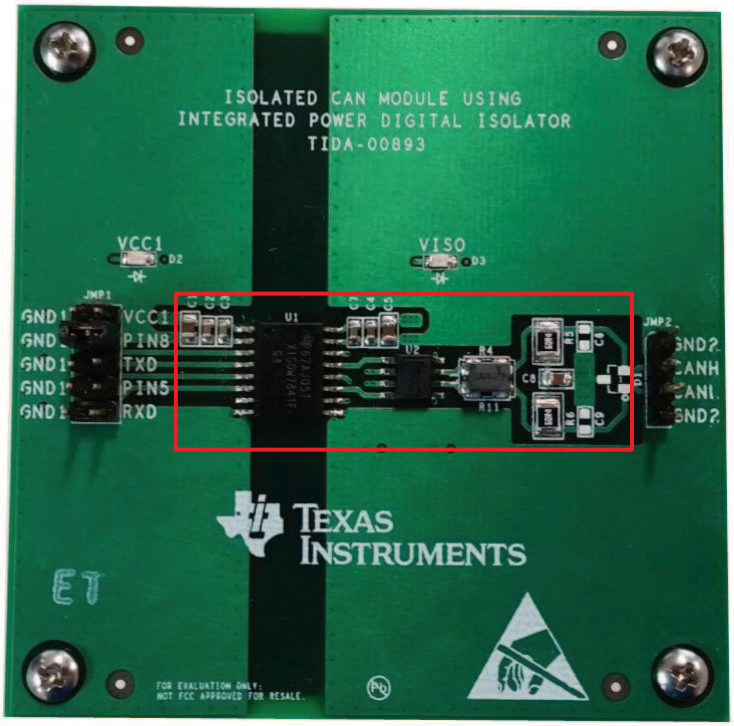


図 2. Component Mounting Area

The transformers used in non-integrated solutions are typically high-inductance magnetic-core transformers with low switching frequencies and are fairly large in size. By scaling the power isolation components into a single device, chip-scale transformers are used to keep small area solutions possible. These small transformers use much fewer turns than the external transformers, reducing the series resistance. As a result, a higher-frequency DC/DC converter is needed to drive the transformer at several tens of megahertz or more.

Because the primary and secondary windings of these small transformers are close together inside the device package, and typically do not use magnetic cores, a parasitic capacitance forms between the two coils of the transformer, which could be fairly large. This capacitance allows a path for the fast transients in the DC/DC converter to couple through to the other side, creating common-mode current between the two sides. However, because the two sides of the ISOW7841 device are completely isolated, the current forms a path through parasitic capacitance on the board itself creating a large current loop and radiated emissions.

The power converter used to drive the transformer has a duty cycle and high-current draw from the V_{CC} input supply during the active portion of the cycle. The low-frequency content of the current is somewhat proportional to the closed-loop regulation bandwidth of the DC/DC converter while the higher frequency content is a result of the switching frequency and harmonics. Therefore, the common-mode current is composed of several different components of varying frequency that need to be addressed.

One of the methods used in this reference design to address this common-mode current is to include a bank of three different valued capacitors at both the input and output voltage pins. This bank helps filter out this frequency content and prevent it from propagating through the power routing. The smallest valued capacitor, 100 nF, is placed closest to the ISOW7841 pins, followed by the 1-µF capacitors and then the 10-µF capacitors, making the area of the power to ground loops as small as possible.

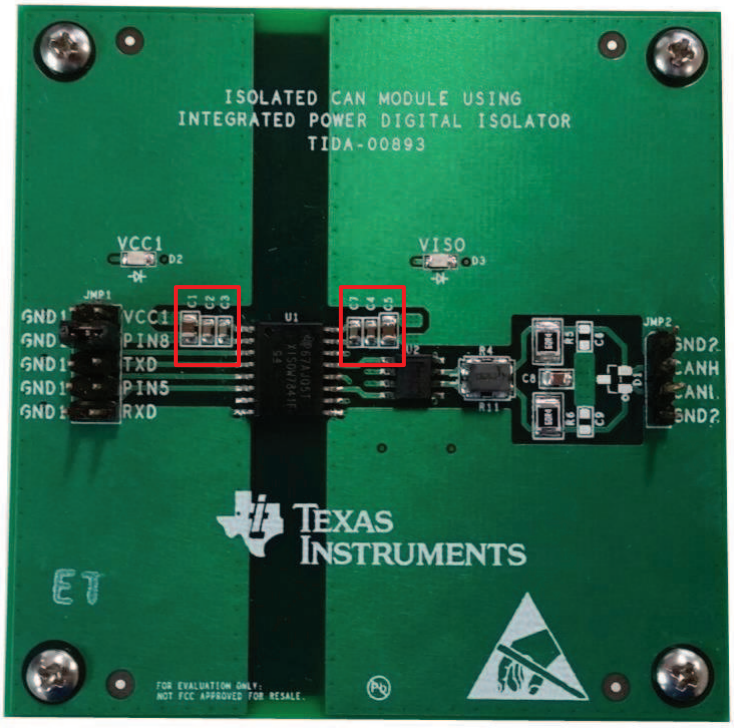


図 3. Decoupling Capacitor Banks

Secondly, this board is a four-layer design and uses the internal layer three for power. Layer two is used for ground along with the majority of the top and bottom layer not used for component placement and signal routing. Stitching vias are placed along the edges of the board and along the isolation channel to form a Faraday cage around any noise on the internal power planes, which can contribute to the radiated emission profile.

Despite all the efforts to filter and contain the transient noise on either side of the isolation channel, there is still some common-mode current that flows through the board parasitic capacitance between the two sides. A capacitor can be added between the GND pins on each side of the isolator, but that capacitor must be a high-voltage capacitor rated to handle the isolation voltage needs. This capacitor also comes with some inductance from the leads and limit the maximum effective frequency range.

Instead of increasing the BOM cost and limiting the maximum effective frequency by adding one of these capacitors to this reference design, a low-inductance capacitor is created in the PCB layout by overlapping the internal PCB layers within the isolation channel region.

The side 1 GND plane on layer two of the board (see 図 23), and connected to pin 8 of the ISOW7841, is extended most of the way into the channel, leaving approximately 0.66 mm of gap between it and the side 2 GND plane. The side 2 VISO plane on layer three (see 図 24) is likewise extended into the isolation channel region, leaving approximately 0.66 mm of gap between VCC on side 1 of the isolation device.

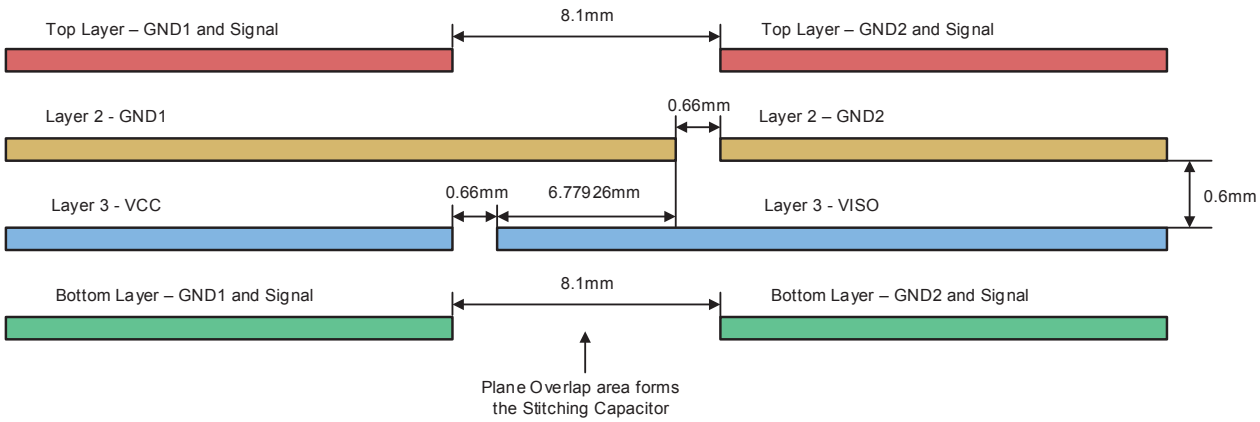
The thickness of the FR-4 dielectric material between the GND1 and VISO planes is 0.6 mm. This material creates a parallel plate stitching capacitance across the isolation region and creates a lower inductance path for the high-frequency switching transients to flow, thereby reducing the amount of radiated emissions.

The capacitance of the stitching capacitor C_i can be calculated with 式 1:

$$C_i = \varepsilon_0 \times \varepsilon_r \times \frac{A}{d} \quad (1)$$

where:

- ε_0 is the absolute permittivity of air (8.854 pF/m)
- ε_r is the relative permittivity of the dielectric (4.2 for FR-4)
- A is the overlapping area
- d is the distance between GND and V_{CC} layers



ε_0	ε_r	D (mm)	L (mm)	W (mm)	→	C_i (pF)
8.85E-12	4.2	0.6	71.12	6.77926		29.88213

図 4. Isolation Channel With Embedded High-Frequency Stitching Capacitor

While creating a stitching capacitance inside the isolation channel improves the radiated emissions, it also brings the power and ground planes from the two sides closer together. The standards for systems with reinforced isolation require a minimum spacing between the two sides to maintain sufficient isolation for the application given the dielectric strength of the board material insulation.

The IEC 66010-1 standard mandates that a reinforced isolated system withstand a 5-second test of 3510 V_{RMS} and a surge or impulse test of 6400 V_{PK} for mains voltage between 300 V_{RMS} and 600 V_{RMS}. The minimum spacing of 0.6 mm is needed for systems that require between 300 V_{RMS} and 600 V_{RMS}, but that spacing can be reduced to 0.4-mm if less than 300 V_{RMS} of isolation is needed. A minimum spacing of 0.6-mm is used in this reference design to provide isolation up to 600 V_{RMS} using FR-4 with a dielectric strength of 20 kV/mm.

Because the breakdown voltage of air is different than that of the FR-4, the power and ground planes are kept away from the edges of the board by more than 0.6 mm to ensure that there is not excessive field stress that could cause an air breakdown along the edge of the board. Sharp corners on the planes also increase the electric field intensity. To reduce the risk of a breakdown occurring between the planes during a high-voltage pulse, all corners of the planes are mitered at 45° to help spread out the charge density and ensure there are no 90° sharp corners that could lead to a breakdown.

It is also common practice to use a common-mode choke on the CAN bus pins to remove any noise coming into the node from the CAN bus and to prevent any noise generated in the node from entering the bus. The TCAN1042 CAN FD transceiver already has excellent emissions performance and does not require a common-mode choke to pass IEC TS 62228; adding one improves the performance even more.

Furthermore, because a high-frequency DC/DC converter is used in the power isolation, a small amount of the common-mode noise can filter into the power supply of the TCAN1042 and find its way into the CAN bus. Using a choke prevents this from occurring. If a common-mode choke is not needed, remove and replace the choke with two low-valued resistors such as 0 Ω.

There is also a placeholder on the board for an external TVS diode to help achieve greater ESD protection than what the TCAN1042 can provide. Loading capacitors are also added to each CAN line that can be populated to help mimic the capacitive load of the cabling on a CAN bus in a lab environment along with pullup and pulldown resistors on the digital signals connector for convenience of the user. Because all of these components are not required for a real system, it is left up to the user to configure them per his or her requirements.

3.1.2 Connector Description

There are only two connectors on this board: one for the power and digital interface side, and the other for the CAN bus side.

The connector on the left side of the board is for the power and digital signals. Connect a 5-V DC power supply between the VCC and GND1 pins. All the other signals are labeled according to their function and have a GND1 pin next to each one to provide easy access to a scope probe GND reference or that of a cable coming from an MCU or signal generator.

Pins 5 and 8 vary in function among CAN transceivers. The TCAN1042 used in this reference design uses pin 8 for a standby mode control, and pin 5 as a VIO supply pin that could be either 5 V or 3.3 V depending on the signal level of the MCU connected to it. The ISOW7841 is capable of supplying an isolated 5 V or 3.3 V on the VISO pin. However, the isolator can not supply both a 5-V VCC rail and 3.3-V VIO rail at the same time.

Therefore, for this reference design, the same 5-V supply level is used for VIO. This pin is isolated from the connector with an uninstalled resistor because this is not a digital signal. Other transceivers could use this pin as a fault indicator pin. If one of those transceivers are evaluated with the ISO7841 instead of the TCAN1042, this signal is available on the connector by populating this resistor with a 0-Ω resistor.

The connector on the right side of the board has the CANH and CANL bus pins along with a GND2 pin next to each one as an easy reference for a ground reference pin of a scope probe.

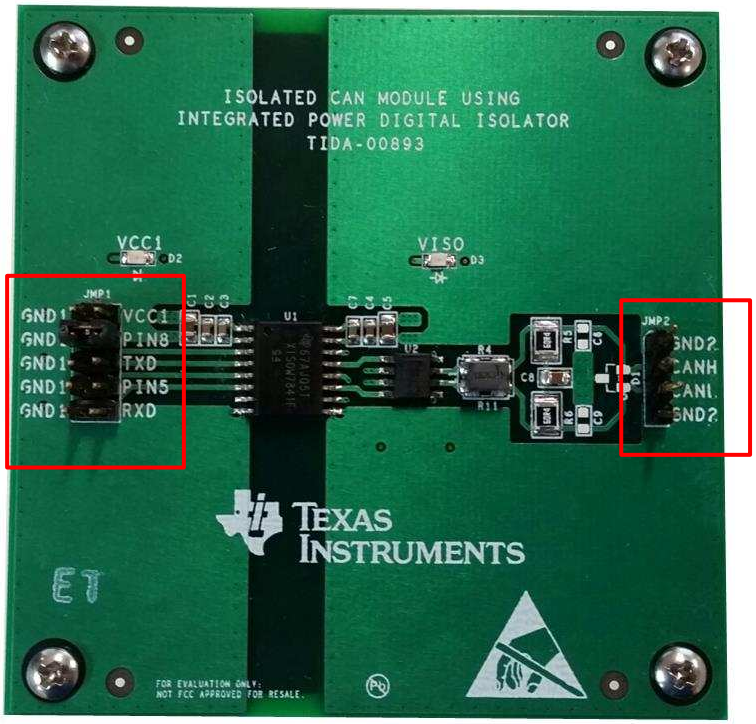


図 5. Board Connectors

3.2 Testing Results—Waveforms and $T_{PROP(LOOP)}$ Measurements

The TCAN1042 transceiver can support both classical CAN applications with data rates up to 1 Mbps and CAN FD applications with data rates up to 5 Mbps. Waveform symmetry is critical in maintaining low common-mode noise and radiated emissions. Therefore, waveforms of the CANH, CANL, TXD, and RXD are captured on a scope at both 1- and 5-Mbps data rates using a square wave input signal from a pattern generator to mimic the maximum data rates of the CAN and CAN FD protocols.

During the arbitration phase of the CAN protocol, the propagation delay of the transceiver and the delay between the nodes is important. To ensure that the node with the highest priority message gains control of the bus, the MCU monitors the data coming into its RXD pin and compares it with the data it is transmitting on its TXD pin. If the MCU transmits a recessive bit on the TXD pin yet detects a dominant bit on the RXD pin, the MCU loses arbitration to a node with a higher priority message and stop transmitting, thereby yielding the bus to the other node. This arbitration must be completed in 255 ns, which is about 25% of the bit period for a 1-Mbps data bit and the maximum allowable loop delay for a signal propagating between the TXD pin and the RXD pin of the transceiver.

Adding isolation between the MCU and the transceiver increases the loop time, can impact the arbitration, and cause bit collisions between two nodes. Having fast transceiver loop delays allows the MCU to perform arbitration quickly, giving a performance margin to the overall system. These delays also allow for margin when adding the additional delay from an isolation device while maintaining the required timing.

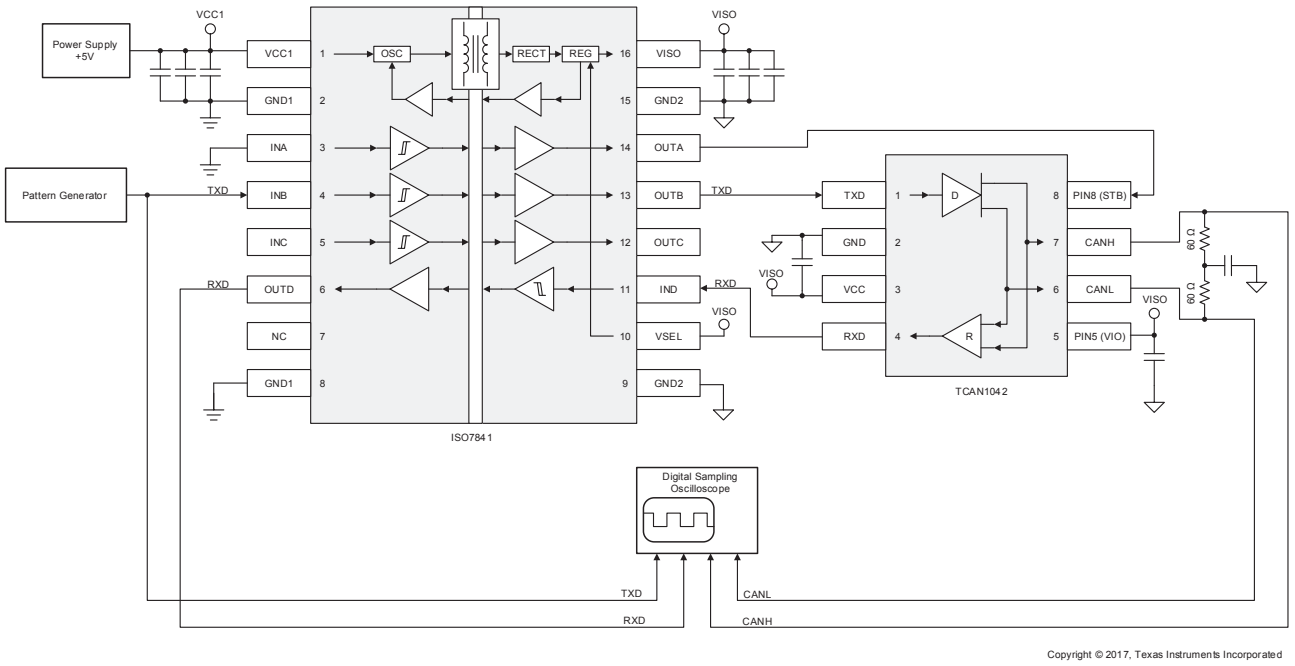


図 6. Scope Waveforms and $T_{PROP(LOOP)}$ Measurement Test Setup

図 7 shows the TXD, RXD, CANH, and CANL signal waveforms with a repeating one-zero data pattern running at 1 Mbps. 図 8 shows the same signals with the data pattern running at 5 Mbps.

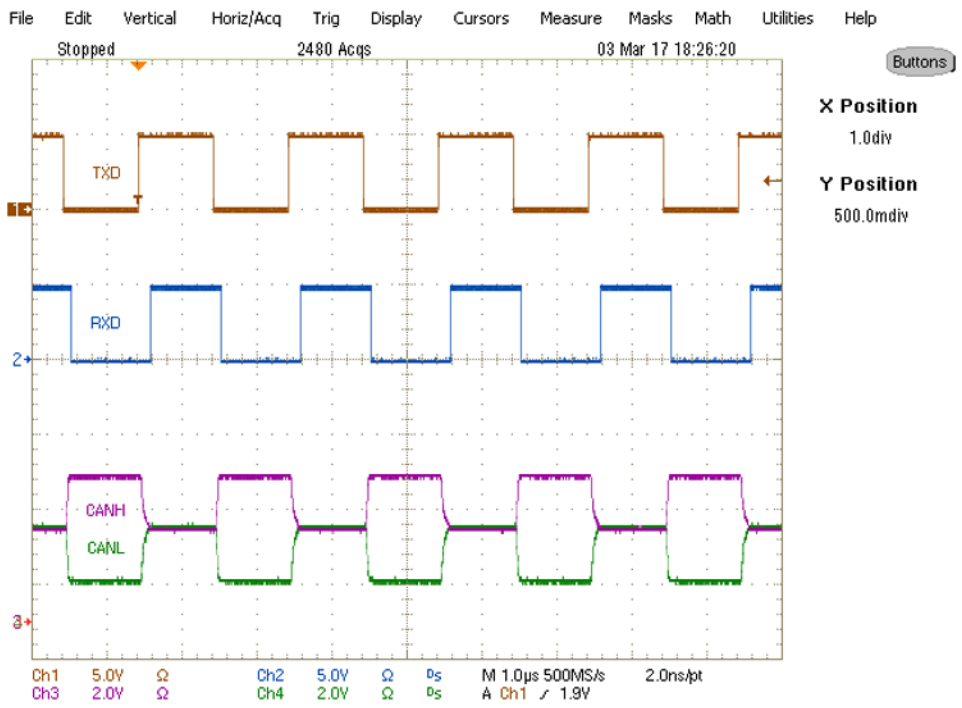


図 7. CAN Waveforms With 1 Mbps of Data

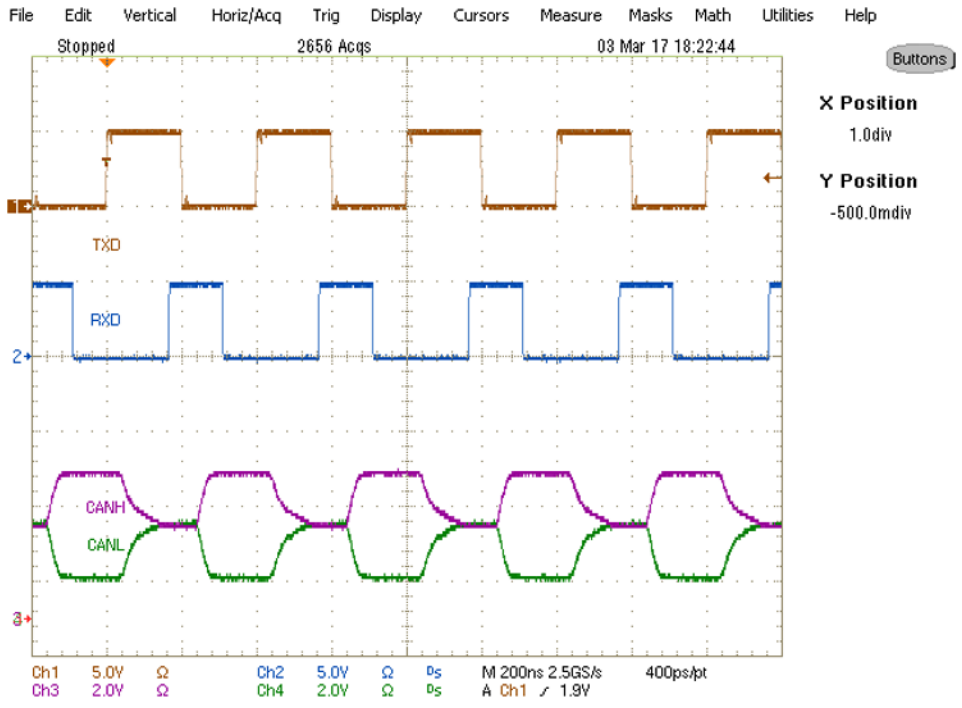


図 8. CAN Waveforms With 5 Mbps of Data

図 9 shows the test circuit and measurement definition of the TCAN1042 $T_{PROP(LOOP)}$.

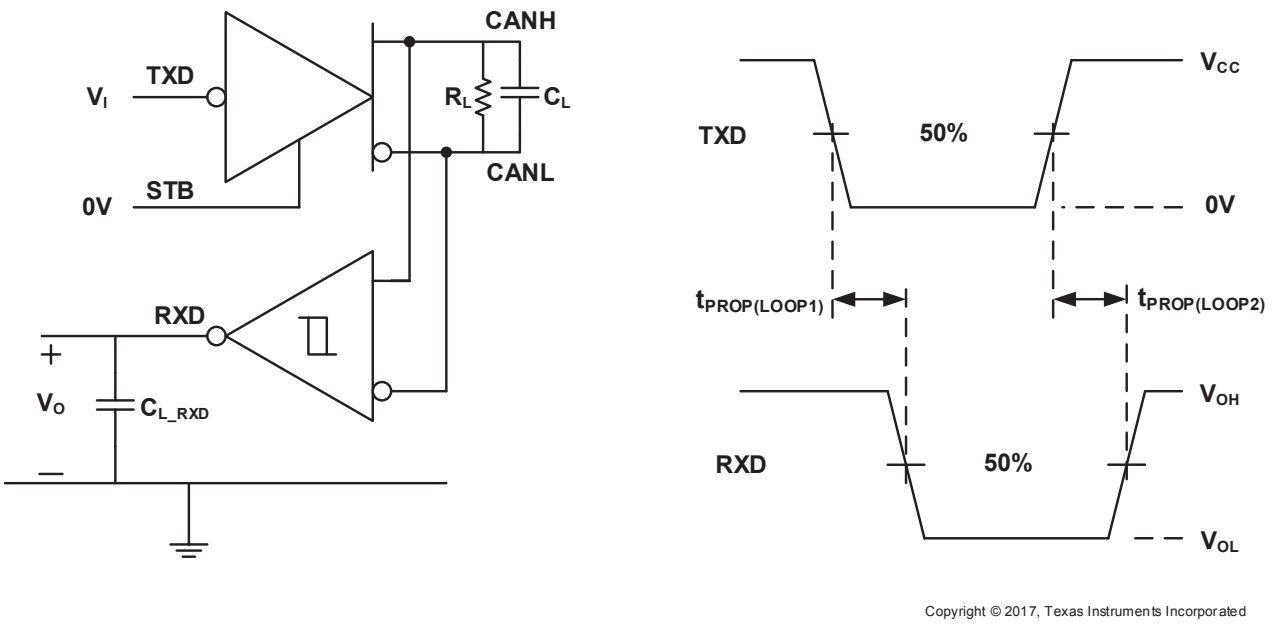


図 9. Test Circuit and Measurement of TCAN1042 $T_{PROP(LOOP)}$

The following figures show the measured $T_{PROP(LOOP)}$ delays of the TCAN1042 with the additional delay of the ISOW7841, as shown in 図 6.

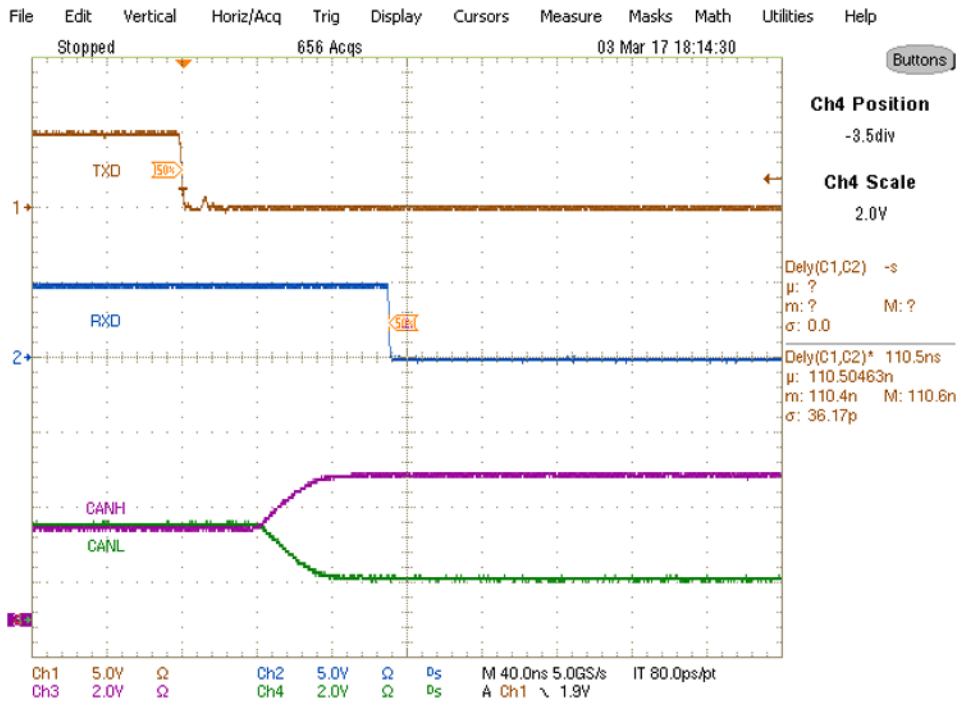


図 10. $T_{PROP(LOOP1)}$ Delay Measured With 1 Mbps of Data

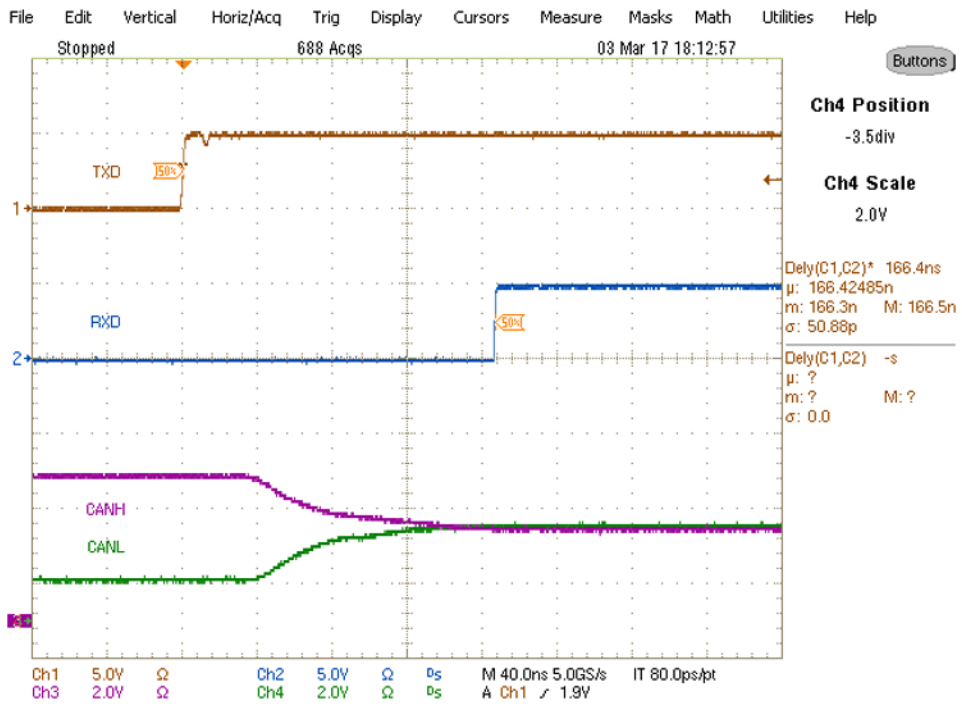


図 11. $T_{PROP(LOOP2)}$ Delay Measured With 1 Mbps of Data

Because the $T_{PROP(LOOP)}$ delay times are fixed, they are not expected to change with the data rate, as shown in the following figures with the data pattern increased to 5 Mbps.

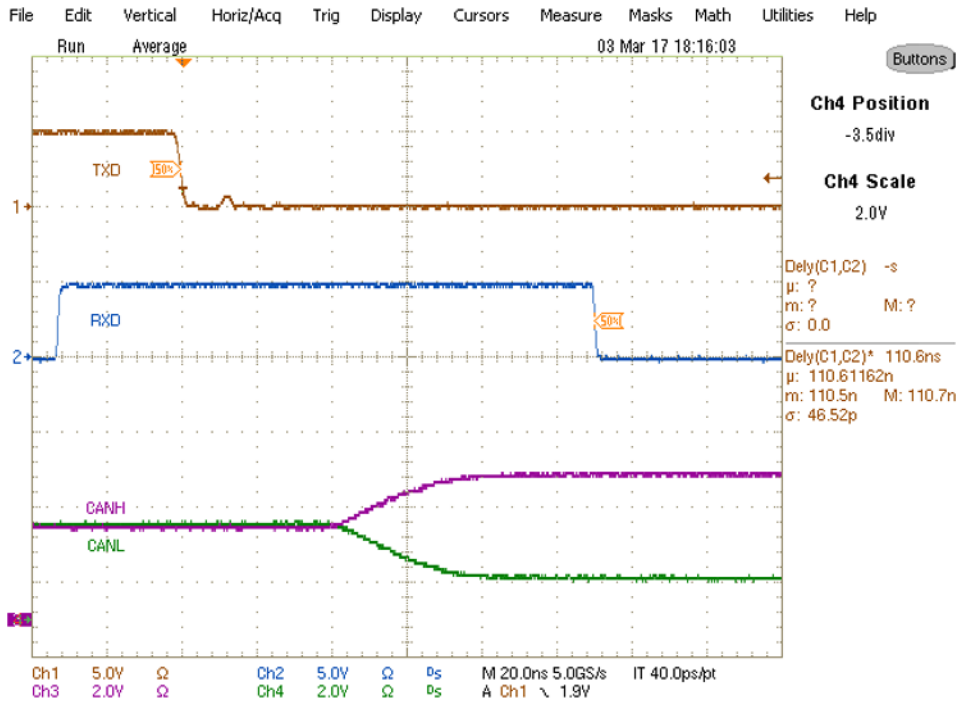


図 12. $T_{PROP(LOOP1)}$ Delay Measured With 5 Mbps of Data

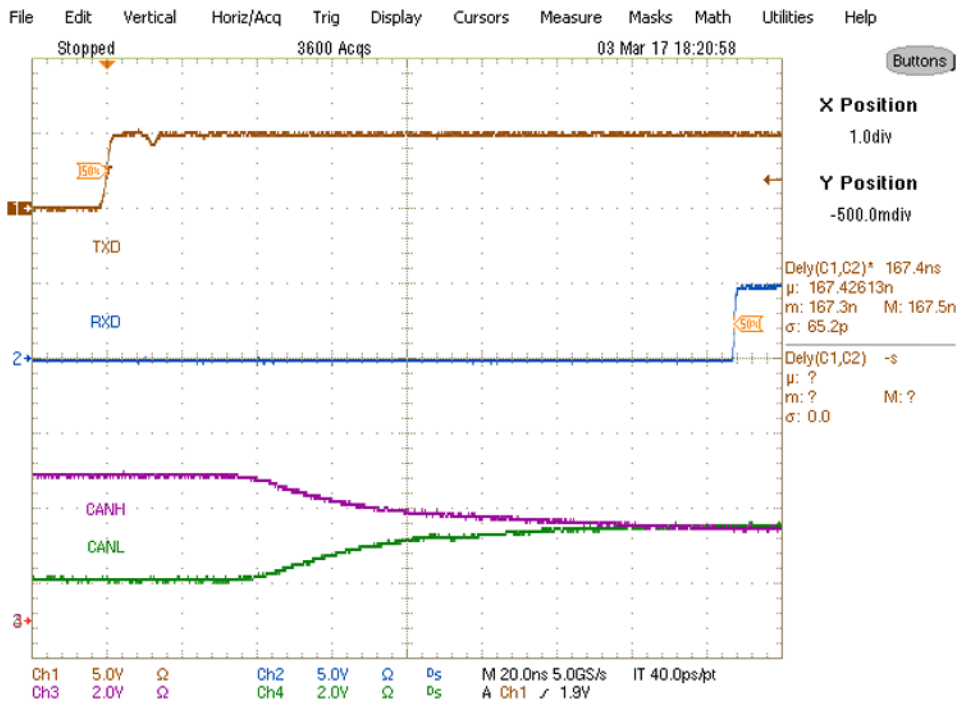


図 13. $T_{PROP(LOOP2)}$ Delay Measured With 5 Mbps of Data

表 2. $T_{PROP(LOOP)}$ Measurement Summary

DATA RATE (Mbps)	$T_{PROP(LOOP1)}$ (ns)	$T_{PROP(LOOP2)}$ (ns)
1	110.5	166.4
5	110.6	167.4

3.3 Testing and Results—Conducted Emissions

Both conducted and radiated emissions concern system designers. The conducted emissions are measured according to the IEC TS 62228 standard using the Zwickau CAN HS EMI/EMS V3.6a BK01/BK13 test circuit board. This board measures the emissions on the CAN bus with three TCAN1042 transceivers or nodes populated, but it does not have provision for the ISOW7841 digital isolator with integrated power. Therefore, to accommodate testing of the conducted emissions, the TCAN1042 is removed from the design board, and the TXD, RXD, VISO, and GND pins of the ISOW7841 are connected to the TCAN1042 device under test on the test circuit board. The conducted emissions test setup is shown in 図 14.

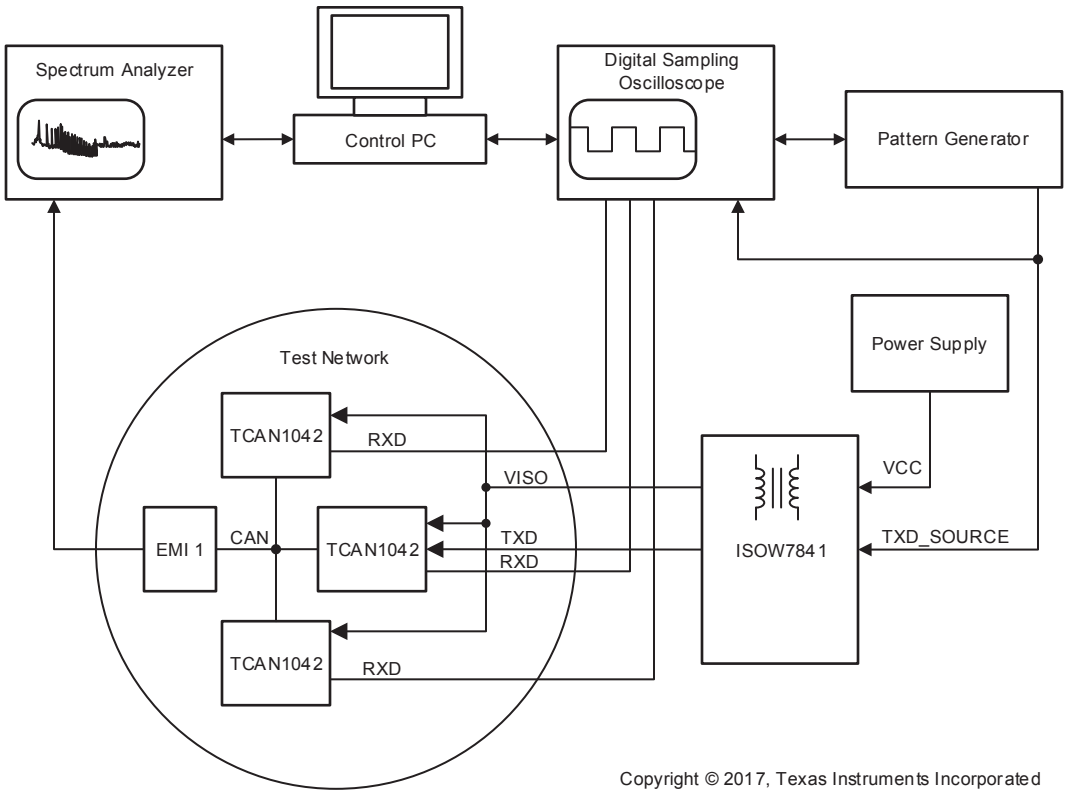


図 14. Conducted Emissions Test Setup

It is important to establish a baseline noise floor for the test setup to use as a comparison when evaluating the cumulative effects of the system under test. 図 15 shows the baseline noise floor of the test setup without the TCAN1042 and ISOW7841 devices.

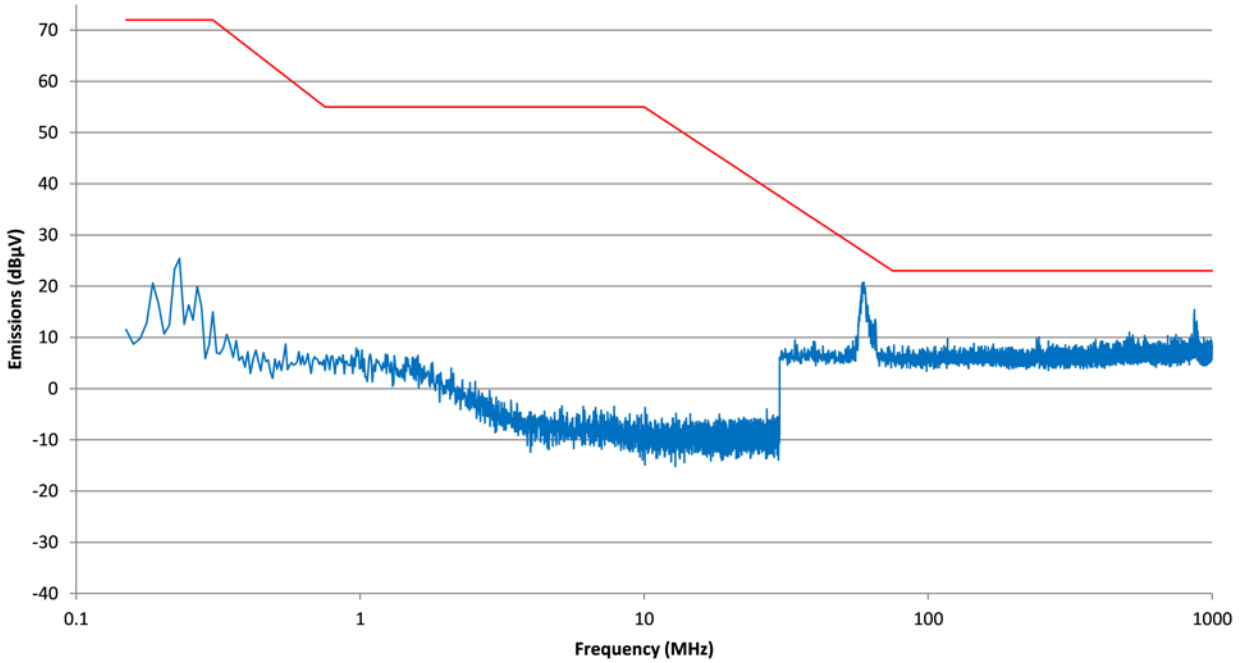


図 15. Noise Floor Measurement of Conducted Emissions Test Equipment

図 16 shows the design is capable of passing the conducted emissions test standard with the use of a common-mode choke.

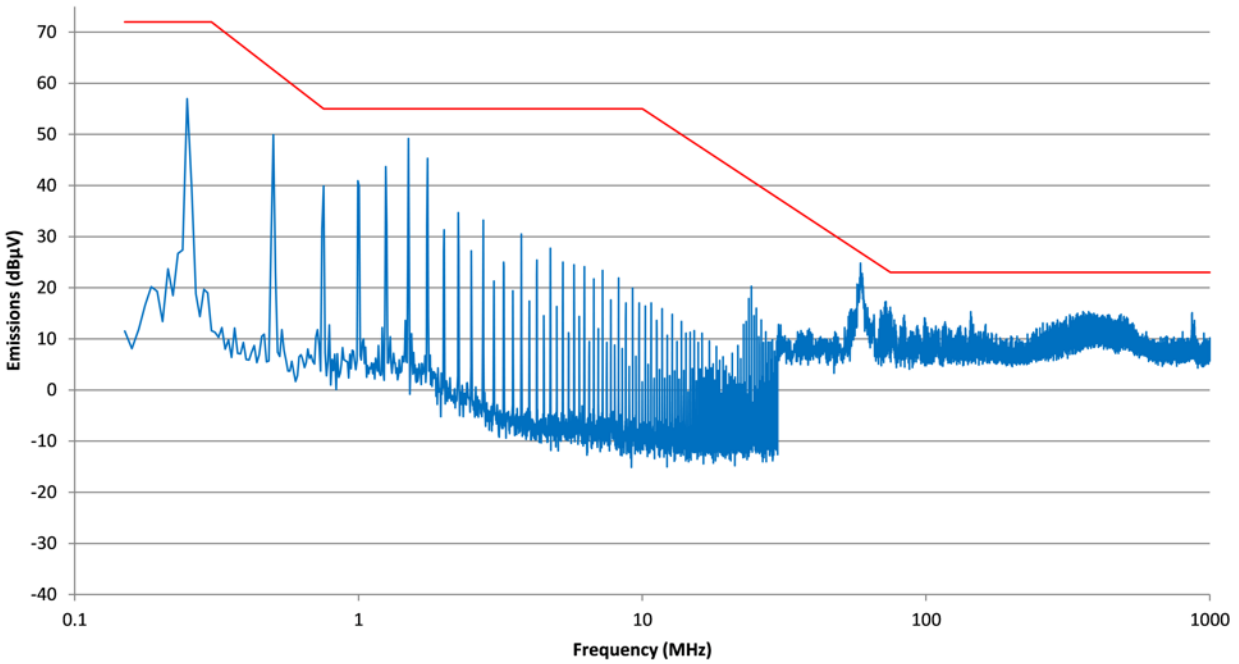


図 16. Common-Mode Choke Measurement of Conducted Emissions Test Equipment

3.4 Testing and Results—Radiated Emissions

Radiated emissions are measured on the ISOW7841 using two different boards against the CISPR 22 Class B limit. One board implements the stitching capacitance PCB layout technique duplicated in this reference design. The other board does not include the stitching capacitance technique and instead implements a traditional isolation channel under the device. Measuring the radiated emissions in this manner allows for a direct comparison on the improvement as a result of implementing the stitching capacitance.

図 17 shows the radiated emissions measurements with and without stitching capacitance. While both tests pass the CISPR 22 Class B test limit, it is easy to see the filtering effect the stitching capacitor has on the higher frequency noise generated by the isolated transformer inside the ISOW7841 and the additional margin that can be gained by implementing it into a design.

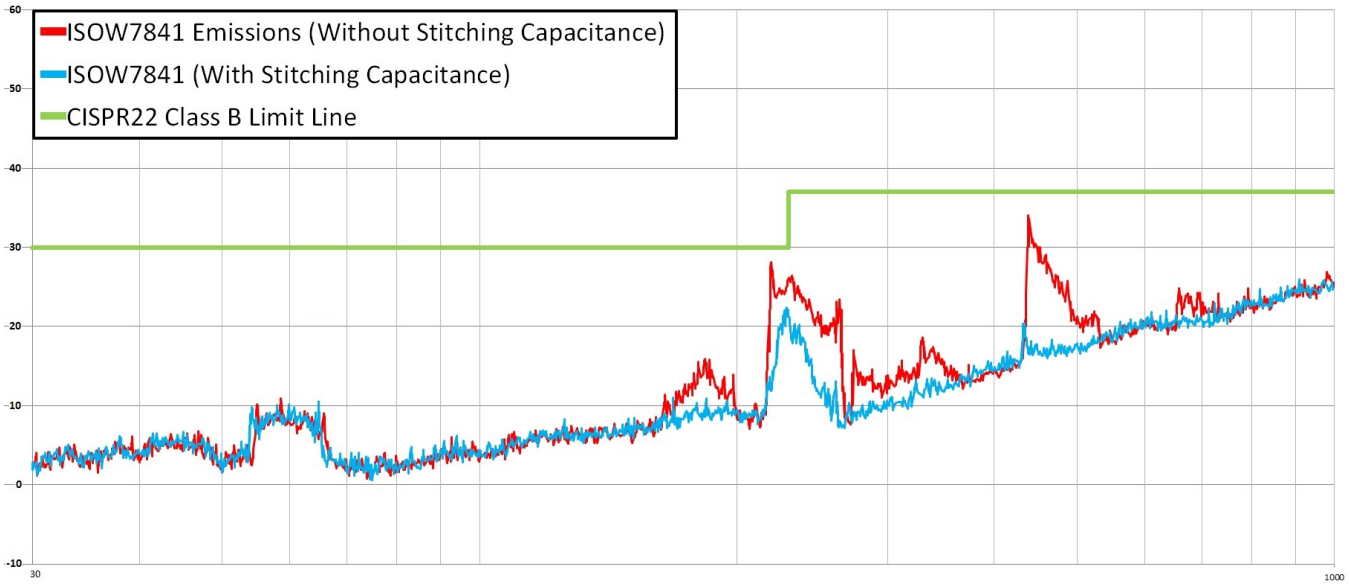


図 17. Radiated Emissions Measurements With and Without Stitching Capacitance

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-00893.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00893.

4.3 PCB Layout Recommendations

The PCB layout shown in this reference design is a good example of how to reduce radiated emissions from the integrated power transformer without adding additional cost to the BOM by creating a stitching capacitor across the isolation barrier using the PCB power and ground layers.

A capacitance of 30 pF is targeted for this reference design with isolation up to 600 V_{RMS}. Adjustments to this basic layout format can be made to accommodate different levels of isolation and capacitance using 式 1. Placing several capacitors of different values across the power and ground pins of both sides of the ISOW7841 device is also recommended as a filter for unwanted power noise being emitted into the system and for improved device performance.

This reference design also demonstrates how to improve the isolation performance during a high-voltage pulse and reduce the risk of a breakdown occurring between the planes of the PCB. It is recommended to remove 90° and sharp corners on the power and ground planes. All corners in this design have been mitered at 45° to reduce the electric field intensity at these locations during high-voltage pulses.

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-00893.

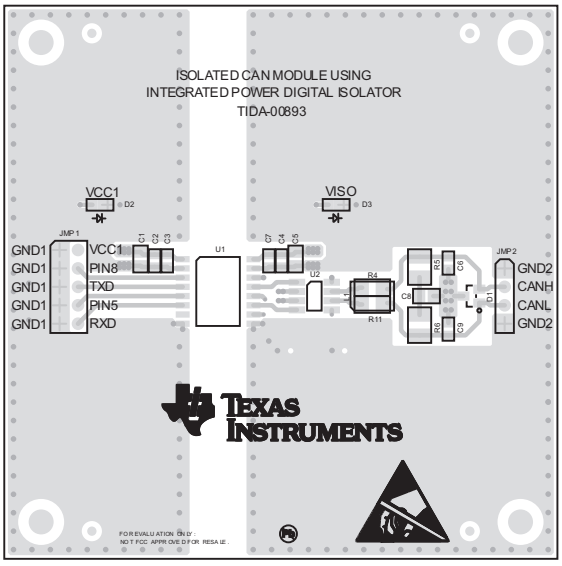


図 18. Top Layer With Silkscreen

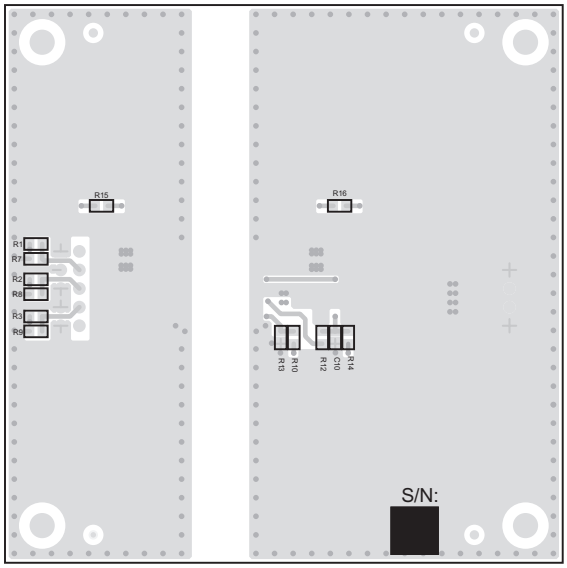


図 19. Bottom Layer With Silkscreen (as Viewed From Top)

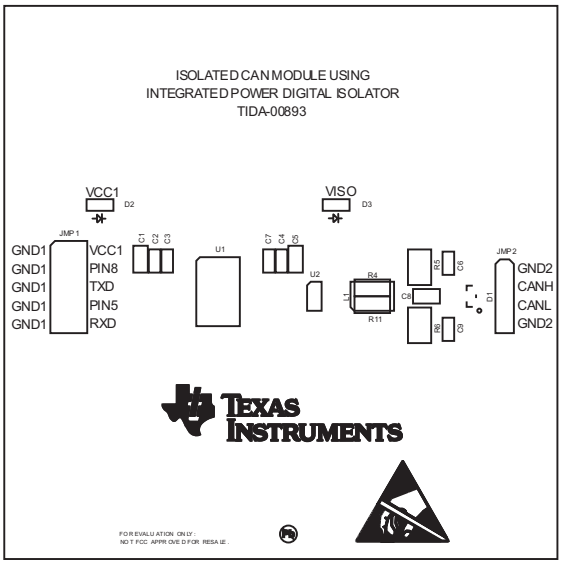


図 20. Top Layer Silkscreen

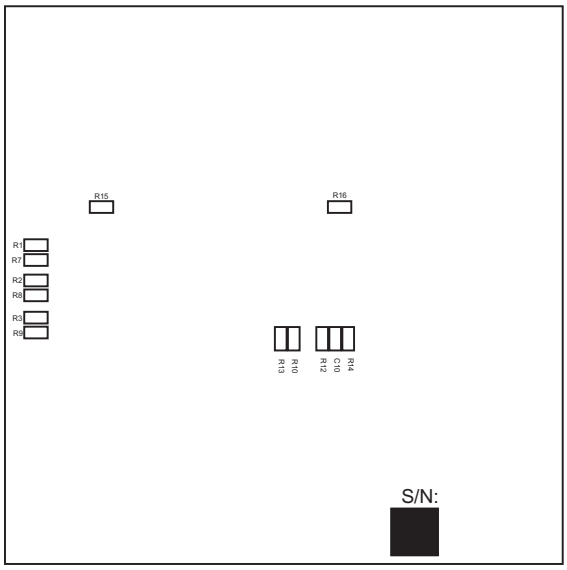


図 21. Bottom Layer Silkscreen (as Viewed From Top)

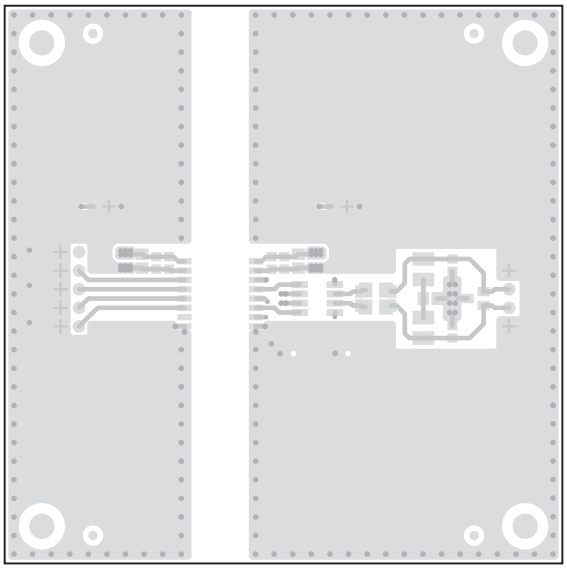


図 22. Top Layer

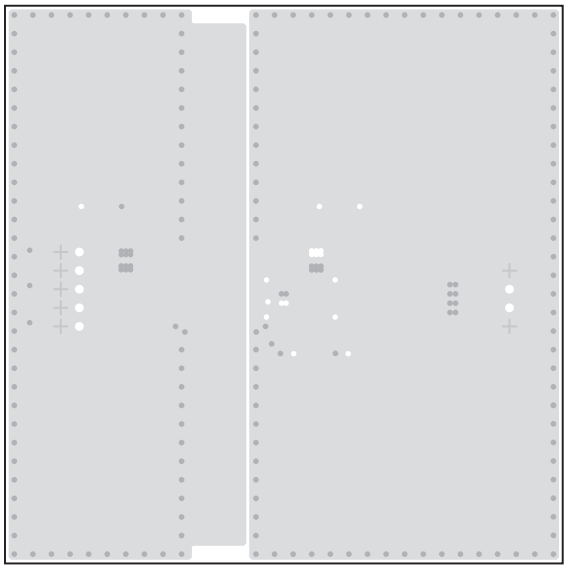


図 23. Layer 2 Ground

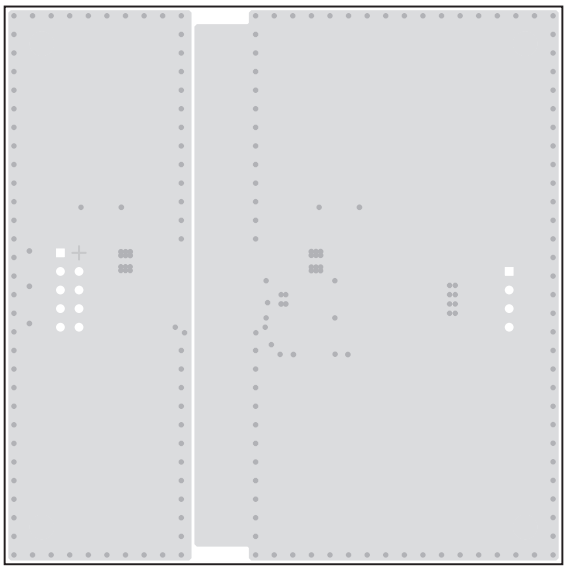


図 24. Layer 3 Power

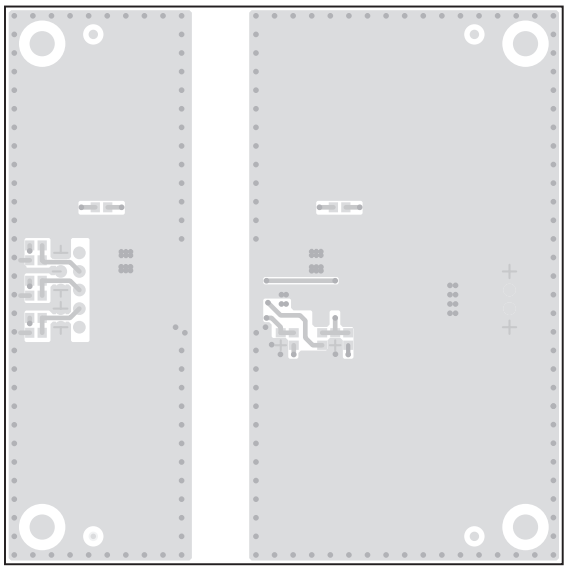


図 25. Bottom Layer
(as Viewed From Top)

4.4 Cadence Project

To download the Cadence project files, see the design files at TIDA-00893.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00893.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00893.

5 Related Documentation

1. Texas Instruments, *TCAN1042-Q1 Automotive Fault Protected CAN Transceiver with CAN FD Data Sheet*
2. Texas Instruments, *ISOW784x High-Performance, 5000-VRMS Reinforced Quad-Channel Digital Isolators With Integrated High-Efficiency, Low-Emissions DC-DC Converter Data Sheet*
3. Texas Instruments, *TIDA-00892 Isolated RS-485 With Integrated Signal and Power Reference Design*
4. Texas Instruments, *TIDA-01230 Isolated RS-232 With Integrated Signal and Power Reference Design*

5.1 商標

6 About the Author

JONATHAN NERGER is an applications engineer at Texas Instruments supporting transceiver interface products used in standards such as CAN, LIN, RS-485, RS-232, IO-Link, and I^2C. Jonathan is responsible for developing EVMs, reference design solutions, and for customer support through direct contact and creating technical content such as application notes, datasheets, white papers, and videos and silicon characterization. Jonathan brings to this role experience in other differential signaling standards such as PECL, LVDS, MLVDS, HDMI, DisplayPort, high-speed SERDES, and optical transceiver applications. Jonathan earned his bachelors of science in electrical engineering (BSEE) from Southern Methodist University (SMU).

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