Application Note

Protecting and Maintaining Signal Integrity in PLC Systems

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ABSTRACT

Electrical fast transients (EFT) are a series of high voltage, fast frequency pulses that can strike analog input and output modules in a factory automation programmable logic controller (PLC) system. EFT bursts typically come from cables surrounding PLC systems and can interrupt data or power through inductive or capacitive couplings. Because of the adverse effects introduced in harsh industrial environments, PLC systems require protection against EFT burst, and permanent miswiring. This document explains how TI's fault-protected multiplexers can be designed into a system to protect signal chain devices from harmful high-voltage signals while simultaneously allowing for continued communication between devices during burst events.

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Trademarks

1 Fault Protected Multiplexer Operation in System and Requirements for EFT Burst Testing

TI has created fault protected multiplexers which have an integrated feature called over-voltage protection (OVP). The OVP feature of these multiplexers are designed to block input signals outside the range of the positive or negative power supply of the mux. For example, looking at Figure1-1 let us assume we have a PLC system where the inputs are 24V and the power supply of the multiplexer are ±15V. In this example, the OVP feature of the TMUX7308F activates and disconnects the source input from passing the signal to protect the downstream components in a PLC system.

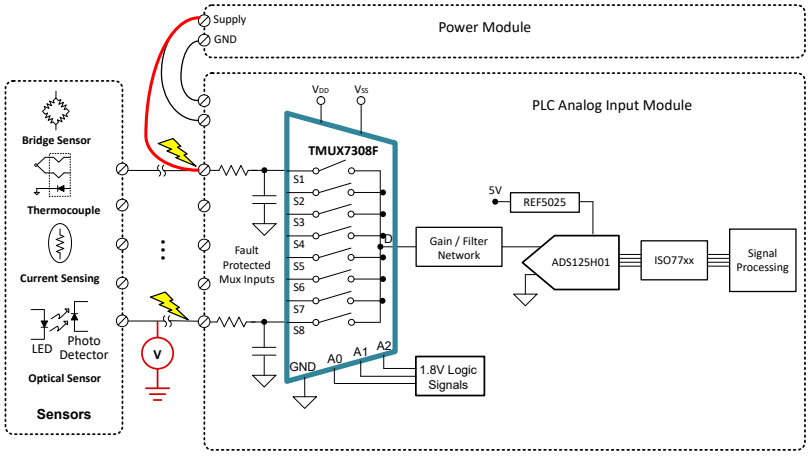

Figure 1-1. Typical Application of Fault Protected Multiplexer in PLC System

This same OVP feature can also be used to block EFT burst signals that strike communication lines between analog input and output modules in a factory automation environment. While the immediate protection of components in factory automation communication is important, the other significant detail is the need for fast recovery of communication lines during an EFT burst event. TI's Fault Protected multiplexers' fast recovery time (*trecover*), allows this family of devices to reconnect the analog signal line faster than the time between EFT burst pulses (*toff*). This maintains that the switch can quickly reconnect PLC modules allowing for accurate communication and minimal signal attenuation during an EFT burst event.

Typical characteristics of EFT burst testing including peak voltage amplitudes, test levels, burst wave shape and timing definitions, and testing repetition times are shown in the figures below (Table 1-1, Figure 1-2, and Figure 1-3).

Table 1-1. IEC61000-4-4 Test Levels for EFT Burst Testing

	Peak Amplitude			
	Power Supply Port		I/O, Signal, Data & Control Lines	
Level	V_{CC} (kV)	I_{SC} (A)	V_{CC} (kV)	I_{SC} (A)
1	0.5	10	0.25	5
2	1	20	0.5	10
3	2	40	1	20
4	4	80	2	40

The EFT pulse waveform is defined as and categorized by:

- *tr* (rise time) = *5ns*
- *tp* (pulse duration) = *50ns*

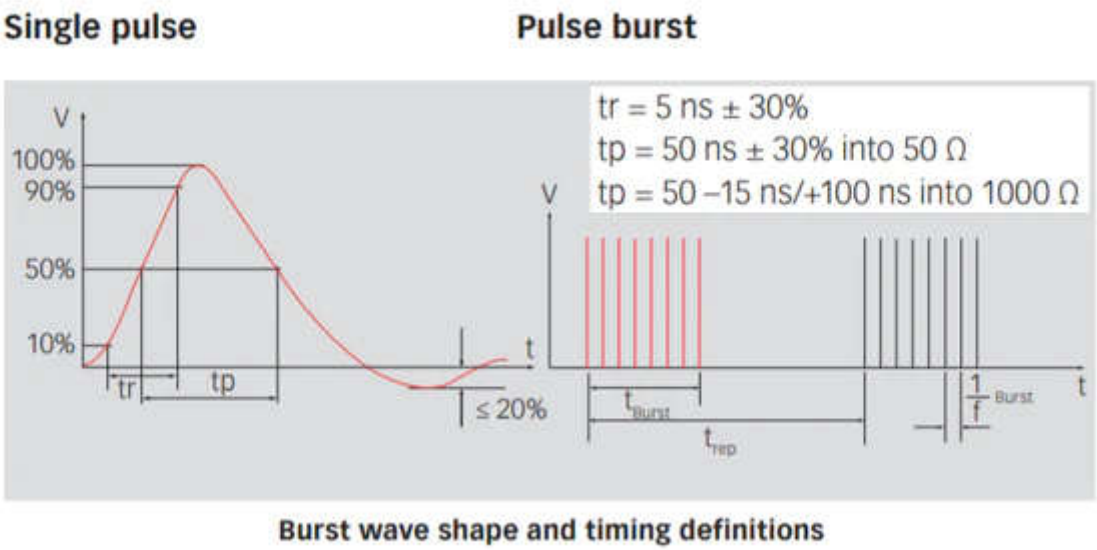

Figure 1-2. Burst Wave Shape and Timing Definitions

These short pulses are repeated 75 time with a time (*trep)* and from a specified burst package.

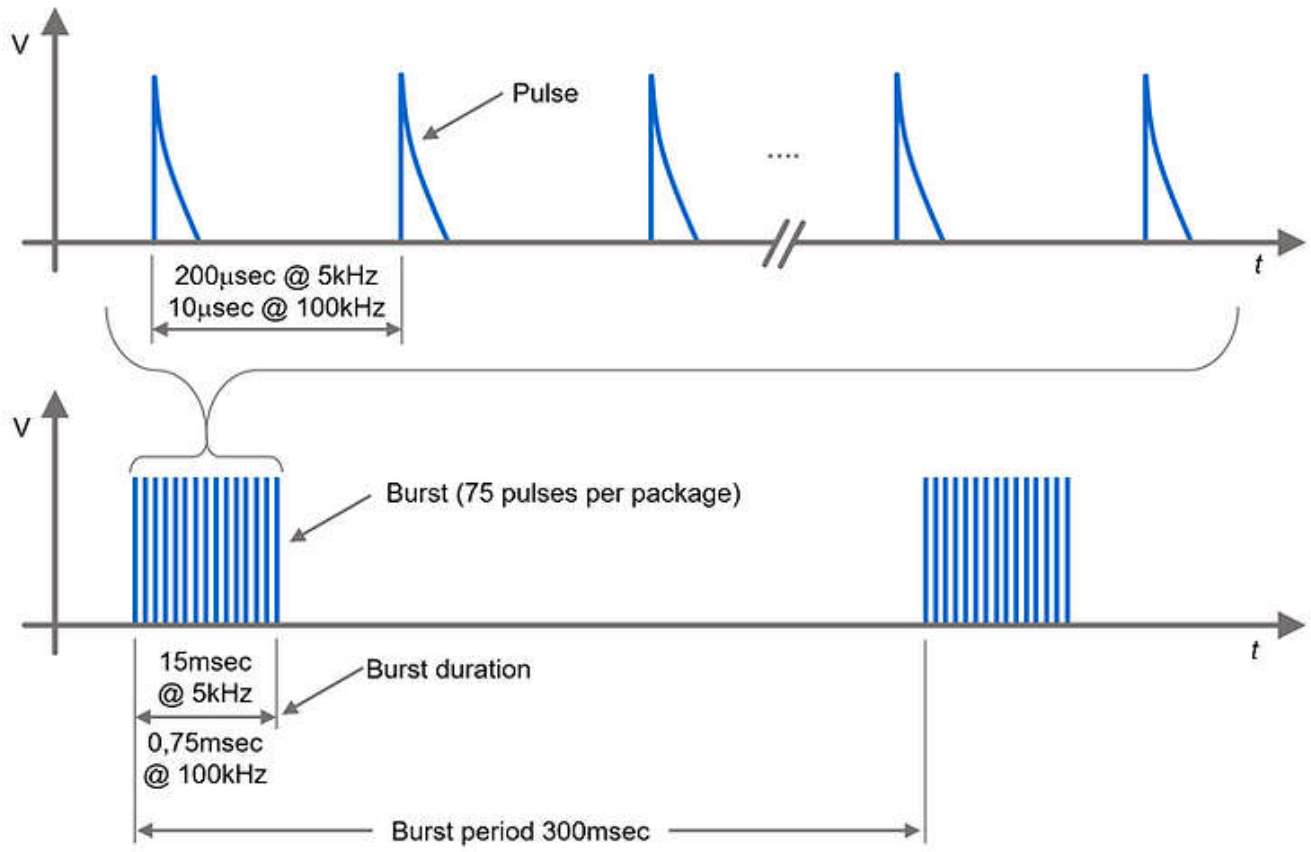

Figure 1-3. Test Repetition Times

The standard offers two repetition times, 200us (100kHz) or 10us (5kHz) within the burst packet. Each package contains 75 pulses. The resulting burst package duration is 15ms or 750us. Burst packages then repeat every 300ms. With this information, the equivalent duty cycle for both EFT burst repetition times is 0.00125%.

For EFT burst immunity testing the following four criteria are defined:

- Performance Criteria A – 'Performance within specification limits'
- Performance Criteria B – 'Temporary degradation which is self-recoverable'
- Performance Criteria C – 'Temporary degradation which requires operator intervention'
- Performance Criteria D – 'Loss of function which is not recoverable'

PLC systems must at a minimum fulfill Criteria B. Failure to meet this baseline can lead to system operators having to shut down and reset to recover acceptable PLC performance. In worst-case scenarios where no protection switch is used, operators have to completely replace permanently damaged components. To fulfill Criteria B, the signal link must not drop but can be degraded in value. For example, a voltage of 10V can be impacted and voltage can degrade by a typical industry standard percentage of 10%, but the signaling must not be lost and the link must not discharge. System self-recoverability maintains that the signal link does not drop during an EFT burst and only lead to temporary degradation. This is the requirement for Criteria B performance.

2 System Level Protection Explanation and Design Based on Fast Fault Recovery Time

To help system designers combat failure due to EFT burst and permanent miswiring, we outline considerations that are important in PLC communication design. First, PLC inputs and outputs are typically protected using TVS diodes either discrete ones or flat clamp diodes like TVS3301. These TVS diodes already clamp the very high burst transients. While TVS diodes can withstand bursts in the kV range, electronic components can not.

On the other hand, electronic circuits for PLC systems must be able to withstand permanent EFT burst pulses and permanent miswiring from external voltage sources. As TVS diodes are conducting under over-voltage conditions, they cannot handle a permanent over-voltage/under-voltage (OV/UV) condition. For analog output or current inputs where higher currents can flow, using a TVS diode with no protection switch introduces a challenge. For example, while burst clamping TVS diodes can trigger at a higher voltage like 36V, a permanent 24V DC into the output can potentially destroy PLC system electronics. A system designer can place a clamping diode that can clamp around 15V to protect a +/-15V supplied output. In case of a 24V miswiring the diode permanently conducts and shunts all the current the supply can deliver. This causes the diode to dissipate a huge amount of energy and eventually be destroyed. Introducing a protection switch solves this problem because the permanent DC miswiring voltage is blocked.

TVS diodes also must not impact analog signals with their leakage currents. This means the clamping voltage must be selected such that they are transparent to the signal and do not conduct within the OVP protection rating of a switch but clamp above this level to protect from burst. This defines the need for a protection switch that can handle permanent EFT burst pulses and can block permanent DC OV/UV conditions following TVS diodes.

Finally, to help maintain signal integrity during EFT burst, designers must select a protection switch with the proper fault recovery time. If the fault recovery time (*trecover)* of the protection switch on the signal link line exceeds the off-time (*toff)* between two pulses within a burst packet, then the system fails Criteria B which means the link discharges and the signal is lost (Figure 2-1). For EFT burst testing the time between two pulses within a burst packet are 10us or 200us depending on the selected repetition time.

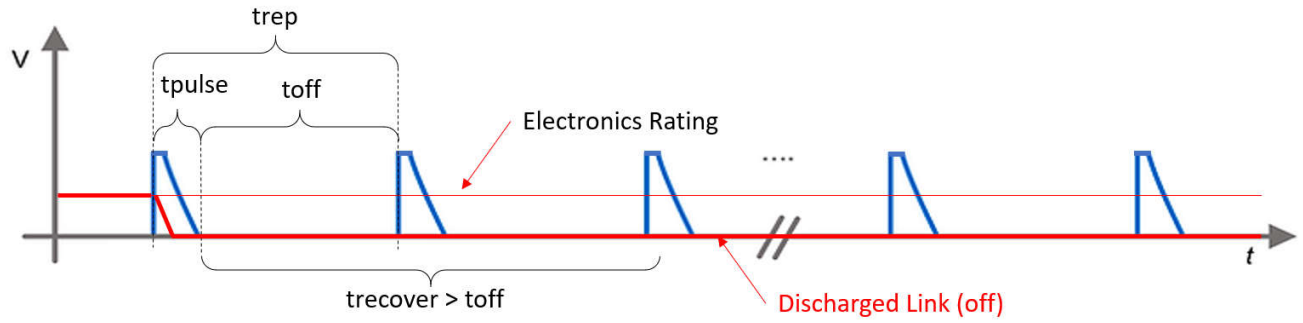

Figure 2-1. Link Discharged During Burst Testing With Too Long Recovery Time

To solve this problem, use a TI Fault Protected Multiplexer which has a fast-enough recovery time such that the link can be recharged between EFT pulses. TI Fault Protected Multiplexers have fault recovery times ranging from 1.1us to 1.6us at a +/-15V supply (Figure 2-2).

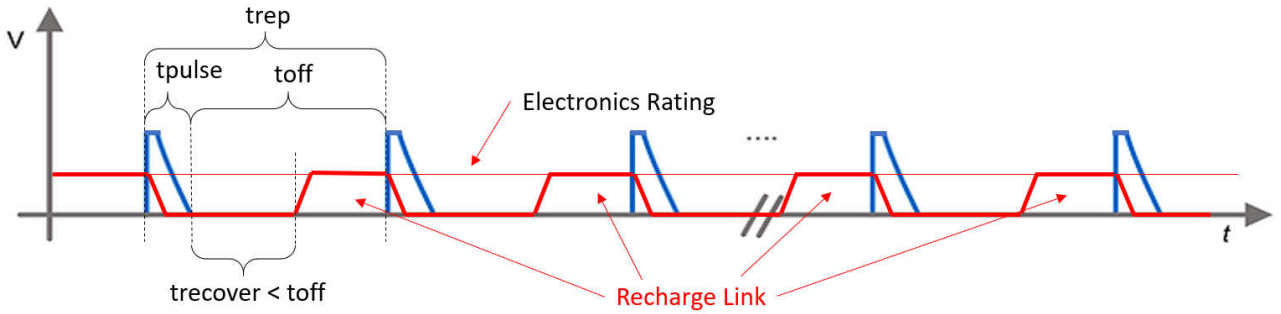

Figure 2-2. Link Recharged During Burst Testing Fulfilling EFT Burst Test Criterion B

To see the expected results, we can also take a look at the Tina-TI model (Figure 2-3). This model represents a PLC communication system where a 10V signal is produced from the OPA990, sent through the Output Protector switch and then finally passed through the receiver also known as an analog output module. In addition, the burst generator is sending a 0 to 20V, 100kHz standard EFT pulse onto the signal line modeling a clamped pulse. The Output Protector has a fault recovery time of 2us.

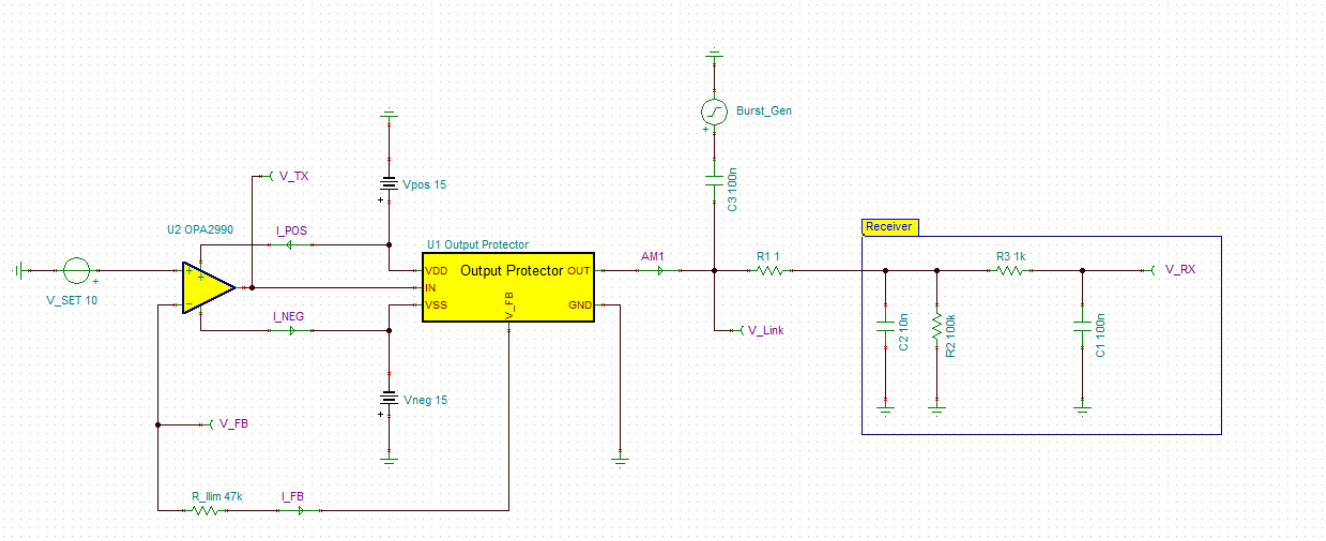

Figure 2-3. Tina-TI Model

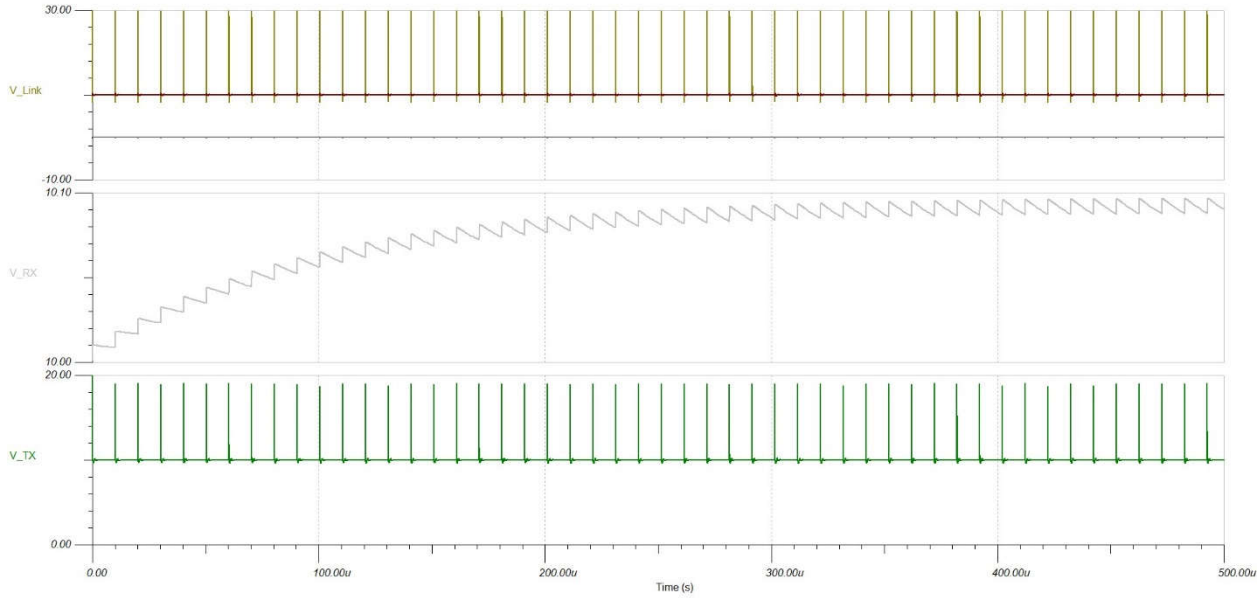

Figure 2-4. Tina-TI Model Results

V_Link shows the burst pulse on top of the signal. V_TX is the output of the amplifier and V_RX is the analog output module. Looking at Figure 2-4, we can expect the fault-protected switch to reconnect the signal line between EFT pulses and the offset voltage error on the output is 100mV. A small voltage error of less than 100mV added to the 10V signal line link is what we expect when testing TI's fault-protected devices with standard EFT pulses.

3 System Level Lab Test Procedure and Results of EFT Burst Testing

In this lab experiment a 5kHz, 5% duty cycle signal was sent onto the line as a simulated EFT burst. Due to lab waveform generator limitations, this test only looks at protection from voltages that are produced after the clamping of a TVS diode on the signal line. While no TVS diode was used during this experiment, note that any clamped voltage within the fault protected multiplexer's acceptable input range (± 60V) is blocked by the devices OVP feature and provide protection from EFT burst. Other limitations include, passive components being chosen based on availability during testing and the ac cap replacing capacitive coupling that happens when a burst pulse is sent onto the shield of a wire in a PLC communication system.

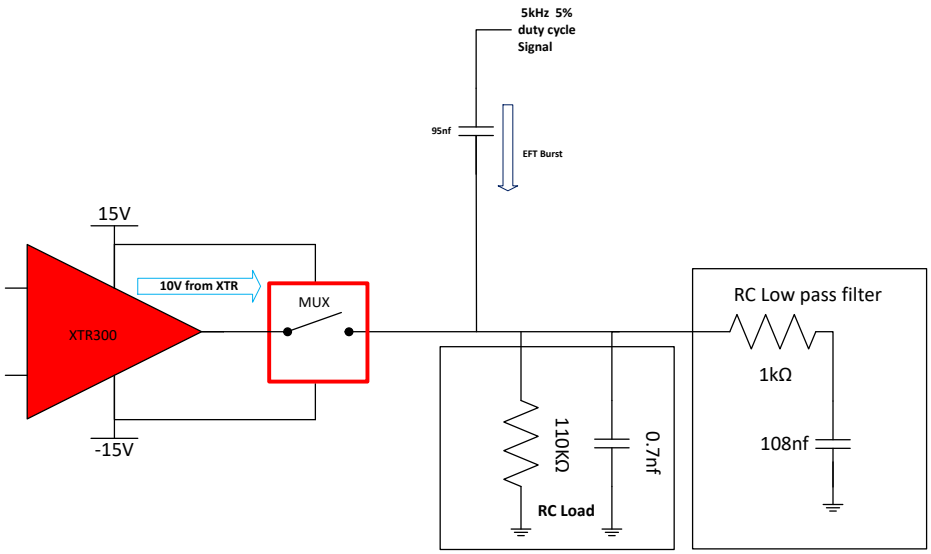

Figure 3-1. EFT Burst Test Setup

Figure 3-1 shows the setup for this EFT burst test using a XTR300 amplifier in Vout mode sending 10v down the analog signal line. First, the RC load provides stability to the amplifier and maintains the 10V signal on the line during the switching of the mux. The RC load represents part of an analog output module.

The switch can recover faster than the time between EFT burst pulses which stops the link from discharging. If this device's fault recovery time was longer than the time between pulses, then the switch stays open circuit and never reconnect the signal line leading to the loss of voltage on the signal link line. This causes failure in communication between the analog input and output modules.

Typical PLC system RC loads range from 1nf-10nf and 100kΩ - 1MΩ. As a result, we can see that systems RC time constants range from 100us to 10,000us. These time constants represent how much time the signal link takes to discharge. This means the switch can recover faster and recharge the signal before the signal can discharge on the line, leading to a consistent 10v signal link that sees little to no degradation during EFT burst.

The next part of the analog output module is the low pass filter which serves the purpose of protecting/smoothing out the EFT burst signal before reaching the ADC input. This low pass filter is another important part of the PLC protection scheme and can be designed directly or can be found integrated inside some ADCs. The expected behavior is that the link is not interrupted and the values on the line are allowed to change within specified ranges provided by the system designers. Figure 3-2 shows the EFT burst test setup with probe locations. This is important so we can understand the behavior of the system with TI's fault protected multiplexers.

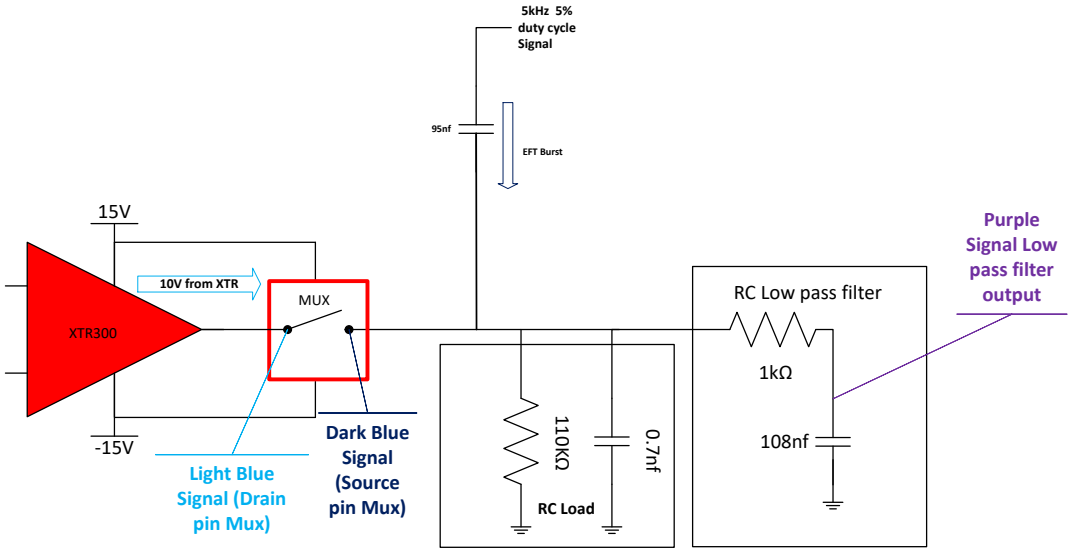

Figure 3-2. EFT Burst Test Setup With Probe Locations

The following screenshots below show waveforms for the EFT burst test. Looking at the TMUX7462F images (Figure 3-3 and Figure 3-4) we can see that the fault protected multiplexer is operating as intended and reconnecting the signal line quickly between burst pulses leading to a continuous 10v signal being sent from the drain pin of the mux to the low pass filter. The difference between the light blue and purple line is called the offset voltage and is a result of the EFT burst being smoothed out by the low pass filter.

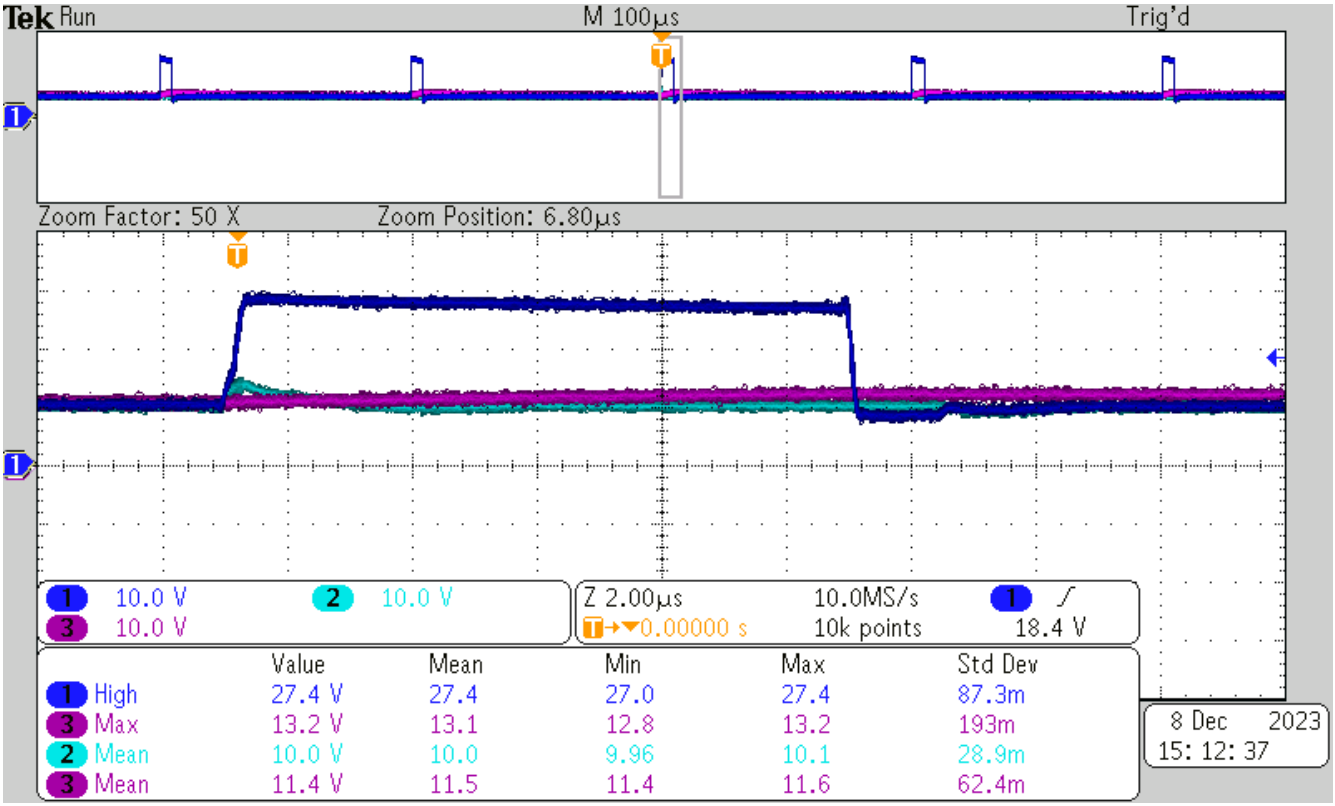

Figure 3-3. 5kHz Simulated EFT Burst Test TMUX7462F Zoomed In

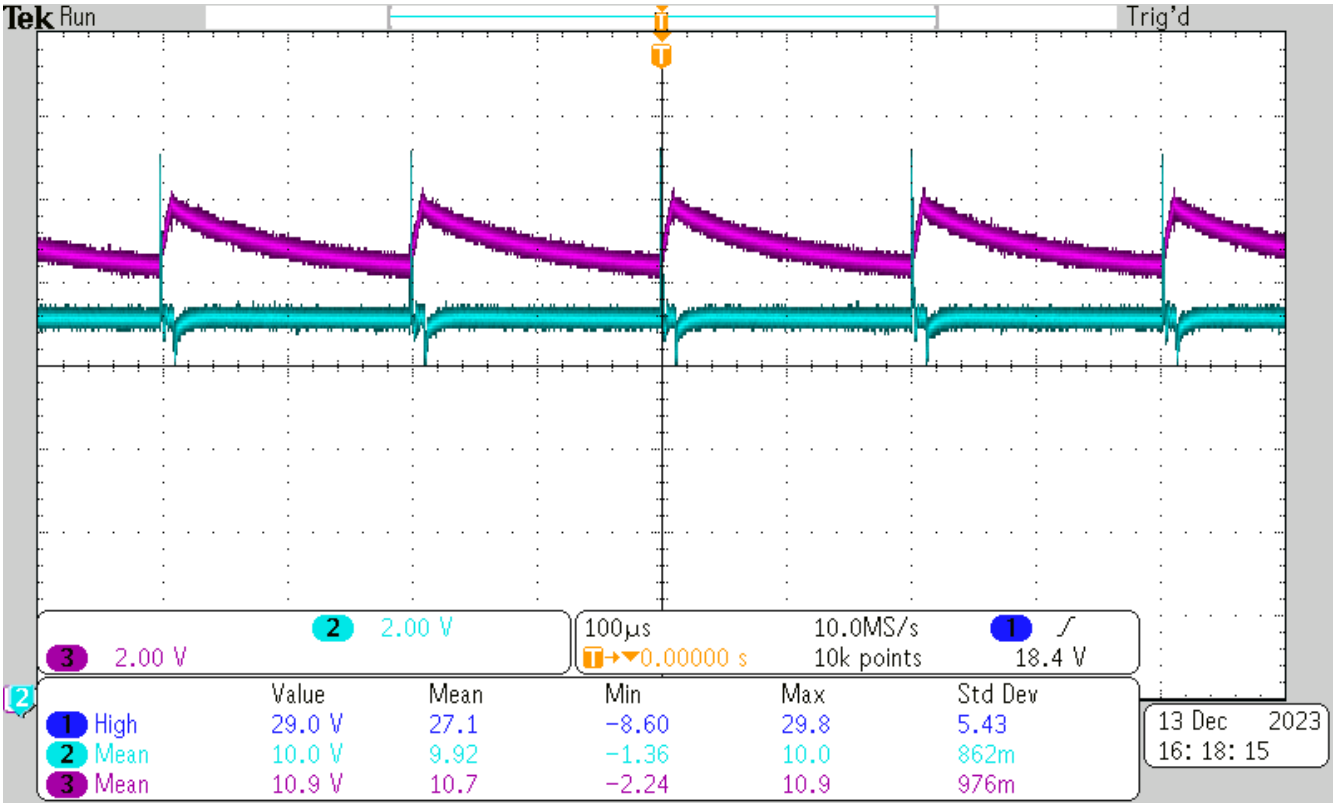

Figure 3-4. TMUX7462F Zoomed Out

When looking at the TMUX7309F (Figure 3-5 and Figure 3-6) we can also see how the system behaves as expected and reconnects the signal link quickly between burst pulses leading to a continuous uninterrupted communication. The offset voltage error during the TMUX7309F test is similar to the TMUX7462F test. Note that when the EFT burst testing is done, both devices pass the amplifier signal from drain to source with no interruption.

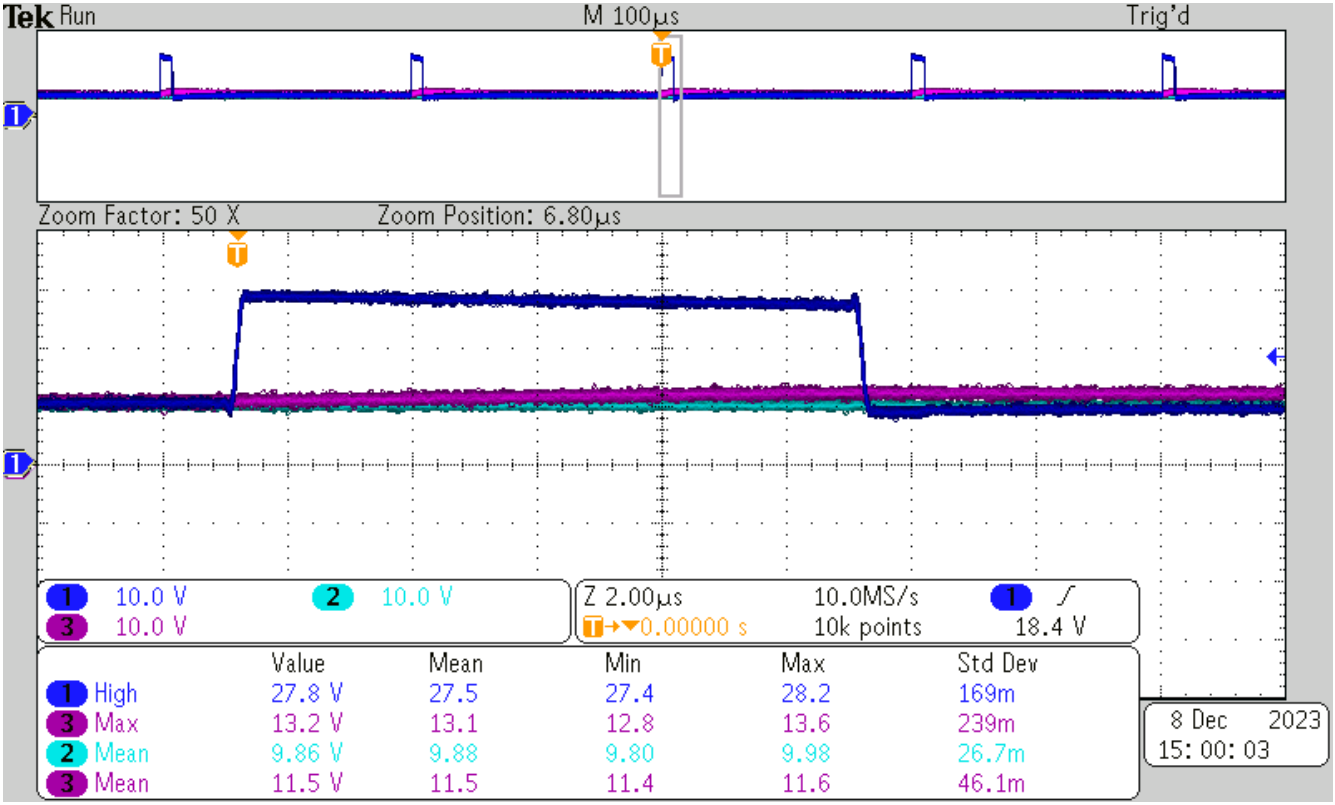

Figure 3-5. 5kHz Simulated EFT Burst Test TMUX7309F Zoomed In

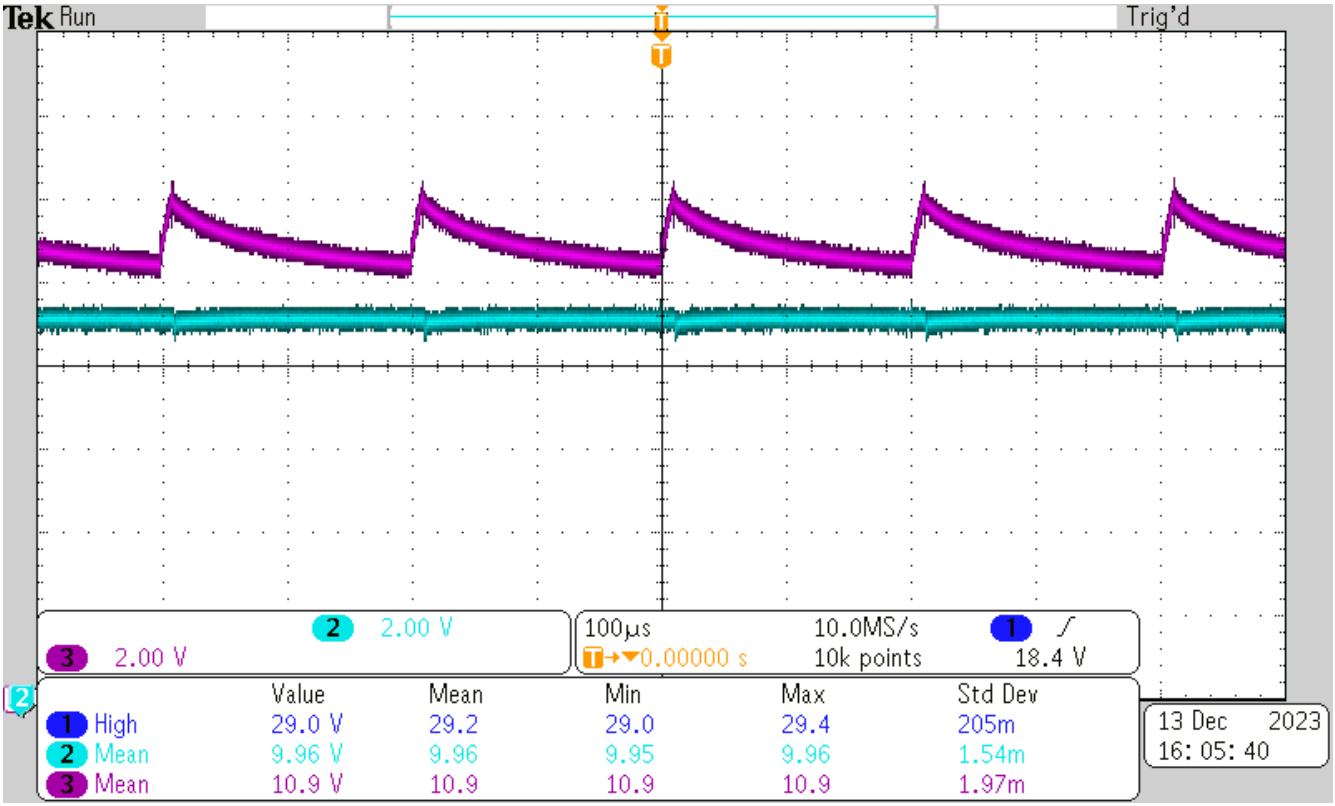

Figure 3-6. TMUX7309F Zoomed Out

Table 3-1 shows more information on the offset voltage for both system setups.

Table 3-1. Offset Voltage Error Table

	TMUX7309F	TMUX7462F
Burst Test Offset Measurements(5kHz)	0.94V	0.9V

In addition, Figure 3-7 shows a 100kHz simulated EFT burst test being performed on the TMUX7462F. Note that this test has the same setup and probe locations as the previous 5kHz test. Due to both tests having the same duty cycles, the error is very similar. This zoomed in picture shows when the switch reconnects and brings the link back to regulation after about 5us.

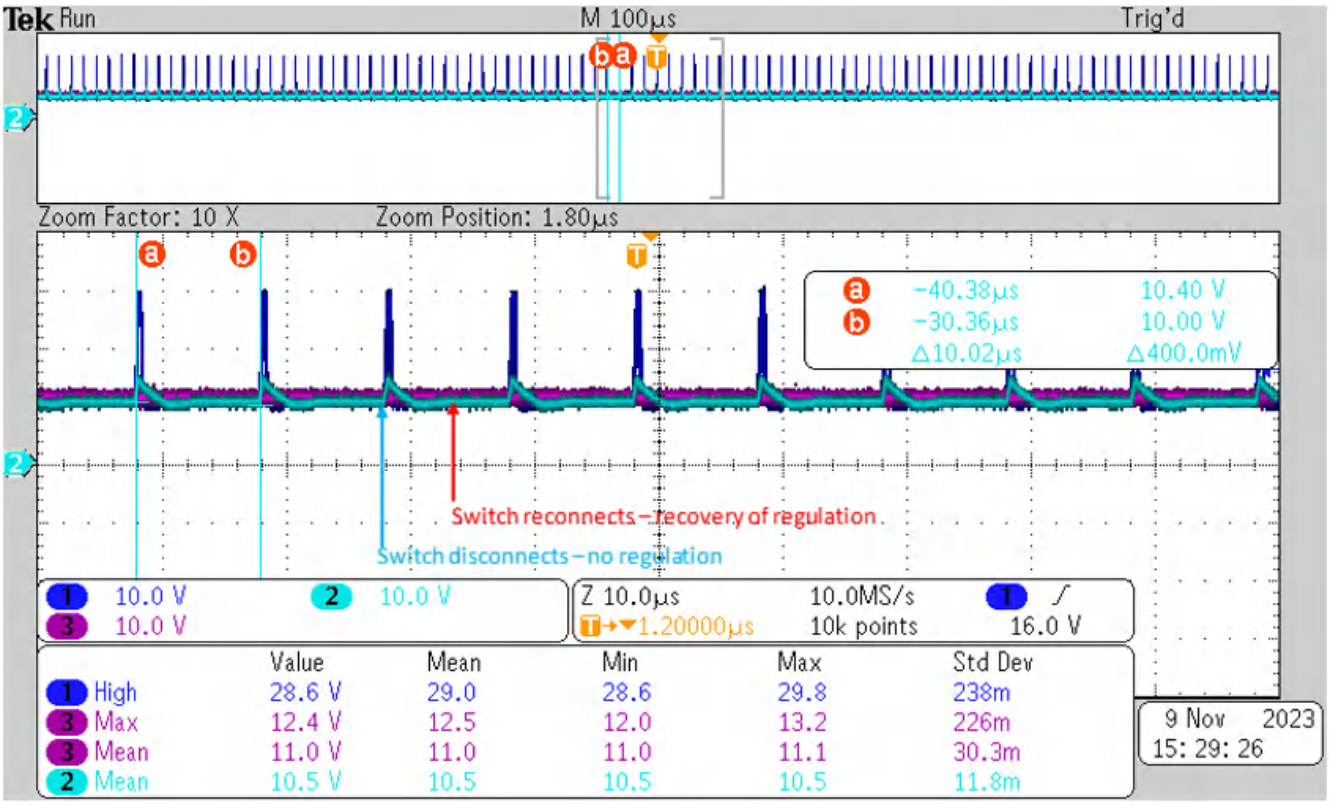

Figure 3-7. 100kHz Simulated EFT Burst Test TMUX7462F

Finally, the offset voltage (the difference between the light blue and purple line) comes from the EFT burst signal injecting energy on the line that shows as an added DC value even after the low pass filter. The expected offset voltage is based on the duty cycle of the EFT burst signal put onto the signal lines.

To understand why there is offset voltage and how that voltage is smaller with a standard EFT burst profile, we can look at the following example. If we send a 0 to 18v and 5% duty cycle signal onto the 10V signal line to simulate an EFT burst, we see approximately 0.9V (18*0.05) added onto the line and show up as an error on the analog output or output of low pass filter. To see what the injected voltage is going to be on the line during an EFT burst test with a standard burst profile, please follow the method below.

- First, find the duty cycle of the EFT Burst signals (Figure 1-2 and Figure 1-3).
  - Time between pulses (TP) = 10us for 100kHz EFT burst or 200us for 5kHz EFT burst test and Pulse Duration (*tp*)= 50ns
- Next, find the duty cycle of the EFT Burst signals when sent in the burst packets as outlined in (Figure 1-3) Test Repetition Times.
  - Duty cycle of EFT Burst = 50ns/10us = 0.5% and Burst Packet Duty cycle = 0.75ms/300ms = 0.25% (100kHz test)
  - Duty cycle of EFT Burst = 50ns/200us = 0.025% and Burst Packet Duty cycle = 15ms/300ms = 5% (5kHz test)
- Finally, multiply the different duty cycles to see what error can be introduced with a standard EFT Burst profile.
  - Duty Cycles of standard EFT Burst signal
  - 100kHz test = 0.5% * 0.25% = 0.00125%
  - 5kHz test = 0.025% * 5% = 0.00125%

So, a system designer can expect to see (18 x 0.00125% = 0.000225 volts) or 0.225mV added on the 10V signal line if 18V is the peak voltage of EFT burst signal. If we compare that error to what is typically acceptable for

customer designs, which is 1-2%, then we can see that 0.225mV provides even better performance than the customer allowable error of 100-200mv.

Note that the fault protected multiplexers do not introduce the offset error themselves and PLC communication systems in this report falls into Performance Criteria A *'Performance within specification limits'* as the added EFT Burst signal error is acceptable for the customer application.

4 Conclusion

Electrical fast transients (EFT) are a series of high voltage, fast frequency pulses that can strike analog input and output modules in factory automation programmable logic controller (PLC) systems. These burst, if not properly accounted for in system design, can cause issues with signal accuracy and potential permanent damage to components. To solve this problem TI has created fault protected multiplexers which have a feature called over voltage protection (OVP) that activates when voltages higher than supply are sent to the input pins. While protecting the signal chain components is important, the additional fast recovery time of TI's fault protected multiplexers allow for accurate communication between PLC modules. This intern leads to system designers being able to generate Performance Criteria A based on EFT Burst test standards. For more information on fault protected multiplexers with fast recovery times please look at Table 4-1.

Table 4-1. TI's Fault Protected Multiplexers for PLC Applications

Device	Configuration	Fault Recovery time at ±15V Supply
TMUX7308F	8:1 x 1	1.2us
TMUX7309F	4:1 x 2	1.2us
TMUX7348F	8:1 x 1	1.4us
TMUX7349F	4:1 x 2	1.4us
TMUX7411F	1:1 x 4	1.6us
TMUX7412F	1:1 x 4	1.6us
TMUX7413F	1:1 x 4	1.6us
TMUX7436F	2:1 x2	1.6us
TMUX7462F	1:1 x2	1.1us

5 References

- Texas Instruments, *Replace Discrete Protection and Optimize Your PLC System Protection*
- Texas Instruments, *Protection Against Overvoltage Events, Miswiring, and Common Mode Voltages*
- Texas Instrument, *Protecting against Overvoltage Events in PLC AIO modules*

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